FlexiForce® Sensors
User Manual

FlexiForce® Sensors User Manual

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Table of Contents

WELCOME

ISO

Tekscan is registered to the following standard(s):

- ISO 9001: 2000
- ISO 13485: 2003

INTRODUCTION

This manual describes how to use Tekscan's ***FlexiForce Sensors***. These sensors are ideal for designers, researchers, or anyone who needs to measure forces without disturbing the dynamics of their tests. The ***FlexiForce*** sensors can be used to measure both static and dynamic forces (up to 1000 lbf.), and are thin enough to enable non-intrusive measurement.

The ***FlexiForce*** sensors use a resistive-based technology. The application of a force to the active sensing area of the sensor results in a change in the resistance of the sensing element in inverse proportion to the force applied.

GETTING ASSISTANCE

Tekscan, Inc. will provide technical assistance for any difficulties you may experience using your ***FlexiForce*** system.

Write, call or fax us with any concerns or questions. Our knowledgeable support staff will be happy to help you. Comments and suggestions are always welcome.

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OVERVIEW

This section outlines Sensor Construction and Application.

FLEXIFORCE SENSORS

The ***FlexiForce*** sensor is an ultra-thin and flexible printed circuit, which can be easily integrated into most applications. With its paper-thin construction, flexibility and force measurement ability, the ***FlexiForce*** force sensor can measure force between almost any two surfaces and is durable enough to stand up to most environments. ***FlexiForce*** has better force sensing properties, linearity, hysteresis, drift, and temperature sensitivity than any other thin-film force sensors. The "active sensing area" is a 0.375" diameter circle at the end of the sensor.

The sensors are constructed of two layers of substrate. This substrate is composed of polyester film (or Polyimide in the case of the High-Temperature Sensors). On each layer, a conductive material (silver) is applied, followed by a layer of pressure-sensitive ink. Adhesive is then used to laminate the two layers of substrate together to form the sensor. The silver circle on top of the pressure-sensitive ink defines the "active sensing area." Silver extends from the sensing area to the connectors at the other end of the sensor, forming the conductive leads.

FlexiForce sensors are terminated with a solderable male square pin connector, which allows them to be incorporated into a circuit. The two outer pins of the connector are active and the center pin is inactive. The length of the sensors can be trimmed by ***Tekscan*** to predefined lengths of 2", 4" and 6" or can be trimmed by the customer. If the customer trims the sensor, a new connector must be attached. This can be accomplished by purchasing staked pin connectors and a crimping tool. A conductive epoxy can also be used to adhere small wires to each conductor.

The sensor acts as a variable resistor in an electrical circuit. When the sensor is unloaded, its resistance is very high (greater than 5 Meg-ohm); when a force is applied to the sensor, the resistance decreases. Connecting an ohmmeter to the outer two pins of the sensor connector and applying a force to the sensing area can read the change in resistance.

Sensors should be stored at temperatures in the range of 15°F (-9°C) to 165°F (74°C)

Standard FlexiForce Sensors

The Standard A201 sensor is available in the following force ranges:

- Sensor A201-1 (0-1 lb. force range)
- Sensor A201-25 (0-25 lb. force range)
- Sensor A201-100 (0-100 lb. force range)*

**** In order to measure forces above 100 lbs. (up to 1000 lbs), apply a lower drive voltage and reduce the resistance of the feedback resistor (1kΩ min.). See the <u>sample drive circuit</u> below.***

High-Temperature FlexiForce Sensors

The High-Temperature HT201 sensor is available in the following force ranges* (as tested with the sample drive circuit).

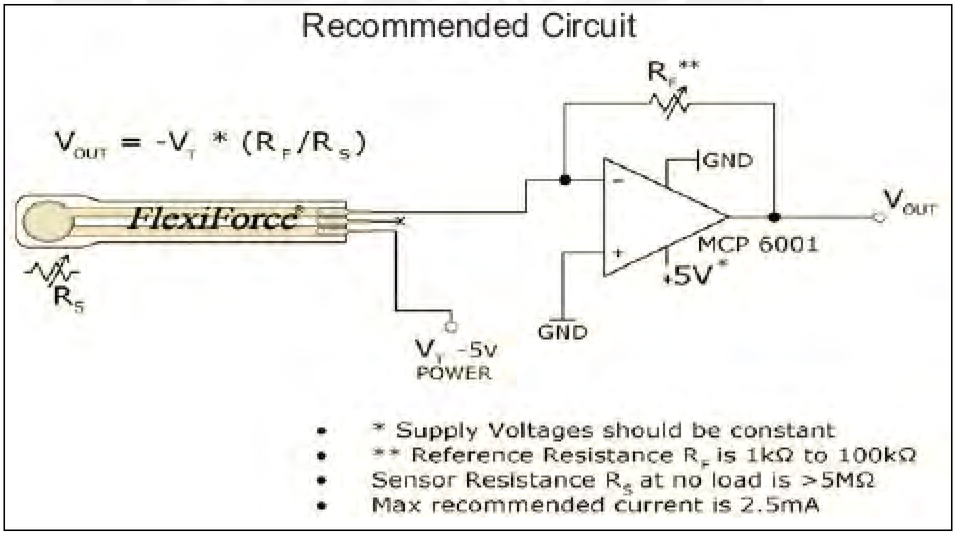
- Sensor HT201-L Low: 0-30lb (133N) force range
- Sensor HT201-H High: 0-100lb (445N) force range

**** In order to measure forces outside specified ranges, use recommended circuit and adjust drive voltage and/or reference resistance***

APPLICATION

There are many ways to integrate the ***FlexiForce*** sensor into an application. One way is to incorporate it into a force-to-voltage circuit. A means of calibration must then be established to convert the output into the appropriate engineering units. Depending on the setup, an adjustment could then be done to increase or decrease the sensitivity of the sensor.

An example circuit is shown below. In this case, it is driven by a -5 V DC excitation voltage. This circuit uses an inverting operational amplifier arrangement to produce an analog output based on the sensor resistance and a fixed reference resistance (R_F). An analog-to-digital converter can be used to change this voltage to a digital output. In this circuit, the sensitivity of the sensor could be adjusted by changing the reference resistance (R_F) and/or drive voltage (VT); a lower reference resistance and/or drive voltage will make the sensor less sensitive, and increase its active force range.



In the circuit shown, the dynamic force range of the sensor can be adjusted by changing the reference resistor (R_F) or by changing the Drive Voltage (V_O). Refer to the Saturation section for additional information.

SENSOR LOADING CONSIDERATIONS

The following general sensor loading guidelines can be applied to most applications, and will help you achieve the most accurate results from your tests. It is important that you read the ***Sensor Performance Characteristics*** section for further information on how to get the most accurate results from your sensor readings.

SENSOR LOADING

The entire sensing area of the ***FlexiForce*** sensor is treated as a single contact point. For this reason, the applied load should be distributed evenly across the sensing area to ensure accurate and repeatable force readings. Readings may vary slightly if the load distribution changes over the sensing area.

Note that the sensing area is the silver circle on the top of the sensor only.

It is also important that the sensor be loaded consistently, or in the same way each time.

If the footprint of the applied load is smaller than the sensing area, the load should not be placed near the edges of the sensing area, to ensure an even load distribution.

It is also important to ensure that the sensing area is the entire load path, and that the load is not supported by the area outside of the sensing area.

If the footprint of the applied load is larger than the sensing area, it may be necessary to use a "puck." A puck is a piece of rigid material (smaller than the sensing area) that is placed on the sensing area to ensure that the entire load path goes through this area. The puck must not touch any of the edges of the sensing area, or these edges may support some of the load and give an erroneous reading.

The ***FlexiForce*** sensor reads forces that are perpendicular to the sensor plane. Applications that impart "shear" forces could reduce the life of the sensor. If the application will place a "shear" force on the sensor, it should be protected by covering it with a more resilient material.

If it is necessary to mount the sensor to a surface, it is recommended that you use tape, when possible. Adhesives may also be used, but make sure that the adhesive will not degrade the substrate (polyester) material of the sensor before using it in an application. Adhesives should not be applied to the sensing area; however, if it is necessary, ensure that the adhesive is spread evenly. Otherwise, any high spots may appear as load on the sensor.

SATURATION

The **Saturation** force is the point at which the device output no longer varies with applied force. The saturation force of each sensor is based on the maximum recommended force specified by Tekscan, which is printed on the system packaging or the actual sensor, along with the "Sensitivity."

The saturation value is based on using the circuit and the values shown in the example circuit in the 'Application' section. In this example, the saturation force (maximum force) of each sensor is related to the RF (reference resistance), and can be altered by changing the sensitivity. The sensitivity of the sensor would be adjusted by changing the reference resistance (RF); a lower reference resistance will make the system less sensitive, and increase its active force range.

It is essential that the sensor(s) do not become saturated during testing.

CONDITIONING SENSORS

Exercising, or **Conditioning** a sensor before calibration and testing is essential in achieving accurate results. It helps to lessen the effects of *drift* and *hysteresis*. Conditioning is required for new sensors, and for sensors that have not been used for a length of time.

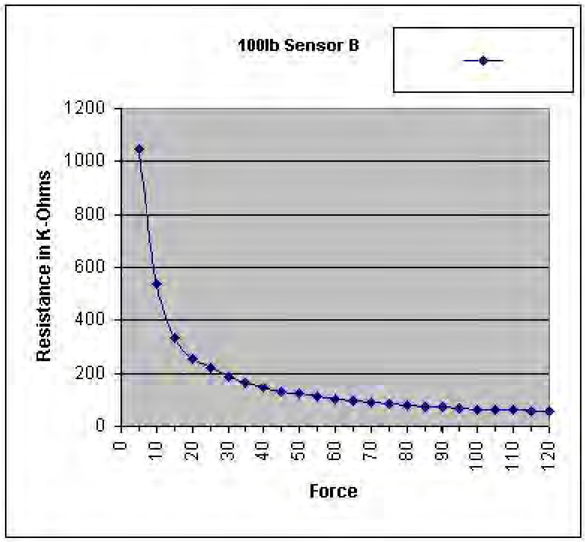
To condition a sensor, place 110% of the test weight on the sensor, allow the sensor to stabilize, and then remove the weight. Repeat this process four or five times. The interface between the sensor and the test subject material should be the same during conditioning as during calibration and actual testing.

IMPORTANT! Sensors must be properly conditioned prior to calibration and use.

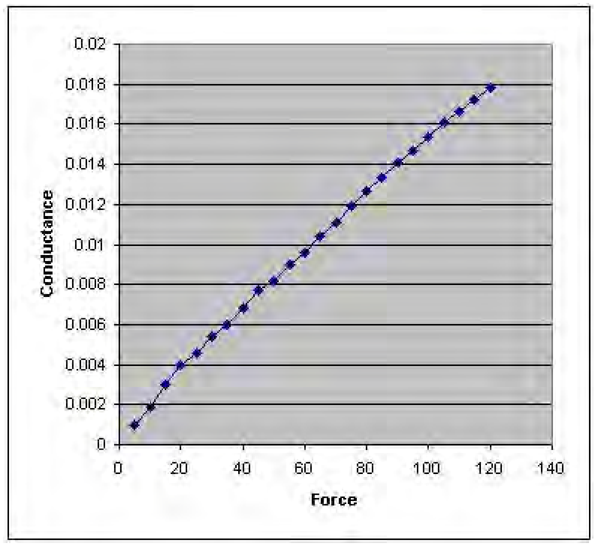
CALIBRATION

Calibration is the method by which the sensor's electrical output is related to an actual engineering unit, such as pounds or Newtons. To calibrate, apply a known force to the sensor, and equate the sensor resistance output to this force. Repeat this step with a number of known forces that approximate the load range to be used in testing. Plot **Force** versus **Conductance (1/R)**. A linear interpolation can then be done between zero load and the known calibration loads, to determine the actual force range that matches the sensor output range.

Resistance Curve:



Conductance Curve:



CALIBRATION GUIDELINES

The following guidelines should be considered when calibrating a sensor:

- Apply a calibration load that approximates the load to be applied during system use, using dead weights or a testing device (such as an ***MTS*** or ***Instron***). If you intend to use a "puck" during testing, also use it when calibrating the sensor. See Sensor Loading Considerations for more information on using a puck.
- Avoid loading the sensor to near saturation when calibrating. If the sensor saturates at a lower load than desired, adjust the "Sensitivity."
- Distribute the applied load evenly across the sensing area to ensure accurate force readings. Readings may vary slightly if the load distribution changes over the sensing area.
- Sensors should be calibrated at the same temperature for which testing will occur. This is especially important for High-Temp Sensors, as these sensors have a wide operating temperature range. If multiple temperatures are used during testing, calibrate the sensors at those same multiple temperatures.

Note: Read the Sensor Performance Characteristics section before performing a Calibration.

SENSOR PERFORMANCE CHARACTERISTICS

There are a number of characteristics of sensors, which can affect your results. This section contains a description of each of these conditions, and recommendations on how to lessen their effects.

REPEATABILITY

Repeatability is the ability of the sensor to respond in the same way to a repeatedly applied force. As with most measurement devices, it is customary to exercise, or "condition" a sensor before calibrating it or using it for measurement. This is done to reduce the amount of change in the sensor response due to repeated loading and unloading. A sensor is conditioned by loading it to 110% of the test weight four or five times. Follow the full procedure in the **Conditioning Sensors** section.

LINEARITY

Linearity refers to the sensor's response (digital output) to the applied load, over the range of the sensor. This response should ideally be linear; and any non-linearity of the sensor is the amount that its output deviates from this line. A calibration is performed to "linearize" this output as much as possible. ***FlexiForce*** standard sensors are linear within +/- 3%. ***FlexiForce*** High-Temperature sensors have a linearity that is 1.2% of full scale.

HYSTERESIS

Hysteresis is the difference in the sensor output response during loading and unloading, at the same force. For static forces, and applications in which force is only increased, and not decreased, the effects of hysteresis are minimal. If an application includes load decreases, as well as increases, there may be error introduced by hysteresis that is not accounted for by calibration.

DRIFT

Drift is the change in sensor output when a constant force is applied over a period of time. If the sensor is kept under a constant load, the resistance of the sensor will continually decrease, and the output will gradually increase. It is important to take drift into account when calibrating the sensor, so that its effects can be minimized. The simplest way to accomplish this is to perform the sensor calibration in a time frame similar to that which will be used in the application.

TEMPERATURE SENSITIVITY

In general, your results will vary if you combine high loads on the sensor with high temperatures.

To ensure accuracy, calibrate the sensor at the temperature at which it will be used in the application. If the sensor is being used at different temperatures, perform a calibration at each of these temperatures, save the calibration files, then load the appropriate calibration file when using the sensor at that temperature.

SENSOR LIFE / DURABILITY

Sensor life depends on the application in which it is used. Sensors are reusable, unless used in applications in which they are subjected to severe conditions, such as against sharp edges, or shear forces. ***FlexiForce*** sensors have been successfully tested at over one million load cycles using a 50 lb. force.

Rough handling of a sensor will also shorten its useful life. For example, a sensor that is repeatedly installed in a flanged joint will have a shorter life than a sensor installed in the same joint once and used to monitor loads over a prolonged period. After each installation, visually inspect your sensors for physical damage.

It is also important to keep the sensing area of the sensor clean. Any deposits on this area will create uneven loading, and will cause saturation to occur at lower applied forces.

SENSOR PROPERTIES

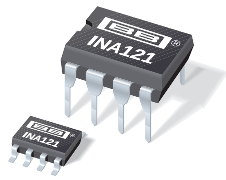
STANDARD FLEXIFORCE SENSOR (MODEL A201)

Sensor Properties	
Thickness	0.008 (0.208 mm)
Length	8” (203 mm) 6” (152 mm) 4” (102 mm) 2” (51 mm)
Width	0.55” (14 mm)
Sensing Area	0.375” (9.53 mm) diameter
Connector	3-pin male square pin (center pin is inactive)
Typical Performance	
Force Ranges	0-1 lb (4.4 N) 0-25 lbs (110 N) 0-100 lbs (440 N)*
Operating Temperature Range	15°F to 140°F (-9°C to 60°C)
Linearity (Error)	+/- 3%
Repeatability	+/- 2.5% of full scale (conditioned sensor, 80% force applied)
Hysteresis	<4.5% of full scale (conditioned sensor, 80% force applied)
Drift	<5% per logarithmic time scale (constant load of 90% sensor rating)
Response Time	<5 microseconds
Output Change/Degree F	Up to 0.2% (~0.36% / °C). Loads <10 lbs, operating temperature can be increased to 165°F (74°C).

HIGH-TEMPERATURE FLEXIFORCE SENSOR (MODEL HT201)

Sensor Properties	
Thickness	0.008” (0.203 mm)
Length	7.75” (197 mm) *Optional:* 6” (152 mm) *Trimmed:* 4” (102 mm) *Lengths:* 2” (51 mm)
Width	0.55” (14 mm)
Sensing Area	0.375” (9.53 mm) diameter
Connector	3-pin Male Square Pin (center pin is inactive)
Substrate	Polyimide (ex: Kapton)
Typical Performance	
Force Ranges	0-30 lbs (133N) 0-100 lbs (445N)
Operating Temperature Range	15°F to 400°F (-9°C to 204°C)
Repeatability	+/- 3.5% of full scale
Linearity	+/- 1.2% of full scale
Hysteresis	3.6% of full scale
Drift	3.3% per log time
Output Change/Degree F	0.16%

BURR - BROWN®



INA121

FET-Input, Low Power INSTRUMENTATION AMPLIFIER

FEATURES

- LOW BIAS CURRENT: ±4pA
- LOW QUIESCENT CURRENT: ±450µA
- LOW INPUT OFFSET VOLTAGE: ±200µV
- LOW INPUT OFFSET DRIFT: ±2µV/°C
- LOW INPUT NOISE:
  20nV/√Hz at f = 1kHz (G =100)
- HIGH CMR: 106dB
- WIDE SUPPLY RANGE: ±2.25V to ±18V
- LOW NONLINEARITY ERROR: 0.001% max
- INPUT PROTECTION TO ±40V
- 8-PIN DIP AND SO-8 SURFACE MOUNT

APPLICATIONS

- LOW-LEVEL TRANSDUCER AMPLIFIERS
  Bridge, RTD, Thermocouple
- PHYSIOLOGICAL AMPLIFIERS
  ECG, EEG, EMG, Respiratory
- HIGH IMPEDANCE TRANSDUCERS
- CAPACITIVE SENSORS
- MULTI-CHANNEL DATA ACQUISITION
- PORTABLE, BATTERY OPERATED SYSTEMS
- GENERAL PURPOSE INSTRUMENTATION

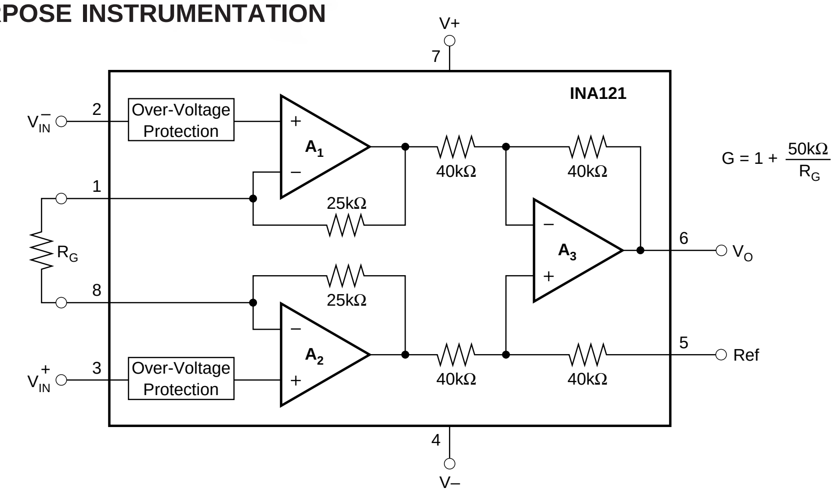
DESCRIPTION

The INA121 is a FET-input, low power instrumentation amplifier offering excellent accuracy. Its versatile three-op amp design and very small size make it ideal for a variety of general purpose applications. Low bias current (±4pA) allows use with high impedance sources.

Gain can be set from 1V to 10,000V/V with a single external resistor. Internal input protection can withstand up to ±40V without damage.

The INA121 is laser-trimmed for very low offset voltage (±200µV), low offset drift (±2µV/°C), and high common-mode rejection (106dB at G = 100). It operates on power supplies as low as ±2.25V (+4.5V), allowing use in battery operated and single 5V systems. Quiescent current is only 450µA.

Package options include 8-pin plastic DIP and SO-8 surface mount. All are specified for the –40°C to +85°C industrial temperature range.



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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1412A
Printed in U.S.A. May, 1998

SPECIFICATIONS: $V_S = \pm15V$

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ, and IA reference = 0V, unless otherwise noted.

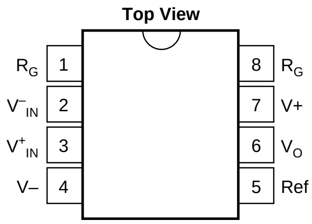
		INA121P, U			INA121PA, UA			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
Offset Voltage, RTI			±200±200/G	±500±500/G		±300±200/G	±1000±1000/G	µV
vs Temperature			±2±2/G	±5±20/G		*	±15±20/G	µV/°C
vs Power Supply	V_S = ±2.25V to ±18V		±5±20/G	±50±150/G		*	*	µV/V
Long-Term Stability			±0.5			*		µV/mo
Impedance, Differential			$10^{12} \parallel 1$			*		Ω ∥ pF
Common-Mode	V_O = 0V		$10^{12} \parallel 12$			*		Ω ∥ pF
Input Voltage Range			See Text and Typical Curves			*		
Safe Input Voltage				±40			*	V
Common-Mode Rejection	V_{CM} = –12.5V to 13.5V							
	G = 1	78	86		72	*		dB
	G = 10	91	100		85	*		dB
	G = 100	96	106		90	*		dB
	G = 1000		106			*		dB
BIAS CURRENT	V_{CM} = 0V		±4	±50		*	*	pA
vs Temperature			See Typical Curve			*		
Offset Current			±0.5			*		pA
vs Temperature			See Typical Curve			*		
NOISE, RTI	R_S = 0Ω							
Voltage Noise: f = 10Hz	G = 100		30			*		nV/√Hz
f = 100Hz	G = 100		21			*		nV/√Hz
f = 1kHz	G = 100		20			*		nV/√Hz
f = 0.1Hz to 10Hz	G = 100		1			*		µVp-p
Current Noise: f = 1kHz			1			*		fA/√Hz
GAIN								
Gain Equation			1 + (50kΩ/R_G)			*		V/V
Range of Gain		1		10,000	*		*	V/V
Gain Error	V_O = –14V to 13.5V							
	G = 1		±0.01	±0.05		*	±0.1	%
	G = 10		±0.03	±0.4		*	±0.5	%
	G = 100		±0.05	±0.5		*	±0.7	%
	G = 1000		±0.5			*		%
Gain vs Temperature[(1)]	G = 1		±1	±10		*	*	ppm/°C
	G > 1		±25	±100		*	*	ppm/°C
Nonlinearity	V_O = –14V to 13.5V							
	G = 1		±0.0002	±0.001		*	±0.002	% of FSR
	G = 10		±0.0015	±0.005		*	±0.008	% of FSR
	G = 100		±0.0015	±0.005		*	±0.008	% of FSR
	G = 1000		±0.002			*		% of FSR
OUTPUT								
Voltage: Positive	R_L = 100kΩ		(V+)–0.9			*		V
Negative	R_L = 100kΩ		(V–)+0.15			*		V
Positive	R_L = 10kΩ	(V+)–1.5	(V+)–0.9		*	*		V
Negative	R_L = 10kΩ	(V–)+1	(V–)+0.25		*	*		V
Capacitance Load Drive			1000			*		pF
Short-Circuit Current			±14			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 1		600			*		kHz
	G = 10		300			*		kHz
	G = 100		50			*		kHz
	G = 1000		5			*		kHz
Slew Rate	V_O = ±10V, G ≤ 10		0.7			*		V/µs
Settling Time, 0.01%	G = 1 to 10		20			*		µs
	G = 100		35			*		µs
	G = 1000		260			*		µs
Overload Recovery	50% Input Overload		5			*		µs
POWER SUPPLY								
Voltage Range		±2.25	±15	±18	*	*	*	V
Quiescent Current	I_O = 0V		±450	±525		*	*	µA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating		–55		125	*		*	°C
Storage		–55		125	*		*	°C
Thermal Resistance, θ_{JA}								
8-Lead DIP			100			*		°C/W
SO-8 Surface Mount			150			*		°C/W

* Specification same as INA121P, U.

NOTE: (1) Temperature coefficient of the “Internal Resistor” in the gain equation. Does not include TCR of gain-setting resistor, R_G.

PIN CONFIGURATION

Top View — 8-Pin DIP and SO-8



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Analog Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

PACKAGE/ORDERING INFORMATION

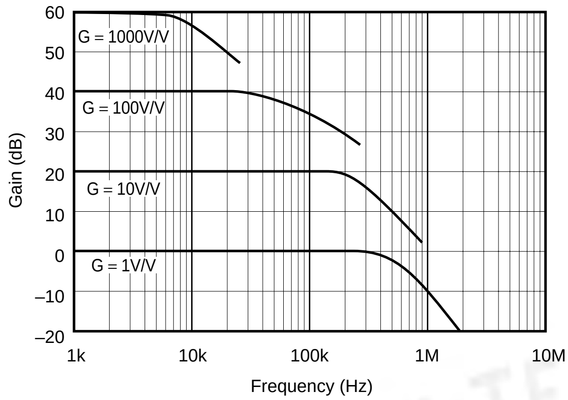
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(2)	TRANSPORT MEDIA
Single						
INA121P	8-Pin DIP	006	–40°C to +85°C	INA121P	INA121P	Rails
INA121PA	8-Pin DIP	006	–40°C to +85°C	INA121PA	INA121PA	Rails
INA121U	SO-8 Surface-Mount	182	–40°C to +85°C	INA121U	INA121U	Rails
"	"	"	"	"	INA121U/2K5	Tape and Reel
INA121UA	SO-8 Surface-Mount	182	–40°C to +85°C	INA121UA	INA121UA	Rails
"	"	"	"	"	INA121UA/2K5	Tape and Reel

NOTES: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book. (2) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "INA121U/2K5" will get a single 2500-piece Tape and Reel. For detailed Tape and Reel mechanical information, refer to Appendix B of Burr-Brown IC Data Book.

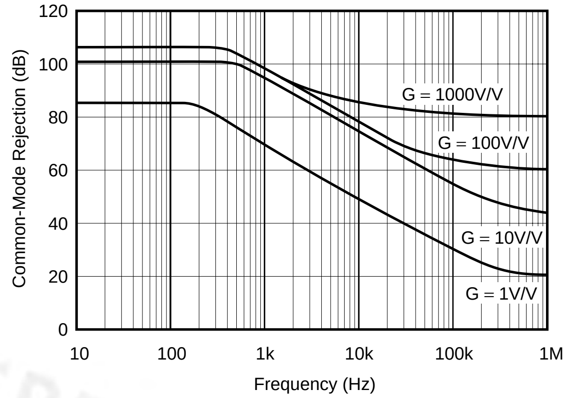
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

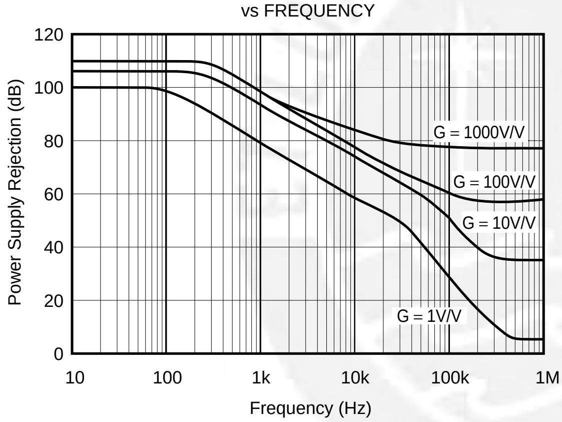
GAIN vs FREQUENCY



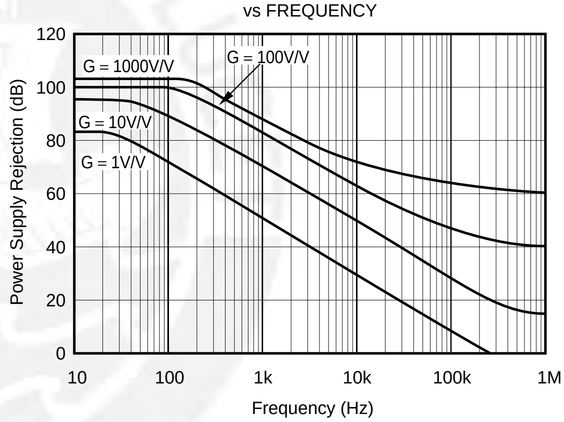
COMMON-MODE REJECTION
vs FREQUENCY



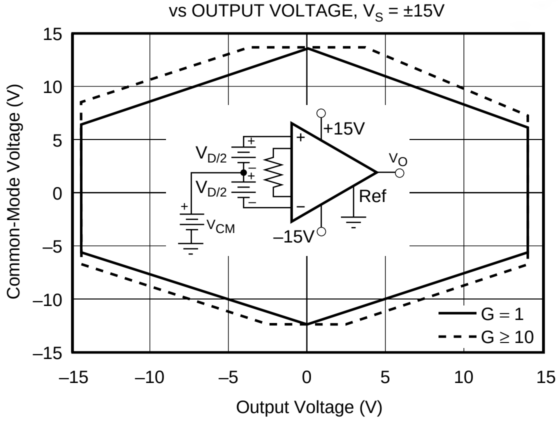
POSITIVE POWER SUPPLY REJECTION
vs FREQUENCY



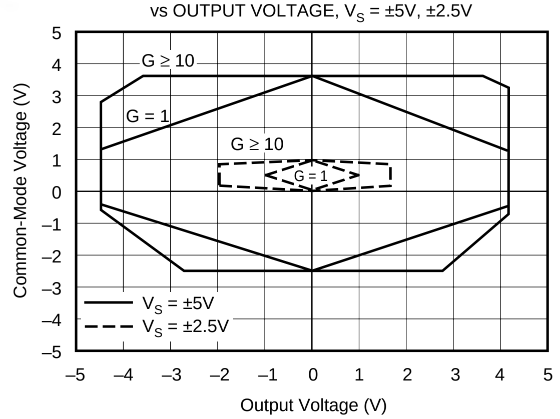
NEGATIVE POWER SUPPLY REJECTION
vs FREQUENCY



INPUT COMMON-MODE RANGE
vs OUTPUT VOLTAGE, V_S = ±15V



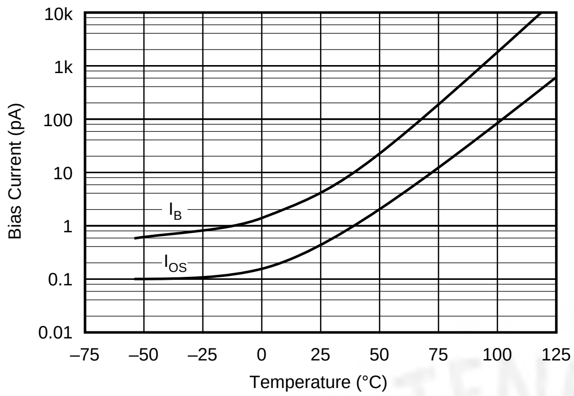
INPUT COMMON-MODE RANGE
vs OUTPUT VOLTAGE, V_S = ±5V, ±2.5V



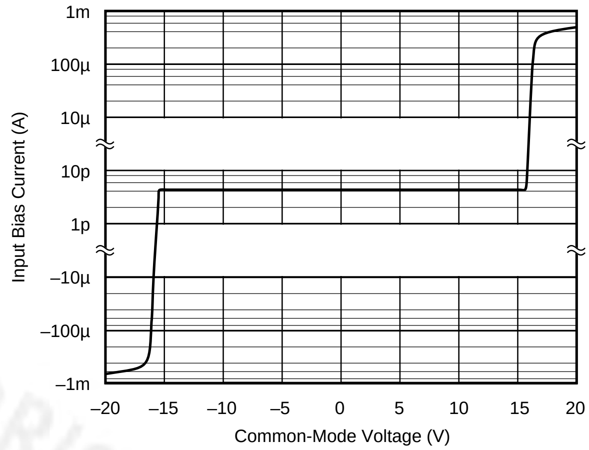
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

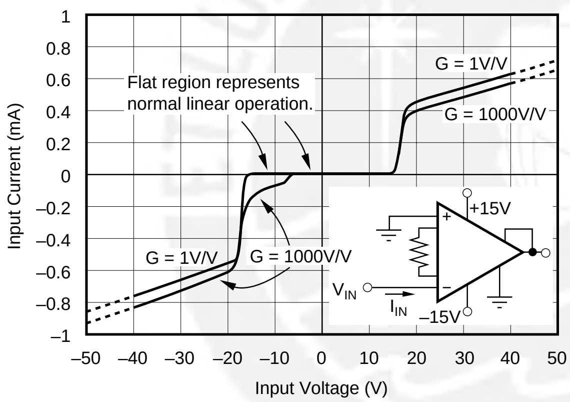
INPUT BIAS CURRENT vs TEMPERATURE



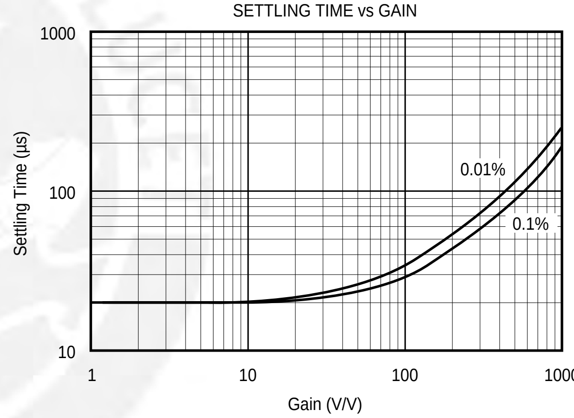
INPUT BIAS CURRENT
vs COMMON-MODE INPUT VOLTAGE



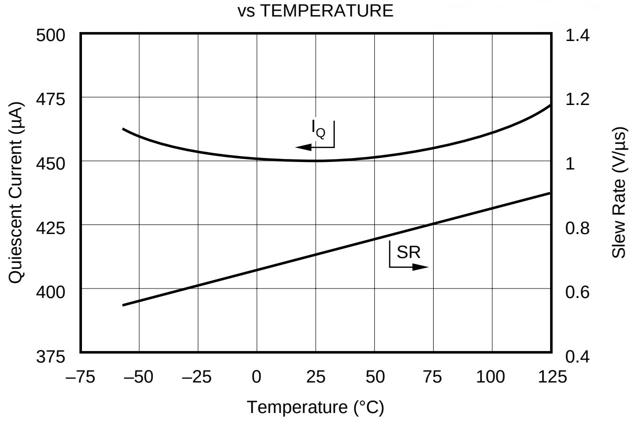
INPUT OVER-VOLTAGE V/I CHARACTERISTICS



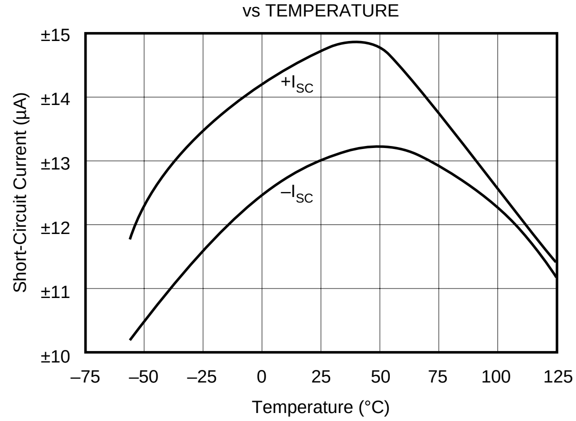
SETTLING TIME vs GAIN



QUIESCENT CURRENT AND SLEW RATE
vs TEMPERATURE



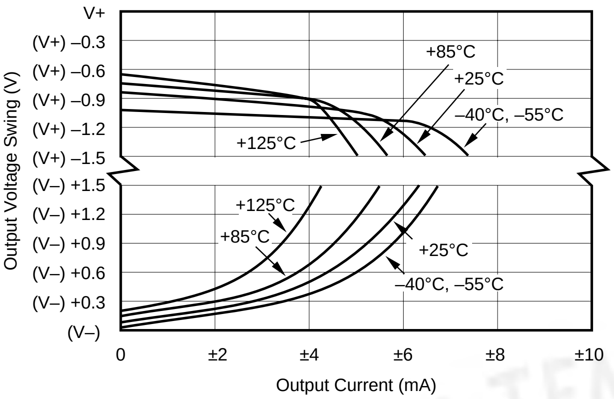
SHORT-CIRCUIT CURRENT
vs TEMPERATURE



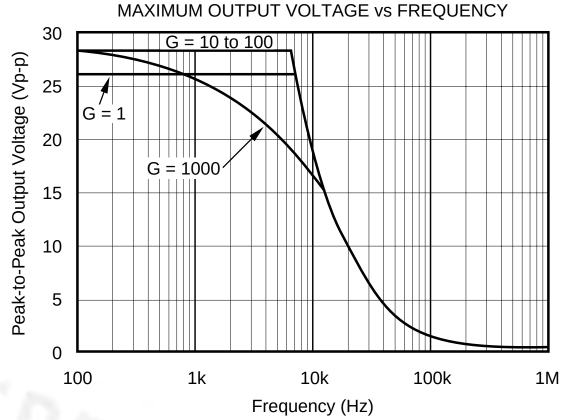
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

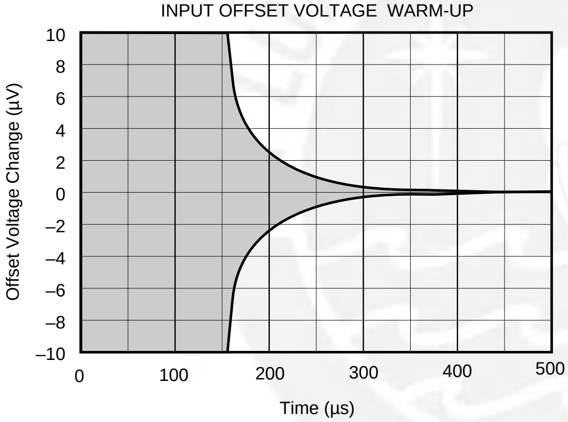
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



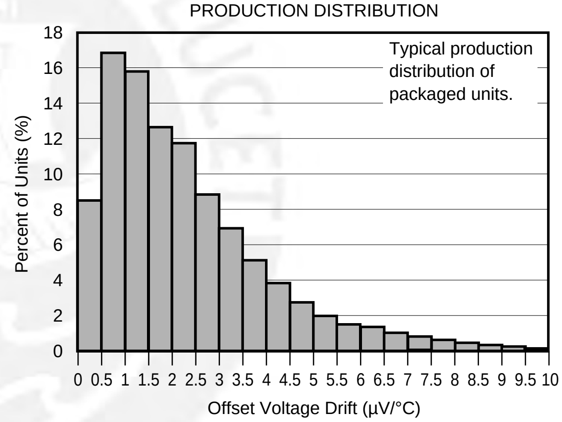
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



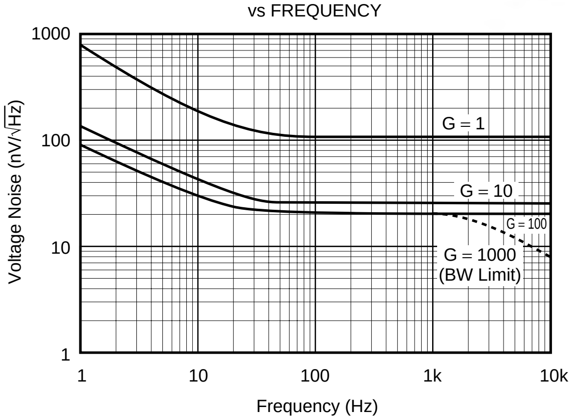
INPUT OFFSET VOLTAGE WARM-UP



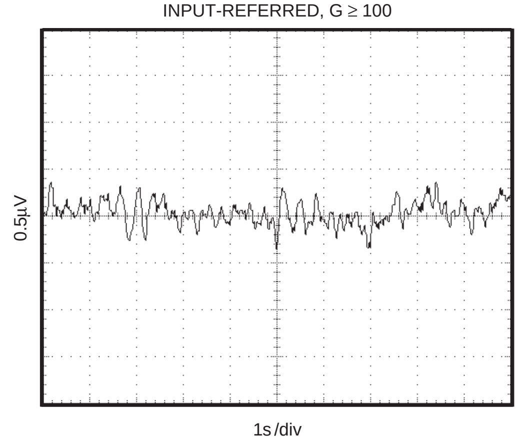
INPUT OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



INPUT-REFERRED NOISE VOLTAGE
vs FREQUENCY



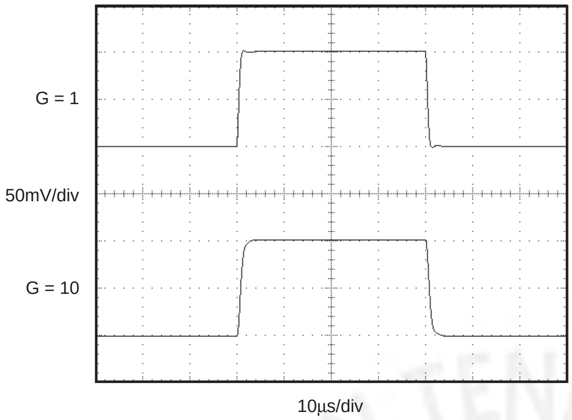
VOLTAGE NOISE 0.1 TO 10Hz
INPUT-REFERRED, G ≥ 100



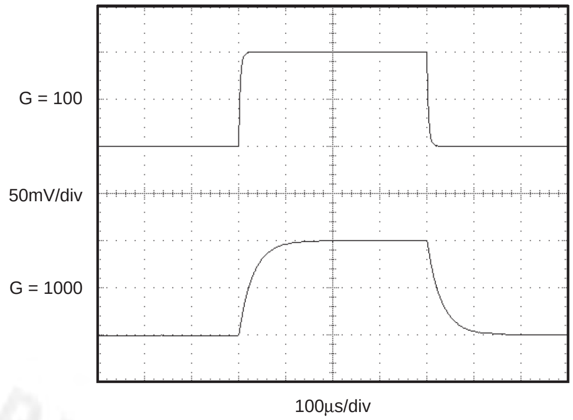
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

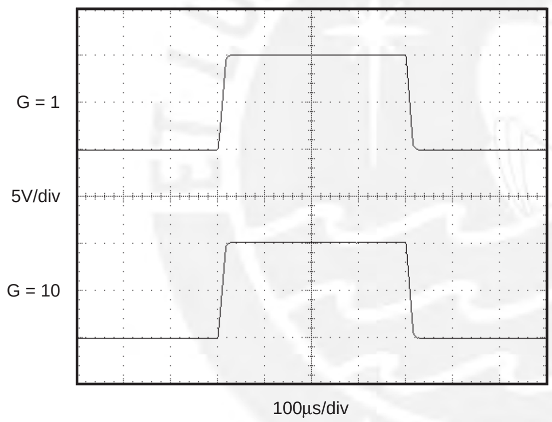
SMALL-SIGNAL STEP RESPONSE
(G = 1, 10)



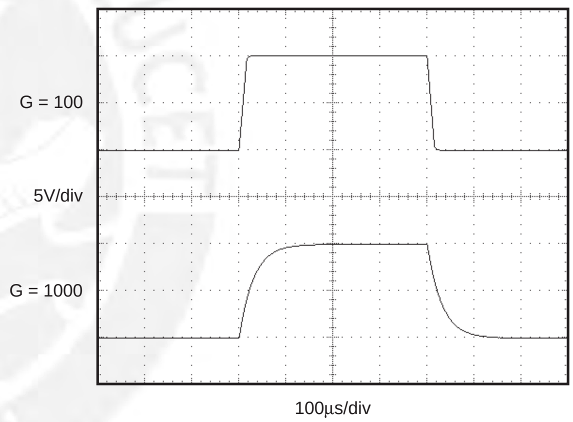
SMALL-SIGNAL STEP RESPONSE
(G = 100, 1000)



LARGE-SIGNAL STEP RESPONSE
(G = 1, 10)



LARGE-SIGNAL STEP RESPONSE
(G = 100, 1000)



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA121. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 8Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

SETTING THE GAIN

Gain of the INA121 is set by connecting a single external resistor, R_G, connected between pins 1 and 8:

$$G = 1 + \frac{50k\Omega}{R_G} \qquad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in Equation 1 comes from the sum of the two internal feedback resistors of A_1 and A_2. These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA121.

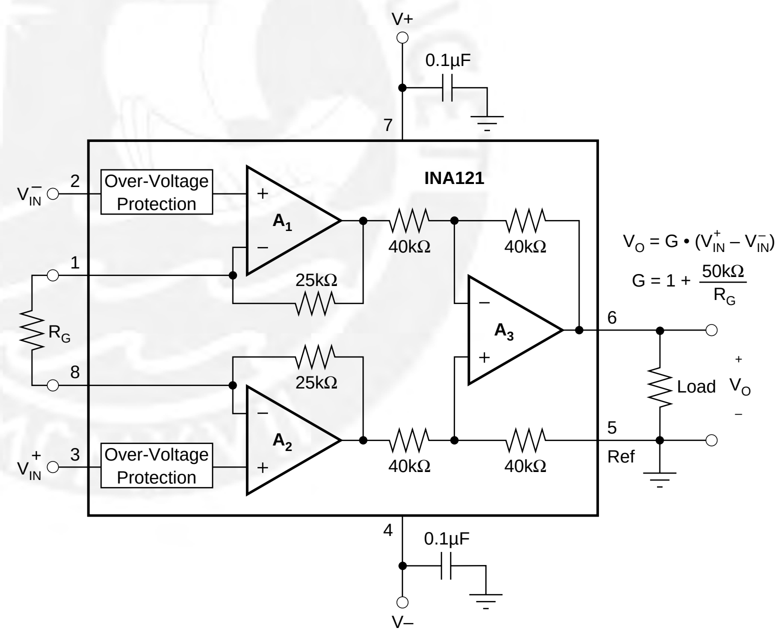
The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

DYNAMIC PERFORMANCE

The typical performance curve "Gain vs Frequency" shows that, despite its low quiescent current, the INA121 achieves wide bandwidth, even at high gain. This is due to the current-feedback topology of the INA121. Settling time also remains excellent at high gain.

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC	NC
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

NC: No Connection.



Also drawn in simplified form:

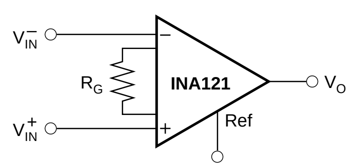


FIGURE 1. Basic Connections.

The INA121 provides excellent rejection of high frequency common-mode signals. The typical performance curve, "Common-Mode Rejection vs Frequency" shows this behavior. If the inputs are not properly balanced, however, common-mode signals can be converted to differential signals. Run the V_{IN}^+ and V_{IN}^- connections directly adjacent each other, from the source signal all the way to the input pins. If possible use a ground plane under both input traces. Avoid running other potentially noisy lines near the inputs.

NOISE AND ACCURACY PERFORMANCE

The INA121's FET input circuitry provides low input bias current and high speed. It achieves lower noise and higher accuracy with high impedance sources. With source impedances of 2kΩ to 50kΩ the INA114, INA128, or INA129 may provide lower offset voltage and drift. For very low source impedance (≤1kΩ), the INA103 may provide improved accuracy and lower noise. At very high source impedances (> 1MΩ) the INA116 is recommended.

OFFSET TRIMMING

The INA121 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection. Trim circuits with higher source impedance should be buffered with an op amp follower circuit to assure low impedance on the Ref pin.

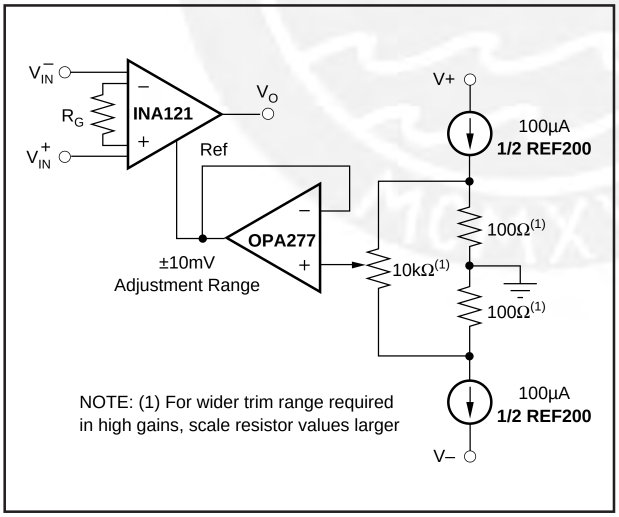


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA121 is extremely high—approximately 10^{12}Ω. However, a path must be provided for the input bias current of both inputs. This input bias current is typically 4pA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA121 is to operate properly. Figure 3 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA121 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

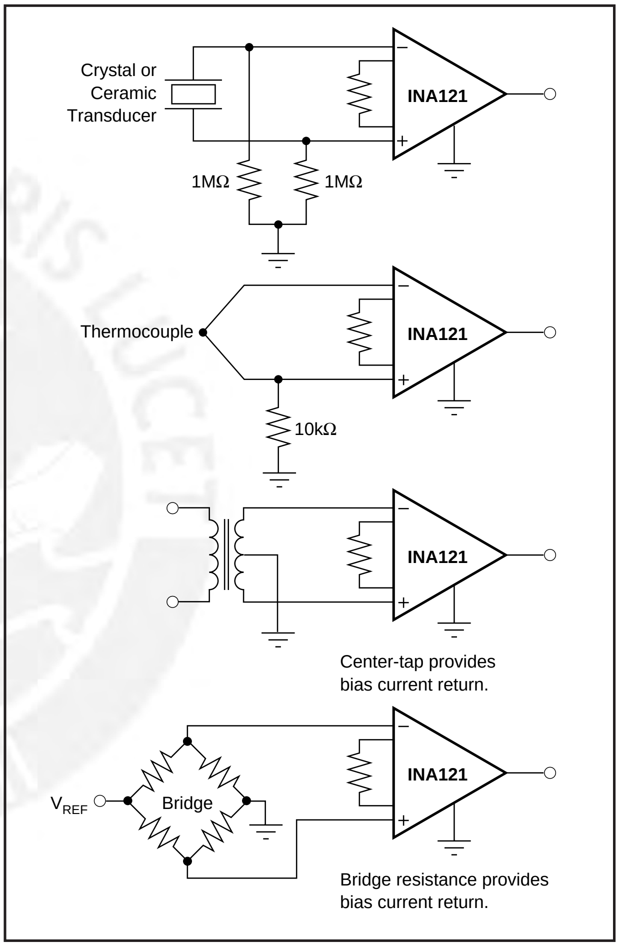


FIGURE 3. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA121 is from approximately 1.2V below the positive supply voltage to 2.1V above the negative supply. A differential input voltage causes the output voltage to increase. The linear input range, however, will be limited by the output voltage swing of amplifiers A_1 and A_2. So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see typical performance curve "Input Common-Mode Range vs Output Voltage".

A combination of common-mode and differential input voltage can cause the output of A_1 or A_2 to saturate. Figure 4 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA121 in a lower gain (see performance curve "Input Common-Mode Voltage Range vs Output Voltage"). If necessary, add gain after the INA121 to increase the voltage swing.

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of A_3 will be near 0V even though both inputs are overloaded.

LOW VOLTAGE OPERATION

The INA121 can be operated on power supplies as low as ±2.25V. Performance remains excellent with power supplies ranging from ±2.25V to ±18V. Most parameters vary only slightly throughout this supply voltage range—see typical performance curves. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Typical performance curves, "Input Common-Mode Range vs Output Voltage" show the range of linear operation for ±15V, ±5V, and ±2.5V supplies.

INPUT FILTERING

The INA121's FET input allows use of an R/C input filter without creating large offsets due to input bias current. Figure 5 shows proper implementation of this input filter to preserve the INA121's excellent high frequency common-mode rejection. Mismatch of the common-mode input time constant (R_1C_1 and R_2C_2), either from stray capacitance or mismatched values, causes a high frequency common-mode signal to be converted to a differential signal. This degrades common-mode rejection. The differential input capacitor, C_3, reduces the bandwidth and mitigates the effects of mismatch in C_1 and C_2. Make C_3 much larger than C_1 and C_2. If properly matched, C_1 and C_2 also improve ac CMR.

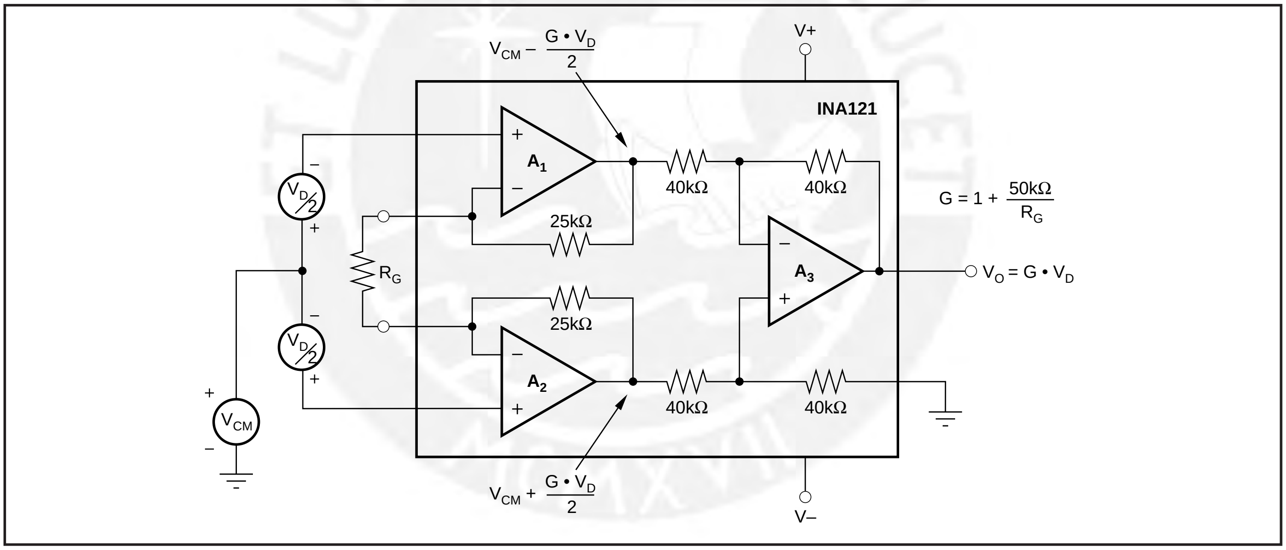


FIGURE 4. Voltage Swing of A_1 and A_2.

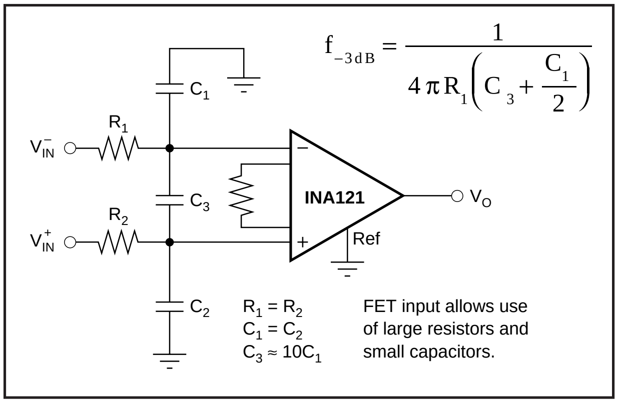


FIGURE 5. Input Low-Pass Filter.

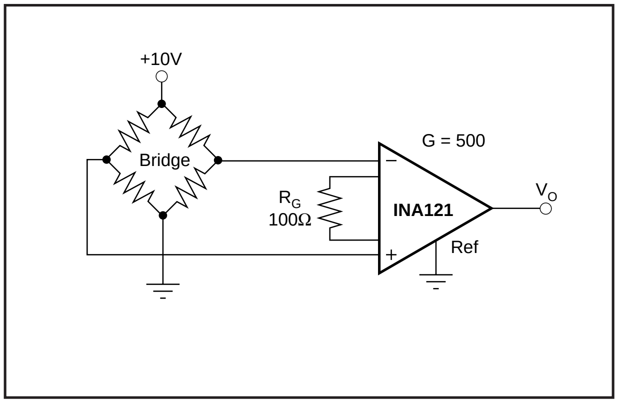


FIGURE 6. Bridge Transducer Amplifier.

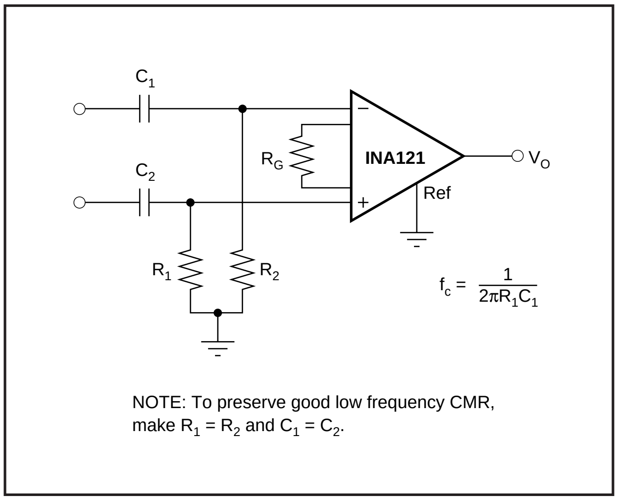


FIGURE 7. High-Pass Input Filter.

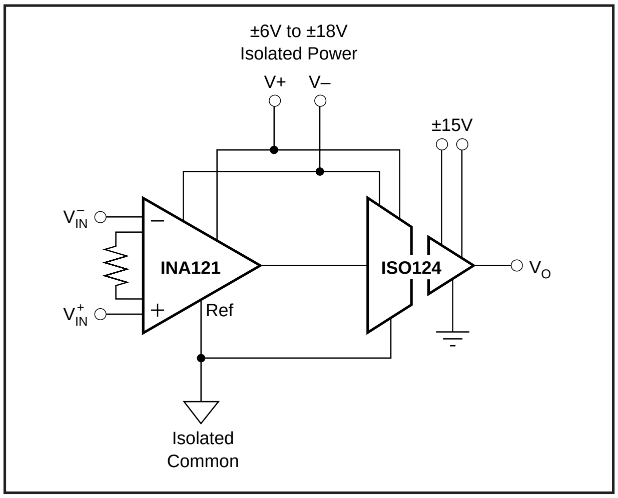


FIGURE 8. Galvanically Isolated Instrumentation Amplifier.

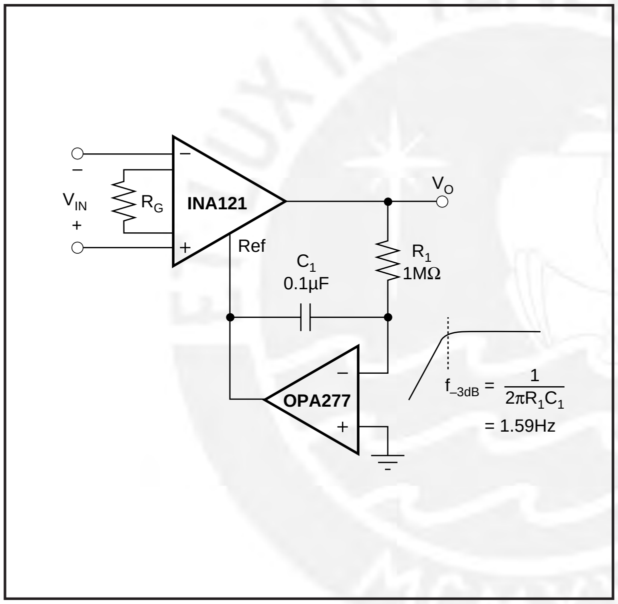


FIGURE 9. AC-Coupled Instrumentation Amplifier.

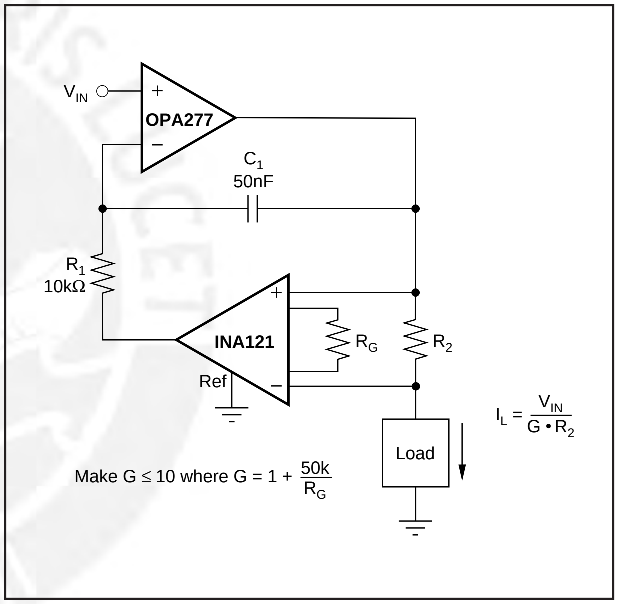


FIGURE 10. Voltage Controlled Current Source.

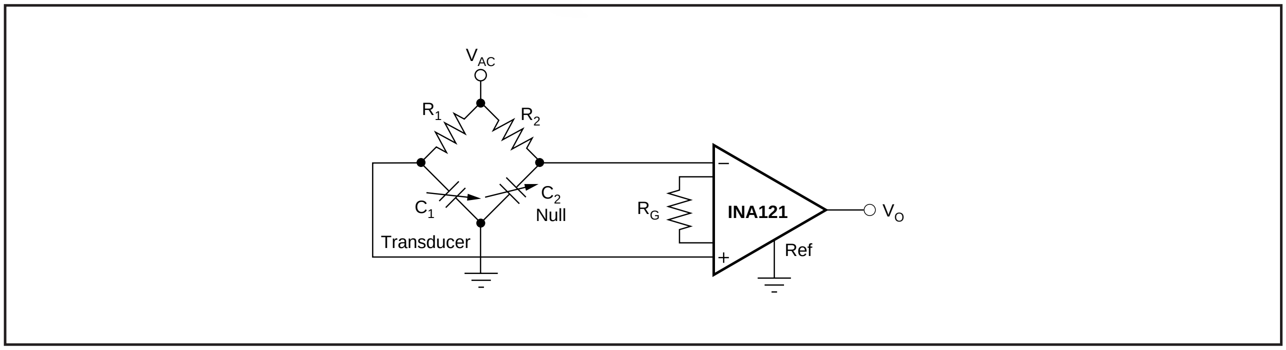


FIGURE 11. Capacitive Bridge Transducer Circuit.

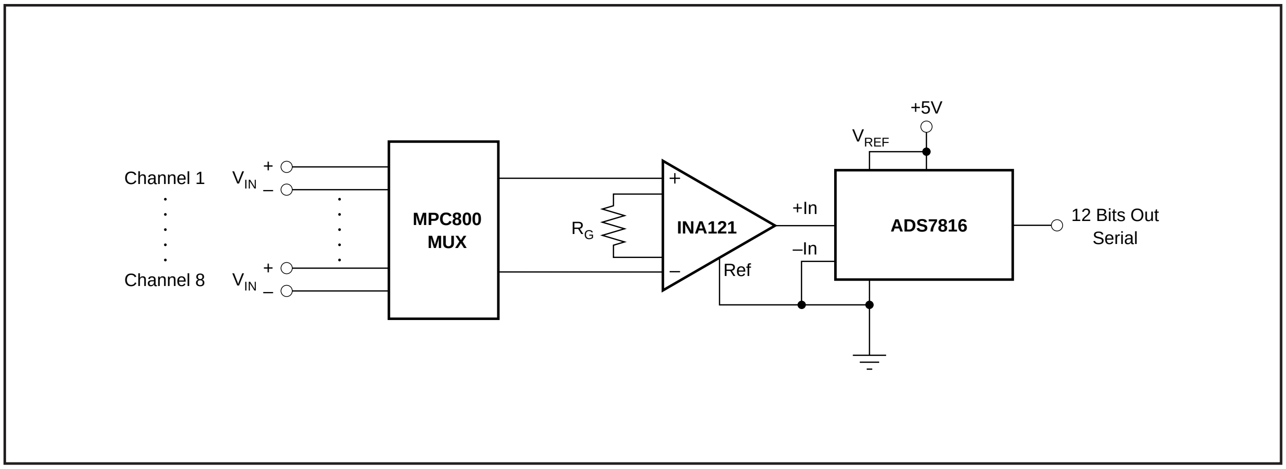


FIGURE 12. Multiplexed-Input Data Acquisition System.

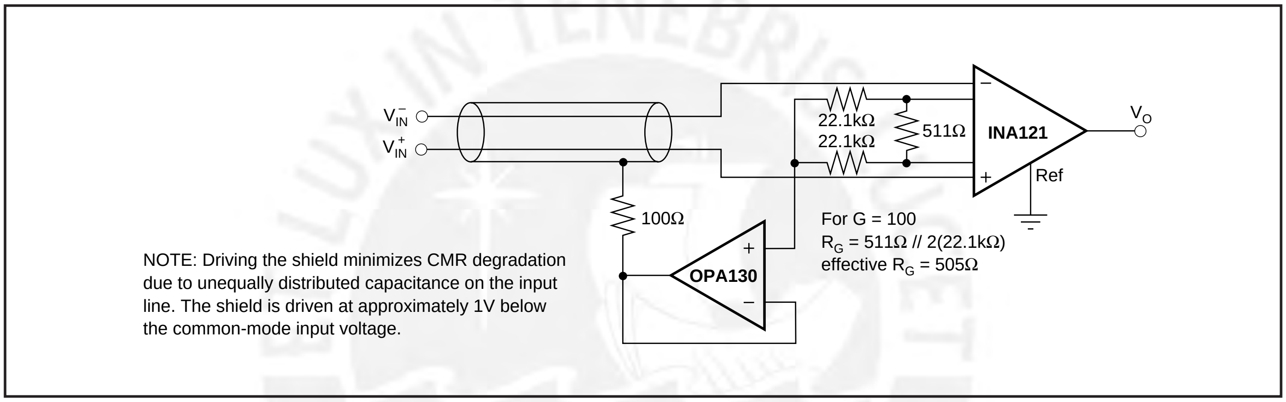


FIGURE 13. Shield Driver Circuit.

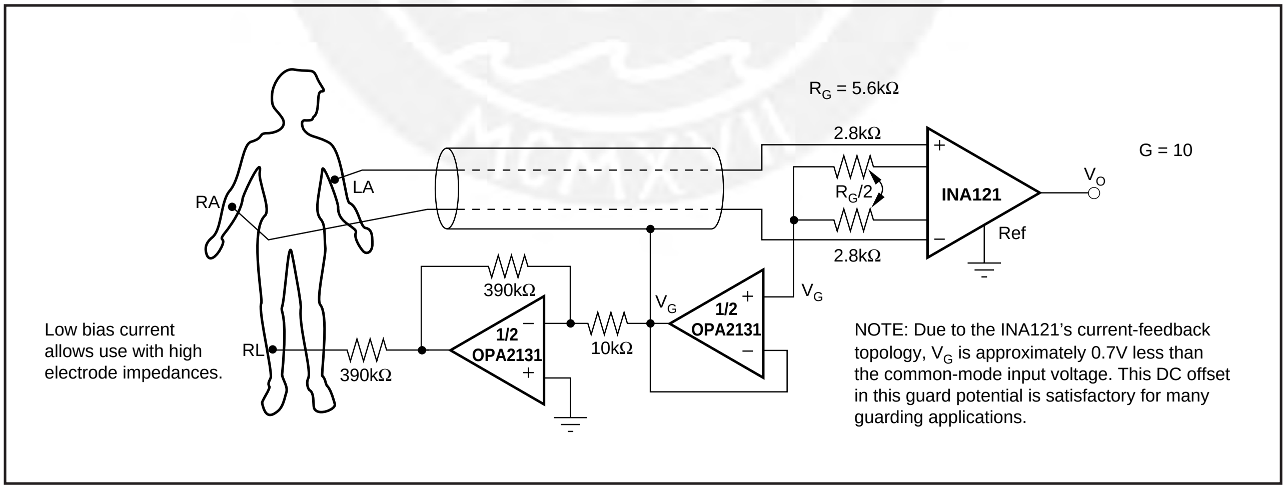


FIGURE 14. ECG Amplifier With Right-Leg Drive.

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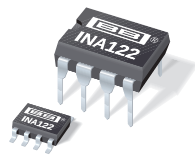


INA122

Single Supply, *Micro*Power INSTRUMENTATION AMPLIFIER

FEATURES

- LOW QUIESCENT CURRENT: 60μA
- WIDE POWER SUPPLY RANGE
  - Single Supply: 2.2V to 36V
  - Dual Supply: –0.9/+1.3V to ±18V
- COMMON-MODE RANGE TO (V–)–0.1V
- RAIL-TO-RAIL OUTPUT SWING
- LOW OFFSET VOLTAGE: 250μV max
- LOW OFFSET DRIFT: 3μV/°C max
- LOW NOISE: 60nV/√Hz
- LOW INPUT BIAS CURRENT: 25nA max
- 8-PIN DIP AND SO-8 SURFACE-MOUNT

APPLICATIONS

- PORTABLE, BATTERY OPERATED SYSTEMS
- INDUSTRIAL SENSOR AMPLIFIER: Bridge, RTD, Thermocouple
- PHYSIOLOGICAL AMPLIFIER: ECG, EEG, EMG
- MULTI-CHANNEL DATA ACQUISITION

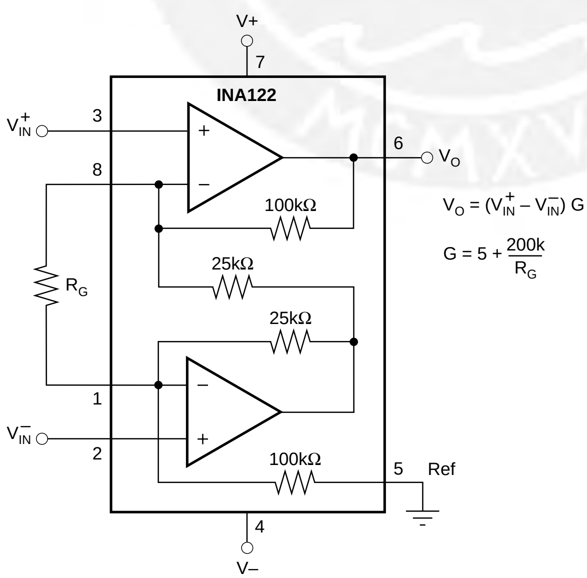
DESCRIPTION

The INA122 is a precision instrumentation amplifier for accurate, low noise differential signal acquisition. Its two-op-amp design provides excellent performance with very low quiescent current, and is ideal for portable instrumentation and data acquisition systems.

The INA122 can be operated with single power supplies from 2.2V to 36V and quiescent current is a mere 60μA. It can also be operated from dual supplies. By utilizing an input level-shift network, input common-mode range extends to 0.1V below negative rail (single supply ground).

A single external resistor sets gain from 5V/V to 10000V/V. Laser trimming provides very low offset voltage (250μV max), offset voltage drift (3μV/°C max) and excellent common-mode rejection.

Package options include 8-pin plastic DIP and SO-8 surface-mount packages. Both are specified for the –40°C to +85°C extended industrial temperature range.



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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

 PDS-1388B Printed in U.S.A. October, 1997

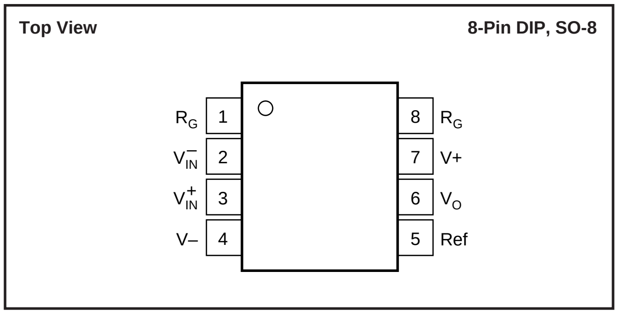
SPECIFICATIONS

At T_A = +25°C, V_S = +5V, R_L = 20kΩ connected to V_S/2, unless otherwise noted.

PARAMETER	CONDITIONS	INA122P, U MIN	INA122P, U TYP	INA122P, U MAX	INA122PA, UA MIN	INA122PA, UA TYP	INA122PA, UA MAX	UNITS
INPUT								
Offset Voltage, RTI			±100	±250		±150	±500	µV
vs Temperature			±1	±3		*	±5	µV/°C
vs Power Supply (PSRR)	V_S = +2.2V to +36V		10	30		*	100	µV/V
Input Impedance			10^{10} || 3			*		Ω || pF
Safe Input Voltage	R_S = 0	(V–)–0.3		(V+)+0.3	*		*	V
	R_S = 10kΩ	(V–)–40		(V+)+40	*		*	V
Common-Mode Voltage Range		0		3.4	*		*	V
Common-Mode Rejection	V_{CM} = 0V to 3.4V	83	96		76	90		dB
INPUT BIAS CURRENT			–10	–25		*	–50	nA
vs Temperature			±40			*		pA/°C
Offset Current			±1	±2		*	±5	nA
vs Temperature			±40			*		pA/°C
GAIN			G = 5 to 10k			*		V/V
Gain Equation			G = 5 + 200kΩ/R_G			*		V/V
Gain Error	G = 5		±0.05	±0.1		*	±0.15	%
vs Temperature	G = 5		5	10		*	*	ppm/°C
Gain Error	G = 100		±0.3	±0.5		*	±1	%
vs Temperature	G = 100		±25	±100		*	*	ppm/°C
Nonlinearity	G = 100, V_O = –14.85V to +14.9V		±0.005	±0.012		*	±0.024	%
NOISE (RTI)								
Voltage Noise, f = 1kHz			60			*		nV/√Hz
f = 100Hz			100			*		nV/√Hz
f = 10Hz			110			*		nV/√Hz
f_B = 0.1Hz to 10Hz			2			*		µVp-p
Current Noise, f = 1kHz			80			*		fA/√Hz
f_B = 0.1Hz to 10Hz			2			*		pAp-p
OUTPUT								
Voltage, Positive	V_S = ±15V	(V+)–0.1	(V+)–0.05		*	*		V
Negative	V_S = ±15V	(V–)+0.15	(V–)+0.1		*	*		V
Short-Circuit Current	Short-Circuit to Ground		+3/–30			*		mA
Capacitive Load Drive			1			*		nF
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 5		120			*		kHz
	G = 100		5			*		kHz
	G = 500		0.9			*		kHz
Slew Rate			+0.08/–0.16			*		V/µs
Settling Time, 0.01%	G = 5		350			*		µs
	G = 100		450			*		µs
	G = 500		1.8			*		ms
Overload Recovery	50% Input Overload		3			*		µs
POWER SUPPLY								
Voltage Range, Single Supply		+2.2	+5	+36	*	*	*	V
Dual Supplies		–0.9/+1.3		±18	*	*	*	V
Current	I_O = 0		60	85		*	*	µA
TEMPERATURE RANGE								
Specification		–40		+85	*		*	°C
Operation		–55		+85	*		*	°C
Storage		–55		+125	*		*	°C
Thermal Resistance, θ_{JA}								
8-Pin DIP			150			*		°C/W
SO-8 Surface-Mount			150			*		°C/W

* Specification same as INA122P, INA122U.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V+ to V–	36V
Signal Input Terminals, Voltage[2]	(V–)–0.3V to (V+)+0.3V
Current[2]	5mA
Output Short Circuit	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. (2) Input terminals are internally diode-clamped to the power supply rails. Input signals that can exceed the supply rails by more than 0.3V should be current-limited to 5mA or less.

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
INA122PA	8-Pin DIP	006
INA122P	8-Pin DIP	006
INA122UA	SO-8 Surface Mount	182
INA122U	SO-8 Surface Mount	182

NOTE: (1) For detailed drawing and dimension table, see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

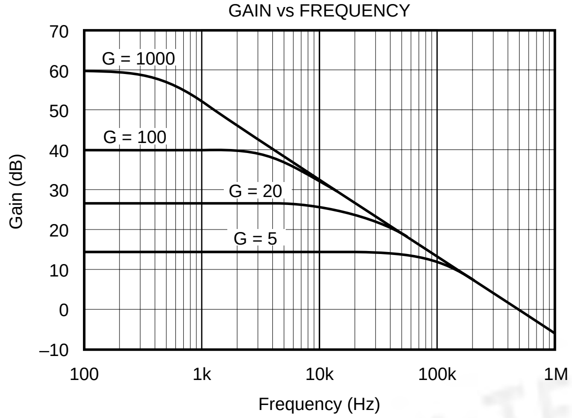
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

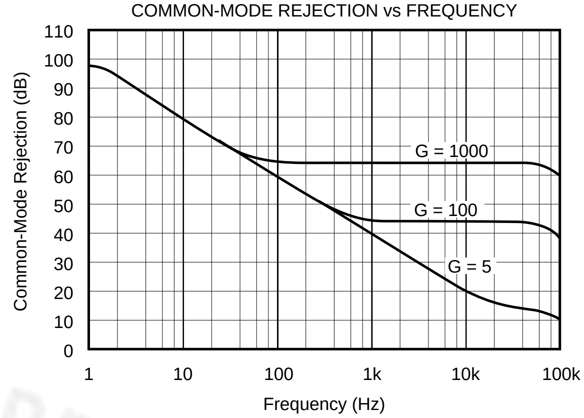
TYPICAL PERFORMANCE CURVES

At T_A = +25°C and V_S = ±5V, unless otherwise noted.

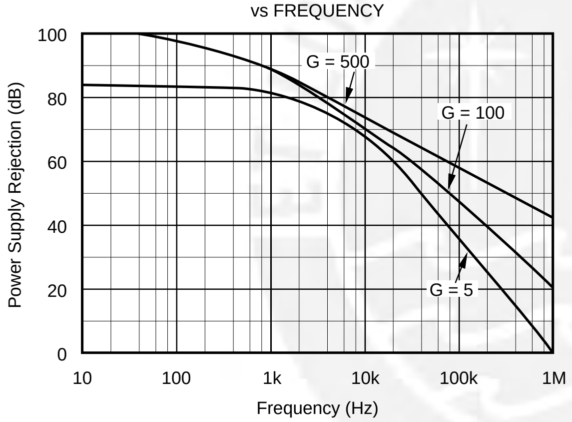
GAIN vs FREQUENCY



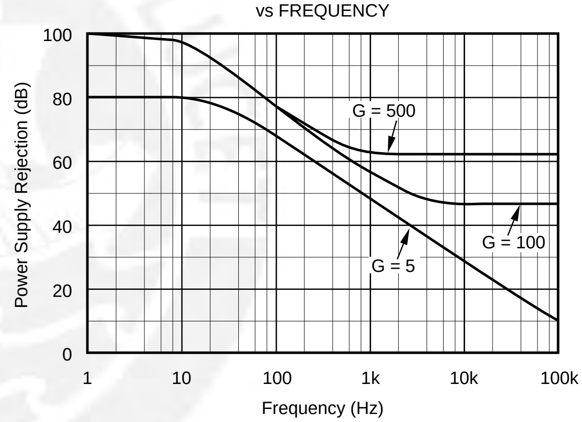
COMMON-MODE REJECTION vs FREQUENCY



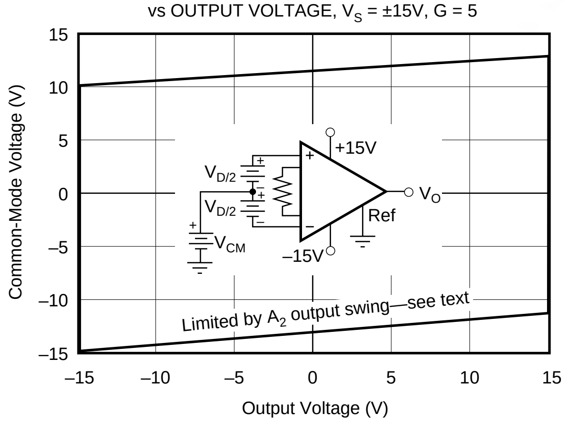
POSITIVE POWER SUPPLY REJECTION
vs FREQUENCY



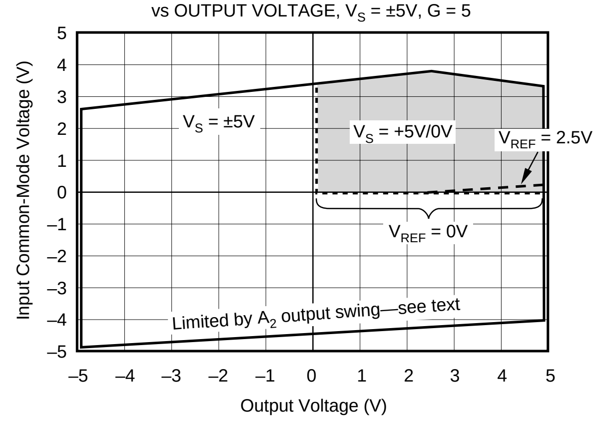
NEGATIVE POWER SUPPLY REJECTION
vs FREQUENCY



INPUT COMMON-MODE RANGE
vs OUTPUT VOLTAGE, V_S = ±15V, G = 5

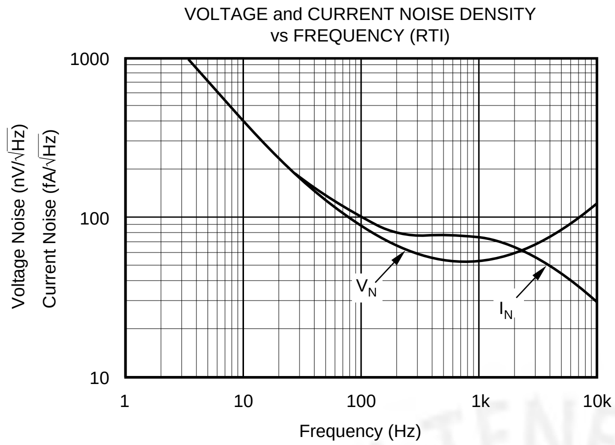


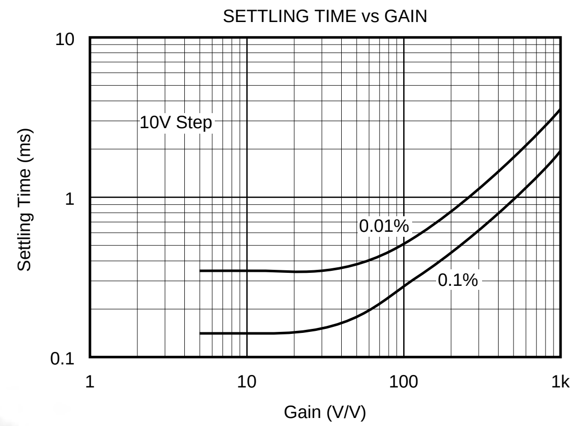
INPUT COMMON-MODE VOLTAGE
vs OUTPUT VOLTAGE, V_S = ±5V, G = 5

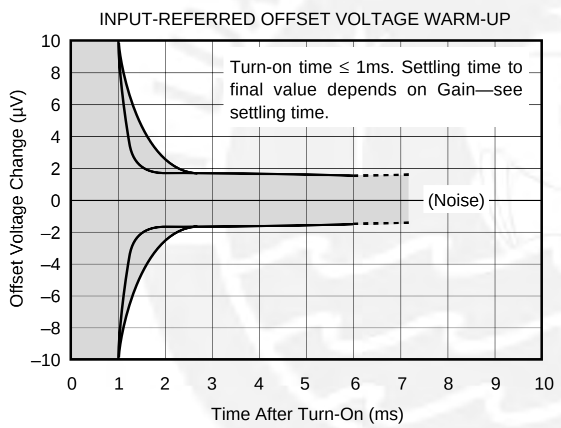


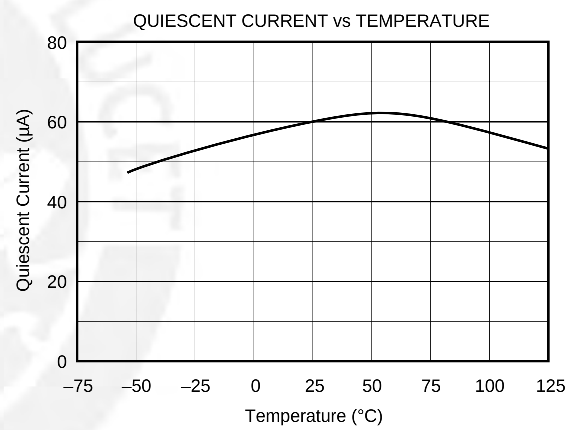
TYPICAL PERFORMANCE CURVES (CONT)

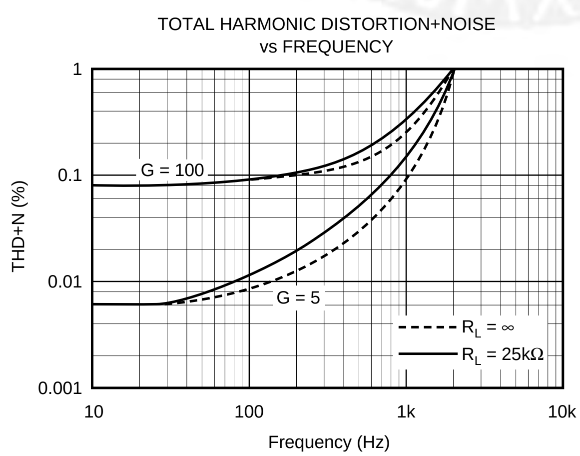
At T_A = +25°C and V_S = ±5V, unless otherwise noted.

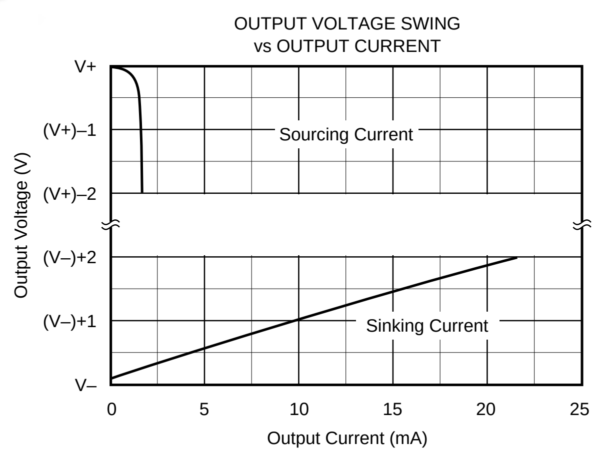








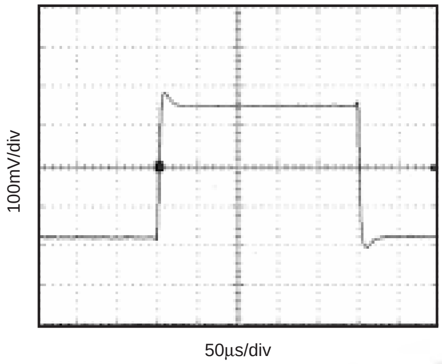




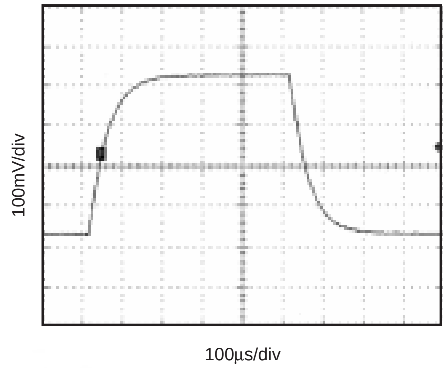
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C and V_S = ±5V, unless otherwise noted.

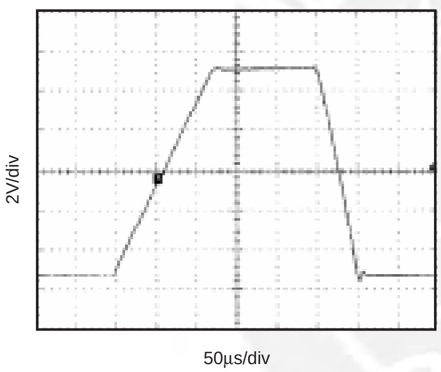
SMALL-SIGNAL STEP RESPONSE
G = 5



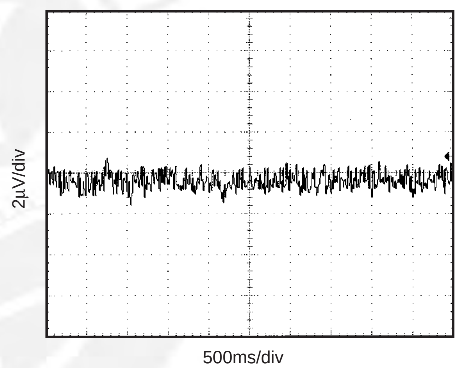
SMALL-SIGNAL STEP RESPONSE
G = 100



LARGE-SIGNAL STEP RESPONSE
G = 5



INPUT-REFERRED NOISE VOLTAGE
0.1Hz to 10Hz



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA122. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to ensure good common-mode rejection. A resistance of 10Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR.

SETTING THE GAIN

Gain of the INA122 is set by connecting a single external resistor, R_G, as shown:

$$G = 5 + \frac{200k\Omega}{R_G} \quad (1)$$

Commonly used gains and R_G resistor values are shown in Figure 1.

The 200kΩ term in equation 1 comes from the internal metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA122.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1).

OFFSET TRIMMING

The INA122 is laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref terminal is added to the output signal. An op amp buffer is used to provide low impedance at the Ref terminal to preserve good common-mode rejection.

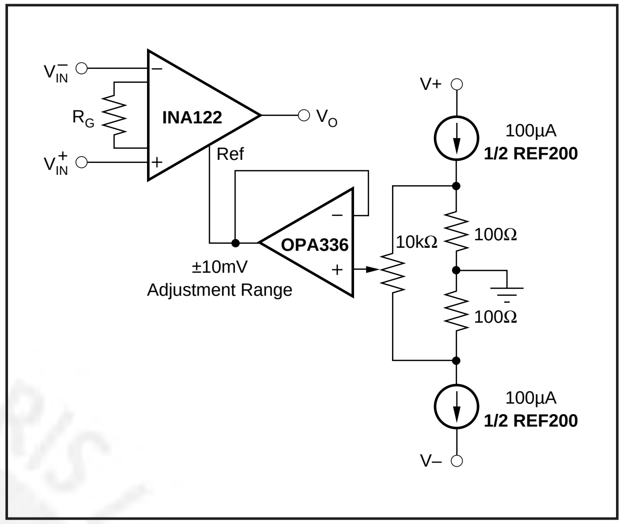


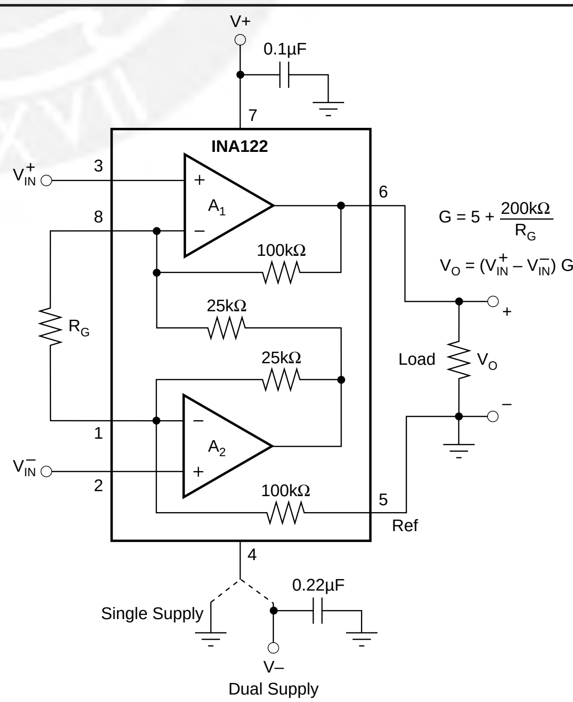
FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA122 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately –10nA (current flows out of the input terminals). High input impedance means that this input bias current changes very little with varying input voltage.

DESIRED GAIN (V/V)	R_G (Ω)	NEAREST 1% R_G VALUE
5	NC	NC
10	40k	40.2k
20	13.33k	13.3k
50	4444	4420
100	2105	2100
200	1026	1020
500	404	402
1000	201	200
2000	100.3	100
5000	40	40.2
10000	20	20

NC: No Connection.



Also drawn in simplified form:

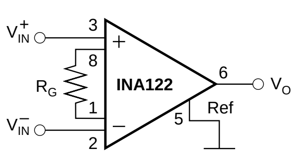


FIGURE 1. Basic Connections.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range of the INA122 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

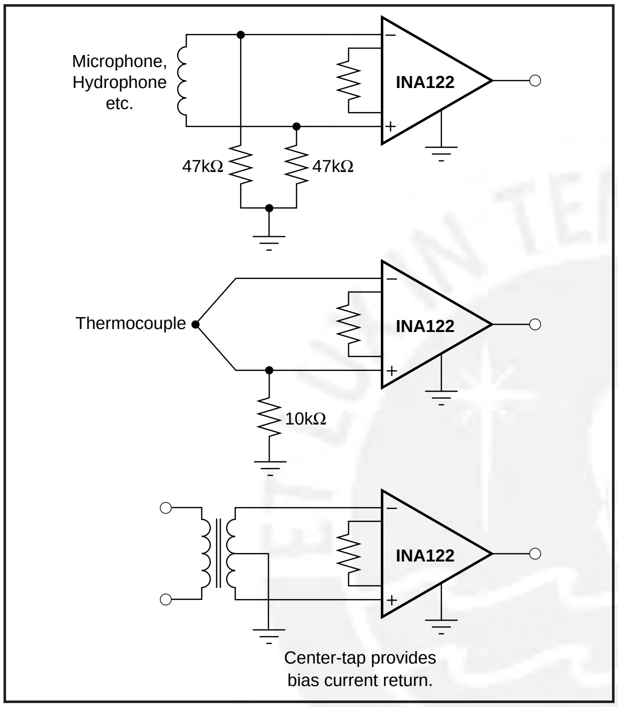


FIGURE 3. Providing an Input Common-Mode Current Path.

INPUT PROTECTION

The inputs of the INA122 are protected with internal diodes connected to the power supply rails (Figure 4). These diodes will clamp the applied signal to prevent it from damaging the input circuitry. If the input signal voltage can exceed the power supplies by more than 0.3V, the input signal current should be limited to less than 5mA to protect the internal clamp diodes. This can generally be done with a series input resistor. Some signal sources are inherently current-limited and do not require limiting resistors.

INPUT COMMON-MODE RANGE

The common-mode range for some common operating conditions is shown in the typical performance curves. The INA122 can operate over a wide range of power supply and V_{REF} configurations, making it impractical to provide a comprehensive guide to common-mode range limits for all possible conditions. The most commonly overlooked overload condition occurs by attempting to exceed the output swing of A_2, an internal circuit node that cannot be measured. Calculating the expected voltages at A_2's output (see equation in Figure 4) provides a check for the most common overload conditions.

The design of A_1 and A_2 are identical and their outputs can swing to within approximately 100mV of the power supply rails, depending on load conditions. When A_2's output is saturated, A_1 can still be in linear operation, responding to changes in the non-inverting input voltage. This may give the appearance of linear operation but the output voltage is invalid.

A single supply instrumentation amplifier has special design considerations. Using commonly available single-supply op amps to implement the two-op amp topology will not yield equivalent performance. For example, consider the condition where both inputs of common single-supply op amps are

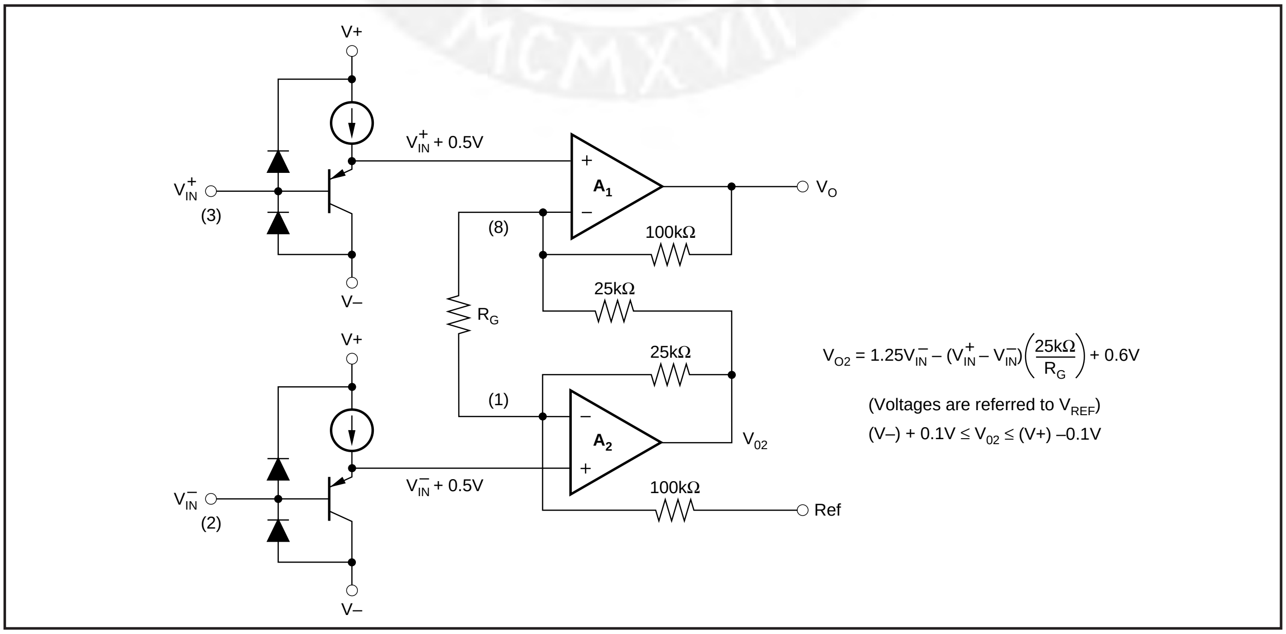


FIGURE 4. INA122 Simplified Circuit Diagram.

equal to 0V. The outputs of both A_1 and A_2 must be 0V. But any small positive voltage applied to V_{IN}^+ requires that A_2's output must swing below 0V, which is clearly impossible without a negative power supply.

To achieve common-mode range that extends to single-supply ground, the INA122 uses precision level-shifting buffers on its inputs. This shifts both inputs by approximately +0.5V, and through the feedback network, shifts A_2's output by approximately +0.6V. With both inputs and V_{REF} at single-supply, A_2's output is well within its linear range. A positive V_{IN}^+ causes A_2's output to swing below 0.6V.

As a result of this input level-shifting, the voltages at pin 1 and pin 8 are not equal to their respective input terminal voltages (pins 2 and 3). For most applications, this is not important since only the gain-setting resistor connects to these pins.

LOW VOLTAGE OPERATION

The INA122 can be operated on a single power supply as low as +2.2V (or a total of +2.2V on dual supplies). Performance remains excellent throughout the power supply range up to +36V (or ±18V). Most parameters vary only slightly throughout this supply voltage range—see typical performance curves.

Operation at very low supply voltage requires careful attention to ensure that the common-mode voltage remains within its linear range.

LOW QUIESCENT CURRENT OPERATION

The INA122 maintains its low quiescent current (60µA) while the output is within linear operation (up to 200mV from the supply rails). When the input creates a condition that overdrives the output into saturation, quiescent current increases. With V_O overdriven into the positive rail, the quiescent current increases to approximately 400µA. Likewise, with V_O overdriven into the negative rail (single supply ground) the quiescent current increases to approximately 200µA.

OUTPUT CURRENT RANGE

Output sourcing and sinking current values versus the output voltage ranges are shown in the typical performance curves. The positive and negative current limits are not equal. Positive output current sourcing will drive moderate to high load impedances. Battery operation normally requires the careful management of power consumption to keep load impedances very high throughout the design.

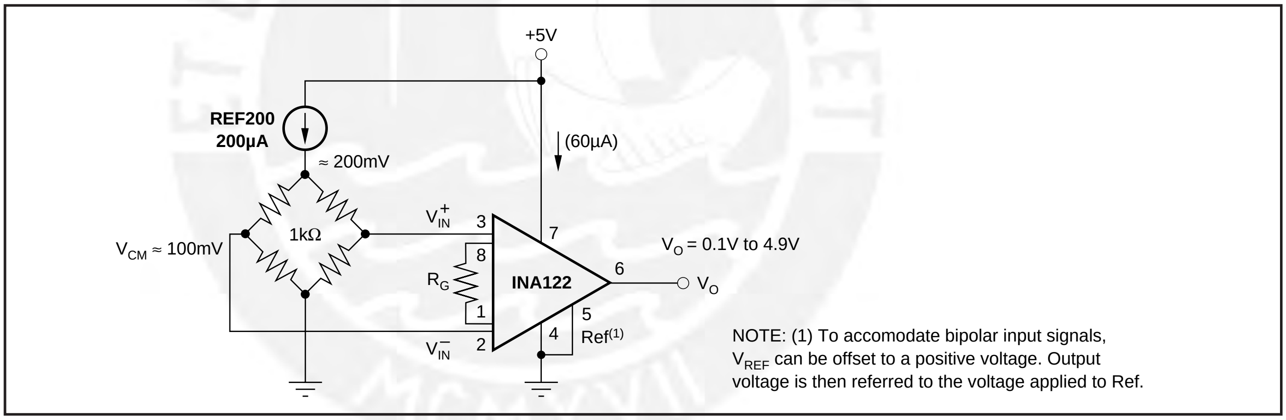


FIGURE 5. Micropower Single Supply Bridge Amplifier.

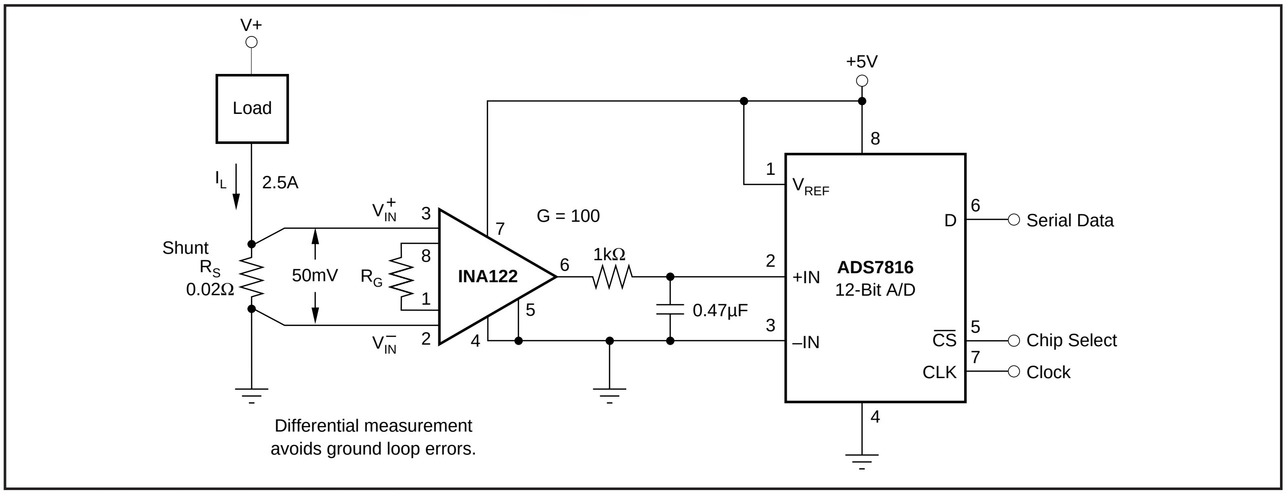


FIGURE 6. Single-Supply Current Shunt Measurement.

SGS-THOMSON MICROELECTRONICS

UA741

GENERAL PURPOSE SINGLE OPERATIONAL AMPLIFIER

- LARGE INPUT VOLTAGE RANGE
- NO LATCH-UP
- HIGH GAIN
- SHORT-CIRCUIT PROTECTION
- NO FREQUENCY COMPENSATION REQUIRED
- SAME PIN CONFIGURATION AS THE UA709

N
DIP8
(Plastic Package)

D
SO8
(Plastic Micropackage)

DESCRIPTION

The UA741 is a high performance monolithic operational amplifier constructed on a single silicon chip. It is intented for a wide range of analog applications.

- Summing amplifier
- Voltage follower
- Integrator
- Active filter
- Function generator

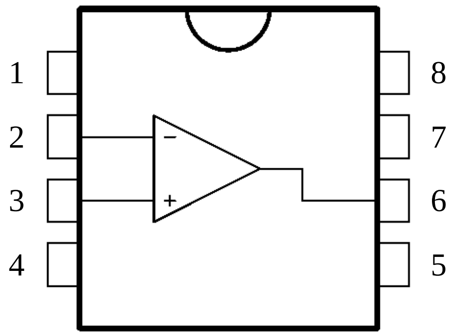
The high gain and wide range of operating voltages provide superior performances in integrator, summing amplifier and general feedback applications. The internal compensation network (6dB/octave) insures stability in closed loop circuits.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
UA741C	0°C, +70°C	•	•
UA741I	-40°C, +105°C	•	•
UA741M	-55°C, +125°C	•	•

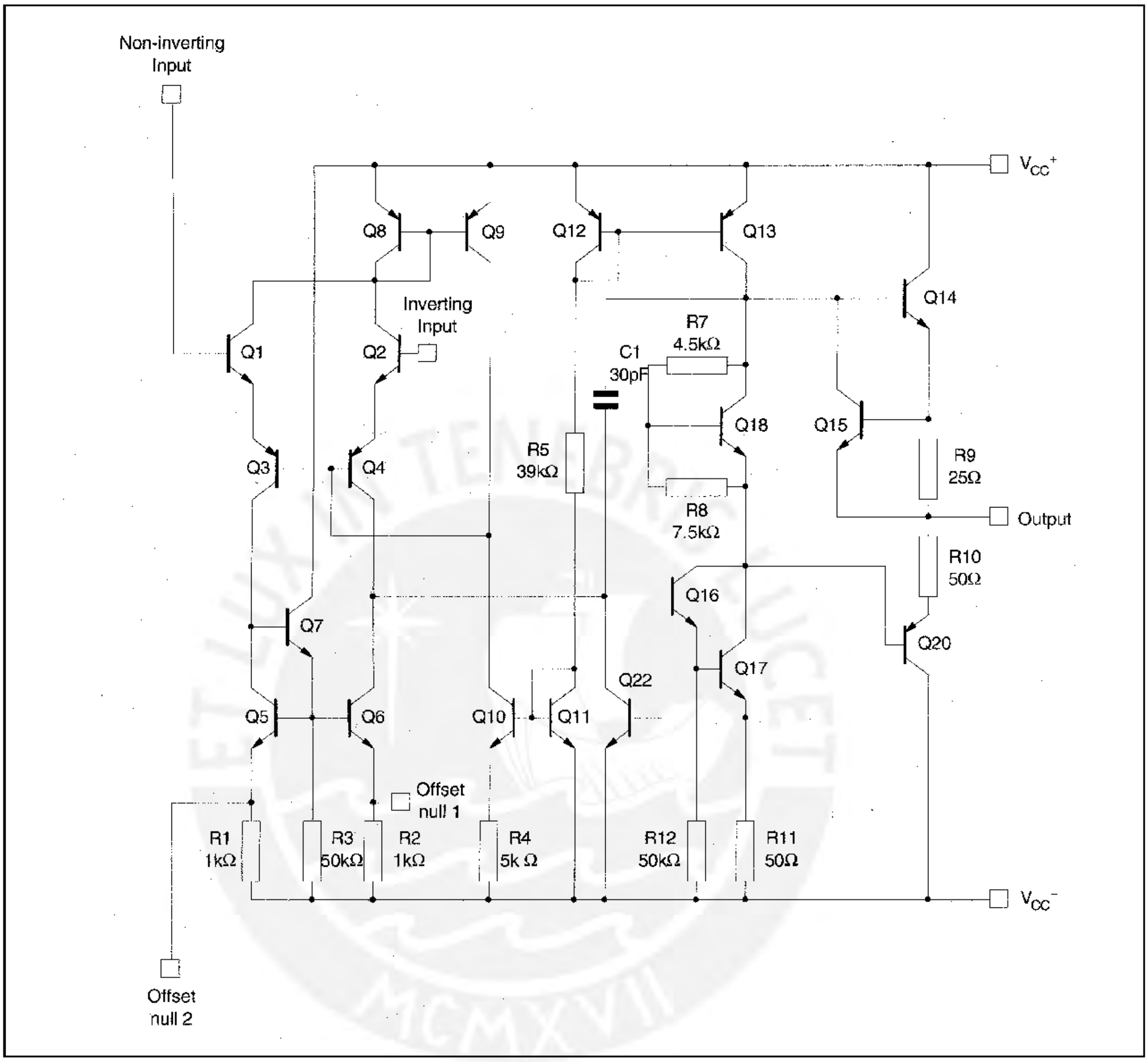
Example : UA741CN

PIN CONNECTIONS (top view)



1 - Offset null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^{-}
5 - Offset null 2
6 - Output
7 - V_{CC}^{+}
8 - N.C.

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

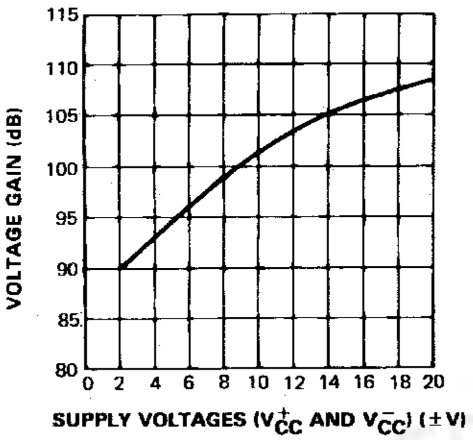
Symbol	Parameter	UA741M	UA741I	UA741C	Unit
V_{cc}	Supply Voltage		±22		V
V_{id}	Differential Input Voltage		±30		V
V_i	Input Voltage		±15		V
P_{tot}	Power Dissipation		500		mW
	Output Short-circuit Duration		Infinite		
T_{oper}	Operating Free Air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to +150	-65 to +150	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15V$, $T_{amb} = +25^oC$ (unless otherwise specified)

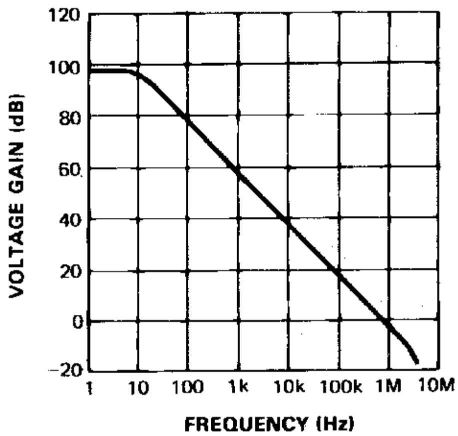
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage ($R_S \leq 10k\Omega$) $T_{amb} = +25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$		1	5 6	mV
I_{io}	Input Offset Current $T_{amb} = +25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$		2	30 70	nA
I_{ib}	Input Bias Current $T_{amb} = +25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$		10	100 200	nA
A_{vd}	Large Signal Voltage Gain * (V_O ±10V, $R_L = 2k\Omega$) $T_{amb} = +25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$	50 25	200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_S \leq 10k\Omega$) $T_{amb} = +25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$	77 77	90		dB
I_{CC}	Supply Current, no load $T_{amb} = +25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$		1.7	2.8 3.3	mA
V_{icm}	Input Common Mode Voltage Range $T_{amb} = +25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$	±12 ±12			V
CMR	Common-mode Rejection Ratio ($R_S \leq 10k\Omega$) $T_{amb} = +25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$	70 70	90		dB
I_{OS}	Output Short-circuit Current	10	25	40	mA
$\pm V_{OPP}$	Output Voltage Swing $T_{amb} = +25^oC$ $R_L = 10k\Omega$ $R_L = 2k\Omega$ $T_{min.} \leq T_{amb} \leq T_{max.}$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	12 10 12 10	14 13		V
SR	Slew Rate (V_i = ±10V, $R_L = 2k\Omega$, C_L= 100pF, $T_{amb} = 25^oC$, unity gain)	0.25	0.5		V/µs
t_r	Rise Time (V_i = ±20mV, $R_L = 2k\Omega$, C_L = 100pF, $T_{amb} = 25^oC$, unity gain)		0.3		µs
K_{OV}	Overshoot (V_i = 20mV, $R_L = 2k\Omega$, CL = 100pF, $T_{amb} = 25^oC$, unity gain)		5		%
R_I	Input Resistance	0.3	2		MΩ
GBP	Gain Bandwidth Product (V_i = 10mV, $R_L = 2k\Omega$, C_L= 100pF, f = 100kHz)	0.7	1		MHz
THD	Total Harmonic Distortion (f = 1kHz, A_V = 20dB, $R_L = 2k\Omega$, $V_O = 2V_{PP}$, C_L = 100pF, $T_{amb} = 25^oC$)		0.06		%
e_n	Equivalent Input Noise Voltage (f = 1kHz, $R_s = 100\Omega$)		23		$\frac{nV}{\sqrt{Hz}}$
Øm	Phase Margin		50		Degrees

OPEN LOOP VOLTAGE GAIN (Typ.)



741-04.EPS

OPEN LOOP FREQUENCY RESPONSE (Typ.)



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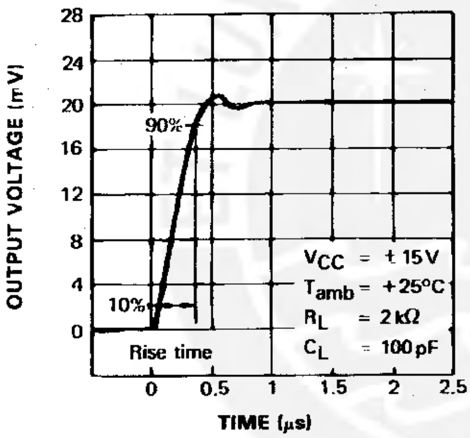
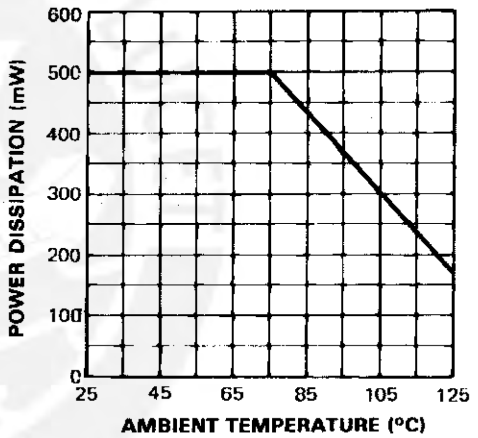
TRANSIENT RESPONSE (Typ.)



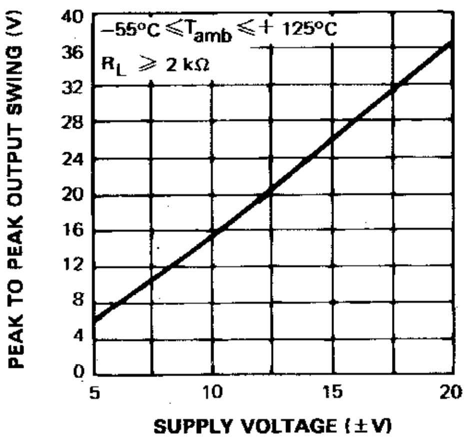
741-06.EPS

ABSOLUTE MAXIMUM POWER DISSIPATION



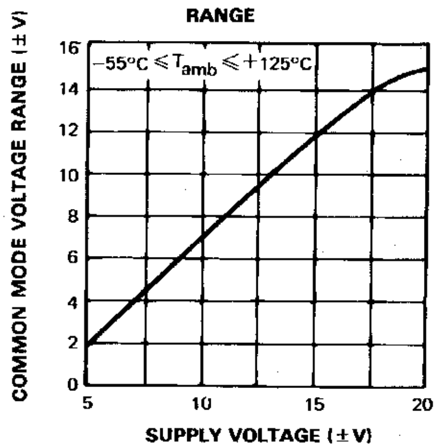
741-07.EPS

OUTPUT VOLTAGE SWING



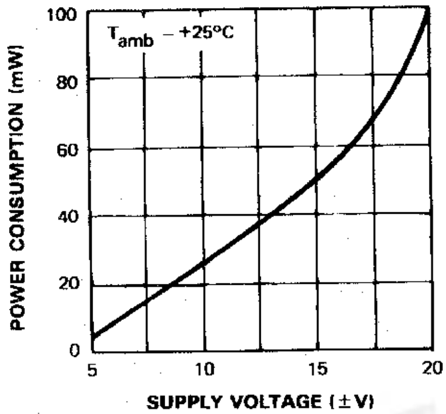
741-08.EPS

INPUT COMMON MODE VOLTAGE RANGE



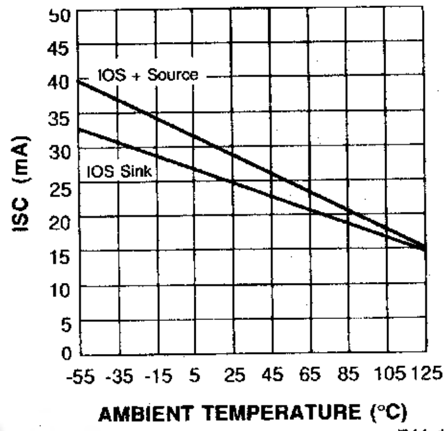
741-09.EPS

POWER CONSUMPTION



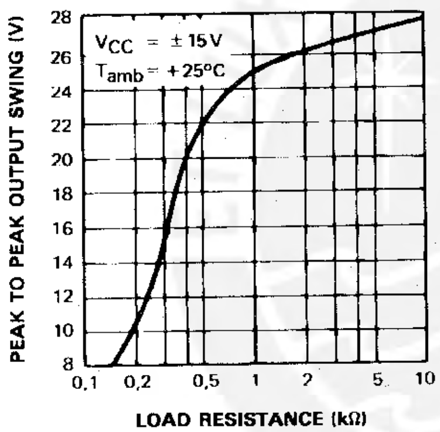
741-10.EPS

OUTPUT CURRENT vs AMBIENT TEMPERATURE



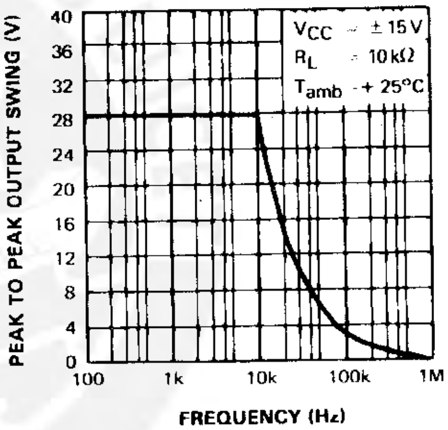
741-11.EPS

OUTPUT VOLTAGE SWING



741-12.EPS

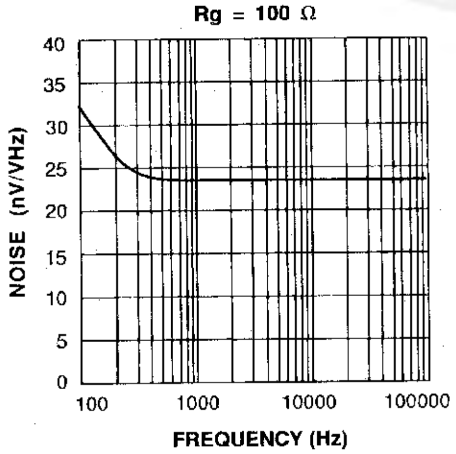
OUTPUT VOLTAGE SWING



741-13.EPS

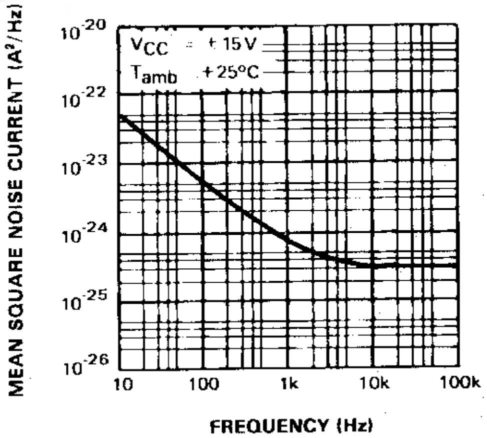
EQUIVALENT INPUT NOISE vs FREQUENCY

Rg = 100 Ω



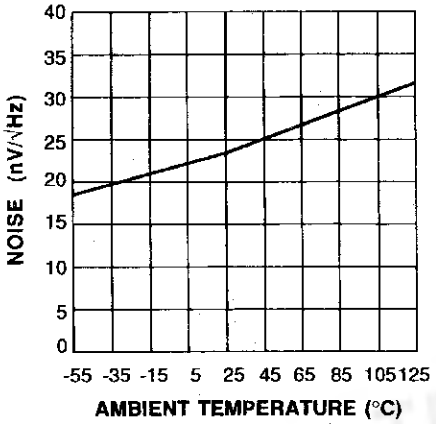
741-14.EPS

INPUT NOISE CURRENT



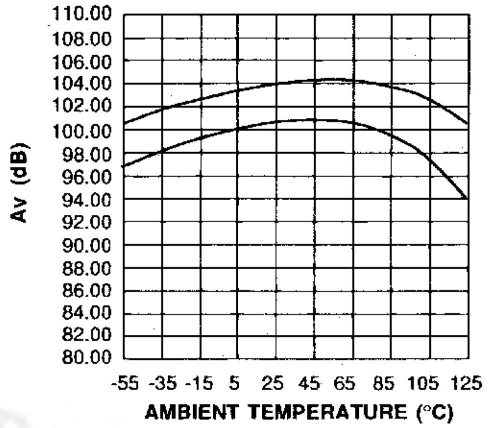
741-15.EPS

EQUIVALENT INPUT NOISE vs AMBIENT TEMPERATURE



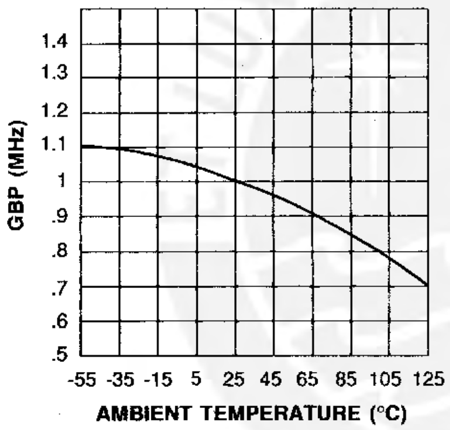
741-16.EPS

LARGE SIGNAL VOLTAGE GAIN vs AMBIENT TEMPERATURE



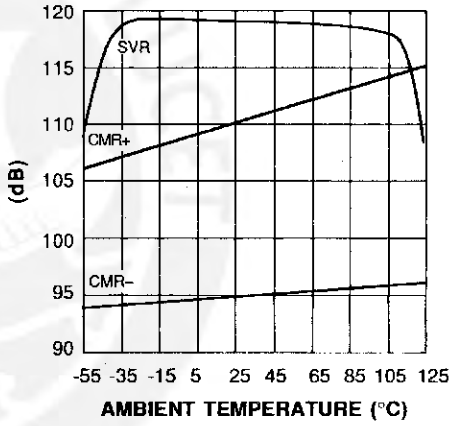
741-17.EPS

GAIN BANDWIDTH PRODUCT vs AMBIENT TEMPERATURE



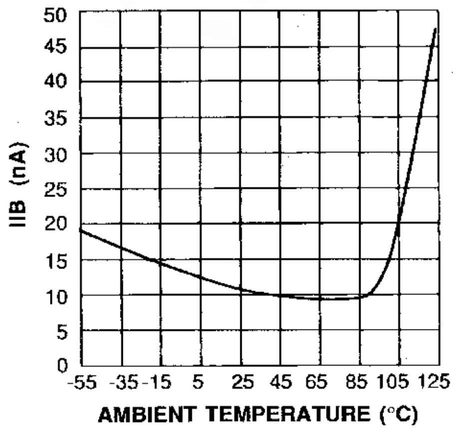
741-18.EPS

POWER SUPPLY & COMMON MODE REJECTION RATIO vs AMBIENT TEMPERATURE



741-19.EPS

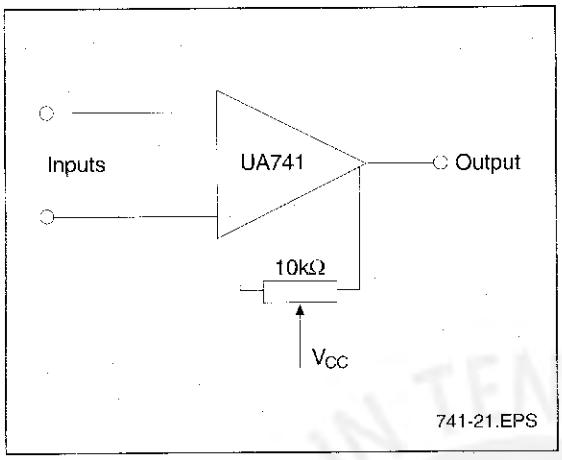
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



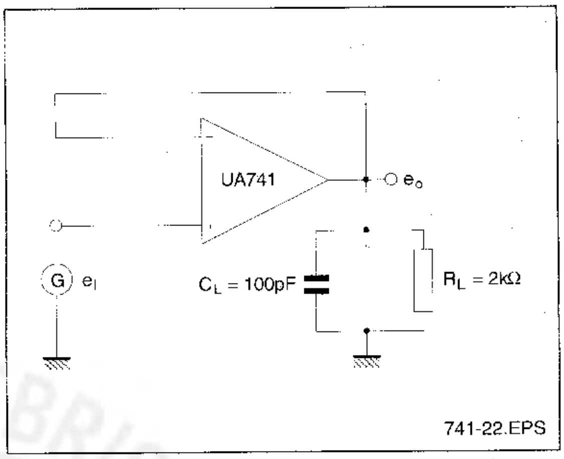
741-20.EPS

MEASUREMENT DIAGRAMS

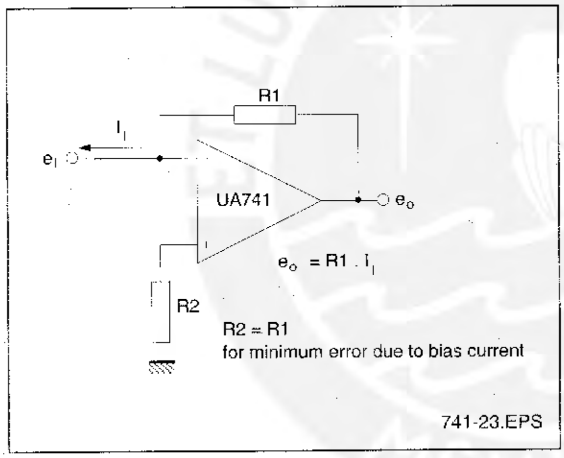
OFFSET VOLTAGE NULL CIRCUIT



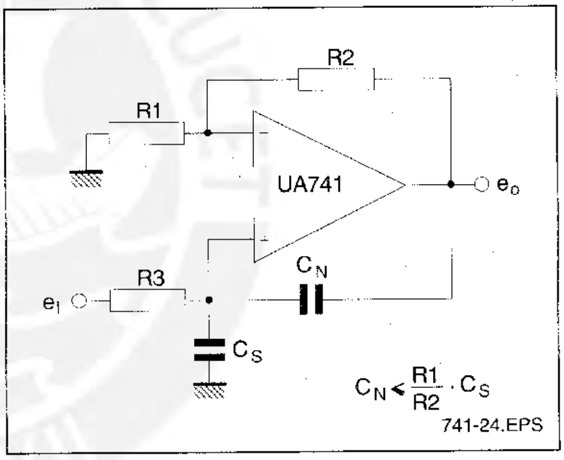
TRANSIENT RESPONSE TEST CIRCUIT



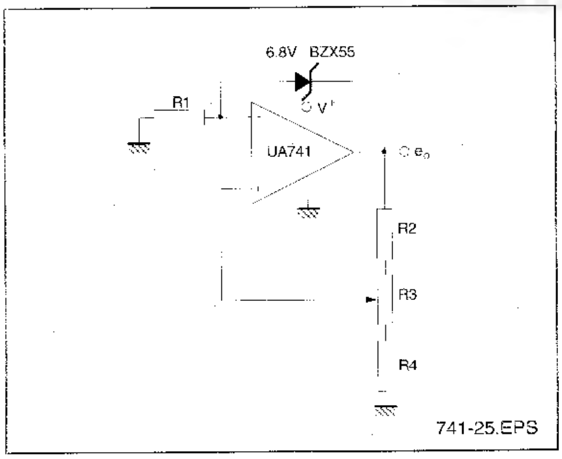
CURRENT TO VOLTAGE CONVERTER



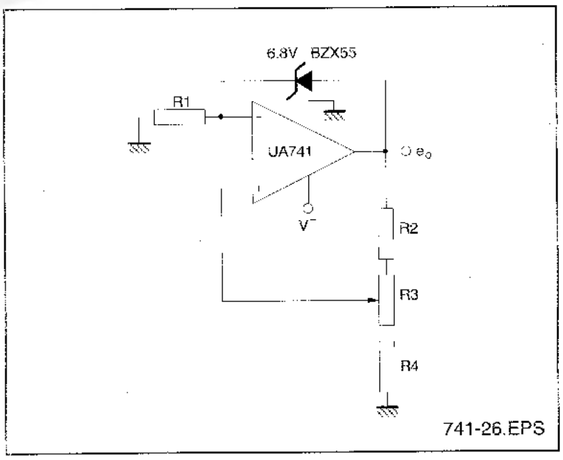
NEUTRALIZING INPUT CAPACITANCE TO OPTIMIZE RESPONSE TIME



POSITIVE VOLTAGE REFERENCE

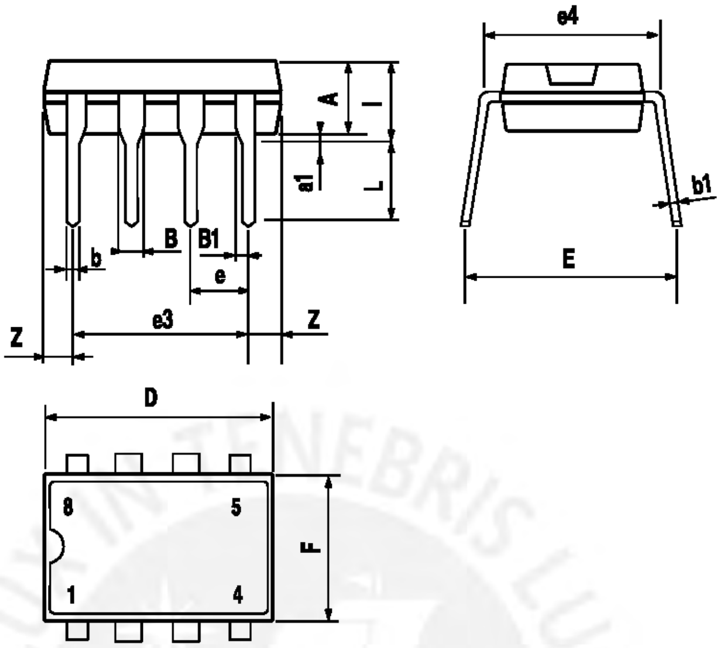


NEGATIVE VOLTAGE REFERENCE



PACKAGE MECHANICAL DATA

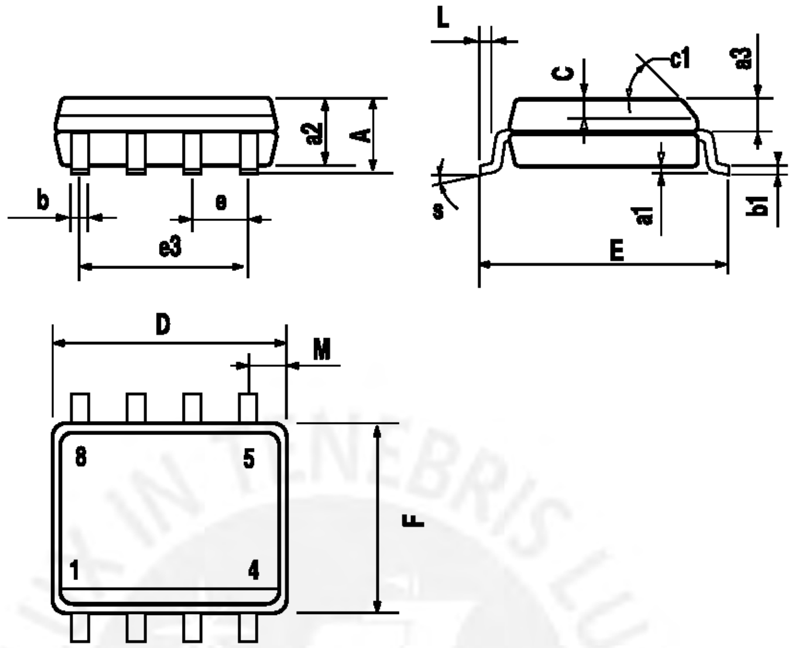
8 PINS - PLASTIC DIP



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC MICROPACKAGE (SO)



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45^{o} (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8^{o} (max.)					

Features

- High-performance, Low-power Atmel®AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 130 Powerful Instructions – Most Single-clock Cycle Execution
  - 32 × 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16MIPS Throughput at 16MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory segments
  - 8Kbytes of In-System Self-programmable Flash program memory
  - 512Bytes EEPROM
  - 1Kbyte Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C[1]
  - Optional Boot Code Section with Independent Lock Bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - Programming Lock for Software Security
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler, one Compare Mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Three PWM Channels
  - 8-channel ADC in TQFP and QFN/MLF package
    Eight Channels 10-bit Accuracy
  - 6-channel ADC in PDIP package
    Six Channels 10-bit Accuracy
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Five Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, and Standby
- I/O and Packages
  - 23 Programmable I/O Lines
  - 28-lead PDIP, 32-lead TQFP, and 32-pad QFN/MLF
- Operating Voltages
  - 2.7V - 5.5V (ATmega8L)
  - 4.5V - 5.5V (ATmega8)
- Speed Grades
  - 0 - 8MHz (ATmega8L)
  - 0 - 16MHz (ATmega8)
- Power Consumption at 4Mhz, 3V, 25°C
  - Active: 3.6mA
  - Idle Mode: 1.0mA
  - Power-down Mode: 0.5µA

8-bit Atmel with 8KBytes In-System Programmable Flash

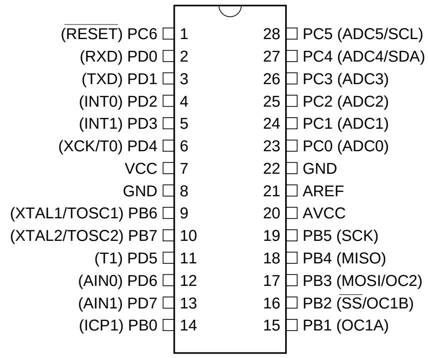
ATmega8 ATmega8L

Summary

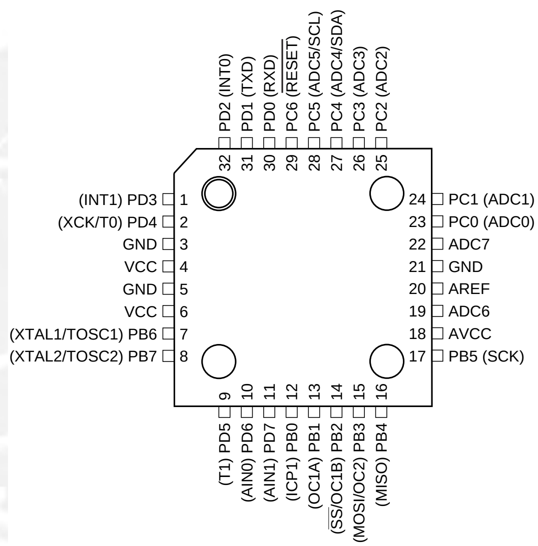
Rev.2486AAS–AVR–02/2013

Pin Configurations

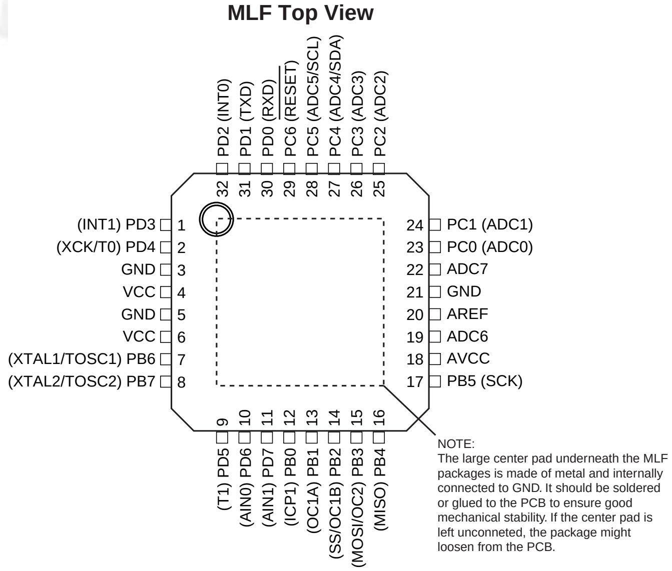
PDIP



TQFP Top View



MLF Top View

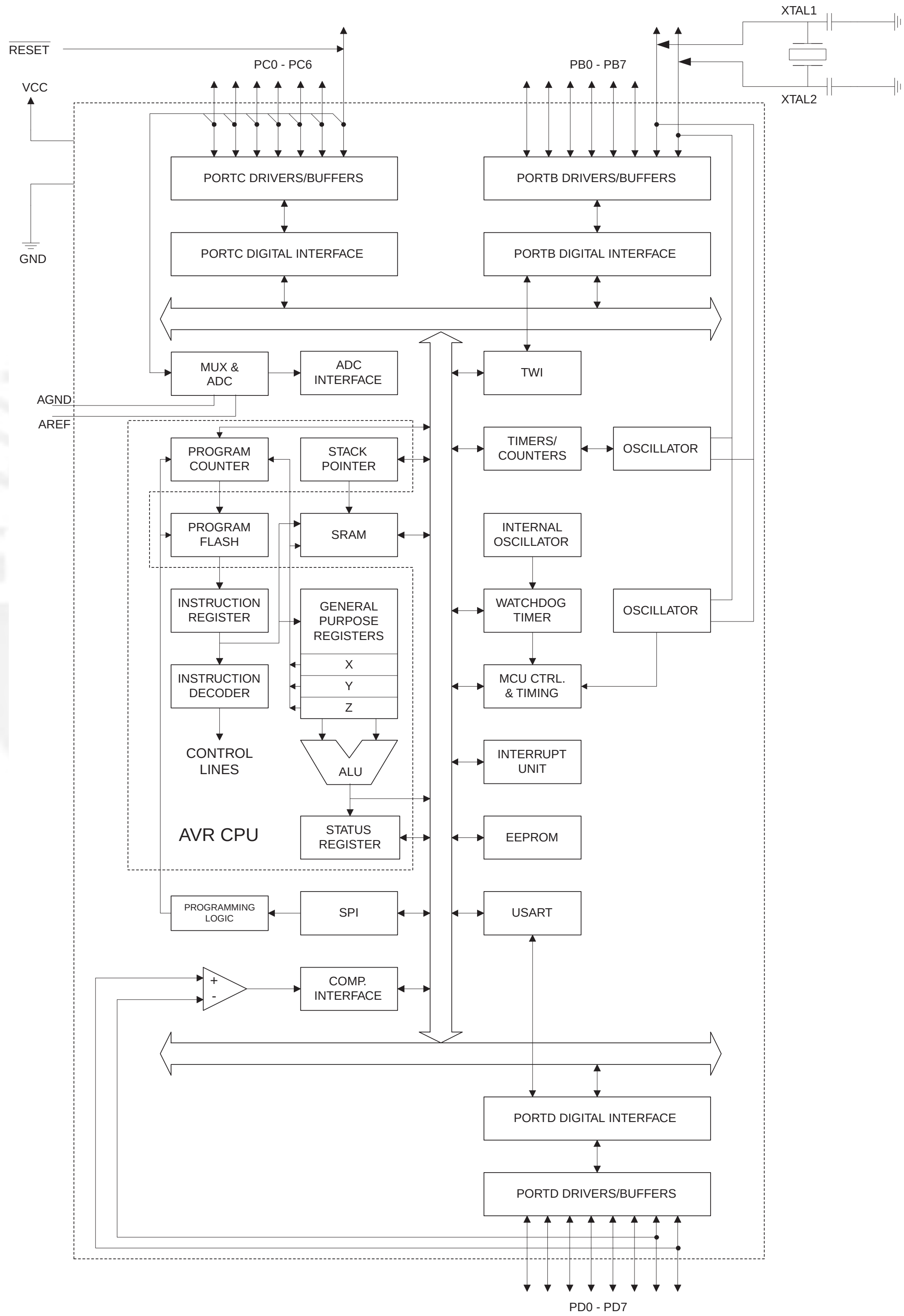


Overview

The Atmel®AVR® ATmega8 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega8 achieves throughputs approaching 1MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed.

Block Diagram

Figure 1. Block Diagram



The Atmel®AVR® core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega8 provides the following features: 8 Kbytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes of EEPROM, 1 Kbyte of SRAM, 23 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, a 6-channel ADC (eight channels in TQFP and QFN/MLF packages) with 10-bit accuracy, a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next Interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The Flash Program memory can be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash Section will continue to run while the Application Flash Section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega8 is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many embedded control applications.

The ATmega8 is supported with a full suite of program and system development tools, including C compilers, macro assemblers, program simulators, and evaluation kits.

Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Minimum and Maximum values will be available after the device is characterized.

Pin Descriptions

VCC Digital supply voltage.

GND Ground.

Port B (PB7..PB0) XTAL1/XTAL2/TOSC1/ TOSC2

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Depending on the clock selection fuse settings, PB6 can be used as input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

Depending on the clock selection fuse settings, PB7 can be used as output from the inverting Oscillator amplifier.

If the Internal Calibrated RC Oscillator is used as chip clock source, PB7..6 is used as TOSC2..1 input for the Asynchronous Timer/Counter2 if the AS2 bit in ASSR is set.

The various special features of Port B are elaborated in "Alternate Functions of Port B" on page 58 and "System Clock and Clock Options" on page 25.

Port C (PC5..PC0)

Port C is an 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

PC6/$\overline{\text{RESET}}$

If the RSTDISBL Fuse is programmed, PC6 is used as an I/O pin. Note that the electrical characteristics of PC6 differ from those of the other pins of Port C.

If the RSTDISBL Fuse is unprogrammed, PC6 is used as a Reset input. A low level on this pin for longer than the minimum pulse length will generate a Reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 38. Shorter pulses are not guaranteed to generate a Reset.

The various special features of Port C are elaborated on page 61.

Port D (PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega8 as listed on page 63.

$\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 38. Shorter pulses are not guaranteed to generate a reset.

Ordering Information

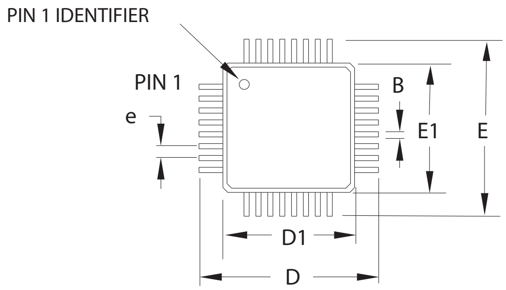
Speed (MHz)	Power Supply (V)	Ordering Code[2]	Package[1]	Operation Range
8	2.7 - 5.5	ATmega8L-8AU ATmega8L-8AUR[3] ATmega8L-8PU ATmega8L-8MU ATmega8L-8MUR[3]	32A 32A 28P3 32M1-A 32M1-A	Industrial (-40°C to 85°C)
16	4.5 - 5.5	ATmega8-16AU ATmega8-16AUR[3] ATmega8-16PU ATmega8-16MU ATmega8-16MUR[3]	32A 32A 28P3 32M1-A 32M1-A	
8	2.7 - 5.5	ATmega8L-8AN ATmega8L-8ANR[3] ATmega8L-8PN ATmega8L-8MN ATmega8L-8MUR[3]	32A 32A 28P3 32M1-A 32M1-A	Industrial (-40°C to 105°C)
16	4.5 - 5.5	ATmega8-16AN ATmega8-16ANR[3] ATmega8-16PN ATmega8-16MN ATmega8-16MUR[3]	32A 32A 28P3 32M1-A 32M1-A	

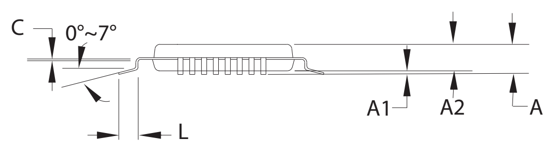
Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green
3. Tape & Reel
4. See characterization specification at 105°C

Package Type	
32A	32-lead, Thin (1.0mm) Plastic Quad Flat Package (TQFP)
28P3	28-lead, 0.300” Wide, Plastic Dual Inline Package (PDIP)
32M1-A	32-pad, 5 × 5 × 1.0 body, Lead Pitch 0.50mm Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

Packaging Information

32A





COMMON DIMENSIONS
(Unit of measure = mm)

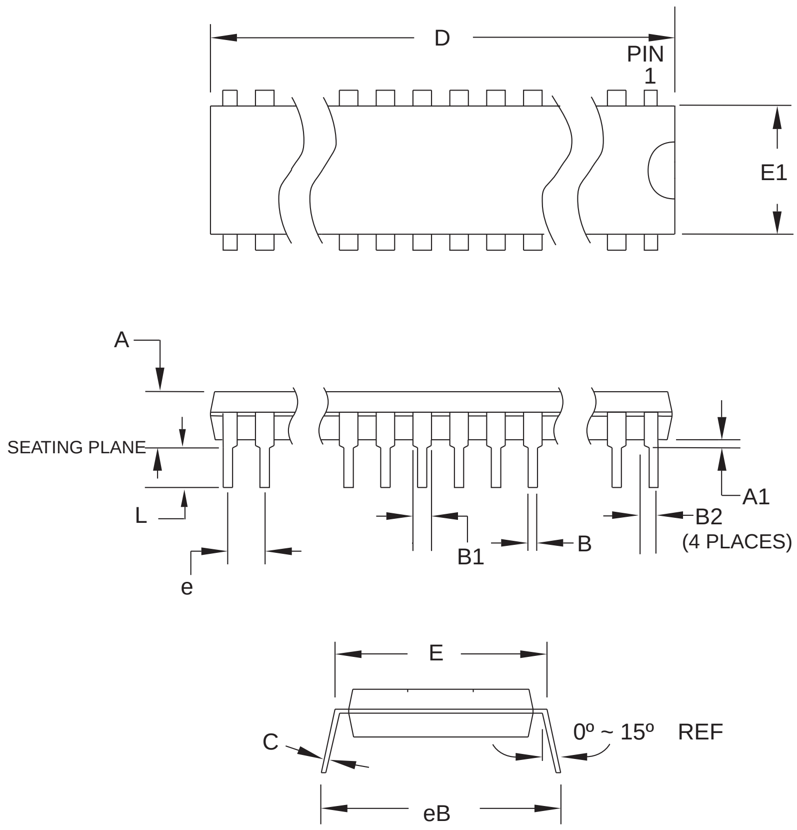
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

2010-10-20

	TITLE	DRAWING NO.	REV.
Atmel	**32A,** 32-lead, 7 x 7mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)	32A	C

28P3



Note: 1. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25mm (0.010").

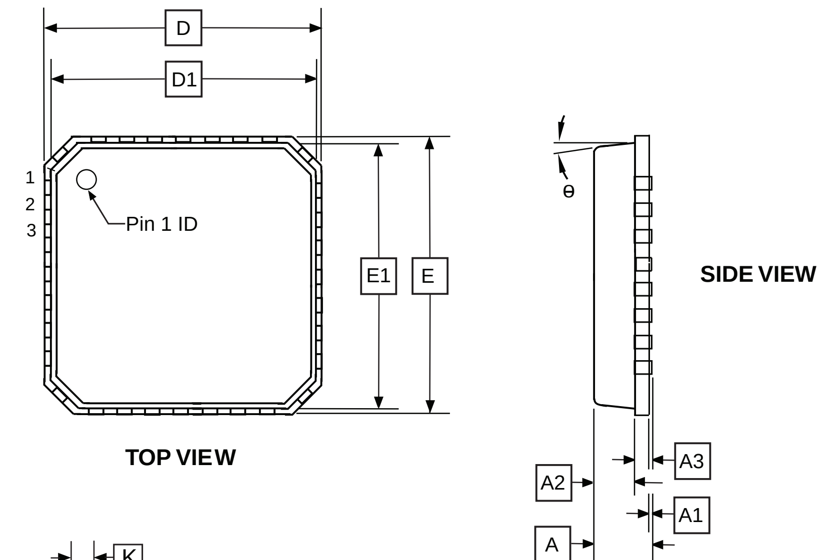
COMMON DIMENSIONS
(Unit of Measure = mm)

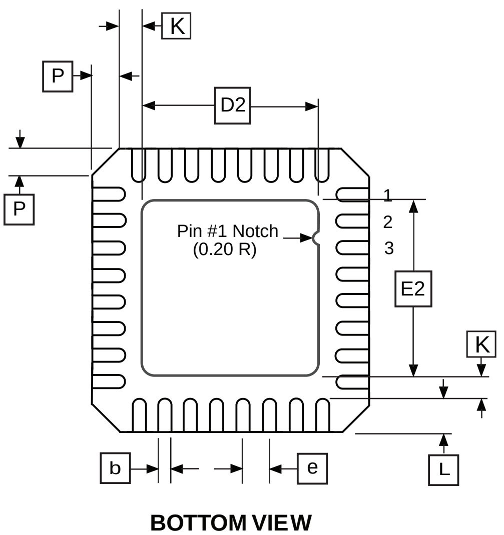
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.5724	
A1	0.508	–	–	
D	34.544	–	34.798	Note 1
E	7.620	–	8.255	
E1	7.112	–	7.493	Note 1
B	0.381	–	0.533	
B1	1.143	–	1.397	
B2	0.762	–	1.143	
L	3.175	–	3.429	
C	0.203	–	0.356	
eB	–	–	10.160	
e	2.540 TYP			

09/28/01

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	**28P3**, 28-lead (0.300"/7.62mm Wide) Plastic Dual Inline Package (PDIP)	28P3	B

32M1-A





COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A2	–	0.65	1.00	
A3		0.20 REF		
b	0.18	0.23	0.30	
D	4.90	5.00	5.10	
D1	4.70	4.75	4.80	
D2	2.95	3.10	3.25	
E	4.90	5.00	5.10	
E1	4.70	4.75	4.80	
E2	2.95	3.10	3.25	
e		0.50 BSC		
L	0.30	0.40	0.50	
P	–	–	0.60	
θ	–	–	12^{o}	
K	0.20	–	–	

Note: JEDEC Standard MO-220, Fig. 2 (Anvil Singulation), VHHD-2.

5/25/06

	TITLE	DRAWING NO.	REV.
ATMEL 2325 Orchard Parkway San Jose, CA 95131	**32M1-A**, 32-pad, 5 x 5 x 1.0mm Body, Lead Pitch 0.50mm, 3.10mm Exposed Pad, Micro Lead Frame Package (MLF)	32M1-A	E

Errata

The revision letter in this section refers to the revision of the ATmega8 device.

ATmega8 Rev. D to I, M

- **First Analog Comparator conversion may be delayed**
- **Interrupts may be lost when writing the timer registers in the asynchronous timer**
- **Signature may be Erased in Serial Programming Mode**
- **CKOPT Does not Enable Internal Capacitors on XTALn/TOSCn Pins when 32KHz Oscillator is Used to Clock the Asynchronous Timer/Counter2**
- **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request**

1. First Analog Comparator conversion may be delayed

If the device is powered by a slow rising V_{CC}, the first Analog Comparator conversion will take longer than expected on some devices.

Problem Fix / Workaround

When the device has been powered or reset, disable then enable theAnalog Comparator before the first conversion.

2. Interrupts may be lost when writing the timer registers in the asynchronous timer

The interrupt will be lost if a timer register that is synchronized to the asynchronous timer clock is written when the asynchronous Timer/Counter register(TCNTx) is 0x00.

Problem Fix / Workaround

Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register(TCCRx), asynchronous Timer Counter Register(TCNTx), or asynchronous Output Compare Register(OCRx).

3. Signature may be Erased in Serial Programming Mode

If the signature bytes are read before a chiperase command is completed, the signature may be erased causing the device ID and calibration bytes to disappear. This is critical, especially, if the part is running on internal RC oscillator.

Problem Fix / Workaround:

Ensure that the chiperase command has exceeded before applying the next command.

4. CKOPT Does not Enable Internal Capacitors on XTALn/TOSCn Pins when 32KHz Oscillator is Used to Clock the Asynchronous Timer/Counter2

When the internal RC Oscillator is used as the main clock source, it is possible to run the Timer/Counter2 asynchronously by connecting a 32KHz Oscillator between XTAL1/TOSC1 and XTAL2/TOSC2. But when the internal RC Oscillator is selected as the main clock source, the CKOPT Fuse does not control the internal capacitors on XTAL1/TOSC1 and XTAL2/TOSC2. As long as there are no capacitors connected to XTAL1/TOSC1 and XTAL2/TOSC2, safe operation of the Oscillator is not guaranteed.

Problem Fix / Workaround

Use external capacitors in the range of 20pF - 36pF on XTAL1/TOSC1 and XTAL2/TOSC2. This will be fixed in ATmega8 Rev. G where the CKOPT Fuse will control internal capacitors also when internal RC Oscillator is selected as main clock source. For ATmega8 Rev. G, CKOPT = 0 (programmed) will enable the internal capacitors on XTAL1 and XTAL2. Customers who want compatibility between Rev. G and older revisions, must ensure that CKOPT is unprogrammed (CKOPT = 1).

5. **Reading EEPROM by using ST or STS to set EERE bit triggers unexpected interrupt request.**

   Reading EEPROM by using the ST or STS command to set the EERE bit in the EECR register triggers an unexpected EEPROM interrupt request.

   Problem Fix / Workaround

   Always use OUT or SBI to set EERE in EECR.

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Fax: (+81) (3) 6417-0370

Sistema de medición de fuerza para Módulo de Transmisibilidad

Programa Principal de uC

```
; ****************************************************
; Sistema envia paquetes de 12 en 12 (Lee, almacena, tx 12)
; aceleracion con rango de 1.5g
; ****************************************************

.include "C:\VMLAB\include\m8def.inc"

; Define here the variables
;
.def  temp  =r16

; Define here Reset and interrupt vectors, if any
;
reset:
   rjmp start
   reti      ; Addr $01
   reti      ; Addr $02
   reti      ; Addr $03
   reti      ; Addr $04
   rjmp MidePeriodo; Addr $05       Interrupción por captura de entrada   ;;;;;
   reti      ; Addr $06          Use 'rjmp myVector'
   reti      ; Addr $07          to define a interrupt vector
   reti      ; Addr $08
   reti      ; Addr $09
   reti      ; Addr $0A
```

```
  reti     ; Addr $0B          This is just an example
  reti     ; Addr $0C          Not all MCUs have the same
  reti     ; Addr $0D          number of interrupt vectors
  reti     ; Addr $0E
  reti     ; Addr $0F
  reti     ; Addr $10

.dseg
fuerza1:                .byte 2
fuerza2:                .byte 2
fuerza3:                .byte 2
fuerza4:                .byte 2
aceleracion:    .byte 2
RPS:                    .byte 2
flanco_ant:   .byte 2

.cseg
; Datos para configurar Acelerómetro
CONFIG_ACEL:
;POWER_CTL -00-link=0autosleep=1measurement=0(standby)sleep=0wakeup=00
.db 0b00101101,0b00000000          ; db 0x2D,0x00
;DATA_FORMAT selftest=0 SPI=0(4-wire)-00-Fullres=1 justify=0 range=01(3g)
.db 0b00110001,0b00001000          ; db 0x31,0x09
;FIFO_CTL fifomode=00trigger=0samples=00000
.db 0b00111000,0b00000000          ; db 0x38,0x00
;BW_RATE -000-lowpower=0rate=1111(3200Hz)
.db 0b00101100,0b00001111          ; db 0x2C,0x0D
;THRESH ACT
.db 0b00100100,0b00000000          ; db 0x24,0x00
```

```
;THRESH_INACT
.db 0b00100101,0b00000000        ; db 0x25,0x00
;TIME_INACT
.db 0b00100110,0b00000000        ; db 0x26,0x00
;ACT_INACT_CTL
.db 0b00100111,0b00000000        ; db 0x27,0x00
;INT_ENABLE
.db 0b00101110,0b00000000        ; db 0x2E,0x00
;INT_MAP
.db 0b00101111,0b00000000        ; db 0x2F,0x00
;Offset X = 0
.db 0b00011110,0b00000000        ; db 0x1E,0x00
;Offset Y = 0
.db 0b00011111,0b00000000        ; db 0x1F,0x00
;Offset Z = 0
.db 0b00100000,0b00000000        ; db 0x20,0x00
;POWER_CTL -00-link=0autosleep=0measuremnt=1sleep=0wakeup=00
.db 0b00101101,0b00001000        ; db 0x2D,0x04


; Program starts here after Reset


start:
        ldi         R16,high(RAMEND)
        out         SPH,R16
        ldi         R16,low(RAMEND)
        out         SPL,R16

        rcall       IniPorts
```

```
        rcall           IniSerial
        rcall           IniTimer1
        rcall   IniSPI
        rcall           ConfigAcelerometro
        rcall   IniADC
        rcall           IniVariables

  cli
lazo:
  clr   R17
  clr   R18
        rcall   RxDato
        cpi     R16,'W'   ; recibe caracter de inicio
        brne            lazo


sensa:

  rcall           MideFuerza1
  rcall   MideFuerza2
  rcall   MideFuerza3
  rcall   MideFuerza4
  rcall   MideAcel
  cli
  rcall           TxVariables
  sei


loop:
```

```
        inc     R17
        cpi     R17,200   ; muestras
                brne            sensa

        inc     R18
        cpi     R18,4
        breq    lazo
        clr     R17
  rjmp    sensa


;*********************************************************************************
;*********************************************************************************
;*********************************************************************************

;*****Subrutinas*****
;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
IniPorts:
        push            R16

        ldi             R16,0b00101100     ; salidas: SCK,MOSI,SS  entradas: MISO,ICP1
        out             DDRB,R16

        pop             R16
        ret
;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
IniSerial:          ;38400,8,n,1
```

```
        push        R16

        ldi         R16,$00
        out         UBRRH,R16
        ldi         R16,$0C
        out         UBRRL,R16
        ldi         R16,$02
        out         UCSRA,R16
        ldi         R16,$86
        out         UCSRC,R16
        ldi         R16,$18
        out         UCSRB,R16

        pop         R16
        ret
;++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
;++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
IniTimer1:      ; Timer 1 en modo normal, PRE=256, Capturador: flanco de bajada
        push        R16

        ldi         R16,$00
        out         TCCR1A,R16
        ldi         R16,$84   ;
        out         TCCR1B,R16
        ;;;;; ;;;;;;;;;;;;;;;;;;;;;;
  ldi     R16,0B00100000
        out     TIMSK,R16
  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
```

```
        pop             R16
        ret
;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
IniSPI:     ; Configurado a 2 MHz
  push          R16

        ldi             R16,0b01011100      ; SPI master, CPOL=1 CPHA=1 Fosc/8
        out             SPCR, R16       ; MSB of the data word is transmitted first
        ldi             R16,0b00000001      ; SPI2X=1
        out             SPSR, R16

        pop             R16
        ret
;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

ConfigAcelerometro:
  push          R16
        push            R17
        push            R18
        push            ZL
        push            ZH

        ldi             R18,0           ; contador
        ldi             ZH,high(CONFIG_ACEL*2)
        ldi             ZL,low(CONFIG_ACEL*2)

configacel:
```

```
	lpm		R16,Z+
  lpm		R17,Z+
	rcall	Tx_SPI
  inc		R18
	cpi		R18,14		; fin de transmision
	brne		configacel

	pop		ZH
	pop		ZL
	pop		R18
	pop		R17
	pop		R16
	ret
;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
Tx_SPI:			; envia por SPI los valores almacenados en r16 y r17
	cbi		PORTB,2		; SS = 0
	out		SPDR, R16		; se envia por el SPI
Tx_SPI_espera1:
	sbis		SPSR, SPIF			; Se espera a que se termine la transmision
	rjmp		Tx_SPI_espera1
	out		SPDR, R17		; se envia por el SPI
Tx_SPI_espera2:
	sbis		SPSR, SPIF			; Se espera a que se termine la transmision
	rjmp		Tx_SPI_espera2
	sbi		PORTB,2		; SS = 1
	ret
;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
```

```
IniADC:
        push        R16

        ldi         R16,0b10000101      ; ADC habilitado, fosc/32 125kHz 101 ...011 500Khz
        out         ADCSR,R16
        ldi         R16,0b01000000      ; AVCC, ADLAR=0, canal 0
        out         ADMUX,R16

        pop         R16
        ret

;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
IniVariables:           ; borra todas las variables
        push        R16
        push        R17
        push        XL
        push        XH

        clr         R16
        clr         R17
        ldi         XH,high(fuerza1)
        ldi         XL,low(fuerza1)

IniVariables_lazo:
        st                  X+,R16
        inc         R17
        cpi         R17,14
        brne        IniVariables_lazo
```

```
	pop		XH
	pop		XL
	pop	R17
	pop		R16
	ret

;++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
;++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
;++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
;++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
;++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

RxDato:
	sbis		UCSRA,RXC
	rjmp		RxDato
	in			R16,UDR
	ret

TxDato:
	sbis		UCSRA,UDRE
	rjmp		TxDato
	out		UDR,R16
	ret

;++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
;++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
;++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
;------------------------------------------------------------------------------
```

```
;---------------------------------------------------------------------------

MideFuerza1:
        push        R16
        push        R17

        ldi         R16,0b01000000        ; canal 0
        out         ADMUX,R16
        sbi         ADCSR,ADSC      ; inicia conversion
MideFuerza1_espera:
  sbis      ADCSR,ADIF
        rjmp        MideFuerza1_espera
        in                  R16, ADCL
        in                  R17, ADCH
        sts         fuerza1,R17     ; ADCH
        sts         fuerza1+1,R16    ; ADCL
        sbi         ADCSR, ADIF          ; limpia bandera ADIF

        pop         R17
        pop         R16
        ret

MideFuerza2:
        push        R16
        push        R17

        ldi         R16,0b01000001        ; canal 1
        out         ADMUX,R16
        sbi         ADCSR,ADSC      ; inicia conversion
```

```
MideFuerza2_espera:
  sbis          ADCSR,ADIF
        rjmp          MideFuerza2_espera
        in                   R16, ADCL
        in                   R17, ADCH
        sts           fuerza2,R17
        sts           fuerza2+1,R16
        sbi           ADCSR, ADIF        ; limpia bandera ADIF

        pop           R17
        pop           R16
        ret

MideFuerza3:
        push          R16
        push          R17

        ldi           R16,0b01000010       ; canal 2
        out           ADMUX,R16
        sbi           ADCSR,ADSC      ; inicia conversion
MideFuerza3_espera:
  sbis          ADCSR,ADIF
        rjmp          MideFuerza3_espera
        in                   R16, ADCL
        in                   R17, ADCH
        sts           fuerza3,R17
        sts           fuerza3+1,R16
        sbi           ADCSR, ADIF        ; limpia bandera ADIF
```

```
        pop         R17
        pop         R16
        ret

MideFuerza4:
        push        R16
        push        R17

        ldi         R16,0b01000011       ; canal 3
        out         ADMUX,R16
        sbi         ADCSR,ADSC     ; inicia conversion
MideFuerza4_espera:
  sbis        ADCSR,ADIF
        rjmp        MideFuerza4_espera
        in                  R16, ADCL
        in                  R17, ADCH
        sts         fuerza4,R17
        sts         fuerza4+1,R16
        sbi         ADCSR, ADIF       ; limpia bandera ADIF

        pop         R17
        pop         R16
  ret

;-----------------------------------------------------------------------------
;-----------------------------------------------------------------------------

;============================================================================
;============================================================================
```

```
MideAcel:
	push		R16
	push		R17

MideAcel_lazo:
	ldi		R16,$B0
	rcall	Rx_SPI2

	andi		R16,0b00000010
	cpi		R16,0
	breq	MideAcel_lazo

	ldi		R16,$F6	;ID=>$C0   $F6 =>DATA Z0
	rcall	Rx_SPI

	sts		aceleracion,R16	;ZH z1
	sts		aceleracion+1,R17	;ZL z0

	pop	R17
	pop		R16
	ret

Rx_SPI:			; envia por SPI la direccion almacenada en R16 y recibe el dato leido en R16
	cbi		PORTB,2		; SS = 0
	out		SPDR, R16		; se envia por el SPI
Rx_SPI_espera:
	sbis		SPSR, SPIF			; Se espera a que se termine la transmision
	rjmp		Rx_SPI_espera
	out		SPDR, R16		; se envia por el SPI
```

```
Rx_SPI_espera2:
  sbis          SPSR, SPIF            ; Se espera a que se termine la transmision
        rjmp          Rx_SPI_espera2

        in            R17, SPDR     ; se recibe por el SPI
        out           SPDR, R16     ; se envia por el SPI
Rx_SPI_espera3:
        sbis          SPSR, SPIF            ; Se espera a que se termine la transmision
        rjmp          Rx_SPI_espera3

  in            R16, SPDR     ; se recibe por el SPI
        sbi           PORTB,2      ; SS = 1
        ret



Rx_SPI2:            ; envia por SPI la direccion almacenada en R16 y recibe el dato leido en R16
        cbi           PORTB,2      ; SS = 0
        out           SPDR, R16     ; se envia por el SPI
Rx_SPI2_espera:
        sbis          SPSR, SPIF            ; Se espera a que se termine la transmision
        rjmp          Rx_SPI2_espera
        out           SPDR, R16     ; se envia por el SPI
Rx_SPI2_espera2:
  sbis          SPSR, SPIF            ; Se espera a que se termine la transmision
        rjmp          Rx_SPI2_espera2

        in            R16, SPDR     ; se recibe por el SPI
        sbi           PORTB,2      ; SS = 1
        ret
```

```
;===============================================================================
;===============================================================================
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
MidePeriodo:
   push      R16
   in        R16,SREG
   push      R16
   push      XL
   push      XH
   push      YL
   push      YH
   push      ZL
   push      ZH

MidePeriodo_Lazo:              ; mide periodo y lo almacena en X

   in        XL,ICR1L          ; lee el valor capturado
   in        XH,ICR1H

   mov       YL,XL             ; copia el valor a reg Y
   mov       YH,XH

   lds       R16,flanco_ant    ; calcula Periodo XHXL <- (Flanco actual - Flanco anterior)
   sub       XL,R16
   lds       R16,flanco_ant+1
   sbc       XH,R16
   brcs      calcula2
   rjmp      almacena_periodo
```

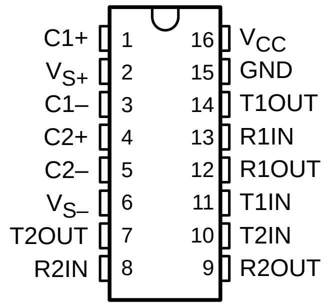
```
calcula2:
   lds      XL,flanco_ant
   lds      XH,flanco_ant+1

   ldi      R16,$FF
   mov      ZL,R16
   mov      ZH,R16
   sub      ZL,XL
   sbc      ZH,XH
   adiw     ZL,1
   clr      R16
   adc      ZH,R16              ;suma 65536=ZHZL+1

   mov      XL,YL               ; copia el valor a reg X
   mov      XH,YH
                        ;suma el( valor actual=YHYl)+65536=XHXL
   add      XL,ZL
   adc      XH,ZH

almacena_periodo:
   sts      flanco_ant,YL       ; Flanco anterior <- Flanco actual
   sts      flanco_ant+1,YH
   inc      R20                 ;bandera de periodo

   cpi      R20,2
   breq     almacena_RPM
   rjmp     mantener_RPM
almacena_RPM:
```

```
    sts         RPS,XH
    sts     RPS+1,XL        ;GUARDO XLXH PORQUE ENVIO XHXL.
    clr     R20

mantener_RPM:
    pop     ZH
    pop     ZL
    pop     YH
    pop     YL
        pop         XH
        pop         XL
    pop     R16
    out     SREG,R16
    pop     R16
    reti
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
TxVariables:
        push        R16
        push    R17
        push        XL
        push        XH

        clr         R17
    ldi         XH,high(fuerza1)
        ldi         XL,low(fuerza1)

TxVariables_lazo:
        ld              R16,X+
```

```
rcall   TxDato
inc         R17
cpi         R17,12
brne        TxVariables_lazo

pop         XH
pop         XL
pop     R17
pop         R16
ret
```

- **Meet or Exceed TIA/EIA-232-F and ITU Recommendation V.28**
- **Operate With Single 5-V Power Supply**
- **Operate Up to 120 kbit/s**
- **Two Drivers and Two Receivers**
- **±30-V Input Levels**
- **Low Supply Current . . . 8 mA Typical**
- **Designed to be Interchangeable With Maxim MAX232**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
- **Applications**
  - **TIA/EIA-232-F**
  - **Battery-Powered Systems**
  - **Terminals**
  - **Modems**
  - **Computers**

MAX232 . . . D, DW, N, OR NS PACKAGE
MAX232I . . . D, DW, OR N PACKAGE
(TOP VIEW)



description/ordering information

The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply EIA-232 voltage levels from a single 5-V supply. Each receiver converts EIA-232 inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V and a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into EIA-232 levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube	MAX232N	MAX232N
	SOIC (D)	Tube	MAX232D	MAX232
		Tape and reel	MAX232DR	
	SOIC (DW)	Tube	MAX232DW	MAX232
		Tape and reel	MAX232DWR	
	SOP (NS)	Tape and reel	MAX232NSR	MAX232
–40°C to 85°C	PDIP (N)	Tube	MAX232IN	MAX232IN
	SOIC (D)	Tube	MAX232ID	MAX232I
		Tape and reel	MAX232IDR	
	SOIC (DW)	Tube	MAX232IDW	MAX232I
		Tape and reel	MAX232IDWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinASIC is a trademark of Texas Instruments.

Function Tables

EACH DRIVER

INPUT TIN	OUTPUT TOUT
L	H
H	L

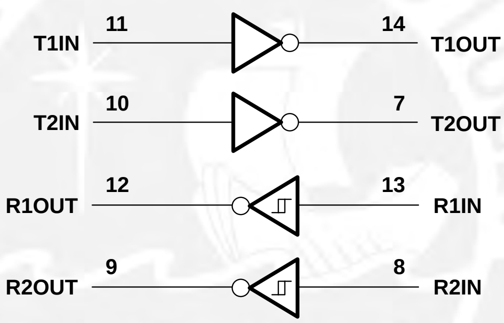
H = high level, L = low level

EACH RECEIVER

INPUT RIN	OUTPUT ROUT
L	H
H	L

H = high level, L = low level

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input supply voltage range, V_{CC} (see Note 1)	–0.3 V to 6 V
Positive output supply voltage range, V_{S+}	V_{CC} – 0.3 V to 15 V
Negative output supply voltage range, $V_{S–}$	–0.3 V to –15 V
Input voltage range, V_I: Driver	–0.3 V to V_{CC} + 0.3 V
Receiver	±30 V
Output voltage range, V_O: T1OUT, T2OUT	$V_{S–}$ – 0.3 V to V_{S+} + 0.3 V
R1OUT, R2OUT	–0.3 V to V_{CC} + 0.3 V
Short-circuit duration: T1OUT, T2OUT	Unlimited
Package thermal impedance, θ_{JA} (see Note 2): D package	73°C/W
DW package	57°C/W
N package	67°C/W
NS package	64°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (T1IN,T2IN)		2			V
V_{IL}	Low-level input voltage (T1IN, T2IN)				0.8	V
R1IN, R2IN	Receiver input voltage				±30	V
T_A	Operating free-air temperature	MAX232	0		70	°C
		MAX232I	–40		85	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 3 and Figure 4)

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5.5 V, All outputs open, T_A = 25°C		8	10	mA

‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTE 3: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 3)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	T1OUT, T2OUT	R_L = 3 kΩ to GND	5	7		V
V_{OL}	Low-level output voltage‡	T1OUT, T2OUT	R_L = 3 kΩ to GND		–7	–5	V
r_o	Output resistance	T1OUT, T2OUT	$V_{S+} = V_{S-}$ = 0, V_O = ±2 V	300			Ω
I_{OS}§	Short-circuit output current	T1OUT, T2OUT	V_{CC} = 5.5 V, V_O = 0		±10		mA
I_{IS}	Short-circuit input current	T1IN, T2IN	V_I = 0			200	µA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
§ Not more than one output should be shorted at a time.
NOTE 3: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Driver slew rate	R_L = 3 kΩ to 7 kΩ, See Figure 2			30	V/µs
SR(t)	Driver transition region slew rate	See Figure 3		3		V/µs
	Data rate	One TOUT switching		120		kbit/s

NOTE 3: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 3)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	R1OUT, R2OUT	I_{OH} = –1 mA	3.5			V
V_{OL}	Low-level output voltage‡	R1OUT, R2OUT	I_{OL} = 3.2 mA			0.4	V
V_{IT+}	Receiver positive-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C		1.7	2.4	V
V_{IT-}	Receiver negative-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V, T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis voltage	R1IN, R2IN	V_{CC} = 5 V	0.2	0.5	1	V
r_i	Receiver input resistance	R1IN, R2IN	V_{CC} = 5, T_A = 25°C	3	5	7	kΩ

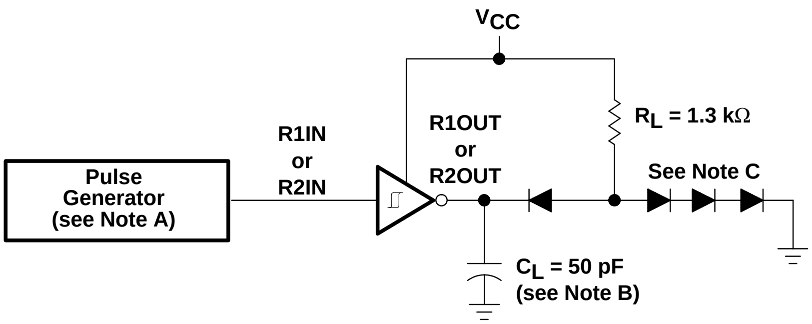
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
NOTE 3: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Note 3 and Figure 1)

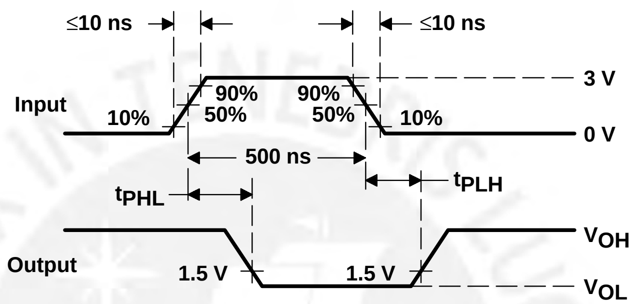
PARAMETER		TYP	UNIT
$t_{PLH(R)}$	Receiver propagation delay time, low- to high-level output	500	ns
$t_{PHL(R)}$	Receiver propagation delay time, high- to low-level output	500	ns

NOTE 3: Test conditions are C1–C4 = 1 µF at V_{CC} = 5 V ± 0.5 V.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

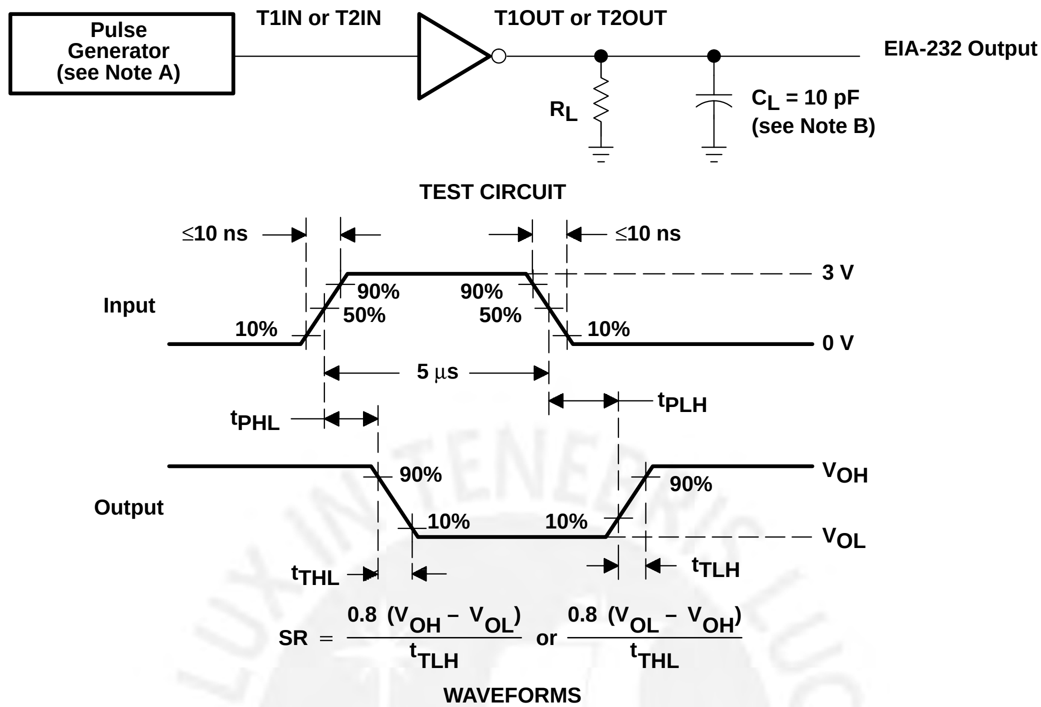


WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

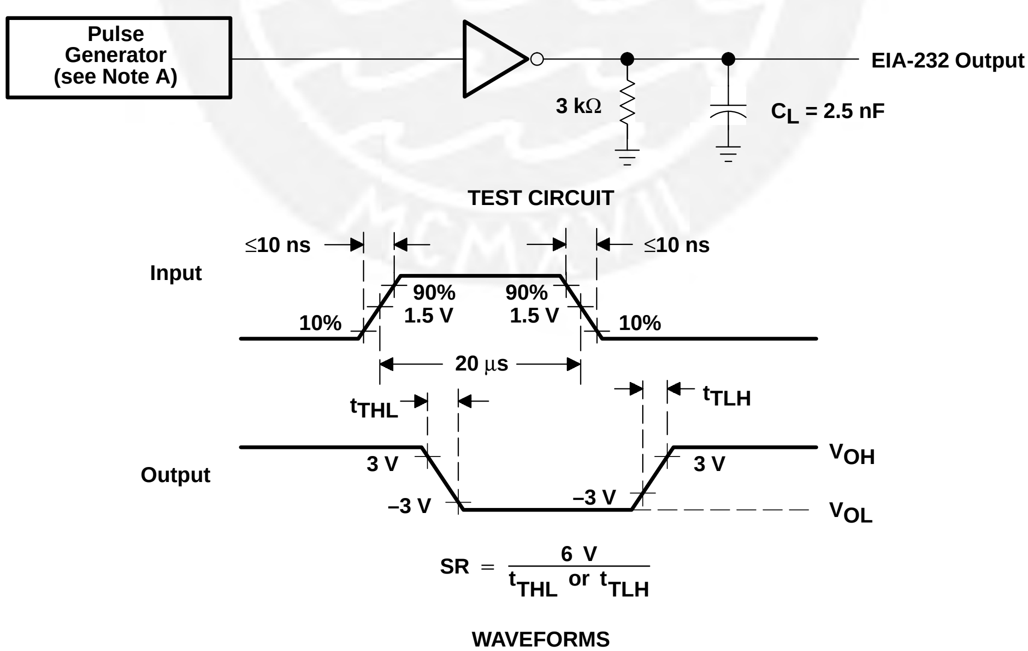
Figure 1. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.

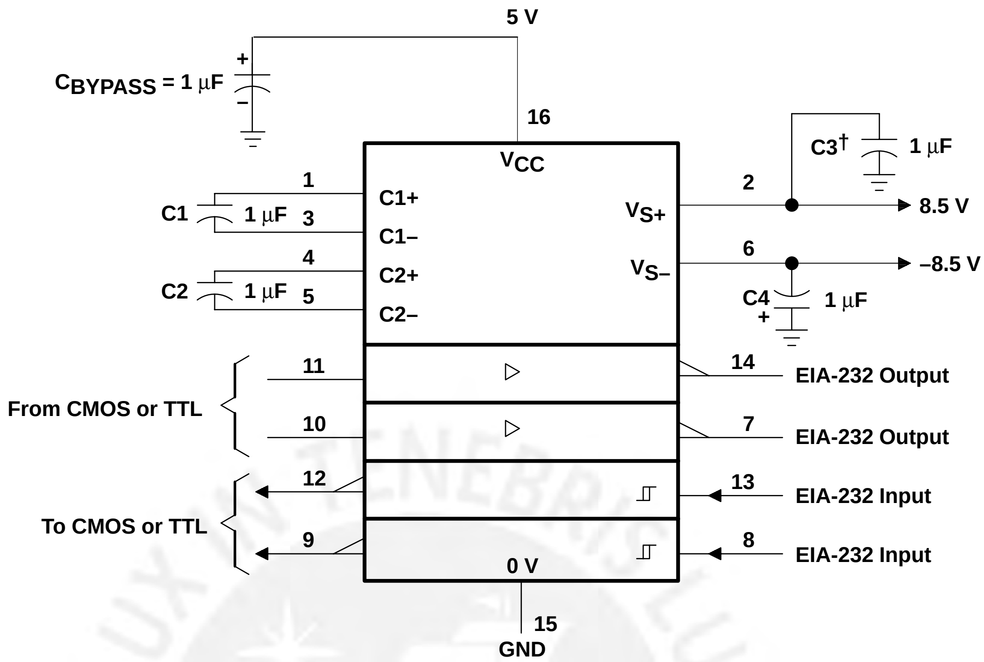
Figure 2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5-µs Input)



NOTE A: The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.

Figure 3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20-µs Input)

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

Figure 4. Typical Operating Circuit

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