

Rx Streaming (Host).vi

Programa principal en el PXI del FFTS basado en la plantilla "Streaming" instalada con los drivers de los modulos FlexRIO. En lugar de procesar las muestras (FFT) en el CPU, envia las muestras mediante un Network Stream hacia el programa del servidor para que estas sean procesadas usando los recursos del GPU Tesla K40c

Rx Streaming

RIO Device
PXI1Slot12

Clock Configuration

Frequency [Hz]
400MHz

LO Frequency [Hz]
400MHz

Reference Level [dBm]
-10dBm

Sample Rate [S/s]
200MS/s

Start Trigger
Software

Number of Samples
1048576

Number of Samples is Finite

Coerced Vertical Range [Vpp]
204.818mV

Buffer del Writer EP
100

Periodo de ADQ en ms
50.000

IP del servidor
192.168.1.2

Envios en cola
0

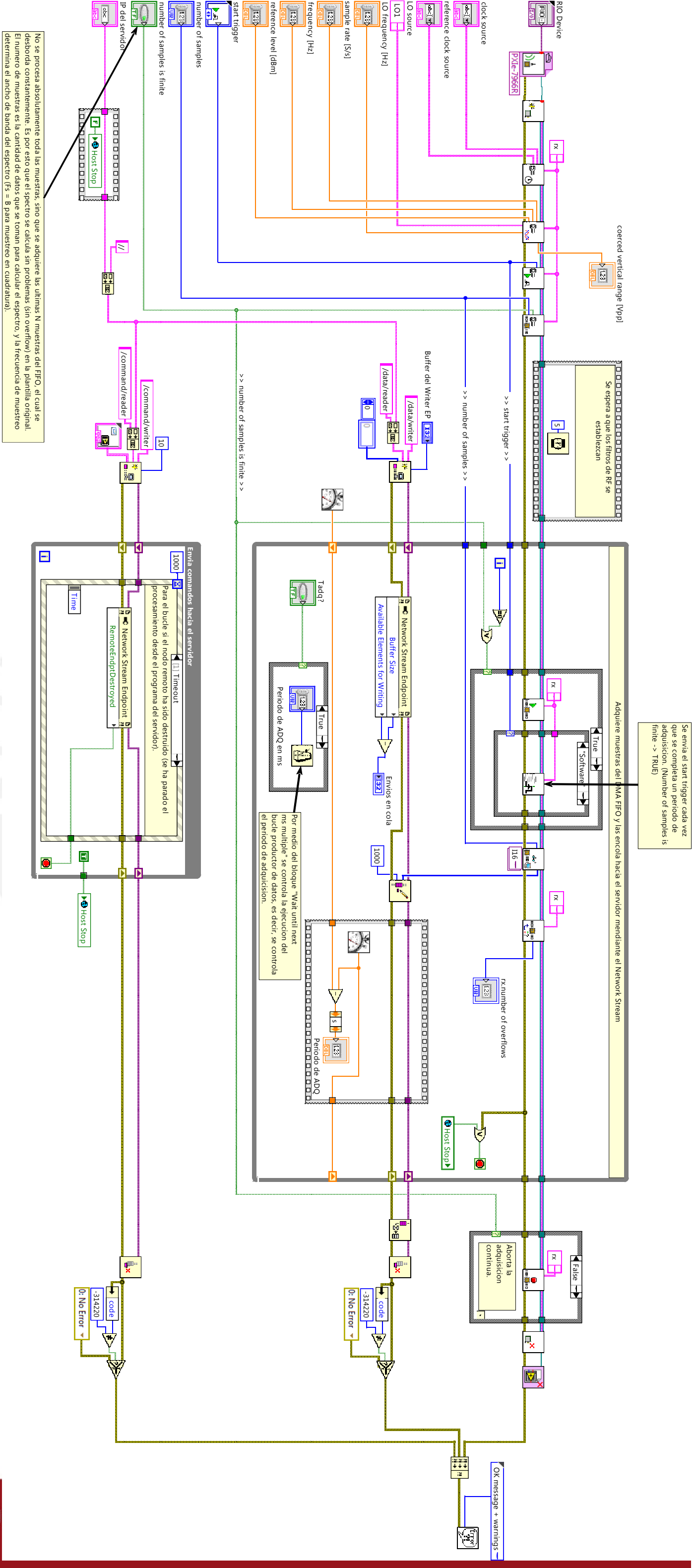
Periodo de ADQ
0.0498912

Tadq?

rx.number of overflows
0

STOP







Streaming Rx (NI 5792) (FPGA).vi

C:\Users\INRAS\Desktop\FlexRIO\FPGA\Streaming Rx (NI 5792) (FPGA).vi

Last modified on 08/02/2017 at 03:19 p.m.

Printed on 08/02/2017 at 03:21 p.m.

Streaming Rx (NI 5792) (FPGA).vi



REGISTER BUS

reg.host read.data 0

reg.reset 0

reg.notify host.go 0

reg.notify host.go rcvd 0

reg.host read.go rcvd 0

Rx Streaming Engine

rx.stream enabled

rx.reset

rx.enable trigger sync

rx.samples to acquire

rx.trigger select

rx.sw trigger

rx.abort

rx.state

rx.samples processed

rx.number of overflows

rx.number of IQ data overflows

Required Controls & Indicators

IO Module\Initialization Done

IO Module\User Error

IO Module\PLL Locked

IO Module\LO Locked

Rx DSP

rx.output sample rate

rx.delay

rx.dsp reset done

rx.frequency shift

rx.phase

rx.impairments

inline gain I

inline gain Q

cross gain I

cross gain Q

pre-gain offset I

pre-gain offset Q

post-gain offset I

post-gain offset Q

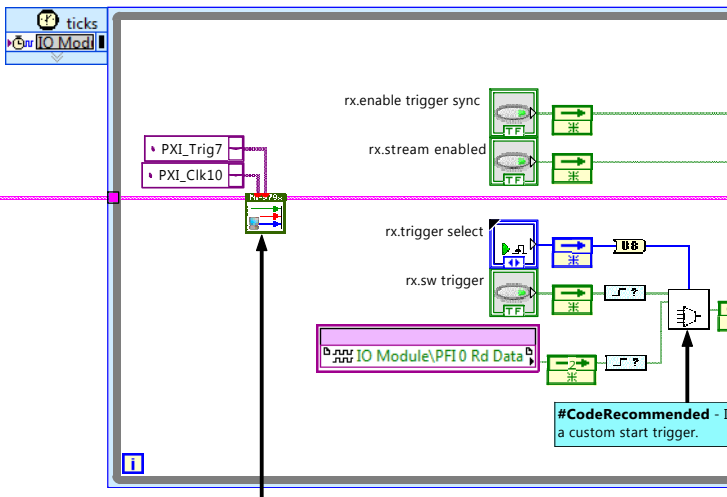
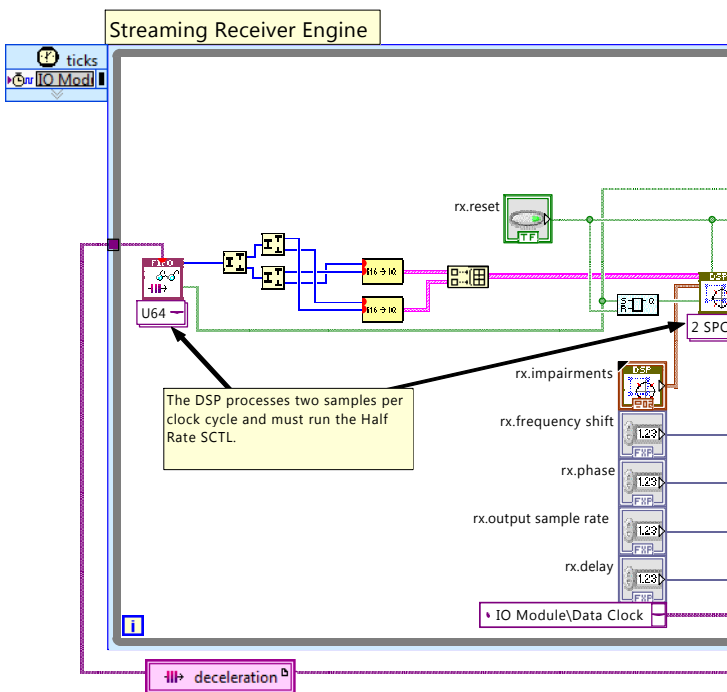
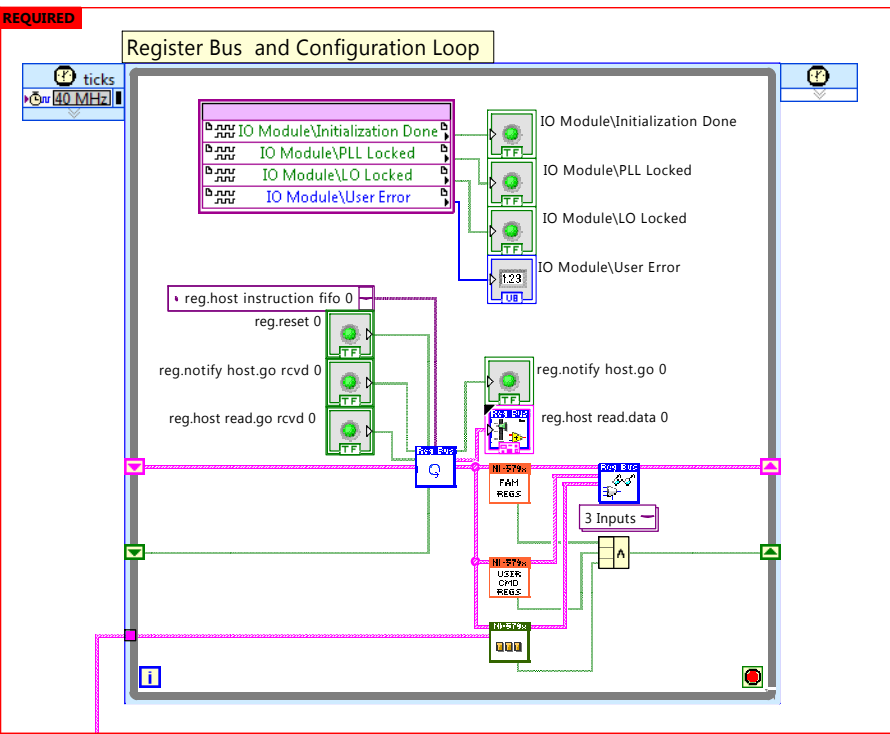


Streaming Rx (NI 5792) (FPGA).vi

C:\Users\INRAS\Desktop\FlexRIO\FPGA\Streaming Rx (NI 5792) (FPGA).vi

Last modified on 08/02/2017 at 03:19 p.m.

Printed on 08/02/2017 at 03:21 p.m.



The Synchronization VIs must run in the Full Rate SCTL to synchronously realize start triggers. DSP VIs cannot run in the Full Rate SCTL due to timing constraints during FPGA compilations. This SCTL handles decelerated from the Full Rate SCTL to the Half Rate SCTL for processing. This SCTL handles transporting the data and associated start trigger.

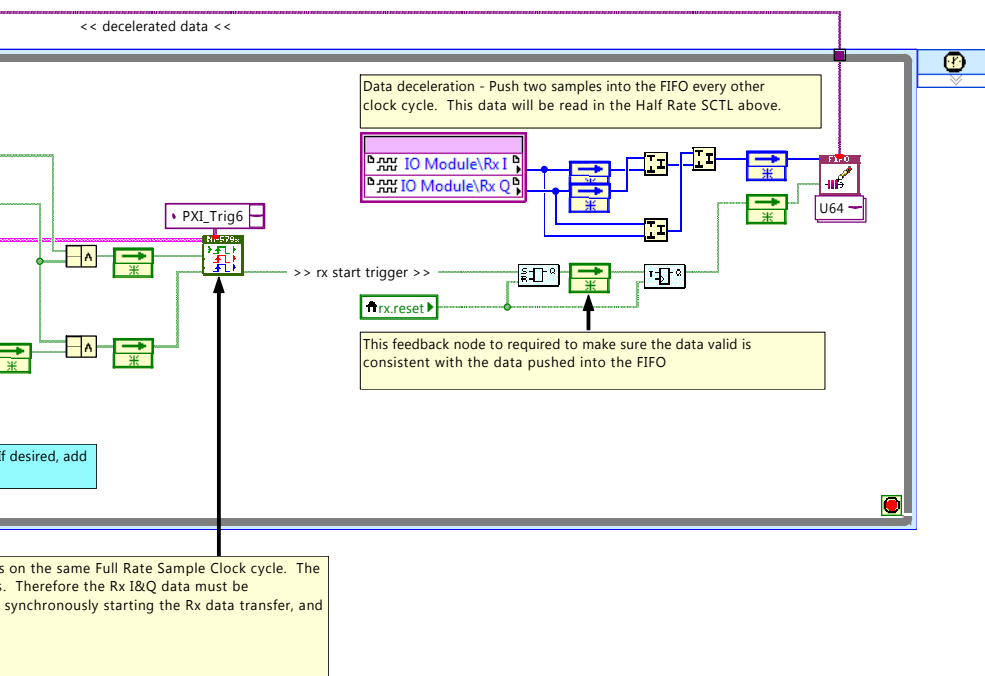
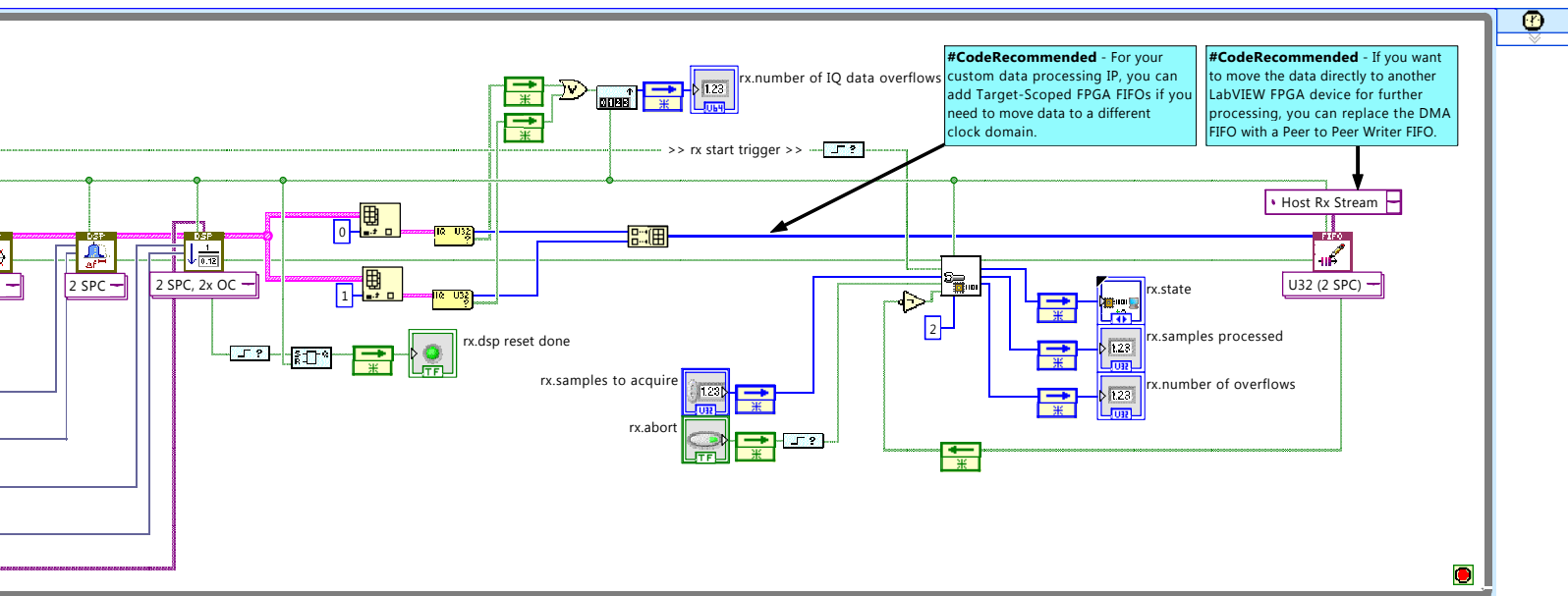


Streaming Rx (NI 5792) (FPGA).vi

C:\Users\INRAS\Desktop\FlexRIO\FPGA\Streaming Rx (NI 5792) (FPGA).vi

Last modified on 08/02/2017 at 03:19 p.m.

Printed on 08/02/2017 at 03:21 p.m.



binshapePFB.vi



Demostración de la tecnica de banco de filtros polifasicos (PFB). El VI muestra la comparación entre respuesta de canal usando FFT directa (sin PFB) y usando un PFB de orden 4.





offset frecuencia

frecuencias N

factor frec

TAP

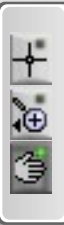
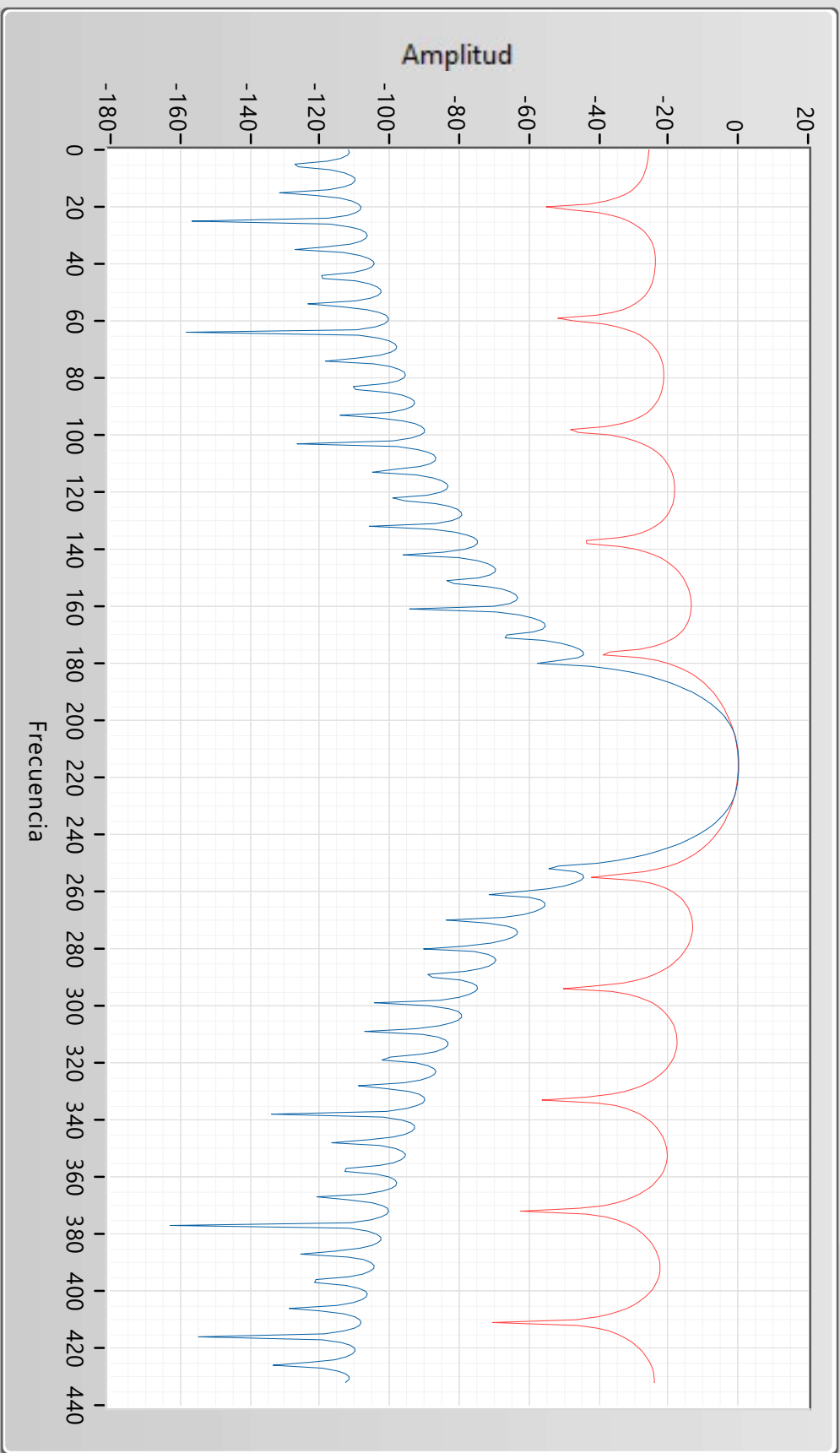
amplitud

index

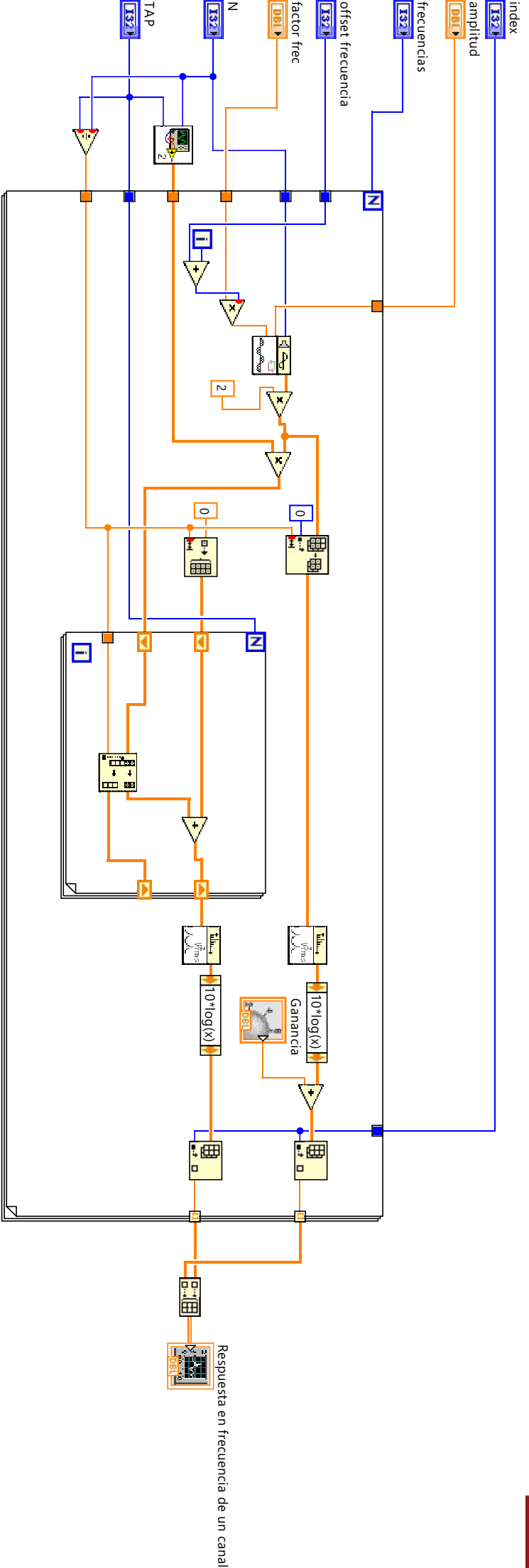
Ganancia



Respuesta en frecuencia de un canal



Plot 0



PFB algoritmo.vi



Demostracion o validacion del algoritmo de banco de filtros polifasicos (PFB). El VI muestra el espectro de potencias de señales simuladas usando FFT directa (sin PFB) y usando un PFB de orden 4.



TAPs noise (rms)

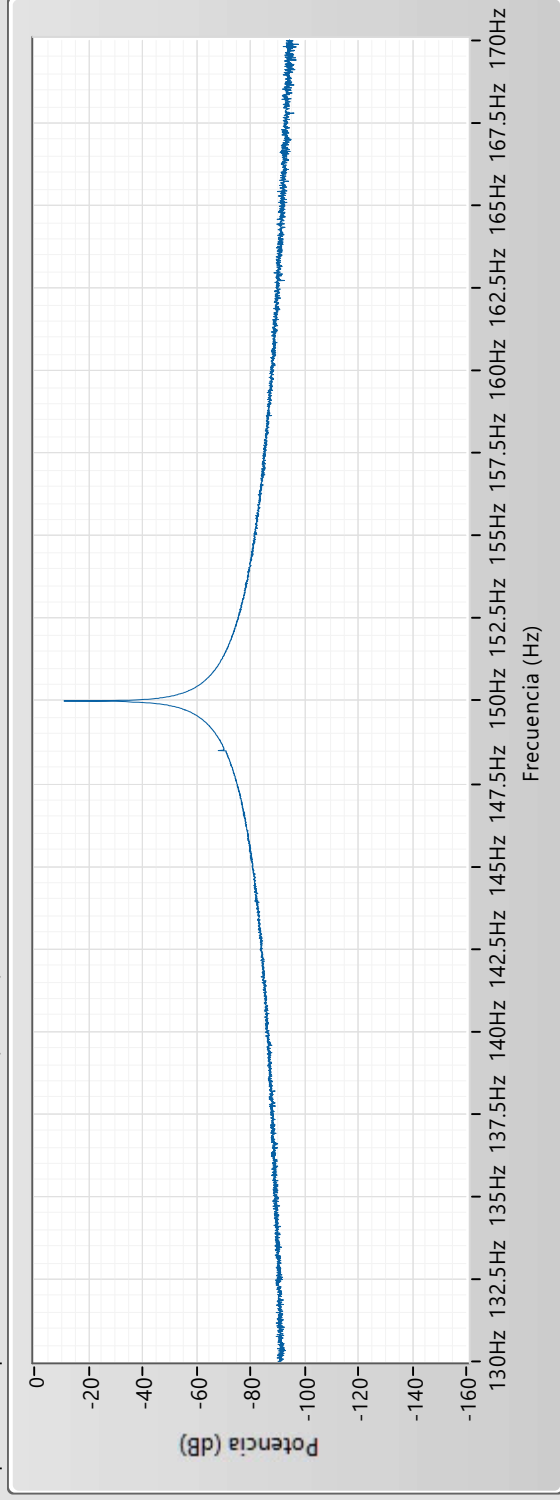
Nmuestras

tones

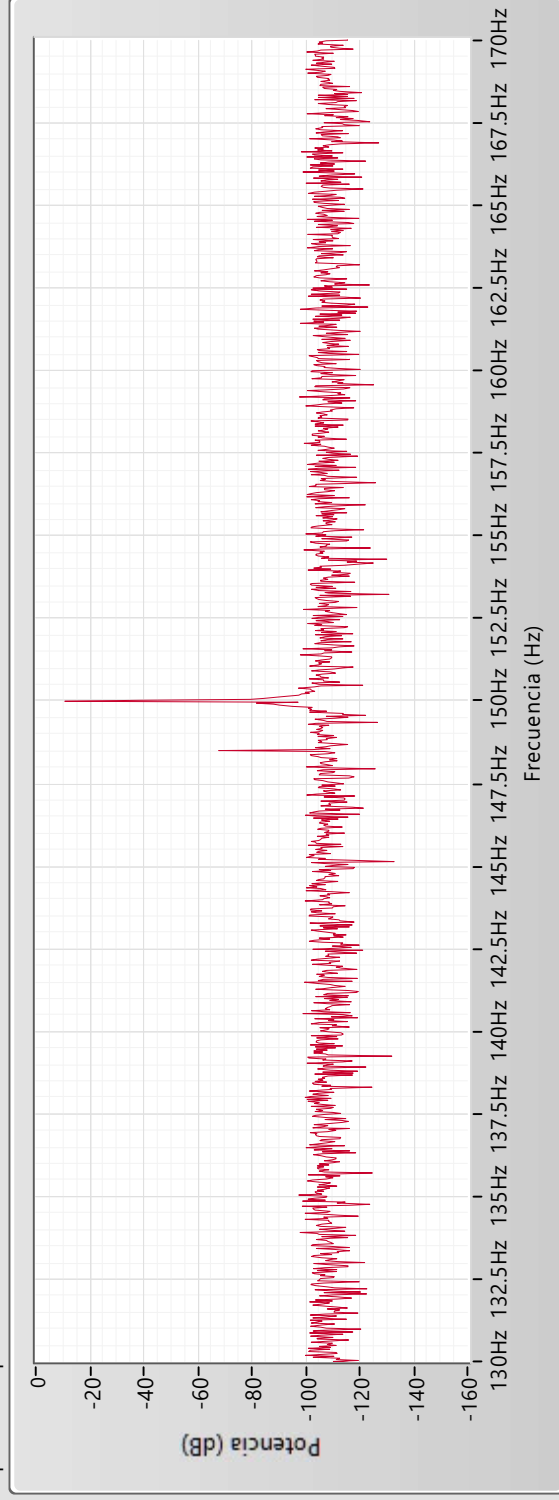
frequency
 amplitude
 phase

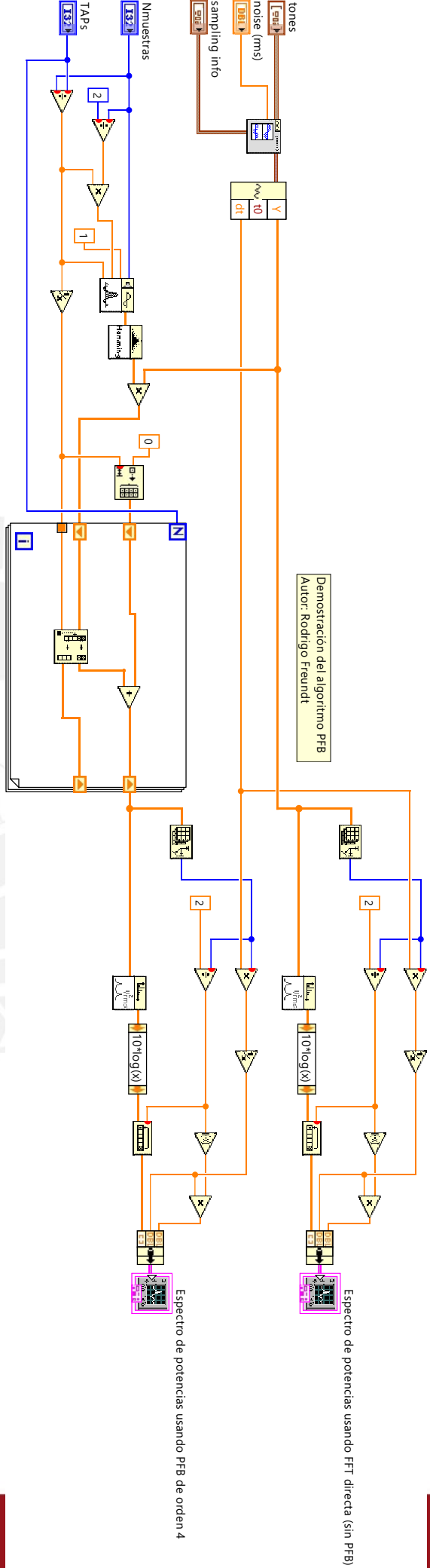
sampling info
 Fs
 #s

Espectro de potencias usando FFT directa (sin PFB)



Espectro de potencias usando PFB de orden 4





```

/*****
Archivo: "kernel.cu"
*****/
Descripción: DLL escrita en CUDA C

-PFBKernel: Realiza el algoritmo WOLA, junto a la FFT implementa un PFB.
-acuKernel: Halla el espectro y lo acumula.
-dbmKernel: Convierte valores de potencia a dBm.
-convVoltKernel: Convierte muestras binarias a valores de voltaje, se usa cuando se configura FFT directa
*****/
Autor: Rodrigo Guillermo Freundt Rueda
Correo: rodrigo.freundt@pucp.edu.pe
Fecha: 21/11/2016
*****/

#include "cuda_runtime.h"
#include "device_launch_parameters.h"
#include "kernel.cuh"
#include <device_functions.h>
#include <windows.h>
#include <cucomplex.h>
#include <math.h>

__global__ void PFBKernel(unsigned int *datain, float *PFBCoef, cuComplex *FFTin, float LSB, unsigned long
    Taps, unsigned long N)
{
    int i = blockIdx.x * blockDim.x + threadIdx.x;
    int m = 0; //indice para las ramas
    int j;

    cuComplex PFB = make_cuComplex(0.0, 0.0);
    unsigned int buff1;
    float buff2;
    float LSBlo = LSB;

    for (j = 0; j < Taps; j++)
    {
        m = (j * N) + i;
        buff1 = datain[m];
        buff2 = PFBCoef[m];

        //****Convercion de binario a voltaje*****/

        unsigned short Ip = (unsigned short)(buff1 & 0x0000FFFFUL);
        unsigned short Qp = (unsigned short)((buff1 & 0xFFFF0000UL) >> 16);
        short Ii = *reinterpret_cast<short*>(&Ip); // Ii = * ((int *) &Ip);
        short Qi = *reinterpret_cast<short*>(&Qp); // Qi = * ((int *) &Qp);
        float I = (float)Ii * LSBlo; //float I = __int2float_rn(Ii);
        float Q = (float)Qi * LSBlo; //float Q = __int2float_rn(Qi);

        //*****

        PFB.x += I * buff2;
        PFB.y += Q * buff2;
    }
    FFTin[i] = PFB;
    return;
}

__global__ void acuKernel(cuComplex *FFT, float *EP, unsigned long size){

    int i = blockDim.x * blockIdx.x + threadIdx.x;
    cuComplex buff = FFT[i];
    buff.x /= (float) size;
    buff.y /= (float) size;
}

```

```

    //temp = 10 * log10f(10 * temp);
    EP[i] += buff.x * buff.x + buff.y * buff.y;
    return;
}

__global__ void dbmKernel(float *EP, unsigned long size){

    int i = blockDim.x * blockIdx.x + threadIdx.x;
    float temp = EP[i];
    //EP[i] /= ((float)nint);
    EP[i] = 10 * log10f(10 * temp) + 2.0;
    return;
}

__global__ void convVoltKernel(unsigned int *datain, cuComplex *dataout, float LSB){

    int i = blockDim.x * blockIdx.x + threadIdx.x;
    unsigned int buff = datain[i];
    float LSBlo = LSB;

    unsigned short Ip = (unsigned short)(buff & 0x0000FFFFUL);
    unsigned short Qp = (unsigned short)((buff & 0xFFFF0000UL) >> 16);
    short Ii = *reinterpret_cast<short*>(&Ip); // Ii = * ((int *) &Ip);
    short Qi = *reinterpret_cast<short*>(&Qp); // Qi = * ((int *) &Qp);
    float I = (float) Ii * LSBlo; //float I = __int2float_rn(Ii);
    float Q = (float) Qi * LSBlo; //float Q = __int2float_rn(Qi);

    dataout[i] = make_cuComplex(I , Q);
    return;
}

BOOL APIENTRY DllMain(HANDLE hModule,
    DWORD ul_reason_for_call,
    LPVOID lpReserved)
{
    return TRUE;
}

extern "C" __declspec(dllexport) void __cdecl DEPdbm(cuComplex *FFT, float *EP, unsigned long size, signed short dump){

    acuKernel <<< size / 256, 256 >>>(FFT, EP, size);
    if (dump){
        dbmKernel <<< size / 256, 256 >>>(EP, size);
    }
    return;
}

extern "C" __declspec(dllexport) void __cdecl convVolt(unsigned int *datain, cuComplex *FFTin, float * PFBcoef, float LSB, unsigned long Taps, unsigned long size){

    unsigned long buff = size/Taps;
    //convVoltKernel <<< size / 256, 256 >>>(datain, FFTin, LSB);
    if (Taps != 1){
        PFBKernel <<< buff / 256, 256 >>>(datain, PFBcoef, FFTin, LSB, Taps, buff);
    }
    else
    {
        convVoltKernel <<< size / 256, 256 >>>(datain, FFTin, LSB);
    }
    return;
}

```

```
/*
*****
Archivo: "kernel.cuh"
*****
Descripción: Cabecera de la DLL escrita en CUDA C

-PFBKernel: Realiza el algoritmo WOLA, junto a la FFT implementa un PFB.
-acuKernel: Halla el espectro y lo acumula.
-dbmKernel: Convierte valores de potencia a dBm.
-convVoltKernel: Convierte muestras binarias a valores de voltaje, se usa cuando se configura FFT directa
*****
Autor: Rodrigo Guillermo Freundt Rueda
Correo: rodrigo.freundt@puclp.edu.pe
Fecha: 21/11/2016
*****/

#ifndef KERNEL_CUH
#define KERNEL_CUH

#include "cuda_runtime.h"
#include "device_launch_parameters.h"
#include <windows.h>
#include <cucomplex.h>
#include <math.h>

extern "C" __declspec(dllexport) void __cdecl DEPdbm(cuComplex *FFT, float *EP, unsigned long size, signed short dump);

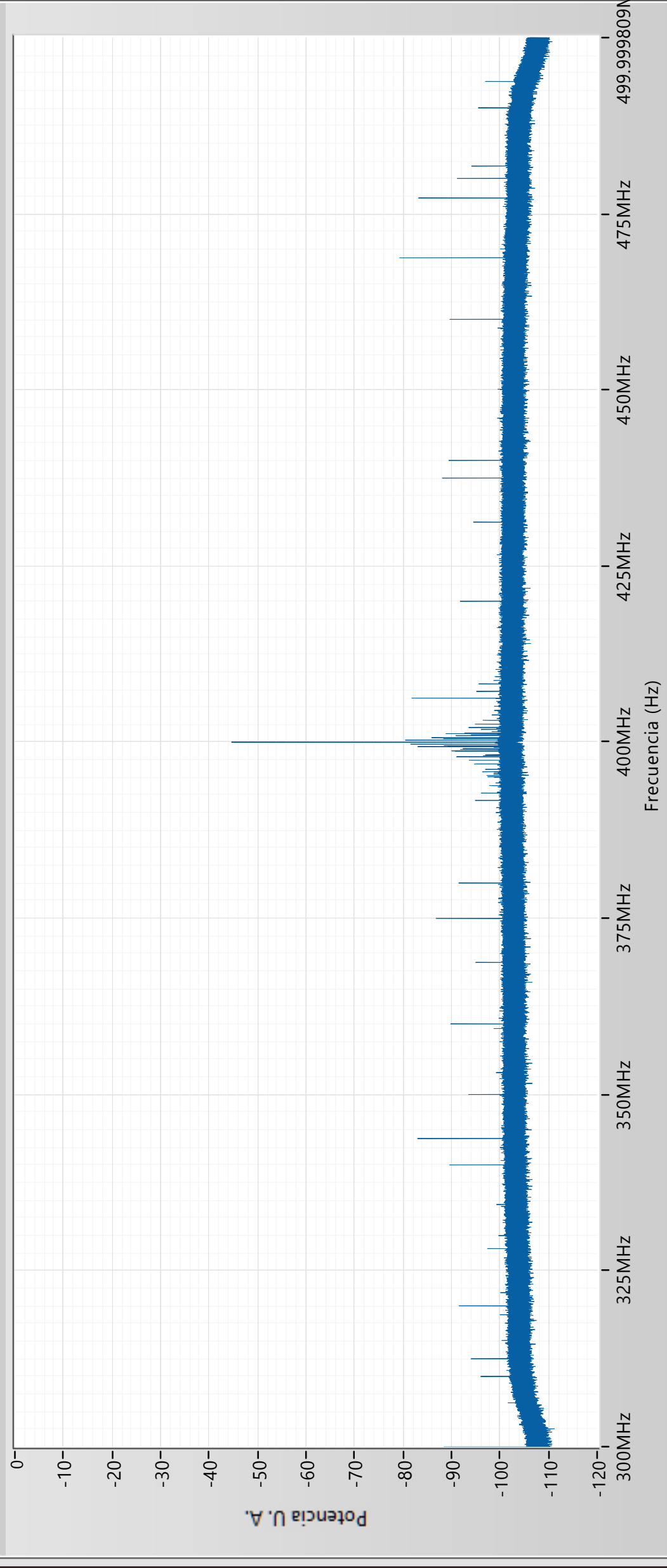
extern "C" __declspec(dllexport) void __cdecl convVolt(unsigned int *datain, cuComplex *FFTin, float * PFBcoef, float LSB, unsigned long Taps, unsigned long size);

#endif
```

FFTS-SERVIDOR.vi

Programa principal del programa de servidor del FFTS. En este VI, se obtienen las muestras del Network Stream y se encolan hacia el bucle de procesamiento principal. Dentro del bucle, se llama al SubVI Procesamiento GPU.vi, el cual llama a todas las funciones necesarias para acelerar el procesamiento del FFTS usando recursos del GPU.

Fs (Msps) Oscilador Local (Hz) N TAPs #Acumulaciones Vref pp buffer NS



CUDA Device ID GPU:

CUDA Version:

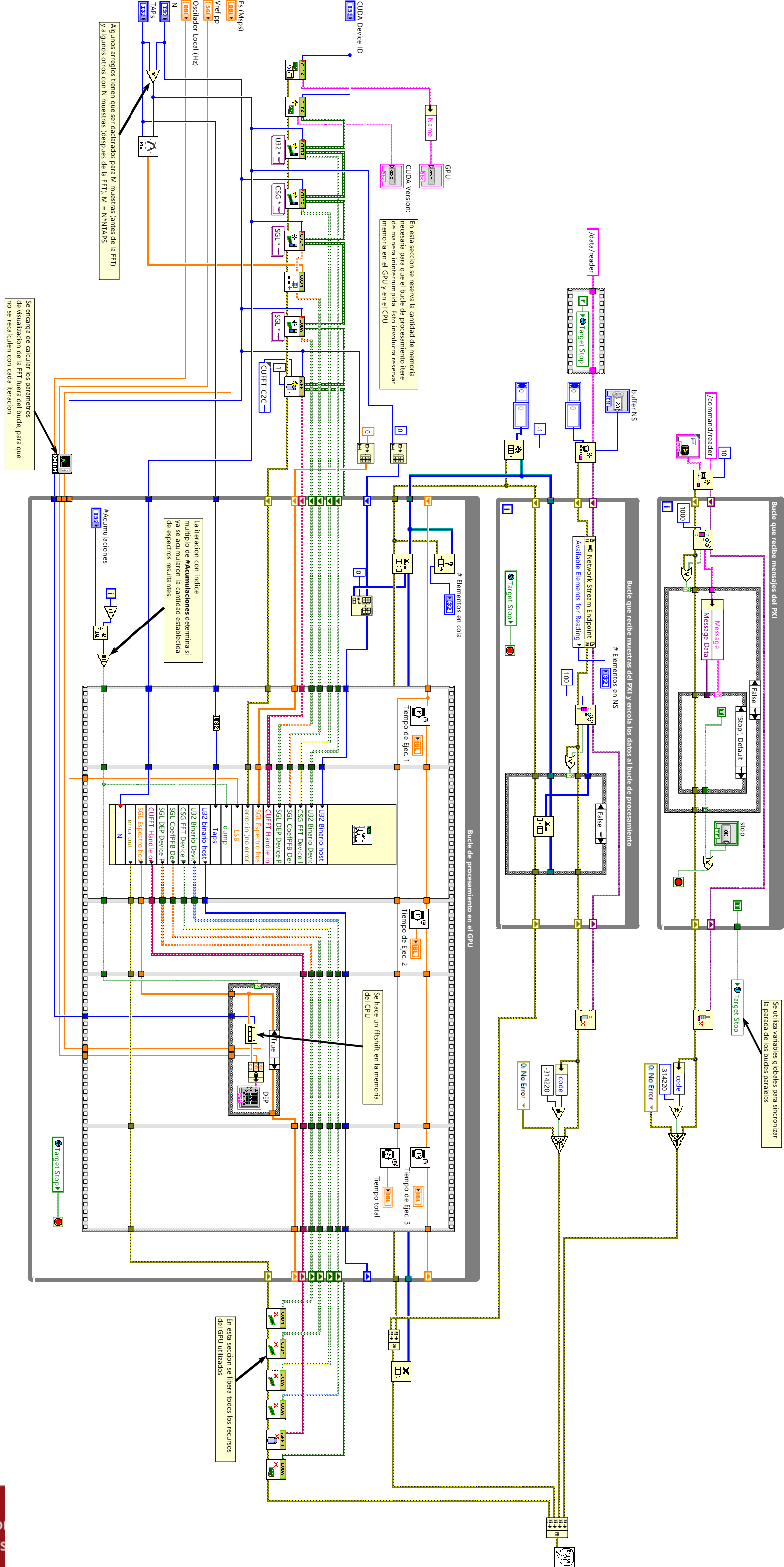
Tiempo de Ejec. 1

Tiempo de Ejec. 2

Tiempo de Ejec. 3

Tiempo total

Elementos en cola # Elementos en NS



Se utiliza variables globales para sincronizar la parada de los bucles paralelos


En esta seccion se reserva la cantidad de memoria necesaria para que el bucle de procesamiento opere de manera ininterrumpida. Esto involucra reservar memoria en el GPU y en el CPU

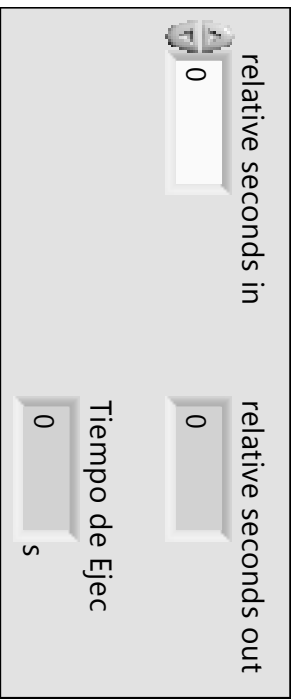
La iteracion con indice multiplo de #Acumulaciones determina si ya se acumularon la cantidad establecida de espectros resultantes.

Se encarga de calcular los parametros de visualizacion de la FFT fuera del bucle, para que no se recalculen con cada iteracion

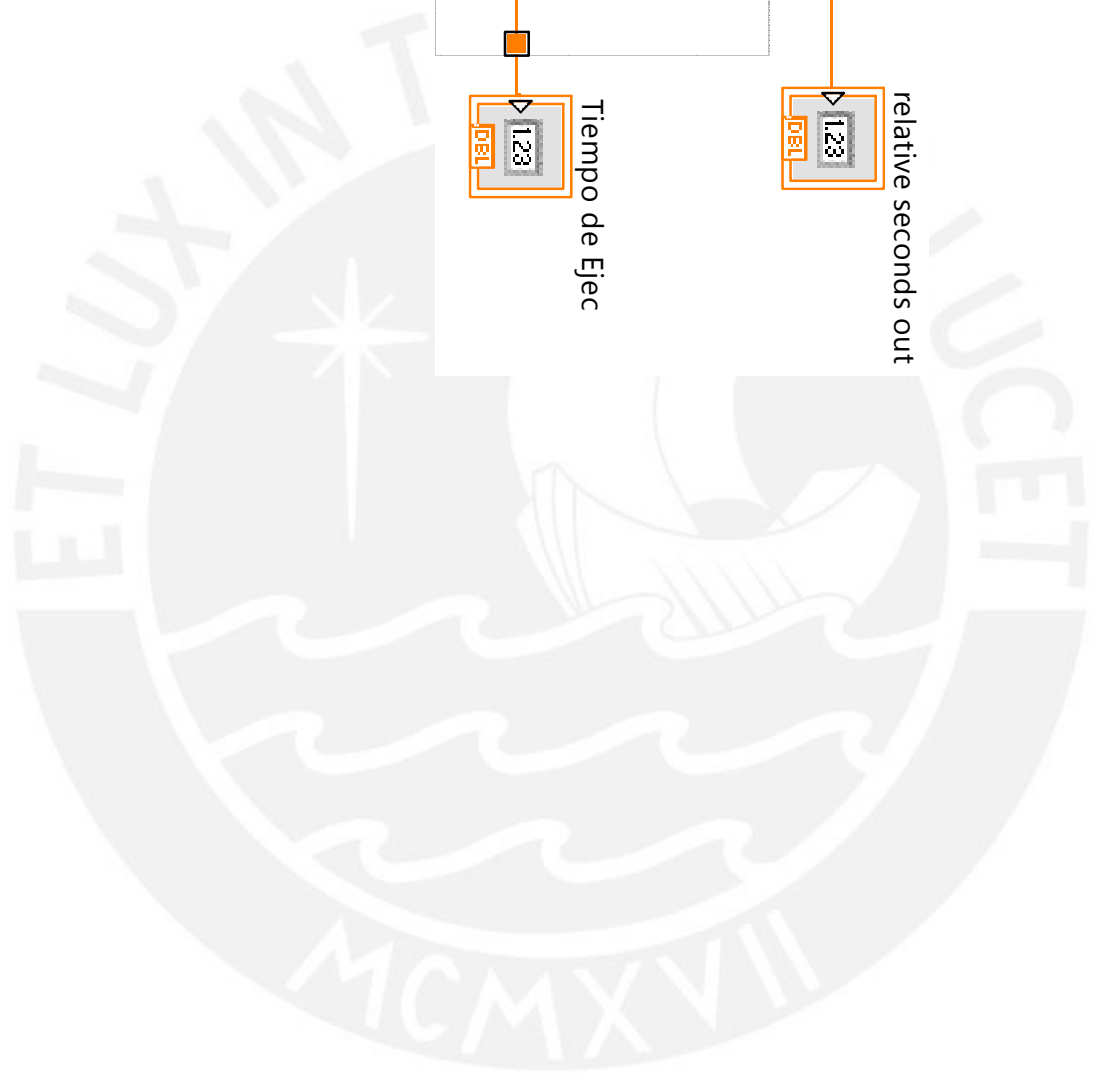
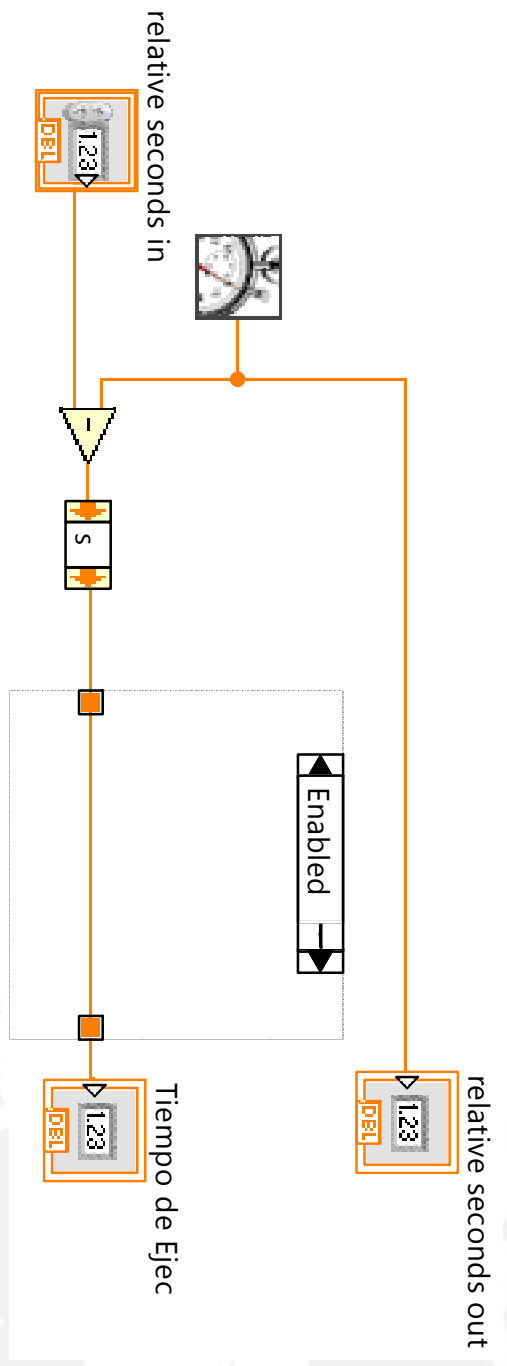
En esta seccion se libera todos los recursos del GPU utilizados

benchmark.vi

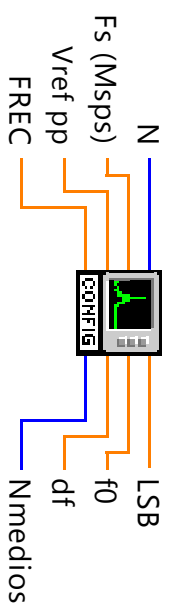
relative seconds in  relative seconds out
Tiempo de Ejec



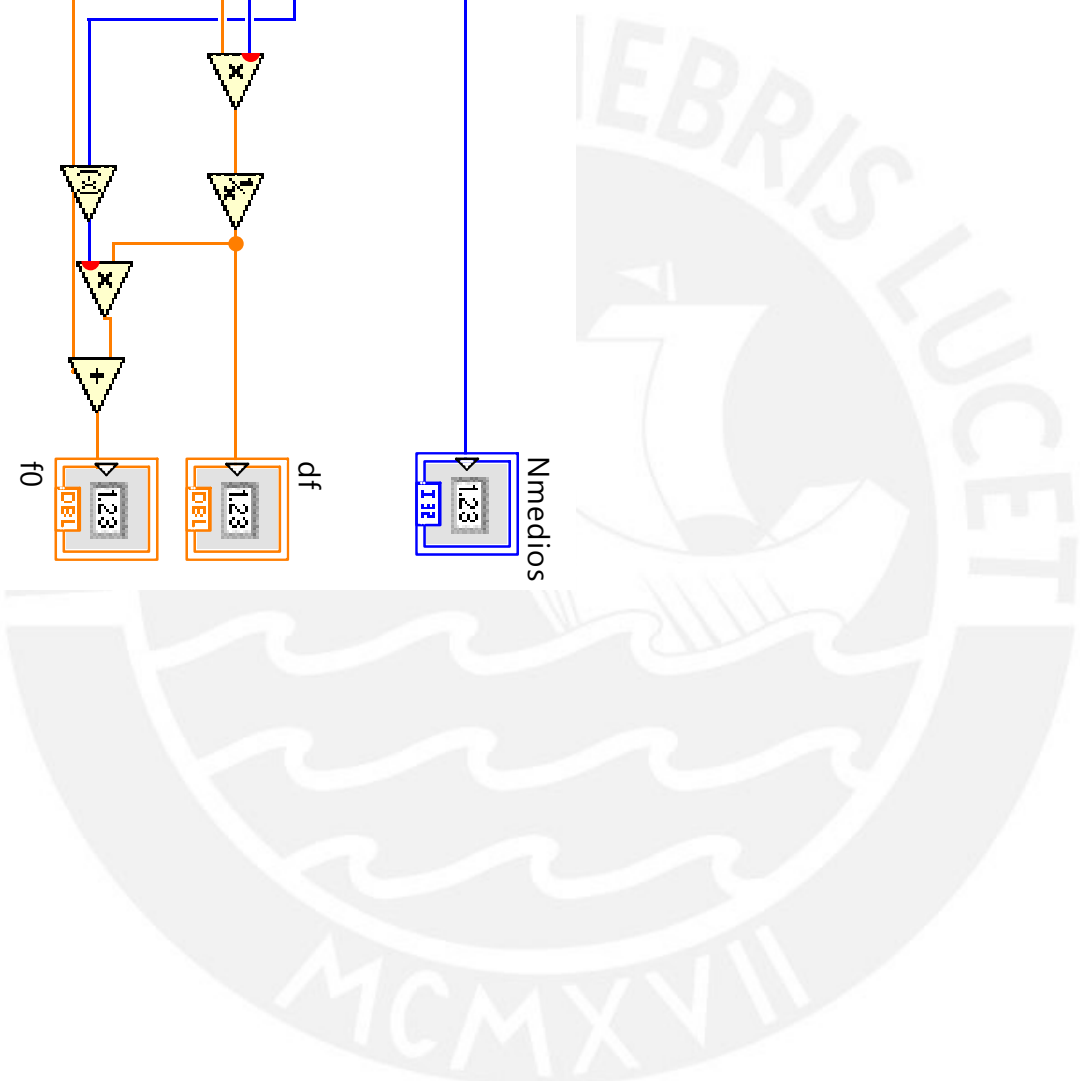
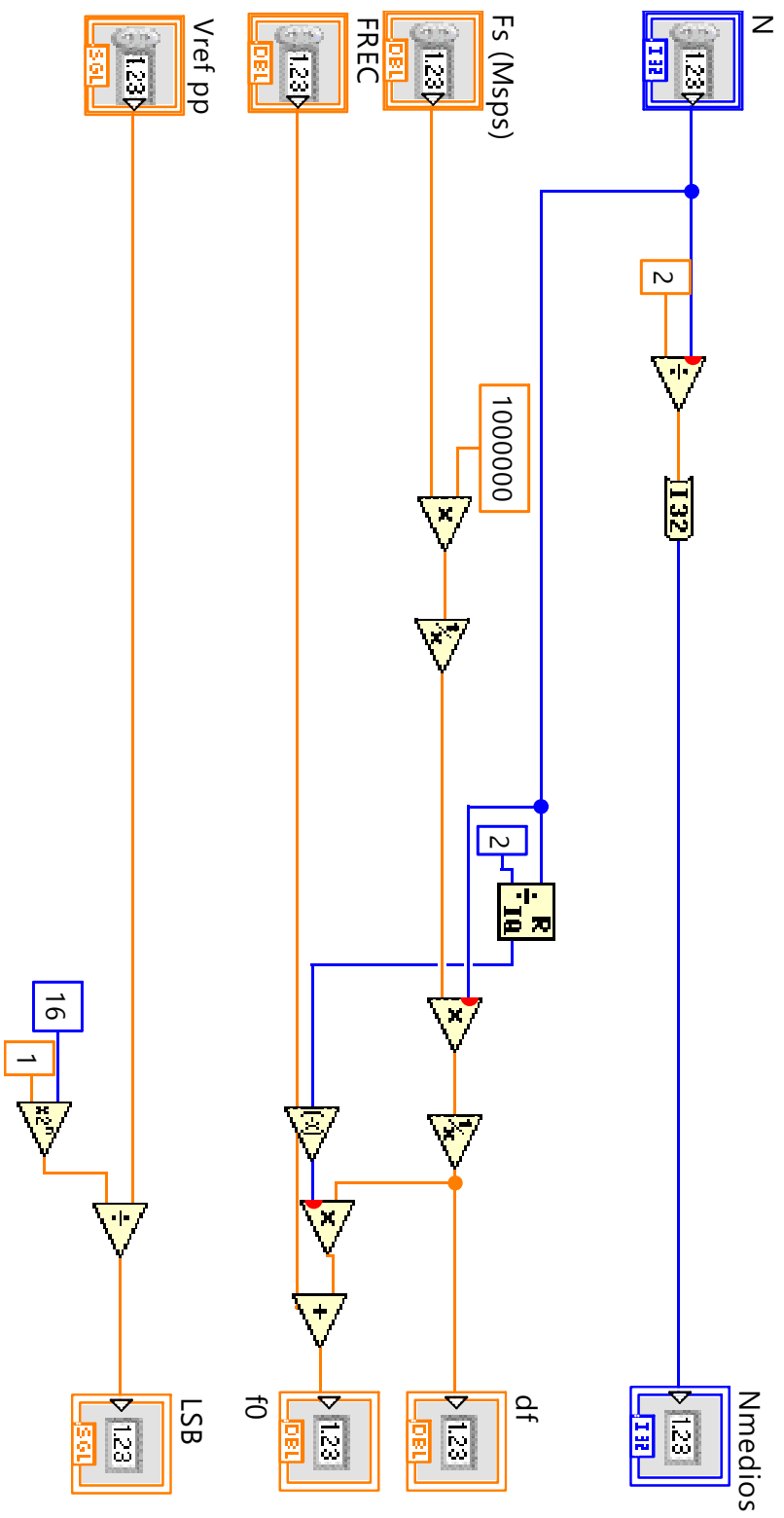
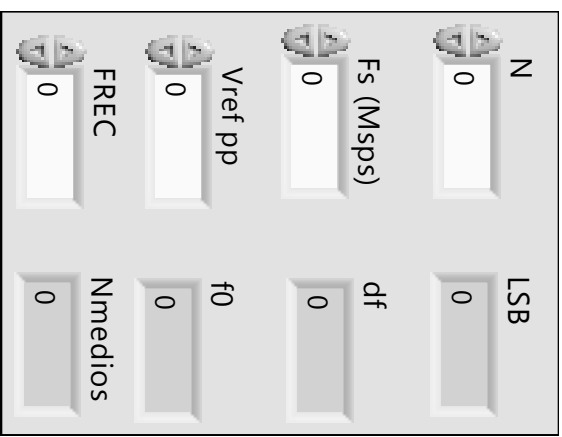
subVI que calcula el tiempo transcurrido a partir de dos timestamps. Usado para simplificar el diagrama de bloques del VI principal.



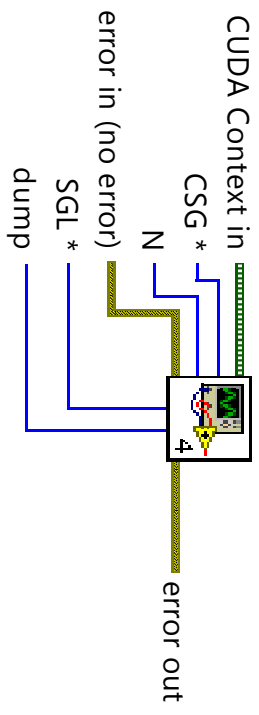
Calcparametros.vi



SubVI que se encarga de calcular los parametros de visualizacion del espectro, como la frecuencia central, el df, etc



FuncExec.vi



Ejecucion del kernel personalizado encargado de calcular el espectro de potencias a partir de la salida de la FFT, acumular el espectro y convertir valores de potencia a dbm.

CUDA Context in

CSG * 0x0000000000000000 SGL * 0x0000000000000000

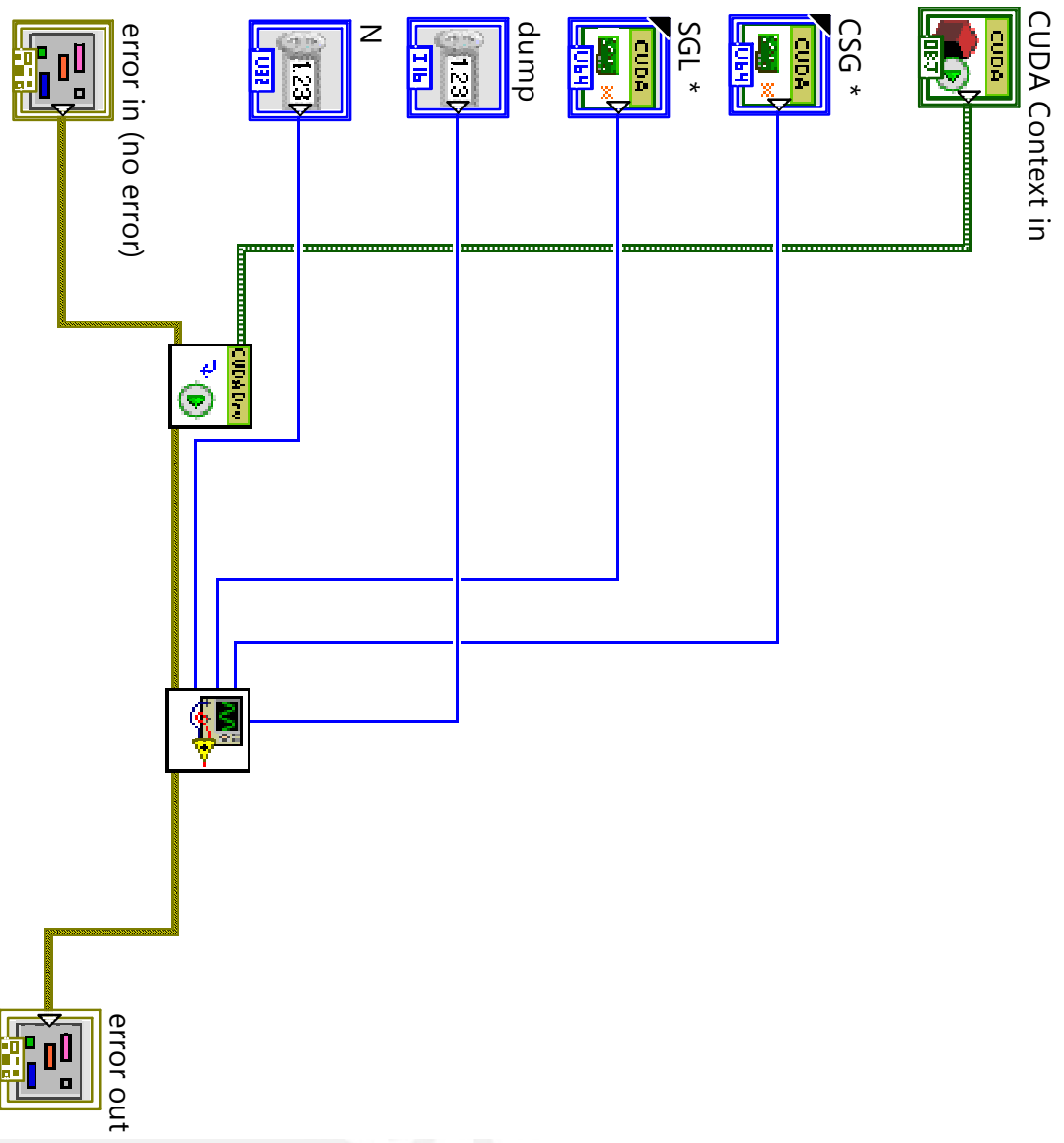
N 0 dump 0

error in (no error) error out

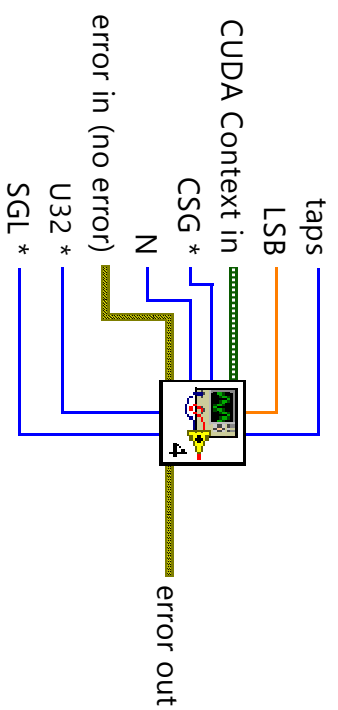
status code 0 source

status code 0 source





FuncExec2.vi



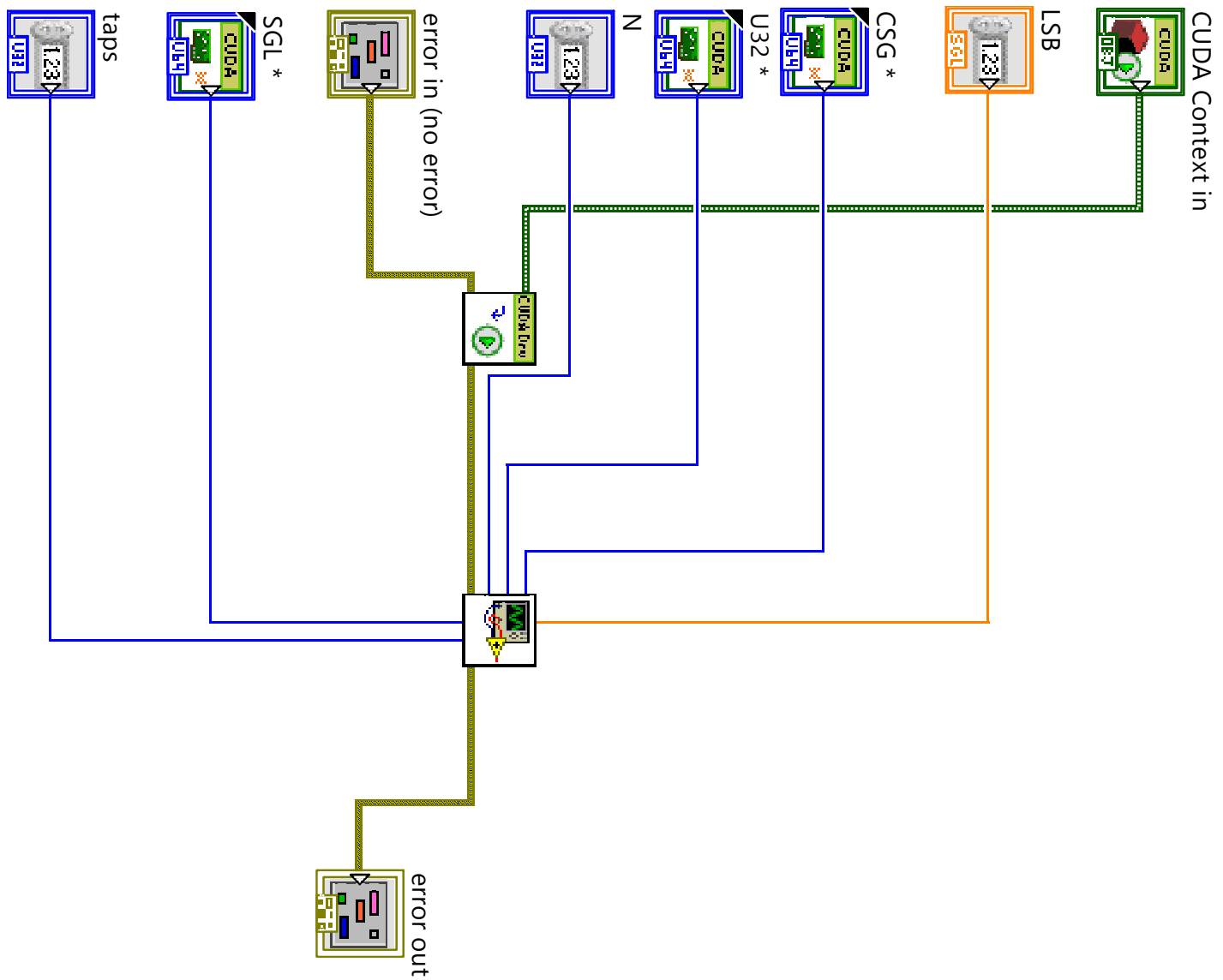
Ejecucion del kernel personalizado encargado de convertir de binario a voltaje y efectuar el PFB.

CUDA Context in

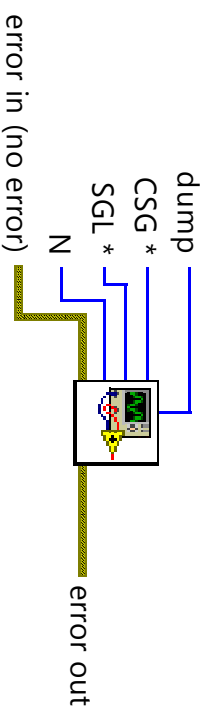
The front panel of the 'FuncExec2.vi' block contains the following elements:

- CSG *:** A numeric keypad with a value of 0x0000000000000000.
- N:** A numeric keypad with a value of 0.
- LSB:** A numeric keypad with a value of 0.
- U32 *:** A numeric keypad with a value of 0x0000000000000000.
- SGL *:** A numeric keypad with a value of 0x0000000000000000.
- taps:** A numeric keypad with a value of 0.
- error in (no error):** A status indicator with a green checkmark, a numeric keypad showing '0', and a 'source' field.
- error out:** A status indicator with a green checkmark, a numeric keypad showing '0', and a 'source' field.



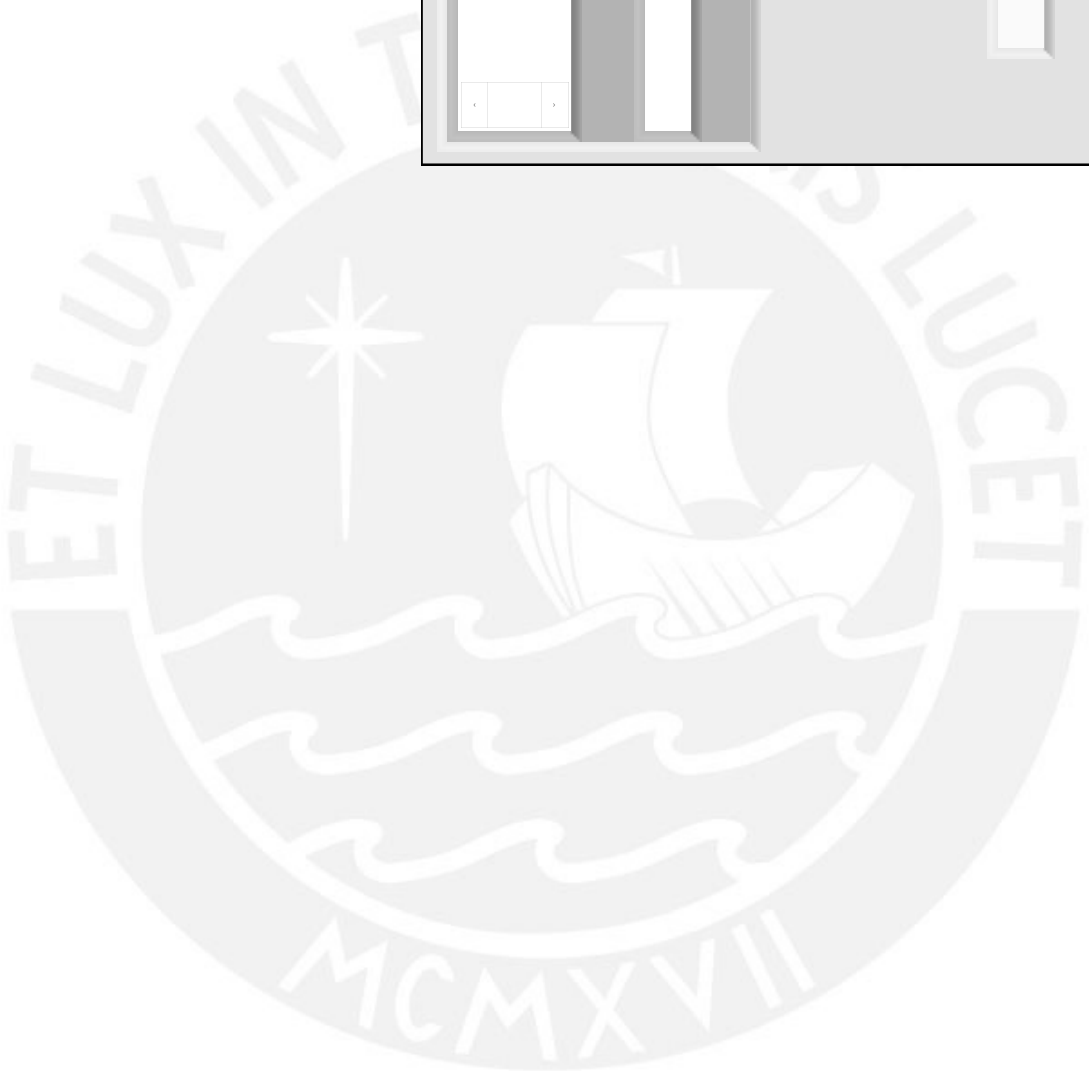
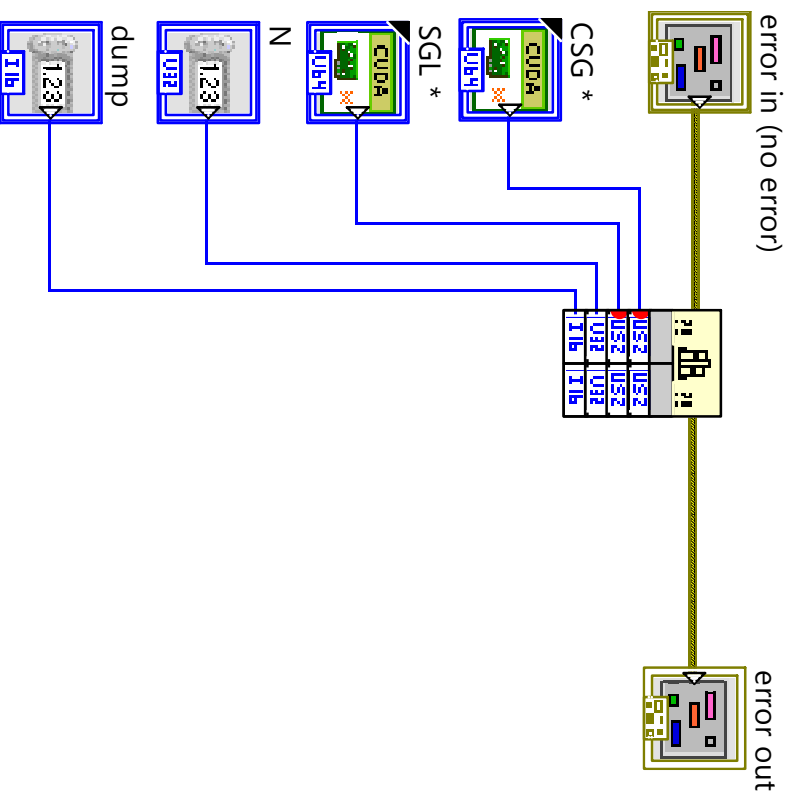


Funclnvoc.vi

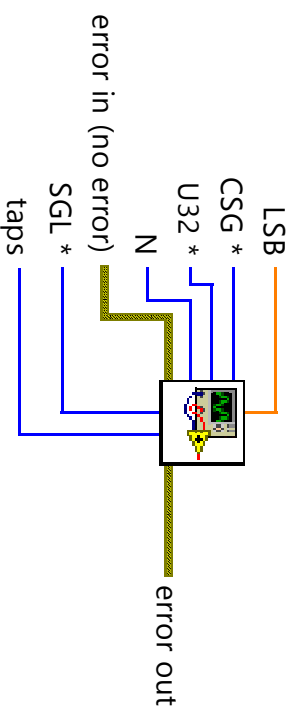


Invocacion del kernel personalizado encargado de calcular el espectro de potencias a partir de la salida de la FFT, acumular el espectro y convertir valores de potencia a dbm.

The screenshot shows the control panel of the 'Funclnvoc.vi' VI. It features two main sections, one for 'CSG *' and one for 'SGL *'. Each section has a memory address field (both showing '0x0000000000000000'), a 'N' field (both showing '0'), and a 'dump' field (both showing '0'). Below these are status indicators (green checkmarks) and 'code' fields (both showing '0'). There are also 'error in (no error)' and 'error out' status indicators with associated 'source' fields.



Funclnvoc2.vi



Invocacion de kernel personalizado encargado de convertir de binario a voltaje y efectuar el PFB.

U32 * 0x0000000000000000 SGL * 0x0000000000000000

CSG * 0x0000000000000000

N 0 LSB 0 taps 0

error in (no error)

status code 0

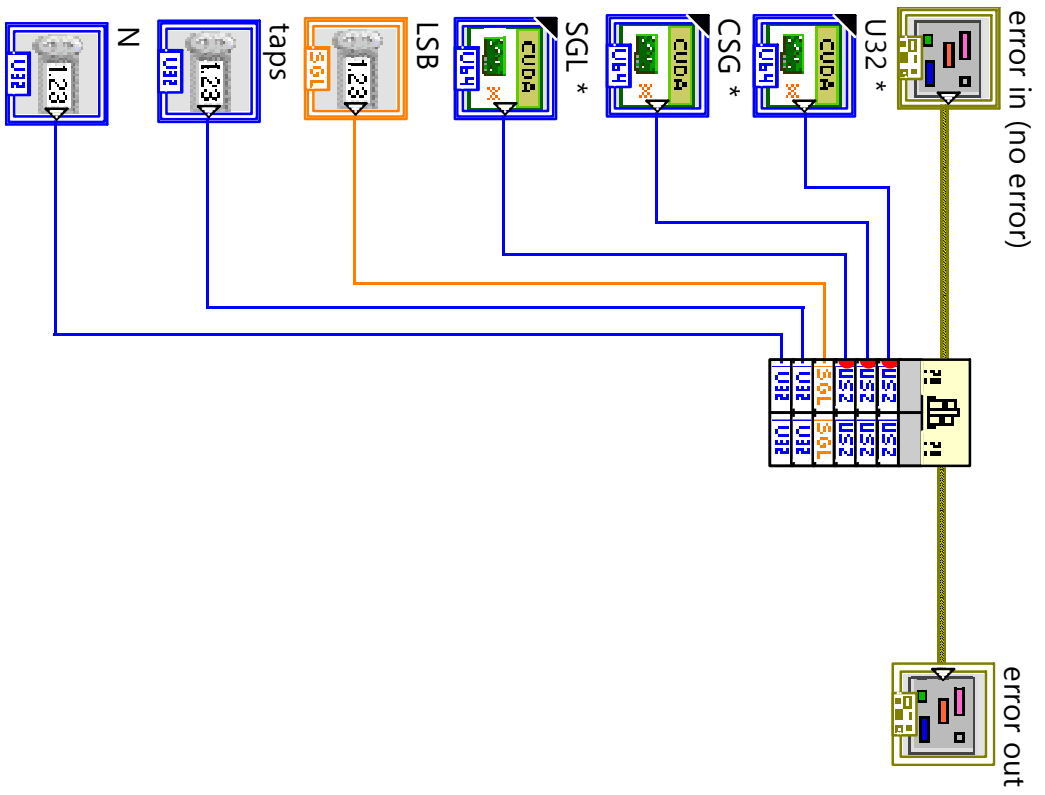
source

error out

status code 0

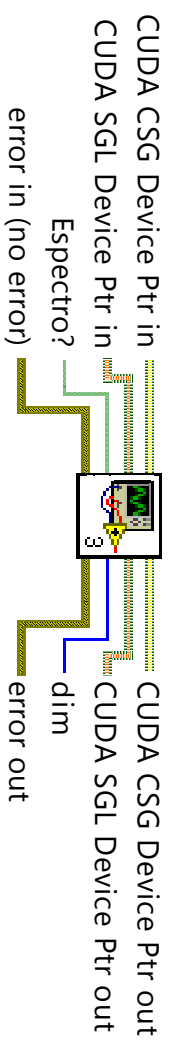
source



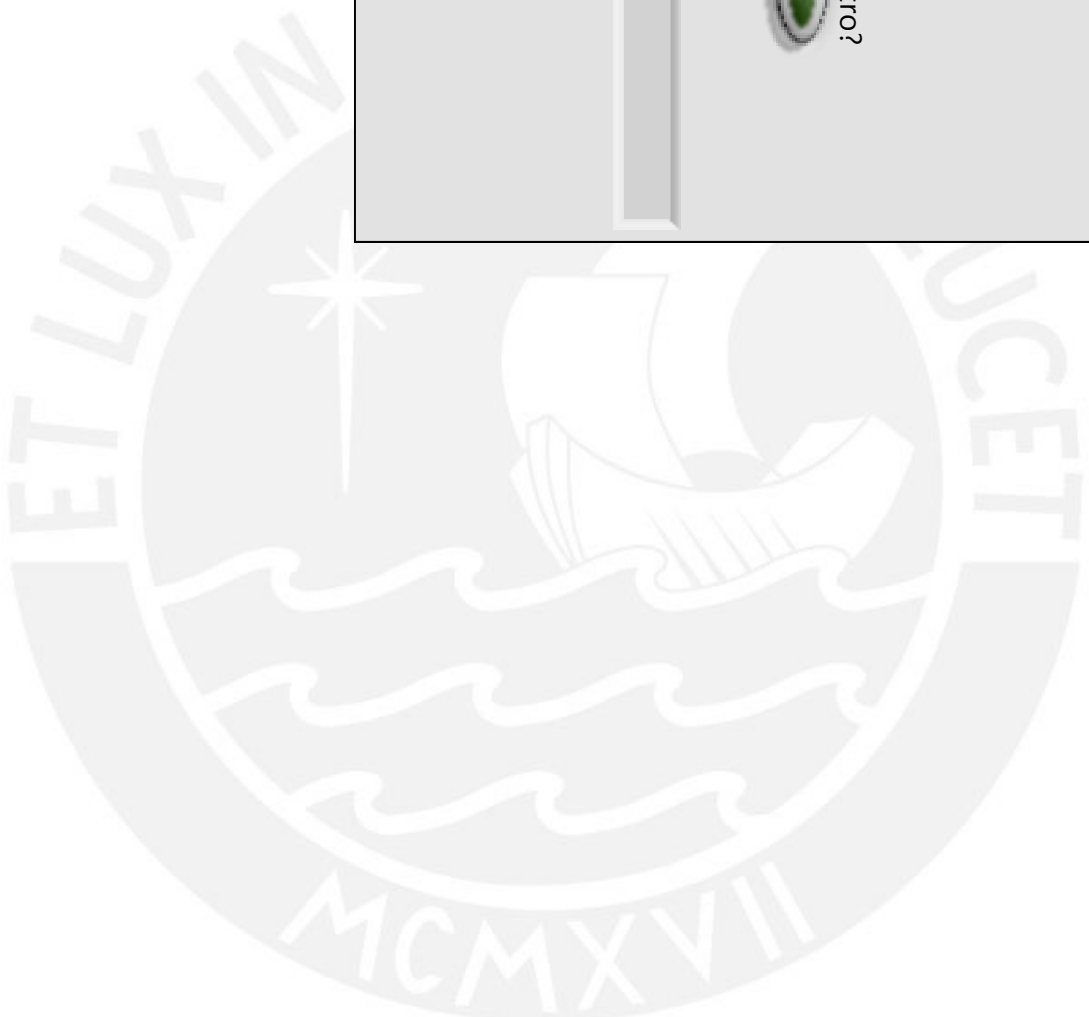


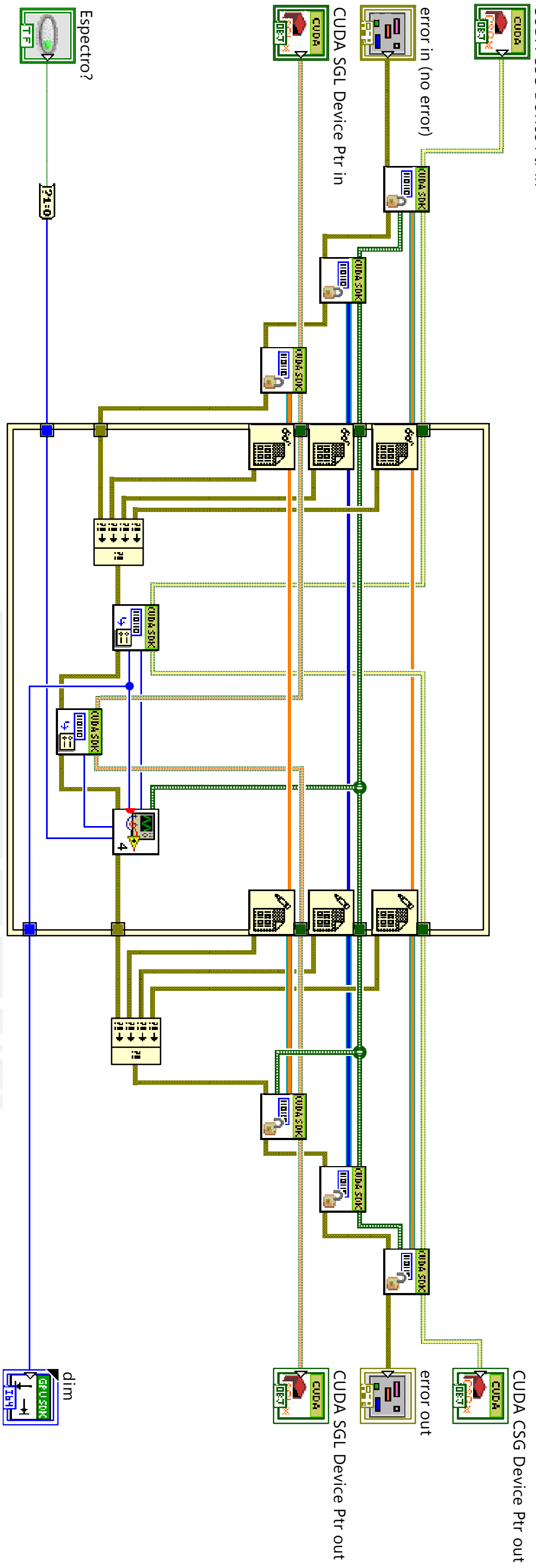


FuncProt.vi

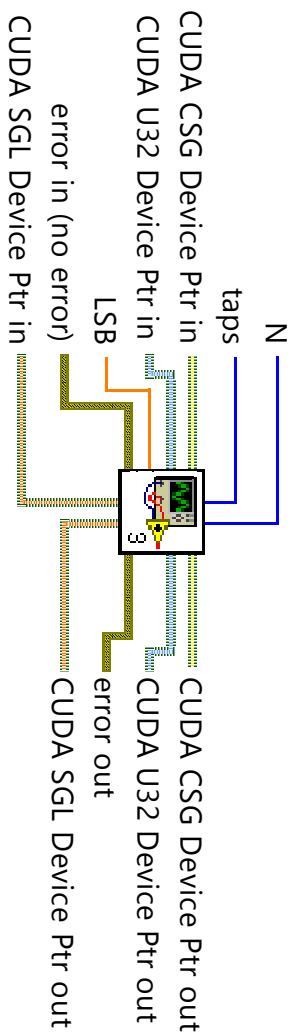


VI wrapper de protección de parametros para llamar al kernel personalizado encargado de calcular el espectro de potencias a partir de la salida de la FFT, acumular el espectro y convertir valores de potencia a dbm.





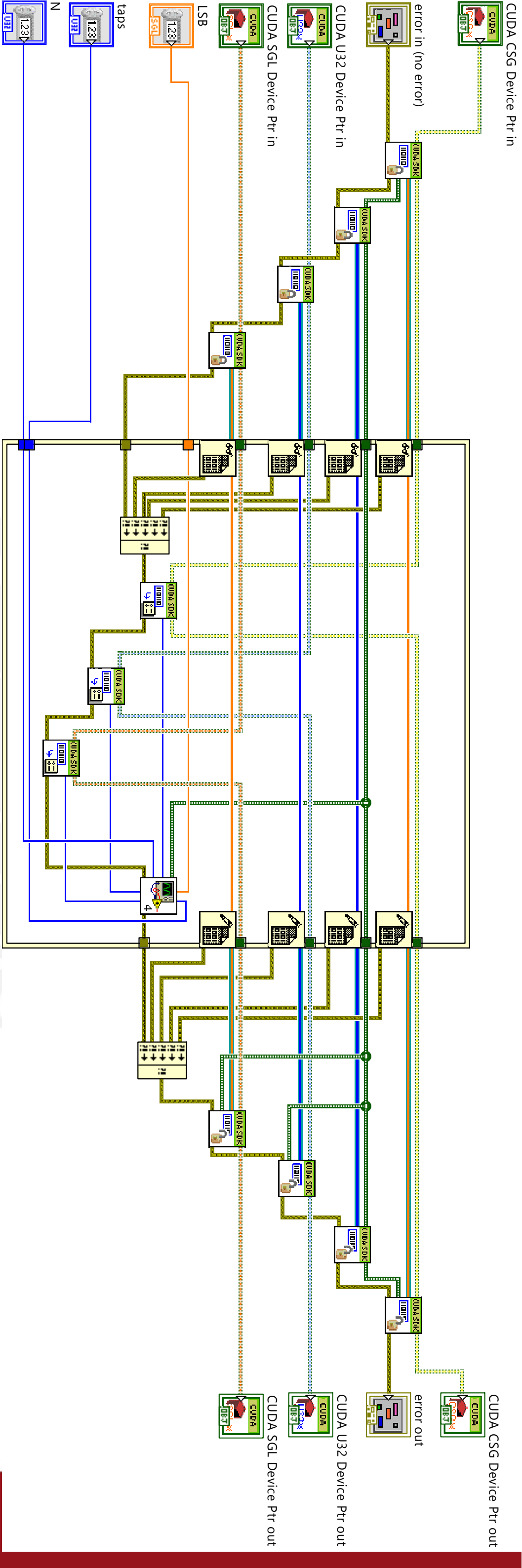
FuncProt2.vi



VI wrapper de protección de parametros para llamar al kernel personalizado encargado de convertir de binario a voltaje y efectuar el PFB.

The front panel of the VI is organized into two main sections. The top section contains six device pointer controls, each with a corresponding icon: 'CUDA SGL Device Ptr in', 'CUDA U32 Device Ptr in', 'CUDA CSG Device Ptr in', 'CUDA SGL Device Ptr out', 'CUDA U32 Device Ptr out', and 'CUDA CSG Device Ptr out'. Below these are three error status indicators: 'error in (no error)', 'error out', and 'error in (no error)', each with a 'status' indicator (a green checkmark) and a 'code' field set to '0'. The bottom section features three control knobs: 'taps' (set to 0), 'LSB' (set to 0), and 'N' (set to 0). Each knob has a 'source' field and a 'status' indicator.

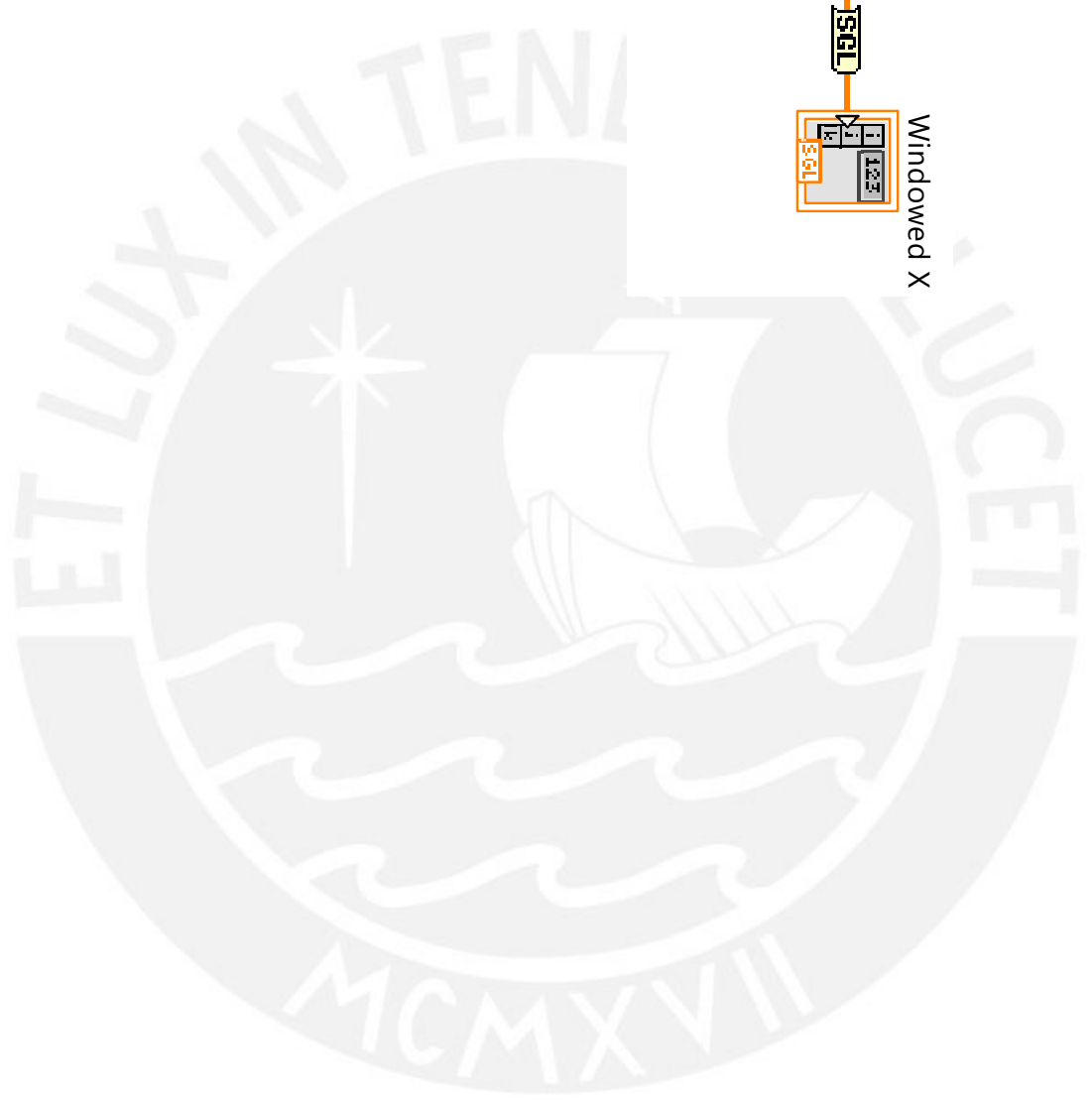
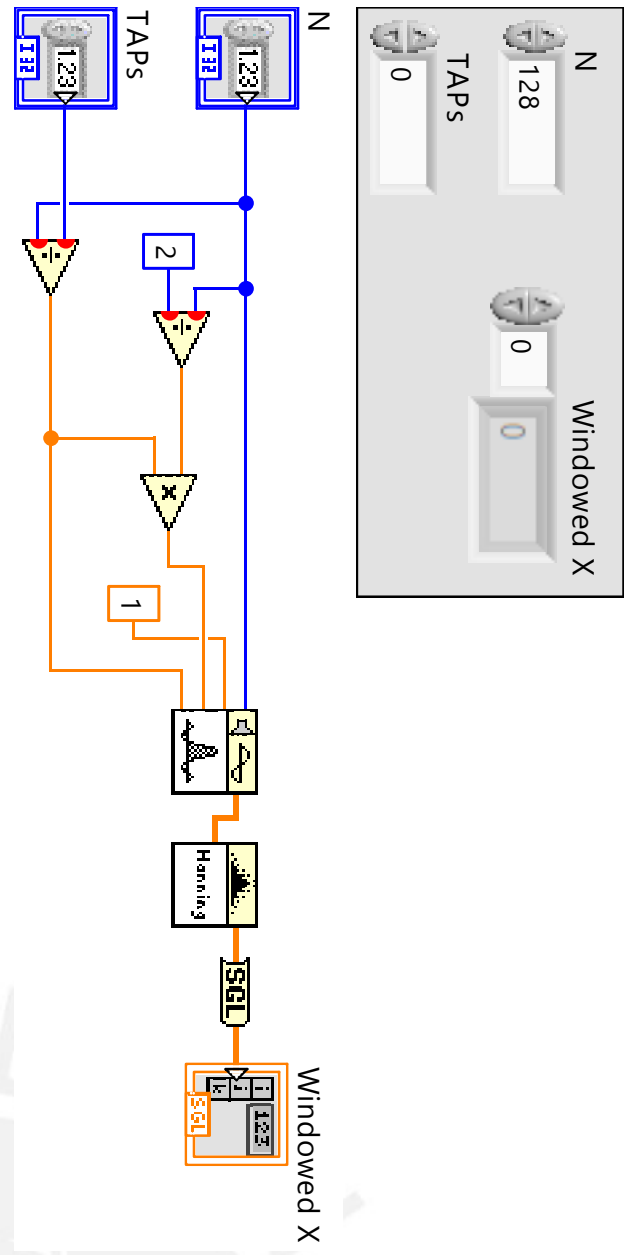




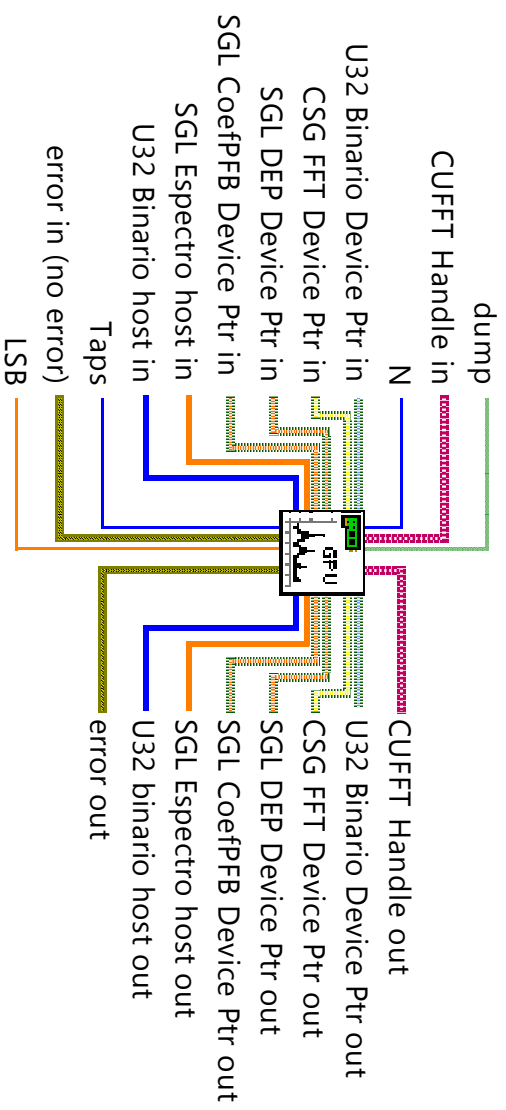
PFBcoef.vi



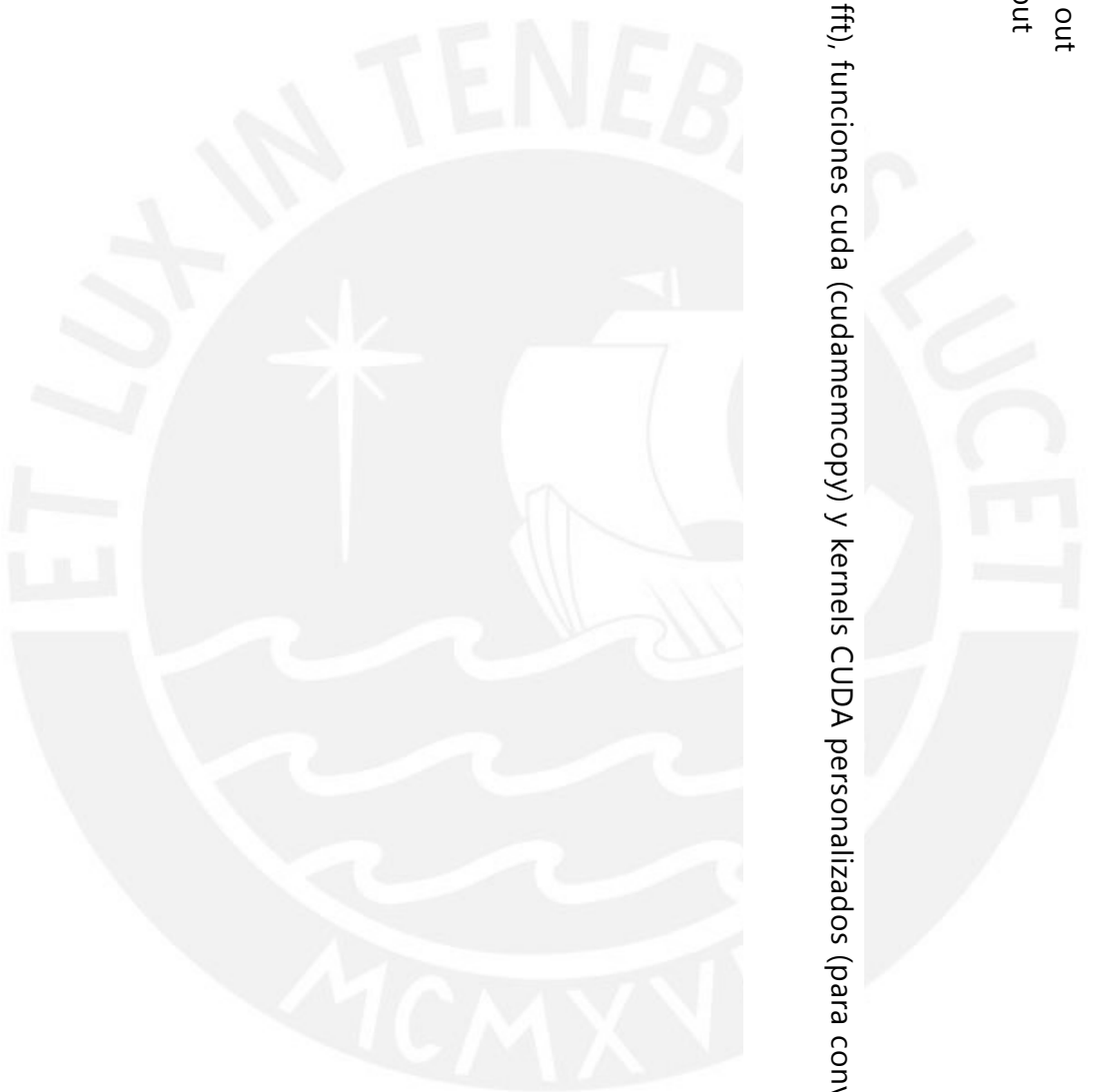
SubVI que calcula los coeficientes del filtro usado en el banco de filtros polifasico (PFB)




ProcesamientoGPU.vi





Reune a los VI wrappers encargados de llamar a las libreria CUDA(cuFFT), funciones cuda (cudamemcopy) y kernels CUDA personalizados (para conversion binario a voltios, PFB, calculo de EP, acumulacion y conversion a dBm)








CSG FFT Device Ptr in 


CSG FFT Device Ptr out 


SGL CoeffFB Device Ptr in 


SGL CoeffFB Device Ptr out 


SGL DEP Device Ptr in 


SGL DEP Device Ptr out 


CUFFT Handle in 


CUFFT Handle out 


U32 Binario Device Ptr in 


U32 Binario Device Ptr out 


SGL Espectro host in 


SGL Espectro host out 


U32 Binario host in 


U32 binario host out 


USB 


dump 


Taps 


N 


error in (no error) 

error out 

status code 

source 

status code 

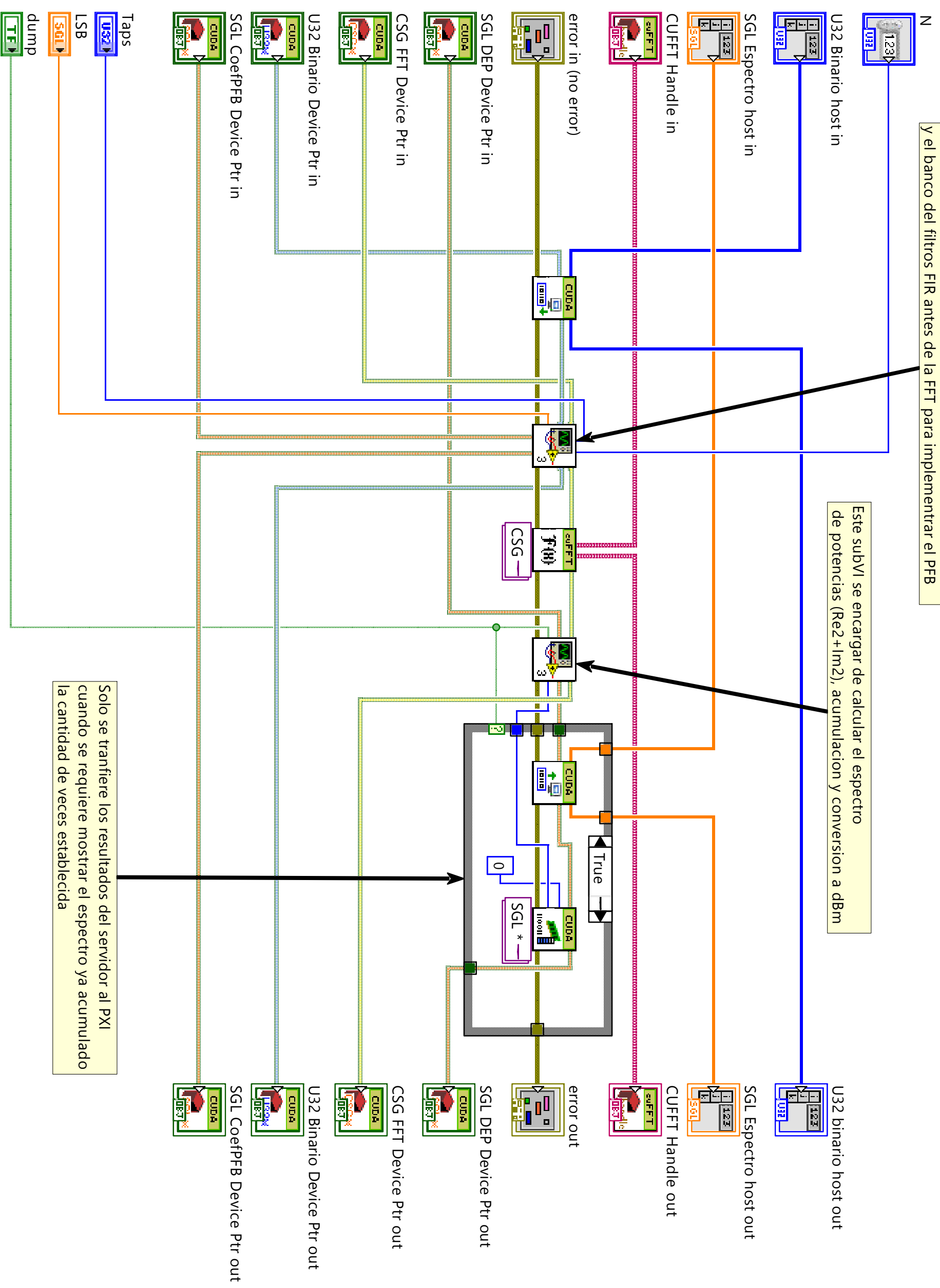
source 



Este subVI se encarga de realizar la conversión de binario a voltaje y el banco de filtros FIR antes de la FFT para implementar el PFB

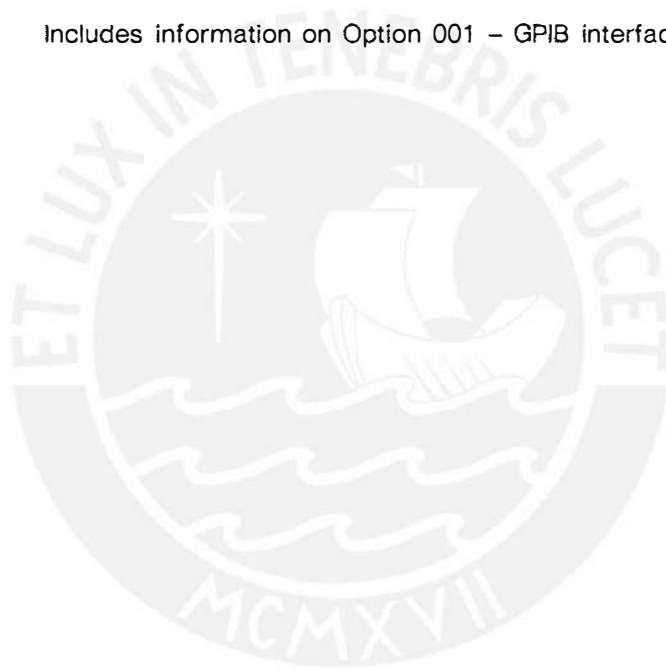
Este subVI se encargar de calcular el espectro de potencias (Re2+Im2), acumulacion y conversión a dBm

Solo se tranfiere los resultados del servidor al PXI cuando se requiere mostrar el espectro ya acumulado la cantidad de veces establecida



10 kHz – 1 GHz AM/FM SIGNAL GENERATOR 2022D

Includes information on Option 001 – GPIB interface



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ASSOCIATED PUBLICATIONS

Service Manual	Part No. 46882-002D
Operating Summary card	46882-003T

PREFACE

WARNINGS, CAUTIONS AND NOTES

These terms have specific meanings in this manual:-





WARNINGS contain information to prevent personal injury.

CAUTIONS contain information to prevent damage to the equipment.

Notes contain important general information.

HAZARD SYMBOLS

The meaning of hazard symbols appearing on the equipment is as follows:-

Symbol	Nature of hazard	Reference in manual
	Dangerous voltages	Page iv
	Beryllia	Page iv
	Static sensitive components	Page v
	Fire hazard	Page iv

MANUAL AMENDMENT STATUS

Each page in this manual bears the date of its original issue or, if it has been amended, the date and status number of the amendment. Any changes subsequent to the latest amendment status are included on Manual Change sheets coded C1, C2 etc at front of the manual.

OPERATING PRECAUTIONS

This product has been designed and tested in accordance with IEC Publication 348 – ‘Safety Requirements for Electronic Measuring Apparatus’. To keep it in a safe condition and avoid risk of injury, the precautions detailed in the WARNINGS below should be observed. To avoid damage to the equipment the precautions detailed in the CAUTIONS should also be observed.

WARNING – ELECTRICAL HAZARDS

AC supply voltage. This equipment conforms with IEC Safety Class 1, meaning that it is provided with a protective earthing lead. To maintain this protection the mains supply lead must always be connected to the source of supply via a socket with an earthing contact. Make sure that the earth protection is not interrupted if the supply is connected through an extension lead or an autotransformer.

Before fitting a non-soldered plug to the mains lead cut off the tinned end of the wires, otherwise cold flowing of the solder could cause intermittent contact.

Do not use the equipment if it is likely that its protection has been impaired as a result of damage.

Fuses. Note that there is a supply fuse in both the live and neutral wires of the supply lead. If only one of these fuses should rupture, certain parts of the equipment could remain at supply potential.

Make sure that only fuses of the correct rating and type are used for replacement. Do not use mended fuses or short-circuited fuse holders.

To provide protection against breakdown of the supply lead, its connectors (and filter if fitted), an external supply fuse with a continuous rating not exceeding 6 A should be used in the live conductor (e.g. fitted in the supply plug).

Removal of covers. Disconnect the supply before removing the covers so as to avoid the risk of exposing high voltage parts. If any internal adjustment or servicing has to be carried out with the supply on, it must only be performed by a skilled person who is aware of the hazard involved.

Remember that capacitors inside the equipment, including any supply filter capacitors, may still be charged after disconnection of the supply. Those connected to high voltage points should be discharged before carrying out work inside the equipment.

WARNING – FIRE HAZARDS

Make sure that only fuses of the correct rating and type are used for replacement

If an integrally fused plug is used on the supply lead, ensure that the fuse rating is commensurate with the current requirements of this equipment. See under ‘Performance Data’ in Chapter 1 for power requirements.

WARNING – OTHER HAZARDS

Parts of this equipment are made from metal pressing, therefore it should be handled with due care to avoid the risk of cuts or scratches.

Some of the components used in this equipment may include resins and other materials which give off toxic fumes if incinerated. Take appropriate precautions, therefore, in the disposal of these items.

Beryllia (beryllium oxide) is used in the construction of transistor TR20 in unit AB1/1. This material, if incorrectly handled, could cause a danger to health – refer to the Service Manual for safe handling and disposal precautions.

CAUTION – LCD HANDLING

When using this equipment take care not to depress the front or rear faces of the display module as this may damage the liquid crystal display elements.

CAUTION – STATIC SENSITIVE COMPONENTS

This equipment contains static sensitive components which may be damaged by handling – refer to the Service Manual for handling precautions.



Declaration of Conformity

We: Marconi Instruments Limited
Longacres
St. Albans
Hertfordshire
England
AL4 0JN

as the manufacturer of the apparatus listed, declare under our sole responsibility that the product(s):

Title: 2022D 10 kHz - 1 GHz Signal Generator

to which this declaration relates are in conformity with the following standards or other normative documents:

Safety: IEC 348:1978 (BS4743)
EMC: EN55011:1991 Class B
EN50082-1:1992
EN60555-2:1987

and therefore conforms with the protection requirements of Council Directive 89/336/EEC relating to electromagnetic compatibility.

Issued on: 1 March 1993

Authorised by: _____



Harold Brown
Technologies Manager

Chapter 1

GENERAL INFORMATION

FEATURES

The 2022D is a light-weight synthesized signal generator having a frequency range of 10 kHz to 1 GHz and providing comprehensive amplitude, frequency and phase modulation facilities with an RF output level range of -127 dBm to +13 dBm. It is designed to cover a wide range of RF applications in development, production and maintenance. Output frequency is phase locked to an internal or external frequency standard and frequencies up to 100 MHz can be set to a resolution of 10 Hz, and above that to a resolution of 100 Hz.



Fig. 1-1 10 kHz to 1 GHz Signal Generator 2022D

Front panel operation is carried out by direct entry of required settings via the keyboard. Microprocessor control ensures flexibility, simplicity of use and allows programming by the General Purpose Interface Bus (GPIB).* This facility is offered as an option enabling the instrument to be used both as a manually operated bench mounted instrument or as part of a fully automated test system.

Output

Calibrated output levels from -127 dBm to +13 dBm are provided. A choice of ten output level unit combinations can be obtained on the front panel. The RF output level can be set to a resolution of 0.1 dB over the entire output voltage range. Protection against the accidental application of up to 50 W of reverse power is provided by a fast responding relay trip. Full protection is also provided when the instrument is switched off.

*GPIB: Marconi Instruments General Purpose Interface Bus in accordance with IEEE Standard 488 - 1978 and IEC Publication 625-1.

An RF level offset capability allows the output level to be varied relative to the indicated value to compensate for external cable losses or to ensure that all instruments in a particular area give identical results.

Modulation

Amplitude, frequency and phase modulation can be provided by internal or external sources. AM depth can be set in 0.5% steps up to 99.5%, FM deviation up to 999 kHz and phase modulation up to 9.99 radians. An auxiliary modulation input allows dual modulation to be applied for receiver testing. An internal modulation oscillator provides switch selected frequencies of 400 Hz, 1 kHz and 3 kHz.

Front panel

All data and units selected are visible on a single liquid crystal display. Data is entered on a keyboard that has been designed to be simple and logical to use. Carrier frequency, modulation and RF level functions may be incremented or decremented using the ↑ (UP) and ↓ (DOWN) keys. Non-volatile store and recall facilities are also provided using an electrically alterable read only memory that does not require a battery back-up system. A front panel cover for protecting the instrument in transit is available as an accessory.

Second function mode of operation

This enables a number of auxiliary functions such as setting the GPIB address, selection of alternative RF level calibration units, access to various calibration routines and an aid to diagnostic fault finding via the internal instrument bus.

PERFORMANCE DATA

Carrier frequency

Range:	10 kHz to 1 GHz.
Displayed resolution:	10 Hz up to 100 MHz, 100 Hz above 100 MHz.
Selection:	By keyboard entry.
Accuracy:	Equal to the frequency standard accuracy – see under 'Frequency standard'.
Indication:	7 digit LCD with units annunciation.

RF output

Level:	-127 to +13 dBm. (0.2 μ V to 2 V EMF). When AM is selected the maximum output power reduces linearly with AM depth to +7 dBm at maximum AM depth.
--------	---

Selection:	By keyboard entry. Units may be μV , mV EMF or PD; dB relative to 1 μV , 1 mV, 1 V EMF or PD; dBm. Conversion between dB and voltage units may be achieved by pressing the appropriate units key (dB or V, mV, μV).
Output impedance:	50 Ω , Type N female socket to MIL 39012/3D.
VSWR:	Better than 1.5:1 for output levels below -7 dBm.
Reverse power protection:	An electronic trip protects the generator output against reverse power of up to 50 W from a 50 Ω source and 25 W with a source VSWR up to 5:1 for frequencies from DC to 1 GHz. The trip may be reset from the front panel or via the GPIB. For safety the protection is also provided when the instrument is switched off.
Output level flatness:	Better than ± 0.5 dB from 10 kHz to 1 GHz for RF levels above -7 dBm.
Output level accuracy:	± 1 dB for output levels above -10 dBm. ± 2 dB for output levels below -10 dBm.
Displayed resolution:	0.1 dB or better over the entire voltage range.
Indication:	4 digit LCD with units annunciators.

Spurious signals

Harmonically related signals for output levels up to +7 dBm:	Better than -35 dBc (typically better than -40 dBc) for carrier frequencies up to 62.5 MHz. Better than -25 dBc (typically better than -35 dBc) for carrier frequencies above 62.5 MHz.
Sub-harmonics for output levels below 0 dBm:	None for carrier frequencies up to 500 MHz, better than -20 dBc for carrier frequencies above 500 MHz.
Non-harmonically related signals for output levels up to +7 dBm and at offsets from the carrier of 3 kHz or greater:	For carrier frequencies above 62.5 MHz, better than -70 dBc. For carrier frequencies below 62.5 MHz, better than -55 dBc in the band up to 150 MHz, and better than -40 dBc in the band above 150 MHz.

Single sideband
phase noise:

Typically less than -120 dBc/Hz at 470 MHz,
Typically less than -130 dBc/Hz at 150 MHz.

Residual FM:
(with FM off)

Less than 7 Hz RMS deviation in a 300 Hz to
3 kHz bandwidth from 250 to 499 MHz and
improving by approximately 6 dB per octave
with reducing carrier frequency down to
62.5 MHz.
Better than 3.5 Hz RMS below 62.5 MHz.

RF leakage:

Less than $0.5 \mu\text{V}$ PD generated in a 50Ω load
by a two turn 25 mm loop, 25 mm or more from
the case of the generator, with the output level
set to less than -10 dBm and the output
terminated in a 50Ω sealed load.

Frequency modulation

Range:

The maximum deviation available varies with
carrier frequency range as shown in the table
below:

Frequency range	Maximum deviation
500 MHz – 1 GHz	999 kHz
250 to 500 MHz	500 kHz
125 to 250 MHz	250 kHz
62.5 to 125 MHz	125 kHz
Below 62.5 MHz	100 kHz

Displayed resolution:

10 Hz for deviations up to 9.99 kHz.
100 Hz for deviations from 10 kHz to 99.9 kHz.
1 kHz for deviations from 100 kHz to 999 kHz.

Selection:

By front panel keyboard. Internal 400 Hz,
1 kHz or 3 kHz modulation or external input
may be selected.

Deviation accuracy:

$\pm 5\%$ of deviation ± 20 Hz at 1 kHz modulating
frequency excluding residual FM.

Frequency response:

± 0.5 dB from 50 Hz to 50 kHz relative to
1 kHz, using external modulation input.

With ALC off the low frequency response is
extended to 10 Hz with a peak deviation value
limited to the lower of 999 kHz or
[$0.047 \times \text{Modulation Freq. (in Hz)} \times \{\text{Carrier Freq. (in MHz)} + 160 \text{ (if Carrier Freq. is below 62.5 MHz)}\}$] kHz.

With ALC off can also be used for 10 Hz square wave switching with a peak deviation value limited to the lower of 999 kHz or 0.6 times the value obtained by the formula above.

Distortion:	Less than 2% total harmonic distortion at 1 kHz modulation frequency and maximum deviation for any carrier above 250 kHz. Less than 0.5% total harmonic distortion at 1 kHz modulation frequency for deviations up to 25 kHz for any carrier frequency above 250 kHz with ALC off.
External modulation:	With modulation ALC on, the deviation is calibrated for input levels between 0.9 V and 1.1 V RMS. A HI or LO message is indicated in the modulation display if the applied level is outside the range of the ALC. With modulation ALC off, the deviation is calibrated for an input level of 1 V PD.
Indication:	Input impedance is 100 k Ω nominal. 3 digit LCD with units annunciators.
Phase modulation	
Range:	Peak deviation from 0 to 9.99 radians.
Displayed resolution:	0.01 radian.
Selection:	By front panel keyboard. Internal 400 Hz, 1 kHz or 3 kHz modulation or external input may be selected.
Deviation accuracy:	$\pm 5\%$ of deviation ± 0.02 radian at 1 kHz modulating frequency excluding residual phase modulation.
Frequency response:	± 1 dB from 10 Hz to 10 kHz relative to 1 kHz using external modulation input and ALC off. ± 1 dB from 50 Hz to 10 kHz relative to 1 kHz using external modulation input and ALC on.
Distortion:	Less than 5% total harmonic distortion at 1 kHz modulating frequency and maximum deviation for any carrier frequency above 250 kHz.

External modulation:	With modulation ALC on the deviation is calibrated for input levels between 0.9 and 1.1 V RMS. A HI or LO message is indicated in the modulation display if the applied level is outside the range of the ALC. With modulation ALC off the deviation is calibrated for an input level of 1 V PD.
	Input impedance is 100 k Ω nominal.
Indication:	3 digit LCD with units annunciators.

Amplitude modulation

Range:	0 to 99.5%.
Resolution:	0.5%.
Selection:	By front panel keyboard. Internal 400 Hz, 1 kHz or 3 kHz modulation or external input may be selected.
Accuracy:	For peak output power levels up to +9 dBm: Better than $\pm(4\%$ of depth setting +1%) for 1 kHz modulating frequency and depths up to 95% for carrier frequencies up to 62.5 MHz. Better than $\pm(4\%$ of depth setting +1%) for 1 kHz modulating frequency and depths up to 80% for carrier frequencies up to 400 MHz.
Frequency response:	± 0.5 dB from 50 Hz to 15 kHz relative to 1 kHz at 80% depth using external modulation input, ALC on and DC coupled with ALC off.
Distortion:	Less than 3% total harmonic distortion at 1 kHz modulating frequency for depths up to 80% for carrier frequencies up to 400 MHz. Less than 5% total harmonic distortion at 1 kHz modulating frequency for depths up to 95% for carrier frequencies up to 62.5 MHz.
External modulation accuracy:	With modulation ALC on the modulation depth is calibrated for input levels between 0.9 and 1.1 V RMS. A HI or LO message is indicated in the modulation display if the level is outside the range of the ALC. With modulation ALC off the modulation depth is calibrated for an input level of 1 V PD. Input impedance is nominally 100 k Ω , DC coupled.
Indication:	3 digit LCD with units annunciators.

Modulation oscillator

Frequency:	400 Hz, 1 kHz and 3 kHz.
Selection:	By repetitive pressing of the INT MOD FREQ key.
Frequency accuracy:	$\pm 5\%$.
Distortion:	Less than 1% total harmonic distortion.
Indication:	One of three LEDs lights to indicate which frequency is selected.

Frequency standard

Internal or external frequency standard may be selected from the front panel. Annunciators show which is selected.

Internal frequency standard

High stability, oven controlled oscillator.

Frequency:	10 MHz.
Temperature stability:	Better than ± 0.05 ppm over the temperature range 0 to 40°C.
Aging rate:	Better than 0.3 ppm per year after one month's continuous use at constant ambient temperature.
Warm up time:	Within 0.5 ppm of final frequency 5 minutes from switch-on at ambient 20°C.

External frequency standard

External standard input:	Accepts a 10 MHz signal of at least 1 V RMS into a 100 Ω nominal impedance.
	A 5 MHz or 1 MHz signal can be accepted by changing an internal link. Connection is via a rear panel BNC socket.

Auxiliary inputs and outputs

Modulation input/output:	A front panel BNC socket provides an output from the modulation oscillator when internal modulation is selected and becomes the external modulation input when external modulation is selected.
Internal modulation oscillator output:	1 V $\pm 10\%$ EMF from a nominal 600 Ω source.
External modulation input:	Input level nominally 1 V RMS into 100 k Ω – see under 'Modulation' for details.
Alternative RF output socket:	A blanked hole is provided so that the RF output socket can be fitted to the rear panel.

Auxiliary modulation input: A rear panel BNC socket provides an auxiliary modulation input with a nominal sensitivity of 20% of the set modulation for a 1 V RMS input.

Input impedance 600 Ω nominal.

GPIB interface: A GPIB interface is available as an optional accessory and can be easily fitted by the user. All functions except the SUPPLY ON switch are remotely programmable.

Capabilities: Complies with the following subsets as defined in IEEE 488 - 1978 and IEC Publication 625-1: SH1, AH1, T6, TE0, L4, LE0, SR1, RL1, PP0, DC1, DT0, C0, E1.

Conditions of storage and transport

Temperature: -40°C to +70°C.

Humidity: Up to 90% relative humidity at 40°C.

Altitude: Up to 2500 m (pressurized freight at 27 kPa differential i.e 3.9 lbf/in²).

Rated range of use (over which the full specification is met)

Temperature: 0 to 55°C.

Safety: Complies with IEC Publication 348.

Radio frequency interference: Conforms with the protection requirements of the EEC Council Directive 89/336/EEC. Complies with the limits specified in the following standards:

EN55011 Class B	CISPR 11
EN50082-1	IEC 801-2, 3, 4
EN60555-2	IEC 555-2

Power requirements

AC supply: Switchable voltage ranges all, $\pm 10\%$:-
105 to 110 V, 115 to 120 V,
210 to 220 V, 230 to 240 V.
45 to 400 Hz.
70 VA max.

Dimensions and Weight

Height:	152 mm (6 in)
Width:	256 mm (10 in)
Depth:	367 mm (14.5 in) (Excluding handle projection)
Weight:	7.5 kg (16.5 lb)

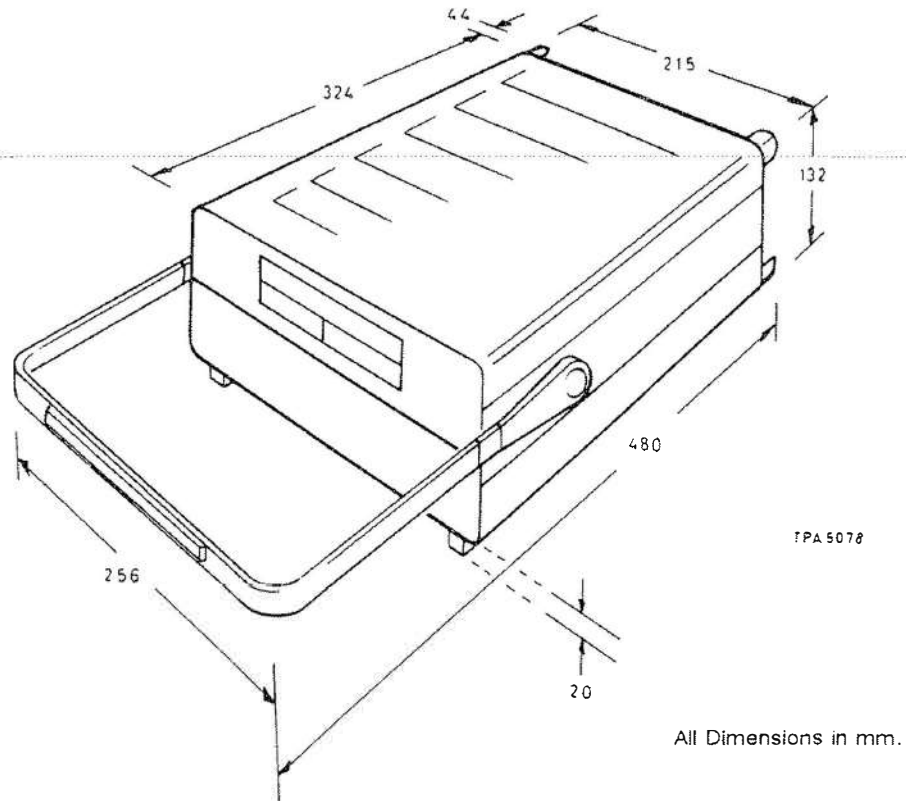


Fig. 1-2 Case dimensions

OPTIONS

001 : GPIB interface fitted.

ACCESSORIES

Supplied accessories

	Part no.
AC supply lead	43129-003W
Operating Manual H 52022-003X (Vol. 1)	46882-001W
Operating summary card	46882-003T

Optional accessories

	Part no.
Service Manual H 52022-003X (Vol. 2)	46882-002D
GPIB module	54433-003N
Front panel protective cover	54124-023J
Rack mounting kit single	46884-502Z
The GPIB Manual H 54811-010P (Contains details of general GPIB protocols)	46881-365R
GPIB lead assembly	43129-189U
Screened GPIB lead assembly (for enhanced RFI performance)	46883-962H
GPIB IEEE/EC connector adapter	46883-408K
RF coaxial cable (N to N type)	54311-095C
Coaxial adapter, type N to BNC	54311-092P
Impedance adapter 50/75 Ω (25 Ω series resistor) BNC	54411-051X
National Instruments Lab Window instrument drivers	59000-183S

Chapter 2

INSTALLATION

UNPACKING AND REPACKING

Retain the container, packing material and the packing instruction note (if included) in case it is necessary to reship the instrument.

If the instrument is to be returned for servicing attach a label indicating the service required, type or model number (on rear label), serial number and your return address including name of contact. Pack the instrument in accordance with the general instructions below or with the more detailed information in the packing instruction note.

- (1) Place supply lead in a suitable plastic bag and tape it to the instrument's rear panel, between the rear feet.
- (2) Spread the inner "wrap-round" padded fitting flat and place the instrument into this with the carrying handle folded underneath and the four feet positioned into the four holes provided.
- (3) Wrap the instrument with the packing all around and seal the two ends together with adhesive tape.
- (4) Position the two end cushion protecting pieces at either end of the outer packing carton, then slide the instrument within its inner wrap round protection into the outer packing carton. Close and seal the outer carton.
- (5) Wrap the container in waterproof paper and secure with adhesive tape.

Mark the package FRAGILE to encourage careful handling.

Note ...

If the original container or materials are not available, use a strong double-wall carton packed with a 7 to 10 cm layer of shock absorbing material around all sides of the instrument to hold it firmly. Protect the front panel controls with a plywood or cardboard load spreader with holes drilled to avoid the projecting RF output, mod in-out sockets and the supply on-off switch; if the rear panel has guard plates or other projections a rear load spreader is also advisable.

CONNECTING TO SUPPLY

Excessive temperatures may affect the instrument's performance; therefore completely remove the plastic cover, if one is supplied over the case, and avoid standing the instrument on or close to other equipment that is hot. Before connecting the instrument to the AC supply check the position of the two voltage selector switches on the rear panel. A locking plate fixes both switches into one of four possible combinations and reveals only the selected voltage range. The instrument is normally despatched with the switches set to 230/240 V. To select a different voltage range remove the locking plate and reposition the switches to the required range as shown in Fig. 2-1 and refit the locking plate.

Note ...

The AC supply fuse may also have to be changed. An indication of the correct fuse rating is given with each displayed voltage range:-

- i.e. 0.5 A-TT (time lag) for the 105 to 120 V ranges
- 0.25 A-TT (time lag) for the 210 to 240 V ranges

The fuses are 20 mm x 5 mm cartridge type.

The free AC supply cable is fitted at one end with a female plug which mates with the AC connector at the rear of the instrument. When fitting a supply plug ensure that conductors are connected as follows:-

Earth	-	Green/yellow
Neutral	-	Blue
Live	-	Brown

When attaching the supply lead to a non-soldered plug it is recommended that the tinned ends of the lead are first cut off to avoid the danger of cold flow resulting in intermittent connections.

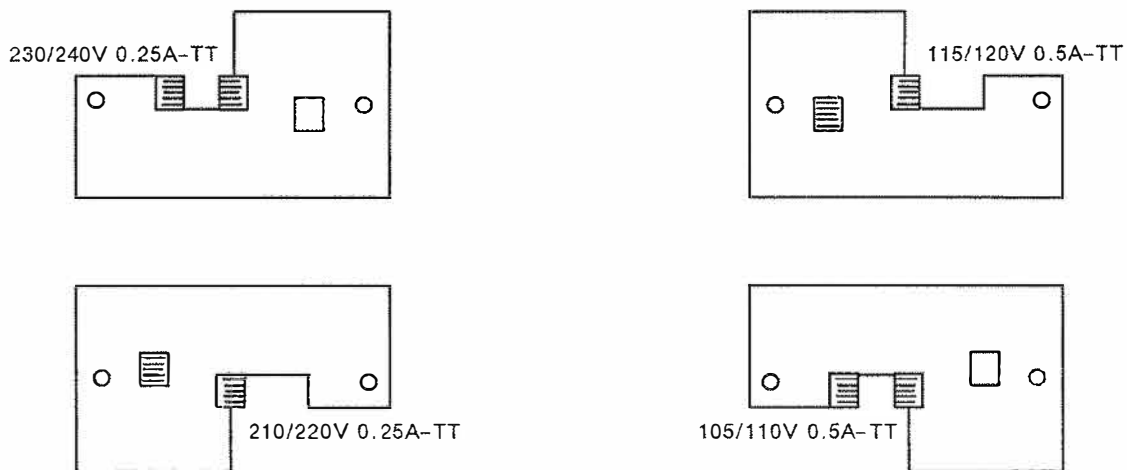


Fig. 2-1 Voltage ranges, showing switch and locking plate positions

SAFETY TESTING

Where safety tests on the AC supply input circuit are required, the following procedures can be applied. These comply with BS 4743 and IEC Publication 348. Tests are to be carried out as follows and in the order given, under ambient conditions, to ensure that AC supply input circuit components and wiring (including earthing) are safe.

(1) Earth lead continuity test from any part of the metal frame to the bared end of the flexible lead for the earth pin of the user's AC supply plug. Preferably a heavy current (about 25 A) should be applied for not more than 5 seconds.

Test limit : not greater than 0.5 Ω .

(2) 500 V DC insulation test from the AC supply circuit to earth.

Test limit : not less than 2 M Ω .

GPIB INTERFACE

The GPIB interface is fitted to the instrument when Option 001 is ordered and is also available as an optional accessory which can easily be fitted as follows:-

(1) Remove the rectangular cover plate from the right-hand side of the rear panel, withdraw the interconnecting lead and discard the cover plate but retain the fixing screws.

(2) Connect the GPIB interface assembly AD0 taking care that the ribbon cable connector SKP is correctly aligned with the connector PLP.

(3) Slide the GPIB assembly into the instrument, engaging top and bottom card guides, and switch the instrument on temporarily. Check that the front panel displays data correctly. If this is satisfactory switch off and continue with step (4); if, however, display data is corrupted, switch off and re-check the alignment of SKP and PLP.

(4) Secure the GPIB assembly into the instrument, engaging the top and bottom card guides, and fasten the assembly to the rear panel using the two screws removed in step (1).

(5) The interface is ready for GPIB operation after setting the appropriate talker/listener address - see Chap. 3 : 'Second function 2'.

(6) Connection to other equipment which has a 24-way bus connector to IEEE Standard 488 can be made with the GPIB lead assembly 43129-189U, available as an optional accessory. Where conformity with the radio frequency interference limits specified by VDE (Verband Deutscher Electrotechniker) is required, an alternative double screened GPIB lead assembly 46883-962H is available. An IEEE-to-IEC adapter 46883-408K is also available for interfacing with systems using a 25-way bus connector to IEC Recommendation 625 - see Fig. 2-2.

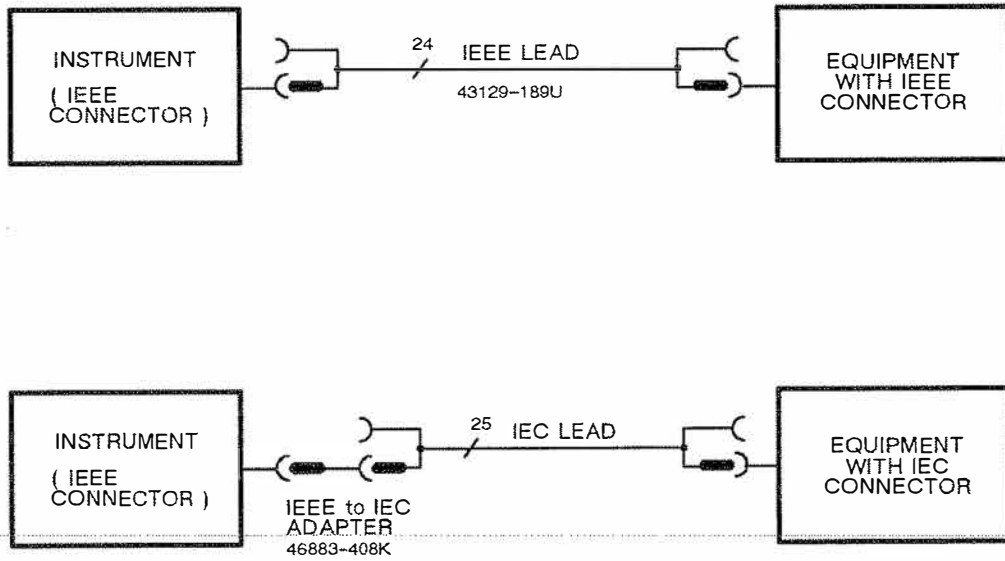


Fig. 2-2 GPIB interconnections

GPIB connector

The contact assignment of the GPIB cable connector and the device connector is as shown in Fig. 2-3.

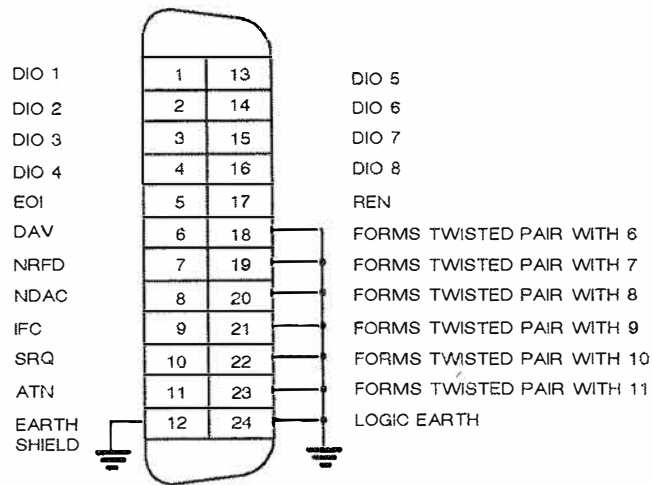


Fig. 2-3 GPIB connector contact assignments

RACK MOUNTING

The instrument may be mounted in a standard 19 inch rack as a single unit using the kit 46883-717K. This contains a pair of side angle plates wide enough to allow the instrument to sit centrally within the rack frame as shown in Fig. 2-4.

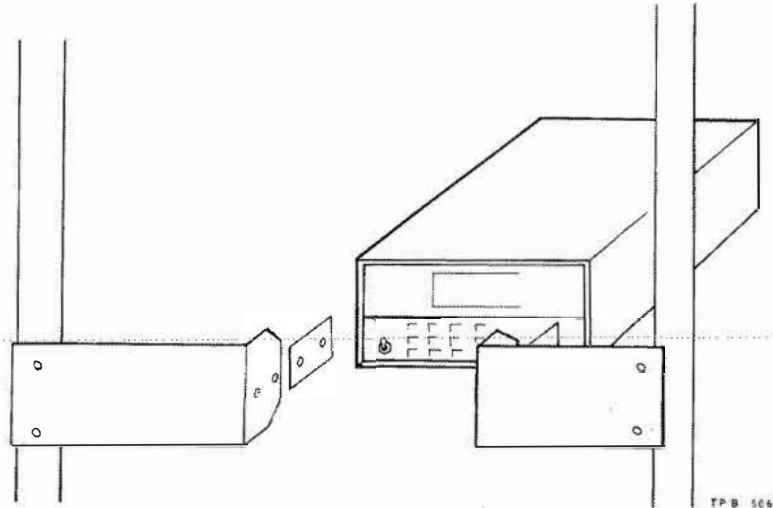


Fig. 2-4 Single unit rack mounting

If rear connection is required in a rack mounted system, the RF OUTPUT socket can be removed and repositioned on the rear panel - see the Service Manual for details.



Chapter 3 OPERATION

PRINCIPLES OF CONTROL

All operating functions of the generator are carried out from the front panel keyboard which is divided into five distinct colour coded areas. Remote operation from a GPIB controller is possible if the optional GPIB interface is fitted.

FRONT PANEL

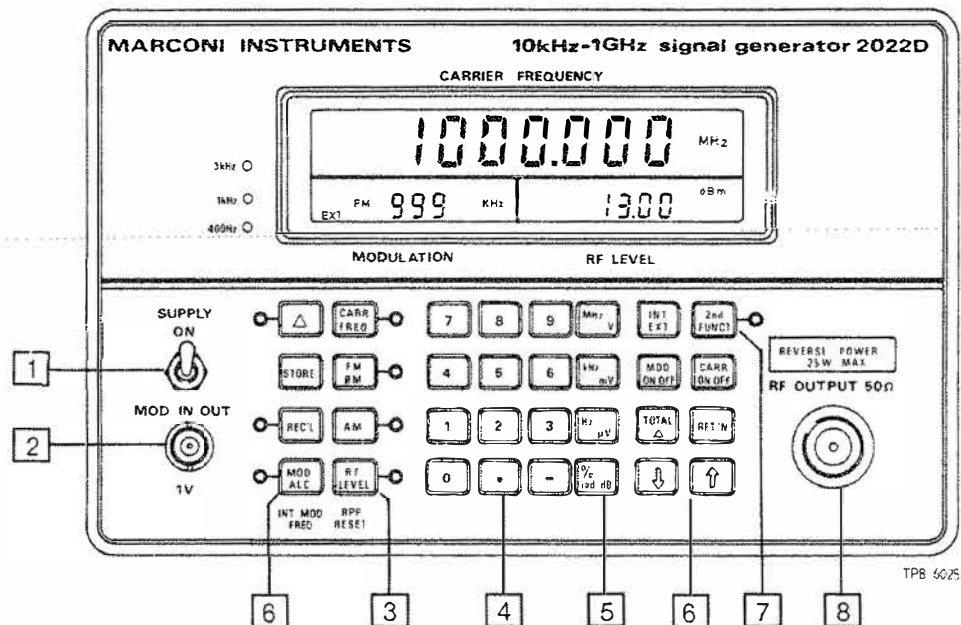


Fig. 3-1 Front panel controls

- ① **SUPPLY switch.** Applies the AC supply voltage.
- ② **MOD IN/OUT socket.** Provides a 600 Ω , nominal 1 V EMF output from the internal 1 kHz modulation oscillator or accepts a modulating input from an external source.
- ③ **Major function keys.** Six of the seven keys have an associated LED to indicate the function selected.
- ④ **Numerical keypad.** For entering numerical value for the function selected, including minus sign and decimal point.
- ⑤ **Units keys.** The four keys assign units of measure and also terminate the numerical entry.
- ⑥ **Miscellaneous functions.** The right-hand group of seven keys is for switching the carrier and modulation on or off, incrementing/decrementing and selecting internal or external modulation. One further key on the left selects modulation ALC and the internal modulation frequency.
- ⑦ **2nd FUNCT (blue).** This key with its associated LED accesses additional secondary control and calibration facilities.
- ⑧ **RF OUTPUT.** 50 Ω N type output socket with reverse power protection.

REAR PANEL

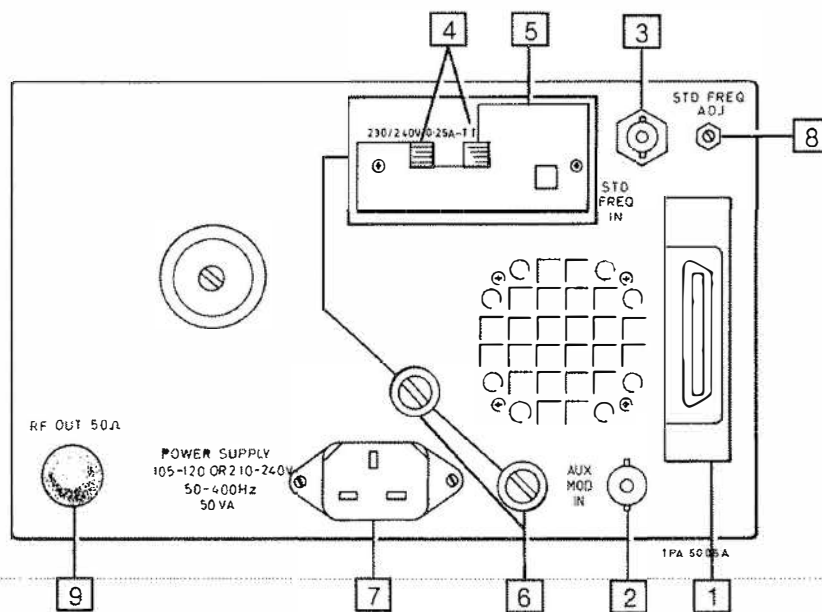


Fig. 3-2 Rear panel layout

- ① **REMOTE CONTROL GPIB INTERFACE.** This optional accessory allows remote control of the instrument. Accepts a 24-way IEEE GPIB connector.
- ② **AUX MOD IN.** A BNC socket which accepts an auxiliary external modulating signal. An input of 1 V RMS produces a secondary modulation at 20% of the indicated primary modulation.
- ③ **STD FREQ IN.** A BNC socket which allows an input from an external 10 MHz standard frequency (or 1 MHz or 5 MHz after resetting an internal link).
- ④ **VOLTAGE SELECTOR switches.** A combination of four positions which select ranges of 105/110 V, 115/120 V, 210/220 V or 230/240 V, each with a 10% tolerance to afford a complete cover over the ranges 95 to 132 V and 190 to 264 V.
- ⑤ **Selector switch plate.** Can be turned and/or reversed to secure the VOLTAGE SELECTOR switches in one of four pre-selected positions.
- ⑥ **AC fuses.** Supply input fuses are rated at 0.25 A (time lag) for the 190 V to 264 V range or 0.5 A (time lag) for the 95 V to 132 V range.
- ⑦ **AC supply input.** The AC supply is connected through this plug which mates with the connector fitted to the supply lead.
- ⑧ **STD FREQ ADJ.** Allows the internal standard to be set against a primary external standard.

CAUTION ...

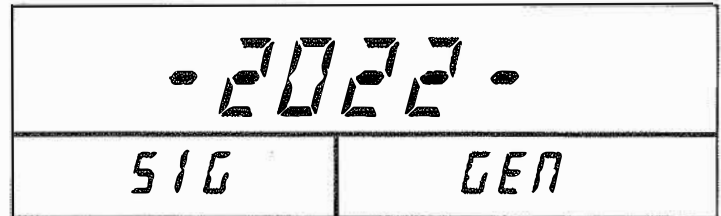
Incorrect adjustment of this preset will impair the frequency accuracy of the generator and it should therefore only be adjusted by an authorized recalibration unit.

- ⑨ **RF OUT.** This blanked hole provides alternative connector locations when the instrument is rack mounted. Fitting instructions are included in Chap. 5 of the Service Manual.

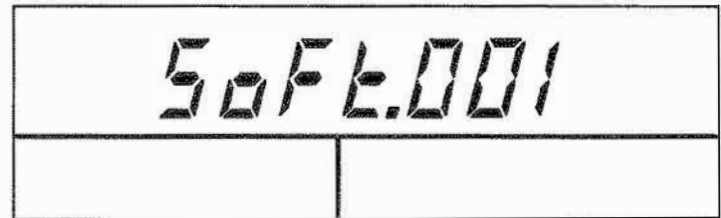
PREPARATION FOR USE

- (1) Switch SUPPLY ON and note that the following three display patterns appear in sequence:

- (i) Instrument type no.



- (ii) Software issue no.



- (iii) Initial operating mode

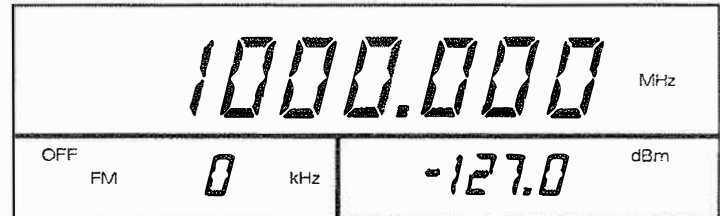


Fig. 3-3 Switch-on displays

Note ...

If second function 16 was in use before the instrument was switched off, the contents of store 10 will be recalled as the initial operating mode instead of the default conditions shown in Fig. 3-3. If store 10 contents are recalled when display blanking (second function 197) is on, none of the settings will be visible. Use REC'L 00 to obtain a visible display.

- (2) Check that the CARRIER FREQUENCY window does not indicate EXT STD, unless an external frequency standard is being used. If this has been inadvertently selected error 11 will be displayed, in which case press CARR FREQ and INT/EXT keys to reselect internal frequency standard.
- (3) During normal operation the instrument's internal reference standard will give an accuracy within the rated performance after a warm-up period of 5 minutes at normal ambient temperatures.

OPERATING PROCEDURES

The general procedure for selecting a numerical parameter such as frequency, modulation or RF level is to enter the following sequence:

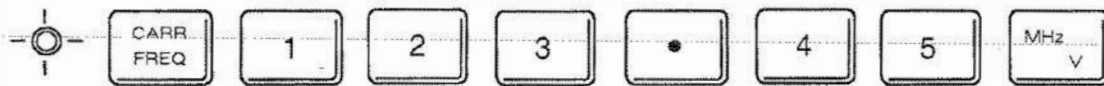
FUNCTION key which lights the adjacent LED.

NUMERICAL VALUE keys including decimal marker and negative sign if required.

UNITS key which acts as terminator.

If an error is made while keying clear the entry by re-selecting the function key. If value entered is outside the rated range, the instrument will set to the nearest end-of-range value.

CARRIER FREQUENCY



Press the CARR FREQ key (unless its LED is already lit). Enter the required value via the numerical key pad and note that the data entered appears in the CARRIER FREQUENCY display. Terminate the instruction by pressing the MHz, kHz or Hz key.

Carrier on/off



The carrier may be switched off or on at any time by pressing the CARR ON-OFF key.

Internal/external frequency standard



At switch-on the instrument will set to either internal or external frequency standard, depending on its last state before switch-off. External standard control is indicated by the annunciator EXT STD in the CARRIER FREQUENCY display. Pressing the INT/EXT key will toggle between internal and external standard.

When INT is selected, the frequency is controlled by an internal high stability 10 MHz crystal controlled oscillator.

When EXT is selected, an external 10 MHz* signal of at least 1 V RMS is required at the rear panel STD FREQ IN socket. The instrument will lock automatically to this signal.

*Or 1 MHz or 5 MHz after resetting an internal link - for details see Service Manual.

Error no. 11 is displayed in the CARRIER FREQUENCY window if the input is of incorrect level (or not connected).

Error no. 12 is displayed if the input frequency is outside the locking range. This error message may also be displayed when the instrument is initially switched on until such time as the internal frequency standard synchronizing circuits have locked to the external frequency standard input. This will take approximately one minute. Subsequent reselections made when the instrument is at or near to its operating temperature will not incur this delay and therefore the error message will not then be displayed.

RF LEVEL



Press the RF LEVEL key and enter the required value including any decimal point or minus sign. The terminator keys give a choice of 3 linear units : volts, millivolts and microvolts and a logarithmic unit (decibels). These units can be further qualified by second function 14 – see page 3-15 – which offers the choice of EMF or PD and allows the logarithmic units to be expressed in dB μ V, dBmV or dBm.

The units in use will be shown on the RF level display. If the level requested is too high at the currently set AM depth then the RF level is set to the maximum available and a warning is given in the form of a flashing colon symbol (:) to the left of the RF LEVEL display.

Note ...

To convert an RF level indication from linear to log units or vice versa, simply press the new units key. For example, to convert an indication in mV to dBm press the dB key.

Reverse power protection

Accidental application of reverse power to the RF OUTPUT socket will trip the reverse power protection (RPP) unit and the REV PWR annunciator will flash on the RF LEVEL display. During this time the keyboard will not respond except to reset commands.

After the source of power has been disconnected reset the RPP by pressing the RF LEVEL function key. Attempting to reset the RPP with power still applied will result in the RPP tripping again.

When the instrument is switched OFF, the output socket is automatically disconnected from the output attenuator a further safety feature.

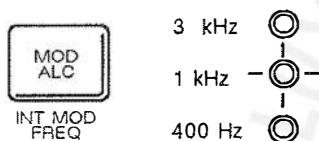
Operation with 75 Ω loads

The performance specification for the instrument assumes operation into 50 Ω loads, but often it is desirable to work into mismatched loads. This is in general possible although an uncertainty of performance may be introduced. In the particular case of a 75 Ω load, this can be accurately matched for carrier frequencies up to 500 MHz by using the 50/75 Ω Impedance Adapter, Part No. 54411-051X, offered as an optional accessory. This 25 Ω series load maintains the correct (open circuit) voltage calibration and allows the reverse power protection circuit to function correctly.

MODULATION

Internal modulation source

In the internal modulation mode, pressing the MOD ALC/INT MOD FREQ key causes the internal modulation oscillator to sequence through its available frequencies (400 Hz, 1 kHz and 3 kHz). Press the key repeatedly until the required modulation frequency is obtained.



In the internal modulation frequency mode, pressing the MOD ALC/INT MOD FREQ key causes the internal modulation oscillator to sequence through its available frequencies (400 Hz, 1 kHz and 3 kHz). Press the key repeatedly until the required modulation frequency is obtained.

External modulation



The instrument normally powers up in the internal mode. To select external modulation press the INT/EXT key after selecting the AM or FM/ Φ M function. This will set the EXT annunciator in the MODULATION display. Press the INT/EXT key again to return to internal modulation.



If external modulation has been selected the modulating signal can be set internally to the correct level (provided the applied voltage is between 0.9 V and 1.1 V) by pressing the MOD ALC key. If the input is outside the range of the ALC system either a HI or LO message will indicate this in the MODULATION display. Selection is indicated by the adjacent LED. The instrument will normally power up with MOD ALC off when in the external modulation mode. The modulation ALC is always on in the internal modulation mode.

Auxiliary modulation

A rear panel BNC socket (AUX MOD IN) allows an external modulation signal to be applied at the same time as the normal internal or external modulation source. A signal level of 1 V RMS at this socket will produce 20% of the indicated modulation setting. For example if the 2022D is set to produce 5 kHz deviation using the internal 1 kHz source and a 1 V RMS signal is applied to the AUX MOD IN socket the combined deviation will be 6 kHz.

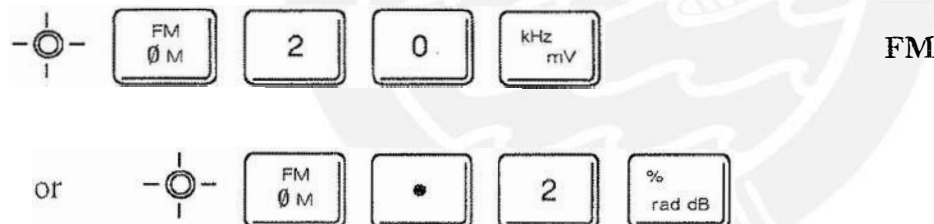
The auxiliary modulation facility is particularly useful for tests on radio receivers when a low level sub-audible signalling tone needs to be applied in addition to the normal modulation.

Amplitude modulation



Press the AM function key (unless its LED is already lit). Enter the required value of modulation depth followed by the % terminator. If the requested value of AM exceeds that allowed by the current RF level setting then the level is reset to the maximum available for the AM depth selected and a warning is given in the form of a flashing colon symbol to the left of the RF LEVEL display.

Frequency or phase modulation



Press the FM/ΦM function key (unless its LED is already lit). Enter the required value of deviation followed by a terminator (MHz, kHz or Hz for FM; RAD for ΦM).

When the first digit of a new setting is entered both FM and ΦM annunciators are set; pressing the terminator key removes the unwanted annunciator. To change from FM to ΦM or vice versa press the FM/ΦM key again, re-enter data and re-select the required terminator key. If the requested FM deviation exceeds that allowed by the current carrier frequency setting, the deviation is set to the maximum available.

MOD
ON-OFF

To turn FM or ΦM off whilst still retaining the current value of entered deviation, (for example in signal-to-noise ratio measurements) press the MOD ON/OFF key. The off condition is indicated by the setting of an OFF annunciator in the MODULATION display. Entering a new value of deviation will automatically restore the modulation.

INCREMENTS

Assigning increment values

To display the current set of increment values press the Δ (delta) key. Unless the values have been changed as below, the following default set will be displayed.

Carrier frequency: 1 kHz
Modulation: FM 1 kHz or Φ M 0.1 rad or AM 1%
RF level: 1dB

To return to the normal display without affecting the current increment values press any function key twice.



To change the increment value of any function press the Δ key followed by the function key; then enter the new value and the terminator. For example to select a carrier frequency increment of 10 kHz follow the sequence shown above. FM, Φ M, AM or RF LEVEL may be similarly incremented but note that for RF LEVEL increments the only valid terminator is the dB key.

Applying increments



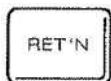
Each press of the \uparrow (UP) key increments the function parameter by the selected value; likewise pressing the \downarrow (DOWN) key decrements by a similar amount.

Holding the UP or DOWN key pressed results in continuous incrementing or decrementing after a delay of one second.

To change from the incrementing mode to the decrementing mode without the one second delay keep the UP key continuously pressed, allowing the instrument to increment, then press the DOWN key also. When the UP key is released the instrument will immediately decrement. Similarly, to change from down to up without delay press the UP key before releasing the DOWN key, and when the DOWN key is released the instrument will immediately increment.

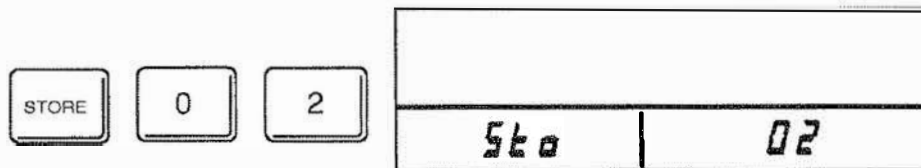


To find the total shift from the original setting press the TOTAL Δ key. While this key is pressed all the displays will show the total shift of each function from its starting value. To return to the initial value of the selected function press the RET'N key.

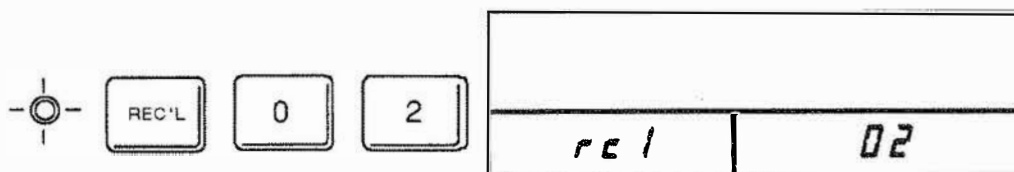


STORE AND RECALL

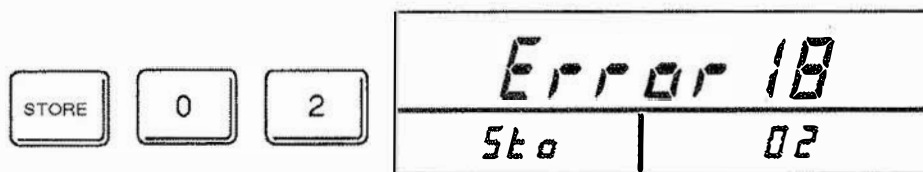
The instrument has 100 non-volatile stores available. Stores numbered 00 to 19 store complete instrument settings (including increment values). Stores 20 to 99 store settings of carrier frequency only.



To store press STORE followed by a two-digit numeric entry. Holding the last entered digit key pressed will keep the store number on the display. The command will be executed only when the key is released.



To recall press REC'L followed by the appropriate two digit numeric entry. Increment or decrement keys can then be used to sequence the recall of stores if required. Pressing the RET'N key will recall the first store selected before incrementing or decrementing took place.



If an attempt is made to store values when second function 196 (protection of store settings) is in operation, this will not succeed and error message 18 will be displayed as shown above. A list of error numbers is given on page 3-24. Also if second function 197 (display blanking) is in operation only the numerals of the stored or recalled store will be displayed in the RF LEVEL window. Further details of second functions 196 and 197 (both of which are second degree protected) are contained in the Service Manual.

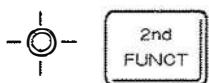
SECOND FUNCTIONS

Second function operations provide a means of controlling various secondary features and calibrations within the instrument. Access to many of these operations is generally not required during routine use of the instrument and some should only be accessed by skilled personnel during the course of realignment, fault finding or repair. There are three levels of operation as follows:

Normal operation. Second functions accessed by a single key entry (0–9) are unprotected.

First level operation. Second functions accessed by a two key entry (10–18) have first degree protection. Access to this level can be gained after operating an unlocking procedure – see ‘Second function 0’.

Second level operation. Second functions accessed by a three key entry (190–199) have second degree protection and can only be accessed by the operation of a special key code. Details of the code are given in the Service Manual.

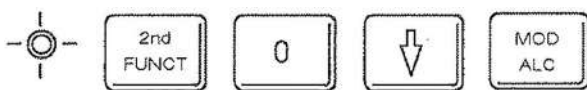


In general the second function mode is entered by pressing the blue 2nd FUNCT key followed by a number corresponding to the second function required. Pressing the 2nd FUNCT key inhibits the action of some keys, but the instrument can always be restored to its normal operating mode by pressing any of the function keys. This means of exit from second function operation is always safe, – it will not corrupt any data or alter any status bits, and the displays will revert to their normal functions.



No data will be permanently altered unless the STORE key is pressed. The operation of each of the secondary functions is as follows:-

Second function 0: ‘Unlock’



Switching on the instrument automatically locks all second functions that have a first or second degree of protection. Access to first level operation is obtained by the UNLOCK procedure:-

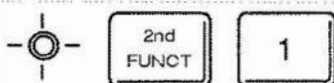
- (1) Press 2nd FUNCT and ‘0’ keys, and note that ‘0’ is displayed in the RF LEVEL window.
- (2) Then press the ↓ and MOD ALC keys simultaneously until ‘1’ is displayed in the FREQUENCY window (this will take approximately 5 seconds).

The instrument will then be unlocked to enable selection of the required second function within the first level group. If the sequence is in error, or aborted part way through, the instrument will remain locked. Once unlocked the instrument remains so until either the 2nd FUNCT and '0' keys are once more pressed or until the instrument power is switched off.

Note ...

Access to all second functions is always available over the GPIB (where fitted). Access to second functions via GPIB selection should be restricted to personnel who have a full knowledge of these operations and require access to them in the course of realignment, fault finding or repair only. If inadvertent selections are made it is possible to invalidate the instrument's calibration.

Second function 1: 'Status'



Entering 2nd FUNCT followed by the numeral 1 key will result in the instrument displaying status information as shown in Fig. 3-4.

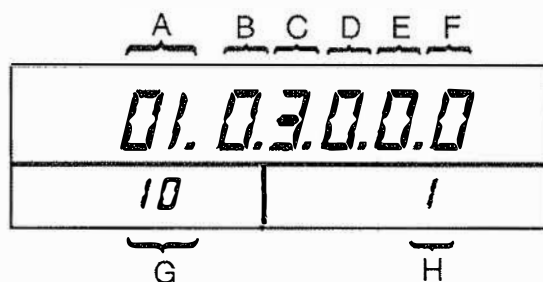


Fig. 3-4 'Status mode' display

where	A = GPIB address:	00 to 30
	B = Offsets:	'0' = off '1' = on (see second function 15)
	C = Level units code:	0 to 9 (see second function 14)
	D = Stores/offsets locking:	'0' = stores and offsets unlocked '1' = stores locked, offsets unlocked '2' = stores unlocked, offsets locked '3' = stores and offsets locked (see second function 196 in Service Manual)
	E = Display blanking of recalled stores:	'0' = off '1' = on (see second function 197 in Service Manual)

F = Protection level: '0' = unprotected
 '1' = first level
 '2' = second level

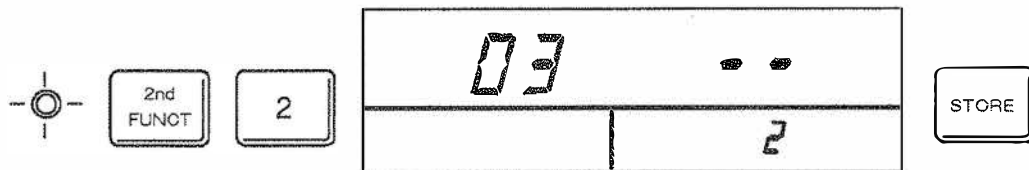
G = Ext. frequency standard: 1, 5 or 10 MHz
 (see second function 10)

H = Indication of second function number currently selected.

GPIB data output in response to QU command when the 2022D is addressed to talk gives the following string, with ' ' indicating a space:-

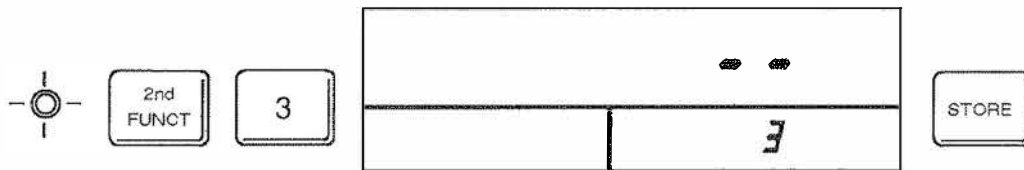
AA₁B₂C₃D₄E₅F₆ GG

Second function 2: 'GPIB address setting'



If the GPIB option is not fitted the sign "--" is displayed in the CARRIER FREQUENCY display; otherwise the current GPIB address is displayed. If a new address is required, this may be entered via the keyboard. Numbers rotate in from the right. When the required address is displayed pressing STORE key will, if the address is acceptable (00 – 30), replace the previous one. If the address is invalid it will be ignored and the current address re-displayed. The GPIB address is stored in the non-volatile memory.

Second function 3: 'Manual latch setting'



This function allows a 6 or 8 bit binary instruction to be directed to any of the instrument's internal latches for testing and fault finding. This facility is fully described in the Service Manual and is an invaluable aid when diagnosing internal instrument bus or latch faults. On exiting from second function 3 all latch data which may have been over-written is restored.

Second function 4: 'SRQ mask setting'

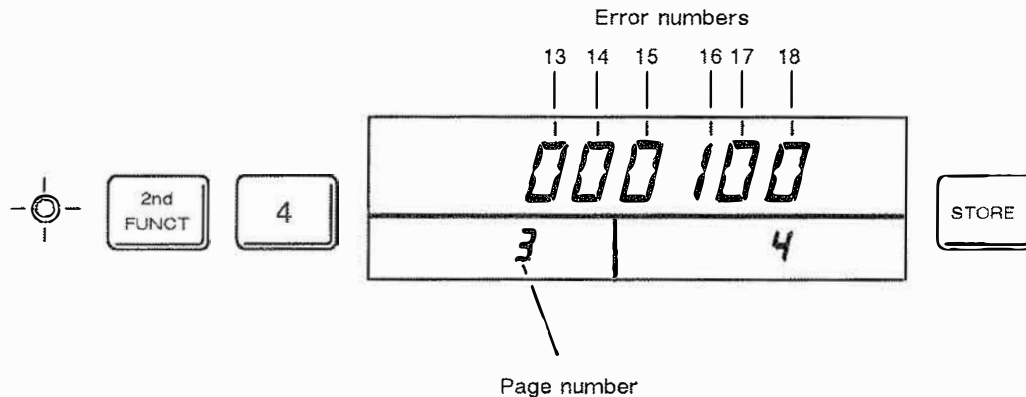


Fig. 3-5 SRQ mask setting display

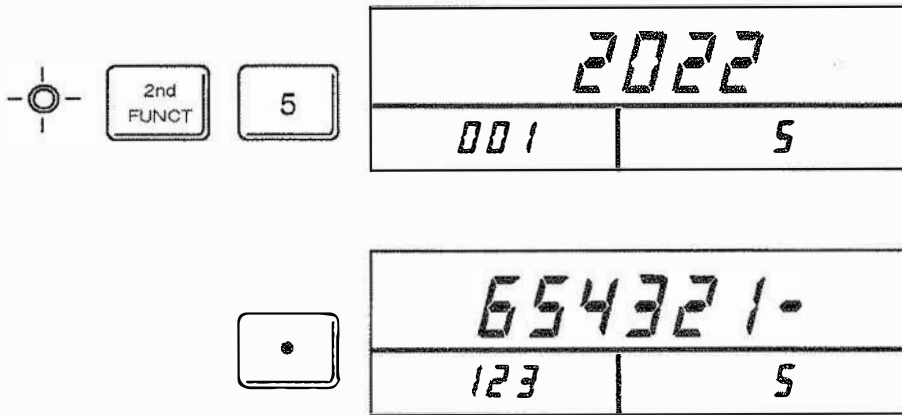
Select 2nd FUNCT followed by numeral 4. The SRQ mask allows an instruction to be made for the 2022D *not* to request service over the GPIB for particular conditions. Error numbers are listed from 1 to 18 inclusive. At switch on all error numbers are unmasked '0'. Selection of second function 4 gives a six bit binary number in the frequency display.

To access all 18 error numbers three 'pages' are required. At switch on (default mode) page 1 is selected and the page number indicated in the modulation display. Error numbers 1 - 6 are represented in the frequency display, the lowest error on the left of the display.

To move to page 2 press the '.' (decimal point) key; the MODULATION display now indicates page 2 and error numbers 7 - 12 are represented from left to right. Again press the decimal point to give access to page 3 representing error numbers 13 - 18. Pressing the decimal point a further time will return you to page 1.

Ones and zeros are entered via the keyboard and rotate in from the right. Enter a bit '1' to mask the desired error and when in position press the STORE key. For more information on the significance of each digit see the paragraph - Error numbers (page 3-24). Fig. 3-5 shows the mask set to ignore a GPIB bus error (Error No. 16).

Second function 5: 'Read identity string'

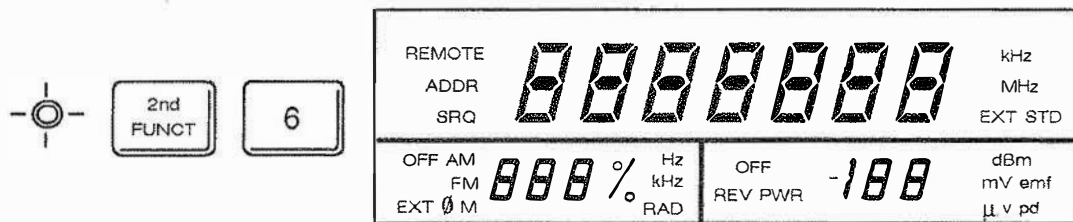


Selection of this facility enables you to confirm the instrument type number, then after pressing the decimal point, its serial number e.g. 2022, Ser. No. 654321-123. If QU command is sent via the optional GPIB interface the following string is put into the output buffer:

2022D 001 654321-123

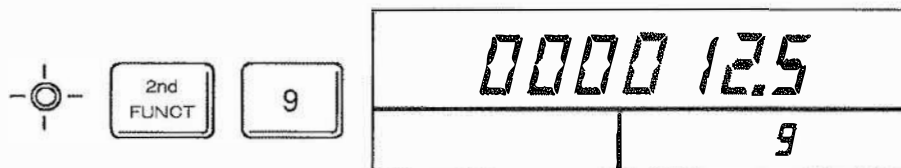
Software issue number (001), although not displayed, is inserted between type and serial number in the string.

Second function 6: 'Test display'



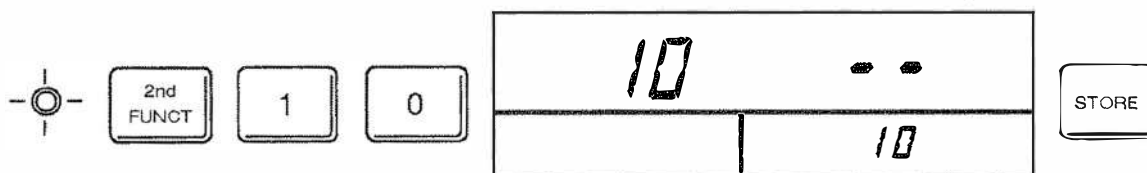
Select 2nd FUNCT followed by numeral 6. All display components are then set to give confirmation of the back-plane drive and LED operation, and also the CMOS logic and LCD segments on the CARRIER FREQUENCY, MODULATION and RF LEVEL displays.

Second function 9: 'Read elapsed time'



This facility enables you to observe the total number of instrument running hours from the last reset. It may be used to indicate, for instance, calibration intervals. The elapsed time is as shown above and has a resolution of 0.5 h. Display characters are not updated while being viewed. The elapsed time can be reset to zero – see Service Manual for details.

Second function 10: 'Record external frequency standard choice'



This facility enables the choice of external frequency standard (1, 5 or 10 MHz as set by the position of the internal link) to be recorded and displayed in the status display mode second function 1. Unlock the instrument to the first level of operation by means of the unlocking procedure – see second function 0. Then select 2nd FUNCT 10 followed by numeral(s) 1, 5 or 10 as appropriate and the STORE key.

Note ...

This function merely records, but does not change, the frequency accepted.

Second function 11: 'Read identity string'



This facility is the same as second function 5 and provides identical display features but is first degree protected. Unlock the instrument to the first level of operation by means of the unlocking procedure – see second function 0. Then select 2nd FUNCT followed by numerals 11.

The purpose of second function 11 is to provide compatibility with Signal Generator 2018A where an identical second function 11 facility allows commonality with GPIB controller instructions. As described in second function 5, if QU is sent via the GPIB the following string is placed in the output buffer, e.g. 2022D 001 654321-123, to confirm the instrument type, software issue and serial number.

Second function 12: 'Write user definable string'

This is a GPIB only facility which enables you to store a string of up to 32 ASCII characters in a non-volatile memory. The second function number is displayed in the RF LEVEL display. Up to 31 ASCII characters can be accepted and then terminated by <lf>. Follow this with ST command to store,

e.g. SF12 – This is a user-defined string <cr> <lf> ST
would store 'This is a user-defined string'.

If an attempt is made to store too many characters then <lf> is automatically inserted as the 32nd.

Second function 13: 'Read user definable string'

This facility provides a means of reading back data set by means of SF12 write facility and is again a bus only facility. The second function number is displayed in the RF LEVEL display and in response to QU command places the user defined string into the GPIB output buffer.

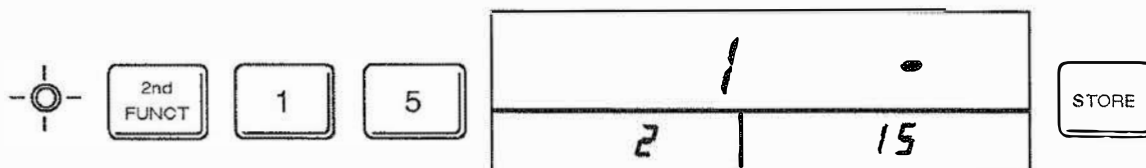
Second function 14: 'RF level units setting'



Unlock the instrument to the first level of operation by means of the unlocking procedure – see second function 0. Then select 2nd FUNCT followed by the numerals 1 and 4. On entering second function 14 a digit is displayed in the FREQUENCY window as shown above. This is the code number for the current RF level units, as shown in the table below. To change the units press the new unit code number. Then press STORE to terminate the entry.

Unit code	Logarithmic unit	Linear unit
0	dBmV EMF	} EMF
1	dB μ V EMF	
2	dBmV PD	
3	dB μ V PD	
4	dBm	
5	dBmV EMF	} PD
6	dB μ V EMF	
7	dBmV PD	
8	dB μ V PD	
9	dBm	

Second function 15: 'RF level offsets'



In addition to the standard calibration for RF output level, the instrument has a capability for overall level adjustment to facilitate matching with other equipment. The output level can be raised or lowered by approximately 2 dB in the offset mode. First select a carrier frequency within the chosen band followed by a suitable RF level.

Complete the unlocking procedure – see second function 0. Then select 2nd FUNCT followed by numerals 1 and 5. There are three carrier frequency bands, <250 MHz, 250–500 MHz and 500–1000 MHz, which are identified in the modulation display as 1, 2 or 3 respectively. One offset value may be set for each frequency band.



Selection of offsets 'on' is made with the numeral 1 key, or 'off' with the 0 key. Indication of the selected state is shown with either 1 or 0 in the CARRIER FREQUENCY display. Either terminate the selection by pressing the STORE key, or before doing so set a value of offset in the following manner.

Ensure offset 'on' (1) is selected and then press the ↑ (UP) key or the ↓ (DOWN) key to increment or decrement the RF level by 0.1 dB. Each successive operation of the key will increment/decrement the RF by a further 0.1 dB. When sufficient offset has been determined press the STORE key to terminate the selection which will, together with the offsets 'on' selection, remain valid until further adjustment is made.

Note ...

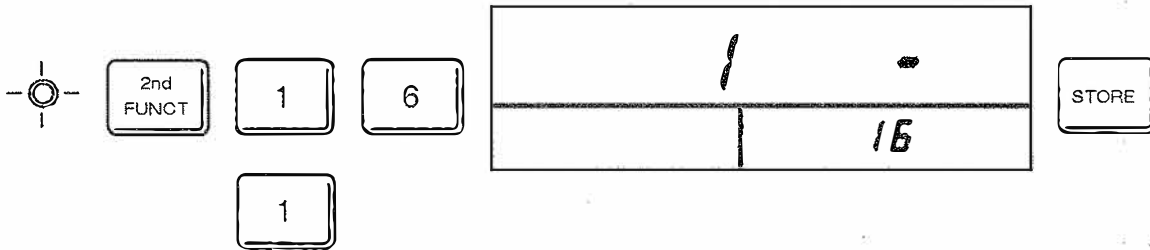
If error 18 appears while setting offsets, this indicates that the offset store has been protected by second function 196.

If an offset value of +0.1 dB is selected when the instrument is set to the limit of its operating range, i.e. +13 dBm or equivalent, a maximum RF level of +12.9 dBm will be displayed (a further +0.1 dB offset increment will decrease this to +12.8 dBm).

Note ...

When an offset value has been selected and stored it will remain valid for all subsequent power on sequences. RF level accuracy of the instrument may therefore be impaired and care should be taken to account for this.

Second function 16: 'Recall STORE 10 at switch on'



This facility allows the instrument to be operated in a remote or unattended location with a pre-selected set of conditions which will remain unchanged in the event of inadvertent switching off and on of the input supply voltage. If this were to happen in the normal operating mode, the instrument would resume the initial operating mode, that is CARRIER FREQ 1000 MHz, INT MOD, no MODULATION and minimum RF LEVEL (-127 dBm or equivalent). These conditions can be superseded by storing the required operating conditions in STORE 10 and carrying out an automatic recall of the STORE 10 settings using the second function 16 mode.

- (1) First select the required CARRIER FREQ, MODULATION and RF LEVEL settings at the keyboard.
- (2) Press the STORE key followed by the numerals 10.
- (3) Complete the first level unlocking procedure – see second function 0. Then select 2nd FUNCT and numerals 1 and 6. Follow this by selecting the recall store 10 mode (numeral 1). Finally press the STORE key to terminate the entry.

If the supply voltage is interrupted and then restored, the instrument will automatically carry out a RECALL 10 instruction and reset to the STORE 10 conditions previously set. To disable the facility first unlock the instrument to first level operation, select 2nd FUNCT 16 followed by the numeral 0, and finally the STORE key. If second function 197 is in use all information normally shown on the front panel will be blanked. Details of this facility are given in the Service Manual.

Second functions 190 – 199: (Second level operation)

The following facilities all have second degree protection. Further information on these and details of the special key code used to unlock to this level are contained in the Service Manual.

Second Function	Facility
190	Identity string setting
191	FM tracking calibration
192	RF level calibration
193	Voltage tuned filter (VTF) calibration
194	AM calibration
195	Set checksum
196	Protection of store and offset settings
197	Display blanking of recalled stores
198	Read total instrument operating time
199	Reset elapsed time

GPIB FUNCTIONS

The GPIB interface, which is an optional accessory, allows the instrument to be coupled to a controller. The essential purpose of the GPIB function is described below. Further information on the general features and applications of the GPIB system can be obtained from 'The GPIB Manual' offered as an optional accessory.

The 2022D has both talker and listener capabilities. One address is used for both talking and listening and is set via the front panel or via the GPIB using second function 2. The instrument can request service (assert SRQ) on certain error conditions under the control of an SRQ mask which is set using second function 4.

SH1 : Source handshake (complete capability)

The source handshake sequences the transmission of each data byte from the instrument over the bus data lines. The sequence is initiated when the function becomes active, and the purpose of the function is to synchronize the rate at which bytes become available to the rate at which accepting devices on the bus can receive the data.

AH1 : Acceptor handshake (complete capability)

The acceptor handshake sequences the reading of the data byte from the bus data lines.

T6 : Talker function (no talk only function)

The talker function provides the 2022D with the ability to send device dependent messages over the bus to the controller. The ability of any device to talk exists only when it has been addressed as a talker.

L4 : Listener function (no listen only function)

The listener function provides a device with the ability to receive device dependent messages over the bus. The capability only exists where the device is addressed to listen via the bus by the controller.

SR1 : Service request function (complete capability)

The service request function gives the 2022D the capability to inform the controller when it requires attention.

RL1 : Remote/local function (complete capability)

The remote/local function allows the 2022D to be controlled either by the local front panel keys or by device dependent messages over the bus.

DC1 : Device clear function (complete capability)

Device clear is a general reset and may be given to all devices in the system simultaneously (DCL) or only to addressed devices (SDC). 2022D resets to the default power-up mode, that is:

Maximum carrier frequency (1000 MHz)
 No AM, FM or Φ M
 Minimum RF level (-127 dBm or equivalent)
 Internal modulation at 1 kHz rate
 Increment settings:

Carrier frequency: 1 kHz
 Modulation: 1 kHz FM, 0.1 rad Φ M or 1% AM
 RF level: 1 dB

Note...

The instrument settings following Device Clear on Selective Device Clear are not affected by the settings of second functions 16 or 197.

Before these conditions are set, a checksum is calculated for the calibration data (FM tracking and RF level) and referred to a number held in the non-volatile memory. If this test of calibration validity fails, the instrument responds by asserting SRQ. The status byte will contain the error number 7 to signal a calibration data fault in addition to the 'SRQ asserted' bit. In order to continue with the device clear (and normal operation thereafter) the instrument must be restarted by sending any valid instruction code (e.g. "CF"). This serves only as a reset and will not be interpreted in the normal way.

E1 : Open collector drivers

The GPIB drivers fitted to 2022D have open collector, rather than tristate, outputs.

Setting the GPIB address

The instrument's talk/listen address is selected by means of second function 2. Acceptable addresses (00 to 30) can be set by this means and the instrument's internal address register will be updated by reading the address at power-on and on receipt of a device clear message. The current GPIB address is shown in the frequency display window when the interface is correctly installed.

GPIB programming codes

Functions	Miscellaneous functions
CF Carrier frequency	ST Store } followed by a
FM Frequency modulation	RC Recall } number 00-99
AM Amplitude modulation	IS Internal freq. standard
PM Phase modulation	XS External freq. standard
LV RF level	IM Internal modulation
DE Delta (Increment/Decrement)	XM External modulation
SF Second function (see note on page 3-11)	C0 Carrier off
RS Reset RPP	C1 Carrier on
QU Query - send current function setting to GPIB buffer	UP Increment up
	DN Increment down
	RT Return

Units				MOD OSC/ALC	
MZ	Megahertz	VL	Volts	L0	Mod ALC off
KZ	Kilohertz	MV	Millivolts	L1	Mod ALC on
HZ	Hertz	UV	Microvolt	M0	Mod off
PC	Percentage	DB	Decibel	M1	Mod on
RD	Radians			F1	400 Hz osc
				F3	1 kHz osc
				F4	3 kHz osc

Listening function

The 2022D is remotely controlled over the GPIB by strings of two-character codes and digits sent in upper case ASCII format. Where possible these codes correspond directly to the front panel keys; however, where the normal front panel control requires a knowledge of the previous state of the instrument (e.g. toggling controls such as on/off), special codes are provided to simplify programming.

In order to improve the readability of control strings, the codes may be separated by commas or spaces after each code pair or data group. These are ignored by the instrument. When data is entered, the syntax is the same over the GPIB as that used in control from the front panel. For example to enter a complex string of instructions such as a carrier frequency of 123.45 MHz with an increment of 25 kHz and an RF level of 1.2 μ V the string can be sent as follows:

"CF 123.45 MZ, DE CF 25 KZ, LV 1.2 UV".

Similarly, if it is required to change the RF level units setting to dBm (second function 14, level unit code 4), the following string should be sent:

"SF 14,4, ST".

Selection of a second function via the GPIB will result in a display of the SF number being shown in the instrument's RF LEVEL display.

The MOD ON/OFF, CARR ON/OFF and INT/EXT controls operate on the function currently active for data entry. This may be specified, e.g. "FM M1"; "AM XM" or implied, e.g. "FM 1.5 KZ, IM" but it is recommended that the function is specified within the string to ensure that the string will always have the same result.

Talking function

On receipt of the QU command the current function setting (e.g. CF,FM) is transferred to the GPIB output buffer in a format corresponding to the GPIB commands needed to set the instrument to the current state. RF level will be displayed in log. or linear units but without a specific reference since this information cannot be re-entered directly. Increment settings are also available if QU is sent whilst in DELTA mode with a current function LED lit. The following tables give the format for each type of string.

TABLE 3-1 MODULATION STRING (18 characters)

Number of characters in field							
2	2	4	2	2	2	2	2
DE **	FM PM AM	3 digits or leading spaces plus decimal point or space	MZ KZ HZ PC RD	M0 M1	IM XM	L0 L1 **	F1 F3 F4 **

* Represents a space which is used when the field has no relevance such as the levelling field when internal modulation is selected.

e.g. DE FM 1.00 KZ M1 IM ** F3

TABLE 3-2 FREQUENCY STRING (17 characters)

Number of characters in field				
2	2	9	2	2
DE **	CF	7 digits or leading spaces plus decimal point or space	MZ KZ	IS XS

e.g. ** CF 123.4567 MZ IS

TABLE 3-3 RF LEVEL STRING (14 characters)

Number of characters in field						
2	2	1	1	4	2	2
DE **	LV	- *	1 0 *	3 digits or leading spaces plus decimal point or space	DB VL MV UV	C0 C1

e.g. ** LV * 100.0 MV C1

The external modulation input level status indicated by the modulation window HI and LO is also accessed. The current status, if outside the specified limit, is transferred to the GPIB output by means of an error message:

Error No. 9 – input too low
Error No. 10 – input too high

Requesting a string to be output will overwrite any string data waiting to be sent. Addressing the instrument to talk without specifying a string to be sent or re-addressing to talk after a string has been completed will result in an error (and SRQ if not masked).

SF1, QU Status string

When accessed by SF1, QU the status of the instrument is sent to the controller, each data field being delimited by one space in the following format:-

XX	X	X	X	X	X	X
GPIB	OFFSETS	LEVEL	STORES	DISPLAY	PROTECTION	FREQ STD
ADDRESS	ON/OFF	UNITS	OFFSETS	BLANKING	LEVEL	1,5 or
		CODE	LOCKING			10 MHz

GPIB address:	00 to 30
Offsets:	'0' = off '1' = on
Level units code:	0 to 9 (see second function 14)
Stores/offsets locking:	'0' = stores and offsets unlocked '1' = stores locked, offsets unlocked '2' = stores unlocked, offsets locked '3' = stores and offsets locked (see second function 196 in Service Manual)
Display blanking of recalled stores:	'0' = off '1' = on (see second function 197 in Service Manual)
Protection level:	'0' = unprotected '1' = first level '2' = second level
Ext. frequency standard:	1, 5 or 10 MHz (see second function 10)

SF11, QU Identity string (read only)

The identity string accessed by SF11, QU allows instrument type number, software issue number and serial number to be read by the controller. The information is stored in non-volatile memory. The string is displayed as described in second function 11. Each data field is delimited by one space.

SF12, User string write facility

Up to 32 ASCII characters can be stored in non-volatile memory by the user. This bus only facility is useful for recording such information as the date the next calibration is due, test gear numbers etc. The string is terminated by the LINEFEED character <lf>, (ASCII code 10) which is included as the last character stored. If an attempt is made to store too many characters then <lf> is automatically inserted as the 32nd.

SF13, QU User string read facility

This facility provides a means of reading back data set by means of SF12 write facility and is again a bus only facility.

Service requests (SRQ)

The 2022D can request service to warn the controller of certain error conditions. In response to a serial poll after asserting the SRQ line, the 2022D will provide a status word (8 bits) in which bit 6 is set to indicate an SRQ request and the first five bits (0 to 4) indicate an error number. The error number is also displayed briefly in the carrier frequency window. Errors 06 and 08 will result in the instrument not functioning. Error 07 can be overridden with a restart command (any function code or digit).

Error numbers

No.	Error condition	Action taken
00	NO ERROR	
01	REQUEST OUTSIDE LIMITS	
02	INCORRECT KEY CODE SEQUENCE	
03	TOO MANY DIGITS	
04	INCORRECT UNIT	
05	RPP TRIP	Wait for reset instruction (RS)
06	RAM CHECK FAILURE (IC9)	
07	EAROM CHECKSUM FAILURE (IC10)	Wait for restart instruction (any function code or digit)
08	EPROM CHECKSUM FAILURE (IC5-IC8)	
09	EXTERNAL MODULATION OUTSIDE ALC RANGE (LOW)	
10	EXTERNAL MODULATION OUTSIDE ALC RANGE (HIGH)	
11	EXT STD SELECTED BUT NOT APPLIED	None

No.	Error condition	Action taken
12	EXT STD FREQ NOT LOCKING	None
13	LATCH WRITE ERROR	
14	EAROM WRITE ERROR	
15	EAROM RECALL ERROR	
16	GPIB BUS ERROR	
17	UNRECOGNIZED GPIB MNEMONIC/ CHARACTER	
18	ATTEMPT TO WRITE TO PROTECTED STORE	Ignore both characters: e.g. if the string "P,CF,M0" was received, the P,C would result in error 17 being displayed and the rest of the string would be inter- preted as "FM,0".

SRQ mask

The SRQ response to the errors listed above can be suppressed by setting a 3–page 6–bit mask, via second function 4. The bits of the mask refer directly to the errors, i.e. the left–most bit set indicates no response to error 1, the second from left no response to error 2, etc.

The mask is displayed by selection of second function 4, and may be changed by entering '1's and '0's via the keyboard. The STORE key is pressed to finalize a change. The SRQ mask is not stored in the non–volatile memory when power is removed. When the instrument is initially switched on the mask is set to all '0's.

Reverse power protection

When tripped by an overload applied to the RF OUTPUT socket, the GPIB SRQ line is asserted, and the status byte (obtainable by the controller conducting a serial poll) will contain the value 69 (decimal). The RPP can be reset via the bus by sending the RS command.

Note ...

If error 05 has been masked using second function 4 the service request action will not be initiated.

Clear, switch on, and return to local

SDC and DCL clear 2022D to the following state:–

Maximum carrier frequency (1000 MHz)

No AM, FM or Φ M

Minimum RF level (–127 dBm or equivalent)

Internal modulation at 1 kHz modulation frequency

Increment settings:

Carrier frequency: 1kHz

Modulation: 1 kHz FM, 0.1 rad Φ M or 1% AM

RF level: 1 dB

To revert from GPIB to front panel control, press the RET'N key.

If a local lock out command has been given the RET'N key operation will be ignored.

Notes ...

- (1) INT/EXT frequency standard selection, the GPIB address and instrument stores are unaffected by the SDC and DCL commands.
- (2) Switching on clears the 2022D to the same state as SDC or DCL unless 'Recall STORE 10 at switch on', conditions apply.

Chapter 4

BRIEF TECHNICAL DESCRIPTION

Frequency synthesizer and signal processing

2022D is a synthesized AM, FM or phase modulated signal generator covering a frequency range of 10 kHz to 1 GHz. Frequencies in the range 250 to 500 MHz are generated from two voltage controlled oscillators. In the range 62.5 to 250 MHz signal frequencies are obtained by divider circuits and in the range 10 kHz to 62.5 MHz by a beat frequency oscillator system. A frequency doubler is used to cover the band 500 to 1000 MHz.

The output frequency is phase locked to a frequency standard and frequencies up to 100 MHz can be set to a resolution of 10 Hz. Above 100 MHz the resolution is 100 Hz. A fractional division scheme allows this resolution to be obtained whilst still keeping the phase locked loop bandwidth reasonably high. Provision is also made for the use of an external frequency standard when this is preferred. Frequencies of 10, 5 or 1 MHz can be used depending on the position of an internal link.

Note...

A full technical description appears in the Service Manual H 52022-930X (Vol. 2) part number 46881-847B.

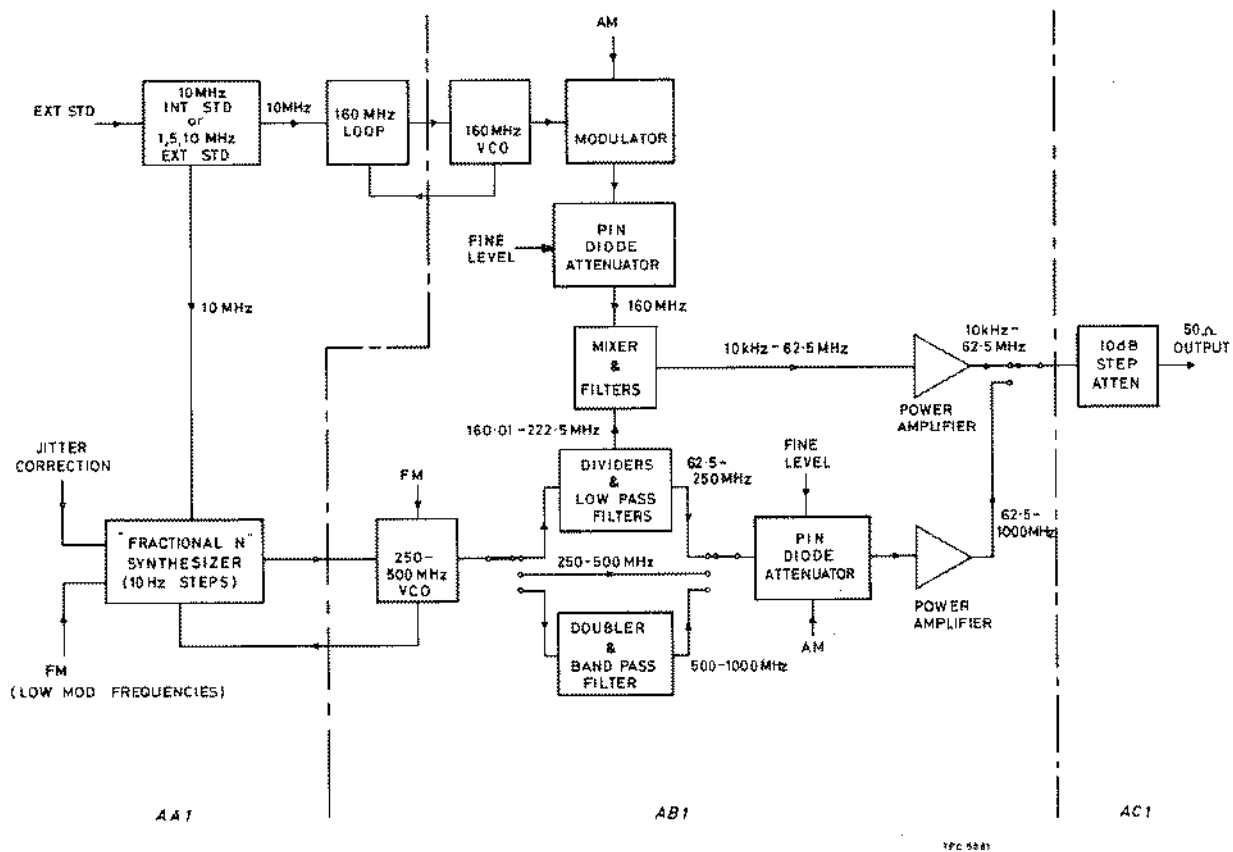


Fig. 4-1 Block schematic diagram

Output

Calibrated output levels from -127 dBm to $+13$ dBm are provided. A combination of ten output level calibration units can be selected on the front panel. The RF output level can be set to a resolution of 0.1 dB over the entire output voltage range with a total cumulative accuracy of ± 2 dB. A precision attenuator provides 120 dB in 10 dB steps and is a self contained module. Three 30 dB, one 20 dB and one 10 dB pad are used, each operated by TO5 relays. 16 dB of fine level control is provided by PIN diode attenuators.

Modulation

Amplitude, frequency and phase modulation can be provided internally from a switchable modulation source at a frequency of 400 Hz, 1 kHz or 3 kHz.

Amplitude modulation. For carrier frequencies greater than 62.5 MHz, modulation depths up to 80% are obtained using PIN diode attenuators and envelope feedback. At carrier frequencies less than 62.5 MHz a fixed frequency modulator operating at a frequency of 160 MHz allows up to 95% depth of modulation. AM is DC coupled.

Frequency modulation. FM is created by applying the modulation signal to varactor(s) in the 250 to 500 MHz oscillator. Simultaneous modulation of the reference frequency prevents fall off in response below the loop bandwidth. FM off (CW mode) gives the lowest residual FM noise. The low frequency response is tailored to optimize the modulation accuracy of low frequency square waves.

Phase modulation. This is obtained using a differentiator in the modulation signal path and then applying the treated signal in the same manner as for FM.

Modulation signal ALC. This is always in circuit when internal modulation is in use and may be selected when switched to external modulation. The circuit uses a JFET and allows up to 10% error in a 1 V input before a HI or LO message in the modulation display indicates that the applied modulation signal level is outside the range of the ALC.

Control

Front panel operation is carried out by direct entry of required settings via the keyboard. Microprocessor control ensures flexibility, simplicity of use and allows programming by the General Purpose Interface Bus (GPIB). This facility is offered as an optional accessory enabling the instrument to be used both as a manually operated bench mounted instrument or as part of a fully automated test system.

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SUPERO®



H8QGL-6F

H8QGL-iF

USER'S MANUAL

Revision 1.1a

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Preface

About This Manual

This manual is written for system integrators, PC technicians and knowledgeable PC users. It provides information for the installation and use of the H8QGL-6/iF serverboards. The H8QGL-6F serverboard includes onboard SAS2 support while the H8QGL-iF does not.

The H8QGL-6/iF serverboard is based on the AMD® Dual SR5690/SP5100 chipset and supports four AMD Socket G34 type processors with up to 512 GB of DDR3-1866/1600/1333/1066 Mhz speed SDRAM.

Please refer to the motherboard specifications pages on our web site for updates on supported processors (<http://www.supermicro.com/aplus/>). This product is intended to be professionally installed.

Manual Organization

Chapter 1 includes a checklist of what should be included in your motherboard box, describes the features, specifications and performance of the motherboard and provides detailed information about the chipset.

Chapter 2 begins with instructions on handling static-sensitive devices. Read this chapter when installing the processor(s) and memory modules and when installing the motherboard in a chassis. Also refer to this chapter to connect the hard disk drives, the various ports, and the power and reset buttons and the system LEDs.

If you encounter any problems, see **Chapter 3**, which describes troubleshooting procedures for the video, the memory and the setup configuration stored in CMOS. For quick reference, a general FAQ (Frequently Asked Questions) section is provided. Instructions are also included for contacting technical support. In addition, you can visit our web site for more detailed information.

Chapter 4 includes an introduction to BIOS and provides detailed information on running the CMOS Setup utility.

Appendix A provides BIOS Error Beep Code Messages.

Appendix B lists BIOS POST Checkpoint Codes.

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Chapter 1

Introduction

1-1 Overview

Checklist

Congratulations on purchasing your computer motherboard from an acknowledged leader in the industry. Supermicro boards are designed with the utmost attention to detail to provide you with the highest standards in quality and performance.

Please check that the following items have all been included with your motherboard. If anything listed here is damaged or missing, contact your retailer.

- One (1) H8QGL-6/iF serverboard
- One (1) I/O shield (MCP-260-00027-0N)
- One (1) 9-pin serial port cable (CBL-0010L)
- Eight (8) (H8QGL-6F) or six (6) (H8QGL-iF) 2ft. Amphenol, SATA cables (CBL-0044L)

Note: For your system to work properly, please follow the links below to download all necessary drivers/utilities and the user's manual for your motherboard.

- Supermicro product manuals: <http://www.supermicro.com/support/manuals/>
- Product drivers and utilities: <ftp://ftp.supermicro.com>
- Product safety information:
http://super-dev/about/policies/safety_information.cfm
- If you have any questions, please contact our support team at:
support@supermicro.com

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Web Site: www.supermicro.com.tw

Figure 1-1. H8QGL-6F Image



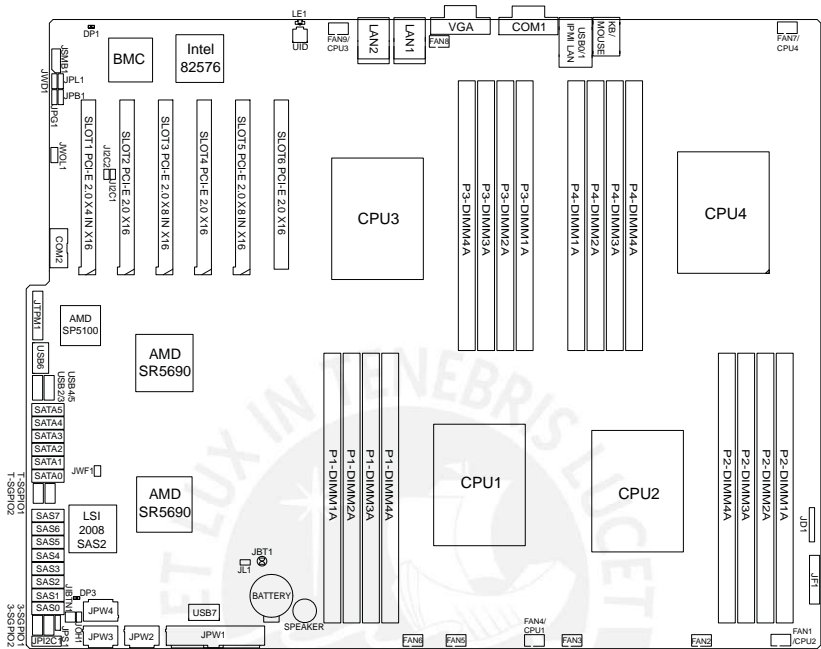
Note: Some components shown in the above image may be changed or unavailable in later revisions of this serverboard.

Figure 1-2. H8QGL-iF Image



Note: Some components shown in the above image may be changed or unavailable in later revisions of this serverboard.

Figure 1-3. H8QGL-6/iF Serverboard Layout
(not drawn to scale)



Note: Jumpers not indicated are for test purposes only. Not all ports, jumpers or LED Indicators are available on all serverboards.

H8QGL-6/iF Quick Reference		
Jumper	Description	Default Setting
JBT1	CMOS Clear	(See Section 2-7)
JI2C1/JI2C2	I2C to PCI-E Slot Enable/Disable	Both Open (Disabled)
JPB1	BMC Enable/Disable	Pins 1-2 (Enabled)
JPG1	VGA Enable/Disable	Pins 1-2 (Enabled)
JPL1	LAN 1/2 Enable/Disable	Pins 1-2 (Enabled)
JPS1	SAS Controller Enable/Disable (only on H8QGL-6F)	Pins 1-2 (Enabled)
JWD1	Watch Dog	Pins 1-2 (Reset)

LED	Description
LAN Ports	LEDs for the LAN Ethernet ports
Dedicated IPMI LAN	LEDs for the dedicated IPMI LAN Ethernet port
LE1	LED for UID Button
DP1	LED for IPMI Heartbeat
DP3	LED for Serverboard Power-On

Connector	Description
COM1/COM2	COM1 Serial Port/Header
FAN 1-9	Chassis/CPU Fan Headers
IPMI LAN	Dedicated IPMI LAN Port
JD1	Speaker Header
JF1	Front Panel Connector
JIBTN1	RAIDKey for RAID 5 SAS support (only on H8QGL-6F)
JL1	Chassis Intrusion Header
JOH1	Overheat Warning Header
JPI2C1	Power I2C Header
JPW1	24-pin Main ATX Power Connector
JPW2/3/4	+12V 8-pin CPU/Memory Power Connectors
JSMB1	System Management Bus Header (SMBus)
JTPM1	Trusted Platform Module Header
JWF1	Compact Flash Card Power Connector
JWOL1	Wake-On-LAN Header
LAN1/2	Gigabit Ethernet (RJ45) Ports
KB/Keyboard	PS2 Mouse/Keyboard connectors
SAS0~3, SAS4~7	SAS Ports (only on H8QGL-6F)
SATA0 ~ SATA5	SATA Ports
3-SGPIO1/3-SGPIO2	Serial General Purpose I/O Header for SAS (only on H8QGL-6F)
T-SGPIO1/T-SGPIO2	Serial General Purpose Input/Output Header for SATA
UID	Unit Identifier Button
USB0/1, USB6, USB2/3, USB4/5	Universal Serial Bus (USB) Ports, Type-A Port and Headers
VGA	VGA Connector

Serverboard Features

CPU

- Quad AMD Opteron 6000 series (AMD Socket G34 type) processors

Note: You must install at least two processors for full functions to be supported.

Memory

- Sixteen (16) single/dual/tri/quad channel DIMM slots supporting up to 512 GB of registered ECC RDIMM/LRDIMM or 128 GB of Unbuffered ECC/non-ECC UDIMM DDR3-1866/1600/1333/1066 Mhz speed, 1 GB, 2 GB, 4 GB, 8 GB, 16 GB or 32 GB size SDRAM at 1.35V or 1.5 voltages

Note: Refer to Section 2-5 before installing memory and our web site for recommended DIMMs.

Note: Refer the tested memory list on the motherboard website.

Chipset

- Dual AMD SR5690 plus one SP5100 Southbridge chipset

Expansion Slots

- Three (3) PCI-Express x16 Gen. 2
- Two (2) PCI-Express x8 (in x16) Gen. 2
- One (1) PCI-Express x4 (in x16) Gen. 2

BIOS

- 16 Mb AMI BIOS® SPI Flash ROM
- APM 1.2, DMI 2.3, PCI 2.2, ACPI 1.0 (ACPI 2.0 is BIOS supported), SMBIOS 2.3, Real Time Clock Wakeup, Plug and Play (PnP), BIOS resume hot keys,

PC Health Monitoring

- Onboard voltage monitors
- Fan status monitor with firmware/software on/off and speed control
- Watch Dog
- Environmental temperature monitoring via BIOS
- Power-up mode control for recovery from AC power loss
- System resource alert (via included utility program)
- Auto-switching voltage regulator for the CPU core
- CPU thermal trip support
- I²C temperature sensing logic

ACPI Features

- Microsoft OnNow
- Slow blinking LED for suspend state indicator
- BIOS support for USB keyboard
- Wake-On-LAN (WOL)
- Internal/external modem ring-on
- Hardware BIOS Virus protection

Onboard I/O

- Six (6) SATA ports supported by an on-chip SATA controller (RAID 0, 1 and 10 supported)
- Eight (8) SAS ports supported by an LSI 2008 SAS2 controller (RAID 0, 1 and 10 supported; RAID 5 supported is optional with the AOC-SAS2-RAID5-KEY add-on card installed (H8QGL-6F only).
- Two (2) Fast UART 16550 compatible serial port (one header and one port)
- Seven (7) USB (Universal Serial Bus 2.0) ports (2x rear, 4x header, 1x type A)
- Two (2) LAN ports supported by an onboard Intel® 82576 dual port Ethernet controller for 10/100/1000Base-T
- One (1) dedicated IPMI LAN port
- One (1) VGA port supported by an onboard Matrox® G200eW graphics controller (with 16 MB DDR2 memory)

Other

- Onboard power LED
- Chassis intrusion detection

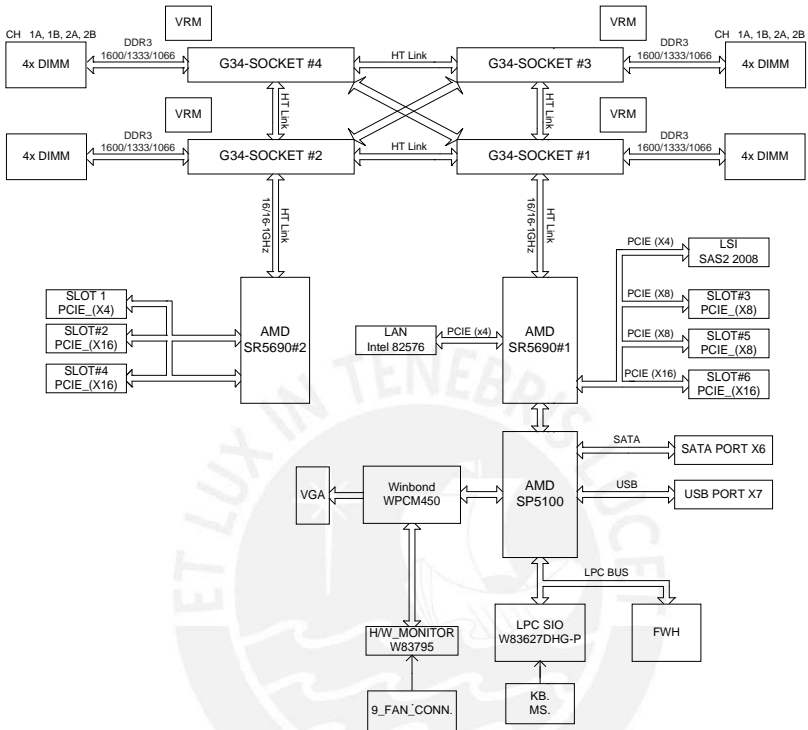
CD Utilities

- BIOS flash upgrade utility
- Super Doctor III
- IPMI 1.5 / 2.0 (Optional)

Dimensions

- Proprietary format: (LxW) 16.48" x 13" (418 x 330 mm)

**Figure 1-4. AMD Dual SR5690/SP5100 Chipset:
System Block Diagram**



Note: This is a general block diagram and may not exactly represent the features on your motherboard. See the previous pages for the actual specifications of your motherboard.

1-3 Chipset Overview

The H8QGL-6/IF serverboard is based on the AMD Dual SR5690/SP5100 chipset. This chipset functions as a Media and Communications Processor (MCP). Controllers for the system memory are integrated directly into AMD Opteron processors.

AMD SR5690/SP5100 Chipsets

The AMD Dual SR5690/SP5100 are each a single-chip, high-performance HyperTransport peripheral controller. It includes a 42-lane PCI Express interface, an AMD Opteron 16-bit Hyper Transport interface link, a six-port Serial ATA interface and a seven-port USB 2.0 interface. This hub connects directly to the CPU.

HyperTransport Technology

HyperTransport technology is a high-speed, low latency point to point link that was designed to increase the communication speed by a factor of up to 48x between integrated circuits. This is done partly by reducing the number of buses in the chipset to reduce bottlenecks and by enabling a more efficient use of memory in multi-processor systems. The end result is a significant increase in bandwidth within the chipset.

1-4 PC Health Monitoring

This section describes the PC health monitoring features of the H8QGL-6/IF serverboard. The serverboard has an onboard System Hardware Monitor chip that supports PC health monitoring.

Onboard Voltage Monitors

The onboard voltage monitor will continuously scan crucial voltage levels. Once a voltage becomes unstable, it will give a warning or send an error message to the screen. Users can adjust the voltage thresholds to define the sensitivity of the voltage monitor. Real time readings of these voltage levels are all displayed in BIOS.

Fan Status Monitor with Firmware/Software Speed Control

The PC health monitor can check the RPM status of the cooling fans. The onboard fans are controlled by thermal management via BIOS.

CPU Overheat/Fan Fail LED and Control

This feature is available when the user enables the CPU overheat/Fan Fail warning function in the BIOS. This allows the user to define an overheat temperature. When this temperature is exceeded or when a fan failure occurs, the Overheat/Fan Fail warning LED is triggered.

Auto-Switching Voltage Regulator for the CPU Core

The 6-phase-switching voltage regulator for the CPU core can support up to AMD Opteron 6000SE series processors. This will allow the regulator to run cooler and thus make the system more stable.

1-5 Power Configuration Settings

This section describes the features of your motherboard that deal with power and power settings.

Microsoft OnNow

The OnNow design initiative is a comprehensive, system-wide approach to system and device power control. OnNow is a term for a PC that is always on but appears to be off and responds immediately to user or other requests.

Slow Blinking LED for Suspend-State Indicator

When the CPU goes into a suspend state, the chassis power LED will start blinking to indicate that the CPU is in suspend mode. When the user presses any key, the CPU will wake-up and the LED will automatically stop blinking and remain on.

BIOS Support for USB Keyboard

If a USB keyboard is the only keyboard in the system, it will function like a normal keyboard during system boot-up.

Main Switch Override Mechanism

The power button can function as a system suspend button. When the user depresses the power button, the system will enter a SoftOff state. The monitor will be suspended and the hard drive will spin down. Depressing the power button again will cause the whole system to wake-up. During the SoftOff state, the power supply provides power to keep the required circuitry in the system alive. In case the system malfunctions and you want to turn off the power, just depress and hold the power button for 4 seconds. The power will turn off and no power will be provided to the motherboard.

Wake-On-LAN (WOL)

Wake-On-LAN is defined as the ability of a management application to remotely power up a computer that is powered off. Remote PC setup, up-dates and access tracking can occur after hours and on weekends so that daily LAN traffic is kept to a minimum and users are not interrupted. The motherboard has a 3-pin header (WOL) to connect to the 3-pin header on a Network Interface Card (NIC) that has WOL capability. Wake-On-LAN must be enabled in BIOS.

1-6 Power Supply

As with all computer products, a stable power source is necessary for proper and reliable operation. It is even more important for processors that have high CPU clock rates.

The H8QGL-6/iF serverboard requires the use of proprietary power supplies. Please refer to the pinout information for the power connectors in Section 6 of Chapter 2 for detailed information on power requirements.

In areas where noisy power transmission is present, you may choose to install a line filter to shield the computer from noise. It is recommended that you also install a power surge protector to help avoid problems caused by power surges.

Warning: To prevent the possibility of explosion, do not use the wrong type of onboard CMOS battery or install it upside down.

1-7 Super I/O

The Super I/O includes a data separator, write pre-compensation circuitry, decode logic, data rate selection, a clock generator, drive interface control logic and interrupt and DMA logic. The wide range of functions integrated onto the Super I/O greatly reduces the number of components required for interfacing with floppy disk drives.

The Super I/O provides two high-speed, 16550 compatible serial communication ports (UARTs), one of which supports serial infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability and a processor interrupt system. Both UARTs provide legacy speed with baud rate of up to 115.2 Kbps as well as an advanced speed with baud rates of 250 K, 500 K, or 1 Mb/s, which support higher speed modems.

The Super I/O provides functions that comply with ACPI (Advanced Configuration and Power Interface), which includes support of legacy and ACPI power management through a SMI or SCI function pin. It also features auto power management to reduce power consumption.

The IRQs, DMAs and I/O space resources of the Super I/O can be flexibly adjusted to meet ISA PnP requirements, which support ACPI and APM (Advanced Power Management).



Chapter 2

Installation

2-1 Standardized Warning Statements

About Standardized Warning Statements

The following statements are industry standard warnings, provided to warn the user of situations which have the potential for bodily injury. Should you have questions or experience difficulty, contact Supermicro's Technical Support department for assistance. Only certified technicians should attempt to install or configure components.

Read this section in its entirety before installing or configuring components in the Supermicro chassis.

These warnings may also be found on our web site at http://www.supermicro.com/about/policies/safety_information.cfm.

Battery Handling



Warning!

There is a danger of explosion if the battery is replaced incorrectly. Replace the battery only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions

電池の取り扱い

電池交換が正しく行われなかった場合、破裂の危険性があります。交換する電池はメーカーが推奨する型、または同等のものを使用下さい。使用済電池は製造元の指示に従って処分して下さい。

警告

電池更換不當會有爆炸危險。請只使用同類電池或製造商推薦的功能相當的電池更換原有電池。請按製造商的說明處理廢舊電池。

警告

電池更換不當會有爆炸危險。請使用製造商建議之相同或功能相當的電池更換原有電池。請按照製造商的說明指示處理廢棄舊電池。

Warnung

Bei Einsetzen einer falschen Batterie besteht Explosionsgefahr. Ersetzen Sie die Batterie nur durch den gleichen oder vom Hersteller empfohlenen Batterietyp. Entsorgen Sie die benutzten Batterien nach den Anweisungen des Herstellers.

Attention

Danger d'explosion si la pile n'est pas remplacée correctement. Ne la remplacer que par une pile de type semblable ou équivalent, recommandée par le fabricant. Jeter les piles usagées conformément aux instructions du fabricant.

¡Advertencia!

Existe peligro de explosión si la batería se reemplaza de manera incorrecta. Reemplazar la batería exclusivamente con el mismo tipo o el equivalente recomendado por el fabricante. Desechar las baterías gastadas según las instrucciones del fabricante.

אזהרה!

קיימת סכנת פיצוץ של הסוללה במידה והוחלפה בדרך לא תקינה. יש להחליף את הסוללה בסוג התואם מחברת יצרן מומלצת.

סילוק הסוללות המשומשות יש לבצע לפי הוראות היצרן.

هناك خطر من انفجار في حالة استبدال البطارية بطريقة غير صحيحة فعليك استبدال البطارية

فقط بنفس النوع أو ما يعادلها كما أوصت به الشركة المصنعة
تخلص من البطاريات المستعملة وفقا لتعليمات الشركة الصانعة

경고!

배터리가 올바르게 교체되지 않으면 폭발의 위험이 있습니다. 기존 배터리와 동일하거나 제조사에서 권장하는 동등한 종류의 배터리로만 교체해야 합니다. 제조사의 안내에 따라 사용된 배터리를 처리하여 주십시오.

Waarschuwing

Er is ontploffingsgevaar indien de batterij verkeerd vervangen wordt. Vervang de batterij slechts met hetzelfde of een equivalent type die door de fabrikant aanbevolen wordt. Gebruikte batterijen dienen overeenkomstig fabrieksvoorschriften afgevoerd te worden.

Product Disposal



Warning!

Ultimate disposal of this product should be handled according to all national laws and regulations.

製品の廃棄

この製品を廃棄処分する場合、国の関係する全ての法律・条例に従い処理する必要があります。

警告

本产品的废弃处理应根据所有国家的法律和规章进行。

警告

本產品的廢棄處理應根據所有國家的法律和規章進行。

Warnung

Die Entsorgung dieses Produkts sollte gemäß allen Bestimmungen und Gesetzen des Landes erfolgen.

¡Advertencia!

Al deshacerse por completo de este producto debe seguir todas las leyes y reglamentos nacionales.

Attention

La mise au rebut ou le recyclage de ce produit sont généralement soumis à des lois et/ou directives de respect de l'environnement. Renseignez-vous auprès de l'organisme compétent.

סילוק המוצר

אזהרה!

סילוק סופי של מוצר זה חייב להיות בהתאם להנחיות וחוקי המדינה.

عند التخلص النهائي من هذا المنتج ينبغي التعامل معه وفقا لجميع القوانين واللوائح الوطنية

경고!

이 제품은 해당 국가의 관련 법규 및 규정에 따라 폐기되어야 합니다.

Waarschuwing

De uiteindelijke verwijdering van dit product dient te geschieden in overeenstemming met alle nationale wetten en reglementen.

2-2 Static-Sensitive Devices

Electrostatic Discharge (ESD) can damage electronic components. To prevent damage to your system board, it is important to handle it very carefully. The following measures are generally sufficient to protect your equipment from ESD.

Precautions

- Use a grounded wrist strap designed to prevent static discharge.
- Touch a grounded metal object before removing the board from the antistatic bag.
- Handle the board by its edges only; do not touch its components, peripheral chips, memory modules or gold contacts.
- When handling chips or modules, avoid touching their pins.
- Put the motherboard and peripherals back into their antistatic bags when not in use.
- For grounding purposes, make sure your computer chassis provides excellent conductivity between the power supply, the case, the mounting fasteners and the motherboard.
- Use only the correct type of CMOS onboard battery as specified by the manufacturer. Do not install the CMOS onboard battery upside down, which may result in a possible explosion.

Unpacking

The motherboard is shipped in antistatic packaging to avoid static damage. When unpacking the board, make sure the person handling it is static protected.

2-3 Processor and Heatsink Installation

Caution: Exercise extreme caution when handling and installing the processor. Always connect the power cord last and always remove it before adding, removing or changing any hardware components.

Installation Procedure

Follow the procedures as listed below to install the motherboard into a chassis.

1. Install the processor(s) and the heatsink(s).
2. Install the motherboard in the chassis.
3. Install the memory and add-on cards.
4. Finally, connect the cables and install the drivers.

Installing the Processors

1. Begin by removing the cover plate that protects the CPU. Lift the lever on the CPU socket until it points straight up.
2. With the lever raised, lift open the silver CPU retention plate.



3. Use your thumb and your index finger to hold the CPU. Locate and align pin 1 of the CPU socket with pin 1 of the CPU. Both are marked with a triangle.
4. Align pin 1 of the CPU with pin 1 of the socket. Once aligned, carefully place the CPU into the socket. *Do not drop the CPU on the socket, move the CPU horizontally or vertically or rub the CPU against the socket or against any pins of the socket, which may damage the CPU and/or the socket.*



Triangle

5. With the CPU inserted into the socket, inspect the four corners of the CPU to make sure that it is properly installed and flush with the socket. Then, gently lower the silver CPU retention plate into place.



6. Carefully press the CPU socket lever down until it locks into its retention tab. For a dual-CPU system, repeat these steps to install another CPU into the CPU#2, #3 and #4 sockets for a quad-CPU configuration).



Note: In single and dual-CPU configurations, memory must be installed in the DIMM slots associated with the installed CPU(s). Memory is limited to a maximum of 128 for single CPU and 256 GB for dual CPU configurations.

Installing the Heatsinks

We recommend the use of active type heatsinks (except for 1U systems). Use any onboard fan header for the CPU's heatsink fan. To install the heatsink, please follow the installation instructions that are included with your heatsink package.

Note: Make sure the heatsink is placed so that the fins of the heatsink are in the direction of the airflow in your system.

2-4 Mounting the Serverboard into a Chassis

All motherboards have standard mounting holes to fit different types of chassis. Make sure that the locations of all the mounting holes for both the motherboard and the chassis match. Although a chassis may have both plastic and metal mounting fasteners, metal ones are highly recommended because they ground the motherboard to the chassis. Make sure that the metal standoffs click in or are screwed in tightly.

Check the Compatibility of the Serverboard Ports and the I/O Shield

7. The H8QGL-6/iF serverboard requires a chassis that can support a board of (LxW) 16.48" x 13" (418 x 330 mm) in size.
8. Make sure that the I/O ports on the motherboard align with their respective holes in the I/O shield at the rear of the chassis.

Mounting the Serverboard onto the Tray in the Chassis

1. Carefully mount the motherboard onto the motherboard tray by aligning the motherboard mounting holes with the raised metal standoffs in the tray.
2. Insert screws into all the mounting holes in the motherboard that line up with the standoffs.
3. Then use a screwdriver to secure the motherboard to the mainboard tray - tighten until just snug (if too tight you might strip the threads). Metal screws provide an electrical contact to the motherboard ground to provide a continuous ground for the system.

2-5 Installing Memory

Installing Memory

Caution: Exercise extreme caution when installing or removing memory modules to prevent any possible damage.

1. Insert each memory module vertically into its slot, paying attention to the notch along the bottom of the module to prevent inserting the module incorrectly (see Figure 2-1).

2. Install to slots CPU1/DIMM1A, CPU1/DIMM2A, CPU1/DIMM3A and CPU1/DIMM4A, etc. Always install in groups of four and in the numerical order of the DIMM slots. See support information below.
3. Gently press down on the memory module until it snaps into place.
4. With four DIMMs installed, repeat step 2 to populate the CPU2 DIMM slots. Always install four DIMMs to both CPU DIMM slots for more efficient operation.

Note: 1 GB, 2 GB, 4 GB, 8 GB, 16 GB or 32 GB size memory modules are supported. It is highly recommended that you remove the power cord from the system before installing or changing memory modules. Please refer to our web site for memory that has been tested on the H8QGL-6/iF serverboard.

Memory Support

The H8QGL-6/iF serverboard supports single/dual/tri/quad-channel, DDR3-1866/1600/1333/1066 Mhz speed registered ECC or Unbuffered ECC/non-ECC SDRAM.

Populating four adjacent slots at a time with memory modules of the same size and type will result in interleaved (128-bit) memory, which is faster than non-interleaved (64-bit) memory.

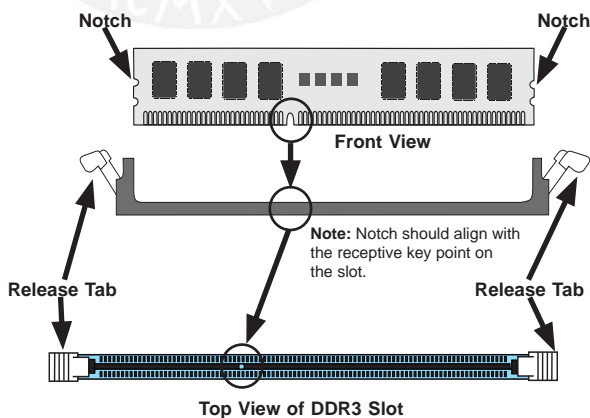
Maximum Memory

The H8QGL-6/iF serverboard supports up to 512 GB of registered ECC RDIMM/LRDIMM or 128 GB of Unbuffered ECC/non-ECC UDIMM SDRAM in 16 slots.

Figure 5-3. Installing DIMM into Slot

To Install: Insert module vertically and press down until it snaps into place. Pay attention to the alignment notch at the bottom.

To Remove: Use your thumbs to gently push the release tabs near both ends of the module. This should release it from the slot.



Memory Population for Optimal Performance -For a Serverboard with One CPU (CPU1) Installed					
# DIMMS	CPU	Channel 1	Channel 2	Channel 3	Channel 4
4 DIMMs	CPU1	P1-1A	P1-2A	P1-3A	P1-4A

Memory Population for Optimal Performance -For a Serverboard with Two CPUs (CPU1 & CPU2) Installed					
# DIMMS	CPU	Channel 1	Channel 2	Channel 3	Channel 4
8 DIMMs	CPU1	P1-1A	P1-2A	P1-3A	P1-4A
	CPU2	P2-1A	P2-2A	P2-3A	P2-4A

Memory Population for Optimal Performance – For a Serverboard with Four CPUs (CPU1, CPU2, CPU3 & CPU4) Installed					
# DIMMS	CPU	Channel 1	Channel 2	Channel 3	Channel 4
16 DIMMs	CPU1	P1-1A	P1-2A	P1-3A	P1-4A
	CPU2	P2-1A	P2-2A	P2-3A	P2-4A
	CPU3	P3-1A	P3-2A	P3-3A	P3-4A
	CPU4	P4-1A	P4-2A	P4-3A	P4-4A

DIMM Module Population Configuration

For memory to work properly, follow the tables below for memory installation:

Per Channel DIMM Populations Options				
DIMM Type	DIMM A	Max. MHz, 1.5V DIMMs	Max. MHz, 1.35V DIMMs	Max. GB/ Channel
UDIMM	SR or DR	1866 MHz	1600 MHz	8 GB
RDIMM	SR or DR	1866 MHz	1600 MHz	16 GB
	QR	1333 MHz	1333 MHz	32 GB
LRDIMM	QR		1333 MHz	32 GB

Note 1: Due to OS limitations, some operating systems may not show more than 4 GB of memory.

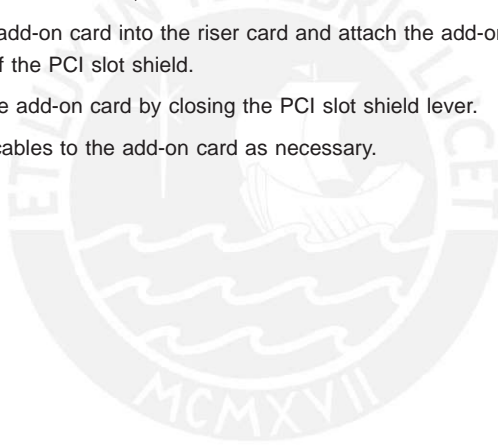
Note 2: Due to memory allocation to system devices, the amount of memory that remains available for operational use will be reduced when 4 GB of RAM is used. The reduction in memory availability is disproportional.

2-6 PCI Expansion Cards

A riser card is used to support one standard size (full height full length) PCI expansion card.

Installing a PCI Expansion Card

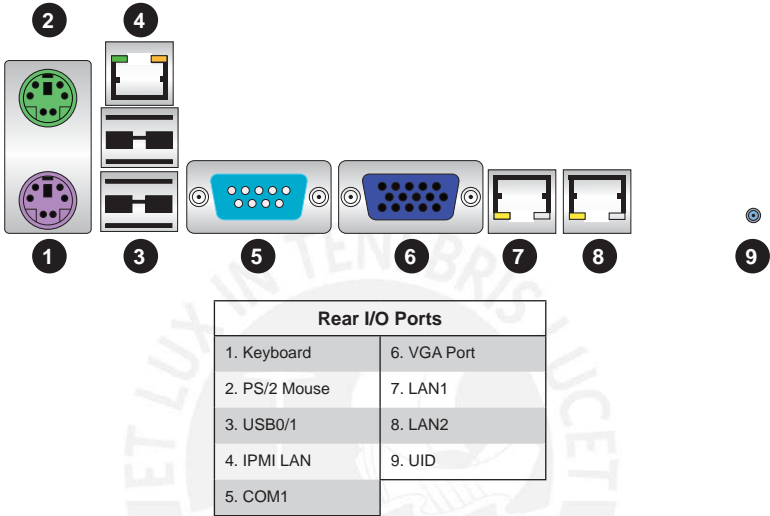
1. Confirm that you have the correct riser card for your chassis model and the add-on card includes a standard bracket.
2. Remove the chassis cover.
3. Install the riser card by sliding card into the appropriate slot in the motherboard.
4. Choose the PCI slot shield in which to place the add-on card.
5. In that slot, open the PCI slot shield lever and slide the shield sideways.
6. From inside the chassis, remove the PCI slot shield.
7. Slide the add-on card into the riser card and attach the add-on card bracket in place of the PCI slot shield.
8. Secure the add-on card by closing the PCI slot shield lever.
9. Connect cables to the add-on card as necessary.



2-7 I/O Port and Control Panel Connections

The I/O ports are color coded to make setting up your system easier. See Figure 2-2 below for the colors and locations of the various I/O ports.

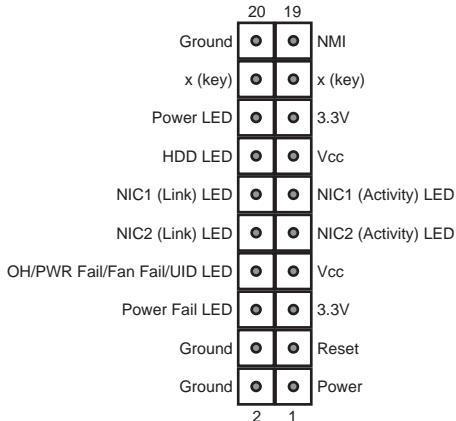
Figure 2-2. I/O Port Locations and Definitions



Front Control Panel

JF1 contains header pins for various front control panel connectors. See Figure 2-3 for the pin definitions of the various connectors. Refer to Section 2-8 for details.

Figure 2-3. JF1: Front Control Panel Header (JF1)



2-8 Connector Definitions

Power Connectors

A 24-pin main power supply connector(JPW1) and three 8-pin CPU/Memory PWR connectors (JPW2/JPW3/JPW4) on the motherboard. These power connectors meet the SSI EPS 12V specification. In addition to the 24-pin ATX power connector, the 12V 8-pin CPU/Memory PWR connectors at JPW2/JPW3/JPW4 must also be connected to your power supply. See the table on the right for pin definitions.

Warning: To prevent damage to the power supply or motherboard, please use a power supply that contains a 24-pin and three 8-pin power connectors. Be sure to connect these connectors to the 24-pin (JPW1) and the three 8-pin (JPW2,JPW3 and JPW4) power connectors on the motherboard. Failure in doing so will void the manufacturer warranty on your power supply and motherboard.

Power Connector

The Power Connector is located on pins 1 and 2 of JF1. Momentarily contacting both pins will power on/off the system. This button can also be configured to function as a suspend button (with a setting in the BIOS - see Chapter 4). To turn off the power when set to suspend mode, press the button for at least 4 seconds. Refer to the table on the right for pin definitions.

ATX Power 24-pin Connector Pin Definitions (JPW1)			
Pin#	Definition	Pin#	Definition
13	+3.3V	1	+3.3V
14	-12V	2	+3.3V
15	COM	3	COM
16	PS_ON	4	+5V
17	COM	5	COM
18	COM	6	+5V
19	COM	7	COM
20	Res (NC)	8	PWR_OK
21	+5V	9	5VSB
22	+5V	10	+12V
23	+5V	11	+12V
24	COM	12	+3.3V

12V 8-pin PWR Connector Pin Definitions (JPW2/3/4)	
Pins	Definition
1 through 4	Ground
5 through 8	+12V

Required Connection

Power Button Pin Definitions (JF1)	
Pin#	Definition
1	Power
2	Ground

Reset Connector

The reset connector is located on pins 3 and 4 of JF1 and attaches to the reset switch on the computer chassis. See the table on the right for pin definitions.

Reset Button Pin Definitions (JF1)	
Pin#	Definition
3	Reset
4	Ground

Power Fail LED

The Power Fail LED connection is located on pins 5 and 6 of JF1. Refer to the table on the right for pin definitions.

PWR Fail LED Pin Definitions (JF1)	
Pin#	Definition
5	3.3V
6	Power Fail LED

Overheat (OH)/Fan Fail/PWR Fail/ UID LED

Connect an LED cable to pins 7 and 8 of JF1 to use the Overheat/Fan Fail/Power Fail and UID LED connections. The Red LED on pin 8 provides warnings of an overheat, fan failure or power failure. The Blue LED on pin 8 works as the UID LED indicator for the front panel UID switch. Refer to the table on the right for pin definitions.

OH/Fan Fail/ PWR Fail (Red) LED and UID (Blue) LED Pin Definitions (JF1)	
Pin#	Definition
7	Vcc
8	OH/Fan Fail/PWS Fail (Red) LED and UID (Blue) LED

OH/Fan Fail/PWR Fail LED Status (Red LED)	
State	Indication
Off	Normal
On	Overheat
Flashing	Fan Fail

NIC2 (Link/Activity) LED

The LED connections for LAN2 link/activity are on pins 9 and 10 of JF1. Attach LAN LED cables to display network activity. See the table on the right for pin definitions.

NIC2 LED Pin Definitions (JF1)	
Pin#	Definition
9	Activity
10	Link

NIC1 (Link/Activity) LED

The LED connections for LAN1 link/activity are on pins 11 and 12 of JF1. Attach LAN LED cables to display network activity. See the table on the right for pin definitions.

NIC1 LED Pin Definitions (JF1)	
Pin#	Definition
11	Activity
12	Link

HDD LED

The HDD LED connections are located on pins 13 and 14 of JF1. Attach a hard-drive LED cable to display HDD or SATA activities. Refer to the table on the right for pin definitions.

HDD LED Pin Definitions (JF1)	
Pin#	Definition
13	Vcc
14	HDD LED

Power LED Connector

The Power LED connector is on pins 15 and 16 of JF1. See the table on the right for pin definitions.

Power LED Pin Definitions (JF1)	
Pin#	Definition
15	3.3V
16	Power LED

NMI Button

The non-maskable interrupt button header is located on pins 19 and 20 of JF1. Refer to the table on the right for pin definitions.

NMI Button Pin Definitions (JF1)	
Pin#	Definition
19	NMI
20	Ground

Universal Serial Bus Ports

Two Universal Serial Bus ports (USB 2.0) are located beside the Keyboard and Mouse PS2 ports (USB0/1). One additional Type A port (USB6) is included on the motherboard. See the table on the right for pin definitions.

Universal Serial Bus Ports Pin Definitions (USB 0/1, USB6)			
USB0/1		USB6	
Pin#	Definition	Pin#	Definition
1	+5V	1	+5V
2	PO-	2	PO-
3	PO+	3	PO+
4	Ground	4	Ground

USB Headers

Four USB 2.0 headers (USB2/3 and USB4/5) are also included on the motherboard. These may be connected to provide front side access. A USB cable (not included) is needed for the connection. See the table on the right for pin definitions.

Universal Serial Bus Headers Pin Definitions (USB2/3, USB4/5)			
JUSB2, JUSB3			
Pin#	Definition	Pin#	Definition
1	+5V	2	+5V
3	PO-	4	PO-
5	PO+	6	PO+
7	Ground	8	Ground
9	Key	10	NC

Note: NC indicates no connection.

LAN1/2 (Ethernet Ports)

Two Gigabit Ethernet ports (designated LAN1 and LAN2) are located beside the VGA port. Additionally, there is a dedicated LAN for IPMI on top of the two rear USB ports. These Ethernet ports accept RJ45 type cables.



LAN Ports (LAN1/2) Pin Definition			
Pin#	Definition	Pin#	Definition
1	P2V5SB	10	SGND
2	TD0+	11	Act LED
3	TD0-	12	P3V3SB
4	TD1+	13	Link 100 LED (Yellow, +3V3SB)
5	TD1-	14	Link 1000 LED (Yellow, +3V3SB)
6	TD2+	15	Ground
7	TD2-	16	Ground
8	TD3+	17	Ground
9	TD3-	18	Ground

Note: NC indicates no connection.

SMBus Header

The header at SMBus is for the System Management Bus. Connect the appropriate cable here to utilize SMB on the system. See the table on the right for pin definitions.

SMBus Header (SMBus) Pin Definitions (JSMB1)	
Pin#	Definition
1	Data
2	Ground
3	Clock
4	No Connection

SGPIO

The T-SGPIO1/ T-SGPIO2 (Serial General Purpose Input/Output) headers provide a bus between the SATA controller and the backplane to provide SATA enclosure management functions. Connect the appropriate cable from the backplane to the T-SGPIO1 header to utilize SATA management functions on your system.

Likewise, the 3-SGPIO1/3-SGPIO2 headers provide the same function between the SAS controller and the backplane, and have the same pin definitions (only on H8QGL-6F)

SGPIO Header Pin Definitions (T-SGPIO1/T-SGPIO2) (3-SGPIO1/3-SGPIO2)			
Pin#	Definition	Pin#	Definition
1	NC	2	Data
3	Ground	4	Data
5	Load	6	Ground
7	CLK	8	NC

Note: NC indicates no connection.

Serial Ports

The COM1 serial port is located beside the VGA port. Refer to the motherboard layout for the location of the COM2 header. See the table on the right for pin definitions.

Serial Port Pin Definitions (COM1/COM2)			
Pin#	Definition	Pin#	Definition
1	DCD	6	DSR
2	RXD	7	RTS
3	TXD	8	CTS
4	DTR	9	RI
5	Ground	10	NC

Note: NC indicates no connection.

Wake-On-LAN

The Wake-On-LAN header is designated JWOL1. See the table on the right for pin definitions. You must have a LAN card with a Wake-On-LAN connector and cable to use the Wake-On-LAN feature.

Wake-On-LAN Pin Definitions (JWOL)	
Pin#	Definition
1	+5V Standby
2	Ground
3	Wake-up

Power SMB (I²C)

The Power System Management Bus (I²C) connector (JPI2C1) monitors the power supply, fan and system temperatures. See the table on the right for pin definitions.

Power SMB I ² C Pin Definitions (JPI2C1)	
Pin#	Definition
1	Clock
2	Data
3	PWR Fail
4	Ground
5	+3.3V

Video Connector

A Video (VGA) connector is located below the COM Port on the IO backplane. This connector is used to provide video and CRT display.

Power LED/Speaker

On the JD1 header, pins 1~3 are used for power LED indication, and pins 4-7 are for the speaker. See the tables on the right for pin definitions. If you wish to use the onboard speaker, you should close pins 6~7 with a jumper. Connect a cable to pins 4~7 of JD1 to use an external speaker.

PWR LED Connector Pin Definitions (JD1)	
Pin Setting	Definition
Pin1	Anode (+)
Pin2	Cathode (-)
Pin3	NA

Speaker Connector Pin Definitions	
Pin Setting	Definition
Pins 4~7	External Speaker
Pins 6~7	Internal Speaker

Overheat LED

Connect an LED to the JOH1 header to provide warning of chassis overheating. See the table on the right for pin definitions.

Overheat LED Pin Definitions (JOH1)	
Pin#	Definition
1	3.3V
2	OH Active

ATX PS/2 Keyboard and PS/2 Mouse Ports

The ATX PS/2 keyboard and PS/2 mouse are located next to the Back Panel USB Ports 0/1 on the motherboard. See the table at right for pin definitions.

PS/2 Keyboard/Mouse Pin Definitions			
PS2 Keyboard		PS2 Mouse	
Pin#	Definition	Pin#	Definition
1	KB Data	1	Mouse Data
2	No Connection	2	No Connection
3	Ground	3	Ground
4	Mouse/KB VCC (+5V)	4	Mouse/KB VCC (+5V)
5	KB Clock	5	Mouse Clock
6	No Connection	6	No Connection

VCC: with 1.5A PTC (current limit)

JIBTN1 Header

A RAIDKey header, located at JIBTN1, provides RAID function support in order to use RAID 5 SAS support. This header is only available on the H8QGL-6F serverboard.

Chassis Intrusion

A Chassis Intrusion header is located at JL1. Attach the appropriate cable to inform you of a chassis intrusion.

Chassis Intrusion Pin Definitions (JL1)	
Pin#	Definition
1	Battery voltage
2	Intrusion signal

Unit Identifier Button

There is a Unit Identifier (UID) button on the rear I/O of the board. There is also another UID button located on the control panel. When you push either UID button, both Rear UID and Front Panel UID Indicators will illuminate. Push either button again to turn off both indicators. These UID indicators provide easy identification of a system unit that may be in need of service.

UID Button Pin Definitions	
Pin#	Definition
1	Ground
2	Ground
3	Button In
4	Ground

Trusted Platform Module Header

The JTPM1 header is used to connect a Trusted Platform Module (TPM), available separately from a third-party vendor. A TPM is a security device that allows encryption and authentication of hard drives, disallowing access if the TPM associated with it is not installed in the system. See the table on the right for pin definitions.

Trusted Platform Module Header Pin Definitions (JTPM1)			
Pin#	Definition	Pin#	Definition
1	LCLK	2	GND
3	LFRAME	4	No Pin
5	LRESET	6	VCC5
7	LAD3	8	LAD2
9	VCC3	10	LAD1
11	LAD0	12	GND
13	RSV0	14	RSV1
15	SB3V	16	SERIRQ
17	GND	18	CLKRUN
19	LPCPD	20	RSV2

Compact Flash Card PWR Connector

A Compact Flash Card Power Connector is located at JWF1.

Fan Headers

This motherboard has nine fan headers (Fan1 to Fan9). These 4-pin fans headers are backward compatible with 3-pin fans. However, fan speed control is available for 4-pin fans only. The fan speeds are controlled by IPMI software. See the table on the right for pin definitions

Fan Header Pin Definitions	
Pin#	Definition
1	Ground
2	+12V
3	Tachometer
4	PWR Modulation



2-9 Jumper Settings

Explanation of Jumpers

To modify the operation of the motherboard, jumpers can be used to choose between optional settings. Jumpers create shorts between two pins to change the function of the connector. Pin 1 is identified with a square solder pad on the printed circuit board. See the diagram at right for an example of jumping pins 1 and 2. Refer to the motherboard layout page for jumper locations.

Note: On two-pin jumpers, "Closed" means the jumper is on and "Open" means the jumper is off the pins.

CMOS Clear

JBT1 is used to clear CMOS, which will also clear any passwords. Instead of pins, this jumper consists of contact pads to prevent accidentally clearing the contents of CMOS.

To Clear CMOS

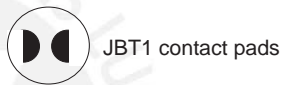
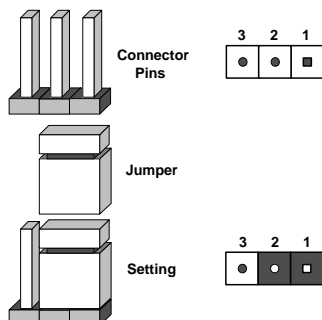
1. First power down the system and unplug the power cord(s). It is also recommended that you remove the onboard battery from the serverboard.
2. With the power disconnected, short the CMOS pads with a metal object such as a small screwdriver.
3. Remove the screwdriver (or shorting device).
4. Reconnect the power cord(s) and power on the system.

Note 1. For an ATX power supply, you must completely shut down the system, remove the AC power cord, and then short JBT1 to clear CMOS.

Note 2. Be sure to remove the onboard CMOS Battery before you short JBT1 to clear CMOS.

Note 3. Clearing CMOS will also clear all passwords.

Note 4: Do not use the PW_ON connector to clear CMOS.



I²C to PCI-Express Slot

JI²C1/JI²C2 allows you to enable the I²C bus to communicate with the PCI-Express slot. For the jumpers to work properly, please set both jumpers to the same setting. If enabled, both jumpers must be enabled. If disabled, both jumpers must be disabled. See the table on the right for jumper settings.

I ² C to PCI-Express Slot Jumper Settings (JI ² C1/JI ² C2)	
Jumper Setting	Definition
Closed	Enabled
Open	Disabled

Watch Dog Enable/Disable

JWD1 enables the Watch Dog function, a system monitor that takes action when a software application freezes the system. Jumping pins 1-2 will have WD reboot the system if a program freezes. Jumping pins 2-3 will generate a non-maskable interrupt for the program that has frozen. See the table on the right for jumper settings. Watch Dog must also be enabled in BIOS.

Watch Dog Jumper Settings (JWD1)	
Jumper Setting	Definition
Pins 1-2	Reset
Pins 2-3	NMI
Open	Disabled

Note: When Watch Dog is enabled, the user must write their own application software to disable the Watch Dog Timer.

VGA Enable/Disable

JPG1 allows you to enable or disable the VGA port. The default position is on pins 1 and 2 to enable VGA. See the table on the right for jumper settings.

VGA Enable/Disable Jumper Settings (JPG1)	
Jumper Setting	Definition
Pins 1-2	Enabled
Pins 2-3	Disabled

LAN1/2 Enable/Disable

Change the setting of jumper JPL1 to enable or disable the LAN1 and LAN2 Ethernet ports. See the table on the right for jumper settings. The default setting is enabled.

LAN1/2 En/Disable Jumper Settings (JPL1)	
Jumper Setting	Definition
Pins 1-2	Enabled
Pins 2-3	Disabled

BMC Jumper

JPB1 is used to enable or disable the BMC (Baseboard Management Control) Chip and the onboard IPMI connection. This jumper is used together with the IPMI settings in the BIOS. The default position is on pins 1 and 2 to Enable BMC. See the table on the right for jumper settings.

BMC Jumper Enable (JPB1) Jumper Settings	
Jumper Setting	Definition
Pins 1-2	Enabled (default)
Pins 2-3	Disabled

SAS Enable/Disable

JPS1 allows you to enable or disable the SAS controller. The default position is on pins 1 and 2 to enable SAS. See the table on the right for jumper settings. This LED is only available on the H8QGL-6F serverboard.

SAS Enable/Disable Jumper Settings (JPS1)	
Jumper Setting	Definition
Pins 1-2	Enabled
Pins 2-3	Disabled

2-10 Onboard Indicators

GLAN LEDs

There are two LAN ports (LAN1/2) on the motherboard. Each Ethernet LAN port has two LEDs. The Yellow LED on the right indicates connection and activity. The Link LED on the left side may be green, amber or off to indicate the speed of the connection. See the tables at right for more information.

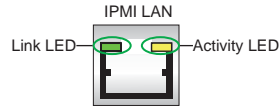


GLAN Activity Indicator (Right) LED Settings		
Color	Status	Definition
Off	No Connections	
Yellow	Flashing	Active

LAN Connection Speed Indicator (Left) LED Settings	
LED Color	Definition
Off	10 MHz
Green	100 MHz
Amber	1 GHz

IPMI Dedicated LAN LEDs

In addition to LAN Ports 1/2, an IPMI Dedicated LAN is also located on the I/O Backplane. The amber LED on the right indicates connection and activity; while the green LED on the left indicates the speed of the connection. See the tables at right for more information.



IPMI LAN Link/Speed LED (Left) & Activity LED (Right)		
Color	Status	Definition
Off	Off	No Connection
Green: Solid	Link/ Speed (Left)	100 Mb/s
Amber Blinking	Activity (Right)	Active

Power LED

DP3 is an Onboard Power LED. When this LED is lit, it means power is present on the serverboard. Be sure to turn off the system and unplug the power cord(s) before removing or installing components.

Power LED (DP3)	
State	System Status
On	Standby power present on motherboard
Off	No power connected

IPMI LED

The serverboard contains an IPMI LED (DP1) located near the corner above the PCI-E slots. When this LED is lit, it means a connection is active for the built-in IPMI on the serverboard.

IPMI LED (DP1)	
State	System Status
On	Active connection
Off	No connection

Note: This LED is not installed on non-IPMI boards.

UID LED (LE1)

A rear UID LED Indicator, located at LE1, works in conjunction with the rear UID switch to provide easy identification for a unit that might be in need of service. Refer to Page 2-18 for further UID details.

2-11 SAS and SATA Drive Connections

SATA Ports

There are no jumpers to configure the SATA ports, which are designated SATA0 through SATA5. See the table on the right for pin definitions.

SATA Ports Pin Definitions (SATA0-SATA5)	
Pin#	Definition
1	Ground
2	TXP
3	TXN
4	Ground
5	RXN
6	RXP
7	Ground

SAS Ports

There are eight SAS ports included only on the H8QGL-6F serverboard. See the table on the right for pin definitions.

Note: JPS1 must be set correctly to enable the SAS controller.

SAS Ports Pin Definitions (SAS0 ~ SAS7)			
Pin#	Definition	Pin#	Definition
1	Ground	2	TXP
3	TXN	4	Ground
5	RXN	6	RXP
7	Ground		

2-12 Enabling SATA RAID

Now that the hardware is set up, you must install the operating system and the SATA RAID drivers, if you wish to use RAID with your SATA drives. The installation procedure differs depending on whether you wish to have the operating system installed on a RAID array or on a separate non-RAID drive. See the instructions below for details.

Serial ATA (SATA)

Serial ATA (SATA) is a physical storage interface that employs a single cable with a minimum of four wires to create a point-to-point connection between devices. This connection is a serial link that supports a SATA transfer rate from 150 MBps. The serial cables used in SATA are thinner than the traditional cables used in Parallel ATA (PATA) and can extend up to one meter in length, compared to only 40 cm for PATA cables. Overall, SATA provides better functionality than PATA.

Installing the OS/SATA Driver

Before installing the OS (operating system) and SATA RAID driver, you must decide if you wish to have the operating system installed as part of a bootable RAID array or installed to a separate non-RAID hard drive. If on a separate drive, you may install the driver either during or after the OS installation. If you wish to have the OS on a SATA RAID array, you must follow the procedure below and install the driver during the OS installation.

Building a Driver Diskette

You must first build a driver diskette from Supermicro drivers for your system. Drivers can be found at <ftp://ftp.supermicro.com>. (You will have to create this disk on a computer that is already running and with the OS installed.)

Building a Driver Diskette

1. Install your system drives from the FTP website. A display as shown in Figure 2-7 will appear.
2. Click on the icon labeled "Build Driver Diskettes and Manuals" and follow the instructions to create a floppy disk with the drivers on it.
3. Once it's been created, remove the floppy and insert the installation CD for the Windows Operating System you wish to install into the CD-ROM drive of the new system you are about to configure.

Note: You need to have an external USB floppy when building the driver diskette. Window's Vista, Windows 2008 or later Windows OS systems can use a USB stick instead of a floppy.

Enabling SATA RAID in the BIOS

Before installing the Windows operating system, you must change some settings in the BIOS. Boot up the system and hit the <Delete> key to enter the BIOS Setup Utility. After the setup utility loads,

1. Use the arrow keys to move to the "Exit" menu. Scroll down using the arrow keys to "Load Optimal Defaults" and press <Enter>. Select "OK" to confirm, then <Enter> to load the default settings.
2. Use the arrow keys to move to the "Advanced" menu, then scroll down to "IDE configuration". On this submenu, scroll down to "OnChip SATA Type" and choose the "RAID" option (Figure 2-4). "RAID Codebase" submenu appears. This setting allows you to select the codebase for your RAID setup. Options are either Adaptec or DotHill.

Figure 2-4. BIOS Setup Screen



3. Press the <Esc> key twice and scroll to the "Exit" menu. Select "Save Changes and Exit" and press <Enter>, then press <Enter> again to verify.
4. After exiting the BIOS Setup Utility, the system reboots. When prompted during the startup, to use the DotHill RAID Utility program press the <CTRL+R> key (Figure 2-5), or to use the Adaptec RAID Utility program press the <CTRL+A> key (Figure 2-6).

Figure 2-5. DotHill RAID Utility Program Screen

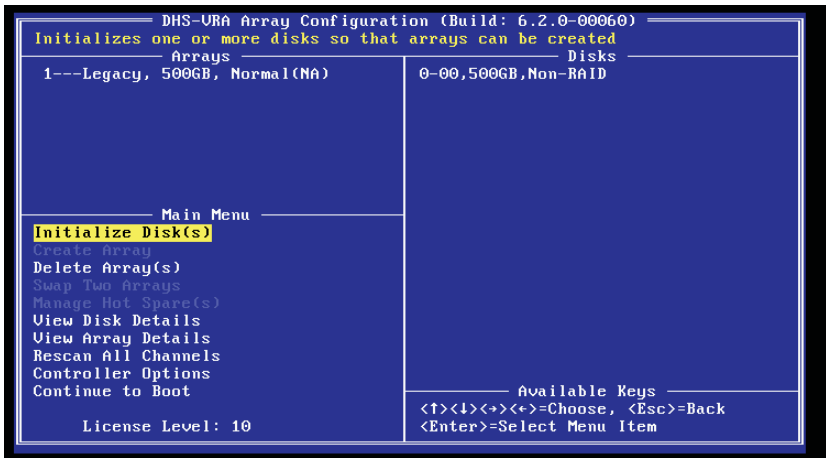
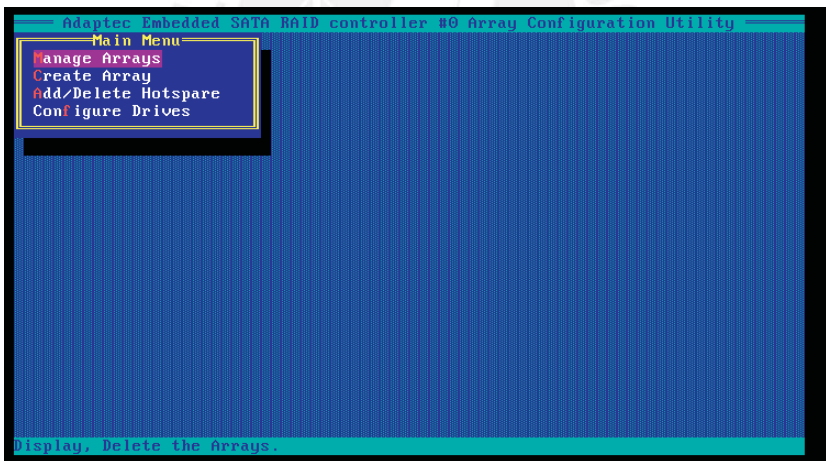


Figure 2-5.Adaptec RAID Utility Program Screen



Using the DotHill and Adaptec RAID Utility

The RAID Utility program allows you to define the drives you want to include in the RAID array and the mode and type of RAID.

Installing the RAID Driver During OS Installation

You may also use the procedure below to install the RAID driver during the Windows OS installation:

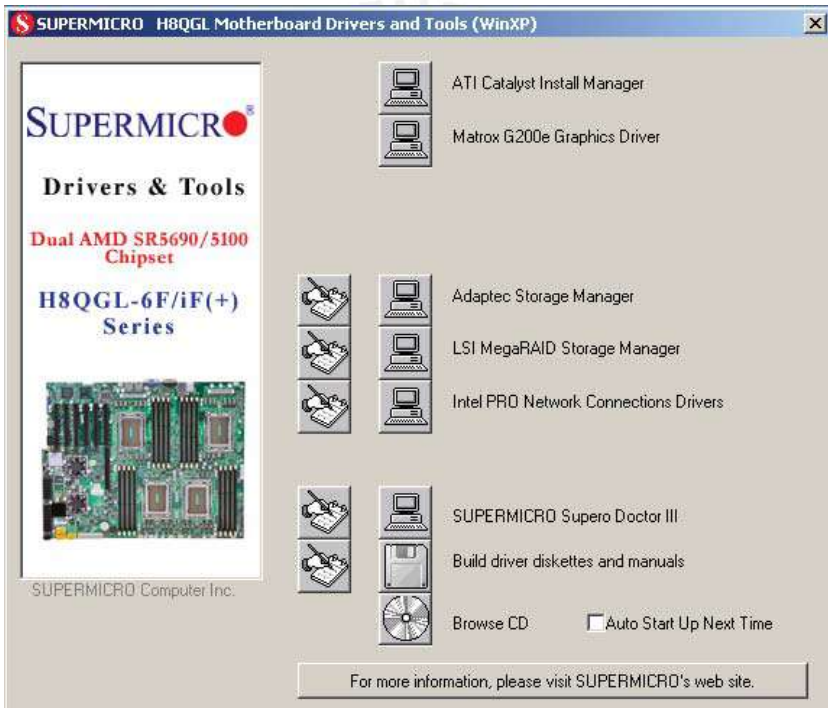
1. With the Windows OS installation CD-ROM in the CD drive, restart the system.
2. Press <Enter> again to continue with the Windows setup.
3. When you see the prompt, hit the <F6> key to enter Windows setup.
4. Eventually a blue screen will appear with a message that begins "Windows could not determine the type of one or more storage devices . . ." When you see the screen, hit the <S> key to "Specify Additional Device", then insert the driver diskette you just created into the floppy drive.
5. Highlight "Manufacturer Supplied Hardware Support Disk" and hit the <Enter> key.
6. Highlight the first "Adaptec RAID" driver shown and press the <Enter> key to install it.

2-13 Installing Drivers

The Supermicro Website contains drivers and utilities for your system at <ftp://ftp.supermicro.com>, some of which must be installed, such as the chipset driver. After downloading and installing the drivers and utilities, the display shown in Figure 2-7 should appear.

Click the icons showing a hand writing on paper to view the readme files for each item. Click the computer icons to the right of these items to install each item (from top to the bottom) one at a time. After installing each item, you should reboot the system before moving on to the next item on the list. The bottom icon with a CD on it allows you to view the entire contents of the utilities.

Figure 2-7. Driver/Tool Installation Display Screen



SuperDoctor III

The SuperDoctor® III program is a Web base management tool that supports remote management capability. It includes Remote and Local Management tools. The local management is called SD III Client. The SuperDoctor III program included on the CD-ROM that came with your motherboard allows you to monitor the environment and operations of your system. SuperDoctor III displays crucial system information such as CPU temperature, system voltages and fan status. See the Figure below for a display of the SuperDoctor III interface.

Note: The default User Name and Password for SuperDoctor III is ADMIN / ADMIN.

Note: When SuperDoctor is first installed, it adopts the temperature threshold settings that have been set in BIOS. Any subsequent changes to these thresholds must be made within SuperDoctor, as the SuperDoctor settings override the BIOS settings. To set the BIOS temperature threshold settings again, you would first need to uninstall SuperDoctor.

Figure 2-8. SuperDoctor III Interface Display Screen (Health Information)



Figure 2-9. SuperDoctor III Interface Display Screen (Remote Control)

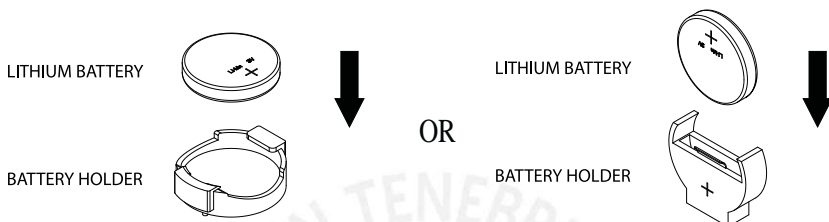


Note: The SuperDoctor III program and User's Manual can be downloaded from the Supermicro web site at <http://www.supermicro.com/products/accessories/software/SuperDoctorIII.cfm>. For Linux, we recommend that you use the SuperDoctor II application instead.

2-14 Serverboard Battery

Caution: There is a danger of explosion if the onboard battery is installed upside down, which will reverse its polarities (see Figure 2-10). This battery must be replaced only with the same or an equivalent type recommended by the manufacturer (CR2032). Dispose of used batteries according to the manufacturer's instructions.

Figure 2-10. Installing the Onboard Battery



Please handle used batteries carefully. Do not damage the battery in any way; a damaged battery may release hazardous materials into the environment. Do not discard a used battery in the garbage or a public landfill. Please comply with the regulations set up by your local hazardous waste management agency to dispose of your used battery properly.

Chapter 3

Troubleshooting

3-1 Troubleshooting Procedures

Use the following procedures to troubleshoot your system. If you have followed all of the procedures below and still need assistance, refer to the 'Technical Support Procedures' and/or 'Returning Merchandise for Service' section(s) in this chapter. Always disconnect the AC power cord before adding, changing or installing any hardware components.

Before Power On

1. Check that the onboard power LED is lit (DP3 on the motherboard).
2. Make sure that the power connector is connected to your power supply.
3. Make sure that no short circuits exist between the motherboard and chassis.
4. Disconnect all cables from the motherboard, including those for the keyboard and mouse.
5. Remove all add-on cards.
6. Install a CPU and heatsink (making sure it is fully seated) and connect the internal (chassis) speaker and the power LED to the motherboard. Check all jumper settings as well.
7. Use the correct type of onboard CMOS battery (CR2032) as recommended by the manufacturer. To avoid possible explosion, do not install the CMOS battery upside down.

No Power

1. Make sure that no short circuits exist between the motherboard and the chassis.
2. Verify that all jumpers are set to their default positions.
3. Check that the 115V/230V switch on the power supply is properly set.
4. Turn the power switch on and off to test the system.
5. The battery on your motherboard may be old. Check to verify that it still supplies ~3VDC. If it does not, replace it with a new one.

No Video

1. If the power is on but you have no video, remove all the add-on cards and cables.
2. Use the speaker to determine if any beep codes exist. Refer to Appendix A for details on beep codes.

Note: If you are a system integrator, VAR or OEM, a POST diagnostics card is recommended. For I/O port 80h codes, refer to Appendix B.

Memory Errors

1. Make sure that the DIMM modules are properly and fully installed.
2. You should be using registered ECC DDR-3 memory (see next page). Also, it is recommended that you use the same memory type and speed for all DIMMs in the system. [See Section 2-5 for memory details.](#)
3. Check for bad DIMM modules or slots by swapping modules between slots and noting the results.
4. Check the power supply voltage 115V/230V switch.

Losing the System's Setup Configuration

1. Make sure that you are using a high quality power supply. A poor quality power supply may cause the system to lose the CMOS setup information. Refer to Section 1-6 for details on recommended power supplies.
2. The battery on your motherboard may be old. Check to verify that it still supplies ~3VDC. If it does not, replace it with a new one.
3. If the above steps do not fix the setup configuration problem, contact your vendor for repairs.

3-2 Technical Support Procedures

Before contacting Technical Support, please take the following steps. Also, note that as a motherboard manufacturer, we do not sell directly to end-users, so it is best to first check with your distributor or reseller for troubleshooting services. They should know of any possible problem(s) with the specific system configuration that was sold to you.

1. Please review the 'Troubleshooting Procedures' and 'Frequently Asked Questions' (FAQs) sections in this chapter or see the FAQs on our web site before contacting Technical Support.
2. BIOS upgrades can be downloaded from our web site.

Note: Not all BIOS can be flashed depending on the modifications to the boot block code.

3. If you still cannot resolve the problem, include the following information when contacting us for technical support:
 - Serverboard model and PCB revision number
 - BIOS release date/version (this can be seen on the initial display when your system first boots up)
 - System configuration

An example of a Technical Support form is posted on our web site.

Distributors: For immediate assistance, please have your account number ready when contacting our technical support department by e-mail.

3-3 Frequently Asked Questions

Question: What type of memory does my motherboard support?

Answer: The H8QGL-6/iF serverboard supports up to sixteen (16) single/dual/tri/quad channel DIMM slots supporting up to 128 GB of ECC/Non-ECC UDIMM or up to 512 GB of ECC RDIMM/LRDIMM DDR3-1866/1600/1333/1066 Mhz speed, 1 GB, 2 GB, 4 GB, 8 GB, 16 GB or 32 GB size SDRAM (or up to 128 GB with a single CPU installed). Both single and dual channel configurations are supported. See Section 2-5 for details on installing memory.

Question: How do I update my BIOS?

Answer: It is recommended that you **not** upgrade your BIOS if you are not experiencing problems with your system. Updated BIOS files are located on our web site. Please check our BIOS warning message and the information on how to update your BIOS on our web site. Also, check the current BIOS revision and make sure it is newer than your current BIOS before downloading.

Select your motherboard model on the web page and download the corresponding BIOS file to your computer. Unzip the BIOS update file, in which you will find the readme.txt (flash instructions), the afudos.smc (BIOS flash utility) and the BIOS image (H8xxx.xxx) files. Copy these files to a bootable floppy disk, insert the disk into drive A and reboot the system. At the DOS prompt after rebooting, enter the command "flash" (without quotation marks) then type in the BIOS file that you want to update with (xxx.xxx).rom).

Use the procedures below to flash from a BIOS flash floppy or USB disk.

For <filename>.exe

1. Run the <filename>.exe file under Windows to create the BIOS flash floppy disk.
2. Insert the floppy, into the system for which you wish to flash the BIOS.
3. Boot up the system for which you wish to flash the BIOS.
4. The BIOS utility will run automatically and begin flashing the BIOS WITHOUT any prompts.
5. After the BIOS completes the flashes, system will reboot or needs manually reboot.
6. It will show "CMOS Checksum Error" on the POST, press F1 key to boot into BIOS setup page.
7. Hit F9 Key to load optimal default setting, and change other BIOS setting if you needed.
8. Hit F10 to save the BIOS setting and system reboots.

For <filename>.zip

1. Prepare a DOS or 98 bootable USB disk.
2. Extract <filename>.zip file under Windows into the USB disk.
3. Boot up system for which BIOS will be flashed from 98 bootable USB disk.
4. At the prompt, type: [flash H8xxxxx.xxx] and hit enter.
5. After the BIOS completes the flashes, system will reboot or needs manually reboot
6. It will show "CMOS Checksum Error" on the POST, press F1 key to boot into BIOS setup page.

Warning: Flashing the wrong BIOS can cause harm to the system.

7. Hit F9 Key to load optimal default setting, and change other BIOS setting if you needed.
8. Hit F10 to save the BIOS setting and system reboots.

Question: What's on the CD that came with my motherboard?

Answer: The supplied compact disc has quite a few drivers and programs that will greatly enhance your system. We recommend that you review the CD and install the applications you need. Applications on the CD include chipset drivers for Windows and security and audio drivers.

Question: Why can't I turn off the power using the momentary power on/off switch?

Answer: The instant power off function is controlled in BIOS by the Power Button Mode setting. When the On/Off feature is enabled, the motherboard will have instant off capabilities as long as the BIOS has control of the system. When the Standby or Suspend feature is enabled or when the BIOS is not in control such as during memory count (the first screen that appears when the system is turned on), the momentary on/off switch must be held for more than four seconds to shut down the system. This feature is required to implement the ACPI features on the motherboard.

3-4 Returning Merchandise for Service

A receipt or copy of your invoice marked with the date of purchase is required before any warranty service will be rendered. You can obtain service by calling your vendor for a Returned Merchandise Authorization (RMA) number. When returning to the manufacturer, the RMA number should be prominently displayed on the outside of the shipping carton, and mailed prepaid or hand-carried. Shipping and handling charges will be applied for all orders that must be mailed when service is complete.

For faster service, RMA authorizations may be requested online (<http://www.supermicro.com/support/rma/>).

This warranty only covers normal consumer use and does not cover damages incurred in shipping or from failure due to the alteration, misuse, abuse or improper maintenance of products.

During the warranty period, contact your distributor first for any product problems.

Notes



Chapter 4

BIOS

4-1 Introduction

This chapter describes the AMIBIOS™ Setup utility for the H8QGL-6/iF serverboard. The 16 Mb AMI BIOS® is stored in a flash chip and can be easily upgraded using a floppy disk-based program.

Note: Due to periodic changes to the BIOS, some settings may have been added or deleted and might not yet be recorded in this manual. Please refer to the Manual Download area of our web site for any changes to BIOS that may not be reflected in this manual.

Starting the Setup Utility

To enter the BIOS Setup Utility, hit the <Delete> key while the system is booting-up. (In most cases, the <Delete> key is used to invoke the BIOS setup screen. There are a few cases when other keys are used, such as <F1>, <F2>, etc.) Each main BIOS menu option is described in this manual.

The Main BIOS screen has two main frames. The left frame displays all the options that can be configured. "Grayed-out" options cannot be configured. The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it. (Note that BIOS has default text messages built in. We retain the option to include, omit, or change any of these text messages.) Settings printed in **Bold** are the default values.

A " ► " indicates a submenu. Highlighting such an item and pressing the <Enter> key will open the list of settings within that submenu.

The BIOS setup utility uses a key-based navigation system called hot keys. Most of these hot keys (<F1>, <F10>, <Enter>, <ESC>, <Arrow> keys, etc.) can be used at any time during the setup navigation process.

4-2 Main Menu

When you first enter AMI BIOS Setup Utility, you will see the Main Menu screen. You can always return to the Main Menu by selecting the **Main** tab on the top of the screen with the arrow keys.

The Main Menu screen provides you with a system overview, which includes the version, built date and ID of the AMIBIOS, the type, speed and number of the processors in the system and the amount of memory installed in the system.

System Time/System Date

You can edit this field to change the system time and date. Highlight *System Time* or *System Date* using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in DAY/MM/DD/YYYY format. The time is entered in HH:MM:SS format. Please note that time is in a 24-hour format. For example, 5:30 A.M. appears as 05:30:00 and 5:30 P.M. as 17:30:00.

4-3 Advanced Settings Menu

► Boot Features

Quick Boot

If enabled, this setting will skip certain tests during POST to reduce the time needed for the system to boot up. The options are **Enabled** and Disabled.

Quiet Boot

If disabled, normal POST messages will be displayed on boot-up. If enabled, this display the OEM logo instead of POST messages. Options are **Enabled** or Disabled.

Add On ROM Display Mode

This sets the display mode for Option ROM. The options are **Force BIOS** or Keep Current.

Bootup Num Lock

This setting selects the power-on state for the NUM lock to either **On** or Off.

Wait for F1 if Error

This setting controls the system response when an error is detected during the boot sequence. When enabled, BIOS will stop the boot sequence when an error is detected, at which point you will need to press the F1 button to re-enter the BIOS setup menu. The options are **Enabled** and Disabled.

Hit 'DEL' Message Display

Use this setting to **enable** or disable the "Press DEL to run setup" message in POST. Options are Enabled or **Disabled**.

Interrupt 19 Capture

Select enabled to allow ROMs to trap Interrupt 19. The options are **Enabled** and Disabled.

Power Button Function

This set the power button function to either **Instant Off** or 4 Seconds Override when pressed.

Restore on AC Power Loss

This sets the action that occurs when an AC power loss occurs. Options include Power Off, Power On and **Last State**.

Watch Dog Timer

This sets the Watch Dog Timer. Options include Enabled or **Disabled**.

► Processor & Clock Options

CPU Configuration and Information

This static display provides information on the Module Version, Socket Count, Node Count and Core Count for the system's processor(s) and clock. Additional information on the installed processor, Revision, Cache sizes (L1, L2 and L3), Speed, Ability to Change Frequency and uCode Patch Level are also shown. The CPU information can be toggled between viewing **CPU Socket 0** and CPU Socket 1.

Note: Zero is always the "Boot Strap Processor" or main CPU with all others being "Application Processors".

GART Error Reporting

This setting should remain **disabled** for normal operation. The driver developer may enable this option for testing purposes. Options are Enabled or **Disabled**.

Microcode Update

This setting **enables** or disables microcode updating. Options are **Enabled** or **Disabled**.

Secure Virtual Machine Mode

This setting allows you to **enable** or disable Secure Virtual Machine Mode (SVM) on your system. Options are **Enabled** or **Disabled**.

Power Now

This setting is used to **enable** or disable the AMD Power Now feature. Options are **Enabled** or **Disabled**.

Power Cap

This setting can decide the highest performance P-state in the Operating System. Options include **P-state 0**, P-state 1, P-state 2, P-state 3 and P-state 4.

CPU DownCore Mode

This sets the CPU DownCore Mode for your system. If you change this option then a cold reset is required. Options include **Disabled**, 1 Core, 2 Cores and 3 Cores.

C1E Support

This enables or disables C1E Support for your system. Options are **Enable** or **Disable**.

► Advanced Chipset Control

Chipset Information

Chipset Information is displayed at the top of this menu on the chipset CIMx version used.

► NorthBridge Chipset Configuration

► Memory Configuration

Bank Interleaving

This setting allows you to enable Bank Interleaving in the system. Options include **Auto** and **Disabled**.

Node Interleaving

This setting allows you to enable Node Interleaving in the system. Options include Auto and **Disabled**.

Channel Interleaving

This setting allows you to enable Channel Interleaving in the system. The options are **Auto** and Disabled.

CS Sparing Enable

This setting will reserve a spare memory rank in each node when enabled. Options are Enable and **Disable**.

Bank Swizzle Mode

This setting **enables** or disables the Bank Swizzle Mode. Options are **Enabled** or Disabled.

► ECC Configuration

ECC Mode

This submenu sets the level of ECC protection. Options include Disabled, **Basic**, Good, Super, Max and User. Selecting User activates the other option for user setting.

Note: The "Super" ECC mode dynamically sets the DRAM scrub rate so all of memory is scrubbed in 8-hours.

DRAM ECC Enable

This setting allows hardware to report and correct memory errors automatically, maintaining system integrity. Options are **Enabled** or Disabled.

► DRAM Timing Configuration

DRAM Timing Config

This setting specifies the DRAM timing configuration. Options are **Auto** and Manual.

HT Speed Support

This setting allows you to select the HT Frequency to use. Cold reset is needed after changing an option for this setting. Option include **Auto** and HT1.

IOMMU

This setting is used to disable or set the GART size in systems without AGP. Options include Enabled and **Disabled**.

Memory Timing Parameters

This selects the which node's timing parameters to display. The only selection for this option is **CPU Node 0**.

Clock Speed Information

Clock speed information for memory is displayed under this Northbridge Chipset Configuration page. This information includes Memory CLK, CAS Latency (Tcl), RAS/CAS Delay (Trcd), Row Precharge Time (Trp), Min Active RAS (Tras), RAS/RAS Delay (Trrd), Row Cycle (Trc), Read to Precharge (Trtp), Write Recover Time (Twr) and Memory Type.

► SouthBridge Chipset Configuration

SouthBridge Chipset Information

SouthBridge chipset information is displayed at the top of this menu on the SouthBridge chipset CIMx version used.

OHCI/EHCI HC Device Functions

These settings allow you to either **enable** or **isable** functions for OHCI or EHCI bus devices. Options are **Enabled** or **Disabled**.

USB 2.0 Controller Mode

Use this setting to configure the USB 2.0 Controller in either **Hi-Speed** (480 Mps) or **Full Speed** (12 Mps) mode.

Legacy USB Support

Select "Enabled" to enable the support for USB Legacy. Disable Legacy support if there are no USB devices installed in the system. "Auto" disabled Legacy support if no USB devices are connected. The options are **Disabled**, **Enabled** and **Auto**.

► IDE/SATA Configuration

OnChip SATA Channel

This setting allows you to **enable** or **disable** the OnChip SATA channel. Options are **Enabled** or **Disabled**.

OnChip SATA Type

Use this setting to set the OnChip SATA type. Options include **Native IDE**, RAID, Legacy IDE and AMD_AHCI.

RAID Codebase

This submenu appears when you choose "RAID" from the "OnChip SATA Type" setting above. This setting allows you to select the codebase for using your RAID setup. Options are either Adaptec or **DotHill**.

SATA IDE Combined Mode

This setting allows you to **enable** or disable the SATA IDE combined mode. Options are **Enabled** or Disabled.

PATA Channel Configuration

This setting allows you to set PATA channel configuration. Options include **SATA as Primary** or SATA as secondary.

► Primary/Secondary/Third IDE Master/Slave

LBA/Large Mode

LBA (Logical Block Addressing) is a method of addressing data on a disk drive. The options are Disabled and **Auto**.

Block (Multi-Sector Transfer)

Block mode boosts IDE drive performance by increasing the amount of data transferred. Only 512 bytes of data can be transferred per interrupt if block mode is not used. Block mode allows transfers of up to 64 KB per interrupt. Select "Disabled" to allow the data to be transferred from and to the device one sector at a time. Select "Auto" to allow the data transfer from and to the device occur multiple sectors at a time if the device supports it. The options are **Auto** and Disabled.

PIO Mode

PIO (Programmable I/O) mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases. The options are **Auto**, 0, 1, 2, 3, and 4. Select Auto to allow BIOS to auto detect the PIO mode.

Use this value if the IDE disk drive support cannot be determined. Select 0 to allow BIOS to use PIO mode 0, which has a data transfer rate of 3.3 MBs. Select 1 to allow BIOS to use PIO mode 1, which has a data transfer rate of 5.2 MBs. Select 2 to allow BIOS to use PIO mode 2, which has a data transfer rate of 8.3 MBs. Select 3 to allow BIOS to use PIO mode 3, which has a data transfer rate of 11.1 MBs. Select 4 to allow BIOS to use PIO mode 4, which has a data transfer rate of 16.6 MBs. This setting generally works with all hard disk drives manufactured after 1999. For other disk drives, such as IDE CD-ROM drives, check the specifications of the drive.

DMA Mode

Selects the DMA Mode. Options are **Auto**, SWDMA0, SWDMA1, SWDMA2, MWDMA0, MDWDMA1, MWDMA2, UDMA0, UDMA1, UDMA2, UDMA3, UDMA4 and UDMA5. (SWDMA=Single Word DMA, MWDMA=Multi Word DMA, UDMA=UltraDMA.)

S.M.A.R.T.

Self-Monitoring Analysis and Reporting Technology (SMART) can help predict impending drive failures. Select "Auto" to allow BIOS to auto detect hard disk drive support. Select "Disabled" to prevent AMI BIOS from using the S.M.A.R.T. Select "Enabled" to allow AMI BIOS to use the S.M.A.R.T. to support hard drive disk. The options are Disabled, Enabled, and **Auto**.

32-Bit Data Transfer

Select "Enabled" to activate the function of 32-Bit data transfer. Select "Disabled" to deactivate the function. The options are **Enabled** and Disabled.

IDE Detect Timeout (Sec)

Use the +/- keys to adjust and select the time out for detecting ATA/ATAPI devices. The default value is **35**.

► PCI/PNP Configuration

Clear NVRAM

Select Yes to clear NVRAM during boot-up. The options are Yes and **No**.

Plug & Play O/S

This setting allows you to configure Plug & Play devices for your system. Select Yes to allow the OS to configure Plug & Play devices. (This is not required for system boot if your system has an OS that supports Plug & Play.) Select **No** to allow the AMIBIOS to configure all devices in the system.

PCI Latency Timer

This option sets the latency of all PCI devices on the PCI bus. Select a value to set the PCI latency in PCI clock cycles. Options are 32, **64**, 96, 128, 160, 192, 224 and 248.

PCI IDE Busmaster

Use this setting to **enable** or disable BIOS enabled uses of PCI Busmastering for reading or writing to IDE drives. Options are **Enabled** or Disabled.

ROM Scan Ordering

This setting determines which kind of option ROM activates prior to another. Options include **Onboard First** or Addon First.

Slot 1 ~ Slot 6 PCI-E OPROM

These four settings (Slot 1 through Slot 4) allow you to **enable** or disable the numbered slot's Op ROM, except for the VGA card. Options are **Enabled** or Disabled.

Load Onboard LAN 1 Option ROM

This setting allows you to enable or disable the loading of onboard LAN1 option ROM. Options are **Enabled** or Disabled.

Load Onboard LAN 2 Option ROM

This setting allows you to enable or disable the loading of onboard LAN2 option ROM. Options are Enabled or **Disabled**.

Onboard NIC Option ROM Select

This setting allows you to disable or select the onboard NIC option ROM. Options include **PXE** and iSCSI.

Boots Graphic Adapter Priority

Use this setting to set which graphic adapter to use on boot-up. Options include **Offboard VGA** and Onboard VGA.

► SuperI/O Configuration

Serial 1 Address

This option specifies the base I/O port address and Interrupt Request address of serial port 1. Select "Disabled" to prevent the serial port from accessing any system resources. When this option is set to *Disabled*, the serial port physically becomes unavailable. Select "3F8/IRQ4" to allow the serial port to use 3F8 as its I/O port address and IRQ 4 for the interrupt address. Options include Disabled, **3F8/IRQ4** and 2E8/IRQ3

Serial 2 Address

This option specifies the base I/O port address and Interrupt Request address of serial port 2. Select "Disabled" to prevent the serial port from accessing any system resources. When this option is set to "Disabled", the serial port physically becomes unavailable. Select "2F8/IRQ3" to allow the serial port to use 2F8 as its I/O port address and IRQ 3 for the interrupt address. Options include Disabled, **2F8/IRQ3** and 2E8/IRQ3.

► Remote Access Configuration

Remote Access

Use this option to **enable** or disable Remote Access in your system. If enabled, the settings below will appear. Options are **Enabled** or Disabled.

Serial Port Number

Use this setting to select the serial port for console redirection. Options include COM1, COM2 or **COM3**. The displayed base address and IRQ for the serial port changes to reflect the selection you make.

Note: Make sure the selected port is enabled.

Serial Port Mode

Selects the serial port settings to use. Options are **(115200 8, n, 1)**, (57600 8, n, 1), (38400 8, n, 1), (19200 8, n, 1) and (09600 8, n, 1).

Flow Control

Selects the flow control to be used for console redirection. Options are **None**, Hardware and Software.

Redirection After BIOS POST

This sets redirection after the BIOS POST for your system.

Options are Disabled (no redirection after BIOS POST), Boot Loader (redirection during POST and during boot loader) and **Always** (redirection always active). Note that some OS's may not work with this set to Always.

Terminal Type

Selects the type of the target terminal. Options are **ANSI**, VT100 and VT-UTF8.

VT-UTF8 Combo Key Support

Allows you to **enable** or disable VT-UTF8 combination key support for ANSI/VT100 terminals. Options are **Enabled** or Disabled.

Sredir Memory Display Delay

Use this setting to set the delay in seconds to display memory information. Options are **No Delay**, 1 sec, 2 secs and 4 secs.

► Hardware Health Configuration

CPU Overheat Temperature

This setting allows you to specify the type of alarm for CPU overheating. Options include The Early Alarm and **The Default Alarm**.

Other items in the submenu are systems monitor displays for the following information:

CPU1 Temperature, CPU2 Temperature, CPU3 Temperature, CPU4 Temperature, System Temperature, CPU1 VCore, CPU2 VCore, CPU3 VCore, CPU4 VCore, CPU1~4 DIMM Voltage, Chipset SR56x0 Voltage, + 5V, +12V, 3.3V Vcc (V), 3.3V standby (Vsb) and Battery Voltage (Vbat).

CPU Temperature Display (CTD)

CPU Temperature descriptions are defined as:

Low → [Tctl Value = Lowest Value, Tctl Value = -45]

Medium → [Tctl Value = -46, Tctl Value = 60]

High → [Tctl Value = -61 and Above]

Note: Only CPU temperature (Low, Medium, High) and system temperature (RT1) are required to be displayed in BIOS and in-system monitoring software. Other

Serverboard components such as memory, chipset, SAS and 10Gb controllers, and others are not required to display temperatures. For debugging and testing purposes, BIOS and system monitoring software can show motherboard components' temperatures (such as memory, chipset, SAS and 10Gb controllers). However for SMCI standard release version BIOS and system monitoring software, motherboard components' temperatures are NOT required to be displayed.

CPU Overheating Alarm (COA)

CPU Overheating Alarm (COA) has “**Early Alarm**” and “**Default Alarm**” (default) options in the BIOS, and is required to be implemented in all fan speed control modes.

The **Early Alarm** is enabled when the Tctl value = 65, and is disabled when the Tctl value drops from 65 to 62.

The **Default Alarm** (default setting) is enabled when the Tctl value = 70, and is disabled when the Tctl value drops from 70 to 67.

When COA (either Early or Default Alarm) is *enabled*, the following actions are required to be executed:

- System overheating LED is required to be ON and to solid red.
- Onboard buzzer or speaker is required to be ON and to be a continuous sound.
- All system fans are required to be operated at full speed.
- System monitoring software (such as Super Doctor and IPMI if available) is required to report and record CPU overheating events in the event logs.

When COA (either Early or Default Alarm) is *disabled*, the following actions are required to be executed:

- System overheating LED is required to be OFF.
- Onboard buzzer or speaker is required to be OFF.
- All system fans are required to be returned to a normal, non-CPU-overheating LFSC condition.

Condition	When a CPU is overheating
Front Panel Overheating LED	On and Solid Red
Onboard Buzzer or Speaker	On and Continuous Sound
System Fan Speed Controls	Full Speed
BMC	Report PROCHOT
BMC Event Log	Record PROCHOT
Super Doctor	Report PROCHOT
Super Doctor Event Log	Record PROCHOT

► System Fan Monitor

This submenu contains lists the system fans and contains RPM information for them.

Fan Speed Control Modes

This submenu allows you to determine how the system will control the speed of the onboard fans. The options are Full Speed/FS (Max Cooling), Performance/PF (Better Cooling), **Balanced/BL** (Balance between performance and energy saving), Energy Saving/ES (Lower Power and Noise).

A display also showing the speeds of FAN1 Speed ~ FAN11 Speed is shown on this page.

► ACPI Configuration

ACPI Aware O/S

Use this setting to enable or disable ACPI support for the operating system if it supports ACPI. Options include **Yes** (enable ACPI support) or **No** (disable ACPI support).

ACPI Version Features

Use this setting to determine which ACPI version to use. Options are ACPI v1.0, **ACPI v2.0** and ACPI v3.0.

ACPI APIC Support

Determines whether to include the ACPI APIC table pointer in the RSDT pointer list. The available options are **Enabled** and **Disabled**.

Headless Mode

Use this setting to enable or **disable** headless operation mode through ACPI. Options are **Enabled** or **Disabled**.

WHEA Support

Use this setting to **enable** or disable Windows Hardware Error Architecture. Options are **Enabled** or **Disabled**.

NUMA Support

Use this setting to **enable** or disable the building of an ACPI SRAT table. Options are **Enabled** or **Disabled**.

► IPMI Configuration

This menu shows static information about the IPMI firmware revision and status of the BMC, as well as options for IPMI configuration.

► View BMC System Event Log

Pressing the Enter key will open the following settings. Use the "+" and "-" keys to navigate through the system event log.

Clear BMC System Event Log

Selecting this and pressing the Enter key will clear the BMC system event log.

► Set LAN Configuration

Use the "+" and "-" keys to choose the desired channel number. This displays Channel Number and Channel Number Status information.

IP Address Source

This sets the IP address source as either Static or **DHCP**. Selecting Static allows you to manually set the IP Address, Subnet Mask and Gateway Address.

IP Address

In the field provided here enter the IP address in the decimal form of xxx.xxx.xxx.xxx with xxx having a value of less than 256 and in decimal form only. The IP address and current IP address in the BMC are shown.

Subnet Mask

In the field provided here enter the Subnet address in the decimal form of xxx.xxx.xxx.xxx with xxx having a value of less than 256 and in decimal form only. The current subnet address in the BMC is shown.

Gateway Address

In the field provided here enter the Gateway address in the decimal form of xxx.xxx.xxx.xxx with xxx having a value of less than 256 and in decimal form only. The current Gateway address in the BMC is shown.

Current MAC Address in BMC

The current MAC address in the BMC is shown in this static display.

► Event Log Configuration

View Event Log

Pressing the Enter key will open the event log. Use the "↑" and "↓" keys to navigate through the system event log.

Mark All Events as Read

Selecting this and pressing the Enter key marks all events as read in the event log.

Clear Event Log

Selecting this and pressing the Enter key clears the system event log.

SR56x0 (RD890S) PCIE Error Log

This setting allows you set an error log ofr PCIE errors. Options include Yes or No.

4-6 Security Settings Menu

AMI BIOS provides a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first.

Change Supervisor Password

Select this option and press <Enter> to access the sub menu, and then type in the password.

Change User Password

Select this option and press <Enter> to access the sub menu, and then type in the password.

Boot Sector Virus Protection

This option is near the bottom of the Security Setup screen. Select "Disabled" to deactivate the Boot Sector Virus Protection. Select "Enabled" to enable boot sector protection. When "Enabled", AMI BIOS displays a warning when any program (or virus) issues a Disk Format command or attempts to write to the boot sector of the hard disk drive. The options are Enabled and **Disabled**.

4-5 Boot Settings Menu

▶ Boot Device Priority

This feature allows you to prioritize the boot sequence from the list of available devices. A device that is in parenthesis has been disabled in the corresponding type menu.

▶ Removable Drives

This feature allows you to specify the boot sequence from the list of available removable drives. A device that is in parenthesis has been disabled in the corresponding type menu.

▶ Hard Disk Drives

This feature allows you to specify the boot sequence from the list of available hard disk drives. A device that is in parenthesis has been disabled in the corresponding type menu.

▶ CD/DVD Drives

This feature allows you to specify the boot sequence from the list of available CD/DVD drives. A device that is in parenthesis has been disabled in the corresponding type menu.

▶ USB Drives

This feature allows you to specify the boot sequence from the list of available USB drives. A device that is in parenthesis has been disabled in the corresponding type menu.

▶ Network Drives

This feature allows you to specify the boot sequence from the list of available network drives. A device that is in parenthesis has been disabled in the corresponding type menu.

► Other Drives

This feature allows you to specify the boot sequence from the list of available other drives. A device that is in parenthesis has been disabled in the corresponding type menu.

Retry Boot Device

This setting allows you to enable or **disable** auto retry of all boot devices. Options are Enabled or **Disabled**.

4-8 Exit Menu

Select the Exit tab from AMI BIOS Setup Utility screen to enter the Exit BIOS Setup screen.

Save Changes and Exit

When you have completed the system configuration changes, select this option to leave BIOS Setup and reboot the computer, so the new system configuration parameters can take effect. Select Save Changes and Exit from the Exit menu and press <Enter>.

Discard Changes and Exit

Select this option to quit BIOS Setup without making any permanent changes to the system configuration and reboot the computer. Select Discard Changes and Exit from the Exit menu and press <Enter>.

Discard Changes

Select this option and press <Enter> to discard all the changes and return to AMI BIOS Utility Program.

Load Optimal Defaults

To set this feature, select Load Optimal Defaults from the Exit menu and press <Enter>. Then Select "OK" to allow BIOS to automatically load the Optimal Defaults as the BIOS Settings. The Optimal settings are designed for maximum system performance, but may not work best for all computer applications.

Load Fail-Safe Defaults

To set this feature, select Load Fail-Safe Defaults from the Exit menu and press <Enter>. The Fail-Safe settings are designed for maximum system stability, but not maximum performance.

Notes



Appendix A

BIOS Error Beep Codes

During the POST (Power-On Self-Test) routines, which are performed each time the system is powered on, errors may occur.

Non-fatal errors are those which, in most cases, allow the system to continue the boot-up process. The error messages normally appear on the screen.

Fatal errors are those which will not allow the system to continue the boot-up procedure. If a fatal error occurs, you should consult with your system manufacturer for possible repairs.

These fatal errors are usually communicated through a series of audible beeps. The numbers on the fatal error list (on the following page) correspond to the number of beeps for the corresponding error. All errors listed, with the exception of Beep Code 8, are fatal errors.

A-1 AMIBIOS Error Beep Codes

Beep Code	Error Message	Description
1 beep	Refresh	Circuits have been reset (Ready to power up)
5 short, 1 long	Memory error	No memory detected in system
1 long, 8 short	Video error	Video adapter disabled or missing

Notes



Appendix B

BIOS POST Checkpoint Codes

When AMIBIOS performs the Power On Self Test, it writes checkpoint codes to I/O port 0080h. If the computer cannot complete the boot process, diagnostic equipment can be attached to the computer to read I/O port 0080h.

B-1 Uncompressed Initialization Codes

The uncompressed initialization checkpoint codes are listed in order of execution:

Checkpoint	Code Description
D0h	The NMI is disabled. Power on delay is starting. Next, the initialization code checksum will be verified.
D1h	Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh and entering 4 GB flat mode next.
D3h	Starting memory sizing next.
D4h	Returning to real mode. Executing any OEM patches and setting the Stack next.
D5h	Passing control to the uncompressed code in shadow RAM at E000:0000h. The initialization code is copied to segment 0 and control will be transferred to segment 0.
D6h	Control is in segment 0. Next, checking if <Ctrl> <Home> was pressed and verifying the system BIOS checksum. If either <Ctrl> <Home> was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.

B-2 Bootblock Recovery Codes

The bootblock recovery checkpoint codes are listed in order of execution:

Checkpoint	Code Description
E0h	The onboard floppy controller if available is initialized. Next, beginning the base 512 KB memory test.
E1h	Initializing the interrupt vector table next.
E2h	Initializing the DMA and Interrupt controllers next.
E6h	Enabling the floppy drive controller and Timer IRQs. Enabling internal cache memory.
Edh	Initializing the floppy drive.
Eeh	Looking for a floppy diskette in drive A:. Reading the first sector of the diskette.
Efh	A read error occurred while reading the floppy drive in drive A:.
F0h	Next, searching for the AMIBOOT.ROM file in the root directory.
F1h	The AMIBOOT.ROM file is not in the root directory.
F2h	Next, reading and analyzing the floppy diskette FAT to find the clusters occupied by the AMIBOOT.ROM file.
F3h	Next, reading the AMIBOOT.ROM file, cluster by cluster.
F4h	The AMIBOOT.ROM file is not the correct size.
F5h	Next, disabling internal cache memory.
FBh	Next, detecting the type of flash ROM.
FCh	Next, erasing the flash ROM.
FDh	Next, programming the flash ROM.
FFh	Flash ROM programming was successful. Next, restarting the system BIOS.

B-3 Uncompressed Initialization Codes

The following runtime checkpoint codes are listed in order of execution.

These codes are uncompressed in F0000h shadow RAM.

Checkpoint	Code Description
03h	The NMI is disabled. Next, checking for a soft reset or a power on condition.
05h	The BIOS stack has been built. Next, disabling cache memory.
06h	Uncompressing the POST code next.
07h	Next, initializing the CPU and the CPU data area.
08h	The CMOS checksum calculation is done next.
0Ah	The CMOS checksum calculation is done. Initializing the CMOS status register for date and time next.
0Bh	The CMOS status register is initialized. Next, performing any required initialization before the keyboard BAT command is issued.
0Ch	The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller.
0Eh	The keyboard controller BAT command result has been verified. Next, performing any necessary initialization after the keyboard controller BAT command test.
0Fh	The initialization after the keyboard controller BAT command test is done. The keyboard command byte is written next.
10h	The keyboard controller command byte is written. Next, issuing the Pin 23 and 24 blocking and unblocking command.
11h	Next, checking if <End> or <Ins> keys were pressed during power on. Initializing CMOS RAM if the Initialize CMOS RAM in every boot AMIBIOS POST option was set in AMIBCP or the <End> key was pressed.
12h	Next, disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2.
13h	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.
14h	The 8254 timer test will begin next.
19h	Next, programming the flash ROM.
1Ah	The memory refresh line is toggling. Checking the 15 second on/off time next.
2Bh	Passing control to the video ROM to perform any required configuration before the video ROM test.
2Ch	All necessary processing before passing control to the video ROM is done. Looking for the video ROM next and passing control to it.
2Dh	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control
23h	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24h	The configuration required before interrupt vector initialization has completed. Interrupt vector initialization is about to begin.
25h	Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.
27h	Any initialization before setting video mode will be done next.
28h	Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.

Checkpoint	Code Description
2Ah	Bus initialization system, static, output devices will be done next, if present. See the last page for additional information.
2Eh	Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2Fh	The EGA/VGA controller was not found. The display memory read/write test is about to begin.
30h	The display memory read/write test passed. Look for retrace checking next.
31h	The display memory read/write test or retrace checking failed. Performing the alternate display memory read/write test next.
32h	The alternate display memory read/write test passed. Looking for alternate display retrace checking next.
34h	Video display checking is over. Setting the display mode next.
37h	The display mode is set. Displaying the power on message next.
38h	Initializing the bus input, IPL, general devices next, if present. See the last page of this chapter for additional information.
39h	Displaying bus initialization error messages. See the last page of this chapter for additional information.
3Ah	The new cursor position has been read and saved. Displaying the Hit message next.
3Bh	The Hit message is displayed. The protected mode memory test is about to start.
40h	Preparing the descriptor tables next.
42h	The descriptor tables are prepared. Entering protected mode for the memory test next.
43h	Entered protected mode. Enabling interrupts for diagnostics mode next.
44h	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45h	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.
46h	The memory wraparound test is done. Memory size calculation has been done. Writing patterns to test memory next.
47h	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory next.
48h	Patterns written in base memory. Determining the amount of memory below 1 MB next.
49h	The amount of memory below 1 MB has been found and verified.
4Bh	The amount of memory above 1 MB has been found and verified. Checking for a soft reset and clearing the memory below 1 MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.
4Ch	The memory below 1 MB has been cleared via a soft reset. Clearing the memory above 1 MB next.
4Dh	The memory above 1 MB has been cleared via a soft reset. Saving the memory size next. Going to checkpoint 52h next.
4Eh	The memory test started, but not as the result of a soft reset. Displaying the first 64 KB memory size next.
4Fh	The memory size display has started. The display is updated during the memory test. Performing the sequential and random memory test next.
50h	The memory below 1 MB has been tested and initialized. Adjusting the displayed memory size for relocation and shadowing next.
51h	The memory size display was adjusted for relocation and shadowing.

Checkpoint	Code Description
52h	The memory above 1 MB has been tested and initialized. Saving the memory size information next.
53h	The memory size information and the CPU registers are saved. Entering real mode next.
54h	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57h	The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.
58h	The memory size was adjusted for relocation and shadowing. Clearing the Hit message next.
59h	The Hit message is cleared. The <WAIT...> message is displayed. Starting the DMA and interrupt controller test next.
60h	The DMA page register test passed. Performing the DMA Controller 1 base register test next.
62h	The DMA controller 1 base register test passed. Performing the DMA controller 2 base register test next.
65h	The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
66h	Completed programming DMA controllers 1 and 2. Initializing the 8259 interrupt controller next.
67h	Completed 8259 interrupt controller initialization.
7Fh	Extended NMI source enabling is in progress.
80h	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
81h	A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
82h	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83h	The command byte was written and global data initialization has completed. Checking for a locked key next.
84h	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85h	The memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next.
86h	The password was checked. Performing any required programming before WINBIOS Setup next.
87h	The programming before WINBIOS Setup has completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next.
88h	Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next.
89h	The programming after WINBIOS Setup has completed. Displaying the power on screen message next.
8Ch	Programming the WINBIOS Setup options next.
8Dh	The WINBIOS Setup options are programmed. Resetting the hard disk controller next.
8Fh	The hard disk controller has been reset. Configuring the floppy drive controller next.
91h	The floppy drive controller has been configured. Configuring the hard disk drive controller next.
95h	Initializing the bus option ROMs from C800 next. See the last page of this chapter for additional information.
96h	Initializing before passing control to the adaptor ROM at C800.

Checkpoint	Code Description
97h	Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next.
98h	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
99h	Any initialization required after the option ROM test has completed. Configuring the timer data area and printer base address next.
9Ah	Set the timer and printer base addresses. Setting the RS-232 base address next.
9Bh	Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next.
9Ch	Required initialization before the Coprocessor test is over. Initializing the Coprocessor next.
9Dh	Coprocessor initialized. Performing any required initialization after the Coprocessor test next.
9Eh	Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.
A2h	Displaying any soft errors next.
A3h	The soft error display has completed. Setting the keyboard typematic rate next.
A4h	The keyboard typematic rate is set. Programming the memory wait states next.
A5h	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7h	NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.
A8h	Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next.
A9h	Returned from adaptor ROM at E000h control. Performing any initialization required after the E000 option ROM had control next.
Aah	Initialization after E000 option ROM control has completed. Displaying the system configuration next.
Abh	Uncompressing the DMI data and executing DMI POST initialization next.
B0h	The system configuration is displayed.
B1h	Copying any code to specific areas.
00h	Code copying to specific areas is done. Passing control to INT 19h boot loader next.

NI 5792R

RF Receiver Adapter Module

The NI 5792 is an RF receiver adapter module designed to work in conjunction with your NI FlexRIO™ FPGA module. The NI 5792 features the following connectors and chips:

- 2-channel, 250 MS/s analog-to-digital converter (ADC) with 14-bit accuracy
- LO input and LO output connectors to support LO sharing for multiple-channel applications
- Timing chip with clocking options from the backplane and the front panel
- Programmable attenuators
- Selectable receive filters
- The following front panel connectors
 - RX IN
 - LO OUT
 - CLK IN
 - CLK OUT
 - LO IN

This document contains signal information and lists the specifications of the NI 5792R, which is composed of the NI FlexRIO FPGA module and the NI 5792. This document also contains tutorial sections that demonstrate how to acquire data using a LabVIEW FPGA Example VI and how to create and run your own LabVIEW project with the NI 5792R.



Note *NI 5792R* refers to the combination of your NI 5792 adapter module and your NI FlexRIO FPGA module. *NI 5792* refers to your NI 5792 adapter module only.



Note The NI 5792 is only compatible with the NI PXIe-796xR FPGA modules.



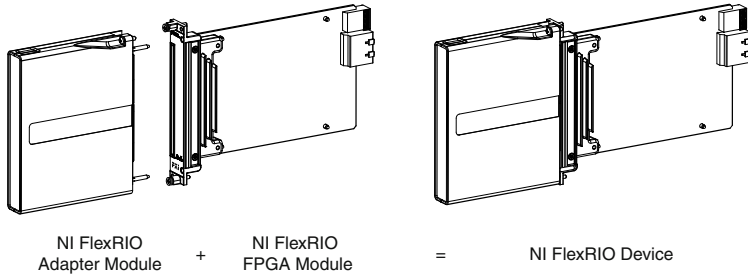
Note Before configuring your NI 5792R, you must install the appropriate software and hardware.



Note For EMC compliance, operate this device according to the documentation.

The following figure shows an example of a properly connected NI FlexRIO device.

Figure 1. NI FlexRIO Device



Related Information

[NI 5792 Specifications](#) on page 21

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Electromagnetic Compatibility Guidelines

This product was tested and complies with the regulatory requirements and limits for electromagnetic compatibility (EMC) stated in the product specifications. These requirements and limits are designed to provide reasonable protection against harmful interference when the product is operated in the intended operational electromagnetic environment.

This product is intended for use in industrial locations. However, harmful interference may occur in some installations, when the product is connected to a peripheral device or test object, or if the product is used in residential or commercial areas. To minimize interference with radio and television reception and prevent unacceptable performance degradation, install and use this product in strict accordance with the instructions in the product documentation.

Furthermore, any modifications to the product not expressly approved by National Instruments could void your authority to operate it under your local regulatory rules.



Caution To ensure the specified EMC performance, operate this product only with shielded cables and accessories.



Caution To ensure the specified EMC performance, the length of all I/O cables must be no longer than 3 m (10 ft).



Caution To ensure the specified EMC performance, you must install PXI EMC Filler Panels (National Instruments part number 778700-1) in adjacent chassis slots.

Related Information

[Installing PXI EMC Filler Panels](#) on page 34

Connecting Cables

1. Use any shielded 50 Ω SMA cable to connect signals to the connectors on the front panel of your device.
2. Use the SHH19-H19-AUX cable (NI part number: 152629-01 or 152629-02) to connect to the digital I/O (DIO) and programmable function interface (PFI) signals on the

AUX I/O connector. NI recommends using the SCB-19 connector block to access the DIO and PFI signals.

Related Information

[NI 5792 Specifications](#) on page 21

How to Use Your NI FlexRIO Documentation Set

Refer to Figure 2 and Table 1 to learn how to use your FlexRIO documentation set.

Figure 2. How to Use Your NI FlexRIO Documentation Set.

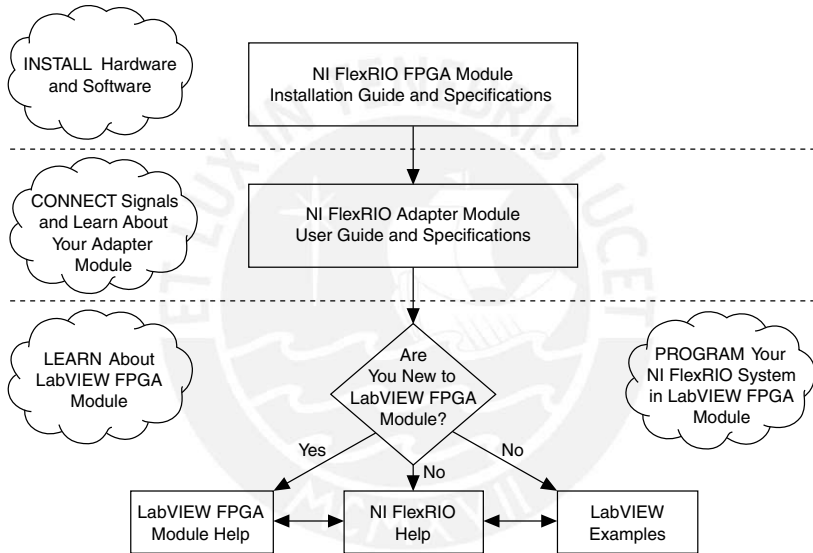


Table 1. NI FlexRIO Documentation Locations and Descriptions

Document	Location	Description
<i>NI FlexRIO FPGA Module Installation Guide and Specifications</i>	Available from the Start menu and at ni.com/manuals .	Contains installation instructions for your NI FlexRIO system and specifications for your FPGA module.
<i>NI 5792R User Manual and Specifications</i> (this document)	Available from the Start menu and at ni.com/manuals .	Contains signal information, examples, CLIP details, and specifications for your adapter module.

Table 1. NI FlexRIO Documentation Locations and Descriptions (Continued)

Document	Location	Description
<i>LabVIEW FPGA Module Help</i>	Embedded in <i>LabVIEW Help</i> and at ni.com/manuals .	Contains information about the basic functionality of the LabVIEW FPGA Module.
<i>NI FlexRIO Help</i>	Available from the Start menu and at ni.com/manuals .	Contains FPGA Module, adapter module, and CLIP configuration information.
LabVIEW Examples	Available in NI Example Finder.	Contains examples of how to run FPGA VIs and Host VIs on your device.
IPNet	ni.com/ipnet	Contains LabVIEW FPGA functions and intellectual property to share.
NI FlexRIO product page	ni.com/flexrio	Contains product information and data sheets for NI FlexRIO devices.

Key Features

The NI 5792 includes the following key features:

RF frequency range.....	200 MHz to 4.4 GHz
ADC.....	14-bit dual channel at 250 MS/s
Phase noise.....	<95 dBc/Hz, 10 kHz offset, 2.4 GHz carrier
Dynamic range.....	>106 dB
Receive (RX) IP ₃	-6 dBm at 2 GHz
Instantaneous bandwidth.....	200 MHz

Front Panel and Connector Pinouts

Table 2 shows the front panel connector and signal descriptions for the NI 5792.

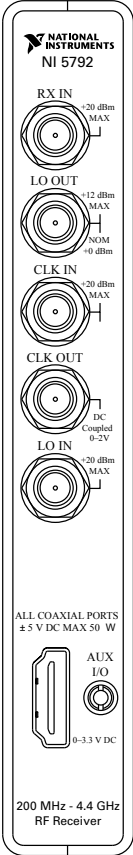


Caution To avoid permanent damage to the NI 5792, disconnect all signals connected to the NI 5792 before powering down the module, and connect signals only after the adapter module has been powered on by the NI FlexRIO FPGA module.



Caution Connections that exceed any of the maximum ratings of any connector on the NI 5792R can damage the device and the chassis. NI is not liable for any damage resulting from such connections.

Table 2. NI 5792 Front Panel Connectors

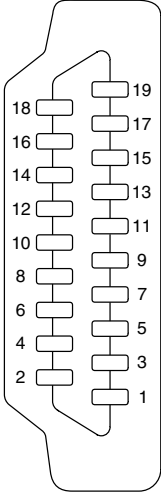
Device Front Panel	Connector	Signal Description
 <p>NATIONAL INSTRUMENTS NI 5792</p> <p>RX IN -20 dBm MAX</p> <p>LO OUT +12 dBm MAX NOM +0 dBm</p> <p>CLK IN -20 dBm MAX</p> <p>CLK OUT DC Coupled 0-2V</p> <p>LO IN -20 dBm MAX</p> <p>ALL COAXIAL PORTS ±5 V DC MAX 50 W</p> <p>AUX I/O 0-3.3 V DC</p> <p>200 MHz - 4.4 GHz RF Receiver</p>	RX IN	Receive channel input, +20 dBm maximum
	LO OUT	Local oscillator output, +12 dBm maximum, +0 dBm nominal
	CLK IN	Reference Clock input, 50 Ω single-ended, +20 dBm maximum
	CLK OUT	Exported clock output, DC-coupled, 0 V to 2 V
	LO IN	Local oscillator input, +20 dBm maximum
	AUX I/O	Refer to the table below for signal list and descriptions.

Related Information

[NI 5792 Specifications](#) on page 21

AUX I/O Connector

Table 3. NI 5792 AUX I/O Connector Pin Assignments

AUX I/O Connector	Pin	Signal	Signal Description
	1	DIO Port 0 (0)	Bidirectional single-ended (SE) digital I/O (DIO) data channel.
	2	GND	Ground reference for signals.
	3	DIO Port 0 (1)	Bidirectional SE DIO data channel.
	4	DIO Port 0 (2)	Bidirectional SE DIO data channel.
	5	GND	Ground reference for signals.
	6	DIO Port 0 (3)	Bidirectional SE DIO data channel.
	7	DIO Port 1 (0)	Bidirectional SE DIO data channel.
	8	GND	Ground reference for signals.
	9	DIO Port 1 (1)	Bidirectional SE DIO data channel.
	10	DIO Port 1 (2)	Bidirectional SE DIO data channel.
	11	GND	Ground reference for signals.
	12	DIO Port 1 (3)	Bidirectional SE DIO data channel.
	13	PFI 0	Bidirectional SE DIO data channel.
	14	NC	No connect.
	15	PFI 1	Bidirectional SE DIO data channel.
	16	PFI 2	Bidirectional SE DIO data channel.
	17	GND	Ground reference for signals.
	18	+5 V	+5 V power (10 mA maximum).
	19	PFI 3	Bidirectional SE DIO data channel.

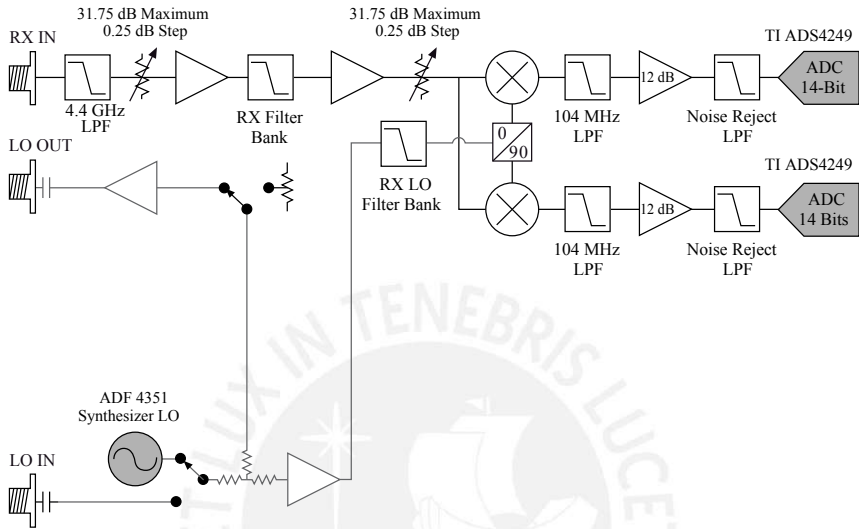


Caution The AUX I/O connector accepts a standard, third-party HDMI cable, but the AUX I/O port is not an HDMI interface. Do not connect the AUX I/O port on the NI 5792 to the HDMI port of another device. NI is not liable for any damage resulting from such signal connections.

Block Diagram

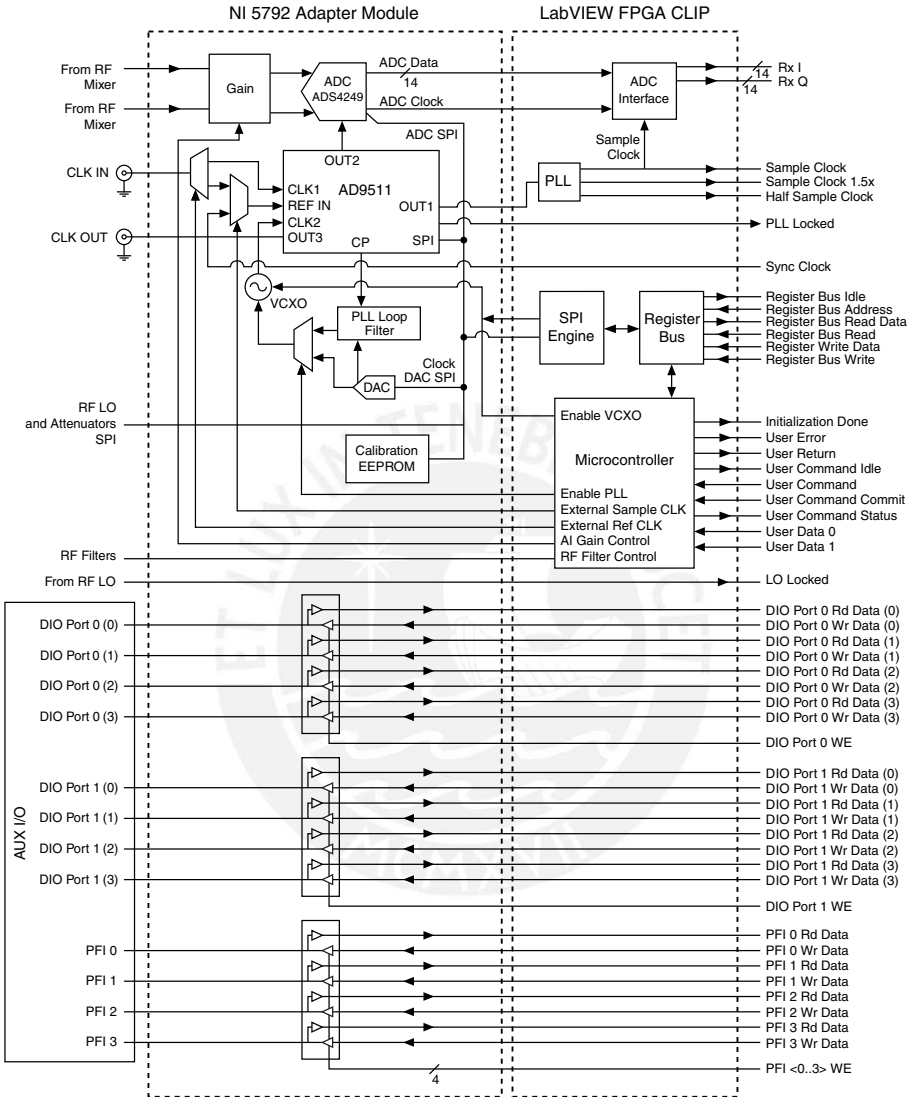
The following figure shows the NI 5792 block diagram.

Figure 3. NI 5792 Block Diagram



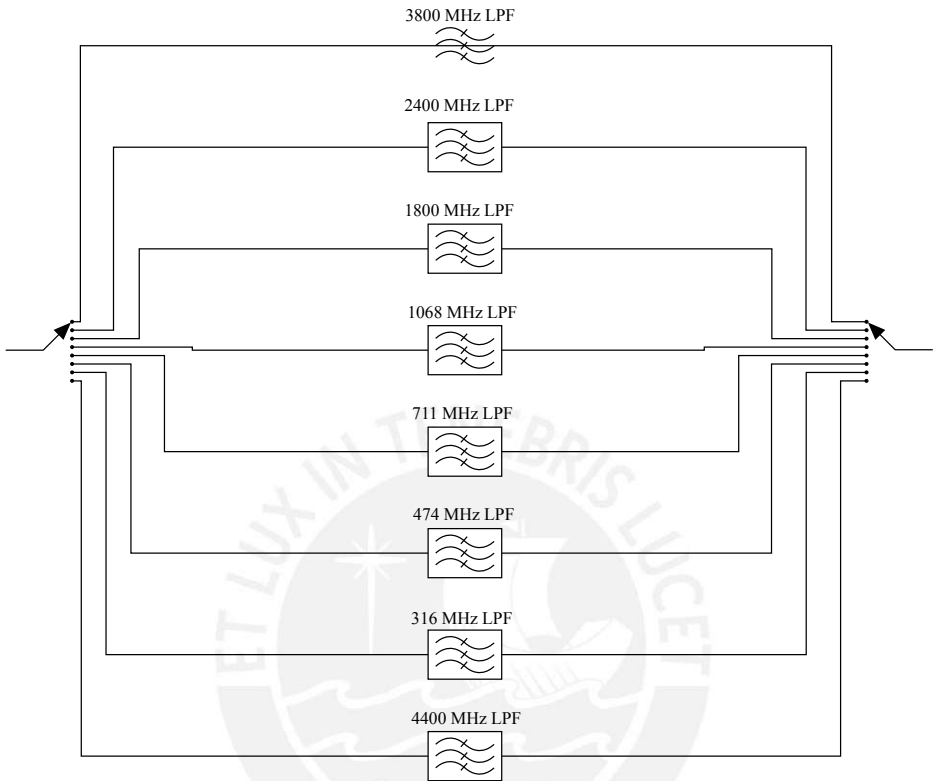
The following figure shows the connections between the NI 5792 and the LabVIEW FPGA CLIP.

Figure 4. NI 5792 Connector Signals and CLIP Signal Block Diagram



The following figure shows the NI 5792 low-pass filter bank.

Figure 5. Low pass Filter (LPF) Bank



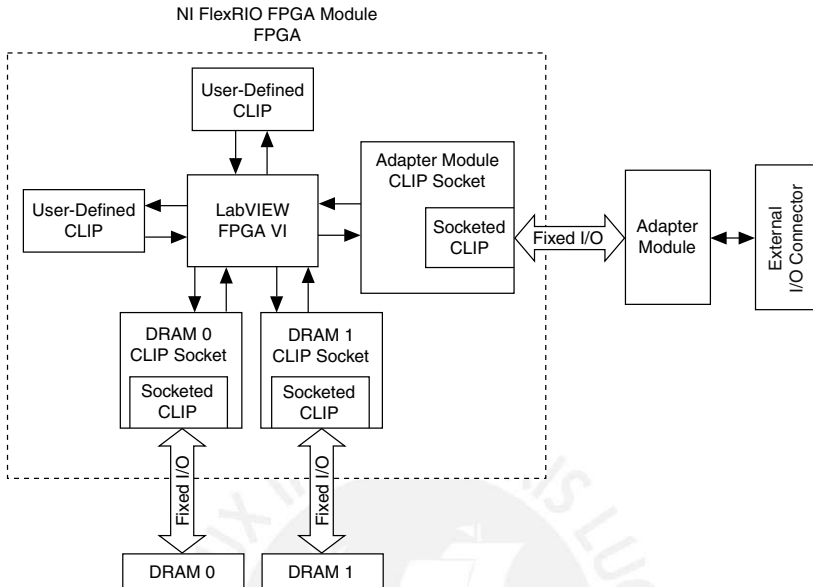
NI 5792 Component-Level Intellectual Property (CLIP)

The LabVIEW FPGA Module includes component-level intellectual property (CLIP) for HDL IP integration. NI FlexRIO devices support two types of CLIP: user-defined and socketed.

- *User-defined CLIP* allows you to insert HDL IP into an FPGA target, enabling VHDL code to communicate directly with an FPGA VI.
- *Socketed CLIP* provides the same IP integration of the user-defined CLIP, but also allows the CLIP to communicate directly with circuitry external to the FPGA. Adapter module socketed CLIP allows your IP to communicate directly with both the FPGA VI and the external adapter module connector interface.

The following figure shows the relationship between an FPGA VI and the CLIP.

Figure 6. CLIP and FPGA VI Relationship



The NI 5792 ships with socketed CLIP items that add module I/O to the LabVIEW project.

5792 CLIP

1. **NI 5792 CLIP**—This CLIP generates one sample per clock cycle at a default sample rate of 250 MHz. You can set a lower sample rate by using an external Sample Clock. This CLIP provides access to I and Q data for one RF receive channel. The CLIP also provides a User Command interface for common configurations of the base-band clocking, programmable attenuators, receive amplifier, receive filters, LO filters, and RF path which includes the ability to import and export the LO. The baseband clocking can be configured using one of the following settings:
 - Internal Sample Clock
 - Internal Sample Clock locked to an external Reference Clock through the CLK IN connector
 - External Sample Clock through the CLK IN connector
 - Internal Sample Clock locked to an external Reference Clock through the Sync Clock
2. **NI 5792 Multiple Sample CLIP**—This CLIP generates two samples per clock cycle at a clock rate that is half the sample rate. This CLIP provides access to I and Q data for one RF receive channel. The CLIP also provides a User Command interface for common configurations of the base-band clocking, programmable attenuators, receive amplifier,

receive filters, LO filters, and RF path which includes the ability to import and export the LO. The baseband clocking can be configured using one of the following settings:

- Internal Sample Clock
- Internal Sample Clock locked to an external Reference Clock through the CLK IN connector
- External Sample Clock through the CLK IN connector
- Internal Sample Clock locked to an external Reference Clock through the Sync Clock

This CLIP also contains a FAM Registers Bus interface, which is a low-level bus interface that directly programs registers on all programmable devices, such as the analog-to-digital converter (ADC). Programming registers on these devices allows for more advanced configuration.



Note You can configure the LO using the User Command interface. Use the FAM Registers Bus interface to program the LO synthesizer, then use the User Command interface to configure the LO filters.

Refer to the *NI FlexRIO Help* for more information about NI FlexRIO CLIP items, how to configure the NI 5792 with a socketed CLIP, and for a list of available socketed CLIP signals.

Programmable Chips

You can program the following chips from the CLIP.

Chip	Part Number
ADC	TI ADS4249
Clock Distribution	ADI AD9511
EEPROM	SST25VF080B
Programmable RF Attenuator	Peregrine PE43703

Using Your NI 5792R with a LabVIEW FPGA Example VI



Note You must install the software before running this example. Refer to the *NI FlexRIO FPGA Installation Guide and Specifications* for more information about installing your software.

The NI FlexRIO Adapter Module Support software includes an example project to help you get started creating your LabVIEW FPGA application. This section explains how to use an existing LabVIEW FPGA example project to acquire samples with the NI 5792R.

For more detailed information about acquiring data on your NI 5792R, refer to the streaming example available at <labview>\examples\instr\ni579x\Streaming.



Note The examples available for your device are dependent on the version of the software and driver you are using. For more information about which software versions are compatible with your device, visit ni.com/info, enter `rdsoftwareversion` in the text field, and click the NI FlexRIO link in the results.

The NI 5792R example project includes the following components:

- A LabVIEW FPGA VI that can be compiled and run on the FPGA embedded in the hardware
- At least one VI that runs on Windows and interacts with the LabVIEW FPGA VI



Note In the LabVIEW FPGA Module software, NI FlexRIO adapter modules are referred to as *IO Modules*.

Using the Included Streaming Example

Complete the following steps to run an example that acquires a waveform using the NI 5792.

1. Connect an antenna to the RX IN connector on the front panel of the NI 5792.
2. Launch LabVIEW.
3. Select **File»Open Project**.
4. Navigate to <labview>\examples\instr\ni579x\Streaming.
5. Select **Streaming.lvproj**.
6. In the **Project Explorer** window, select **Rx Streaming (Host).vi** under **My Computer** to open the host VI. The Open FPGA VI Reference function in this VI uses the NI 7966R as the FPGA target by default. If you are using an NI FlexRIO FPGA module other than the NI 7966R, complete the following steps to change to the FPGA VI to support your target.
 - a) Specify the center frequency in the **LO Frequency [Hz]** control.
 - b) On the block diagram, right-click the Open FPGA VI Reference (PXI-7966R) function and select **Configure Open FPGA VI Reference**.
 - c) In the **Configure Open FPGA VI Reference** dialog box, click the **Browse** button next to the **Bitfile** button.
 - d) In the **Select Bitfile** dialog box that opens, select the bitfile for your desired target. The bitfile name is based on the adapter module, example type, and FPGA module.
 - e) Click the **Select** button.
 - f) Click **OK** in the **Configure Open FPGA VI Reference** dialog box.
 - g) Save the VI.
7. On the front panel, in the **RIO Device** pull-down menu, select an NI 5792 resource that corresponds with the target configured in step 6.
8. Configure your measurement.
 - a) Specify the center frequency in the **LO Frequency [Hz]** control.
 - b) Specify the reference level in the **Reference Level [dBm]** control.
 - c) Specify the sample rate in the **Sample Rate [S/s]** control.
9. Click the **Run** button to run the VI.

10. The VI acquires data and displays the captured waveform on the **Power Level, Power Spectrum, and I & Q Data** graphs.
11. Click the **STOP** button to stop the VI.
12. Close the VI.

Creating a LabVIEW Project

This section explains how to set up your target and create an FPGA VI and host VI for data communication. This section focuses on proper project configuration, proper CLIP configuration, and how to access NI 5792 I/O nodes.

Creating a Project

1. Launch LabVIEW, or if LabVIEW is already running, select **File»Create Project**.
2. In the **Create Project** dialog box, select **LabVIEW FPGA Project** and click **Finish**.
3. Select **FlexRIO on My Computer** and click **Next**.
4. Either discover a LabVIEW FPGA target in your system or create a new system and specify an FPGA target for which to construct a project.
5. Click **Finish** in the **Project Preview** dialog box.
6. Click **File»Save** and specify a name for the project.

Creating an FPGA Target VI

1. In the **Project Explorer** window, expand **FPGA Target**.
2. Right-click **FPGA Target** and select **New»FPGA Base Clock**.
3. In the **Resource** pull-down menu, select **200 MHz Clock** and click **OK**.
4. Right-click **IO Module** in the **Project Explorer** window and select **Properties**.
5. Select **Enable IO Module**.
6. Select the NI 5792 from the **IO Module** list. The available CLIP for the NI 5792 is displayed in the **Component Level IP** pane.
7. Select NI 5792 or NI 5792 Multi Sample CLIP in the **Name** list of the **Component Level IP** pane.
8. In the **Clock Selections** category, select **200 MHz Clock** from the pull-down menu for **Clock 200 MHz**. Leave **Clock 40 MHz** configured as the **Top-Level Clock**.
9. Click **OK**.



Note Configuring these clocks is required for proper CLIP operation. Refer to the NI 5792 CLIP topics in the *NI FlexRIO Help* for more information about configuring your clocks.

10. Select **File»Open** and select `<labview>\instr.lib\ni579x\config\v1\FPGA\Public\ni579x Config FPGA Template.vi`.
11. Select **File»Save As**.
12. Select **Copy»Open Additional Copy** and check **Add Copy to <your project name>.lvproj**.
13. Select the destination folder for the new file, specify a file name, and click **OK**. Use this FPGA VI with the NI-579x Configuration Design Library.

14. In the **Project Explorer** window, expand **IO Module Tree View**. Use any element under **IO Module (NI 5792 : NI 5792)** in the block diagram of the FPGA VI.



Note If you are using the NI 5792 CLIP, use Rx I and Rx Q (from the CLIP IO Node) in a single-cycle Timed Loop running on IO Module\Sample Clock (the 250 MHz clock). This CLIP provides one sample per cycle at the 250 MHz rate.



Note If you are using the NI 5792 Multiple Sample CLIP, use Rx I N, Rx I N-1, Rx Q N, Rx Q N-1 (from the CLIP IO Node) in a single-cycle Timed Loop running on IO Module\Half Sample Clock (the 125 MHz clock). This CLIP provides two samples per cycle at the 125 MHz rate.



Note For either CLIP, if you are using the DSP Instrument Design Library, you must use the "2 samples per cycle, 2x overclocking" instances of the DSP VIs. Place these VIs in a single-cycle Timed Loop running on IO Module\Half Sample Clock, and wire IO Module\Sample Clock to the "clock x 2" terminals.

15. Add any FPGA code, controls, and indicators that you need. Refer to `Streaming.lvproj` for example FPGA code, controls, and indicators.
16. Click the **Run** button. LabVIEW creates a default build specification and begins compiling the VI. The **Generating Intermediate Files** window displays the code generation process. The **Compilation Status** window displays the progress of the compilation. The compilation takes several minutes.
17. Click **Close** in the **Compilation Status** window.
18. Save and close the VI.
19. Save the project.

Creating a Host VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New»VI** to open a blank VI.
2. Select **Window»Show Block Diagram** to open the VI block diagram.
3. Add the Open FPGA VI Reference function from the FPGA Interface palette to the block diagram.
4. Right-click the Open FPGA VI Reference function and select **Configure Open FPGA VI Reference**.
5. In the **Configure Open FPGA VI Reference** dialog box, select **VI** in the **Open** section.
6. In the **Select VI** dialog box, select your project under your device and click **OK**.
7. Click **OK** in the **Configure Open FPGA VI Reference** dialog box. The target name appears under the Open FPGA VI Reference function in the block diagram.
8. Open the FPGA Interface palette.
9. Add any Read/Write Control or Invoke Method nodes necessary to configure and communicate with your FPGA VI.
10. Add the Close FPGA VI Reference function to your block diagram.
11. Wire the FPGA VI Reference function to the Close FPGA VI Reference function.
12. Save and close the VI.

13. Save the project.

Run the Host VI

1. Open the front panel of your host VI.
2. Click the **Run** button to run the VI.

NI-579x Configuration Design Library

The NI-579x Configuration Design Library consists of host and FPGA VIs that provide an interface to configure the hardware on the NI 5792.

The library allows you to perform the following actions:

- Configure the mixers
- Configure the RF signal path, including attenuators, amplifiers, and filters
- Read from and write to the EEPROM
- Configure the reference level for the Rx channel.
- Configure the clocks
- Reinitialize the CLIP
- Query for CLIP errors

The NI-579x Configuration Design Library relies on the Register Bus Design Library. The Register Bus provides a packet-based configuration interface which exposes all of the address spaces of the configurable chips and subsystems of the adapter module, without requiring hundreds of controls and indicators on your FPGA VI front panel.

The NI-579x Configuration Design Library host VIs all require a register bus object for the device you want to configure. Create the register bus object using `Open Session.vi`, or use `ni579x Open.vi`.

For more information about how to use the NI-579x Configuration Design Library, refer to the example located at `<labview>\examples\instr\ni579x\Streaming\Streaming.lvproj`.

FPGA VI Requirements

Copy all the controls, indicators, and FPGA logic required to use the NI-579x Configuration Design Library from the following VI: `<labview>\instr.lib\ni579x\Config\v1\FPGA\Public\ni579x Config FPGA Template.vi`. The FAM Support installer installs this VI on your system.

Configure your FPGA target to contain a FIFO with the following configuration.

- Name: `reg.host instruction fifo 0`
- Type: Host to Target - DMA
- Requested number of elements: 1,023
- Data type: U64
- Arbitration for read: Arbitrate if multiple requestors only
- Number of elements per read: 1

Host VI Requirements

Configure your host VI to use the NI-579x Configuration Design Library using the following configuration:

1. Create a Register Bus object for your device and initialize the session using ni579x Open.vi.
2. Use any of the NI-579x Configuration Design Library Host VIs using the Register Bus object returned by the ni579x Open VI.
3. To access the Host VIs, select **Functions»Instrument I/O»Instrument Drivers»NI-579x Configuration**.
4. Close the session using the ni579x Close VI.

Synchronization Overview

Synchronization coordinates Sample Clock cycles across multiple NI FlexRIO devices.

Sources of error, such as common clock propagation delay, cabling and cable lengths, analog delays in the FPGA module and/or adapter module, and skew/jitter in the common clock, can affect frequency and phase relationships between devices.

Use the programming example to synchronize across multiple NI FlexRIO adapter modules.

Synchronization aligns the devices so that the devices are synchronized to the nearest Sample Clock cycle. The devices may be offset by up to one half of one Sample Clock cycle, if the devices are ± 180 degrees out of phase. If the devices are zero degrees out of phase, device alignment offset is also zero degrees.



Note For the best synchronization results, minimize the phase offset between devices.



Caution Before attempting to synchronize your NI FlexRIO devices, notice the following caveats:

- Synchronization does not account for differences in analog signal paths.
- Synchronization does not account for data pipeline delays that occur before and after the synchronization VIs. For example, synchronization does not account for ADC/DAC pipeline delays.
- The synchronized edge is always delayed relative to the unsynchronized edge. The application is responsible for accounting for this delay, if necessary. The synchronization VIs provide the actual synchronization delay value.
- Lock all devices to a common time reference. Use the Reference Clock as the time reference.
- Set the synchronization registers for the Reference Clock to zero.
- Synchronization does not account for propagation delays of the Reference Clock.
- All Sample Clocks must have a fixed phase relationship with each other.
- The Common Periodic Time Reference (CPTR) period must be greater than the maximum propagation delay of a signal from the master device to any slave device across the selected FPGA I/O line.

- The CPTR period must be the same across all devices. Devices can have different Sample Clock frequencies if the device Sample Clocks have a fixed phase relationship.
- Route the FPGA I/O lines to all the devices that you are synchronizing.

Synchronization Versions

The synchronization library provides two alignment methods depending on user needs: FPGA self-synchronization and host-driven synchronization. Both synchronization methods produce the same quality of synchronization, but differ in their requirements and versatility of operation.

FPGA Self-Synchronization

FPGA self-synchronization does not require host involvement. Using the host VIs is optional. The FPGAs can all independently align their CPTRs. To perform a self-synchronization, your devices must meet the following requirements:

- Sample Clocks are locked to the same Reference Clock.
- Sample Clocks are an integer multiple of the Reference Clock.
- All the devices are fewer than 60 degrees out-of-phase with each other.



Note FPGA self-synchronization is repeatable only if the devices meet all the requirements. If the devices do not meet the requirements, use host-driven synchronization.

Host-Driven Synchronization

Host-driven synchronization allows you to perform the following actions:

- Decouple the Sample Clock and the Reference Clock
- Use an external Sample Clock
- Set the CPTR period manually

Host-driven synchronization requires an additional FPGA I/O line and host involvement for CPTR alignment.



Note Host-driven synchronization is repeatable only if the phase relationships between devices remain constant.

Host-driven synchronization guarantees that the maximum phase offset between the master and slave device is one-half of a Sample Clock period. The phase offset approaches zero as the phase relationships between the devices approach zero.



Note The phase relationship between the device and the Reference Clock does not affect host-driven synchronization.

Synchronization Example

You can find examples of both FPGA code and host code for synchronization at `<labview>\examples\instr\ni579x\Streaming`.

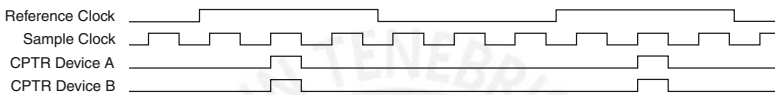
How Synchronization Works

When you share triggers between multiple devices, propagation delays on the signal path cause the trigger to arrive at different times on each device. The synchronization library uses the CPTR to slow down the trigger evaluation rate. All devices must produce a CPTR signal that is equal in frequency and phase-aligned.

The synchronization FPGA VIs produce and align a CPTR that occurs simultaneously across all the FPGAs. The CPTR is periodic, and the Sample Clock rate controls the CPTR period.

When you power on the FPGAs, the CPTRs are not aligned. The alignment FPGA VI and the host VI align the CPTRs. The following figure shows the relationship between the CPTRs, the Reference Clock, and the Sample Clock.

Figure 7. CPTR Alignment



Note Lock Device A and Device B to a common clock.

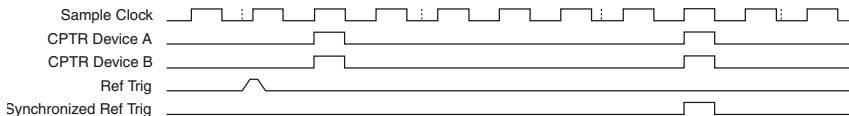
Once the CPTRs are aligned, synchronize an edge across multiple FPGAs. The master device distributes the signal across an FPGA I/O line. All devices monitor the same FPGA I/O line. The edge is synchronized at the next CPTR edge. After all the device CPTRs are aligned, an edge sent out on the FPGA I/O lines is read at the same clock cycle across all the devices.



Note The quality of synchronization is only as good as the quality of Sample Clock locking. Some static skew may exist. You can calibrate to eliminate this skew if necessary.

The following figure shows the relationship between the time that the master device reads a Reference Trigger (*Ref Trig*) and the time that all the devices read the synchronized version of the Reference Trigger (*Synchronized Ref Trig*). This synchronization requires CPTR alignment on all the devices.

Figure 8. Reading the Reference Triggers



Synchronization Checklist

Verify that the project settings in the system, the project, the host VI, and the FPGA VI are configured as follows.

- System settings:
 - Route the FPGA I/O lines to all the devices.
 - Depending on your chassis size, you may have to route PXI trigger lines using Measurement & Automation Explorer (MAX). Refer to the *Measurement & Automation Explorer (MAX) Help* at ni.com/manuals for more information about routing PXI trigger lines with MAX.
- Project settings:
 - Configure the adapter module IoModSyncClock (either PXI_CLK10 or DStarA) if you are not driving the adapter module CLK IN connector.
 - Add the FPGA Reference Clock.
 - Configure the Reference Clock to have zero synchronization registers. In the **FPGA IO Property** dialog box, set **Number of Synchronization Registers for Read** to 0.
 - Add the FPGA I/O lines that you are synchronizing. Do not remove synchronization registers.
- Host VI:
 - Configure the adapter module clock source based on the project settings.
 - Lock the adapter module clock to the clock source.
 - Run the Synchronization VI.
 - Refer to the example FPGA code at `<labviewdir>\examples\instr\ni579x\Streaming.`
- FPGA VI:
 - Configure the CPTR period. The synchronization library ensures that the CPTR period is the same on the host and the FPGA.
 - Refer to the example FPGA code at `<labviewdir>\examples\instr\ni579x\Streaming.`

Clocking

The NI 5792 clock source controls the sample rate and other timing functions on the device. The following table contains information about the possible NI 5792 clock sources.

Table 4. NI 5792R Clock Sources

Clock	Frequency	Source Options
Sample Clock	250 MHz	<ul style="list-style-type: none"> Free-running and internally sourced External through the CLK IN front panel connector
Reference Clock	10 MHz	<ul style="list-style-type: none"> Free-running and internally sourced External through the CLK IN front panel connector Sourced through PXI-CLK

579x Sample Projects

The NI 5792 software contains sample projects that are a starting point for application development. The projects are available in LabVIEW under **Create Project»Sample Projects»NI-579X**.

NI 5792 Specifications

Specifications are warranted by design and under the following conditions unless otherwise noted:

- Chassis fan speed is set to High. In addition, NI recommends using slot blockers and EMC filler panels in empty module slots to minimize temperature drift.
- The NI 5792 uses NI LabVIEW and LabVIEW FPGA software.

Specifications describe the warranted product performance over ambient temperature ranges of 0 °C to 55 °C, unless otherwise noted.

Typical values describe useful product performance beyond specifications that are not covered by warranty and do not include guardbands for measurement uncertainty or drift. Typical values may not be verified on all units shipped from the factory. Unless otherwise noted, typical values cover the expected performance of units over ambient temperature ranges of 23 °C ± 5 °C with a 90% confidence level, based on measurements taken during development or production.

Nominal values (or supplemental information) describe additional information about the product that may be useful, including expected performance that is not covered under *Specifications* or *Typical* values. Nominal values are not covered by warranty.

Related Information

[Front Panel and Connector Pinouts](#) on page 5

[Connecting Cables](#) on page 3

[NI 5792 User Manual and Specifications](#) on page 1

RX IN

RX IN Amplitude Range



RX input attenuation.....0 dB to 63.5 dB in 0.25 dB steps

Absolute Amplitude Accuracy



Note All values are typical.

Table 5. Absolute Amplitude Accuracy

Center Frequency	Absolute Amplitude Accuracy, Temperature 23 °C ± 5 °C (dB)
>200 MHz to 1 GHz	0.55
>1 GHz to 2 GHz	0.55
>2 GHz to 3 GHz	0.65
>3 GHz to 3.9 GHz	1.3
>3.9 GHz to 4.4 GHz	1.6
 Note Absolute amplitude accuracy uses a correction coefficient in EEPROM to improve performance. Performance is verified over the first 45 dB of RX attenuation.	
 Note Correction coefficients in EEPROM are valid only when the baseband amplifier is in the signal path.	

RX IN Average Noise Floor



Note All values are typical.

Table 6. Average Noise Floor

Center Frequency	Average Noise Level (dBm/Hz)
	Temperature 23 °C ±5 °C
>200 MHz to 1 GHz	-165
>1 GHz to 2 GHz	-165
>2 GHz to 3 GHz	-164

Table 6. Average Noise Floor (Continued)

Center Frequency	Average Noise Level (dBm/Hz)
	Temperature 23 °C ±5 °C
>3 GHz to 3.9 GHz	-160
>4 GHz to 4.4 GHz	-151


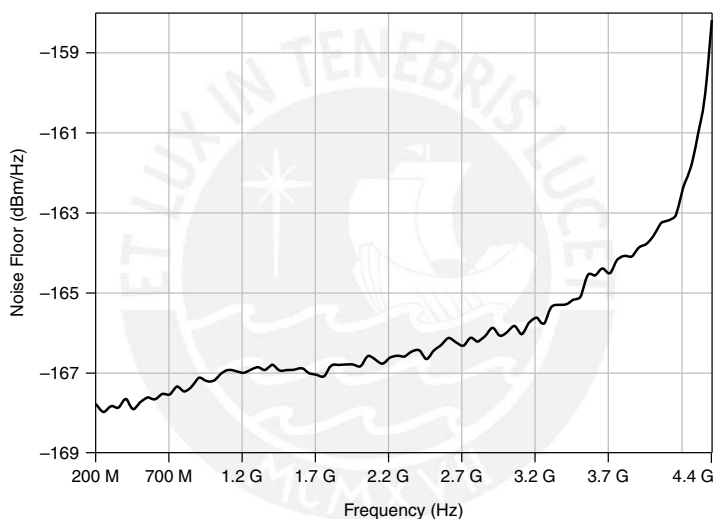

 **Note** Performance is measured with 0 dB of RX attenuation.

Figure 9. Average Noise Floor



Voltage Standing Wave Ratio (VSWR)

 **Note** All values are nominal.

Input impedance.....50 Ω

Input VSWR with 10 dB of RX attenuation

2.0 GHz.....1.5:1

2.0 GHz <math>f < 3\text{ GHz}</math>.....1.1:1

>3 GHz.....1.9:1

Spurious Responses



Note All responses are typical.

Non-input related residual spurs

<3.0 GHz.....	-101 dBm
3.0 to 3.9 GHz.....	-100 dBm
<4.4 GHz.....	-91 dBm



Note Performance is measured with 0 dB of RX attenuation and a 1.5 kHz resolution bandwidth (RBW).


RX LO Residual Power



Note All values are nominal.

Table 7. Residual Power

Center Frequency	Temperature 23 °C ± 5 °C (dBFS)
>200 MHz to 300 MHz	-30
>300 MHz to 1 GHz	-42
>1 GHz to 2 GHz	-52
>2 GHz to 3 GHz	-52
>3 GHz to 3.9 GHz	-52
>3.9 GHz to 4.4 GHz	-52

 **Note** Receiver LO suppression is measured at the same RX attenuation after an I/Q correction.

RX Sideband Image Suppression




Note All values are nominal.

Table 8. Sideband Image Suppression

Center Frequency	Temperature 23 °C ± 5 °C (dBc)
>200 MHz to 300 MHz	-27
>300 MHz to 1 GHz	-39

Table 8. Sideband Image Suppression (Continued)

Center Frequency	Temperature 23 °C ± 5 °C (dBc)
>1 GHz to 2 GHz	-58
>2 GHz to 3 GHz	-54
>3 GHz to 3.9 GHz	-45
>3.9 GHz to 4.4 GHz	-35

 **Note** The image suppression specifications hold at the center frequency of the acquired instantaneous bandwidth after the device performs a single recent point I/Q impairment self-correction.

RX Third-Order Intermodulation Distortion (IP₃)



 **Note** All values are nominal.

Table 9. RX IP₃

Frequency	Temperature 23 °C ± 5 °C (dBm)
>200 MHz to 1 GHz	-9
>1 GHz to 2 GHz	-7
>2 GHz to 3 GHz	-6
>3 to 3.9 GHz	-4
>3.9 GHz to 4.4 GHz	-1

 **Note** Values are based on two input tones spaced 1 MHz apart such that the tones are 6 db less than full-scale with 0 dB of RX attenuation.

Gain Compression



 **Note** All values are nominal.

Table 10. Gain Compression

Frequency	Temperature 23 °C ± 5 °C (dBm)
>200 MHz to 1 GHz	-20
>1 GHz to 2 GHz	-18

Table 10. Gain Compression (Continued)

Frequency	Temperature 23 °C ± 5 °C (dBm)
>2 GHz to 3.9 GHz	-15
>3.9 GHz to 4.4 GHz	-12

 **Note** Values are based on two input tones spaced 250 MHz apart, with 0 dB of RX attenuation and with one tone placed out of band.

Dynamic Range


 **Note** All values are nominal.

Table 11. Dynamic Range at 900 MHz

Reference Level (dBm)	IP ₃ (dBm)	Noise Floor (dBm/Hz)	Dynamic Range (dB)
-5	25	-138	109
-15	15	-148	109
-25	5	-158	109
-35	-4	-167	109



 **Note** The signal level of each tone is set to 6 dB less than the reference level to prevent overload. Dynamic range = $2/3 \times (IP_3 - \text{Noise Floor})$

Table 12. Dynamic Range at 2,400 MHz

Reference Level (dBm)	IP ₃ (dBm)	Noise Floor (dBm/Hz)	Dynamic Range (dB)
-5	21	-142	109
-15	12	-151	109
-25	2	-161	109
-35	-3	-166	109

 **Note** The signal level of each tone is set to 6 dB less than the reference level to prevent overload. Dynamic range = $2/3 \times (IP_3 - \text{Noise Floor})$

RX IN Frequency Characteristics

- Frequency range.....200 MHz to 4.4 GHz
- Instantaneous bandwidth (6 dB).....200 MHz
- Tuning resolution¹.....<250 kHz
- LO step size²
 - Integer mode.....4 MHz, 6 MHz, 12 MHz, and 24 MHz step sizes
 - Fractional mode.....100 kHz step size

Frequency Settling Time

- Settling time³.....< 50 ms per 100 MHz step

Phase Noise



Note All values are nominal.

Table 13. Phase Noise at 2.4 GHz

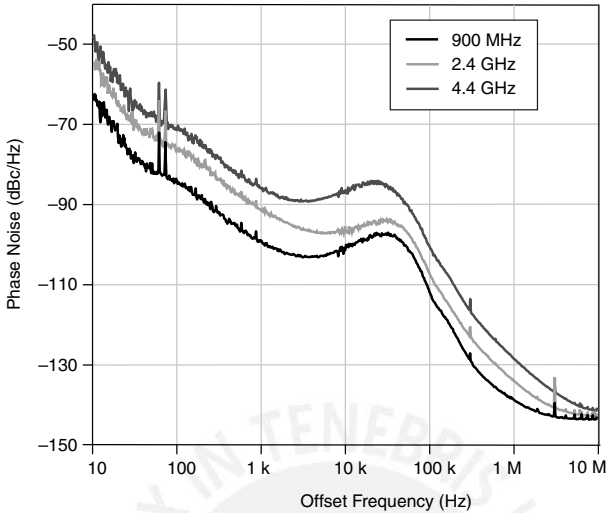
Offset Frequency	Loop Phase Noise (dBc/Hz)
1 kHz	-85
10 kHz	-95
100 kHz	-97
1 MHz	-100
10 MHz	-110

¹ Tuning resolution combines LO step size capability and frequency shift DSP implemented on the FPGA.

² All LO step size specifications are assumed to be with fractional mode enabled and 100 kHz LO step size.

³ The settling time specification only includes frequency settling, and it excludes any residual amplitude settling that may occur as a result of large frequency changes. Driver and operating system timing can affect transition times. This specification reflects only hardware settling.

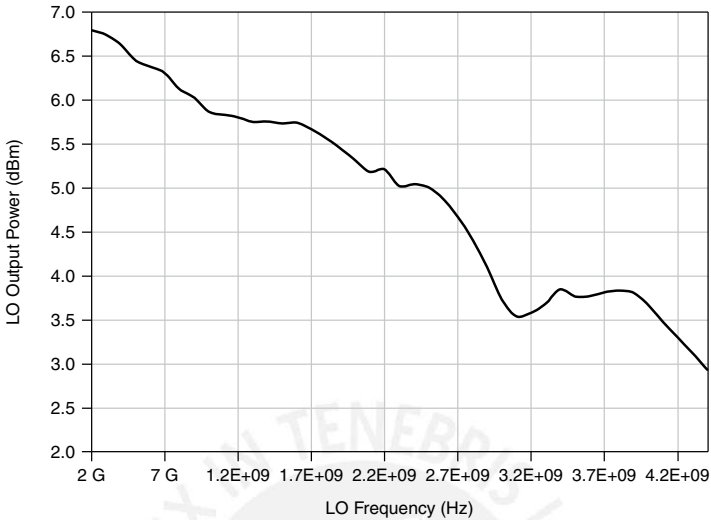
Figure 10. Phase Noise



LO OUT Front Panel Connector

Frequency range.....	200 MHz to 4.4 GHz
Power.....	3 dBm, ± 3 dB, nominal
Output power resolution.....	0.15 dB
Output impedance.....	50 Ω , nominal
Output VSWR.....	1.78:1
Amplitude settling time.....	< 0.25 dB in less than 10 ms, typical
Maximum DC voltage.....	± 0.5 V _{DC}

Figure 11. LO Output Power vs. LO Frequency



LO IN Front Panel Connector

Frequency range.....	200 MHz to 4.4 GHz
Input power.....	3 dBm \pm 3 dB, nominal
Input impedance.....	50 Ω
Input VSWR.....	1.78:1
Absolute maximum power.....	+15 dBm
Maximum DC power.....	\pm 0.5 V _{DC}

Baseband Characteristics

Analog-to-Digital Converters (ADC)⁴

Resolution.....	14 bits
Data rate.....	250 MS/s
I/Q data rate.....	1.84 kS/s to 250 MS/s ⁵

⁴ ADCs are dual-channel components with each channel assigned to I and Q, respectively.

⁵ The NI 5792 decimates the data rate using Fractional Decimation DSP blocks implemented in the LabVIEW FPGA target.

CLK IN Front Panel Connector

Frequency

Reference Clock.....	10 MHz
Sample Clock.....	250 MHz

Amplitude

Square.....	0.7 V _{pk-pk} to 5.0 V _{pk-pk} into 50 Ω, typical
Sine.....	1.4 V _{pk-pk} to 5.0 V _{pk-pk} (1 V _{RMS} to 3.5 V _{RMS}) into 50 Ω, typical

Input impedance.....50 Ω, nominal

Coupling.....AC

CLK OUT Front Panel Connector

Interface standard.....3.3 V LVCMOS

Interface logic

Maximum V _{OL}	0.55 V
Minimum V _{OH}	2.7 V
Maximum V _{OH}	3.6 V
Output impedance.....	50 Ω ±20%
Coupling.....	DC
I _{out} (DC).....	±32 mA

Dimensions and Weight

Dimensions.....12.9 × 2.0 × 12.1 cm (5.1 × 0.8 × 4.7 in)

Weight.....413 g (14.6 oz)

I/O.....RX IN, LO OUT, LO IN, CLK IN, CLK OUT

Power.....6 W

AUX I/O (Port 0 DIO <0..3>, Port 1 DIO <0..3>, and PFI <0..3>)

Number of channels.....12 bidirectional (8 DIO and 4 PFI)

Connector type.....HDMI

Interface standard.....3.3 V LVCMOS

Interface logic

Maximum V_{IL}	0.8 V
Minimum V_{IH}	2.0 V
Maximum V_{OL}	0.4 V
Minimum V_{OH}	2.7 V
Maximum V_{OH}	3.6 V
Z_{out}	$50 \Omega \pm 20\%$
I_{out} (DC).....	± 2 mA
Pull-down resistor.....	150 k Ω
Recommended operating voltage.....	-0.3 V to 3.6 V
Overvoltage protection.....	± 10 V
Maximum toggle frequency.....	6.6 MHz
+5 V maximum power.....	10 mA
+5 V voltage tolerance.....	4.2 V to 5 V

Environment

Maximum altitude.....	2,000 m (at 25 °C ambient temperature)
Pollution Degree.....	2
Indoor use only.	

Operating Environment

Ambient temperature range.....	0 °C to 55 °C (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.)
Relative humidity range.....	10% to 90%, noncondensing (Tested in accordance with IEC-60068-2-56.)

Storage Environment

Ambient temperature range.....	-40 °C to 70 °C (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.)
Relative humidity range.....	5% to 95%, noncondensing (Tested in accordance with IEC-60068-2-56.)
Operational shock.....	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)
Random vibration	
Operating.....	5 Hz to 500 Hz, 0.3 g _{rms}
Nonoperating.....	5 Hz to 500 Hz, 2.4 g _{rms} (Tested in accordance with IEC-60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Compliance and Certifications

Safety

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1



Note For UL and other safety certifications, refer to the product label or the [Online Product Certification](#) section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions



Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe,

Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.



Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.



Note For EMC declarations, certifications, and additional information, refer to the *Online Product Certification* section.

CE Compliance

This product meets the essential requirements of applicable European Directives, as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

To obtain product certifications and the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial not only to the environment but also to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)



EU Customers At the end of the product life cycle, all products must be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste Electrical and Electronic Equipment, visit ni.com/environment/weee.htm.

电子信息产品污染控制管理办法（中国 RoHS）



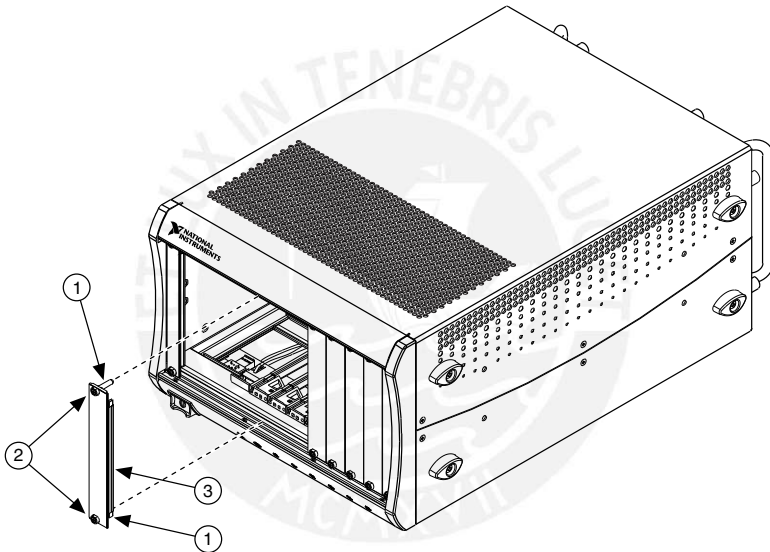
中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

Installing PXI EMC Filler Panels

To ensure specified EMC performance, PXI EMC filler panels must be properly installed in your NI FlexRIO system. The PXI EMC filler panels (National Instruments part number 778700-01) must be purchased separately. For more installation information, refer to the *NI FlexRIO FPGA Module Installation Guide and Specifications*.

1. Remove the captive screw covers.
2. Install the PXI EMC filler panels by securing the captive mounting screws to the chassis, as shown in the figure below. Make sure that the EMC gasket is on the right side of the PXI EMC filler panel.

Figure 12. PXI EMC Filler Panels and Chassis



1. Captive Screw Covers
2. Captive Mounting Screws
3. EMC Gasket



Note You must populate all slots with a module or a PXI EMC filler panel to ensure proper module cooling. Do not over tighten screws (2.5 lb · in maximum). For additional information about the use of PXI EMC filler panels in your PXI system, visit ni.com/info and enter `emcpanels`.

Related Information

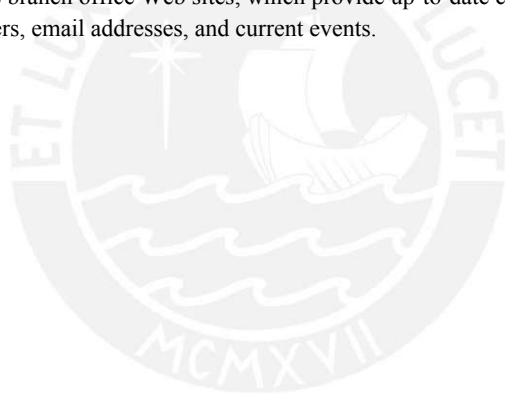
[Electromagnetic Compatibility Guidelines](#) on page 3

Where to Go for Support

The National Instruments Web site is your complete resource for technical support. At ni.com/support you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from NI Application Engineers.

A Declaration of Conformity (DoC) is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting ni.com/certification. If your product supports calibration, you can obtain the calibration certificate for your product at ni.com/calibration.

National Instruments corporate headquarters is located at 11500 North Mopac Expressway, Austin, Texas, 78759-3504. National Instruments also has offices located around the world to help address your support needs. For telephone support in the United States, create your service request at ni.com/support and follow the calling instructions or dial 512 795 8248. For telephone support outside the United States, visit the Worldwide Offices section of ni.com/niglobal to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.





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Ordering Information

For user manuals and dimensional drawings, visit the product page resources tab on ni.com.

Last Revised: 2014-11-06 07:15:06.0

NI HDD-8266

24-Drive, Up to 24 TB RAID Enclosure



- 5.7 TB SSD: 3.6 GB/s sustained read and write speeds for entire storage capacity in RAID-0
- 3.5 TB SAS: 3.6 GB/s sustained read and write speeds for 90 percent of total storage capacity in RAID-0
- 24 TB SATA: 1.6 GB/s sustained read and write speeds for 85 percent of total storage capacity in RAID-0
- 50g non-operational shock and 2.46g non-operational vibration (SSD variant)
- 25g operational shock and 0.31g operational vibration (SSD variant)
- Supports RAID-0/1/10/5/6 modes
- Features programmatic control and monitoring of hard drive and RAID partitions
- Supports hot swap of hard drives and offers endless record mode
- Windows 7 Only

Overview

The NI HDD-8266 external hard-drive redundant array of inexpensive disks (RAID) enclosure expands NI high-speed streaming solutions by offering higher data streaming rates and storage capacities. It includes a hardware RAID controller and a set of 24 either 1 TB SATA hard drives for a total capacity of 24 TB or 146 GB SAS hard drives for a total capacity of 3.5 TB or 240 GB SSD hard drives for a total capacity of 5.7 TB. For maximum streaming bandwidth, you should interface the HDD-8266 to the NI PXIe-1085 chassis via an NI PXIe-8384 PCI Express x8 Gen 2 module in a peripheral slot and a x8 cabled PCI Express cable.

The HDD-8266 offers up to 2.6 GB/s read and write speed for the SATA drive option and up to 3.6 GB/s read and write speed for the SAS and SSD drive option.

The SSD version offers excellent shock and vibration protection that makes the RAID suitable for rugged applications.

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Comparison Tables

Product Name	Total RAID-0 Storage Capacity	RAID-0 Sustained Read/Write Rates	RAID-5 Sustained Read/Write Rates	Supported RAID Modes	Programmatic Control and Monitoring
NI HDD-8266 SATA	24 TB	1.6 GB/s	1.6 GB/s	RAID-0/1/10/5/6	Yes
NI HDD-8266 SAS	3.5 TB	3.6 GB/s	3.6 GB/s	RAID-0/1/10/5/6	Yes
NI HDD-8266 SSD	5.7 TB	3.6 GB/s	3.6 GB/s	RAID-0/1/10/5/6	Yes

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Application and Technology

Hardware

The PXI Express data streaming system based on an HDD-8266 consists of an NI PXIe-8384 module in a PXI Express peripheral slot of a PXI Express chassis cabled, via a PCI Express x8 Gen 2 cable, to the HDD-8266 external hard-drive enclosure. The external enclosure includes a hardware RAID controller and a set of 24 drives. RAID-0 configuration,

or striping without parity, provides the highest performance for streaming data to and from disk because it distributes data evenly across a set of hard drives. RAID-5 configuration, or striping with parity, offers protection against the failure of a single drive by storing parity information related to the data. The process of calculating the data parity and storing it on the disks reduces the data streaming rates in the RAID-5 configuration as compared to the RAID-0 configuration. To learn more about the different RAID configurations, refer to the white paper "[Understanding RAID](#)."

Theory of Operation

After installing the provided driver software, you can configure the HDD-8266 hard drives in various RAID configurations and volumes either during system boot or using the RAID GUI. When configured as a GPT disk in Windows 7, the entire capacity appears as a single logical partition. You can then access them as standard hard drives in Windows and programmatically access them using standard file I/O APIs in development environments.

Aggregate Multiple HDD-8266 Enclosures for Higher Data Rates and Storage Capacity

In a high-performance PXI Express chassis such as the NI PXIe-1085, you can increase the total stream to/from disk rates by using multiple HDD-8266 RAID enclosures. For example, in a single NI PXIe-1085 chassis with an NI PXIe-8135 embedded controller, you can interface two HDD-8266 enclosures to achieve a total stream to/from data rate of 7.2 GB/s.

You can adopt the same approach of using multiple HDD-8266 enclosures in a chassis to increase the total storage space.

Programmatic Control and Monitoring of Hard Drives and RAID Partitions

NI provides an NI LabVIEW instrument driver for the HDD-8266 that allows programmatic control and monitoring of the hard drives and RAID partitions. Using this feature, you can not only monitor the status and health of the HDD-8266 but also create, modify, and delete RAID partitions. This feature helps you build more flexible high-speed record and playback systems.

Support for Hot Swapping Hard Drives

The HDD-8266 supports the hot swapping of hard drives. In the event of a hard-drive failure, you can use this feature to replace the failed hard drive instead of powering down the entire system.

Endless Record Mode

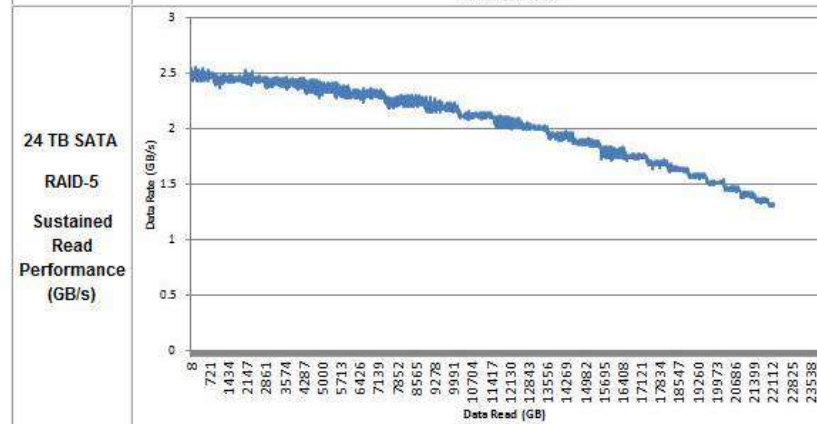
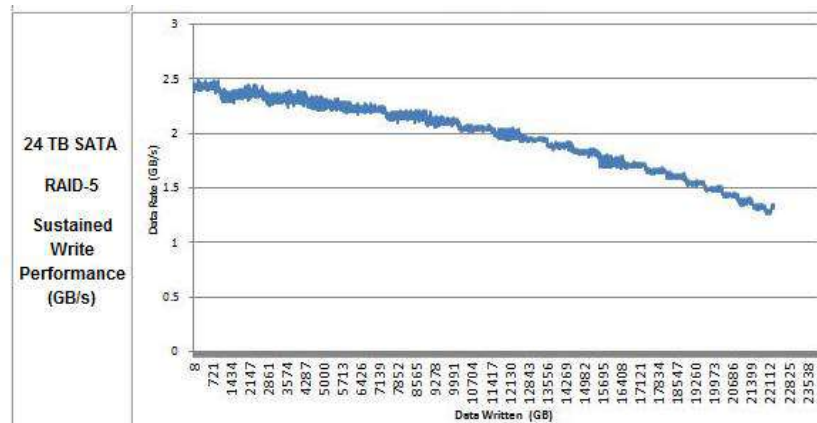
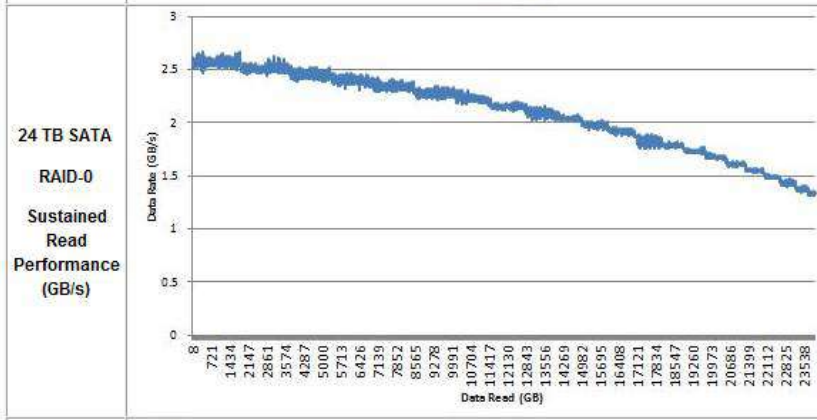
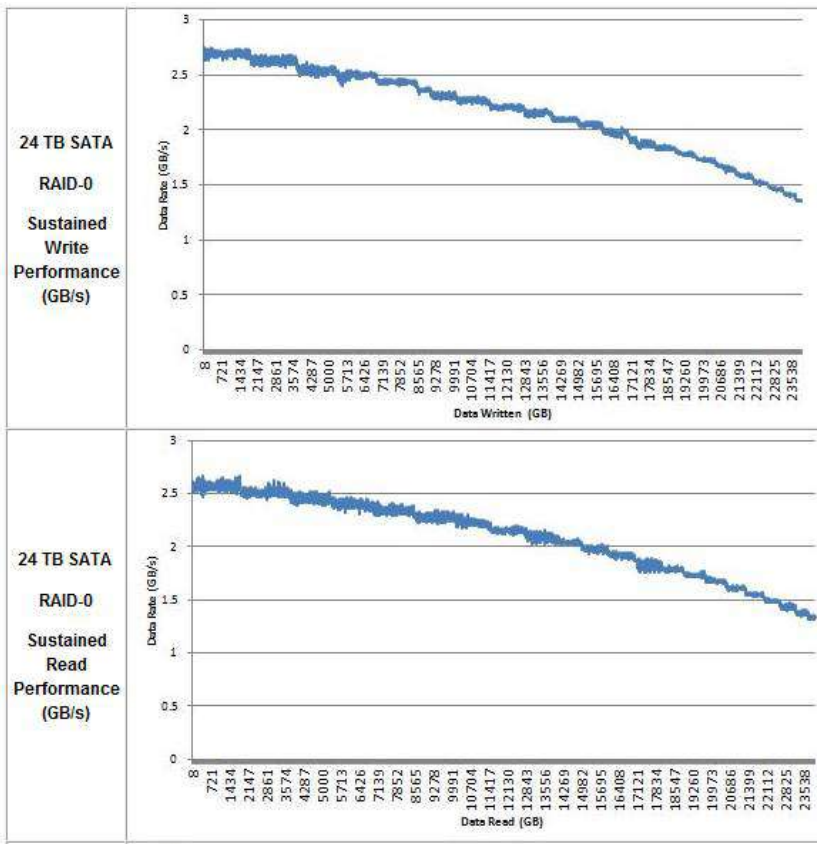
By combining programmatic control and monitoring with support for hot swapping hard drives, the HDD-8266 can be configured in an endless record mode. You can configure the 24 drives in the HDD-8266 as two discrete partitions (for example, Drive D: and E:). In your application, you can write to one of the partitions, and, once it is full, you can switch to the second partition. While writing to the second partition, you can programmatically disable the first partition, physically remove the hard drives, replace them with blank hard drives, and then programmatically create a new partition. Once the second partition is full, you can switch to this new partition to continue writing data to disk. The hard drives removed from the system still contain valid data and can later be plugged in the HDD-8266 for data removal or playback.

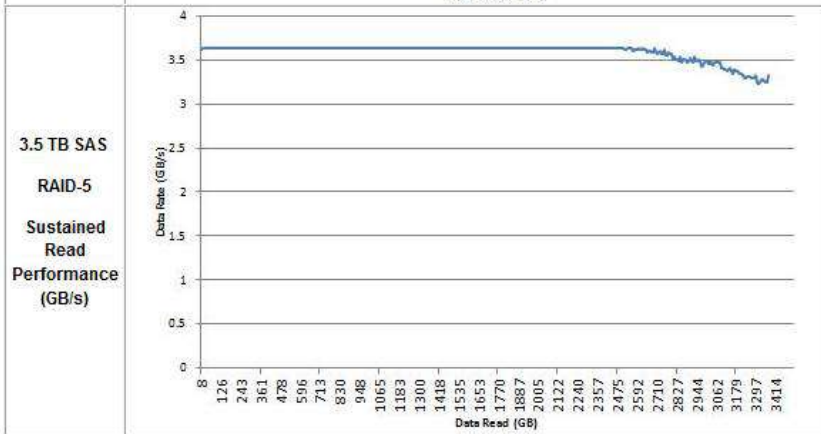
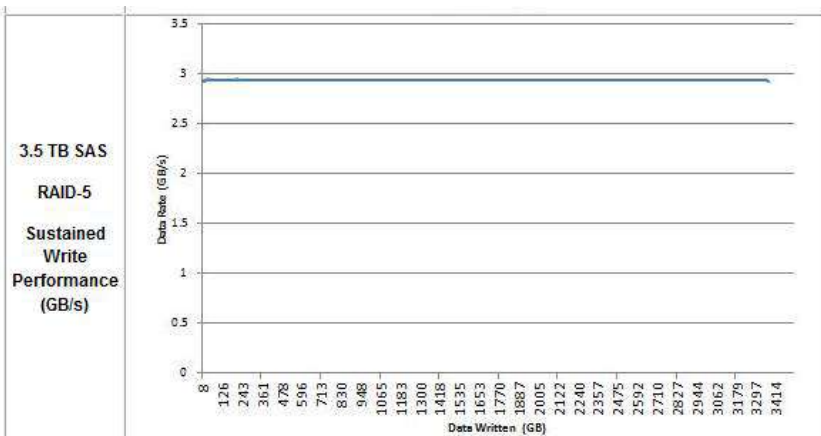
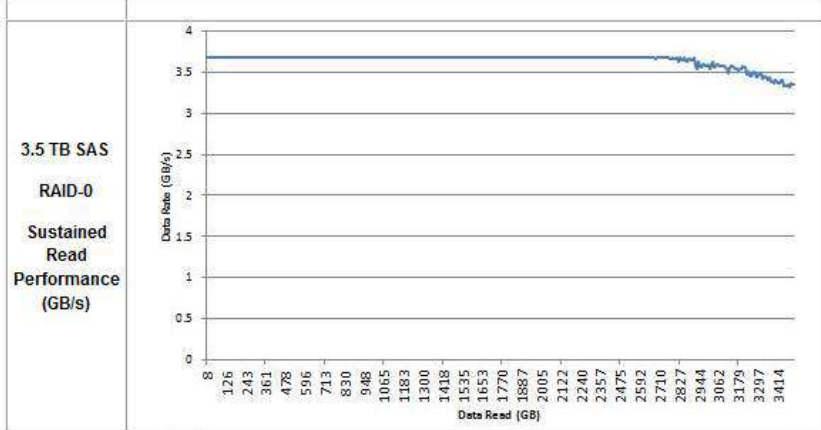
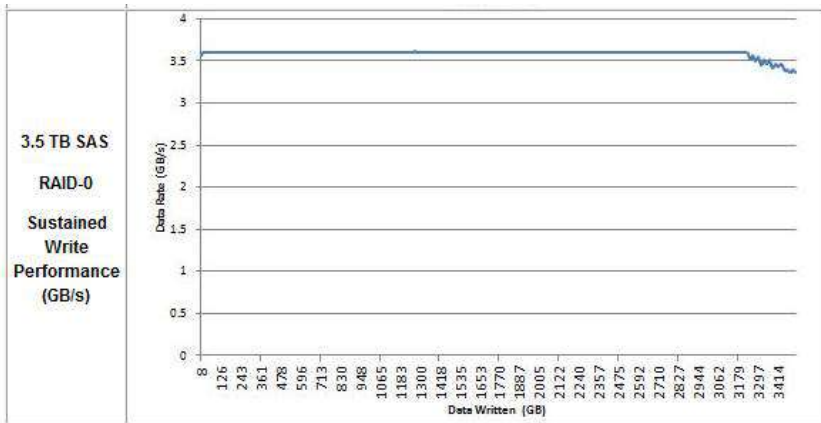
Recommended Chassis and Controller

To achieve the best streaming performance from an HDD-8266, National Instruments recommends using the NI PXIe-8135 embedded controller and the NI PXIe-1085 chassis because these products are optimized for high-speed streaming.

Streaming Benchmarks for NI HDD-8266:

The system configuration for this benchmarking included an NI PXIe-8135 PXI Express embedded controller running Windows 7 64-bit OS with 8 GB system RAM in an NI PXIe-1085 PXI Express chassis.





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Ordering Information

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For a complete list of accessories, visit the product page on ni.com.

Products	Part Number	Recommended Accessories	Part Number
NI HDD-8266 Options			
NI 8266, 24-Drive, 24TB SATA, Cabled PCIe HDD Enclosure w/RAID	782854-01	No accessories required.	
NI 8266 24-Drive, 3.5TB SAS, Cabled PCIe HDD Enclosure w/RAID	782858-01	No accessories required.	
MXI-Express Cable			
x8 MXI-Express Cable, 3 m	782317-03	No accessories required.	
Connectivity to PXI Express Chassis			
x8 MXI Express Cable, 3m	782317-03	No accessories required.	
NI PXIe-8384, x8 Gen 2 MXI Express DaisyChain Interface	782363-01	No accessories required.	

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Support and Services

System Assurance Programs

NI system assurance programs are designed to make it even easier for you to own an NI system. These programs include configuration and deployment services for your NI PXI, CompactRIO, or Compact FieldPoint system. The NI Basic System Assurance Program provides a simple integration test and ensures that your system is delivered completely assembled in one box. When you configure your system with the NI Standard System Assurance Program, you can select from available NI system driver sets and application development environments to create customized, reorderable software configurations. Your system arrives fully assembled and tested in one box with your software preinstalled. When you order your system with the standard program, you also receive system-specific documentation including a bill of materials, an integration test report, a recommended maintenance plan, and frequently asked question documents. Finally, the standard program reduces the total cost of owning an NI system by providing three years of warranty coverage and calibration service. Use the online product advisors at ni.com/advisor to find a system assurance program to meet your needs.

Calibration

NI measurement hardware is calibrated to ensure measurement accuracy and verify that the device meets its published specifications. To ensure the ongoing accuracy of your measurement hardware, NI offers basic or detailed recalibration service that provides ongoing ISO 9001 audit compliance and confidence in your measurements. To learn more about NI calibration services or to locate a qualified service center near you, contact your local sales office or visit ni.com/calibration.

Technical Support

Get answers to your technical questions using the following National Instruments resources.

- **Support** - Visit ni.com/support to access the NI KnowledgeBase, example programs, and tutorials or to contact our applications engineers who are located in NI sales offices around the world and speak the local language.
- **Discussion Forums** - Visit forums.ni.com for a diverse set of discussion boards on topics you care about.
- **Online Community** - Visit community.ni.com to find, contribute, or collaborate on customer-contributed technical content with users like you.

Repair

While you may never need your hardware repaired, NI understands that unexpected events may lead to necessary repairs. NI offers repair services performed by highly trained technicians who quickly return your device with the guarantee that it will perform to factory specifications. For more information, visit ni.com/repair.

Training and Certifications

The NI training and certification program delivers the fastest, most certain route to increased proficiency and productivity using NI software and hardware. Training builds the skills to more efficiently develop robust, maintainable applications, while certification validates your knowledge and ability.

- **Classroom training in cities worldwide** - the most comprehensive hands-on training taught by engineers.
- **On-site training at your facility** - an excellent option to train multiple employees at the same time.
- **Online instructor-led training** - lower-cost, remote training if classroom or on-site courses are not possible.
- **Course kits** - lowest-cost, self-paced training that you can use as reference guides.
- **Training memberships** and training credits - to buy now and schedule training later.

Visit ni.com/training for more information.

Extended Warranty

NI offers options for extending the standard product warranty to meet the life-cycle requirements of your project. In addition, because NI understands that your requirements may change, the extended warranty is flexible in length and easily renewed. For more information, visit ni.com/warranty.

OEM

NI offers design-in consulting and product integration assistance if you need NI products for OEM applications. For information about special pricing and services for OEM customers, visit ni.com/oem.

Alliance

Our Professional Services Team is comprised of NI applications engineers, NI Consulting Services, and a worldwide National Instruments Alliance Partner program of more than 700 independent consultants and integrators. Services range from start-up assistance to turnkey system integration. Visit ni.com/alliance.

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NI FlexRIO FPGA Modules



Overview

The NI FlexRIO family consists of PXI and PXI Express field-programmable gate array (FPGA) modules coupled to I/O adapter modules. Programmed with the NI LabVIEW FPGA Module, these modules together provide high-performance I/O and user-defined hardware processing on the PXI platform. NI FlexRIO FPGA modules feature the latest in FPGA technology and high-performance bus interfaces. National Instruments and third parties offer NI FlexRIO adapter modules, and you can build your own adapter modules using the NI FlexRIO Adapter Module Development Kit (MDK). With custom adapter modules, you can implement the exact analog and digital I/O your application requires, along with graphical FPGA programming provided by LabVIEW. View a current list of NI and third-party adapter modules at ni.com/flexrio.

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Requirements and Compatibility

OS Information

- FPGA
- Real-Time OS
- Windows 2000/XP
- Windows 7
- Windows Vista

Driver Information

- NI FlexRIO Adapter Module Support
- NI-RIO

Software Compatibility

- LabVIEW
- LabVIEW FPGA Module

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Application and Technology

Model	Bus/Form Factor	FPGA	FPGA Slices	FPGA DSP Slices	FPGA Memory (Block RAM)	Onboard Memory (DRAM)
NI PXIe-7965R/ 7966R ¹	PXI Express	Virtex-5 SX95T	14,720	640	8,784 kbit	512 MB
NI PXIe-7962R	PXI Express	Virtex-5 SX50T	8,160	288	4,752 kbit	512 MB
NI PXIe-7961R	PXI Express	Virtex-5 SX50T	8,160	288	4,752 kbit	0 MB
NI PXI-7954R	PXI	Virtex-5 LX110	17,280	64	4,608 kbit	128 MB
NI PXI-7953R	PXI	Virtex-5 LX85	12,960	48	3,456 kbit	128 MB
NI PXI-7952R	PXI	Virtex-5 LX50	7,200	48	1,728 kbit	128 MB
NI PXI-7951R	PXI	Virtex-5 LX30	4,800	32	1,152 kbit	0 MB

¹These two devices have different speed grade FPGAs: (-1) for the NI PXIe-7965R and (-2) for the NI PXIe-7966R. For more information on Xilinx Virtex-5 FPGA speed grades, refer to the Virtex-5 FPGA Data Sheet: DC and Switching Characteristics at xilinx.com.

Table 1. NI FlexRIO FPGA Module Options

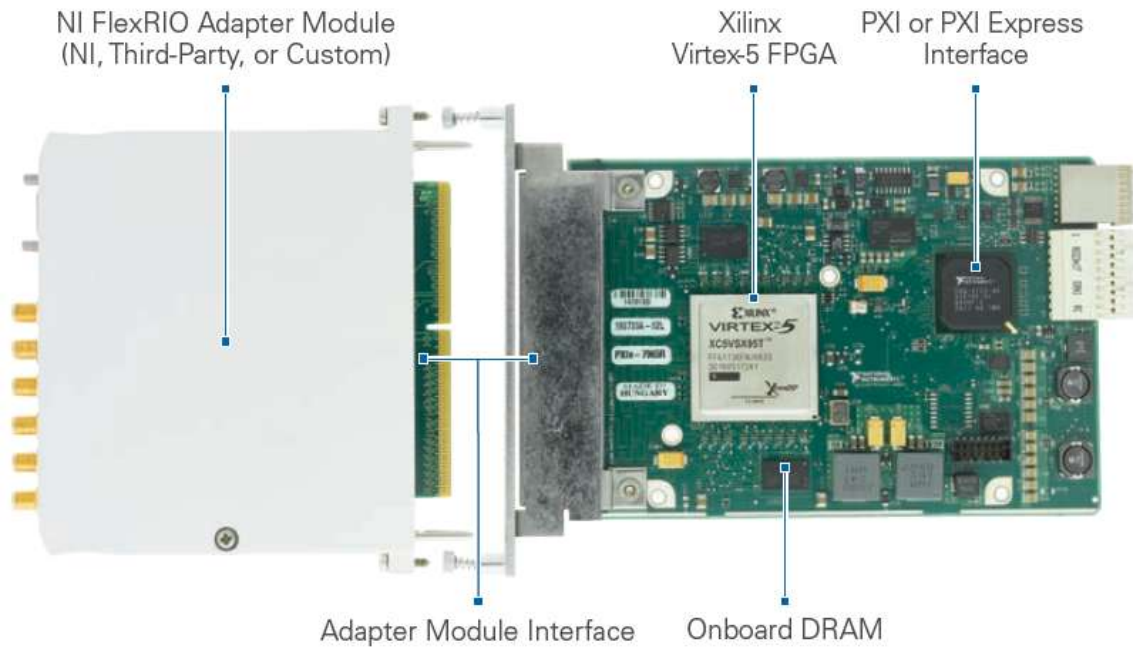


Figure 1. NI FlexRIO Architecture

Application	Example Algorithm
Inline signal processing	Continuous filtering, thresholding, peak detections, data reduction/compression, zero suppression, averaging
Custom triggering	Multievent, protocol-specific, variable hysteresis, logical AND/OR, data mask, multichannel
Software defined radio	Digital upconversion, downconversion, modulation, demodulation, packet assembly
"Protocol aware" semiconductor test systems	DUT-specific master and slave protocols
Custom RF communication scheme development and test	Custom modulation and demodulation, bit error rate test, fading profiles, additive noise
High-speed serial communication protocols	Serialization, deserialization, parallel algorithms
Deterministic analog or digital closed-loop control and interfacing	Frequency-based control loops, PID, emergency stop criteria evaluations, and assertion
High-performance and custom control or PXI-based test systems	Deterministic, low-latency instrument sequencing; high-performance DUT control
FPGA-based coprocessing/hardware acceleration	Algorithms exploiting FPGA throughput and parallelism, complementing host processing

Table 2. Example Applications and Algorithms That Benefit From User-Defined FPGA Processing and High-Performance I/O on the PXI Platform

NI FlexRIO FPGA Modules for PXI Express

PXI Express NI FlexRIO FPGA modules feature Xilinx Virtex-5 SXT FPGAs with up to 512 MB of onboard DRAM, which you can access at bandwidths up to 3.2 GB/s. In addition to general-purpose reconfigurable logic, SXT FPGAs are optimized for high-speed digital signal processing (DSP), with up to 640 DSP slices for single-cycle multiplication and filtering functions. PXI Express NI FlexRIO FPGA modules also feature the NI STC-3 application-specific integrated circuit (ASIC) to provide an optimized, high-bandwidth PCI Express x4 communications link to the backplane of the PXI Express chassis. This ASIC reduces the FPGA resources needed to implement host communication and enables new data transfer technology in the unique peer-to-peer streaming feature.

For multiadapter module synchronization, PXI Express NI FlexRIO FPGA modules include the I/O Module Synchronization Clock, which you can use to synchronize multiple adapter modules, provided the adapter module supports this signal.



Figure 2. NI ASIC technology and Xilinx FPGAs provide a high-performance platform for flexible, user-customizable instrumentation.

Peer-to-Peer Data Streaming

With NI peer-to-peer data streaming technology, you can continually transfer data to and from PXI Express NI FlexRIO FPGA modules at rates greater than 800 MB/s with minimal latency. High-performance data switches on NI PXI Express chassis offer high-bandwidth communication, and routing data from one module directly to another (without transferring data through the host controller) minimizes the latency of the transfer. Peer-to-peer transfers are supported between multiple PXI Express NI FlexRIO FPGA modules and between select NI PXI Express digitizers and PXI Express NI FlexRIO FPGA modules. Figure 3 depicts a peer-to-peer system with an NI PXIe-5122 digitizer and two NI PXIe-7965R NI FlexRIO FPGA modules for distributed serial data processing.

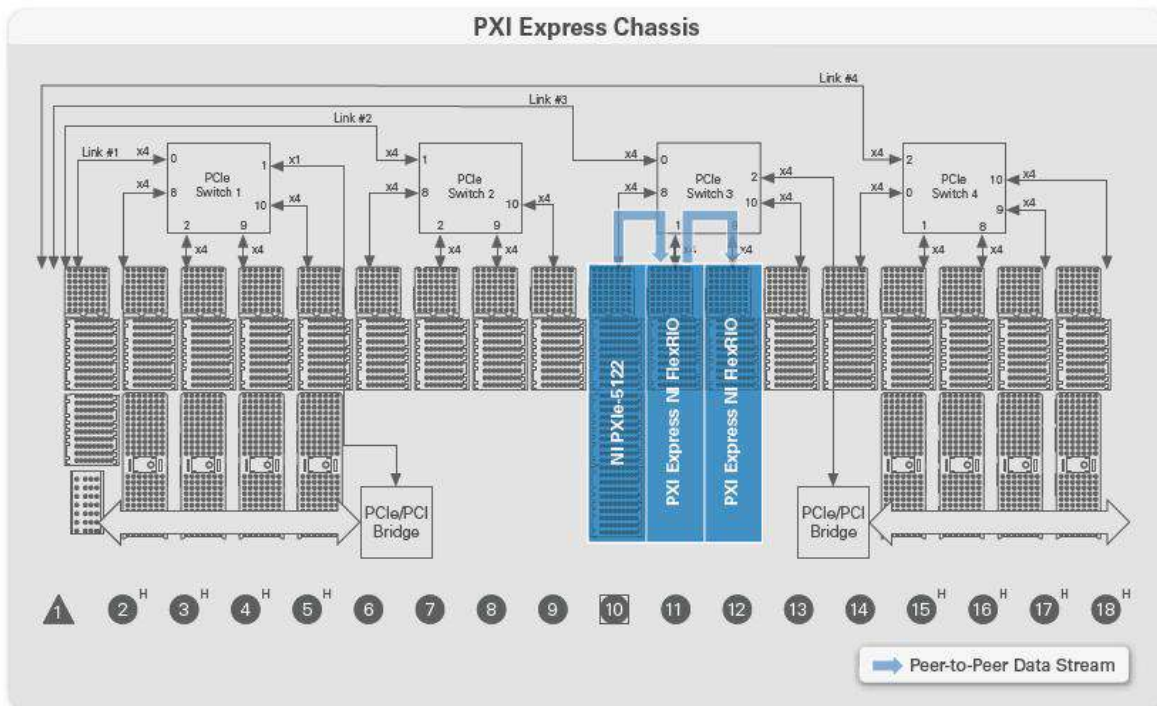


Figure 3. Peer-to-peer systems rely on high-performance PXI Express chassis and controllers as well as proprietary NI data streaming technology on NI FlexRIO FPGA modules and NI modular instruments.

In LabVIEW FPGA, you access these peer-to-peer streams through simple first-in-first-out (FIFO) nodes. An easy-to-use API on the host controller sets up a peer-to-peer stream between multiple FPGA modules after you configure peer-to-peer FIFOs on each.

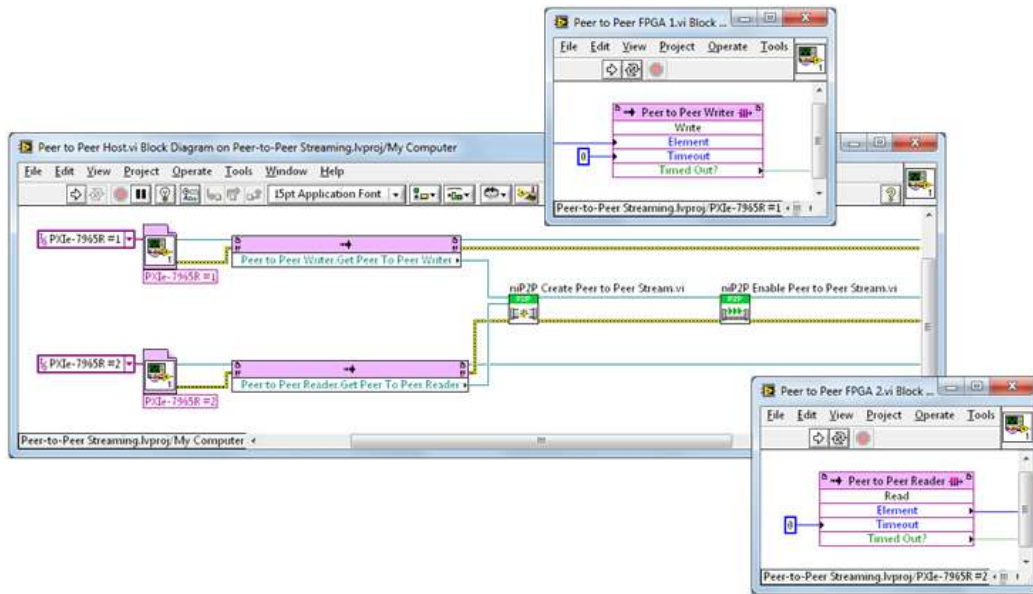


Figure 4. The NI-P2P driver offers simple, high-level access to the high-performance capabilities of peer-to-peer streaming, and intuitive nodes on the FPGA block diagram simplify data transfer.

NI FlexRIO FPGA Modules for PXI

PXI NI FlexRIO FPGA modules feature Xilinx Virtex-5 LX FPGAs with up to 128 MB of onboard DRAM, which you can access at bandwidths up to 1.6 GB/s. They feature all of the benefits of the PXI platform including synchronization, triggering, and high-speed data transfer to and from their hosts.

Feature	PXI NI FlexRIO FPGA Modules	PXI Express NI FlexRIO FPGA Modules
Xilinx Virtex-5 FPGAs		
132-Line Adapter Module Interface		
I/O Module Synchronization		
Peer-to-Peer Data Streaming		

Table 3. PXI and PXI Express FPGA Module Comparison

NI FlexRIO Adapter Modules

NI and National Instruments Alliance Partners offer NI FlexRIO adapter modules. You also can build your own with the NI FlexRIO Adapter MDK. View a list of NI FlexRIO adapter modules at ni.com/flexrio.

NI Adapter Modules

NI FlexRIO adapter modules provide high-performance I/O that you can customize with the NI FlexRIO FPGA module. With these adapter modules, National Instruments includes the module-specific Component-Level IP (CLIP) Node, which defines the interface between LabVIEW and the adapter module. This helps you begin programming your application immediately, without a low-level understanding of the adapter module design or functionality. Examples demonstrate how to effectively use the CLIP Node.

Third-Party Adapter Modules

In addition to NI FlexRIO adapter modules built by National Instruments, NI Alliance Partners can build adapter modules with the same degree of performance, functionality, and integration. These modules are available as either standard or custom products.

Custom Adapter Modules

If you cannot find an adapter module that meets your application needs from National Instruments or an NI Alliance Partner, you can build your own custom adapter module using the NI FlexRIO Adapter Module Development Kit (MDK).



Figure 5. The NI FlexRIO Adapter Module Development Kit (MDK) features the documentation, design files, and adapter module enclosures to build your own NI FlexRIO adapter module.

With the NI FlexRIO Adapter MDK, you receive the following:

- A comprehensive module development user manual
- Example adapter module support files
- Three blank adapter module enclosures
- One windowed adapter module enclosure for debugging
- Mechanical drawings for the adapter module PCB, card-edge connector, and front panel
- Direct support from NI R&D engineers, including a one-hour design review to help ensure electrical compatibility with NI FlexRIO FPGA modules

Programming NI FlexRIO With the LabVIEW FPGA Module

Graphical FPGA Programming

NI LabVIEW and the LabVIEW FPGA Module deliver graphical development for FPGA devices on NI reconfigurable I/O (RIO) hardware targets. You can create embedded FPGA VIs that combine direct access to I/O with user-defined LabVIEW logic to define custom hardware.

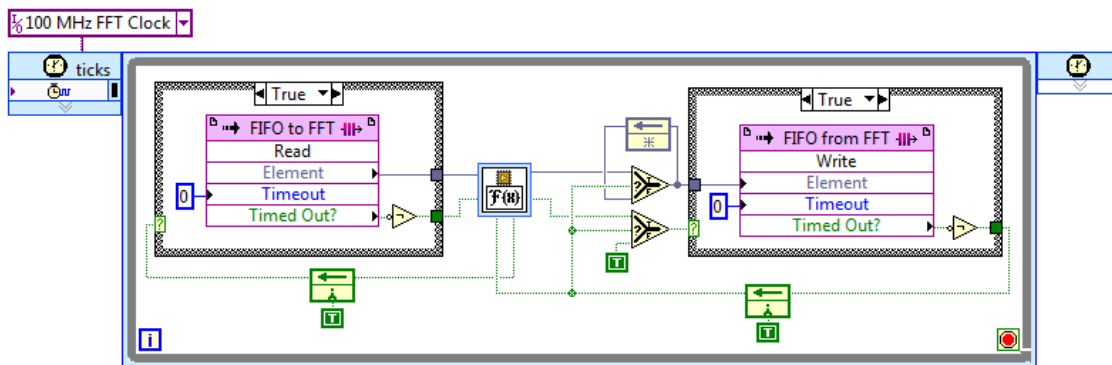
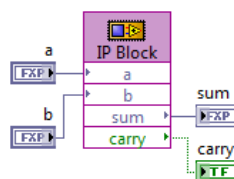


Figure 6. This LabVIEW code depicts a user-configurable, hardware-based FFT operation. It features fixed-point data processing, a dedicated 100 MHz clock domain in a single-cycle Timed Loop (100 MHz FFT clock), FIFOs to enter and exit the clock domain (FIFO to FFT and FIFO from FFT), flow control to ensure sample-accurate execution and account for multicycle IP latency, and a user-configurable FFT function (FFT).

Integrating HDL

While LabVIEW is an effective tool for FPGA programming, you may have existing hardware description language (HDL) intellectual property (IP) that you must integrate into your NI FlexRIO hardware applications. You have three options for doing this. The first is the IP Integration Node. This node provides a simple, inline interface to HDL IP and Xilinx CORE Generator XCO files. It features automatic LabVIEW interface generation and the ability to generate cycle-accurate simulation models for host execution. Using the latter functionality, you can run your LabVIEW FPGA VI on the host to ensure proper functionality before compiling it for the FPGA.



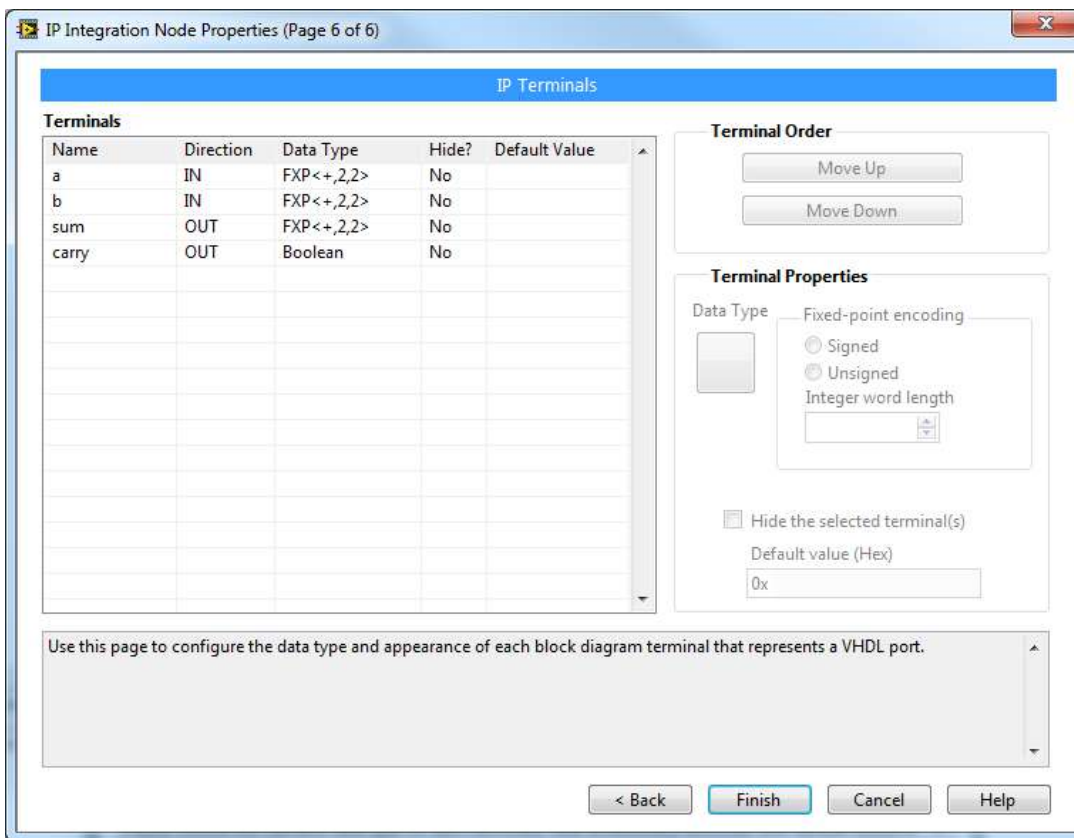
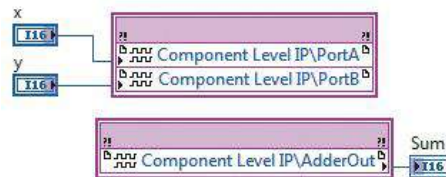


Figure 7. With the IP Integration Node, you can import VHDL and Xilinx CORE Generator XCO files. It automatically generates the LabVIEW interface (for use in a single clock domain) and creates a cycle-accurate simulation model for host PC code emulation.

For more complex HDL that may use multiple clock domains and execute asynchronously, the CLIP Node offers an interface. Through an XML wrapper, you import the HDL into LabVIEW and access it through I/O nodes. You also use the CLIP Node to interface to the NI FlexRIO adapter module as well as the FPGA module onboard DRAM. The CLIP Node executes asynchronously to the LabVIEW block diagram, can support multiple clocks, and is required for customizing certain features of the hardware such as the adapter module interface. This is different from the IP Integration Node, which executes inline with the LabVIEW block diagram and can be accurately simulated with the LabVIEW host simulation.



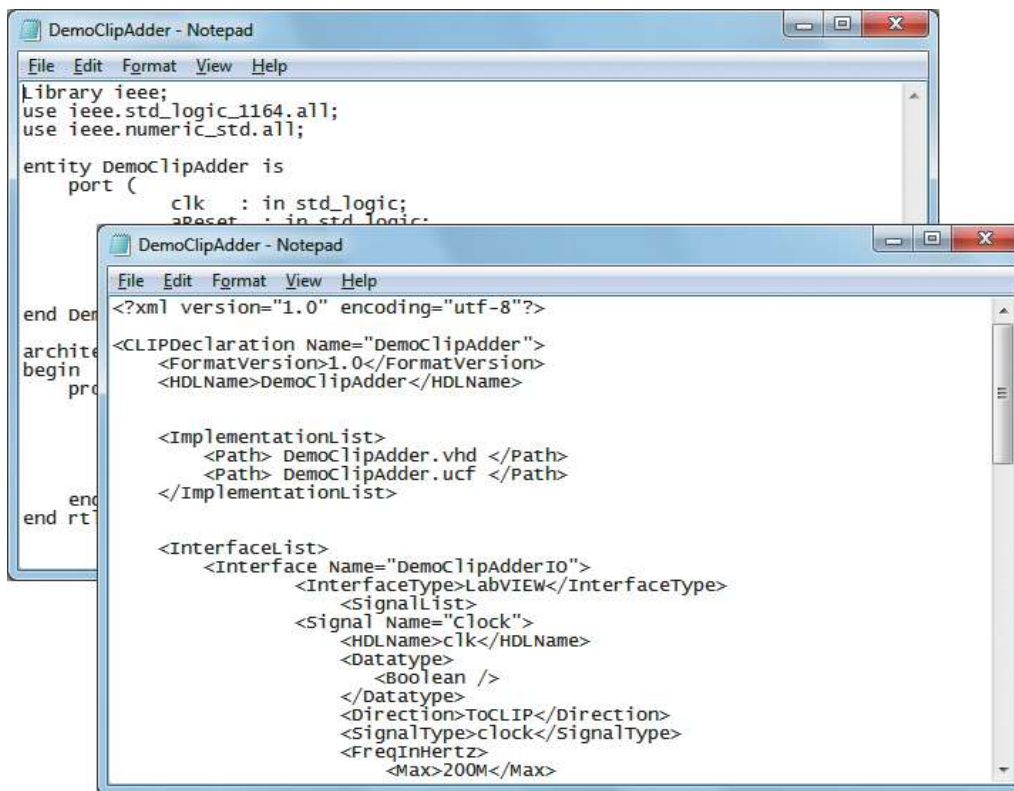
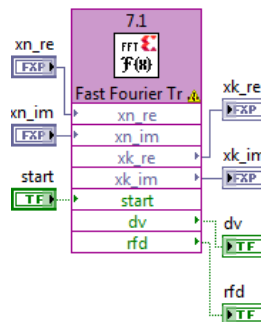


Figure 8. With the CLIP Node, you can import HDL or netlists through an XML wrapper file for asynchronous execution.

The Xilinx CORE Generator IP functions are designed to streamline the process for importing Xilinx CORE Generator files. The Xilinx CORE Generator uses the IP Integration Node to conveniently incorporate Xilinx CORE Generator IP into an FPGA VI by allowing you to configure the Xilinx CORE from within the LabVIEW environment.



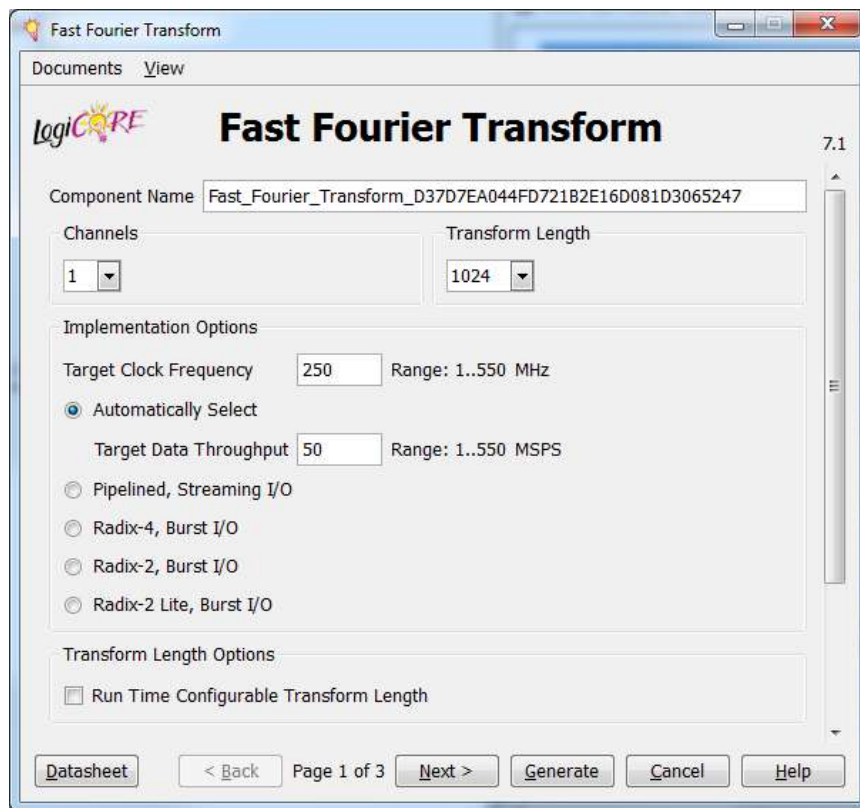


Figure 9. The Xilinx CORE Generator IP functions incorporate the IP Integration Node and Xilinx CORE Generator so you can configure the Xilinx CORE from within LabVIEW.

NI FlexRIO Development Tools

NI FlexRIO development tools consist of the NI FlexRIO Instrument Development Library and the NI-573xR Example Instrument Driver. Both are available for download from ni.com/labs.

NI FlexRIO Instrument Development Library

The NI FlexRIO Instrument Development Library is a collection of LabVIEW Host and FPGA code designed to provide FPGA capabilities commonly found in instruments such as acquisition engines, DRAM interfaces, and trigger logic, along with the associated host APIs. This code is open and modular, so you can choose only the components you need, and it delivers efficient implementation. You also can use it to modify the code provided in the library, if necessary, to meet your unique application needs.

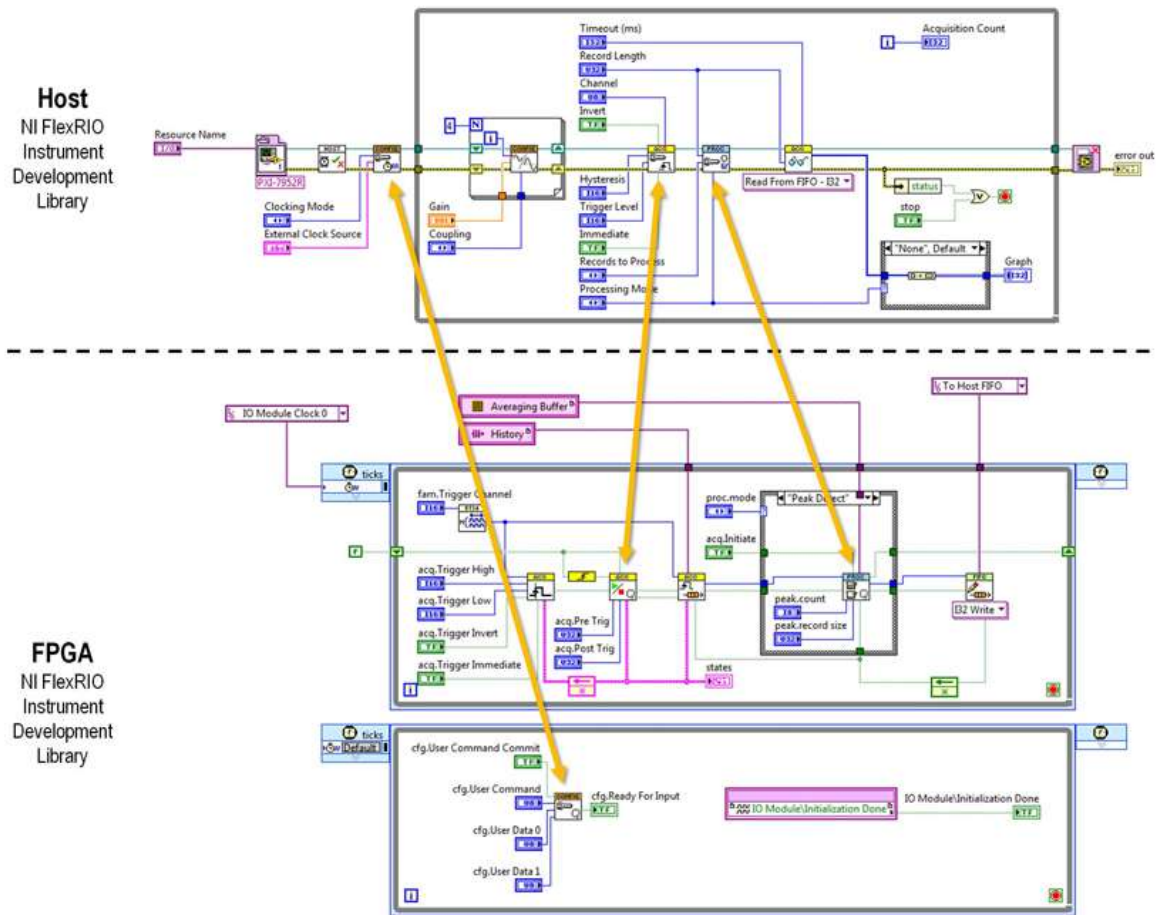


Figure 10. The NI FlexRIO Instrument Development Library provides LabVIEW Host and FPGA code building blocks for capabilities commonly found in instruments.

NI-573xR Example Instrument Driver

The NI-573xR Example Instrument Driver builds on the NI FlexRIO Instrument Development Library to deliver a familiar software API and default FPGA personality for NI 573xR digitizer adapter modules. It helps you quickly begin taking measurements, modify both the LabVIEW Host and FPGA code to suit your application, and provides access to the full capabilities of user-customizable instrumentation hardware.

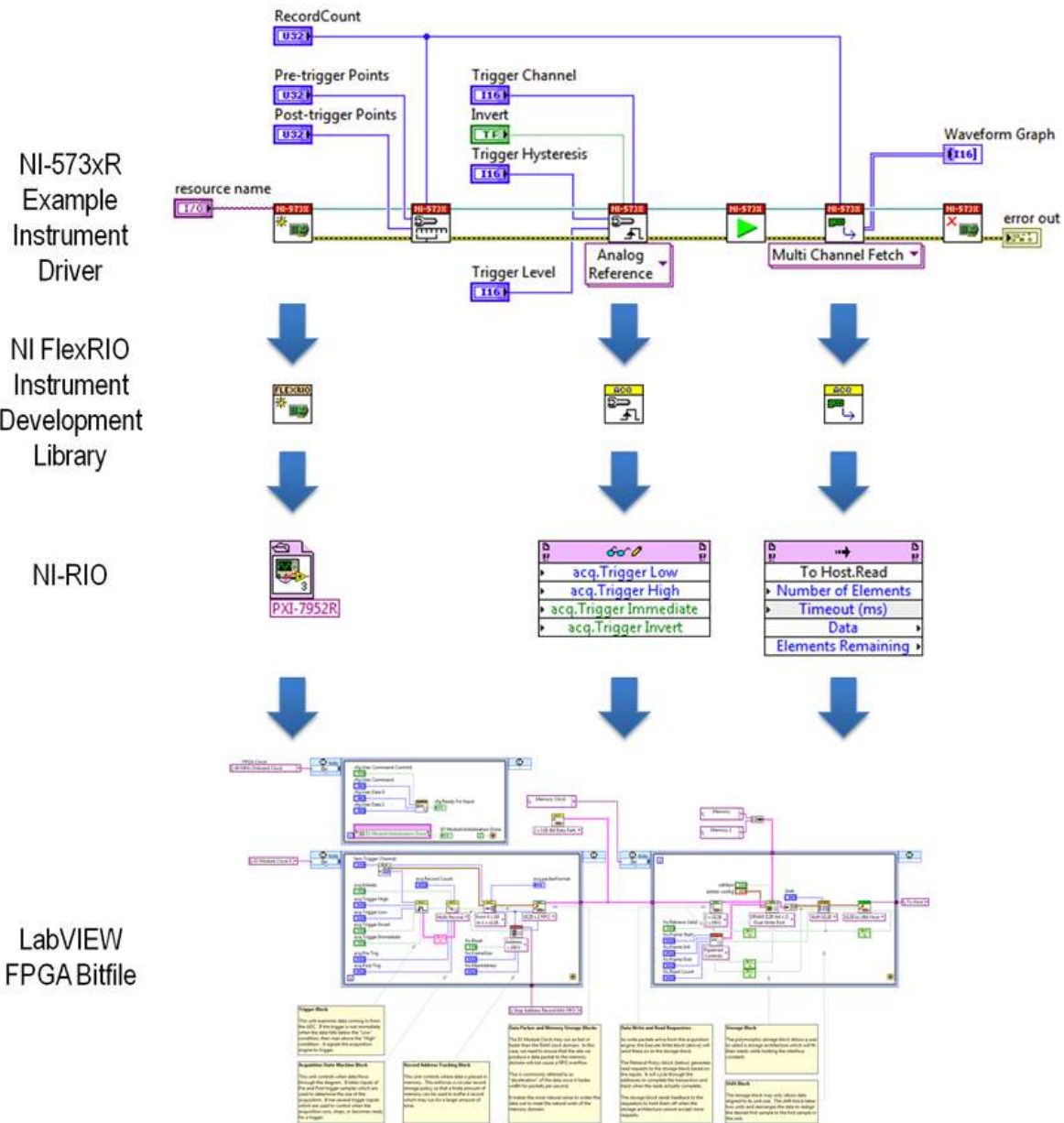
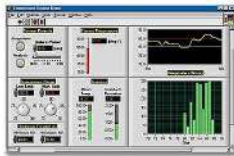


Figure 11. The NI-573xR Example Instrument Driver builds on the NI FlexRIO Instrument Development Library to provide a high-level Host API with an underlying FPGA acquisition engine.

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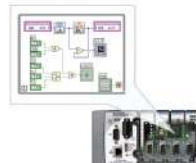
Software Recommendations

LabVIEW Professional Development System for Windows



- Advanced software tools for large project development
- Automatic code generation using DAQ Assistant and Instrument I/O Assistant
- Tight integration with a wide range of hardware
- Advanced measurement analysis and digital signal processing
- Open connectivity with DLLs, ActiveX, and .NET objects
- Capability to build DLLs, executables, and MSI installers

NI LabVIEW FPGA Module



- Design FPGA applications for NI reconfigurable I/O (RIO) hardware targets
- Program with the same graphical environment used for desktop and real-time applications
- Execute control algorithms with loop rates up to 300 MHz
- Implement custom timing and triggering logic, digital protocols, and DSP algorithms
- Incorporate existing HDL code and third-party IP including Xilinx CORE Generator functions
- Included in the LabVIEW Embedded Control and Monitoring Suite

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Support and Services

System Assurance Programs

NI system assurance programs are designed to make it even easier for you to own an NI system. These programs include configuration and deployment services for your NI PXI, CompactRIO, or Compact FieldPoint system. The NI Basic System Assurance Program provides a simple integration test and ensures that your system is delivered completely assembled in one box. When you configure your system with the NI Standard System Assurance Program, you can select from available NI system driver sets and application development environments to create customized, reorderable software configurations. Your system arrives fully assembled and tested in one box with your software preinstalled. When you order your system with the standard program, you also receive system-specific documentation including a bill of materials, an integration test report, a recommended maintenance plan, and frequently asked question documents. Finally, the standard program reduces the total cost of owning an NI system by providing three years of warranty coverage and calibration service. Use the online product advisors at ni.com/advisor to find a system assurance program to meet your needs.

Technical Support

Get answers to your technical questions using the following National Instruments resources.

- **Support** - Visit ni.com/support to access the NI KnowledgeBase, example programs, and tutorials or to contact our applications engineers who are located in NI sales offices around the world and speak the local language.
- **Discussion Forums** - Visit forums.ni.com for a diverse set of discussion boards on topics you care about.
- **Online Community** - Visit community.ni.com to find, contribute, or collaborate on customer-contributed technical content with users like you.

Repair

While you may never need your hardware repaired, NI understands that unexpected events may lead to necessary repairs. NI offers repair services performed by highly trained technicians who quickly return your device with the guarantee that it will perform to factory specifications. For more information, visit ni.com/repair.

Training and Certifications

The NI training and certification program delivers the fastest, most certain route to increased proficiency and productivity using NI software and hardware. Training builds the skills to more efficiently develop robust, maintainable applications, while certification validates your knowledge and ability.

- **Classroom training in cities worldwide** - the most comprehensive hands-on training taught by engineers.
- **On-site training at your facility** - an excellent option to train multiple employees at the same time.
- **Online instructor-led training** - lower-cost, remote training if classroom or on-site courses are not possible.
- **Course kits** - lowest-cost, self-paced training that you can use as reference guides.
- **Training memberships** and training credits - to buy now and schedule training later.

Visit ni.com/training for more information.

Extended Warranty

NI offers options for extending the standard product warranty to meet the life-cycle requirements of your project. In addition, because NI understands that your requirements may change, the extended warranty is flexible in length and easily renewed. For more information, visit ni.com/warranty.

OEM

NI offers design-in consulting and product integration assistance if you need NI products for OEM applications. For information about special pricing and services for OEM customers, visit ni.com/oem.

Alliance

Our Professional Services Team is comprised of NI applications engineers, NI Consulting Services, and a worldwide National Instruments Alliance Partner program of more than 700 independent consultants and integrators. Services range from start-up assistance to turnkey system integration. Visit ni.com/alliance.

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Detailed Specifications

Reconfigurable FPGA				
Device	FPGA	LUTs/Flip-Flops	DSP48 Slices (25 x 18 Multiplier)	Embedded Block RAM (kbits)
NI PXI-7951R	Virtex-5 LX30	19,200	32	1,152
NI PXI-7952R	Virtex-5 LX50	28,800	48	1,728
NI PXI-7953R	Virtex-5 LX85	51,840	48	3,456
NI PXI-7954R	Virtex-5 LX110	69,120	64	4,608
NI PXI-7961R	Virtex-5 SX50T	32,640	288	4,752
NI PXI-7962R	Virtex-5 SX50T	32,640	288	4,752
NI PXI-7965R	Virtex-5 SX95T	58,880	640	8,784

Default timebase 40MHz

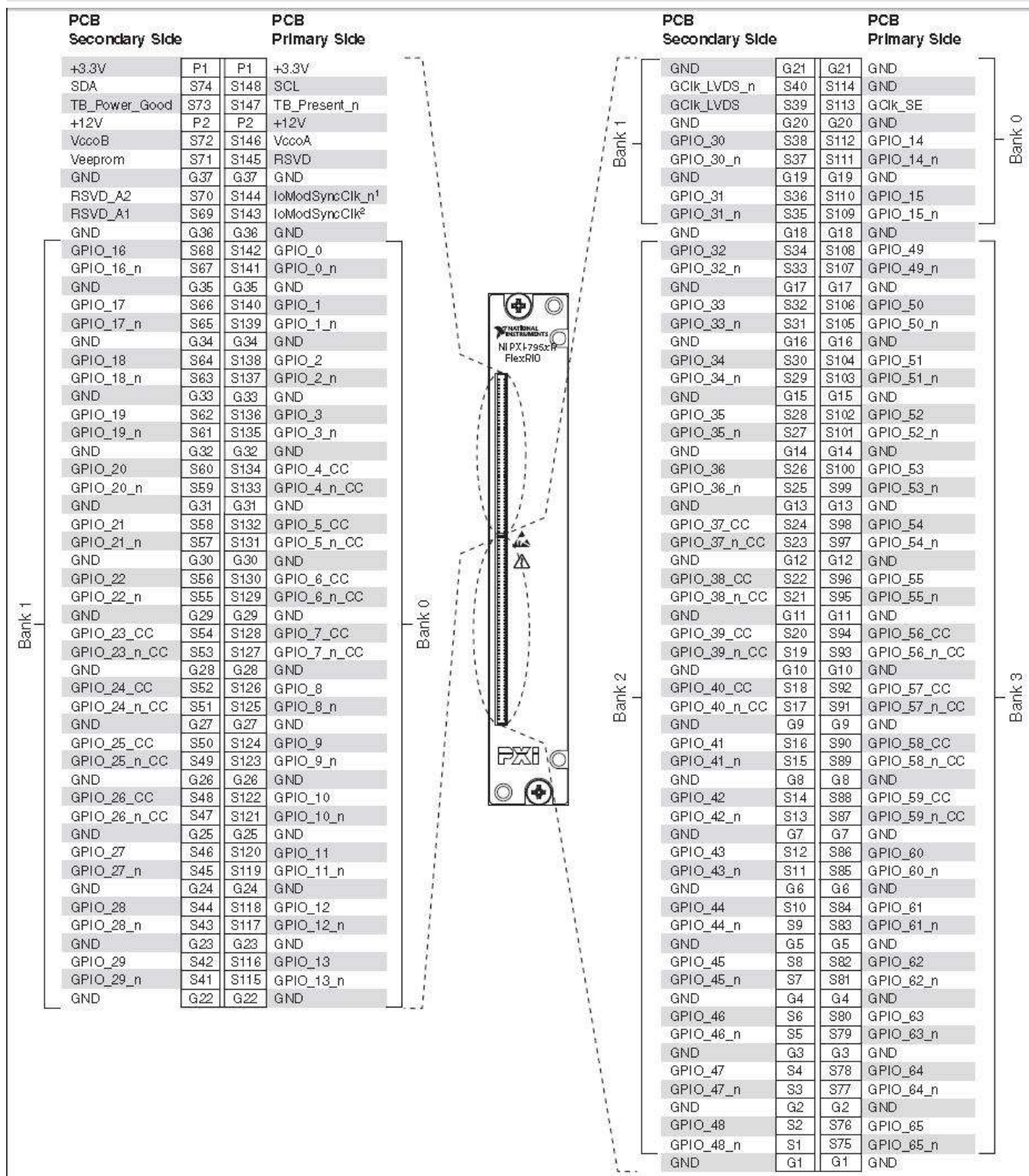
Timebase reference sources

NI PXI-795xR PXI 10 MHz
NI PXI-796xR PXIe 100 MHz

Timebase accuracy

NI PXI-795xR ±100 ppm, 250 ps

	peak-to-peak jitter
NI PXI-796xR	±50 ppm, 250 ps peak-to-peak jitter
Data transfers	DMA, interrupts, programmed I/O
Number of DMA channels	
NI PXI-795xR	3
NI PXI-796xR	16
FPGA Digital Input/Output	
Number of general-purpose channels	132, configurable as 132 single-ended, 66 differential, or a combination of both ¹
Channels per bank	
Bank 0/Bank 2	32, single-ended per bank
Bank 1/Bank 3	34, single-ended per bank
Compatibility	Configured via FPGA, 1.2 V to 3.3 V I/O standards (refer to www.xilinx.com)
Protection	Refer to www.xilinx.com
Current	Refer to www.xilinx.com
Maximum I/O data rates	
Single-ended	400 Mb/s for LVDCI25
Differential	1 Gb/s for LVDS
Global clock inputs	1 LVTTTL, 1 LVDS
Connection resources	
NI PXI-795xR	PXI triggers, Clk10, and PXI star trigger
NI PXI-796xR	PXI triggers, Clk10, PXI star trigger, DStarA, DStarB, DStarC, and Sync100
Device Signals	



1 RSVD_B2 on the NI PXI-795xR

2 RSVD_B1 on the NI PXI-795xR

Figure 1. NI FlexRIO FPGA Module Front Connector Pin Assignments and Locations

Onboard DRAM

Memory size

NI PXI-795xR	2 banks; 64 MB per bank
NI PXI-796xR	2 banks; 256 MB per bank

Maximum theoretical data rate

NI PXI-795xR	800 MB/s per bank
NI PXI-796xR	1.6 GB/s per bank

Bus Interface

PXI	Master, slave
PXI Express	
Form factor	x4 PXI Express, specification v1.0 compliant
Slot compatibility	x4, x8, and x16 PXI Express or PXI Express hybrid slots

Maximum Power Requirement

PXI	Master, slave
NI PXI-795xR	
+5 VDC (±5%)	2 A
+3.3 VDC (±5%)	2 A
+12 V	0.5 A
-12 V	0 A
NI PXI-796xR	
+5 VDC (±5%)	3 A
+3.3 VDC (±5%)	2 A

Physical

Dimensions (not including connectors)

NI PXI-795xR	18.8 cm × 12.9 cm (7.4 in. × 5.1 in.)
NI PXI-796xR	16.1 cm × 10.8 cm (6.3 in. × 4.3 in.)

Weight

NI PXI-795xR	190 g (6.7 oz)
NI PXI-796xR	213 g (7.5 oz)

I/O connector High-density card edge

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth	0 V to 3.3 V, Measurement Category I
Channel-to-channel	0 V to 3.3 V, Measurement Category I



Caution Do not use this device for connection to signals in Measurement Categories II, III, or IV.

Environmental

This device is intended for indoor use only.

Operating environment	0°C to 55°C, tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.
Relative humidity range	10% to 90%, noncondensing, tested in accordance with IEC-60068-2-56.
Altitude	2,000 m at 25°C ambient temperature
Pollution Degree	2
Storage environment	
Ambient temperature range	-40°C to 70°C, tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.
Relative humidity range	5% to 95%, noncondensing, tested in accordance with IEC-60068-2-56.

Shock and Vibration

Operational shock	30 g peak, half-sine, 11 ms pulse, tested in accordance with IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.
Random vibration	
Operating	5 Hz to 500 Hz, 0.3 grms
Nonoperating	5 Hz to 500 Hz, 2.4 grms, tested in accordance with IEC-60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.

Safety

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1



Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326 (IEC 61326): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions



Note For the standards applied to assess the EMC of this product, refer to the *Online Product Certification* section.



Note EMC compliance evaluated with a wrapback adapter module and general purpose I/O (GPIO) signals configured to LVTTTL I/O standard, slew rate set to slow, and drive strength set to 6 mA. EMC compliance of other I/O standards, faster slew rates, and greater drive strength is not guaranteed.

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit ni.com/certification, search by module number or product line, and click the appropriate link in the Certification column.

Environmental Management

National Instruments is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial not only to the environment but also to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)



EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste Electrical and Electronic Equipment, visit ni.com/environment/weee.htm.

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NI PXIe-7966R

FPGA Module

This document explains how to install your NI FlexRIO system, comprised of the NI PXIe-7966R FlexRIO FPGA module and an NI FlexRIO adapter module. This document also contains the specifications for the NI PXIe-7966R FlexRIO FPGA module.

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Electromagnetic Compatibility Guidelines

This product was tested and complies with the regulatory requirements and limits for electromagnetic compatibility (EMC) stated in the product specifications. These requirements and limits provide reasonable protection against harmful interference when the product is operated in the intended operational electromagnetic environment.

This product is intended for use in industrial locations. However, harmful interference may occur in some installations, when the product is connected to a peripheral device or test object, or if the product is used in residential or commercial areas. To minimize interference with radio and television reception and prevent unacceptable performance degradation, install and use this product in strict accordance with the instructions in the product documentation.

Furthermore, any changes or modifications to the product not expressly approved by National Instruments could void your authority to operate it under your local regulatory rules.



Caution To ensure the specified EMC performance, operate this product only with shielded cables and accessories.



Caution Refer to the *Read Me First: Safety and Electromagnetic Compatibility* document for important safety and electromagnetic compatibility information. To obtain a copy of this document online, visit ni.com/manuals, and search for the document title.



Caution When exposed to transient electromagnetic phenomena such as electrostatic discharge (ESD) or power surges, this product may experience a temporary upset or other performance degradation that requires more than 10 seconds for self-recovery.



Caution The NI FlexRIO FPGA module front panel interface is sensitive to electrostatic discharge. Use caution when handling the NI FlexRIO FPGA module to prevent damage to the internal components exposed by this interface.



Caution Using the NI PXIe-7966R in a manner not described in this document may impair the protection the NI PXIe-7966R provides.

How to Use Your NI FlexRIO Documentation Set

Refer to Figure 1 and Table 1 to learn how to use your FlexRIO documentation set.

Figure 1. How to Use Your NI FlexRIO Documentation Set.

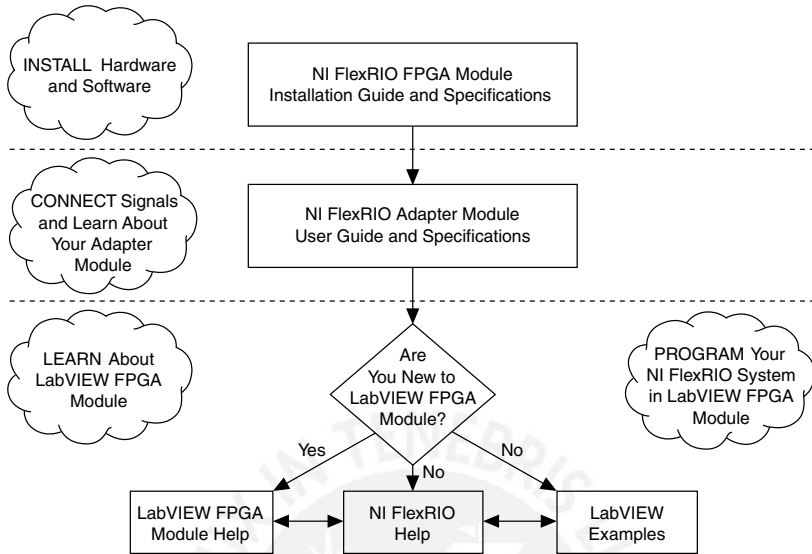


Table 1. NI FlexRIO Documentation Locations and Descriptions

Document	Location	Description
<i>NI PXIe-7966R Installation Guide and Specifications</i> (this document)	Available from the Start menu and at ni.com/manuals .	Contains installation instructions for your NI FlexRIO system and specifications for your FPGA module.
<i>Adapter Module User Manual and Specifications</i>	Available from the Start menu and at ni.com/manuals .	Contains signal information, examples, CLIP details, and specifications for your adapter module.
<i>LabVIEW FPGA Module Help</i>	Embedded in <i>LabVIEW Help</i> and at ni.com/manuals .	Contains information about the basic functionality of the LabVIEW FPGA Module.
<i>NI FlexRIO Help</i>	Available from the Start menu and at ni.com/manuals .	Contains FPGA Module, adapter module, and CLIP configuration information.
LabVIEW Examples	Available in NI Example Finder.	Contains examples of how to run FPGA VIs and Host VIs on your device.

Table 1. NI FlexRIO Documentation Locations and Descriptions (Continued)

Document	Location	Description
IPNet	ni.com/ipnet	Contains LabVIEW FPGA functions and intellectual property to share.
NI FlexRIO product page	ni.com/flexrio	Contains product information and data sheets for NI FlexRIO devices.

Required Components

The following items are necessary to set up and use your NI FlexRIO system:

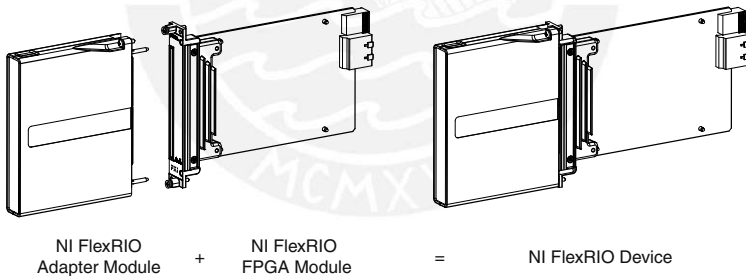
- The NI FlexRIO hardware device, comprised of the following items:
 - NI PXIe-7966R
 - NI FlexRIO adapter module



Note You can use the NI FlexRIO FPGA module without an adapter module for coprocessing or peer-to-peer streaming. The adapter module installation instructions in this document do not apply to these circumstances.

The figure below shows the combined module.

Figure 2. Combining Your Adapter Module and FPGA Module



- The following software packages:
 - LabVIEW
 - LabVIEW FPGA Module
 - NI FlexRIO Support



Note The most recent version of NI FlexRIO Support is available at ni.com. Visit ni.com/info and enter `flexriosoftware` as the Info Code to download the latest version of NI FlexRIO Support.

- NI FlexRIO Adapter Module Support¹



Note The most recent version of NI FlexRIO Adapter Module Support is available at ni.com. Visit ni.com/info and enter `famsoftware` as the Info Code to download the latest version of NI FlexRIO Adapter Module Support. You do not need this software if you are not using an adapter module.

- (Optional) LabVIEW Real-Time Module.
- One of the following chassis:
 - PXI/CompactPCI chassis
 - PXI Express/CompactPCI Express chassis
- One of the following controllers:
 - PXI/CompactPCI embedded controller
 - PXI Express/CompactPCI Express embedded controller
 - MXI kit and a PC
- One of the following operating systems:
 - Windows 8
 - Windows 7
 - Windows Vista
 - Windows XP Pro x32 Service Pack 2 or Service Pack 3
- At least one cable for connecting signals to the NI FlexRIO device. Refer to your adapter module documentation for a list of applicable cables and accessories for your NI FlexRIO system.

Related Information

[Installing the Application Software and Driver](#) on page 5

Installing the Application Software and Driver

Before installing your hardware, you must install the application software and instrument driver. Visit ni.com/info and enter `rdsoftwareversion` as the Info Code to determine which minimum software versions you need for your device. Install the software in the following order:

1. Install LabVIEW. Refer to the *LabVIEW Installation Guide* for installation instructions for LabVIEW and system requirements for the LabVIEW software. Refer to the *LabVIEW Upgrade Notes* for additional information about upgrading to the most recent version of LabVIEW for Windows.

Documentation for LabVIEW is available at ni.com/manuals and by selecting **Start»All Programs»National Instruments»LabVIEW»LabVIEW Manuals**.

¹ The NI 1483 adapter module requires the NI-IMAQ instrument driver instead of NI FlexRIO Adapter Module Support.

2. Install the LabVIEW FPGA Module. Refer to the *LabVIEW FPGA Module Release and Upgrade Notes* for installation instructions and information about getting started with the LabVIEW FPGA Module.

Documentation for the LabVIEW FPGA Module is available at ni.com/manuals and by selecting **Start»All Programs»National Instruments»LabVIEW»LabVIEW Manuals**.

3. (Optional) Install the LabVIEW Real-Time Module. Refer to the *LabVIEW Real-Time Module Release and Upgrade Notes* for system requirements, installation instructions, and additional information about using the LabVIEW Real-Time Module.
4. Install NI FlexRIO. Refer to the *NI FlexRIO Readme* on the NI FlexRIO installation media for system requirements and installation instructions for NI FlexRIO Support.

Documentation for NI FlexRIO Support is available at ni.com/manuals and by selecting **Start»All Programs»National Instruments»NI FlexRIO**.



Note If you are not using an adapter module, skip step 5.

5. Install NI FlexRIO Adapter Module Support. Refer to the *NI FlexRIO Adapter Module Support Readme* on the NI FlexRIO Adapter Module Support installation media for system requirements and installation instructions.

Documentation for NI FlexRIO Adapter Module Support is available at ni.com/manuals and by selecting **Start»All Programs»National Instruments»NI FlexRIO**.

Related Information

[Installing the NI FlexRIO FPGA Module](#) on page 7

[Required Components](#) on page 4

[NI FlexRIO FPGA Module Signals](#) on page 9

Installing the NI FlexRIO Devices



Note You must install the software before installing the hardware.

Unpacking

The NI PXIe-7966 modules ship in antistatic packages to prevent electrostatic discharge from damaging module components. To prevent such damage when handling the modules, ground yourself using a grounding strap or by holding a grounded object, such as your computer chassis, and complete the following steps:

1. Touch the antistatic package to a metal part of the computer chassis before removing the module from the package.



Caution Never touch the exposed pins of connectors.

2. Remove each module from the package and inspect it for loose components or any other sign of damage.

Notify NI if the modules appear damaged in any way. Do not install a damaged module into the chassis.

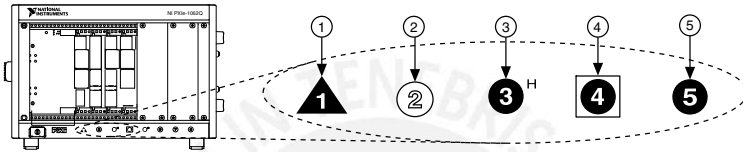
Installing the NI FlexRIO FPGA Module



Note You must install the software before you install the hardware.

1. Power off and unplug the PXI Express chassis. Refer to your chassis manual to install or configure the chassis.
2. Identify a supported PXI Express slot in the chassis. The figure below shows the symbols that indicate the slot types in a PXI Express chassis.

Figure 3. Symbols for PXI Express Slots

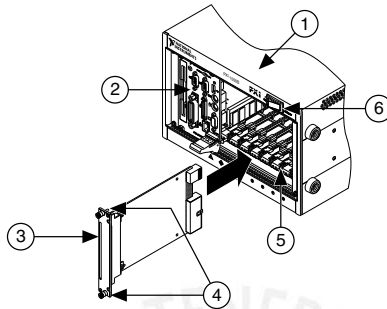


- | | |
|---------------------------------------|-----------------------------------|
| 1. PXI Express System Controller Slot | 4. PXI Express System Timing Slot |
| 2. PXI Peripheral Slot | 5. PXI Express Peripheral Slot |
| 3. PXI Express Hybrid Peripheral Slot | |

If you are using a PXI Express chassis, you can place PXI devices in the PXI slots. If a PXI device is hybrid slot compatible, you can use the PXI Express Hybrid slots. PXI Express devices can be placed only in PXI Express slots and PXI Express Hybrid slots. Refer to the chassis documentation for details.

3. Remove the filler panel of an unused PXI Express slot.
4. Touch any metal part of the chassis to discharge any static electricity. Place the PXI Express module edges into the module guides at the top and bottom of the chassis, and slide the module into the chassis until the module is fully inserted, as shown in the figure below.

Figure 4. Installing an NI FlexRIO FPGA Module in the PXI Express Chassis



- | | |
|--------------------------------------|--------------------------------|
| 1. PXI/PXI Express Chassis | 4. Front-Panel Mounting Screws |
| 2. PXI/PXI Express System Controller | 5. Module Guides |
| 3. NI FlexRIO FPGA Module | 6. Power Switch |

5. Secure the device front panel to the chassis front panel mounting rail using the front panel mounting screws.
6. Plug in and power on the PXI Express chassis.

Related Information

[Installing the Application Software and Driver](#) on page 5

Confirming that Measurement & Automation Explorer (MAX) Recognizes the Device

Use Measurement & Automation Explorer (MAX) to configure your National Instruments hardware. MAX informs other programs about which devices reside in the system and how they are configured. MAX is automatically installed with NI FlexRIO Support.

1. Launch MAX by navigating to **Start»All Programs»NI MAX** or by clicking the NI MAX desktop icon.
2. In the Configuration pane, double-click **Devices and Interfaces** to see the list of installed devices. Installed devices appear under the name of their associated chassis.
3. Expand your **Chassis** tree item. MAX lists all devices installed in the chassis. Your default device names may vary.



Note If you do not see your hardware listed, press <F5> to refresh the list of installed devices. If the device is still not listed, power off the system, ensure the device is correctly installed, and restart.

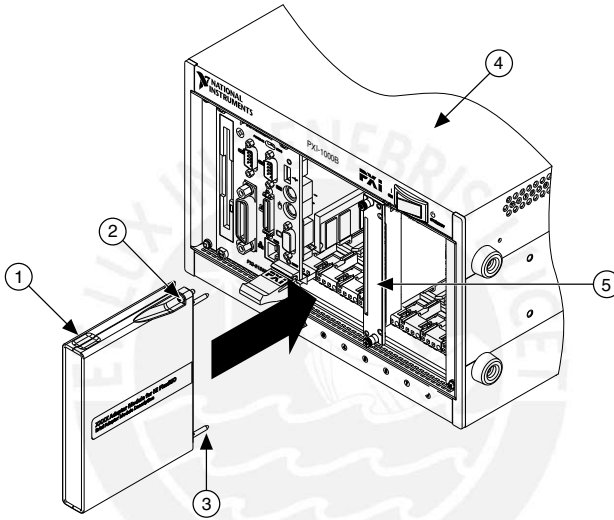
Installing the NI FlexRIO Adapter Module



Note Skip this step if you are not using an adapter module.

1. Gently insert the guide pins and the high-density card edge of the NI FlexRIO adapter module into the corresponding connectors of the NI FlexRIO FPGA module, as shown in the figure below. The connection may be tight, but do not force the adapter module into place.

Figure 5. Installing the NI FlexRIO Adapter Module



- | | |
|------------------------------|----------------------------|
| 1. NI FlexRIO Adapter Module | 4. PXI/PXI Express Chassis |
| 2. Captive Screw | 5. NI FlexRIO FPGA Module |
| 3. Guide Pin | |

2. Tighten the captive screws on the NI FlexRIO adapter module to secure it to the NI FlexRIO FPGA module. NI recommends using the laser-tipped screwdriver (part number 748677-01) included in the NI PXIe-7966R packaging.
3. Launch LabVIEW to begin configuring your NI FlexRIO system.

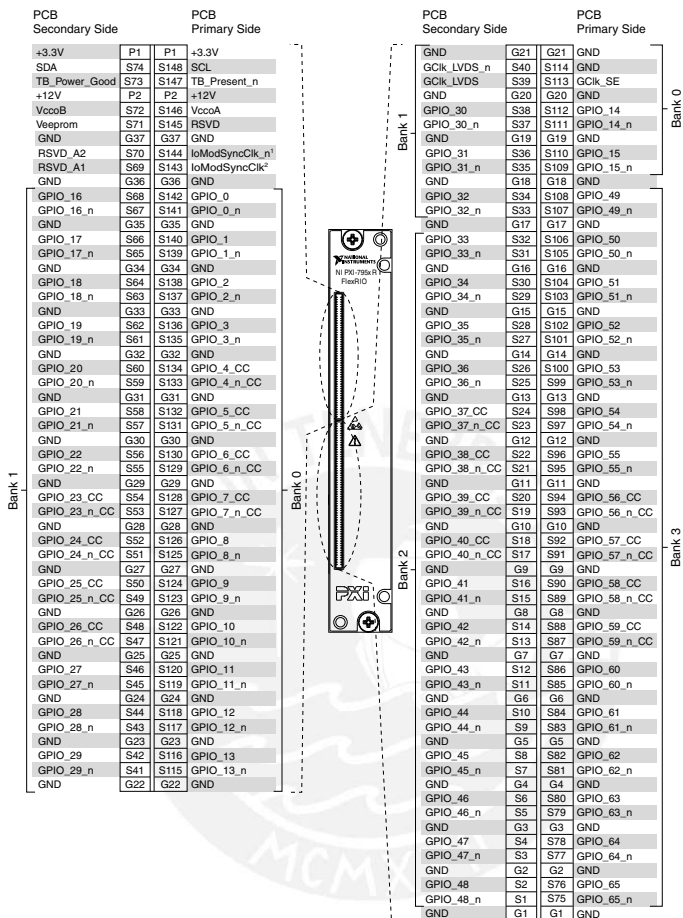


Note MAX only recognizes FPGA modules that are in the chassis. Your adapter module will not appear in MAX.

NI FlexRIO FPGA Module Signals

The figure below shows the available signals on the NI FlexRIO FPGA module. Refer to your adapter module specifications for your adapter module pinout.

Figure 6. NI FlexRIO FPGA Module Front Connector Pin Assignments and Locations



Related Information

[Installing the Application Software and Driver](#) on page 5
[Specifications](#) on page 11

Specifications

This section lists the specifications for your NI FlexRIO FPGA module. Refer to your adapter module documentation for the adapter module specifications.



Note Typical values are representative of an average unit operating at room temperature. These specifications are typical at 25 °C unless otherwise noted.

Related Information

[NI FlexRIO FPGA Module Signals](#) on page 9

Reconfigurable FPGA

FPGA.....	Virtex-5 SX95T
LUTs.....	58,880
DSP48 Slices (25 × 18 Multiplier).....	640
Embedded Block RAM (kbits).....	8,784
Default timebase.....	40 MHz
Timebase reference sources.....	PXI Express 100 MHz (PXIe_CLK100)
Timebase accuracy.....	±50 ppm, 250 ps peak-to-peak jitter
Data transfers.....	DMA, interrupts, programmed I/O
Number of channels.....	16
DMA interrupts.....	32 interrupt channels numbered 0-31

FPGA Digital Input/Output

Number of general-purpose channels.....	132, configurable as 132 single-ended, 66 differential, or a combination of both ²
Channels per bank	
Bank 0/Bank 2.....	32, single-ended per bank
Bank 1/Bank 3.....	34, single-ended per bank
Compatibility.....	Configured through the FPGA and based on the attached adapter module; 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V I/O standards (refer to www.xilinx.com)
Protection.....	Refer to www.xilinx.com

² The 132 channels span across four FPGA banks.

Current.....	Refer to www.xilinx.com
Maximum I/O data rates	
Single-ended.....	400 Mb/s for LVDCI25
Differential.....	1 Gb/s for LVDS
Global clock inputs.....	1 LVTTTL, 1 LVDS
Connection resources.....	PXI triggers, PXI_CLK10, PXI star trigger, PXIe_DStarA, PXIe_DStarB, PXIe_DStarC, and PXIe_Sync100

Onboard DRAM

Memory size.....	2 banks, 256 MB per bank
Maximum theoretical data rate.....	1.6 GB/s per bank

Bus Interface

PXI.....	Master, slave
PXI Express	
Form factor.....	x4 PXI Express, specification v1.0 compliant
Slot compatibility.....	x4, x8, and x16 PXI Express or PXI Express hybrid slots

Maximum Power Requirements



Note Power requirements are dependent on the adapter module and contents of the LabVIEW FPGA VI used in your application.

+3.3 VDC (±5%).....	3 A
+12 V.....	2 A

Physical

Dimensions (not including connectors).....	16.1 cm × 10.8 cm (6.3 in. × 4.3 in.)
Weight.....	213 g (7.5 oz)
I/O connector.....	High-density card edge

Clean the hardware with a soft, nonmetallic brush. Make sure that the hardware is completely dry and free from contaminants before returning it to service.

Maximum Working Voltage



Note Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel-to-earth.....0 V to 3.3 V, Measurement Category I

Channel-to-channel.....0 V to 3.3 V, Measurement Category I



Caution Do not use this device for connecting to signals in Measurement Categories II, III, or IV.



Note Measurement Categories CAT I and CAT O (Other) are equivalent. These test and measurement circuits are not intended for direct connection to the MAINS building installations of Measurement Categories CAT II, CAT III, or CAT IV.

Environment

Maximum altitude.....2,000 m (at 25 °C ambient temperature)

Pollution Degree.....2

Indoor use only.

Operating Environment

Ambient temperature range.....0 °C to 55 °C (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.)

Relative humidity range.....10% to 90%, noncondensing (Tested in accordance with IEC-60068-2-56.)

Storage Environment

Ambient temperature range.....-20 °C to 70 °C (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.)

Relative humidity range.....5% to 95%, noncondensing (Tested in accordance with IEC-60068-2-56.)

Operational shock.....30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)

Random vibration

Operating.....	5 Hz to 500 Hz, 0.3 g _{rms}
Nonoperating.....	5 Hz to 500 Hz, 2.4 g _{rms} (Tested in accordance with IEC-60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Compliance and Certifications

Safety

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1



Note For UL and other safety certifications, refer to the product label or the [Online Product Certification](#) section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions



Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.



Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.



Note For EMC declarations, certifications, and additional information, refer to the [Online Product Certification](#) section.

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This product meets the essential requirements of applicable European Directives, as follows:

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PXI Express™

NI PXIe-1085 Series User Manual



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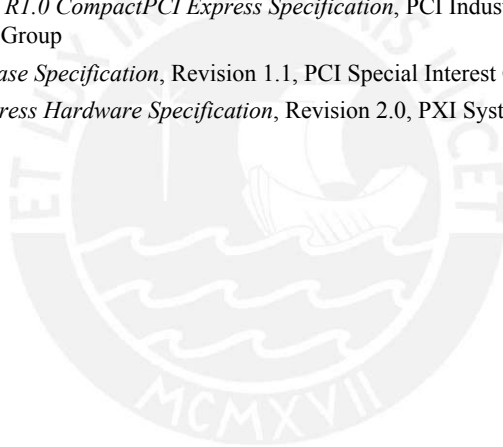
About This Manual

The *NIPXIe-1085 Series User Manual* describes the features of the NI PXIe-1085 Series chassis and contains information about configuring the chassis, installing the modules, and operating the chassis.

Related Documentation

The following documents contain information that you might find helpful as you read this manual:

- IEEE 1101.1-1991, *IEEE Standard for Mechanical Core Specifications for Microcomputers Using IEC 603-2 Connectors*
- IEEE 1101.10, *IEEE Standard for Additional Mechanical Specifications for Microcomputers Using IEEE 1101.1 Equipment Practice*
- *PICMG EXP.0 R1.0 CompactPCI Express Specification*, PCI Industrial Computers Manufacturers Group
- *PCI Express Base Specification*, Revision 1.1, PCI Special Interest Group
- *PXI-5 PXI Express Hardware Specification*, Revision 2.0, PXI Systems Alliance



Getting Started

This chapter describes the key features of the NI PXIe-1085 Series chassis and lists the kit contents and optional equipment you can order from National Instruments.

Unpacking

Carefully inspect the shipping container and the chassis for damage. Check for visible damage to the metal work. Check to make sure all handles, hardware, and switches are undamaged. Inspect the inner chassis for any possible damage, debris, or detached components. If damage appears to have been caused during shipment, file a claim with the carrier. Retain the packing material for possible inspection and/or reshipment.

What You Need to Get Started

The NI PXIe-1085 Series chassis kit contains the following items:

- NI PXIe-1085 12 GB/s chassis or NI PXIe-1085 24 GB/s chassis
- Filler panels
- AC power cable—refer to Table 1-1 for AC power cables
- NI PXIe-1085 Series User Manual*
- Software media with *PXI Platform Services 3.0* or higher
- Chassis number labels
- Screw to permanently restrain the front panel
- Eight-position connector for remote voltage monitoring and control

Table 1-1. AC Power Cables

Power Cable	Reference Standards
Standard 120 V (USA)	ANSI C73.11/NEMA 5-15-P/IEC83
Switzerland 220 V	SEV
Australia 240 V	AS C112
Universal Euro 230 V	CEE (7), II, IV, VII IEC83
United Kingdom 230 V	BS 1363/IEC83

If you are missing any of the items listed in Table 1-1, or if you have the incorrect AC power cable, contact National Instruments.

Key Features

The NI PXIe-1085 Series chassis combines a high-performance 18-slot PXI Express backplane with a high-output power supply and a structural design that has been optimized for maximum usability in a wide range of applications. The chassis' modular design ensures a high level of maintainability, resulting in a very low mean time to repair (MTTR). The NI PXIe-1085 Series chassis fully complies with the *PXI-5 PXI Express Hardware Specification*, offering advanced timing and synchronization features.

The key features of the NI PXIe-1085 Series chassis include the following:

High Performance for Instrumentation Requirements

- **NI PXIe-1085 12 GB/s chassis**—Up to 4 GB/s (single direction) per PXI Express slot dedicated bandwidth (x8 Gen-2 PCI Express).
- **NI PXIe-1085 24 GB/s chassis**—Up to 8 GB/s (single direction) per PXI Express slot dedicated bandwidth (x8 Gen-3 PCI Express).
- 38.25 W per slot cooling meets increased PXI Express cooling requirements
- Low-jitter internal 10 MHz reference clock for PXI/PXI Express slots with ± 25 ppm stability
- Low-jitter internal 100 MHz reference clock for PXI Express slots with ± 25 ppm stability
- Quiet operation for 0 to 30 °C at 51.2 dBA
- Variable speed fan controller optimizes cooling and acoustic emissions
- Remote power-inhibit control
- Complies with PXI and CompactPCI Specifications

High Reliability

- 0 to 55 °C extended temperature range
- Power supply, temperature, and fan monitoring
- Field replaceable power supply and fans

Multi-Chassis Support

- PXI Express System Timing Slot for tight synchronization across chassis
- Front panel CLK10 I/O connectors
- Switchless CLK10 routing

Optional Features

- Front and rear rack-mount kits
- Replacement power supply
- EMC filler panels
- Slot blockers for improved cooling performance
- Factory installation services
- Replacement fan modules

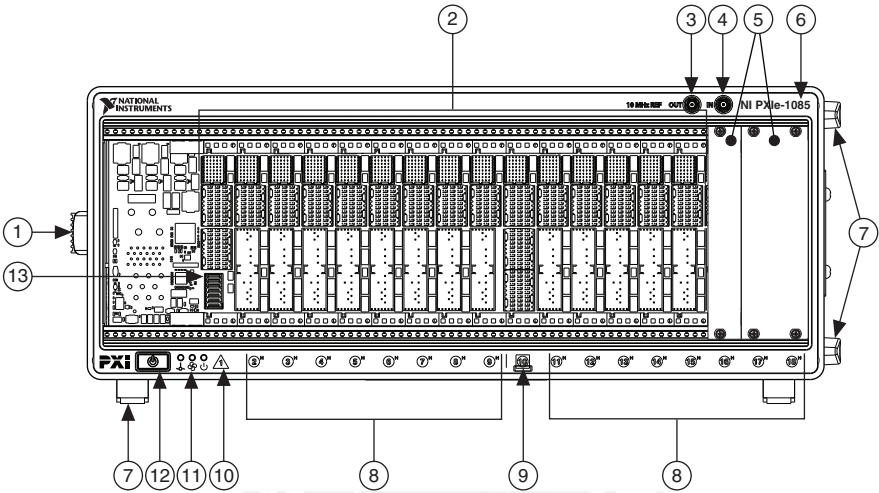
Chassis Description

Figures 1-1 and 1-2 show the key features of the NI PXIe-1085 Series chassis front and back panels. Figure 1-1 shows the front view of the series chassis. Figure 1-2 shows the rear view of the series chassis.



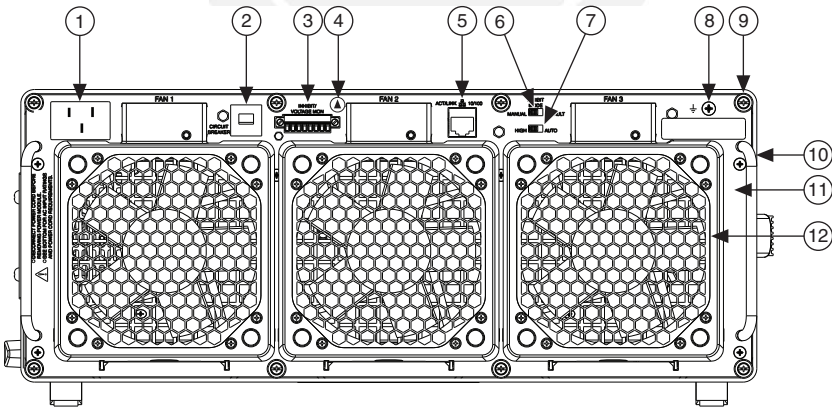
Note The NI PXIe-1085 24 GB/s chassis can be identified by the blue **24 GB/s** graphic to the left of the 10 MHz REF OUT SMA connector. The NI PXIe-1085 12 GB/s chassis does not have this mark.

Figure 1-1. Front View of the NI PXIe-1085 Series Chassis



- | | |
|------------------------|---|
| 1 Chassis Carry Handle | 8 PXI Express Hybrid Peripheral Slots (16x) |
| 2 Backplane Connectors | 9 PXI Express System Timing Slot |
| 3 10 MHz REF OUT SMA | 10 PXI Express System Controller Slot |
| 4 10 MHz REF IN SMA | 11 Temperature, Fan, and Power LEDs |
| 5 PXI Filler Panels | 12 Power Inhibit Switch |
| 6 Chassis Model Name | 13 System Controller Expansion Slot |
| 7 Removable Feet | |

Figure 1-2. Rear View of the NI PXIe-1085 Series Chassis



- | | |
|---|---|
| 1 Universal AC Input | 7 Fan Speed Selector Switch |
| 2 Push-Reset Circuit Breaker | 8 Chassis Ground Screw |
| 3 Remote Inhibit and Voltage Monitoring Connector | 9 Power Supply Shuttle Mounting Screws (8x) |
| 4 Electrostatic-Sensitive Device Symbol | 10 Power Supply Shuttle Handle (2x) |
| 5 Ethernet Port | 11 Power Supply Shuttle |
| 6 Inhibit Mode Selector Switch | 12 Fan Module (3x) |

Optional Equipment

Contact National Instruments to order the following options for the NI PXIe-1085 Series chassis.

EMC Filler Panels

Optional EMC filler panel kits are available from National Instruments.

Rack Mount Kit

There are two required kits for mounting the NI PXIe-1085 Series chassis into a rack. The first is a pair of mounting brackets for use on the front of the chassis. The second is a rear rack mount kit. For more information, refer to Figure A-3, *NI Chassis Rack Mount Kit Components*.

Slot Blockers

Optional PXI Slot Blocker kits are available from National Instruments for improved thermal performance when all slots are not used.

Replacement Power Supply

Optional replacement power supply kits are available from National Instruments. You easily can install replacement power supplies without the use of tools.

Replacement Fan Modules

Optional replacement fan modules are available from National Instruments. You easily can install fans in seconds without the use of tools and without powering down the system.

NI PXIe-1085 Series Backplane Overview

This section provides an overview of the backplane features for the NI PXIe-1085 Series chassis.



Note The differences between the NI PXIe-1085 12 GB/s chassis and the NI PXIe-1085 24 GB/s chassis are noted where applicable.

Interoperability with CompactPCI

The design of the NI PXIe-1085 Series chassis provides you the flexibility to use the following devices in a single PXI Express chassis:

- PXI Express compatible products
- CompactPCI Express compatible 2-Link system controller products
- CompactPCI Express compatible Type-2 peripheral products
- PXI peripheral products modified to fit in a hybrid slot
- Standard CompactPCI peripheral products modified to fit in a hybrid slot

System Controller Slot

NI PXIe-1085 12 GB/s

The system controller slot is Slot 1 of the chassis and is a 2-Link configuration system slot as defined by the CompactPCI Express and PXI Express specifications. It has three system controller expansion slots for system controller modules that are wider than one slot. These slots allow the system controller to expand to the left to prevent the system controller from using peripheral slots.

The backplane connects the system slot to two PCI Express switches using a Gen-2 x8 and a Gen-2 x16 PCI Express link. These switches distribute PCI Express connections to the peripheral slots and to two PCI Express-to-PCI bridges to provide PCI buses to the hybrid peripheral slots. Refer to Figure 1-3 for an overview of the NI PXIe-1085 Series architecture.

System slot link 1 is a Gen-2 x8 PCI Express link to PCI Express switch 1, providing a nominal bandwidth of 4 GB/s (single direction) between the system controller and PCI Express switch 1. PXI Express peripheral slots 2-10 are connected to PCI Express switch 1 with Gen-2 x8 PCI Express links and are downstream of system slot link 1. PCI Express-to-PCI bridge 1 is connected to PCI Express switch 1 and provides a 32-bit, 33 MHz PCI bus for hybrid peripheral slots 2-9.

System slot link 2 is a Gen-2 x16 PCI Express link to PCI Express switch 2, providing a nominal bandwidth of 8 GB/s (single direction) between the system controller slot and PCI Express switch 2. PXI Express peripheral slots 11-18 are connected to PCI Express switch 2 with Gen-2 x8 PCI Express links and are downstream of system slot link 2. PCI Express-to-PCI bridge 2 is connected to PCI Express switch 2 and provides a 32-bit, 33 MHz PCI bus for hybrid peripheral slots 11-18.

The system controller slot also has connectivity to some PXI features such as: PXI_CLK10, PXI Star, PXI Trigger Bus and PXI Local Bus 6.

By default, the system controller will control the power supply with the PS_ON# signals. A logic low on this line will turn the power supply on.



Note The Inhibit Mode switch on the rear of the chassis must be in the **Default** position for the system controller to have control of the power supply. Refer to the [Inhibit Mode Switch](#) section of Chapter 2, *Installation and Configuration*, for details about the Inhibit Mode switch.

NI PXIe-1085 24 GB/s

The system controller slot is Slot 1 of the chassis and is a 2-Link configuration system slot as defined by the CompactPCI Express and PXI Express specifications. It has three system controller expansion slots for system controller modules that are wider than one slot. These slots allow the system controller to expand to the left to prevent the system controller from using peripheral slots.

The backplane connects the system slot to two PCI Express switches using a Gen-3 x8 and a Gen-3 x16 PCI Express link. These switches distribute PCI Express connections to the peripheral slots and to two PCI Express-to-PCI bridges to provide PCI buses to the hybrid peripheral slots. Refer to Figure 1-3 for an overview of the NI PXIe-1085 Series architecture.

System slot link 1 is a Gen-3 x8 PCI Express link to PCI Express switch 1, providing a nominal bandwidth of 8 GB/s (single direction) between the system controller and PCI Express switch 1. PXI Express peripheral slots 2-10 are connected to PCI Express switch 1 with Gen-3 x8 PCI Express links and are downstream of system slot link 1. PCI Express-to-PCI bridge 1 is connected to PCI Express switch 1 and provides a 32-bit, 33 MHz PCI bus for hybrid peripheral slots 2-9. PCI Express switch 1 also is connected to PCI Express switch 2 with a Gen-3 x8 PCI Express link for advanced backplane configurations.

System slot link 2 is a Gen-3 x16 PCI Express link to PCI Express switch 2, providing a nominal bandwidth of 16 GB/s (single direction) between the system controller slot and PCI Express switch 2. PXI Express peripheral slots 11-18 are connected to PCI Express switch 2 with Gen-3 x8 PCI Express links and are downstream of system slot link 2. PCI Express-to-PCI bridge 2 is connected to PCI Express switch 2 and provides a 32-bit, 33 MHz PCI bus for hybrid peripheral slots 11-18. PCI Express switch 2 also is connected to PCI Express switch 1 with a Gen-3 x8 PCI Express link for advanced backplane configurations.

The system controller slot also has connectivity to some PXI features such as: PXI_CLK10, PXI Star, PXI Trigger Bus and PXI Local Bus 6.

By default, the system controller will control the power supply with the PS_ON# signals. A logic low on this line will turn the power supply on.



Note The Inhibit Mode switch on the rear of the chassis must be in the Default position for the system controller to have control of the power supply. Refer to the [Inhibit Mode Switch](#) section of Chapter 2, *Installation and Configuration*, for details about the Inhibit Mode switch.

Hybrid Peripheral Slots

The chassis provides 16 hybrid peripheral slots as defined by the *PXI-5 PXI Express Hardware Specification*: slots 2-9 and slots 11-18. A hybrid peripheral slot can accept the following peripheral modules:

- **NI PXIe-1085 12 GB/s**—A PXI Express peripheral with x8, x4, or x1 PCI Express link through a switch to the system slot. Each PXI Express peripheral slot can link up to a Gen-2 x8 PCI Express, providing a maximum nominal single-direction bandwidth of 4 GB/s.
- **NI PXIe-1085 24 GB/s**—A PXI Express peripheral with x8, x4, or x1 PCI Express link through a switch to the system slot. Each PXI Express peripheral slot can link up to a Gen-3 x8 PCI Express, providing a maximum nominal single-direction bandwidth of 8 GB/s.
- A CompactPCI Express Type-2 Peripheral with x8, x4, or x1 PCI Express link through a switch to the system slot.
- A hybrid-compatible PXI Peripheral module that has been modified by replacing the J2 connector with an XJ4 connector installed in the upper eight rows of J2. Refer to the *PXI Express Specification* for details. The PXI Peripheral communicates through the backplane’s 32-bit PCI bus.
- A CompactPCI 32-bit peripheral on the backplane’s 32-bit PCI bus.

The hybrid peripheral slots provide full PXI Express functionality and 32-bit PXI functionality except for PXI Local Bus. The hybrid peripheral slot only connects to PXI Local Bus 6 left and right.

Figure 1-3. NI PXIe-1085 12 GB/s PCI Express Backplane Diagram

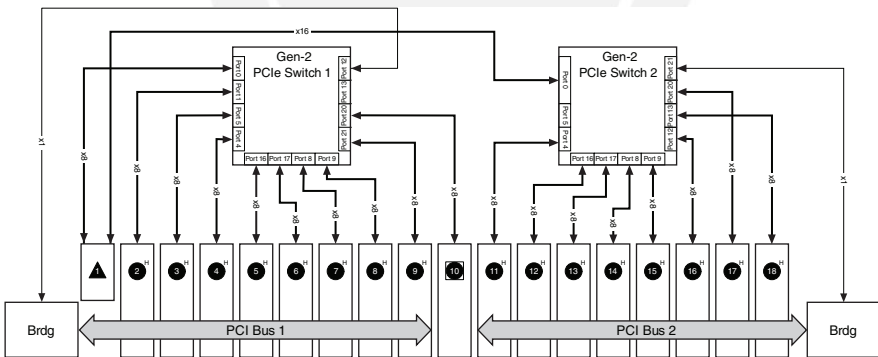
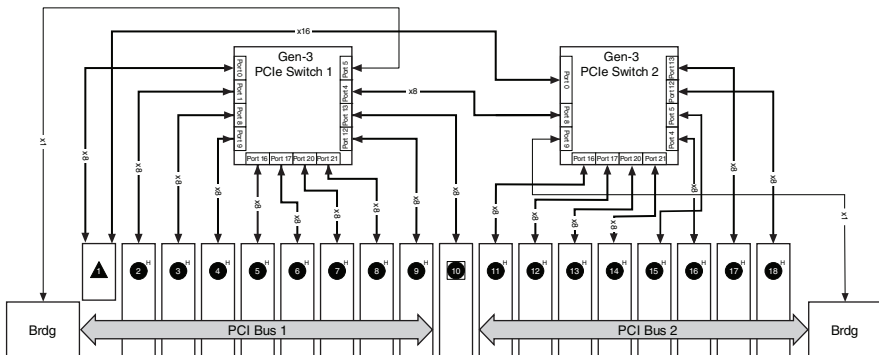


Figure 1-4. NI PXIe-1085 24 GB/s PCI Express Backplane Diagram

System Timing Slot

The System Timing Slot is slot 10. The system timing slot will accept the following peripheral modules:

- **NI PXIe-1085 12 GB/s**—A PXI Express System Timing Module with x8, x4, or x1 PCI Express link to the system slot through a PCI Express switch. Each PXI Express peripheral slot can link up to a Gen-2 x8 PCI Express, providing a maximum nominal single-direction bandwidth of 4 GB/s.
- **NI PXIe-1085 24 GB/s**—A PXI Express System Timing Module with x8, x4, or x1 PCI Express link to the system slot through a PCI Express switch. Each PXI Express peripheral slot can link up to a Gen-3 x8 PCI Express, providing a maximum nominal single-direction bandwidth of 8 GB/s.
- A PXI Express Peripheral with x8, x4, or x1 PCI Express link to the system slot through a PCI Express switch.
- A CompactPCI Express Type-2 Peripheral with x8, x4, or x1 PCI Express link to the system slot through a PCI Express switch.

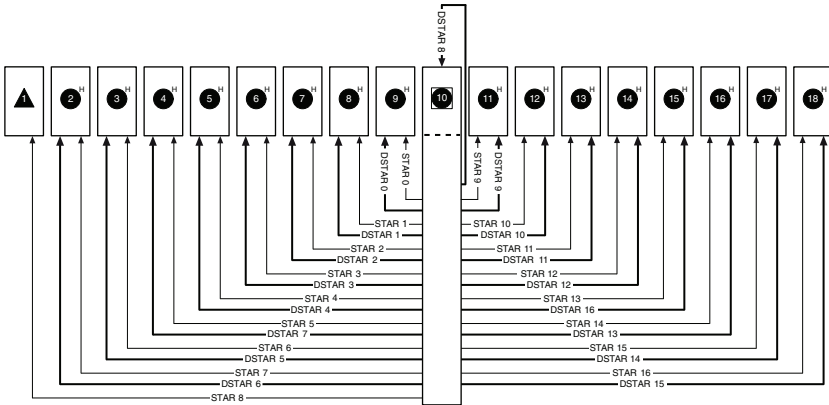
The system timing slot has 3 dedicated differential pairs (PXIe_DSTAR) connected from the TP1 and TP2 connectors to the XP3 connector for each PXI Express hybrid peripheral slot, as well as routed back to the XP3 connector of the system timing slot as shown in Figure 1-5. The PXIe_DSTAR pairs can be used for high-speed triggering, synchronization and clocking. Refer to the *PXI Express Specification* for details.

The system timing slot also has a single-ended (PXI Star) trigger connected to every slot. Refer to Figure 1-5 for details.

The system timing slot has a pin (PXI_CLK10_IN) through which a system timing module may source a 10 MHz clock to which the backplane will phase-lock. Refer to the [System Reference Clock](#) section for details.

The system timing slot has a pin (PXIe_SYNC_CTRL) through which a system timing module can control the PXIe_SYNC100 timing. Refer to the *PXI Express Specification* and the *PXIe_SYNC_CTRL* section of this chapter for details.

Figure 1-5. PXI Express Star Connectivity Diagram



PXI Local Bus

The PXI backplane local bus is a daisy-chained bus that connects each peripheral slot with adjacent peripheral slots to the left and right, as shown in Figure 1-6.

The backplane routes PXI Local Bus 6 between all slots. The left local bus 6 from slot 1 is not routed anywhere and the right local bus signals from slot 18 are not routed anywhere.

Local bus signals may range from high-speed TTL signals to analog signals as high as 42 V.

Initialization software uses the configuration information specific to each adjacent peripheral module to evaluate local bus compatibility.

PXI Trigger Bus

All slots on the same PXI bus segment share eight PXI trigger lines. You can use these trigger lines in a variety of ways. For example, you can use triggers to synchronize the operation of several different PXI peripheral modules. In other applications, one module located in the system timing slot can control carefully timed sequences of operations performed on other modules in the system. Modules can pass triggers to one another, allowing precisely timed responses to asynchronous external events the system is monitoring or controlling.

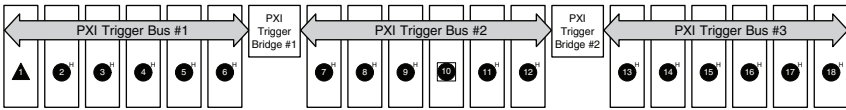
The PXI trigger lines from adjacent PXI trigger bus segments can be routed in either direction across the PXI trigger bridges through buffers. This allows you to send trigger signals to, and receive trigger signals from, every slot in the chassis. Static trigger routing (user-specified line and directional assignments) can be configured through Measurement & Automation Explorer

(MAX). Dynamic routing of triggers (automatic line assignments) is supported through certain National Instruments drivers like NI-DAQmx.



Note Although any trigger line may be routed in either direction, it cannot be routed in more than one direction at a time.

Figure 1-6. PXI Trigger Bus Connectivity Diagram



System Reference Clock

The NI PXIe-1085 Series chassis supplies PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 independently driven to each peripheral slot.

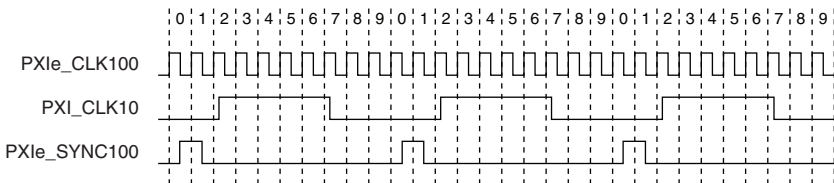
An independent buffer (having a source impedance matched to the backplane and a skew of less than 1 ns between slots) drives PXI_CLK10 to each slot. You can use this common reference clock signal to synchronize multiple modules in a measurement or control system.

An independent buffer drives PXIe_CLK100 to each peripheral slot. These clocks are matched in skew to less than 100 ps. The differential pair must be terminated on the peripheral with LVPECL termination for the buffer to drive PXIe_CLK100 so that when there is no peripheral or a peripheral that does not connect to PXIe_CLK100, there is no clock being driven on the pair to that slot.

An independent buffer drives PXIe_SYNC100 to each peripheral slot. The differential pair must be terminated on the peripheral with LVPECL termination for the buffer to drive PXIe_SYNC100 so that when there is no peripheral or a peripheral that does not connect to PXIe_SYNC100, there is no SYNC100 signal being driven on the pair to that slot.

PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 have the default timing relationship described in Figure 1-7.

Figure 1-7. System Reference Clock Default Behavior



To synchronize the system to an external clock, you can drive PXI_CLK10 from an external source through the PXI_CLK10_IN pin on the System Timing Slot. Refer to Table B-8, *XP4 Connector Pinout for the System Timing Slot*, for the pinout. When a 10MHz clock is detected

on this pin, the backplane automatically phase-locks the PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 signals to this external clock and distributes these signals to the slots. Refer to Appendix A, *Specifications*, for the specification information for an external clock provided on the PXI_CLK10_IN pin of the system timing slot.

You also can drive a 10 MHz clock on the 10 MHz REF IN connector on the front panel of the chassis. When a 10 MHz clock is detected on this connector, the backplane automatically phase-locks the PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 signals to this external clock and distributes these signals to the slots. Refer to Appendix A, *Specifications*, for the specification information for an external clock provided on the 10 MHz REF IN connector on the front panel of the chassis.

If the 10 MHz clock is present on both the PXI_CLK10_IN pin of the System Timing Slot and the 10 MHz REF IN connector on the front of the chassis, the signal on the System Timing Slot is selected. Refer to Table 1-2 which explains how the 10 MHz clocks are selected by the backplane.

Table 1-2. Backplane External Clock Input Truth Table

System Timing Slot PXI_CLK10_IN	Front Chassis Panel 10 MHz REF IN	Backplane PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100
No clock present	No clock present	Backplane generates its own clocks
No clock present	10 MHz clock present	PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 all phase-locked to Front Chassis Panel—10 MHz REF IN
10 MHz clock present	No clock present	PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 all phase-locked to System Timing Slot— PXI_CLK10_IN
10 MHz clock present	10 MHz clock present	PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 all phase-locked to System Timing Slot— PXI_CLK10_IN

A copy of the backplane's PXI_CLK10 is exported to the 10 MHz REF OUT connector on the front panel of the chassis. This clock is driven by an independent buffer. Refer to Appendix A, *Specifications*, for the specification information for the 10 MHz REF OUT signal on the front panel of the chassis.

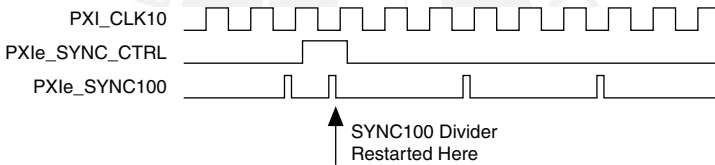
PXIe_SYNC_CTRL

PXIe_SYNC100 is by default a 10 ns pulse synchronous to PXI_CLK10. The frequency of PXIe_SYNC100 is $10/n$ MHz, where n is a positive integer. The default for n is 1, giving PXIe_SYNC100 a 100 ns period. However, the backplane allows n to be programmed to other integers. For instance, setting $n = 3$ gives a PXIe_SYNC100 with a 300 ns period while still maintaining its phase relationship to PXI_CLK10. The value for n may be set to any positive integer from 1 to 255.

The system timing slot has a control pin for PXIe_SYNC100 called PXIe_SYNC_CTRL for use when $n > 1$. Refer to Table B-7, *XP3 Connector Pinout for the System Timing Slot*, for system timing slot pinout. Refer to Appendix A, *Specifications*, for the PXIe_SYNC_CTRL input specifications.

By default, a high-level detected by the backplane on the PXIe_SYNC_CTRL pin causes a synchronous restart for the PXIe_SYNC100 signal. On the next PXI_CLK10 edge the PXIe_SYNC100 signal will restart. This will allow several chassis to have their PXIe_SYNC100 in phase with each other. Refer to Figure 1-8 for timing details with this method.

Figure 1-8. PXIe_SYNC100 at 3.33 MHz Using PXIe_SYNC_CTRL as Restart



Installation and Configuration

This chapter describes how to prepare and operate the NI PXIe-1085 Series chassis.

Before connecting the chassis to a power source, read this chapter and the *Read Me First: Safety and Electromagnetic Compatibility* document included with your kit.

Safety Information



Cautions Before undertaking any troubleshooting, maintenance, or exploratory procedure, carefully read the following caution notices.

Protection equipment may be impaired if equipment is not used in the manner specified.

This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.

- **Chassis Grounding**—The chassis requires a connection from the premise wire safety ground to the chassis ground. The earth safety ground must be connected during use of this equipment to minimize shock hazards. Refer to the [Connecting Safety Ground](#) section for instructions on connecting safety ground.
- **Live Circuits**—Operating personnel and service personnel *must* not remove protective covers when operating or servicing the chassis. Adjustments and service to internal components must be undertaken by qualified service technicians. During service of this product, the mains connector to the premise wiring must be disconnected. Dangerous voltages may be present under certain conditions; use extreme caution.
- **Explosive Atmosphere**—Do *not* operate the chassis in conditions where flammable gases are present. Under such conditions, this equipment is unsafe and may ignite the gases or gas fumes.
- **Part Replacement**—Only service this equipment with parts that are exact replacements, both electrically and mechanically. Contact National Instruments for replacement part information. Installation of parts with those that are not direct replacements may cause harm to personnel operating the chassis. Furthermore, damage or fire may occur if replacement parts are unsuitable.
- **Modification**—Do *not* modify any part of the chassis from its original condition. Unsuitable modifications may result in safety hazards.

Chassis Cooling Considerations

The NI PXIe-1085 Series chassis is designed to operate on a bench or in an instrument rack. The chassis must be oriented horizontally for benchtop use. Vertical orientation with the chassis handle up is not a supported configuration. Regardless of the configuration, you must provide the cooling clearances as outlined in the following sections.

Providing Adequate Clearance

The primary cooling exhaust vent for the NI PXIe-1085 Series is on the top of the chassis. The primary intake vent is on the rear of the chassis. The secondary intake and exhaust vents are located along the sides of the chassis. Adequate clearance between the chassis and surrounding equipment or blockages must be maintained to ensure proper cooling of the chassis power supply as well as the modules plugged into the chassis. These clearances are outlined in Figure 2-1. The vent locations for the NI PXIe-1085 Series chassis are shown in Figure 2-2. Failure to provide these clearances may result in thermal-related failures in the chassis or modules.

Figure 2-1. NI PXIe-1085 Series Chassis Cooling Clearances

Dimensions are in inches (millimeters)

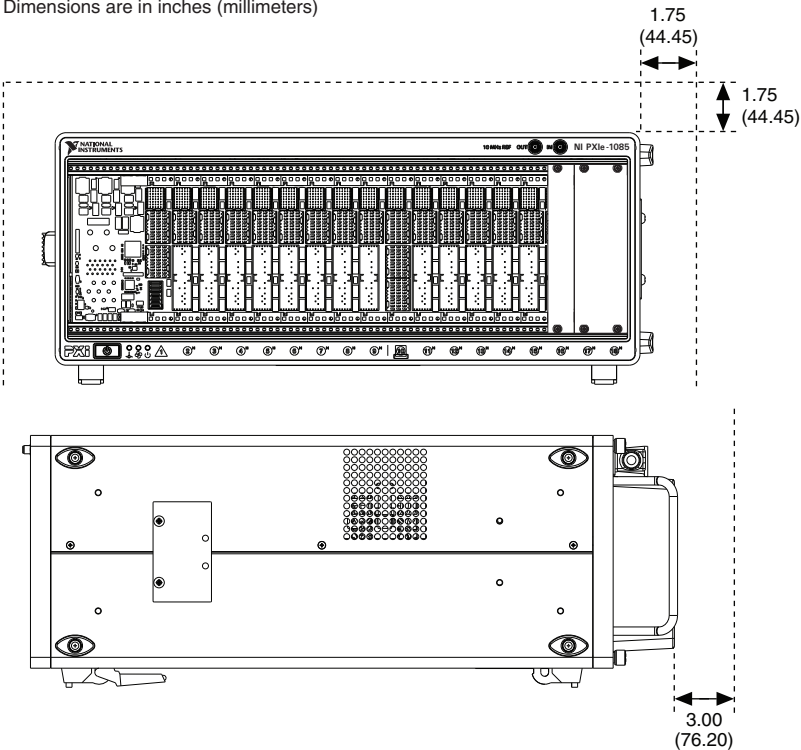
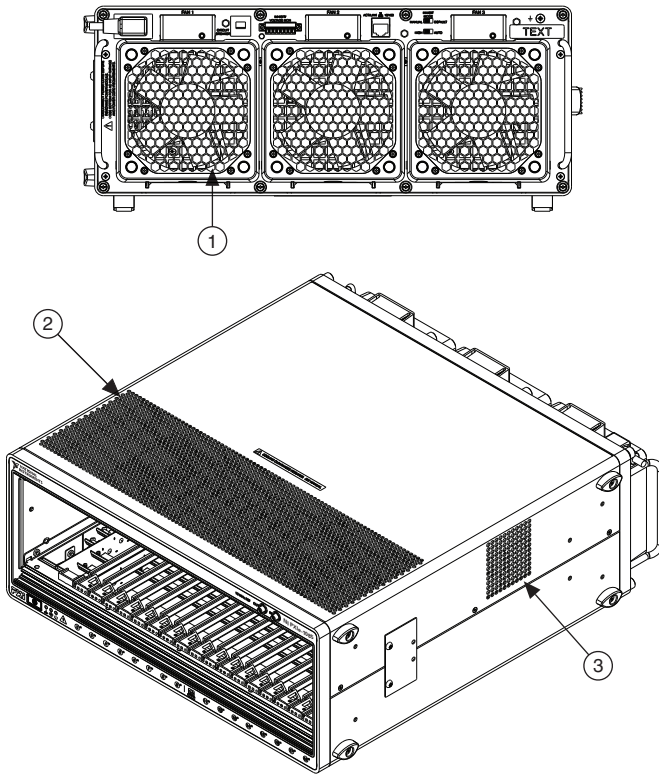


Figure 2-2. NI PXIe-1085 Series Chassis Vents



-
- | | |
|--------------------------------|---|
| 1 Primary Air Intake Vent (3x) | 3 Secondary Air Intake/Exhaust Vents (Both Sides) |
| 2 Primary Air Exhaust Vent | |
-

Chassis Ambient Temperature Definition

The chassis fan control system uses intake air temperature as the input for controlling fan speeds when in Auto Fan Speed mode. Because of this, the chassis ambient temperature is defined as the temperature that exists just outside of the fan intake vents on the rear of the chassis. Note that this temperature may be higher than ambient room temperature depending on the surrounding equipment and/or blockages present. It is the user's responsibility to ensure that this ambient temperature does not exceed the rated ambient temperature as stated in Appendix A, *Specifications*. If the temperature exceeds the stated spec, the temperature LED blinks red, as discussed in the *Front Panel and Fan Module LED Indicators* section of this chapter.

Setting Fan Speed

The fan-speed selector switch is on the rear panel of the NI PXIe-1085 Series chassis. Refer to Figure 1-2, *Rear View of the NI PXIe-1085 Series Chassis*, to locate the fan-speed selector switch. Select **High** for maximum cooling performance or **Auto** for improved acoustic performance. When set to **Auto**, the fan speed is determined by chassis intake air temperature.

Considerations for High Vibration Environment

For the best performance in a high vibration environment, tighten the modular power supply screws and the power supply shuttle mounting screws to 11.5 lb · in. (1.3 N · m) using a #2 Phillips screwdriver. See Figure 3-1, *Removing Power Supply Shuttle*, for screw locations.

Installing Filler Panels

To maintain proper module cooling performance, install filler panels (provided with the chassis) in unused or empty slots. Secure with the captive mounting screws provided.

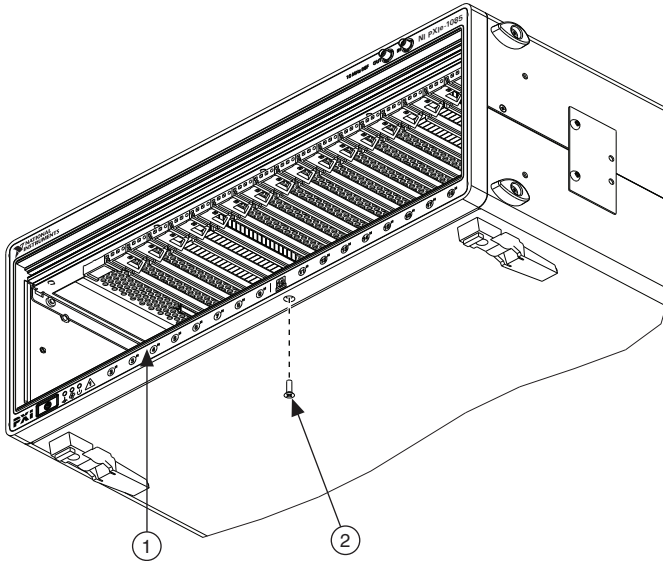
Installing Slot Blockers

The cooling performance of the chassis can be improved by installing optional slot blockers. Refer to ni.com for more details.

Securing Front Panel

To permanently secure the removable front panel, use the screw in the accessory kit. Attach the screw through the bottom of the front bezel using a #2 Phillips screwdriver, as shown in Figure 2-3.

Figure 2-3. Securing Removable Front Panel



1 Removable Front Panel

2 Screw to Secure Front Panel

Rack Mounting

Rack mount applications require the optional rack mount kits available from National Instruments. Refer to the instructions supplied with the rack mount kits to install your NI PXIe-1085 Series chassis in an instrument rack. Refer to Figure A-3, [NI Chassis Rack Mount Kit Components](#).



Note You may want to remove the feet from the NI PXIe-1085 Series chassis when rack mounting. To do so, remove the screws holding the feet in place.

Connecting Safety Ground



Caution The NI PXIe-1085 Series chassis are designed with a three-position NEMA 5-15 style plug for the U.S. that connects the ground line to the chassis ground. To minimize shock hazard, make sure the electrical power outlet you use to power the chassis has an appropriate earth safety ground.

If your power outlet does not have an appropriate ground connection, you must connect the premise safety ground to the chassis grounding screw located on the rear panel. Refer to Figure 1-2, *Rear View of the NI PXIe-1085 Series Chassis*, to locate the chassis grounding screw. To connect the safety ground, complete the following steps:

1. Connect a 16 AWG (1.3 mm) wire to the chassis grounding screw using a grounding lug. The wire must have green insulation with a yellow stripe or must be noninsulated (bare).
2. Attach the opposite end of the wire to permanent earth ground using toothed washers or a toothed lug.

Connecting to Power Source



Cautions Do *not* install modules prior to performing the following power-on test.

To completely remove power, you *must* disconnect the AC power cable.

Attach input power through the rear AC inlet using the appropriate AC power cable supplied. Refer to Figure 1-2, *Rear View of the NI PXIe-1085 Series Chassis*, to locate the AC inlet.

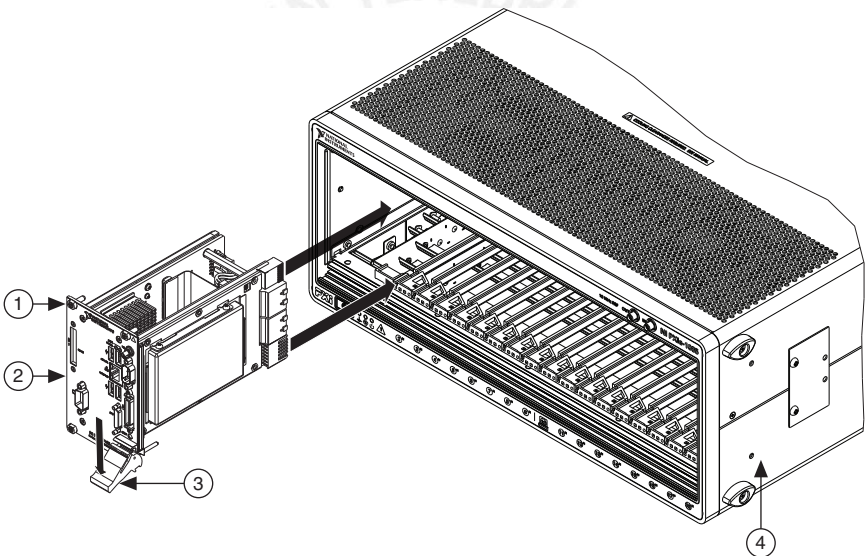
The Inhibit Mode switch allows you to power on the chassis or place it in standby mode. Set the Inhibit Mode switch on the back of the chassis to the **Manual** position. Observe that all fans become operational and all three front panel LEDs are a steady green. Switching the Inhibit Mode switch to the **Default** position allows the system controller to control the power supply.

Installing a PXI Express System Controller

This section contains general installation instructions for installing a PXI Express system controller in a NI PXIe-1085 Series chassis. Refer to your PXI Express system controller user manual for specific instructions and warnings. To install a system controller, complete the following steps:

1. Connect the AC power source to the PXI Express chassis before installing the system controller. The AC power cord grounds the chassis and protects it from electrical damage while you install the system controller.
2. Install the system controller into the system controller slot (slot 1, indicated by the red card guides) by first placing the system controller PCB into the front of the card guides (top and bottom). Slide the system controller to the rear of the chassis, making sure that the injector/ejector handle is pushed down as shown in Figure 2-4.

Figure 2-4. Installing a PXI Express System Controller

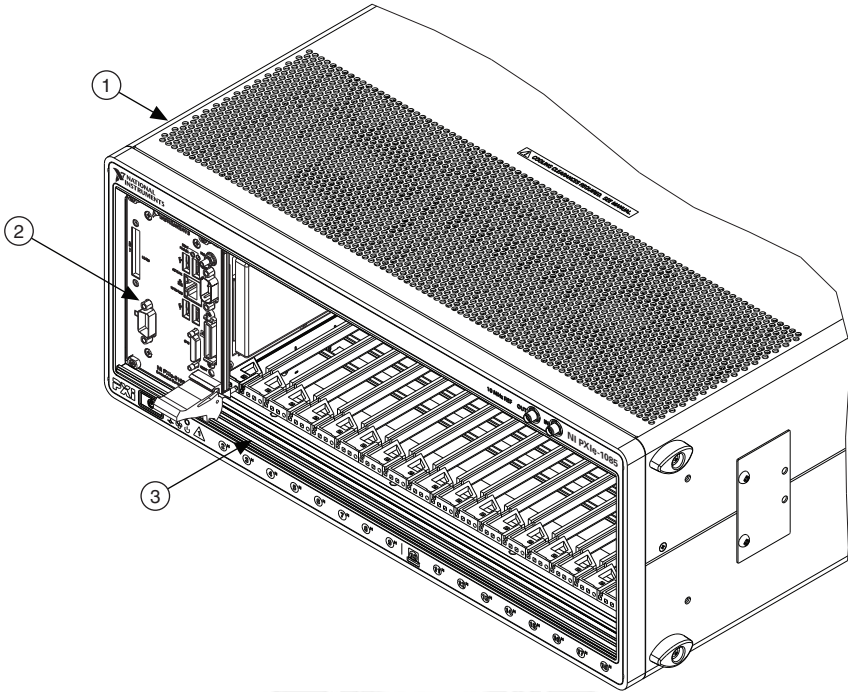


1 System Controller Front Panel Mounting Screws (4x)	3 Injector/Ejector Handle
2 NI PXI Express System Controller	4 NI PXIe-1085 Series Chassis

3. When you begin to feel resistance, pull up on the injector/ejector handle to seat the system controller fully into the chassis frame. Secure the system controller front panel to the chassis using the system controller front-panel mounting screws.
4. Connect the keyboard, mouse, and monitor to the appropriate connectors. Connect devices to ports as required by your system configuration.
5. Power on the chassis. Verify that the system controller boots. If the system controller does not boot, refer to your system controller user manual.

Figure 2-5 shows a PXI Express system controller installed in the system controller slot of a NI PXIe-1085 Series chassis. You can place CompactPCI, CompactPCI Express, PXI, or PXI Express modules in other slots depending on the slot type.

Figure 2-5. NI PXI Express System Controller Installed in a NI PXIe-1085 Series Chassis



1 NI PXIe-1085 Series Chassis 2 NI PXI Express System Controller 3 Injector/Ejector Rail

Installing Peripheral Modules



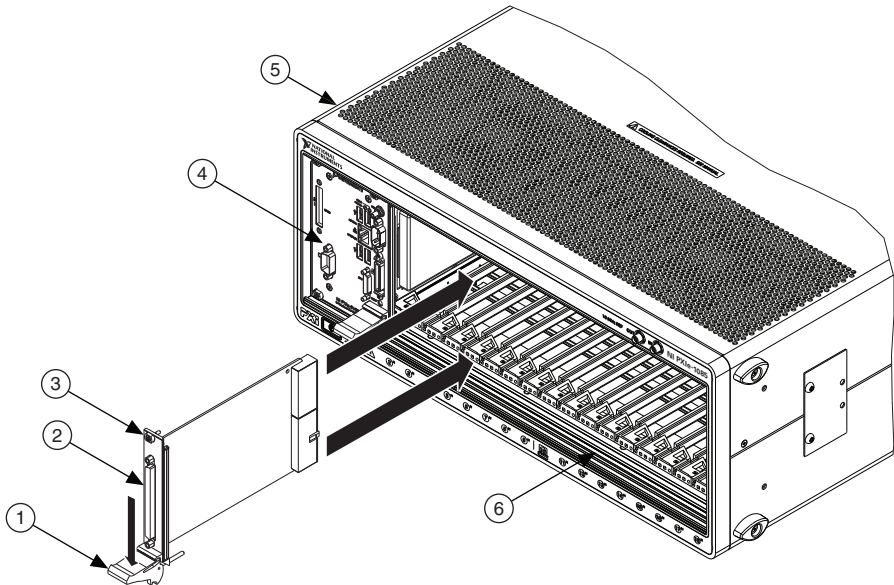
Caution The NI PXIe-1085 Series chassis has been designed to accept a variety of peripheral module types in different slots. To prevent damage to the chassis, ensure that the peripheral module is being installed into a slot designed to accept it. Refer to Chapter 1, [Getting Started](#), for a description of the various slot types.

This section contains general installation instructions for installing a peripheral module in a NI PXIe-1085 Series chassis. Refer to your peripheral module user manual for specific instructions and warnings. To install a module, complete the following steps:

1. Connect the AC power source to the PXI Express chassis before installing the module. The AC power cord grounds the chassis and protects it from electrical damage while you install the module.
2. Ensure that the chassis is powered off.

3. Install a module into a chassis slot by first placing the module card PCB into the front of the card guides (top and bottom), as shown in Figure 2-6. Slide the module to the rear of the chassis, making sure that the injector/ejector handle is pushed down as shown in Figure 2-6.
4. When you begin to feel resistance, push up on the injector/ejector handle to fully seat the module into the chassis frame. Secure the module front panel to the chassis using the module front-panel mounting screws.

Figure 2-6. Installing PXI, PXI Express, or CompactPCI Peripheral Modules



- | | | | |
|---|--|---|----------------------------------|
| 1 | Injector/Ejector Handle | 4 | NI PXI Express System Controller |
| 2 | PXI Peripheral Module | 5 | NI PXIe-1085 Series Chassis |
| 3 | Peripheral Module Front Panel Mounting Screws (2x) | 6 | Injector/Ejector Rail |

Remote System Monitoring

The NI PXIe-1085 Series chassis provides an Ethernet port on the rear panel of the chassis. You can use this Ethernet port to monitor the chassis operating parameters remotely over a network. Refer to Figure 1-2, *Rear View of the NI PXIe-1085 Series Chassis*, to locate the Ethernet connector.

The Ethernet port on the chassis supports communication speeds of 10 Mbps and 100 Mbps. Contact your network administrator to determine whether your network supports DHCP. If your network uses DHCP, the network configuration is performed automatically.

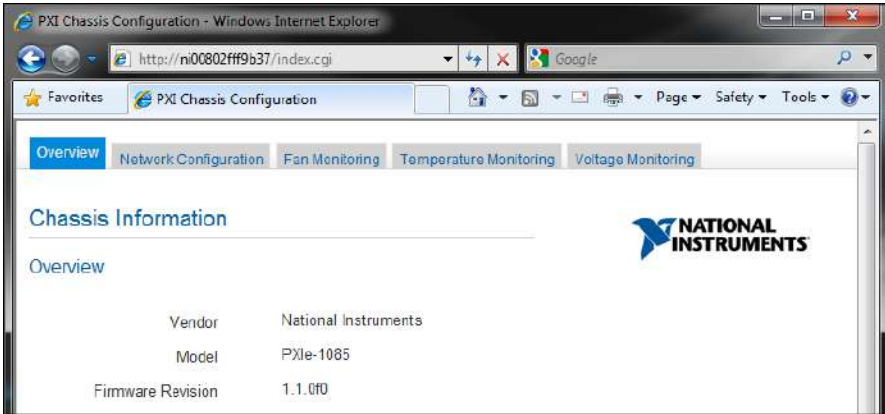
To use the remote monitoring interface, connect one end of an Ethernet cable to your NI PXIe-1085 Series chassis. Connect the other end of the cable to your Ethernet network.



Note The Ethernet controller can perform automatic crossover, thus eliminating the need for crossover cables.

Through the remote monitoring Ethernet interface of the chassis, you can access a web page with information about the current chassis operating parameters. You can access this page in most browsers. Enter the IP address or hostname currently assigned to the chassis into the browser's address bar. Figure 2-7 shows an example of the web page.

Figure 2-7. Chassis Configuration Web Page



The Ethernet connector has two LEDs that indicate the current status of the Ethernet link. Table 2-1 describes the behavior of these LEDs.

Table 2-1. Ethernet LED Behavior

LED	State	Description
ACT/Link	Off	Link is not established.
	Steady green	Link is established.
	Blinking green	Chassis is communicating with another device on the network.
10/100	Off	10 Mbps data rate is selected.
	Steady green	100 Mbps data rate is selected

Default Configuration Settings

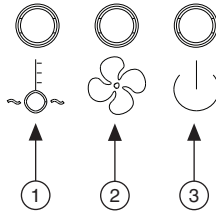
The chassis ships from the factory with the following default configuration settings:

- DHCP with Auto IP fallback
- Default hostname as printed on the product label

Front Panel and Fan Module LED Indicators

Figure 2-8 shows the front panel LEDs. Table 2-2 describes the LED states.

Figure 2-8. Front Panel LEDs



1 Temperature LED

2 Fan LED

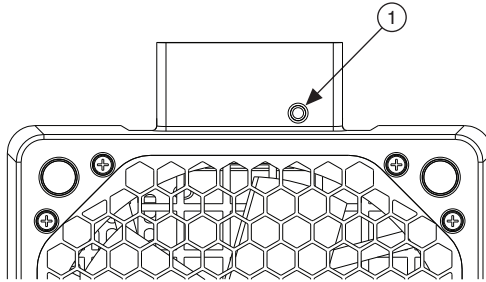
3 Power LED

Table 2-2. Front Panel LED States

LED	State	Description
Temperature LED	Off	Chassis is powered off.
	Steady green	Intake temperature is within chassis operating range.
	Blinking red	Intake temperature is outside of chassis operating range.
	Steady red	Intake temperature has reached critical limits.
Fan LED	Off	Chassis is powered off.
	Steady green	All chassis fans are enabled and operating normally.
	Blinking red	A single chassis fan has failed, but chassis can continue to operate.
	Steady red	Two or more chassis fans have failed, and chassis must shut itself down.
Power LED	Off	Chassis is powered off.
	Steady green	Power supply is active, and all voltages are within normal operating ranges.
	Blinking red	Power supply is active, and at least one voltage is out of range.
	Steady red	Power supply has failed.

Figure 2-9 shows a fan module LED. Table 2-3 describes the LED states.

Figure 2-9. Fan Module LED



1 Fan Module LED

Table 2-3. Fan Module LED States

LED	State	Description
Fan module LED	Off	Chassis is powered off.
	Steady green	Fan is operating normally.
	Steady red	Fan has failed.



Note If two system fans or both of the power supply fans fail, the chassis shuts down automatically, preventing the chassis and modules from damage due to overheating.

Remote Voltage Monitoring and Control

The NI PXIe-1085 Series chassis supports remote voltage monitoring and inhibiting through a female 8-pin connector on the rear panel. Table 2-4 shows the pinout of the 8-pin connector.



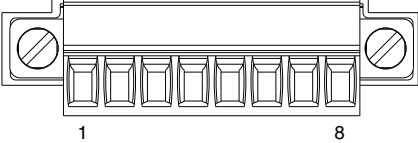
Note The NI PXIe-1085 Series chassis accessory kit includes one 8-pin connector. To order additional connectors, use Phoenix Contact part number MC 1.5/8-STF-3.5-BK or 1847181.



Caution The Inhibit/Voltage Mon port can be damaged if subjected to Electrostatic Discharge (ESD). To prevent damage, industry-standard ESD prevention measures must be employed during installation, maintenance, and operation.

Table 2-4. Remote Inhibit and Voltage Monitoring Connector Pinout

Pin	Signal
1	Inhibit (Active Low)
2	Fault (Active High)
3	Logic Ground
4	+5 VDC
5	+3.3 VDC
6	+12 VDC
7	-12 VDC
8	Logic Ground




Caution When connecting digital voltmeter probes to the rear 8-pin connector, be careful not to short the probe leads together.

You can use a digital voltmeter to ensure all voltage levels in the NI PXIe-1085 Series chassis are within the allowable limits. Referring to Table 2-5, connect one lead of the voltmeter to a supply pin on the 8-pin remote voltage monitoring connector on the rear panel. Refer to Table 2-4 for a pinout diagram of the remote voltage monitoring connector. Connect the reference lead of the voltmeter to one of the ground pins. Compare each voltage reading to the values listed in Table 2-5.



Note Use the rear-panel 8-pin connector to check voltages only. Do not use the connector to supply power to external devices.

Table 2-5. Power Supply Voltages at Voltage Monitoring Connector

Pin	Supply	Acceptable Voltage Range
4	+5 V	4.75 to 5.25 V
5	+3.3 V	3.135 to 3.465 V

Table 2-5. Power Supply Voltages at Voltage Monitoring Connector (Continued)

Pin	Supply	Acceptable Voltage Range
6	+12 V	11.4 to 12.6 V
7	-12 V	-12.6 to -11.4 V
3, 8	Logic Ground	0 V

If the voltages fall within the specified ranges, the chassis complies with the CompactPCI voltage-limit specifications.

Inhibit Mode Switch

On the rear panel of the chassis there is an Inhibit Mode switch. Refer to Figure 1-2, *Rear View of the NI PXIe-1085 Series Chassis*, for the location.

The Inhibit Mode switch should be in the **Default** position when normal power inhibit switch functionality is desired. If the user needs to power on a chassis without a system controller installed the switch should be in the **Manual** position.

When the Inhibit Mode switch is set to the **Manual** position, the power supplies are enabled, and you can use the Inhibit signal (active low) on pin 1 of the Remote Inhibit and Voltage Monitoring connector to power off the chassis. To remotely power off the chassis, connect the Inhibit pin (pin 1) to a Logic Ground pin (pin 3 or 8). As long as this connection exists, the chassis will remain off (standby); when you remove this connection, the chassis turns on.



Note For the Remote Inhibit signal to control the On/Off (standby) state of the chassis, the Inhibit Mode switch must be in the **Manual** position.

PXI_CLK10 Front Panel Connectors

There are two SMA connectors on the front of the NI PXIe-1085 Series chassis for PXI_CLK10. The connectors are labeled IN and OUT. You can use them for supplying the backplane with PXI_CLK10 or routing the backplane's PXI_CLK10 to another chassis. Refer to the *System Reference Clock* section of Chapter 1, *Getting Started*, for details about these signals.

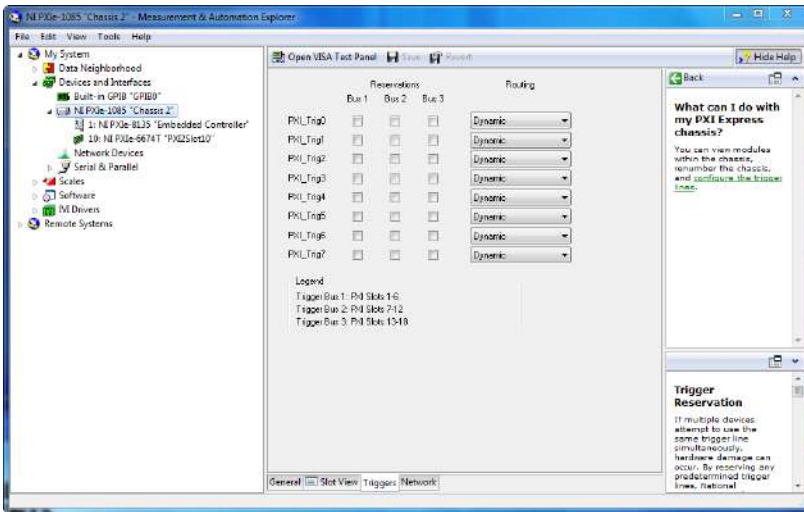
PXI Express System Configuration with MAX

The PXI Platform Services software included with your chassis automatically identifies your PXI Express system components to generate a `pxiesys.ini` file. You can configure your entire PXI system and identify PXI-1 chassis through Measurement & Automation Explorer (MAX), included with your system controller. MAX creates the `pxiesys.ini` and `pxisys.ini` file, which define your PXI system parameters. MAX also provides an interface to route and reserve triggers so dynamic routing, through drivers such as DAQmx, avoids

double-driving and potentially damaging trigger lines. For more information about routing and reserving PXI triggers, refer to KnowledgeBase 3TJDOND8 at ni.com/support.

The configuration steps for single or multiple-chassis systems are the same.

Figure 2-10. Multichassis Configuration in MAX



PXI-1 System Configuration

1. Launch MAX.
2. In the **Configuration** tree, click the **Devices and Interfaces** branch to expand it.
3. If the PXI system controller has not yet been configured, it is labeled **PXI System (Unidentified)**. Right-click this entry to display the pop-up menu, then select the appropriate system controller model from the **Identify As** submenu.
4. Click the PXI system controller. The chassis (or multiple chassis, in a multichassis configuration) is listed below it. Identify each chassis by right-clicking its entry, then selecting the appropriate chassis model through the **Identify As** submenu. Further expanding the **PXI System** branch shows all devices in the system that can be recognized by NI-VISA. When your system controller and all your chassis are identified, the required `pxisys.ini` file is complete.

The PXI specification allows for many combinations of PXI chassis and system modules. To assist system integrators, the manufacturers of PXI chassis and system modules must document the capabilities of their products. PXI Express devices must provide a driver and `.ini` file for identification. These files are provided as part of the PXI Platform Services software included with your system controller. The minimum documentation requirements for PXI-1 are contained in `.ini` files, which consist of ASCII text. System integrators, configuration utilities, and device drivers can use these `.ini` files.

The capability documentation for a PXI-1 chassis is contained in a `chassis.ini` file provided by the chassis manufacturer. The information in this file is combined with information about the system controller to create a single PXI-1 system initialization file called `pxisys.ini` (PXI System Initialization). The NI system controller uses MAX to generate the `pxisys.ini` file from the `chassis.ini` file.

Device drivers and other utility software read the `pxiesys.ini` and `pxisys.ini` file to obtain system information. For detailed information about initialization files, refer to the PXI specification at www.pxisa.org.

Trigger Configuration in MAX

Each chassis has one or more trigger buses, each with eight lines numbered 0 through 7 that can be reserved and routed statically or dynamically. Static reservation *pre-allocates* a trigger line to prevent its configuration by a user program. Dynamic reservation/routing/deallocation is *on the fly* within a user program based upon National Instruments APIs such as NI-DAQmx. Static reservation of trigger lines can be implemented by the user in MAX through the **Triggers** tab. Reserved trigger lines will not be used by PXI modules dynamically configured by programs such as NI-DAQmx. This prevents the instruments from double-driving the trigger lines, possibly damaging devices in the chassis. In the default configuration, trigger lines on each bus are independent. For example, if trigger line 3 is asserted on trigger bus 0, by default it will not be automatically asserted on any other trigger bus.

Complete the following steps to reserve these trigger lines in MAX.

1. In the Configuration tree, click on the PXI chassis branch you want to configure.
2. Then, in the right-hand pane, toward the bottom, click on the **Triggers** tab.
3. Select which trigger lines you would like to statically reserve.
4. Click the **Save** button.

PXI Trigger Bus Routing

Some National Instruments chassis, such as the NI PXIe-1085 Series and the NI PXI-1044/1045, have the capability to route triggers from one bus to others within the same chassis using the **Trigger Routing** tab in MAX, as shown in Figure 2-10.



Note Selecting any non-disabled routing automatically reserves the line in all trigger buses being routed to. If you are using NI-DAQmx, it will reserve and route trigger lines for you, so you won't have to route trigger lines manually.

Complete the following steps to configure trigger routings in MAX.

1. In the **Configuration** tree, select the chassis in which you want to route trigger lines.
2. In the right-hand pane, select the **Trigger Routing** tab near the bottom.

3. For each trigger line, select **Route Right**, **Route Outward From Middle**, or **Route Left** to route triggers on that line in the described direction, or select **Disabled** for the default behavior with no manual routing.
4. Click the **Apply** button.

Using System Configuration and Initialization Files

The PXI Express specification allows many combinations of PXI Express chassis and system modules. To assist system integrators, the manufacturers of PXI Express chassis and system modules must document the capabilities of their products. The minimum documentation requirements are contained in `.ini` files, which consist of ASCII text. System integrators, configuration utilities, and device drivers can use these `.ini` files.

The capability documentation for the NI PXIe-1085 Series chassis is contained in the `chassis.ini` file on the software media that comes with the chassis. The information in this file is combined with information about the system controller to create a single system initialization file called `pxisys.ini` (PXI System Initialization). The system controller manufacturer either provides a `pxisys.ini` file for the particular chassis model that contains the system controller or provides a utility that can read an arbitrary `chassis.ini` file and generate the corresponding `pxisys.ini` file. System controllers from NI provide the `pxisys.ini` file for the NI PXIe-1085 Series chassis, so you should not need to use the `chassis.ini` file. Refer to the documentation provided with the system controller or to ni.com/support for more information on `pxisys.ini` and `chassis.ini` files.

Device drivers and other utility software read the `pxisys.ini` file to obtain system information. The device drivers should have no need to directly read the `chassis.ini` file. For detailed information regarding initialization files, refer to the PXI Express specification at www.pxisa.org.

Maintenance

This chapter describes basic maintenance procedures you can perform on the NI PXIe-1085 Series chassis.



Caution Disconnect the power cable prior to servicing a NI PXIe-1085 Series chassis.

Service Interval

Clean dust from the chassis exterior (and interior) as needed, based on the operating environment. Periodic cleaning increases reliability.

Preparation

The information in this section is designed for use by qualified service personnel. Read the *Read Me First: Safety and Electromagnetic Compatibility* document included with your kit before attempting any procedures in this chapter.



Caution Many components within the chassis are susceptible to static discharge damage. Service the chassis only in a static-free environment. Observe standard handling precautions for static-sensitive devices while servicing the chassis. *Always* wear a grounded wrist strap or equivalent while servicing the chassis.

Cleaning

Cleaning procedures consist of exterior and interior cleaning of the chassis. Refer to your module user documentation for information on cleaning the individual CompactPCI or PXI Express modules.



Caution *Always* disconnect the AC power cable before cleaning or servicing the chassis.

Interior Cleaning

Use a dry, low-velocity stream of air to clean the interior of the chassis. Use a soft-bristle brush for cleaning around components.

Exterior Cleaning

Clean the exterior surfaces of the chassis with a dry lint-free cloth or a soft-bristle brush. If any dirt remains, wipe with a cloth moistened in a mild soap solution. Remove any soap residue by wiping with a cloth moistened with clear water. Do not use abrasive compounds on any part of the chassis.



Cautions Avoid getting moisture inside the chassis during exterior cleaning, especially through the top vents. Use just enough moisture to dampen the cloth.

Do *not* wash the front- or rear-panel connectors or switches. Cover these components while cleaning the chassis.

Do *not* use harsh chemical cleaning agents; they may damage the chassis. Avoid chemicals that contain benzene, toluene, xylene, acetone, or similar solvents.

Resetting the AC Mains Circuit Breaker

If the NI PXIe-1085 Series chassis is connected to an AC source and encounters an over-current condition, the circuit breaker on the rear panel will trip to prevent damage to the chassis. Complete the following steps to reset the circuit breaker.

1. Turn off the chassis.
2. Disconnect the AC power cable.
3. Depress the circuit breaker to reset it.
4. Reconnect the AC power cable.
5. Turn on the chassis.

If the circuit breaker trips again, complete the following steps:

1. Turn off the chassis.
2. Disconnect the AC power cable.
3. Remove all modules from the chassis.
4. Complete the procedure described in the [Connecting to Power Source](#) section of Chapter 2, [Installation and Configuration](#). If the power switch LED is not a steady green, contact National Instruments.
5. Verify that the NI PXIe-1085 Series chassis can meet the power requirements of your CompactPCI or PXI Express modules. Overloading the chassis can cause the breaker to trip. Refer to Appendix A, [Specifications](#).
6. The over-current condition that caused the circuit breaker to trip may be due to a faulty CompactPCI or PXI Express module. Refer to the documentation supplied with the modules for troubleshooting information.

Replacing the Modular Power Supply

This section describes how to remove, configure, and install the AC power supply shuttle in the NI PXIe-1085 Series chassis.



Caution Disconnect the power cable prior to replacing the power supply.

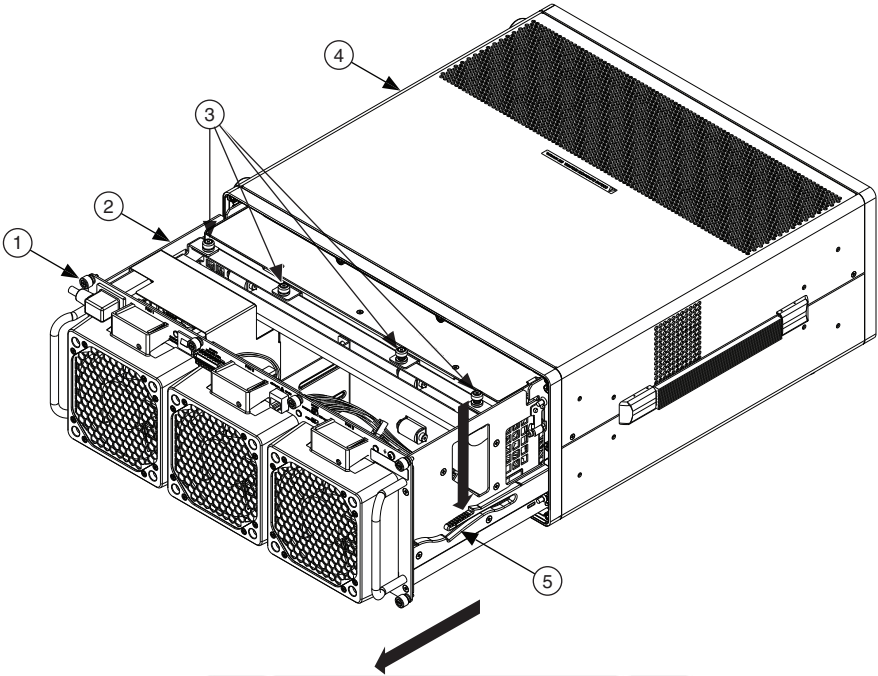
Before connecting the power supply shuttle to a power source, read this section and the *Read Me First: Safety and Electromagnetic Compatibility* document included with the kit.

Removal

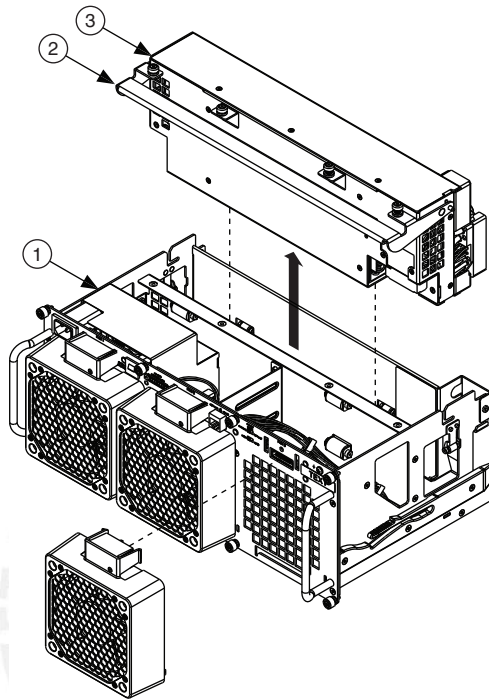
The NI PXIe-1085 Series power supply is a replacement part for the NI PXIe-1085 Series chassis. Before attempting to replace the power supply, verify that there is adequate clearance behind the chassis. Disconnect the power cable from the power supply shuttle on the back of the chassis. Identify the eight mounting screws for the chassis that attach the power supply shuttle to the chassis. Refer to Figure 1-2, *Rear View of the NI PXIe-1085 Series Chassis*, for the screw locations. Using a Phillips screwdriver, remove the screws. Pull on the two rear handles of the power supply shuttle to remove it from the back of the chassis, as shown in Figure 3-1. About halfway through removing the shuttle, the shuttle rail safety catches engage to prevent the shuttle from falling out. Press down on the shuttle rail safety catches to remove the shuttle the rest of the way, as shown in Figure 3-1.

After removing the shuttle from the chassis, you can access the modular power supply. To remove the modular power supply, first loosen the four screws that retain it. Refer to Figure 3-1 for the screw locations. After loosening the screws, you can remove the modular power supply by rotating the handle away from the fans and pulling upward when it is in the upright position, as shown in Figure 3-2.

Figure 3-1. Removing Power Supply Shuttle



- | | |
|---|--|
| 1 Power Supply Shuttle Mounting Screws (8x) | 4 NI PXIe-1085 Series Chassis |
| 2 Power Supply Shuttle | 5 Shuttle Rail Safety Catch (Both Sides) |
| 3 Modular Power Supply Screws (4x) | |

Figure 3-2. Removing Modular Power Supply from Power Supply Shuttle

1 Power Supply Shuttle 2 Modular Power Supply Handle 3 Modular Power Supply

Installation

Ensure that there is no visible damage to the new power supply assembly. Verify that the housing and connector on the new power supply assembly have no foreign material inside. Install the new power supply assembly into the opening in the shuttle in the reverse order of removal. Replace and tighten the four screws with a Phillips screwdriver or by hand.

After installing the power supply assembly, slide the power supply shuttle into the opening in the rear of the chassis. Tighten the eight screws with a Phillips screwdriver.

Configuration

The fan-speed selector switch is on the rear panel of the power supply shuttle. Refer to Figure 1-2, *Rear View of the NI PXIe-1085 Series Chassis*, to locate the fan-speed selector. Select **High** for maximum cooling performance (recommended) or **Auto** for quieter operation. Set the Inhibit Mode switch to the **Default** position.

Connecting Safety Ground

Refer to the *Connecting Safety Ground* section of Chapter 2, *Installation and Configuration*.

Connecting to Power Source

Refer to the *Connecting to Power Source* section of Chapter 2, *Installation and Configuration*.

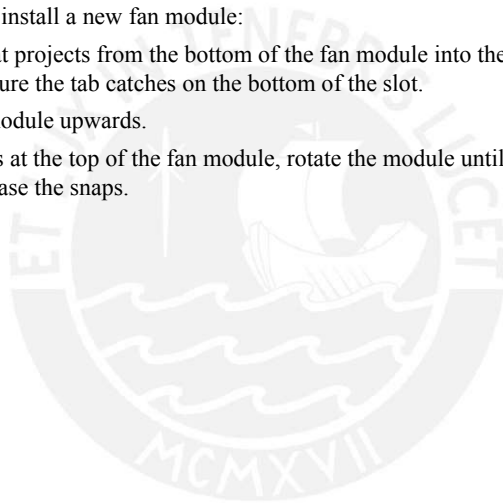
Installing Replacement Fan Modules

Follow these steps to remove a failed fan module:

1. Pinch both snaps at the top of the fan module simultaneously.
2. Rotate the fan module downwards and remove from the chassis, as shown in Figure 3-3.

Follow these steps to install a new fan module:

1. Insert the tab that projects from the bottom of the fan module into the slot on the back of the chassis. Be sure the tab catches on the bottom of the slot.
2. Rotate the fan module upwards.
3. Pinch both snaps at the top of the fan module, rotate the module until it is flush with the chassis, and release the snaps.



Specifications

This appendix contains specifications for the NI PXIe-1085 Series chassis.



Caution Specifications are subject to change without notice.

Electrical

AC Input

Input voltage range	100 to 240 VAC
Operating voltage range ¹	90 to 264 VAC
Input frequency	50/60 Hz
Operating frequency range ¹	47 to 63 Hz
Input current rating	12 to 6 A
Over-current protection	15 A circuit breaker
Line regulation	
3.3 V	<±0.2%
5 V	<±0.1%
±12 V	<±0.1%
Efficiency	70% typical
Power disconnect	The AC power cable provides main power disconnect. Do not position the equipment so that it is difficult to disconnect the power cord. The front-panel power switch causes the internal chassis power supply to provide DC power to the CompactPCI/PXI Express backplane. You also can use the rear-panel 8-pin connector and inhibit mode switch to control the internal chassis power supply.

¹ The operating range is guaranteed by design.

DC Output

DC current capacity (I_{MP})

Voltage	Maximum Current
+3.3 V	61 A
+5 V	48 A
+12 V	62 A
-12 V	4 A
5 V _{AUX}	2.0 A



Note Maximum total available power is 791 W.

Backplane slot current capacity

Slot	+5 V	V(I/O)	+3.3 V	+12 V	-12 V	5 V _{AUX}
System Controller Slot	15 A	—	15 A	30 A	—	1 A
System Timing Slot	—	—	6 A	4 A	—	1 A
Hybrid Peripheral Slot with PXI-1 Peripheral	6 A	5 A	6 A	1 A	1 A	—
Hybrid Peripheral Slot with PXI-5 Peripheral	—	—	6 A	4 A	—	1 A
PXI-1 Peripheral Slot	6 A	11 A	6 A	1 A	1 A	—



Notes Total system slot current should not exceed 45 A.

PCI V(I/O) pins in PXI-1 peripheral slots and hybrid peripheral slots are connected to +5 V.

The maximum power dissipated in the system slot should not exceed 140 W.

The maximum power dissipated in a peripheral slot should not exceed 38.25 W.

Load regulation

Voltage	Load Regulation
+3.3 V	<5%
+12 V	<5%
+5 V	<5%
-12 V	<5%

Maximum ripple and noise (20 MHz bandwidth)

Voltage	Maximum Ripple and Noise
+3.3 V	50 mV _{pp}
+12 V	50 mV _{pp}
+5 V	50 mV _{pp}
-12 V	50 mV _{pp}

Over-current protection All outputs protected from short circuit and overload with automatic recovery

Over-voltage protection
 3.3 V and 5 V Clamped at 20 to 30% above nominal output voltage

Power supply shuttle MTTR..... Replacement in under 5 minutes

Chassis Cooling

Module cooling system

NI PXIe-1085 Series chassis Forced air circulation (positive pressurization) through three 169 cfm fans with High/Auto speed selector

Slot airflow direction Bottom of module to top of module

Module cooling intake Bottom rear of chassis

Module cooling exhaust..... Along both sides and top of chassis

Power supply cooling system Forced air circulation through two integrated fans

Power supply cooling intake..... Right side of chassis

Power supply cooling exhaust Left side of chassis

Environmental

Maximum altitude 2,000 m (800 mbar)
(at 25 °C ambient)

Pollution Degree 2

For indoor use only.

Operating Environment

Ambient temperature range 0 to 55 °C
(Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.)

Relative humidity range 10 to 90%, noncondensing
(Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range -40 to 71 °C
(Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 limits.)

Relative humidity range 5 to 95%, noncondensing
(Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Operational shock 30 g peak, half-sine, 11 ms pulse
(Tested in accordance with IEC 60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)

Random Vibration 5 to 500 Hz, 0.3 g_{rms}

Acoustic Emissions

Sound Pressure Level (at Operator Position)

(Tested in accordance with ISO 7779. Meets MIL-PRF-28800F requirements.)

Auto fan (up to ~30 °C ambient) 51.2 dBA

High fan 64.1 dBA

Sound Power

Auto fan (up to ~30 °C ambient) 60.8 dBA

High fan 75.9 dBA



Caution The protection provided by the NI PXIe-1085 Series can be impaired if it is used in a manner not described in this document.



Note Specifications are subject to change without notice.

Safety

This product is designed to meet the requirements of the following standards of safety for information technology equipment:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1



Note For UL and other safety certifications, refer to the product label or the [Online Product Certification](#) section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions



Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia and New Zealand (per CISPR 11) Class A equipment is intended for use only in heavy-industrial locations.



Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.



Note For EMC declarations and certifications, and additional information, refer to the [Online Product Certification](#) section.

CE Compliance

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)



EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）



中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息, 请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

Backplane

Size.....	3U-sized; one system slot (with three system expansion slots) and 17 peripheral slots. Compliant with IEEE 1101.10 mechanical packaging. PXI Express Specification compliant. Accepts both PXI Express and CompactPCI (PICMG 2.0 R 3.0) 3U modules.
Backplane bare-board material	UL 94 V-0 Recognized

Backplane connectors Conforms to IEC 917 and IEC 1076-4-101, and are UL 94 V-0 rated

System Synchronization Clocks (PXI_CLK10, PXIe_CLK100, PXIe_SYNC100)

10 MHz System Reference Clock: PXI_CLK10

Maximum slot-to-slot skew 1 ns
 Accuracy ± 25 ppm max. (guaranteed over the operating temperature range)
 Maximum jitter 5 ps RMS phase-jitter (10 Hz to 1 MHz range)
 Duty-factor 45% to 55%
 Unloaded signal swing 3.3 V ± 0.3 V



Note For other specifications refer to the *PXI-1 Hardware Specification*.

100 MHz System Reference Clock: PXIe_CLK100 and PXIe_SYNC100

Maximum slot-to-slot skew 100 ps
 Accuracy ± 25 ppm max. (guaranteed over the operating temperature range)
 Maximum jitter 3 ps RMS phase-jitter (10 Hz to 12 kHz range);
 2 ps RMS phase-jitter (12 kHz to 20 MHz range)
 Duty-factor for PXIe_CLK100 45% to 55%
 Absolute single-ended voltage swing
 (When each line in the differential pair
 has 50 Ω termination to 1.30 V
 or Thévenin equivalent) 400 to 1000 mV



Note For other specifications refer to the *PXI-5 PXI Express Hardware Specification*.

External 10 MHz Reference Out (SMA on front panel of chassis)

Accuracy ± 25 ppm max. (guaranteed over the operating temperature range)
 Maximum jitter 5 ps RMS phase-jitter (10 Hz to 1 MHz range)
 Output amplitude 1 V_{pp} $\pm 20\%$ square-wave into 50 Ω
 2 V_{pp} unloaded
 Output impedance 50 Ω ± 5 Ω

External Clock Source

Frequency.....	10 MHz \pm 100 PPM
Input amplitude	
Rear panel BNC.....	200 mV _{PP} to 5 V _{PP} square-wave or sine-wave
System timing slot	
PXI_CLK10_IN.....	5 V or 3.3 V TTL signal
Front panel SMA input impedance.....	50 Ω \pm 5 Ω
Maximum jitter introduced	
by backplane	1 ps RMS phase-jitter (10 Hz to 1 MHz range)

PXle_SYNC_CTRL

V _{IH}	2.0 to 5.5 V
V _{IL}	0 to 0.8 V

PXI Star Trigger

Maximum slot-to-slot skew	250 ps
Backplane characteristic impedance.....	65 Ω \pm 10%



Notes For PXI slot to PXI Star mapping refer to the [NI PXIe-1085 24 GB/s PCI Express Backplane Diagram](#) section of Chapter 1, *Getting Started*.

For other specifications refer to the *PXI-1 Hardware Specification*.

PXI Differential Star Triggers (PXIe-DSTARA, PXIe-DSTARB, PXIe-DSTARC)

Maximum slot-to-slot skew	150 ps
Maximum differential skew	25 ps
Backplane differential impedance.....	100 Ω \pm 10%



Notes For PXI Express slot to PXI_DSTAR mapping refer to the [NI PXIe-1085 24 GB/s PCI Express Backplane Diagram](#) section of Chapter 1, *Getting Started*.

For other specifications, the NI PXIe-1085 Series chassis complies with the *PXI-5 PXI Express Hardware Specification*.

Mechanical

Overall dimensions

Standard chassis

Height	6.97 in. (177.1 mm)
Width	18.30 in. (464.8 mm)
Depth	19.38 in. (492.3 mm)



Note 0.57 in. (14.5 mm) is added to height when feet are installed. When tilted with front feet extended on table top, height is increased approximately 2.08 in. (52.8 mm) in front and 0.583 in. (14.8 mm) in rear.

Weight.....	40.3 lb (18.28 kg)
Chassis materials	Sheet Aluminum (5052-H32, 5754-H22), Extruded Aluminum (6063-T5, 6060-T6), Plate Aluminum (6063-T5, 6061-T6), Cold Rolled Steel, Cold Rolled Stainless Steel, Sheet Copper (C110), Santoprene, Urethane Foam, PC-ABS, Nylon, Polycarbonate, Delrin, Polyethylene, Polyamide (FR-106), Neodymium Magnet
Finish	Conductive Clear Iridite on Aluminum, Electroplated Nickel on Cold Rolled Steel, Electroplated Zinc on Cold Rolled Steel, Electroplated Nickel on Copper

Figures A-1 and A-2 show the NI PXIe-1085 Series chassis dimensions. The holes shown are for the installation of the optional rack mount kits. You can install those kits on the front or rear of the chassis, depending on which end of the chassis you want to face toward the front of the instrument cabinet. Notice that the front and rear chassis mounting holes (size M4) are symmetrical.

Figure A-1. NI PXIe-1085 Series Chassis Dimensions (Front and Side)

Dimensions are in inches (millimeters)

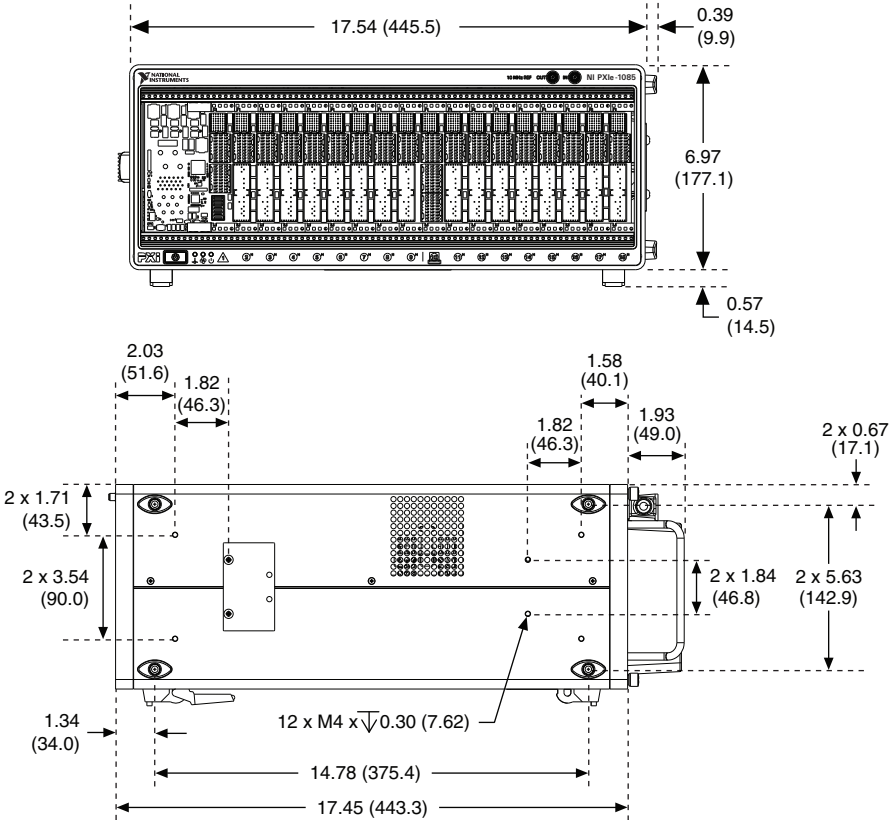


Figure A-2. NI PXIe-1085 Series Chassis Dimensions (Bottom)

Dimensions are in inches (millimeters)

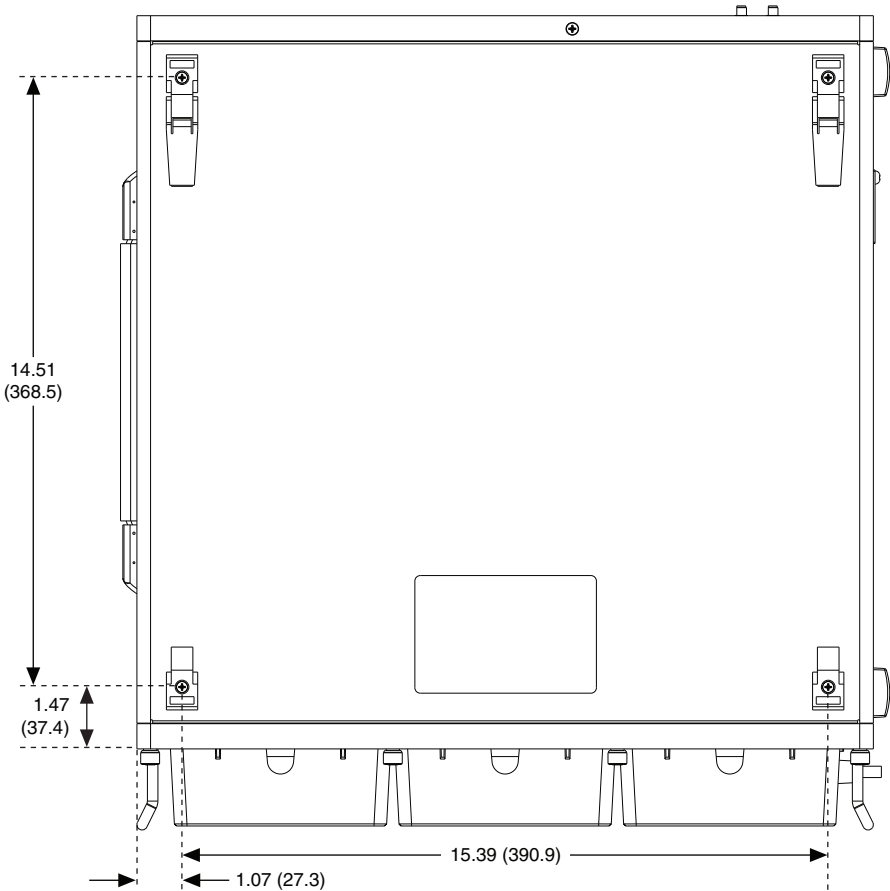
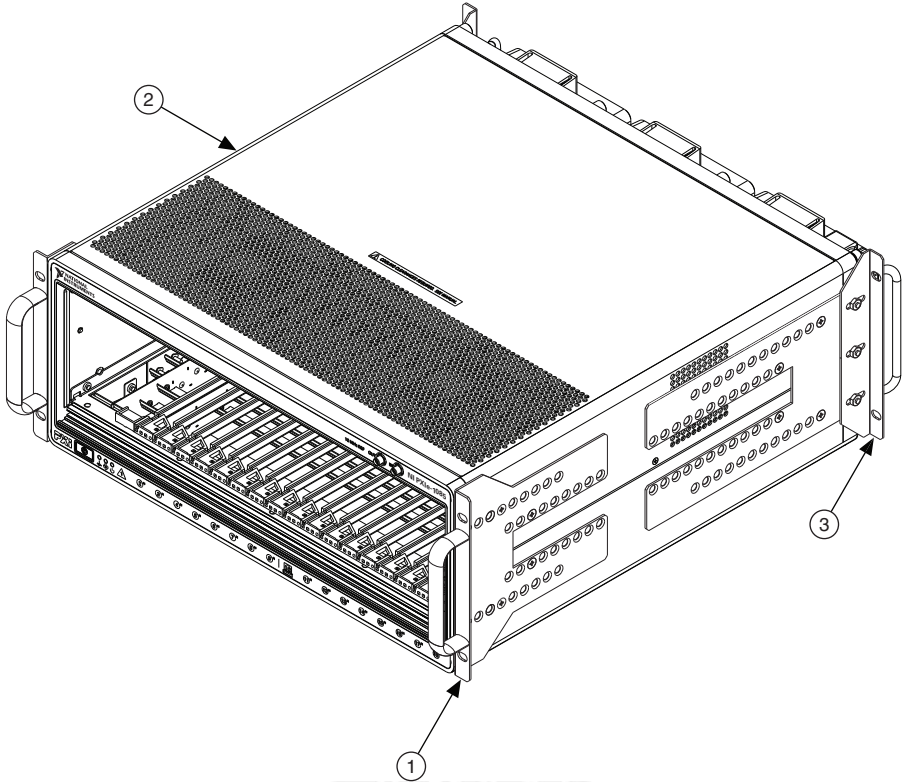


Figure shows the chassis rack mount kit components.

Figure A-3. NI Chassis Rack Mount Kit Components



1 Front Rack Mount Kit

2 NI PXIe-1085 Series Chassis

3 Rear Rack Mount Kit

Pinouts

This appendix describes the connector pinouts for the NI PXIe-1085 Series chassis backplane.

Table B-1 shows the XP1 Connector Pinout for the System Controller slot.

Table B-2 shows the XP2 Connector Pinout for the System Controller slot.

Table B-3 shows the XP3 Connector Pinout for the System Controller slot.

Table B-4 shows the XP4 Connector Pinout for the System Controller slot.

Table B-5 shows the TP1 Connector Pinout for the System Controller slot.

Table B-6 shows the TP2 Connector Pinout for the System Timing slot.

Table B-7 shows the XP3 Connector Pinout for the System Timing slot.

Table B-8 shows the XP4 Connector Pinout for the System Timing slot.

Table B-9 shows the P1 Connector Pinout for the peripheral slots.

Table B-10 shows the P2 Connector Pinout for the peripheral slots.

Table B-11 shows the P1 Connector Pinout for the Hybrid peripheral slots.

Table B-12 shows the XP3 Connector Pinout for the Hybrid peripheral slots.

Table B-13 shows the XP4 Connector Pinout for the Hybrid peripheral slots.

For more detailed information, refer to the *PXI-5 PXI Express Hardware Specification*, Revision 2.0. Contact the PXI Systems Alliance for a copy of the specification.

System Controller Slot Pinouts

Table B-1. XP1 Connector Pinout for the System Controller Slot

Pins	Signals
A	GND
B	12V
C	12V
D	GND
E	5V
F	3.3V
G	GND

Table B-2. XP2 Connector Pinout for the System Controller Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	2PETp1	2PETn1	GND	2PERp1	2PERn1	GND	2PETp2	2PETn2	GND
2	2PETp3	2PETn3	GND	2PERp3	2PERn3	GND	2PERp2	2PERn2	GND
3	2PETp4	2PETn4	GND	2PERp4	2PERn4	GND	2PETp5	2PETn5	GND
4	2PETp6	2PETn6	GND	2PERp6	2PERn6	GND	2PERp5	2PERn5	GND
5	2PETp7	2PETn7	GND	2PERp7	2PERn7	GND	2PETp8	2PETn8	GND
6	2PETp9	2PETn9	GND	2PERp9	2PERn9	GND	2PERp8	2PERn8	GND
7	2PETp10	2PETn10	GND	2PERp10	2PERn10	GND	2PETp11	2PETn11	GND
8	2PETp12	2PETn12	GND	2PERp12	2PERn12	GND	2PERp11	2PERn11	GND
9	2PETp13	2PETn13	GND	2PERp13	2PERn13	GND	2PETp14	2PETn14	GND
10	2PETp15	2PETn15	GND	2PERp15	2PERn15	GND	2PERp14	2PERn14	GND

Table B-3. XP3 Connector Pinout for the System Controller Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
2	RSV	RSV	GND	PWR_OK	PS_ON#	GND	LINKCAP	PWRBTN#	GND
3	SMBDAT	SMBCLK	GND	RSVD	RSVD	GND	RSVD	RSVD	GND
4	RSV	PERST#	GND	2RefClk+	2RefClk-	GND	1RefClk+	1RefClk-	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND
10	2PETp0	2PETn0	GND	2PERp0	2PERn0	GND	1PERp7	1PERn7	GND

Table B-4. XP4 Connector Pinout for the System Controller Slot

Pin	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND
3	GND	RSV	RSV	RSV	RSV	RSV	GND
4	GND	RSV	RSV	RSV	RSV	RSV	GND
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND
6	GND	PXI_TRIG2	GND	RSV	PXI_STAR	PXI_CLK10	GND
7	GND	PXI_TRIG1	PXI_TRIG0	RSV	GND	PXI_TRIG7	GND
8	GND	RSV	GND	RSV	RSV	PXI_LBR6	GND

System Timing Slot Pinouts

Table B-5. TP1 Connector Pinout for the System Timing Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	PXle_DSTAR3+	PXle_DSTAR3-	GND	NC	NC	GND	NC	NC	GND
2	PXle_DSTAR4+	PXle_DSTAR4-	GND	PXl_STAR12	PXl_STAR13	GND	NC	NC	GND
3	PXle_DSTARB4+	PXle_DSTARB4-	GND	NC	NC	GND	NC	NC	GND
4	PXle_DSTARA4+	PXle_DSTARA4-	GND	NC	NC	GND	NC	NC	GND
5	PXle_DSTAR5+	PXle_DSTAR5-	GND	PXl_STAR14	PXl_STAR15	GND	NC	NC	GND
6	PXle_DSTARB5+	PXle_DSTARB5-	GND	NC	NC	GND	NC	NC	GND
7	PXle_DSTAR5+	PXle_DSTAR5-	GND	NC	NC	GND	NC	NC	GND
8	PXle_DSTAR6+	PXle_DSTAR6-	GND	PXl_STAR16	RSV	GND	NC	NC	GND
9	PXle_DSTARB6+	PXle_DSTARB6-	GND	NC	NC	GND	NC	NC	GND
10	PXle_DSTAR6+	PXle_DSTAR6-	GND	NC	NC	GND	NC	NC	GND



Table B-6. TP2 Connector Pinout for the System Timing Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	NC	NC	GND	PXIe_DSTARC8+	PXIe_DSTARC8-	GND	PXIe_DSTARB8+	PXIe_DSTARB8-	GND
2	NC	NC	GND	NC	NC	GND	PXIe_DSTARA8+	PXIe_DSTARA8-	GND
3	NC	NC	GND	PXIe_DSTARC1+	PXIe_DSTARC1-	GND	NC	NC	GND
4	PXIe_DSTARB1+	PXIe_DSTARB1-	GND	PXI_STAR0	PXI_STAR1	GND	NC	NC	GND
5	PXIe_DSTARA1+	PXIe_DSTARA1-	GND	PXI_STAR2	PXI_STAR3	GND	NC	NC	GND
6	PXIe_DSTARC2+	PXIe_DSTARC2-	GND	PXI_STAR4	PXI_STAR5	GND	NC	NC	GND
7	PXIe_DSTARB2+	PXIe_DSTARB2-	GND	PXI_STAR6	PXI_STAR7	GND	NC	NC	GND
8	PXIe_DSTARA2+	PXIe_DSTARA2-	GND	PXI_STAR8	PXI_STAR9	GND	PXIe_DSTARC11+	PXIe_DSTARC11-	GND
9	PXIe_DSTARC3+	PXIe_DSTARC3-	GND	PXI_STAR10	PXI_STAR11	GND	PXIe_DSTARA11+	PXIe_DSTARA11-	GND
10	PXIe_DSTARB3+	PXIe_DSTARB3-	GND	NC	NC	GND	PXIe_DSTARB11+	PXIe_DSTARB11-	GND

Table B-7. XP3 Connector Pinout for the System Timing Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	PXle_CLK100+	PXle_CLK100-	GND	PXle_SYNC100+	PXle_SYNC100-	GND	PXle_DSTARC+	PXle_DSTARC-	GND
2	PRSNT#	PWREN#	GND	PXle_DSTARB+	PXle_DSTARB-	GND	PXle_DSTARA+	PXle_DSTARA-	GND
3	SMBDAT	SMBCLK	GND	RSV	RSV	GND	RSV	RSV	GND
4	MPWRGD*	PERST#	GND	RSV	RSV	GND	1RefClk+	1RefClk-	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	GND

Table B-8. XP4 Connector Pinout for the System Timing Slot

Pin	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND
3	GND	12V	12V	GND	GND	GND	GND
4	GND	GND	GND	3.3V	3.3V	3.3V	GND
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND
6	GND	PXI_TRIG2	GND	ATNLED	PXI_CLK10_IN	PXI_CLK10	GND
7	GND	PXI_TRIG1	PXI_TRIG0	ATNSW#	GND	PXI_TRIG7	GND
8	GND	PXIe_SYNC_CTRL	GND	RSV	PXI_LBL6	PXI_LBR6	GND

Peripheral Slot Pinouts

Table B-9. P1 Connector Pinout for the Peripheral Slot

Pin	Z	A	B	C	D	E	F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
12 to 14	Key Area						
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND
4	GND	IPMB_PWR	HEALTHY	V(I/O)	INTP	INTS	GND

Table B-9. P1 Connector Pinout for the Peripheral Slot (Continued)

Pin	Z	A	B	C	D	E	F
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND

Table B-10. P2 Connector Pinout for the Peripheral Slot

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	PXI_LBR0	GND	PXI_LBR1	PXI_LBR2	PXI_LBR3	GND
20	GND	PXI_LBR4	PXI_LBR5	PXI_LBL0	GND	PXI_LBL1	GND
19	GND	PXI_LBL2	GND	PXI_LBL3	PXI_LBL4	PXI_LBL5	GND
18	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND
17	GND	PXI_TRIG2	GND	RSV	PXI_STAR	PXI_CLK10	GND
16	GND	PXI_TRIG1	PXI_TRIG0	RSV	GND	PXI_TRIG7	GND
15	GND	PXI_BRSA15	GND	RSV	PXI_LBL6	PXI_LBR6	GND
14	GND	RSV	RSV	RSV	GND	RSV	GND
13	GND	RSV	GND	V(I/O)	RSV	RSV	GND
12	GND	RSV	RSV	RSV	GND	RSV	GND
11	GND	RSV	GND	V(I/O)	RSV	RSV	GND
10	GND	RSV	RSV	RSV	GND	RSV	GND
9	GND	RSV	GND	V(I/O)	RSV	RSV	GND
8	GND	RSV	RSV	RSV	GND	RSV	GND
7	GND	RSV	GND	V(I/O)	RSV	RSV	GND
6	GND	RSV	RSV	RSV	GND	RSV	GND
5	GND	RSV	GND	V(I/O)	RSV	RSV	GND
4	GND	V(I/O)	64EN#	RSV	GND	RSV	GND
3	GND	PXI_LBR7	GND	PXI_LBR8	PXI_LBR9	PXI_LBR10	GND
2	GND	PXI_LBR11	PXI_LBR12	UNC	PXI_LBL7	PXI_LBL8	GND
1	GND	PXI_LBL9	GND	PXI_LBL10	PXI_LBL11	PXI_LBL12	GND

Hybrid Slot Pinouts

Table B-11. P1 Connector Pinout for the Hybrid Slot

Pin	Z	A	B	C	D	E	F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
12 to 14	Key Area						
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND
4	GND	IPMB_PWR	HEALTHY#	V(I/O)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND

Table B-12. XP3 Connector Pinout for the Hybrid Slot

Pin	A	B	ab	C	D	cd	E	F	ef
1	PXle_CLK100+	PXle_CLK100-	GND	PXle_SYNC100+	PXle_SYNC100-	GND	PXle_DSTARC+	PXle_DSTARC-	GND
2	PRSNT#	PWREN#	GND	PXle_DSTARB+	PXle_DSTARB-	GND	PXle_DSTARA+	PXle_DSTARA-	GND
3	SMBDAT	SMBCLK	GND	RSV	RSV	GND	RSV	RSV	GND
4	MPWRGD*	PERST#	GND	RSV	RSV	GND	IRefClk+	IRefClk-	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	1PETp1	1PETn1	GND
6	1PETp2	1PETn2	GND	1PERp2	1PERn2	GND	1PERp1	1PERn1	GND
7	1PETp3	1PETn3	GND	1PERp3	1PERn3	GND	1PETp4	1PETn4	GND
8	1PETp5	1PETn5	GND	1PERp5	1PERn5	GND	1PERp4	1PERn4	GND
9	1PETp6	1PETn6	GND	1PERp6	1PERn6	GND	1PETp7	1PETn7	GND
10	RSV	RSV	GND	RSV	RSV	GND	1PERp7	1PERn7	GND

Table B-13. XP4 Connector Pinout for the Hybrid Slot

Pin	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5Vaux	GND	SYSEN#	WAKE#	ALERT#	GND
3	GND	12V	12V	GND	GND	GND	GND
4	GND	GND	GND	3.3V	3.3V	3.3V	GND
5	GND	PXI_TRIG3	PXI_TRIG4	PXI_TRIG5	GND	PXI_TRIG6	GND
6	GND	PXI_TRIG2	GND	ATNLED	PXI_STAR	PXI_CLK10	GND
7	GND	PXI_TRIG1	PXI_TRIG0	ATNSW#	GND	PXI_TRIG7	GND
8	GND	RSV	GND	RSV	PXI_LBL6	PXI_LBR6	GND

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Glossary

Symbol	Prefix	Value
p	pico	10^{-12}
n	nano	10^{-9}
μ	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^3
M	mega	10^6
G	giga	10^9
T	tera	10^{12}

Symbols

- ° Degrees.
- \geq Equal or greater than.
- \leq Equal or less than.
- % Percent.

A

- A Amperes.
- AC Alternating current.
- ANSI American National Standards Institute.
- Auto Automatic fan speed control.
- AWG American Wire Gauge.

B

backplane An assembly, typically a printed circuit board, with connectors and signal paths that bus the connector pins.

C

C Celsius.

cfm Cubic feet per minute.

CFR Code of Federal Regulations.

cm Centimeters.

CompactPCI An adaptation of the Peripheral Component Interconnect (PCI) Specification 2.1 or later for industrial and/or embedded applications requiring a more robust mechanical form factor than desktop PCI. It uses industry standard mechanical components and high-performance connector technologies to provide an optimized system intended for rugged applications. It is electrically compatible with the PCI Specification, which enables low-cost PCI components to be utilized in a mechanical form factor suited for rugged environments.

CSA Canadian Standards Association.

D

daisy-chain A method of propagating signals along a bus, in which the devices are prioritized on the basis of their position on the bus.

DC Direct current.

DoC Declaration of Conformity.

E

efficiency Ratio of output power to input power, expressed as a percentage.

EIA Electronic Industries Association.

EMC	Electromagnetic Compatibility.
EMI	Electromagnetic Interference.
F	
FCC	Federal Communications Commission.
filler panel	A blank module front panel used to fill empty slots in the chassis.
G	
g	(1) grams; (2) a measure of acceleration equal to 9.8 m/s ² .
GPIO	General Purpose Interface Bus (IEEE 488).
g _{RMS}	A measure of random vibration. The root mean square of acceleration levels in a random vibration test profile.
H	
hr	Hours.
Hz	Hertz; cycles per second.
I	
IEC	International Electrotechnical Commission; an organization that sets international electrical and electronics standards.
IEEE	Institute of Electrical and Electronics Engineers.
I _{MP}	Mainframe peak current.
in.	Inches.
inhibit	To turn off.

J

jitter A measure of the small, rapid variations in clock transition times from their nominal regular intervals. Units: seconds RMS.

K

kg Kilograms.

km Kilometers.

L

lb Pounds.

LED Light emitting diode.

line regulation The maximum steady-state percentage that a DC voltage output will change as a result of a specified change in input AC voltage (step change from 90 to 132 VAC or 180 to 264 VAC).

load regulation The maximum steady-state percentage that a DC voltage output will change as a result of a step change from no-load to full-load output current.

M

m Meters.

MHz Megahertz. One million Hertz; one Hertz equals one cycle per second.

mi Miles.

ms Milliseconds.

MTBF Mean time between failure.

MTTR Mean time to repair.

N

NEMA	National Electrical Manufacturers Association.
NI	National Instruments.

P

power supply shuttle	A removable module that contains the chassis power supply.
PXI	PCI eXtensions for Instrumentation.
PXI_CLK10	10 MHz PXI system reference clock.

R

RH	Relative humidity.
RMS	Root mean square.

S

s	Seconds.
skew	Deviation in signal transmission times.
slot blocker	An assembly installed into an empty slot to improve the airflow in adjacent slots.
SMA	SubMiniature version A connector; a commonly used coaxial connector.
standby	The backplane is unpowered (off), but the chassis is still connected to AC power mains.
System controller	A module configured for installation in Slot 1 of a PXI chassis. This device is unique in the PXI system in that it performs the system controller functions, including clock sourcing and arbitration for data transfers across the backplane. Installing such a device into any other slot can damage the device, the PXI backplane, or both.

Glossary

system reference clock A 10 MHz clock, also called PXI_CLK10, that is distributed to all peripheral slots in the chassis, as well as a BNC connector on the rear of chassis labeled *10 MHz REF OUT*. The system reference clock can be used for synchronization of multiple modules in a measurement or control system. The 10 MHz REF IN and OUT BNC connectors on the rear of the chassis can be used to synchronize multiple chassis to one reference clock. The PXI backplane specification defines implementation guidelines for PXI_CLK10.

System Timing slot This slot is located at slot 4 and has dedicated trigger lines to other slots.

T

TTL Transistor-transistor logic.

U

UL Underwriter's Laboratories.

V

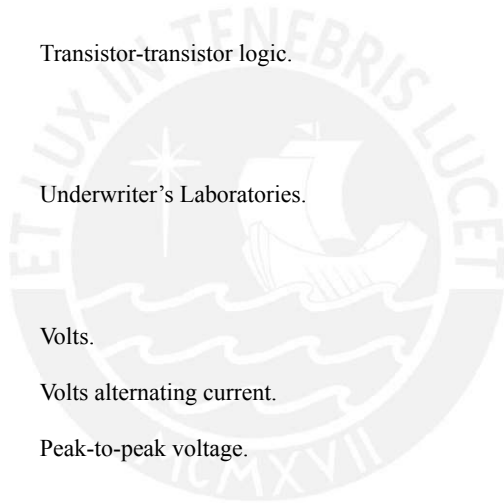
V Volts.

VAC Volts alternating current.

V_{pp} Peak-to-peak voltage.

W

W Watts.



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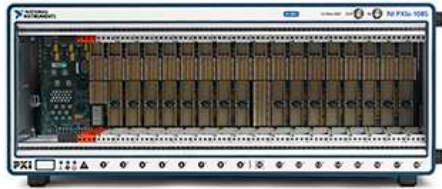
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For user manuals and dimensional drawings, visit the product page resources tab on ni.com.

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18-Slot, All-Hybrid PXI Express Chassis

NI PXIe-1085



- 16 hybrid slots, 1 PXI Express system timing slot
- Up to 8 GB/s per-slot dedicated bandwidth, 24 GB/s system bandwidth
- 925 W total power for 0 to 55 °C
- 38.25 W power and cooling capability per slot
- Ethernet port to monitor chassis component health
- Hot-swappable rear cooling fans
- Removable power supply
- Variable speed fan controller optimizes cooling and acoustic emissions
- Accepts 3U PXI, PXI Express, CompactPCI, and CompactPCI Express modules
- Complies with PXI and CompactPCI specifications

Overview

The NI PXIe-1085 18-slot chassis features a high-bandwidth, all-hybrid backplane to meet a wide range of high-performance test and measurement application needs. The hybrid connector type in every peripheral slot enables the most flexibility in terms of instrumentation module placement. It also incorporates all the features of the latest PXI specification including support for both PXI and PXI Express modules with a built-in 10 MHz reference clock, PXI trigger bus, and PXI star trigger for PXI modules and a built-in 100 MHz reference clock, SYNC100, and PXI differential star trigger for PXI Express modules.

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Application and Technology

High Performance

- Up to 8 GB/s per-slot in all slots, 24 GB/s system bandwidth
- All hybrid peripheral slots
- 925 W from 0 to 55 °C without derating
- 38.25 W power and cooling per-slot for filled chassis

Multichassis Synchronization

- PXI Express system timing slot for tight synchronization across chassis
- Front CLK10 I/O connectors
- Switchless CLK10 routing

Optional Features

- Front and rear rack-mount kits
- Replacement power supply and fans
- Filler panels
- Slot blockers for improved cooling performance
- System assurance programs

Slot	PXI Express System (Controller)	Hybrid (PXI)
Bus Signaling	PCI Express Gen 3 (1 x16, 1 x8)	PCI Express Gen 3 (x8) PCI (32/33)
Bandwidth (theoretical)	24 GB/s dedicated for PXI Express 132 MB/s shared for PXI	8 GB/s dedicated (PXI Express) ¹ 132 MB/s shared (PXI)
Number of Slots	1	16

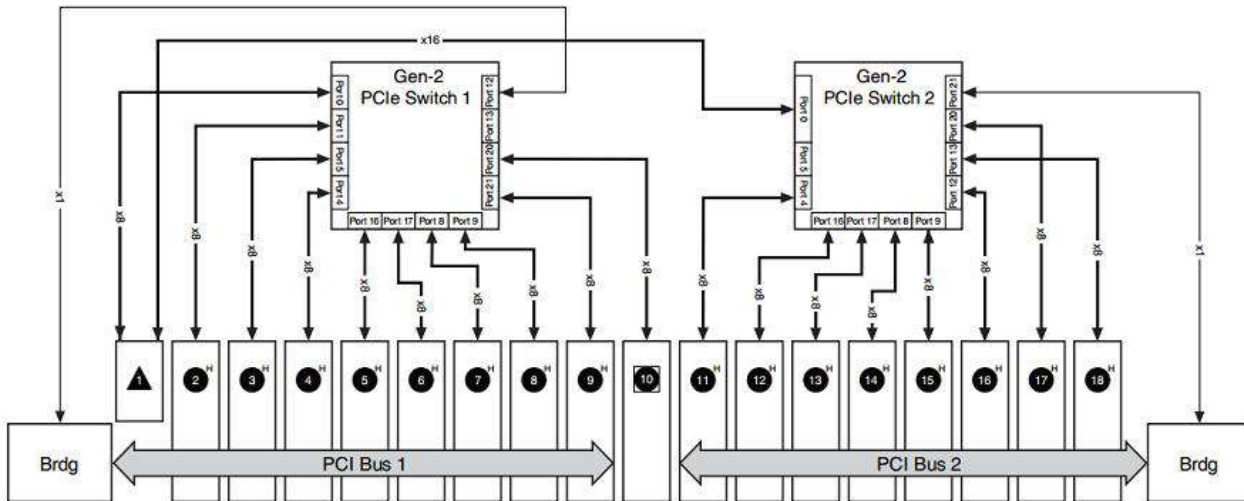
¹ Each slot provides up to 4 GB/s dedicated bandwidth; however, 12 GB/s total bandwidth is shared across all devices.

Slot Types Accept PXI and PXI Express Modules

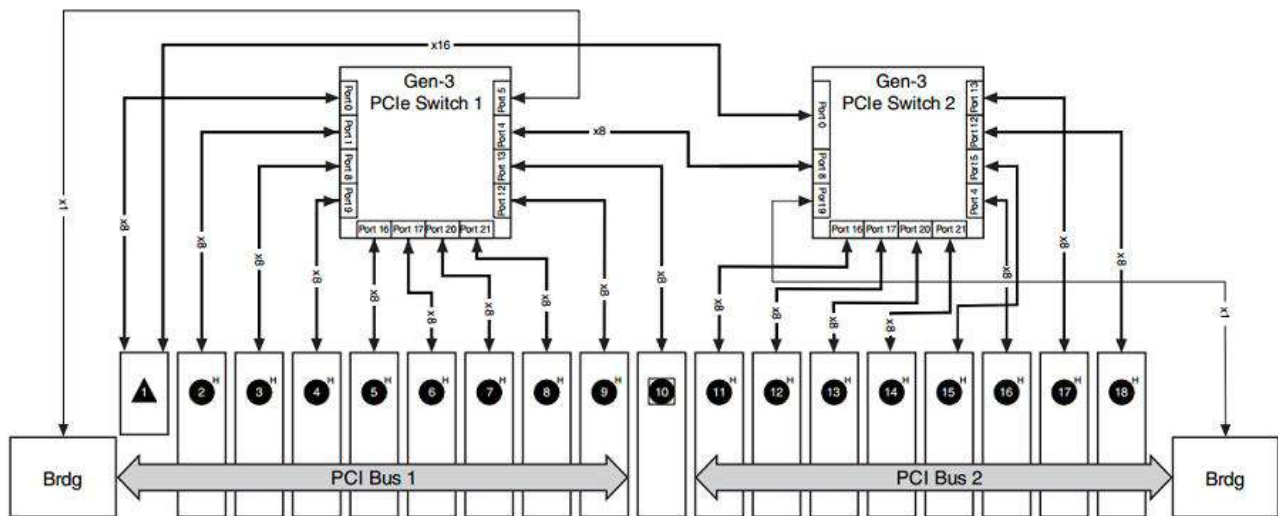
This chassis enables higher-bandwidth systems and provides the flexibility you need to work with both hybrid-compatible PXI and PXI Express modules. There are a total of 16 PXI hybrid-compatible slots and one PXI Express system timing slot that can accept either a PXI Express system timing module or PXI Express module.

The PXI Express system slot offers one x16 and one x8 PCI Express Gen 3 link to two switches. Each switch provides a x8 PCI Express link to eight or nine peripheral slots. Also, each slot is capable of up to 8 GB/s dedicated bandwidth; however, 24 GB/s total bandwidth is shared across all devices.

There are also two x1 PCI Express links to two PCI Express-to-PCI translation bridges on the backplane. The PXI Express system timing slot accepts a PXI Express module or a PXI Express system timing controller for advanced timing and synchronization. The PXI Express hybrid slots deliver connectivity to either a x8 PCI Express link or to the 32-bit, 33 MHz PCI bus on the backplane.



NI PXIe-1085 12 GB/s Chassis Backplane



NI PXIe-1085 24 GB/s Chassis Backplane

Optimized Cooling and Acoustic Emissions

The NI PXIe-1085 chassis integrates three PWM system fans to provide forced-air cooling that meets the increased cooling demands of PXI Express and CompactPCI Express. It offers a HIGH fan setting to maximize cooling at any ambient temperature and an AUTO fan setting to minimize acoustic emissions at ambient temperatures below 30 °C. The chassis monitors air intake temperature and adjusts fan speed accordingly. With this technology, the NI PXIe-1085 achieves acoustic noise levels as low as 51 dBA (sound pressure level measured at operator position according to ISO 7779).

PXI Timing and Synchronization

For PXI modules, the NI PXIe-1085 backplane is fully compliant with PXI timing and synchronization standards. The chassis includes a 10 MHz reference clock with an accuracy of ± 25 parts per million (ppm), less than 5 ps jitter, and a maximum slot-to-slot skew of 1 ns. For triggering and handshaking needs, the NI PXIe-1085 offers the PXI trigger bus and PXI star trigger. PXI modules should be designed for use in PXI hybrid-compatible slots.

For PXI Express modules, in addition to PXI timing and synchronization features, the NI PXIe-1085 backplane supplies a differential 100 MHz reference clock with an accuracy of ± 25 ppm, less than 3 ps jitter, and a maximum slot-to-slot skew of 100 ps. The chassis also provides differential star triggers to the PXI Express slots to offer less than 200 ps intermodule skew. With the SYNC100, a peripheral module installed in the NI PXIe-1085 can generate its own CLK10 signal, deriving it from the 100 MHz reference clock.

Individually Replaceable Power Supply and Cooling Fans

The NI PXIe-1085 incorporates the power supply components into a modular unit that you can replace quickly, resulting in a mean time to repair (MTTR) of less than five minutes. Additionally, the three cooling fans are hot-swappable and easily replaceable with access to the rear of the chassis.

Power Supply, Temperature, and Fan Monitoring

The NI PXIe-1085 chassis monitors power supply health/voltages, air intake temperature, and fan health/speed. It also provides any failure feedback to the user via status LEDs located on the front bezel of the chassis. Furthermore, you can monitor the chassis' health information remotely through the use of the Ethernet connection on the rear of the chassis via a web service portal.

External 10 MHz Reference Clock I/O Connectors

This chassis includes IN/OUT SMA connectors for the 10 MHz reference clock on the front of the chassis. When the backplane detects a 10 MHz signal on the IN connector, it phase locks PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 to the external clock. The OUT connector provides a buffered, non-TTL version of the 10 MHz reference clock.

High-Performance Platform

For unlocking the full high-throughput capabilities of the NI PXIe-1085, National Instruments recommends the NI PXIe-8880 embedded controller. The combination of these PXI Express platform products enables more high-performance instruments streaming at their maximum rate to be combined in a single chassis.

Software System Configuration

The NI PXIe-1085 chassis is configured with NI Measurement & Automation Explorer (MAX). With this software configuration tool, you can easily configure NI PXIe-1085 systems without time-consuming manual installation of initialization files. MAX creates the pxisys.ini file that defines the layout and parameters of your PXI system including chassis, controller, and plug-in modules.

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Ordering Information

For a complete list of accessories, visit the product page on ni.com.

Products	Part Number	Recommended Accessories	Part Number
Related Accessories			
18-Slot Chassis Filler Panel Kit (to cover 17 slots)	778646-01	No accessories required.	
NI 14/18-Slot Chassis Rear Rack Mount Kit	778644-02	No accessories required.	
NI PXI Slot Blocker, Set of 5	199198-01	No accessories required.	
Replacement Power Supply for NI PXIe-1085	781719-01	No accessories required.	
NI 14/18-Slot Chassis Front Rack Mount Kit	778644-01	No accessories required.	
Replacement Fan Assembly for NI PXIe-1085	782459-01	No accessories required.	
NI PXIe-1085			
NI PXIe-1085, 18-Slot 3U PXI Express Chassis, 12 GB/s System BW Requires: 1 Cable	781813-01	Cable: Shielded - Power Cord, AC, U.S., 125 VAC, 15 A	763830-01
		Cable: Shielded - Power Cord, 240 V, 10 A, North American	763068-01
NI PXIe-1085, 18-Slot 3U PXI Express Chassis, 24 GB/s System BW Requires: 1 Cable	783588-01	Cable: Shielded - Power Cord, AC, U.S., 125VAC, 15A	763830-01
		Cable: Shielded - Power Cord, 240 V, 10 A, North American	763068-01

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Support and Services

System Assurance Programs

NI system assurance programs are designed to make it even easier for you to own an NI system. These programs include configuration and deployment services for your NI PXI, CompactRIO, or Compact FieldPoint system. The NI Basic System Assurance Program provides a simple integration test and ensures that your system is delivered completely assembled in one box. When you configure your system with the NI Standard System Assurance Program, you can select from available NI system driver sets and application development environments to create customized, reorderable software configurations. Your system arrives fully assembled and tested in one box with your software preinstalled. When you order your system with the standard program, you also receive system-specific documentation including a bill of materials, an integration test report, a recommended maintenance plan, and frequently asked question documents. Finally, the standard program reduces the total cost of owning an NI system by providing three years of warranty coverage and calibration service. Use the online product advisors at ni.com/advisor to find a system assurance program to meet your needs.

Technical Support

Get answers to your technical questions using the following National Instruments resources.

- **Support** - Visit ni.com/support to access the NI KnowledgeBase, example programs, and tutorials or to contact our applications engineers who are located in NI sales offices around the world and speak the local language.
- **Discussion Forums** - Visit forums.ni.com for a diverse set of discussion boards on topics you care about.
- **Online Community** - Visit community.ni.com to find, contribute, or collaborate on customer-contributed technical content with users like you.

Repair

While you may never need your hardware repaired, NI understands that unexpected events may lead to necessary repairs. NI offers repair services performed by highly trained technicians who quickly return your device with the guarantee that it will perform to factory specifications. For more information, visit ni.com/repair.

Training and Certifications

The NI training and certification program delivers the fastest, most certain route to increased proficiency and productivity using NI software and hardware. Training builds the skills to more efficiently develop robust, maintainable applications, while certification validates your knowledge and ability.

- **Classroom training in cities worldwide** - the most comprehensive hands-on training taught by engineers.
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- **Online instructor-led training** - lower-cost, remote training if classroom or on-site courses are not possible.
- **Course kits** - lowest-cost, self-paced training that you can use as reference guides.
- **Training memberships** and training credits - to buy now and schedule training later.

Visit ni.com/training for more information.

Extended Warranty

NI offers options for extending the standard product warranty to meet the life-cycle requirements of your project. In addition, because NI understands that your requirements may change, the extended warranty is flexible in length and easily renewed. For more information, visit ni.com/warranty.

OEM

NI offers design-in consulting and product integration assistance if you need NI products for OEM applications. For information about special pricing and services for OEM customers, visit ni.com/oem.

Alliance

Our Professional Services Team is comprised of NI applications engineers, NI Consulting Services, and a worldwide National Instruments Alliance Partner program of more than 700 independent consultants and integrators. Services range from start-up assistance to turnkey system integration. Visit ni.com/alliance.

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Detailed Specifications


This appendix contains specifications for the NI PXIe-1085 chassis.



Caution Specifications are subject to change without notice.

Electrical	
AC Input	
Input voltage rating	100 to 240 VAC
Operating voltage range ¹	90 to 264 VAC
Input frequency	50/60 Hz
Operating frequency range ¹	47 to 63 Hz
Input current rating	12–6 A
Over-current protection	15 A circuit breaker
Line regulation	
3.3 V	<±0.2%
5 V	<±0.1%
±12 V	<±0.1%
Efficiency	70% typical
Power disconnect	The AC power cable provides main power disconnect. Do not position the equipment so that it is difficult to disconnect the power cord. The front-panel power switch causes the internal chassis power supply to provide DC power to the CompactPCI/PXI Express backplane. You also can use the rear-panel 8-pin connector and inhibit mode switch to control the internal chassis power supply.
DC Output	

DC current capacity (I_{MP})	
Voltage	Maximum Current
+3.3 V	61 A
+5 V	48 A
+12 V	62 A
-12 V	4 A
5 V _{AUX}	2.0 A

 **Notes** Maximum combined +3.3 V, +5 V, and +12 V power is 699 W.

Maximum total usable power is 701.5 W.

Backplane slot current capacity						
Slot	+5 V	V (I/O)	+3.3 V	+12 V	-12 V	5 V _{AUX}
System Controller Slot	15 A	-	15 A	30 A	-	1 A
System Timing Slot	-	-	6 A	4 A	-	1 A
Hybrid Peripheral Slot with PXI-1 Peripheral	6 A	5 A	6 A	1 A	1 A	-
Hybrid Peripheral Slot with PXI-5 Peripheral	-	-	6 A	4 A	-	1 A
PXI-1 Peripheral Slot	6 A	11 A	6 A	1 A	1 A	-

Notes Total system slot current should not exceed 45 A.

PCI V(I/O) pins in PXI-1 peripheral slots and hybrid peripheral slots are connected to +5 V.

The maximum power dissipated in the system slot should not exceed 140 W.

The maximum power dissipated in a peripheral slot should not exceed 38.25 W.



Load regulation	
Voltage	Load Regulation
+3.3 V	<5%
+12 V	<5%
+5 V	<5%
-12 V	<5%

Maximum ripple and noise (20 MHz bandwidth)	
Voltage	Maximum Ripple and Noise
+3.3 V	50 mV _{pp}
+12 V	50 mV _{pp}
+5 V	50 mV _{pp}
-12 V	50 mV _{pp}






Over-current protection All outputs protected from short circuit and overload with automatic recovery

Over-voltage protection
3.3 V and 5 V Clamped at 20 to 30% above nominal output voltage

Power supply shuttle MTTR Replacement in under 5 minutes

Chassis Cooling

Module cooling system	
NI PXIe-1085	Forced air circulation (positive pressurization) through three 169 cfm fans with High/Auto speed selector
Slot airflow direction	Bottom of module to top of module
Module cooling intake	Bottom rear of chassis
Module cooling exhaust	Along both sides and top of chassis

Power supply cooling system	Forced air circulation through two integrated fans
Power supply cooling intake	Right side of chassis
Power supply cooling exhaust	Left side of chassis
Environmental	
Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient)
Pollution Degree	2
For indoor use only.	
Operating Environment	
Ambient temperature range	0 to 55 °C (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.)
Relative humidity range	10 to 90%, noncondensing (Tested in accordance with IEC-60068-2-56.)
Storage Environment	
Ambient temperature range	-40 to 71 °C (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 limits.)
Relative humidity range	5 to 95%, noncondensing (Tested in accordance with IEC-60068-2-56.)
Shock and Vibration	
Operational shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC-60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)
Random Vibration	5 to 500 Hz, 0.3 g _{rms}
Acoustic Emissions	
Sound Pressure Level (at Operator Position)	
(Tested in accordance with ISO 7779. Meets MIL-PRF-28800F requirements.)	
Auto fan (up to ~30 °C ambient)	51.2 dBA
High fan	64.1 dBA
Sound Power	
Auto fan (up to ~30 °C ambient)	60.8 dBA
High fan	75.9 dBA
 Note Specifications are subject to change without notice.	
Safety	
This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:	
<ul style="list-style-type: none"> IEC 61010-1, EN 61010-1 UL 61010-1, CSA 61010-1 	
 Note For UL and other safety certifications, refer to the product label or the <i>Online Product Certification</i> section.	
Electromagnetic Compatibility	
This product is designed to meet the requirements of the following standards of EMC for electrical equipment for measurement, control, and laboratory use:	
<ul style="list-style-type: none"> EN 61326 (IEC 61326): Class A emissions; Basic immunity EN 55011 (CISPR 11): Group 1, Class A emissions AS/NZS CISPR 11: Group 1, Class A emissions FCC 47 CFR Part 15B: Class A emissions ICES-001: Class A emissions 	
 Note For the standards applied to assess the EMC of this product, refer to the Online Product Certification section.	
 Note For EMC compliance, operate this device with shielded cabling.	
CE Compliance 	

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)



EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste Electrical and Electronic Equipment, visit ni.com/environment/weee.htm.

Backplane

Size	3U-sized; one system slot (with three system expansion slots) and 17 peripheral slots. Compliant with IEEE 1101.10 mechanical packaging. PXI Express Specification compliant. Accepts both PXI Express and CompactPCI (PICMG 2.0 R 3.0) 3U modules.
Backplane bare-board material	UL 94 V-0 Recognized
Backplane connectors	Conforms to IEC 917 and IEC 1076-4-101, and are UL 94 V-0 rated

System Synchronization Clocks (PXI_CLK10, PXIe_CLK100, PXIe_SYNC100)

10 MHz System Reference Clock: PXI_CLK10

Maximum slot-to-slot skew	1 ns
Accuracy	±25 ppm max. (guaranteed over the operating temperature range)
Maximum jitter	5 ps RMS phase-jitter (10 Hz–1 MHz range)
Duty-factor	45%–55%
Unloaded signal swing	3.3 V ±0.3 V

Note For other specifications refer to the *PXI-1 Hardware Specification*.

100 MHz System Reference Clock: PXIe_CLK100 and PXIe_SYNC100

Maximum slot-to-slot skew	100 ps
Accuracy	±25 ppm max. (guaranteed over the operating temperature range)
Maximum jitter	3 ps RMS phase-jitter (10 Hz–12 kHz range) 2 ps RMS phase-jitter (12 kHz–20 MHz range)
Duty-factor for PXIe_CLK100	45%–55%
Absolute single-ended voltage swing (When each line in the differential pair has 50 W termination to 1.30 V or Thévenin equivalent)	400–1000 mV

Note For other specifications refer to the *PXI-5 PXI Express Hardware Specification*.

External 10 MHz Reference Out (SMA on front panel of chassis)

Accuracy	±25 ppm max. (guaranteed over the operating temperature range)
Maximum jitter	5 ps RMS phase-jitter (10 Hz–1 MHz range)
Output amplitude	1 V _{PP} ±20% square-wave into 50 Ω 2 V _{PP} unloaded
Output impedance	50 Ω ±5 Ω

External Clock Source

Frequency	10 MHz \pm 100 PPM
Input amplitude	
Rear panel BNC	200 mV _{pp} to 5 V _{pp} square-wave or sine-wave
System timing slot PXI_CLK10_IN	5 V or 3.3 V TTL signal
Rear panel BNC input impedance	50 Ω \pm 5 Ω
Maximum jitter introduced by backplane	1 ps RMS phase-jitter (10 Hz–1 MHz range)

PXIe_SYNC_CTRL

V _{IH}	2.0–5.5 V
V _{IL}	0–0.8 V

PXI Star Trigger

Maximum slot-to-slot skew	250 ps
Backplane characteristic impedance	65 Ω \pm 10%



Note For PXI slot to PXI Star mapping refer to the *System Timing Slot* section of the *NI PXIe-1085 User Manual*. For other specifications refer to the *PXI-1 Hardware Specification*.

PXI Differential Star Triggers (PXIe-DSTARA, PXIe-DSTARB, PXIe-DSTARC)

Maximum slot-to-slot skew	150 ps
Maximum differential skew	25 ps
Backplane differential impedance	100 Ω \pm 10%



Note For PXIe slot to PXI_DSTAR mapping refer to the *System Timing Slot* section of the *NI PXIe-1085 User Manual*. For other specifications, the NI PXIe-1085 complies with the *PXI-5 PXI Express Hardware Specification*.

Mechanical

Overall dimensions	
Standard chassis	
Height	6.97 in. (177.1 mm)
Width	17.54 in. (445.5 mm)
Depth	20.33 in. (516.4 mm)
Note 0.57 in. (14.5 mm) is added to height when feet are installed. When tilted with front feet extended on table top, height is increased approximately 2.08 in. (52.8 mm) in front and 0.583 in. (14.8 mm) in rear.	
Weight	18.28 kg (40.3 lb)
Chassis materials	Sheet Aluminum (5052-H32, 5754-H22), Extruded Aluminum (6063-T5, 6060-T6), Plate Aluminum (6063-T5, 6061-T6), Cold Rolled Steel, Cold Rolled Stainless Steel, Sheet Copper (C110), Santoprene, Urethane Foam, PC-ABS, Nylon, Polycarbonate, Delrin, Polyethylene, Polyamide (FR 106), Neodymium Magnet
Finish	Conductive Clear Iridite on Aluminum, Electroplated Nickel on Cold Rolled Steel, Electroplated Zinc on Cold Rolled Steel, Electroplated Nickel on Copper

Figures A-1 and A-2 show the NI PXIe-1085 chassis dimensions. The holes shown are for the installation of the optional rack mount kits. You can install those kits on the front or rear of the chassis, depending on which end of the chassis you want to face toward the front of the instrument cabinet. Notice that the front and rear chassis mounting holes (size M4) are symmetrical.

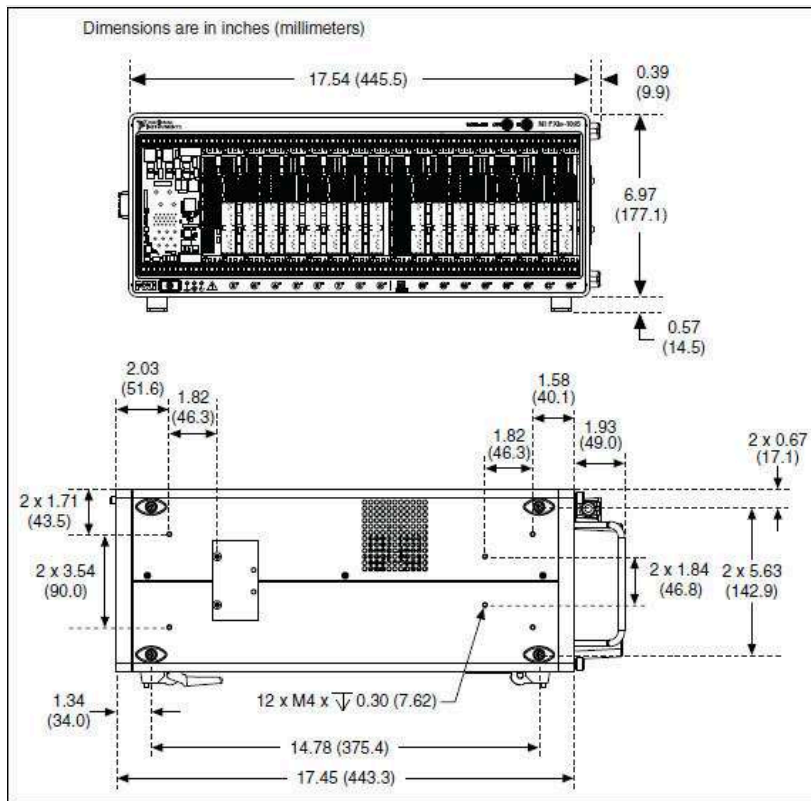


Figure A-1. NI PXle-1085 Chassis Dimensions (Front and Side)

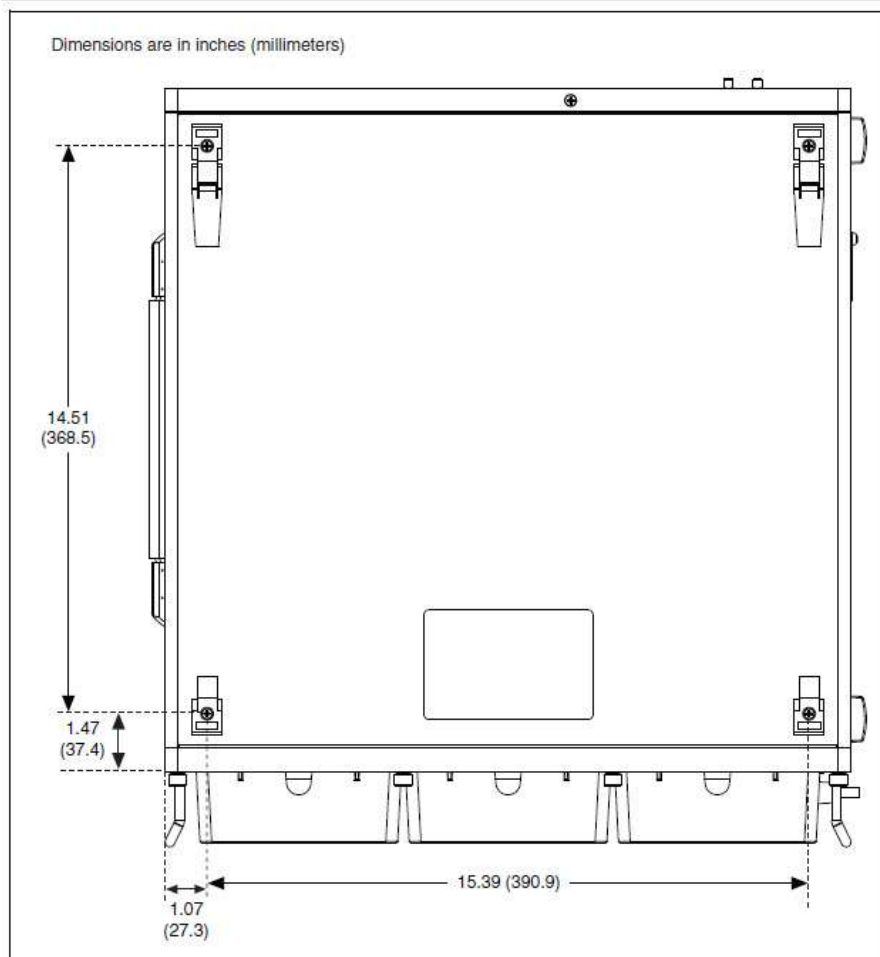


Figure A-2. NI PXle-1085 Chassis Dimensions (Bottom)

Figure A-3 shows the chassis rack mount kit components.

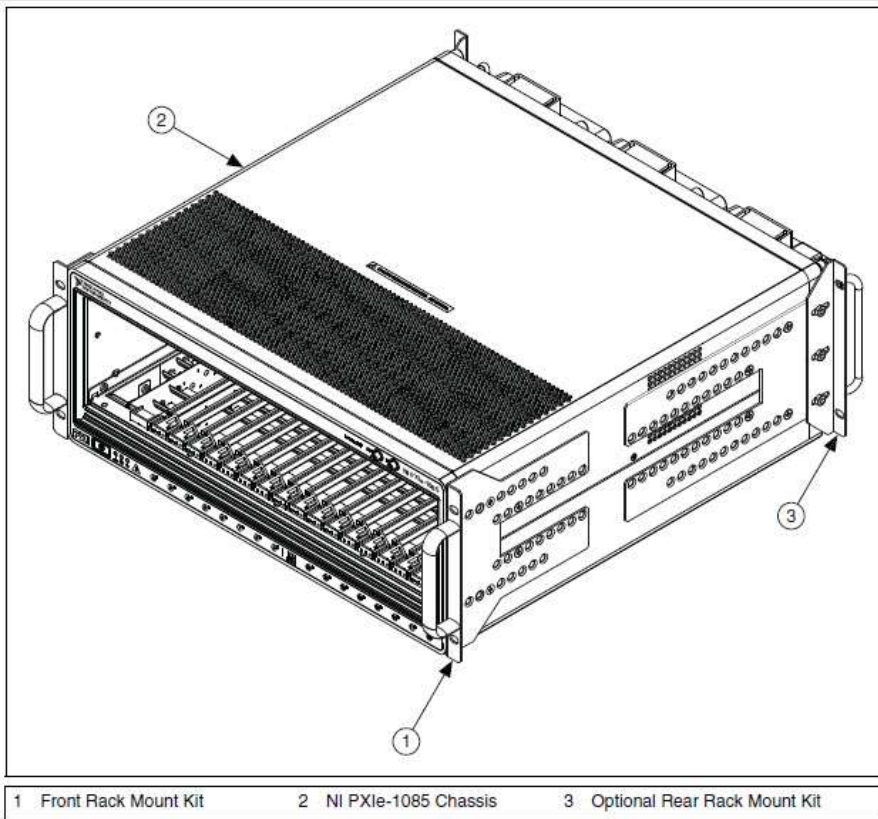


Figure A-3. NI Chassis Rack Mount Kit Components

¹ The operating range is guaranteed by design.

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2.3 GHz Quad-Core Embedded Controller for PXI Express

NI PXIe-8135



- Intel Core i7-3610QE quad-core processor (2.3 GHz (base), 3.3 (single-core Turbo Boost))
- Up to 8 GB/s system, up to 4 GB/s slot bandwidth
- 4 GB (1 x 4 GB DIMM) dual-channel 1600 MHz DDR3 standard, 16 GB (2 x 8 GB DIMM) maximum
- High-performance 7200 rpm integrated hard drive with standard option
- Six USB ports - 2 SuperSpeed USB, 4 Hi-Speed USB
- Two 10/100/1000BASE-TX Ethernet ports
- Other peripherals (GPIB (IEEE 488) controller, RS232 serial port, and IEEE 1284 ECP/EPP parallel port)
- In-ROM memory and hard drive diagnostics
- Software - already installed OS and drivers and hard-drive-based recovery image
- Complete PXI system configuration at ni.com/pxiadvisor

Overview

The NI PXIe-8135 is a high-performance Intel Core i7-3610QE processor-based embedded controller for PXI Express systems. With the 2.3 GHz base frequency, 3.3 GHz (single-core Turbo Boost) quad-core processor, and dual-channel 1600 MHz DDR3 memory, the NI PXIe-8135 is ideal for processor-intensive, modular instrumentation, and data acquisition applications.

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Requirements and Compatibility

OS Information

- Windows 7
- Windows XP

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Application and Technology

NI PXIe-8135 Features

CPU	Intel Core i7-3610QE, 2.3 GHz (base), 3.3 GHz (single-core Turbo Boost mode), 3.2 GHz (dual-core Turbo Boost mode), 3.1 GHz (quad-core Turbo Boost mode) ¹
L3 cache	6 MB shared Intel smart cache
System bandwidth	Up to 8 GB/s
Slot bandwidth	Up to 4 GB/s
PXI Express 4-link configuration	Four x4 links or two x8 links
Dual-channel 1600 MHz DDR3 RAM, standard	4 GB (1 x 4 GB)
Dual-channel 1600 MHz DDR3 RAM, maximum	16 GB (2 x 8 GB)

Hard drive (standard option), minimum	250 GB SATA (7200 rpm)
Hard drive (extended temperature and 24/7 option), minimum	80 GB SATA (5400 rpm)
10/100/1000BASE-TX (Gigabit) Ethernet ports	2
SuperSpeed USB ports	2
Hi-Speed USB ports	4
GPIO (IEEE 488) controller	
Serial port (RS232)	
Parallel port	
Watchdog/trigger SMB	
Installed OS ²	Windows 7 Professional, Windows XP Professional SP3 for Embedded Systems ³

¹ Processor should not throttle CPU frequency under reasonable, worst-case processor workloads in high operating temperature.

² Contact National Instruments or visit ni.com/pxiadvisor for information on other available operating systems.

³ Windows XP Pro for Embedded Systems contains the same software bits and operates identically to Windows XP Pro. The main difference is the licensing that is used for Windows XP Pro for Embedded Systems.

Due to the [Microsoft support life cycle](#) for Windows XP, National Instruments will be unable to provide PXI embedded controllers with Windows XP preinstalled after 2015. View the [Microsoft support life cycle](#) for full details about Windows XP end of life for OEM partners.

Table 1. NI PXIe-8135 Features

Quad-Core Processor

The NI PXIe-8135 includes the quad-core Intel Core i7-3610QE processor. Quad-core processors contain four cores, or computing engines, in one physical package. To increase the number of threads that you can process, the NI PXIe-8135 incorporates Intel Hyper-Threading technology that takes each of the four physical cores and splits them into two virtual cores, for a total of eight virtual cores. These eight virtual cores can execute eight computing tasks, which is advantageous in multitasking environments such as Windows 7. Multithreaded system development environments, such as NI LabVIEW, can take full advantage of the processing cores on the NI PXIe-8135 by automatically separating their tasks into independent threads. Figure 1 compares the SYSmark 2012 overall performance of the NI PXIe-8135 controller with other PXI embedded controllers.

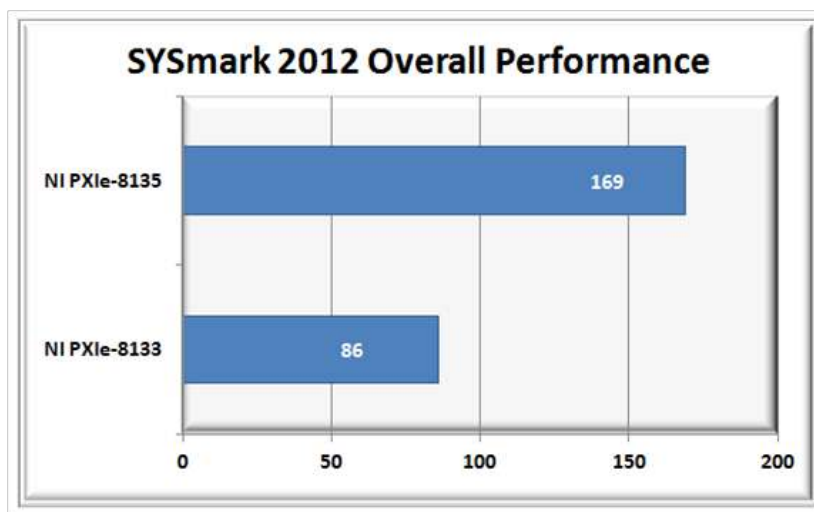


Figure 1. The NI PXIe-8135 provides up to 97 percent better performance than the NI PXIe-8133 embedded controller.

Previously, to fully exercise the four physical cores on the NI PXIe-8135, applications had to be architected to create four independent execution threads by implementing programming strategies such as task parallelism, data parallelism, and pipelining. However, Intel introduced Turbo Boost technology to provide performance benefits for all types of applications without requiring the application to be optimized for multicore processors. The NI PXIe-8135 has a 2.3 GHz base clock frequency, and, with Intel Turbo Boost technology, the frequency automatically increases based on the application type. For example, when running applications that generate only a single processing thread, the CPU places the three unused cores into an idle state and increases the active core's clock frequency from 2.3 to 3.3 GHz.¹ For applications that are processing two threads, the CPU places the two unused cores into an idle state and increases the active core's clock frequency from 2.3 to 3.2 GHz.¹ For applications using four threads, the CPU increases from 2.3 to 3.1 GHz.¹ Turbo Boost provides performance increases for all types of applications and can significantly reduce test times for applications that are processor-intensive.

¹Processor should not throttle CPU frequency under reasonable, worst-case processor workloads in high operating temperatures.

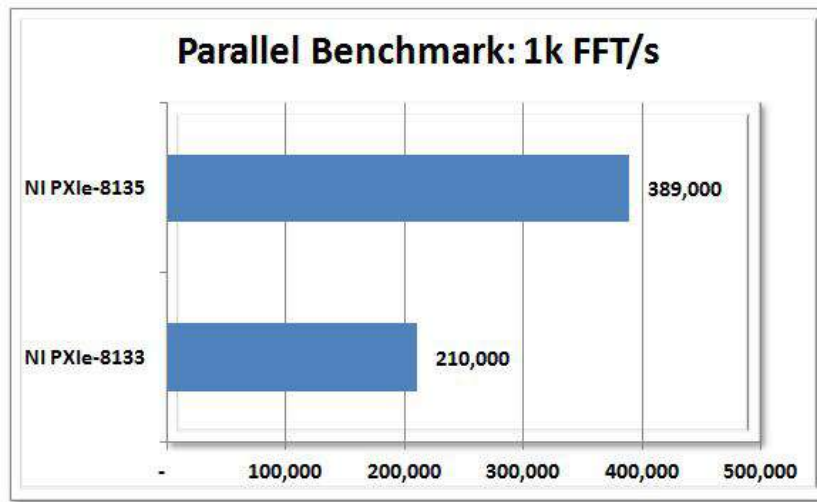


Figure 2. The NI PXIe-8135 can process 389,000 1K FFTs per second, which is up to 85 percent faster than the NI PXIe-8133 embedded controller.

High Bandwidth

This controller features the Intel Core i7-3610QE processor and takes advantage of advancements in PCI Express technology. This processor provides four x4 (“by four”) PCI Express Gen 2 lanes to the PXI chassis backplane. This generates up to 4 GB/s of dedicated slot bandwidth with the overall system bandwidth of up to 8 GB/s. Pairing the NI PXIe-8135 with a PXI Express chassis, such as the NI PXIe-1085, you can simultaneously stream a larger set of I/O channels to the controller’s system RAM, allowing for the creation of larger and more complex data record and playback applications. For example, by using an NI PXIe-1085 PXI Express chassis and an NI PXIe-8135 embedded controller, you can stream data from 32 input channels with 16-bit resolution sampled at 100 MS/s into system memory for analysis or postprocessing.

Building Hybrid Test Systems

The NI PXIe-8135 has two Ethernet ports, which enable the development of a hybrid test system. With the ability to use the second Ethernet port, you can combine multiple buses into your test systems. By taking advantage of hybrid test systems that combine components from multiple platforms, you can integrate new buses into existing test systems to help balance design considerations, take advantage of various technologies, and extend the life of your systems.

Hardware

With state-of-the-art packaging, the NI PXIe-8135 integrates the Intel Core i7-3610QE processor and all standard and extended PC I/O ports into a single unit. Because many of the I/O ports on the controller are integrated, all active slots in the chassis remain available for measurement and control modules. This rugged controller design minimizes integration issues and eliminates the need for complex cabling to daughter boards. The NI PXIe-8135 block diagram is shown in Figure 3.

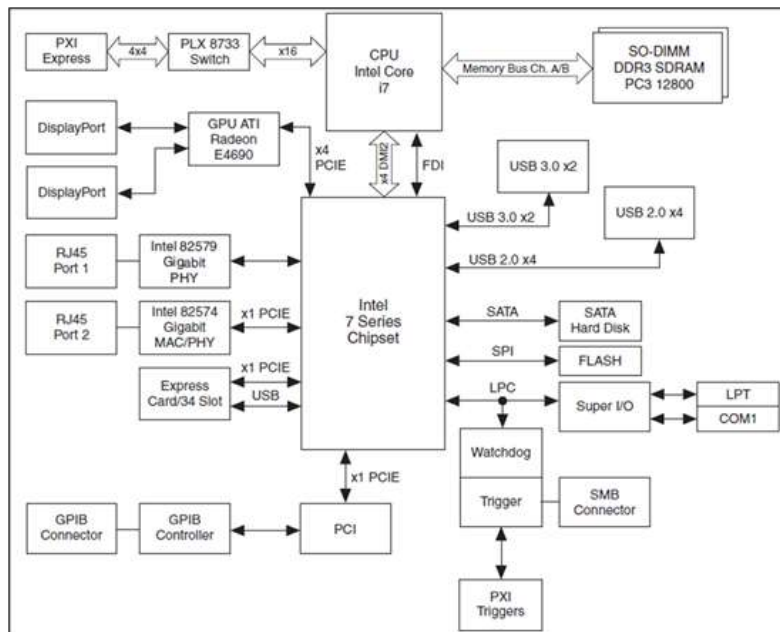


Figure 3. NI PXIe-8135 Block Diagram

Peripheral I/O

This module includes high-performance peripheral I/O such as two 10/100/1000BASE-TX (Gigabit) Ethernet ports, two SuperSpeed USB ports, and four Hi-Speed USB ports for connection to a keyboard, mouse, CD-ROM/DVD-ROM drive for software installation, or other standard PC peripherals such as speakers, printers, or memory sticks. Use the IEEE 1284 ECP/EPP parallel port to connect to a wide variety of devices, including tape backup drives and printers. An RS232 port is available for connecting to serial devices. Additionally, the NI PXIe-8135 controller includes an integrated GPIB (IEEE 488) controller, which provides control of external instrumentation, saving additional cost and a slot.

Video

The NI PXIe-8135 includes an integrated ATI Radeon E4690 graphics processing unit, which delivers intense, realistic 3D graphics with sharp images, fast rendering, smooth motion, and high detail, without the need for an additional video card or peripheral. This unique architecture provides balanced memory usage between graphics and the system

for optimal performance. Additionally, the NI PXIe-8135 features two Display Port video connectors. A Display Port to VGA adapter is included with the controller for use with VGA monitors. For information on approved Display Port to DVI adapters, reference this [KnowledgeBase](#).

Dual Monitor Support

The dual Display Port video ports on the NI PXIe-8135 support simultaneous output. With this built-in capability, you can connect two monitors to your PXI system at the same time with independent displays. This negates the need for a separate PXI or CompactPCI video module to connect two monitors to your PXI system.

Memory

The NI PXIe-8135 uses dual-channel 1600 MHz DDR3 SDRAM, which makes the controller ideal for data-intensive applications requiring significant analysis. It has two SO-DIMM sockets for the DDR3 SDRAM. 4 GB (1 x 4 GB DIMM) of RAM is standard with upgrade options to 16 GB.

Memory Options	Configuration	Part Number	
		Included in Kit	Additional P/N Required
Standard - 4 GB	1 x 4 GB DIMM	1 x 4 GB DIMM	N/A
8 GB	2 x 4 GB DIMM	1 x 4 GB DIMM	Add 1 x 782341-4096
12 GB	1 x 4 GB DIMM and 1 x 8 GB DIMM	1 x 4 GB DIMM	Add 1 x 782341-8192
16 GB	2 x 8 GB DIMM	N/A	2 x 782341-8192

Table 2. Memory Upgrade Options

Extended Temperature and 24/7 Operation Option

You can choose from two versions of the NI PXIe-8135 embedded controller to address different environmental and usage conditions. The primary difference between the versions is that the version for extended temperature and 24/7 operation uses a different hard drive that is designed for both reliability in low- and high-temperature extremes and 24/7 operation. The standard version of the controllers has an operating temperature of 5 to 50 °C and a storage temperature of -40 to 65 °C. The extended temperature and 24/7 operation version has an operating temperature of 0 to 55 °C and a storage temperature of -40 to 70 °C.

You can also use the extended temperature and 24/7 operation version for applications that require continuous operation for up to 24 hours/day, seven days/week because the hard drive is rated for 24/7 operation. The hard drive in the standard version of the controllers is designed to be powered on for eight hours/day, five days/week. Additionally, 24/7 operation applications may subject the hard drive to a high-duty cycle (the percentage of the maximum sustained throughput of the hard drive). The hard drive in the extended temperature and 24/7 operation version has a capacity of 80 GB (minimum). See specifications for further details.

USB Peripherals

National Instruments offers a USB-to-dual-PS/2 keyboard/mouse adapter cable to connect a legacy PS/2 keyboard and mouse to a single USB port on your embedded controller. Additionally, NI offers external USB CD-ROM/DVD-ROM and USB floppy drives for use with your embedded controller. Connect these drives to your embedded controller for easy software installation and upgrades. Both are completely powered through the USB ports, so no external power connections are required. Additional USB peripherals, such as USB speakers to add audio or USB memory sticks to add easily removable memory, are widely available from PC peripheral manufacturers.

In-ROM Memory and Hard-Drive Diagnostics

To improve the serviceability of the NI PXIe-8135, in-ROM diagnostics for the hard drive and memory can be quickly accessed without requiring external third-party tools. By running these diagnostics, the results of analysis can determine if replacement of the hard drive or memory is required. The design of the controller allows for quick field replacement of critical components such as the hard drive and the memory without affecting the warranty. To ease the process of buying spare components, you can purchase hard drive and memory upgrades with the NI PXIe-8135. The combination of this and the in-ROM diagnostics significantly improves NI PXIe-8135 serviceability.

Hard-Drive-Based Recovery Image

The NI PXIe-8135 embedded controller is shipped with a factory image of the software installation stored on a separate partition of the hard drive. In the case of software corruption, you can invoke a recovery tool during the controller's boot-up process that can use this backup image to restore the controller to its shipping software configuration. You also can use this recovery tool to create custom images that you can store on external mass storage devices such as a USB memory stick, USB hard drives, and USB CD/DVD drives. With this ability, you can create custom backup images that you can use to either recover an NI PXIe-8135 controller or replicate the installation on other NI PXIe-8135 controllers. For more information on this tool, refer to [KnowledgeBase 2ZKC02OK](#).

Software

The NI PXIe-8135 comes with the following minimum set of software already installed:

- Microsoft Windows 7 Professional OS (contact National Instruments or visit ni.com/pxiadvisor for localized versions of Windows XP and for other available OSs)
- Hard-drive-based recovery image
- NI-VISA and NI-488.2 drivers
- Drivers for all built-in I/O ports

With an NI system assurance program (base or standard) added to your PXI system order, your embedded controller is shipped already configured with all software and drivers applicable for your system. For example, assume you order a PXI system that includes NI LabVIEW and NI TestStand software, as well as data acquisition modules, a digitizer, an arbitrary waveform generator, and a digital multimeter (DMM). With an NI system assurance program, NI not only assembles and tests your system but also fully configures the embedded controller with the appropriate NI-DAQmx, NI-SCOPE, NI-FGEN, and NI-DMM drivers, as well as LabVIEW and NI TestStand.

Additionally, your embedded controller is configured with a customized hard-drive-based recovery image, so you can restore your controller to the as-shipped configuration at any time. This combination of software configuration and recovery tools provides both a productive and reliable development experience with your PXI system out of the box. To configure a complete PXI system with an NI system assurance program, contact National Instruments or visit ni.com/pxiadvisor.

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Support and Services

System Assurance Programs

NI system assurance programs are designed to make it even easier for you to own an NI system. These programs include configuration and deployment services for your NI PXI, CompactRIO, or Compact FieldPoint system. The NI Basic System Assurance Program provides a simple integration test and ensures that your system is delivered completely assembled in one box. When you configure your system with the NI Standard System Assurance Program, you can select from available NI system driver sets and application development environments to create customized, reorderable software configurations. Your system arrives fully assembled and tested in one box with your software preinstalled. When you order your system with the standard program, you also receive system-specific documentation including a bill of materials, an integration test report, a recommended maintenance plan, and frequently asked question documents. Finally, the standard program reduces the total cost of owning an NI system by providing three years of warranty coverage and calibration service. Use the online product advisors at ni.com/advisor to find a system assurance program to meet your needs.

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- **Online Community** - Visit community.ni.com to find, contribute, or collaborate on customer-contributed technical content with users like you.

Repair

While you may never need your hardware repaired, NI understands that unexpected events may lead to necessary repairs. NI offers repair services performed by highly trained technicians who quickly return your device with the guarantee that it will perform to factory specifications. For more information, visit ni.com/repair.

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Visit ni.com/training for more information.

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NI offers options for extending the standard product warranty to meet the life-cycle requirements of your project. In addition, because NI understands that your requirements may change, the extended warranty is flexible in length and easily renewed. For more information, visit ni.com/warranty.

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NI offers design-in consulting and product integration assistance if you need NI products for OEM applications. For information about special pricing and services for OEM customers, visit ni.com/oem.

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Detailed Specifications

This appendix lists the electrical, mechanical, and environmental specifications of the NI PXIe-8135 embedded controller.

Features

NI PXIe-8135

CPU	Intel Core i7 3610 QE
CPU Frequency	2.3 GHz (base), 3.3 GHz (single-core Turbo mode)
On-die L2 cache	256 KB x4 (256 KB per core)
Dual-Channel DDR3 RAM, PC3 12800	4 GB Standard 16 GB Maximum
Hard Drive	250 GB or larger Serial ATA *
Ethernet	10/100/1000 BaseTX, 2 ports
PXI Express 4 Link Configuration	x4, x4, x4, x4
PXI Express 2 Link Configuration	x8, x8
GPIO (IEEE 488 Controller)	Yes
Serial Ports (RS-232)	Yes (1)
Parallel Port	Yes (1)
Hi-Speed USB (2.0) Ports	Yes (4)
Hi-Speed USB (3.0) Ports	Yes (2)
ExpressCard/34 Slot	Yes
PS/2 Keyboard/Mouse Connector	No

PXI Express Trigger Bus Input/Output	Yes
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NI PXIe-8135

Installed Operating System	Windows 7 Professional, Windows XP Professional SP3 for Embedded Systems
* Extended-temperature 24/7 option provides 80 GB minimum hard drive. Controllers configured for LabVIEW RT provide a 80 GB (minimum) SATA hard drive.	

Electrical


Voltage (V)	Current (Amps)	
	Typical	Maximum
+3.3 V	3.75 A	5.4 A
+5 V	1.5 A	2.0 A
+12 V	3.5 A	5.0 A
-12 V	0.00 A	0.00 A
+5 V Aux	0.3 A	0.4 A

Physical

Board dimensions	Four-wide 3U PXI Express module
Slot requirements	One system slot plus three controller expansion slots
Compatibility	Fully compatible with PXI Express Specification 1.0
Weight	1.30 kg (2.87 lb) typical

Environmental

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2
Indoor use only.	

 **Caution** Clean the NI PXIe-8135 with a soft nonmetallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

NI PXIe-8135

Ambient temperature range	
Standard	5 to 50 °C1 (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 high temperature limit.)
Extended Temperature	
Option	0 to 55 °C1 (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC-60068-2-56.)

 **Caution** The operating temperature must not be exceeded, even when used in a chassis with a higher temperature range.

Storage Environment


NI PXIe-8135

Ambient temperature range	
Standard	-40 to 65 °C (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit.)
Extended Temperature	
Option	-40 to 71 °C (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 limits.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC-60068-2-56.)

Shock and Vibration

Operating Shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC-60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)
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Random Vibration	
Operating	5 to 500 Hz, 0.3 g _{rms} (with solid-state hard drive)
Nonoperating	5 to 500 Hz, 2.4 g _{rms} (Tested in accordance with IEC-60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)


 **Note** Specifications are subject to change without notice.

Safety

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1


 **Note** For UL and other safety certifications, refer to the product label or the Online Product Certification section.


 **Caution** Using the NI PXIe-8135 in a manner not described in this document may impair the protection the NI PXIe-8135 provides.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

 **Note** In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia and New Zealand (per CISPR 11) Class A equipment is intended for use only in heavy-industrial locations.

 **Note** Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generates radio frequency energy for the treatment of material or inspection/analysis purposes.

 **Note** For EMC declarations and certifications, and additional information, refer to the Online Product Certification section.

CE Compliance

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification


To obtain product certifications and the Declaration of Conformity (DoC) for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management


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 **EU Customers** At the end of the product life cycle, all products must be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit ni.com/environment/weee.

Battery Replacement and Disposal

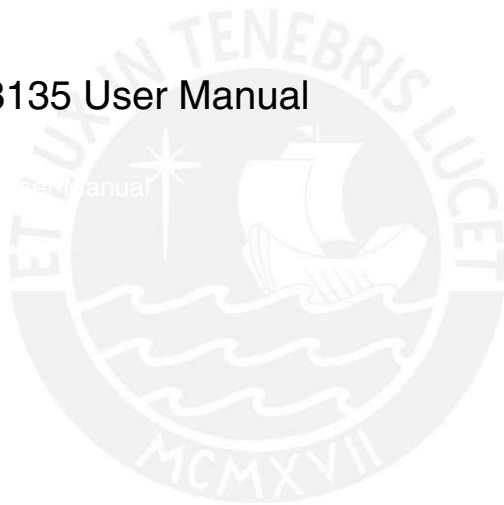
 This device contains a long-life coin cell battery. If you need to replace it, use the Return Material Authorization (RMA) process or contact an authorized National Instruments service representative. For more information about compliance with the EU Battery Directive 2006/66/EC about Batteries and Accumulators and Waste Batteries and Accumulators, visit ni.com/environment/batterydirective.

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PXI Express

NI PXIe-8135 User Manual



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A Return Material Authorization (RMA) number must be obtained from the factory and clearly marked on the outside of the package before any equipment will be accepted for warranty work. National Instruments will pay the shipping costs of returning to the owner parts which are covered by warranty.

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Compliance

Electromagnetic Compatibility Information

This hardware has been tested and found to comply with the applicable regulatory requirements and limits for electromagnetic compatibility (EMC) as indicated in the hardware's Declaration of Conformity (DoC)¹. These requirements and limits are designed to provide reasonable protection against harmful interference when the hardware is operated in the intended electromagnetic environment. In special cases, for example when either highly sensitive or noisy hardware is being used in close proximity, additional mitigation measures may have to be employed to minimize the potential for electromagnetic interference.

While this hardware is compliant with the applicable regulatory EMC requirements, there is no guarantee that interference will not occur in a particular installation. To minimize the potential for the hardware to cause interference to radio and television reception or to experience unacceptable performance degradation, install and use this hardware in strict accordance with the instructions in the hardware documentation and the DoC¹.

If this hardware does cause interference with licensed radio communications services or other nearby electronics, which can be determined by turning the hardware off and on, you are encouraged to try to correct the interference by one or more of the following measures:

- Reorient the antenna of the receiver (the device suffering interference).
- Relocate the transmitter (the device generating interference) with respect to the receiver.
- Plug the transmitter into a different outlet so that the transmitter and the receiver are on different branch circuits.

Some hardware may require the use of a metal, shielded enclosure (windowless version) to meet the EMC requirements for special EMC environments such as, for marine use or in heavy industrial areas. Refer to the hardware's user documentation and the DoC¹ for product installation requirements.

When the hardware is connected to a test object or to test leads, the system may become more sensitive to disturbances or may cause interference in the local electromagnetic environment.

Operation of this hardware in a residential area is likely to cause harmful interference. Users are required to correct the interference at their own expense or cease operation of the hardware.



Caution Changes or modifications not expressly approved by National Instruments could void the user's right to operate the hardware under the local regulatory rules. To ensure the specified EMC performance, operate this product only with shielded cables and accessories.

¹ The Declaration of Conformity (DoC) contains important EMC compliance information and instructions for the user or installer. To obtain the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

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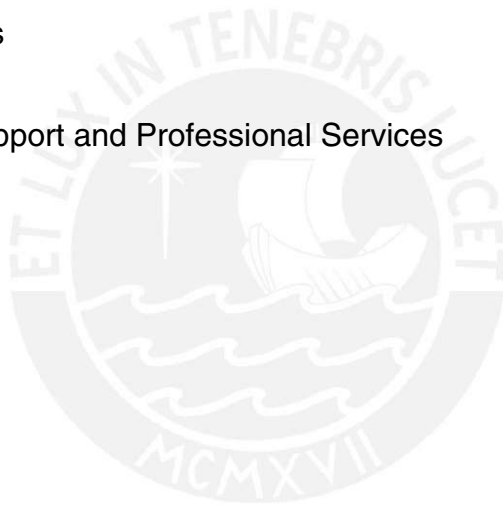
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About This Manual

This manual contains detailed instructions for installing and configuring the National Instruments PXIe-8135 embedded computer kit.

How to Use the Documentation Set

Begin by reading the *NI PXIe-8135 Installation Guide*, a brief quick-start guide that describes how to install and get started with your controller.

This manual, the *NI PXIe-8135 User Manual*, contains more details about changing the installation or configuration from the defaults and using the hardware.

Related Documentation

The following documents contain information you may find helpful as you read this manual:

- *PICMG EXP.0 R1.0 CompactPCI Express Specification*, PCI Industrial Computers Manufacturers Group
- IEEE Standard P1284.1-1997 (*C/MM*) *Standard for Information Technology for Transport Independent Printer/System Interface*
- *PCI Express Base Specification*, Revision 2.1, PCI Special Interest Group
- *PXI-5 PXI Express Hardware Specification*, Revision 1.0, PXI Systems Alliance
- *PXI-6 PXI Express Software Specification*, Revision 1.1, PXI Systems Alliance
- *Serialized IRQ Support for PCI Systems Specification*, Revision 6.0, Compaq Computer et al.
- *ExpressCard Standard*, Release 2.0, PCMCIA

Introduction

This chapter provides overview information for PXI Express and the NI PXIe-8135 embedded controller.

Benefits of PXI Express

The PXI (PCI eXtensions for Instrumentation) industry standard, an open specification governed by the PXI Systems Alliance (PXISA), has quickly gained adoption and grown in prevalence in test, measurement, and control systems since its release in 1998. One of the key elements driving the rapid adoption of PXI is its use of PCI in the communication backplane. As the commercial PC industry has improved the available bus bandwidth by evolving PCI to PCI Express, PXI is now able to meet even more application needs by integrating PCI Express into the PXI standard. By taking advantage of PCI Express technology in the backplane, PXI Express increases the available PXI bandwidth from up to 132 MB/s to up to 8 GB/s for a more than 60x improvement in bandwidth.

PXI Express maximizes both hardware and software compatibility with PXI modules. PXI Express hybrid slots deliver both PCI and PCI Express signaling to accept devices that use PXI communication and triggering or the newer PXI Express standard. Software compatibility is maintained because PCI Express uses the same OS and driver model as PCI, resulting in complete software compatibility among PCI-based systems, for example PXI, and PCI Express-based systems such as PXI Express.

PXI Express, like PXI, leverages from the CompactPCI specification to define a rugged, modular form factor that offers superior mechanical integrity and easy installation and removal of hardware components. PXI Express products offer higher and more carefully defined levels of environmental performance required by the shock, vibration, temperature, and humidity extremes of industrial environments. Mandatory environmental testing and active cooling is added to the CompactPCI mechanical specification to ease system integration and ensure multivendor interoperability.

The demanding timing and synchronization requirements of instrumentation systems are met by the integrated features of PXI Express. Not only are the trigger bus, 10 MHz system reference clock, and star trigger bus available in PXI retained by PXI Express, but new timing and synchronization features that include a 100 MHz differential system reference clock for the synchronization of multiple modules and three differential star trigger buses for the distribution of precise clock and trigger signals have been added. Differential timing and synchronization signals provide PXI Express systems with increased noise immunity and the ability to transmit clock signals at higher frequencies.

NI PXIe-8135

Description

The NI PXIe-8135 PXI Express/CompactPCI Express embedded computer is a high bandwidth PXI Express/CompactPCI Express-compatible system controller. The NI PXIe-8135 controller integrates standard I/O features in a single unit by using state-of-the-art packaging. Combining an NI PXIe-8135 embedded controller with a PXI Express-compatible chassis, such as the NI PXIe-1085, results in a fully PC-compatible computer in a compact, rugged package.

The standard I/O on each module includes two DisplayPort video ports, one RS-232 serial port, a parallel port, four high-speed USB 2.0 ports, two high-speed USB 3.0 ports, a PCI-based GPIB controller, two Gigabit Ethernet connectors, a reset button, and PXI Express triggers.

The NI PXIe-8135 has a quad-core Intel Core i7-3610QE processor, dual channel DDR3, 1600 MHz memory controller, all the standard I/O, and an integrated hard drive.



Note The removable hard drive variant has single channel DDR3.

The NI PXIe-8135 also has an optional ExpressCard/34 expansion slot variant, and an optional front panel-accessible, removable hard drive.

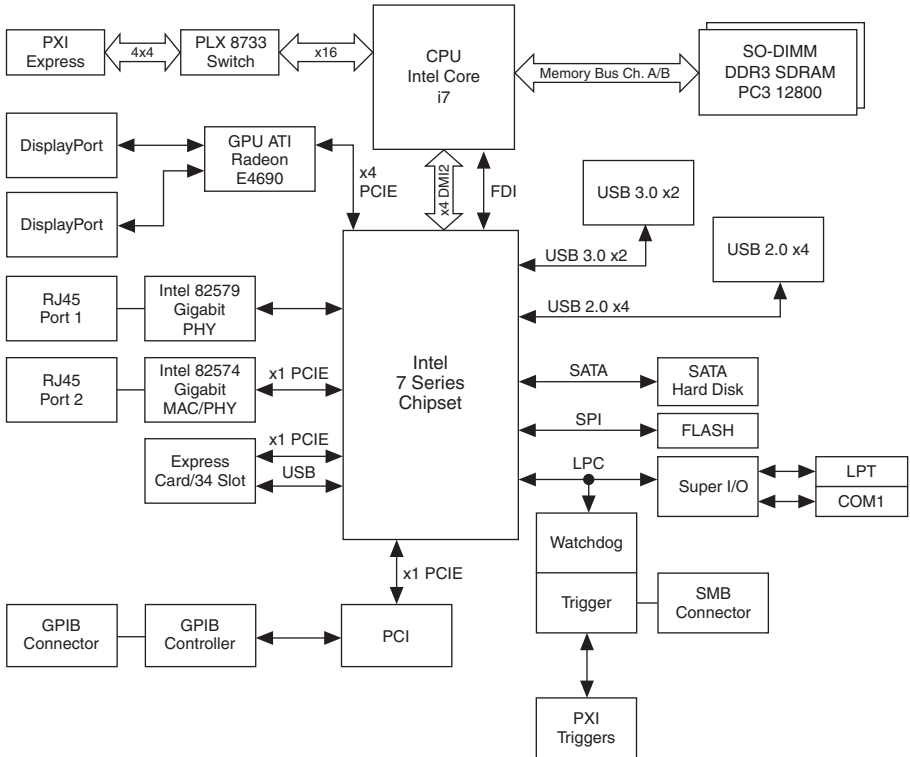
Functional Overview

This section contains functional descriptions of each major logic block on the NI PXIe-8135 embedded computer.

NI PXIe-8135 Functional Description

The NI PXIe-8135 is a modular PC in a PXI Express 3U-size form factor. Figure 1-1 is a functional block diagram of the NI PXIe-8135. Following the diagram is a description of each logic block shown.

Figure 1-1. NI PXIe-8135 Block Diagram



The NI PXIe-8135 consists of the following logic blocks on the CPU module and the I/O (daughter card) module. The CPU module has the following logic blocks:

- The *SO-DIMM* block consists of two 64-bit DDR3 SDRAM sockets that can hold up to 8 GB each, for a total of 16 GB.



Note The NI PXIe-8135 removable hard drive variant has a single SDRAM socket, for a total of up to 8 GB.

- The *SMB to PXI Express Trigger* provides a routable connection of the PXI Express triggers to/from the SMB on the front panel.
- The *ATI Radeon E4690 Embedded GPU* drives the graphics.

- The *Watchdog Timer* block consists of a watchdog timer that can reset the controller or generate a trigger.
- The *Intel 7 Series* chipset connects to the PCI, USB, Serial ATA, ExpressCard, PXI Express, and LPC buses.
- The *USB Connectors* connect the Intel 7 Series chipset to the Hi-Speed USB 2.0 interface and USB 3.0 interfaces.
- The *Serial ATA Hard Disk* is a 250 GB or larger notebook hard disk.¹ The Serial ATA interface enables transfer rates up to 600 MB/s. The hard disk also supports Native Command Queuing.



Note The NI PXIe-8135 removable hard drive Serial ATA interface enables transfer rates up to 300 MB/s.

- The *PXI Express Connector* connects the NI PXIe-8135 to the PXI Express/CompactPCI Express backplane.
- The *Super I/O* block represents the other peripherals supplied by the NI PXIe-8135. The NI PXIe-8135 has one serial port, and an ECP/EPP parallel port.
- Both the *82579* and *82574 Gigabit Enet ports* connect to either 10 Mbit, 100 Mbit, or 1,000 Mbit Ethernet interfaces. Both ports are housed in a dual stacked Ethernet connector.
- The *GPIB* block contains the GPIB interface.
- The *ExpressCard/34* slot accommodates an ExpressCard/34 module.

National Instruments Software

National Instruments has developed several software tools you can use with the NI PXIe-8135.

National Instruments' hardware and software work together to help you make the most of your PXI Express system. The LabVIEW, Measurement Studio, and LabWindows™/CVI™ application development environments combine with leading hardware drivers such as NI-DAQmx to provide exceptional control of NI hardware. Instrument drivers are available at ni.com/idnet to simplify communication with instruments over a variety of buses.

LabVIEW is a powerful and easy-to-use graphical programming environment you can use to acquire data from thousands of different instruments including USB, IEEE 488.2, VXI, serial, PLCs, and plug-in boards. LabVIEW helps you convert acquired data into meaningful results using powerful data analysis routines. Add-on tools provide additional specialized functionality. For more information visit ni.com/labview and ni.com/toolkits.

If you prefer to use Microsoft's Visual Basic, Visual C++, and Visual Studio .NET for the core of your application, Measurement Studio adds tools for Measurement and Automation to each language. For more information visit ni.com/mstudio.

¹ The extended-temperature, 24/7 option controller provides a 80 GB hard drive.

LabWindows/CVI is an interactive ANSI C programming environment designed for building virtual instrument applications. LabWindows/CVI delivers a drag-and-drop editor for building user interfaces, a complete ANSI C environment for building your test program logic, and a collection of automated code generation tools, as well as utilities for building automated test systems, monitoring applications, or laboratory experiments. For more information visit ni.com/lwcvl.

NI-DAQmx provides an extensive library of functions that you can call from your application development environment or interactive environment such as NI Signal Express. These functions provide an intuitive API for National Instruments' multifunction DAQ products. Features available include analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation, digital I/O, counter/timer operations, SCXI signal conditioning, RTSI or PXI Express synchronization, self-calibration, messaging, and acquiring data to extended memory. For more information visit ni.com/daq.

National Instruments' Modular Instruments use specialized drivers suited to each product's specialization. Express VIs provide customized, interactive programming of instruments in a single interface and soft front panels provide an interface for testing the functionality of each instrument with no programming required. NI Switches, DMMs, High-Speed DIO, High-Speed Digitizers, and Sources each have customized drivers for high-end modular instrumentation systems. RF applications leverage two drivers, NI-RFSG and NI-RFSA and Dynamic Signal Acquisition is available through NI-DAQmx. For more information visit ni.com/modularinstruments.

You can expand the timing and triggering functionality of your PXI Express system with PXI Express Timing and Synchronization products. These products provide precision clock sources, custom routing of triggers for multi-chassis synchronization, clock sharing, and more and are programmed with NI-Sync. For more information visit ni.com/pxi.

NI-VISA is the National Instruments implementation of the VISA specification. VISA is a uniform API for communicating and controlling USB, Serial, GPIB, PXI, PXI Express, VXI, and various other types of instruments. This API aids in the creation of portable applications and instrument drivers. For information on writing your own PXI Express instrument driver with NI-VISA, refer to the *NI-VISA Getting Started Manual* and the `readme.txt` file in the NI-VISA directory. For more information visit ni.com/visa.

With LabVIEW for Linux and support for over two hundred devices on Linux with the NI-DAQmx driver, you can now create Virtual Instruments based on the Linux OS. Instrument control in Linux has been improved by the NI-VISA driver for Linux and NI Modular Instruments are partially supported. For more information visit ni.com/linux.

Cleaning

Use a dry, low-velocity stream of air to clean the NI PXIe-8135 controller. If needed, use a soft-bristle brush for cleaning around components.

Installation and Configuration

This chapter contains information about installing and configuring your NI PXIe-8135 controller.

Installing the NI PXIe-8135

This section contains general installation instructions for the NI PXIe-8135. Consult your PXI Express chassis user manual for specific instructions and warnings.

1. Plug in your chassis before installing the NI PXIe-8135. The power cord grounds the chassis and protects it from electrical damage while you install the module.

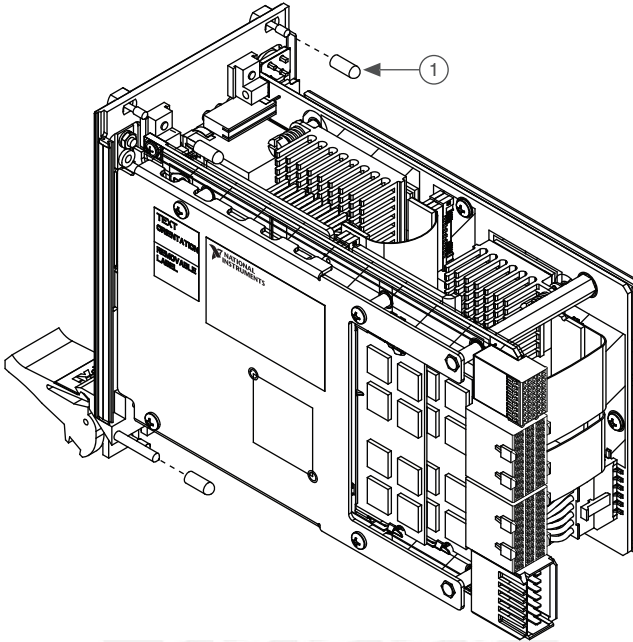


Caution To protect both yourself and the chassis from electrical hazards, leave the chassis powered off until you finish installing the NI PXIe-8135 module.

2. Remove any filler panels blocking access to the system controller slot (Slot 1) in the chassis.
3. Touch the metal part of the case to discharge any static electricity that might be on your clothes or body.

4. Remove the protective plastic covers from the four bracket-retaining screws as shown in Figure 2-1.

Figure 2-1. Removing Protective Screw Caps



1 Protective Screw Cap (4x)

5. Make sure the injector/ejector handle is in its downward position. Align the NI PXIe-8135 with the card guides on the top and bottom of the system controller slot.



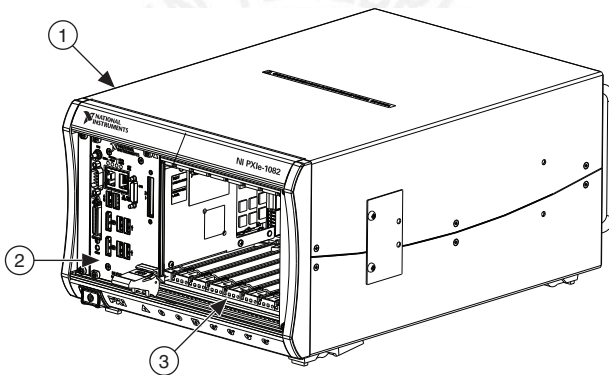
Caution Do *not* raise the injector/ejector handle as you insert the NI PXIe-8135. The module will not insert properly unless the handle is in its downward position so that it does not interfere with the injector rail on the chassis.

6. Hold the handle as you slowly slide the module into the chassis until the handle catches on the injector/ejector rail.
7. Raise the injector/ejector handle until the module firmly seats into the backplane receptacle connectors. The front panel of the NI PXIe-8135 should be even with the front panel of the chassis.
8. Tighten the four bracket-retaining screws on the top and bottom of the front panel to secure the NI PXIe-8135 to the chassis.
9. Check the installation.

10. Connect the keyboard and mouse to the appropriate connectors. If you are using a PS/2 keyboard and a PS/2 mouse, a Y-splitter adapter is available to connect both to a single USB connector. Refer to Figure 4-1, *Y-Splitter Cable*.
11. Connect the DisplayPort monitor video cable to a DisplayPort connector, or use the DisplayPort-to-VGA adapter included with your controller to connect a VGA monitor to the DisplayPort connector.
12. Connect devices to ports as required by your system configuration.
13. Power on the chassis.
14. Verify that the controller boots. If the controller does not boot, refer to the *What if the NI PXIe-8135 does not boot?* section of Chapter 5, *Troubleshooting*.

Figure 2-2 shows an NI PXIe-8135 installed in the system controller slot of a National Instruments NI PXIe-1082 chassis.

Figure 2-2. NI PXIe-8135 Controller Installed in a PXI Express Chassis



1 NI PXIe-1082 Chassis
2 NI PXIe-8135 Controller

3 Injector/Ejector Rail

How to Remove the Controller from the PXI Express Chassis

The NI PXIe-8135 controller is designed for easy handling. To remove the unit from the PXI Express chassis, complete the following steps.

1. Power off the chassis.
2. Unscrew the 4 bracket-retaining screws in the front panel.
3. Press the injector/ejector handle down.
4. Slide the unit out of the chassis.



Note If the PXI Express chassis Inhibit Mode Selector Switch is not in the Default position, any attempt to shut down the NI PXIe-8135 through the push button reset or using Windows will result in the controller Power OK LED blinking. The user will be required to use the Remote Inhibit pin on the Remote Inhibit and Voltage Monitoring Connector to turn off the chassis. Refer to the PXI Express chassis user manual for details on the functionality of the Remote Inhibit and Voltage Monitoring controls.

BIOS Setup Utility

You can change the NI PXIe-8135 configuration settings in the BIOS setup program. The BIOS is the low-level interface between the hardware and operating system software that configures and tests your hardware when you boot the system. The BIOS setup program includes menus for configuring settings and enabling NI PXIe-8135 controller features.

Most users do not need to use the BIOS setup program, as the NI PXIe-8135 controller ships with default settings that work well for most configurations.



Caution Changing BIOS settings may lead to incorrect controller behavior and possibly an unbootable controller. If this happens, follow the instructions for restoring default settings in the *System CMOS* section. In general, do *not* change a setting unless you are absolutely certain what it does.

Accessing BIOS Setup Utility

Complete the following steps to start the BIOS setup program.

1. Power on or reboot your NI PXIe-8135 controller.
2. When the message **Press to enter setup** appears, press the <Delete> key. The setup program loads after a short delay.

The **Main** menu is displayed when you first enter the BIOS setup program.

Use the following keys to navigate through the BIOS setup program:

- **Left Arrow, Right Arrow**—Use these keys to move between the different setup menus. If you are in a submenu, these keys have no effect, and you must press <Esc> to leave the submenu first. (To use the arrows on the numeric keypad, you must turn off Num Lock.)
- **Up Arrow, Down Arrow**—Use these keys to move between the options within a setup menu. (To use the arrows on the numeric keypad, you must turn off Num Lock.)
- **<Enter>**—Use this key either to enter a submenu or display all available settings for a highlighted configuration option.
- **<Esc>**—Use this key to return to the parent menu of a submenu. At the top-level menus, this key serves as a shortcut to the **Exit** menu.
- **<+> and <->**—Use these keys to cycle between all available settings for a selected configuration option.

- **<Tab>**—Use this key to select time and date fields.
- **<F9>**—Use this key to load the optimal default values for BIOS configuration settings. The optimal default values are the same as the shipping configuration default values.

Main Setup Menu

The most commonly accessed and modified BIOS settings are in the **Main** setup menu. The **Main** setup menu reports the following configuration information:

- **BIOS Version and Build Date**—These values indicate the version of the NI PXIe-8135 controller BIOS and the date on which the BIOS was built.
- **Embedded Firmware Version**—This value helps identify the built-in hardware capabilities.
- **Processor Type, Base Processor Frequency, and Active Processor Cores**—These values indicate the type of processor used in the NI PXIe-8135 controller, the speed of the processor, and the number of active processor cores.
- **Total Memory**—This value indicates the size of system RAM detected by the BIOS.
- **PXIe Chassis Information**—These values indicate the overall chassis link configuration, the link width of each link, and the link speed of each link.

The **Main** setup menu also includes the following settings:

- **System Time**—This setting controls the time of day, which is stored in a battery-backed real-time clock. Most operating systems also include a way to change this setting. Use <+> and <-> in conjunction with <Enter> and <Tab> to change these values.
- **System Date**—This setting controls the date, which is stored in a battery-backed real-time clock. Most operating systems also include a way to change this setting. Use <+> and <-> in conjunction with <Enter> and <Tab> to change these values.

Advanced Setup Menu

This menu contains BIOS settings that normally do not require modification. If you have specific problems such as unbootable disks or resource conflicts, you may need to examine these settings.



Caution Changing settings in this menu may result in an unstable or unbootable controller. If this happens, follow the procedures outlined in the [System CMOS](#) section to restore BIOS settings to their factory defaults.

The **Advanced** setup menu includes the following settings and submenus:

- **SATA Configuration**—Use this setting to access the **SATA Configuration** submenu. Refer to the [SATA Configuration Submenu](#) section for more information.
- **CPU Configuration**—Use this setting to access the **CPU Configuration** submenu. Refer to the [CPU Configuration Submenu](#) section for more information.

- **Video Configuration**—Use this setting to access the **Video Configuration** submenu. Refer to the *Video Configuration Submenu* section for more information.
- **Power/Wake Configuration**—Use this setting to access the **Power/Wake Configuration** submenu. Refer to the *Power/Wake Configuration Submenu* section for more information.
- **ExpressCard Configuration**—Use this setting to access the **ExpressCard Configuration** submenu. Refer to the *ExpressCard Configuration Submenu* section for more information.
- **PCI Configuration**—Use this setting to access the **PCI Configuration** submenu. Refer to the *PCI Configuration Submenu* section for more information.
- **Memory Configuration**—Use this setting to access the **Memory Configuration** submenu. Refer to the *Memory Configuration Submenu* section for more information.
- **AMT Configuration**—Use this setting to access the **AMT Configuration** submenu. Refer to the *AMT Configuration Submenu* section for more information.
- **USB Configuration**—Use this setting to access the **USB Configuration** submenu. Refer to the *USB Configuration Submenu* section for more information.
- **Serial/Parallel Port Configuration**—Use this setting to access the **Serial/Parallel Port Configuration** submenu. Refer to the *Serial/Parallel Port Configuration Submenu* section for more information.

SATA Configuration Submenu

Use this submenu to apply alternate settings to the hard disk drive (HDD) interfaces. Normally, you do not need to modify these settings, as the factory default settings provide the most compatible and optimal configuration possible.

- **SATA Controller**—This setting specifies whether or not the onboard SATA controller is enabled or disabled. The default value is **Enabled**.
 - **SATA Mode Selection**—This setting determines whether AHCI mode is enabled or disabled for the SATA port. Some operating systems, such as Windows 2000, do not support AHCI mode. You can use this setting to disable AHCI mode and enable IDE mode so that non-compatible OSes function correctly. The default value is **AHCI**.
- **Internal Drive (SATA)**—This item displays the onboard SATA drive detected in the system.
- **Removable Hard Drive**—This item displays the removable hard drive, if installed.

CPU Configuration Submenu

Use this submenu to apply alternate settings to the CPU. Normally, you do not need to modify these settings, as the factory default settings provide the most compatible and optimal configuration possible.

- **Hyper Threading**—This setting enables or disables Intel Hyper-Threading technology. The default value is **Enabled**. Enabling Hyper-Threading increases performance for some applications by adding virtual CPU cores. Hyper-Threading can increase application jitter, so care should be taken when enabling this setting on a Real Time system. When the BIOS

is configured to boot LabVIEW Real-Time, Hyper-Threading will be automatically disabled. In order to manually enable Hyper-Threading performance when in LabVIEW Real-Time mode, see the [LabVIEW RT Configuration Overrides Submenu](#).

- **Enabled CPU Cores**—This setting selects the number of active CPU cores for the processor. Valid values are **All**, **3**, **2**, or **1**. The default value is **All**.
- **Turbo Boost**—This setting enables or disables Intel Turbo Boost technology. The default value is **Enabled**. Enabling Turbo Boost allows CPU cores to run at higher than their base frequency for short durations, while other cores are idle. Enabling Turbo Boost can also increase application jitter, so care should be taken when enabling this setting on a Real Time system. To achieve maximum possible Turbo Boost frequencies, also enable the C-States setting. When the BIOS is configured to boot LabVIEW Real-time, Turbo Boost will be automatically disabled. In order to manually enable Turbo Boost performance when in LabVIEW Real-Time mode, see the [LabVIEW RT Configuration Overrides Submenu](#).
- **C-States**—This setting enables or disables CPU power management. The default value is **Enabled**. Enabling C-States allows the processor to put idle CPU cores to sleep, allowing active cores to run at higher than base frequencies when Turbo Boost is enabled. Enabling C-States can increase application jitter, so care should be taken when enabling this setting on a Real Time system. When the BIOS is configured to boot LabVIEW Real-time, C-States will be automatically disabled. In order to manually enable C-States when in LabVIEW Real-Time mode, see the [LabVIEW RT Configuration Overrides Submenu](#).
- **Hardware Prefetcher**—This setting enables or disables CPU cache hardware prefetching. The default value is **Disabled** when booting LabVIEW Real-Time, enabled when booting other OSs. Enabling hardware prefetching can increase system performance for some applications, but can cause control algorithms to behave less deterministically.
- **Adjacent Cache Line Prefetch**—This setting enables or disables prefetching of adjacent cache lines from memory to the CPU cache. The default value is **Disabled** when booting LabVIEW Real-Time, enabled when booting other OSs. Enabling adjacent cache line prefetching can increase system performance for some applications, but can cause control algorithms to behave less deterministically.

Video Configuration Submenu

Use this submenu to apply alternate settings to the video configuration. Normally, you do not need to modify these settings, as the factory default settings provide the most compatible and optimal configuration possible.

- **Primary Display**—This setting specifies which video adapter the BIOS should use as the primary adapter if more than one is present. To use an external video adapter as the primary graphics adapter, choose **Add-in Board Video**. The default value is **Onboard ATI Video**.

Power/Wake Configuration Submenu

Use this submenu to apply alternate configurations to the power and wake features of the chipset and controller. Normally, you do not need to modify these settings, as the factory default settings provide the most compatible and optimal configuration possible.

- **Restore After Power Loss**—This setting specifies the power state that the controller should return to after AC power is lost. Valid values are **Stay Off** and **Turn On**. The default is **Stay Off**. When set to **Stay Off**, the controller will return to the soft off power state after AC power is restored. When set to **Turn On**, the controller will power on when AC power is restored.
- **Power Button Off Behavior**—This setting specifies how the PXI Express power button should behave. Valid options are **Normal** and **Disable**. The default value is **Normal**. When set to **Normal**, the power button will be controlled by the OS. When set to **Disable**, pressing the power button has no effect. The **Disable** option should only be used in conjunction with the PXI Express chassis' inhibit mode switch.
- **ExpressCard WAKE#**—This setting enables or disables an ExpressCard device's ability to wake a powered-off system. The default value is **Disabled**.
- **PXIe Backplane WAKE#**—This setting enables or disables a PXI Express peripheral module's ability to wake a powered-off system. The default value is **Disabled**.
- **SMBus ALERT#**—This setting enables or disables a System Management device's ability to wake a powered off system by asserting the ALERT# signal. The default value is **Disabled**.

ExpressCard Configuration Submenu

Use this submenu to apply alternate settings to the ExpressCard configuration. These settings determine how much memory space, I/O space, and PCI bus numbers will be pre-allocated for the ExpressCard port, allowing non-PCI Express-aware operating systems to support hot-plugging ExpressCard devices. Normally, you do not need to modify these settings, as the factory default settings provide the most compatible and optimal configuration possible.

- **ExpressCard Resources**—This setting enables or disables the setting of the **Reserved Buses**, **Reserved Memory**, and **Reserved I/O** settings. The default value for this setting is **Enabled**. If this setting is disabled, the bus, memory, and I/O options disappear from this submenu. Disabling this setting effectively sets **Reserved Buses to 0**, **Reserved Memory to 0M**, and **Reserved I/O to 0K**.
- **Reserved Buses**—This setting determines the number of PCI buses that will be reserved by the BIOS for ExpressCard PCI-PCI bridges that may be hot-plugged in the ExpressCard slot. The default value for this setting is **8** PCI buses.
- **Reserved Memory**—This setting determines the amount of memory space, in bytes, that will be reserved by the BIOS for PCI-PCI bridges that may be hot-plugged in the ExpressCard slot. The default value for this setting is **64M** bytes of memory.
- **Reserved I/O**—This setting determines the amount of I/O space, in bytes, that will be reserved by the BIOS for PCI-PCI bridges that may be hot-plugged in the ExpressCard slot. The default value for this setting is **4K** bytes of I/O space.

PCI Configuration Submenu

Use this submenu to apply alternate settings to PCI devices. Normally, you do not need to modify these settings, as the factory default settings provide the most compatible and optimal configuration possible.

- **64-bit Memory-Mapped IO**—This setting enables or disables support for memory-mapped IO above the 4 GB boundary. It can be useful when using a 64-bit OS and a large number of PCI devices. The default value is **Disabled**.
- **PCIe Max Payload Size**—This setting determines the maximum payload size of PCIe devices. Valid options are **Auto** and **128 Bytes**. The default value is **Auto**, which allows the BIOS to choose an optimal value based on which devices are present.
- **Option ROM Monitor**—This setting enables or disables a limit on option ROM execution time. The default value is **Disabled**.
- **Option ROM Monitor Timeout**—This setting specifies the number of seconds to wait for an option ROM to execute. If an option ROM does not execute in this time, the system will reboot. This setting is only visible if **Option ROM Monitor** is set to **Enabled**. The default value is **1** second.

Memory Configuration Submenu

Use this submenu to apply alternate settings to memory. Normally, you do not need to modify these settings, as the factory default settings provide the most compatible and optimal configuration possible.

- **Memory Performance Mode**—This setting enables or disables performance mode for memory. The default value is **Enabled**.

AMT Configuration Submenu

Use this submenu to apply alternate settings for Intel Advanced Management Technology (AMT) and its Management Engine. Normally, you do not need to modify these settings, as the factory default settings provide the most compatible and optimal configuration possible.

- **Management Engine Setup Prompt**—This setting enables or disables the Intel AMT Management Engine setup prompt on the BIOS POST screen. When this is set to **Enabled**, you will be allowed to press <Ctrl-P> at the BIOS POST screen to configure the Management Engine. The default value is **Disabled**.
- **Unconfigure Management Engine**—This setting allows the Management Engine to be reset to factory settings on the next boot. This option will revert to its default value after the Management Engine is reset. The default value is **Disabled**.
- **USB-Based Configuration**—This setting enables or disables automatic configuration of the Management Engine based on Management Engine configuration files which may be present on USB devices plugged into the controller. The default value is **Disabled**.

USB Configuration Submenu

Use this submenu to apply alternate configurations to the USB ports. Normally, you do not need to modify these settings, as the factory default settings provide the most compatible and optimal configuration possible.

- **USB Devices**—This item lists the total number of devices detected in the system, categorized by device type.
- **Legacy USB Support**—This setting specifies whether or not legacy USB support is enabled. Legacy USB support refers to the ability to use a USB keyboard and mouse during system boot or in a legacy operating system such as DOS. The default value is **Enabled**. This option is automatically disabled when booting LabVIEW Real-Time in order to reduce application jitter.
- **Overcurrent Reporting**—This setting allows the BIOS to notify the operating system of any USB ports which sources too much current. The default value for this setting is **Disabled**.
- **Transfer Timeout**—This setting specifies the timeout value for Control, Bulk, and Interrupt USB transfers. The default value for this setting is **20** seconds.
- **Device Reset Timeout**—This setting specifies the number of seconds the Power-On Self Test will wait for a USB mass storage device to start. The default is **20** seconds.
- **Device Power-Up Delay**—This setting specifies the maximum time a device will take before it properly reports itself to the host controller. When set to **Auto**, a root port is granted 100 ms, and for a hub port, the delay value is taken from the hub descriptor. The default value for this setting is **Auto**.
- **Device Power-Up Delay in Seconds**—This setting specifies the number of seconds the Power-On Self Test will wait for a USB device or hub to power on. This setting is only visible if **Device Power-Up Delay** is set to **Manual**. The default is **5** seconds.

In addition, the following option is available for each detected device if a USB mass storage device is present:

- **Emulation Type**—This setting specifies how the BIOS will present the USB mass storage device to the system. This option can be used to present a USB mass storage device as a floppy, Zip, hard disk, or CD-ROM drive. The default is **Auto**, which allows the BIOS to treat small USB flash disk drives as floppy drives and larger USB flash disk drives as hard disk drives.

Serial/Parallel Port Configuration Submenu

Use this submenu to apply alternate configurations to the serial and parallel ports. Normally, you do not need to modify these settings, as the factory default settings provide the most compatible and optimal configuration possible.

- **Serial Port Configuration**—Use this setting to access the **Serial Port Configuration** submenu. Refer to the [Serial Port Configuration Submenu](#) section for more information.
- **Parallel Port Configuration**—Use this setting to access the **Parallel Port Configuration** submenu. Refer to the [Parallel Port Configuration Submenu](#) section for more information.

Serial Port Configuration Submenu

- **Serial Port**—This setting enables or disables the onboard serial port. The default value is **Enabled**.
- **Device Settings**—This item displays the current base address and interrupt request level (IRQ) information for the onboard serial port.
- **Change Settings**—This setting changes the base address and interrupt request level (IRQ) information for the onboard serial port. The default value is **Auto**.

Parallel Port Configuration Submenu

- **Parallel Port**—This setting enables or disables the onboard parallel port. The default value is **Enabled**.
- **Device Settings**—This item displays the current base address and interrupt request level (IRQ) information for the onboard parallel port.
- **Device Mode**—This setting enables alternate modes of operation for the parallel port. Usually the default setting works for all applications. The default is **STD Printer Mode**.
- **Change Settings**—This setting changes the base address and interrupt request level (IRQ) information for the onboard parallel port. The default value is **Auto**. Note that the options available vary based upon the **Device Mode** selected for the parallel port.

LabVIEW RT Setup Menu

Use this menu to configure boot options for LabVIEW RT if it is installed on the controller. If you are not using LabVIEW RT, you should leave these settings at default.



Note The settings below override the behavior of the switches shown in Figure 2-4. Refer to the [LabVIEW RT Configuration Switches](#) section for more information. To use the settings from the switches, select **Use Switch Setting** for each option.

- **Boot Configuration**—This setting selects whether the controller should boot LabVIEW RT, LabVIEW RT Safe Mode, or an installed OS such as Windows 7. The default is **Use Switch Setting**.
- **Reset IP Address**—If the controller is deployed to a different subnet from which it was originally configured, or if the current IP address is invalid, use this switch to reset the IP address and other TCP/IP settings to their factory defaults during LabVIEW RT startup. The default is **Use Switch Setting**.



Note By default, the target will automatically attempt to connect to the network using DHCP. If the target is unable to initiate a DHCP connection, the target connects to the network with a link-local IP address of 169.254.x.x.

- **Disable Startup VI**—If the controller becomes inaccessible because of a startup VI, this switch can prevent VIs from automatically running at startup. The default is **Use Switch Setting**.
- **LabVIEW RT Configuration Overrides**—Use this setting to access the **LabVIEW RT Configuration Overrides** submenu. Refer to the *LabVIEW RT Configuration Overrides Submenu* section for more information.

Current Hardware Switch Settings

This submenu displays the current values of the LabVIEW RT configuration switches, indicating Boot Configuration, Reset IP Address, and Disable Startup VI switch status. For more information on these settings and the switches that control them, refer to the *LabVIEW RT Configuration Switches* section of this chapter.

LabVIEW RT Configuration Overrides Submenu

In order to minimize jitter when booting into LabVIEW Real-Time mode, the following features are automatically disabled. These features can be manually enabled. Refer to the *CPU Configuration Submenu* for specific details on what each feature enables.

- **CPU Hyper Threading**—The default is **Use RT Default**.
- **CPU C-States**—The default is **Use RT Default**.

Boot Setup Menu

Use this menu to configure settings related to the boot process and boot device priority.

- **Boot Settings Configuration**—Use this setting to access the **Boot Settings Configuration** submenu. Refer to the *Boot Settings Configuration Submenu* section for more information.
- **PXI Drive Boot**—This setting specifies whether or not boot support is enabled for legacy mass storage devices, such as SCSI drives. When enabled, legacy mass storage controllers with boot support will be displayed in the **Boot Option Priorities** menu. The default value is **Enabled**.
- **PXE Network Boot**—This setting specifies whether or not the PXE network boot agent is enabled. When enabled, the Intel Boot Agent will be displayed in the **Boot Option Priorities** menu, allowing you to boot from a PXE server on the local subnet. Note that the Intel Boot Agent device names are preceded by **IBA GE Slot 00c9 v1310** in the **Boot Option Priorities** menu. The system must be restarted for this setting to take effect. The default value is **Disabled**.
- **Boot Option Priorities**—These settings specify the order in which the BIOS checks for bootable devices, including the local hard disk drive, removable devices such as USB flash disk drives or USB CD-ROM drives, or the PXE network boot agent. The BIOS will first attempt to boot from the device associated with **1st Boot Device**, followed by **2nd Boot Device**, and **3rd Boot Device**. If multiple boot devices are not present, the BIOS setup utility will not display all of these configuration options. To select a boot device, press <Enter> on the desired configuration option and select a boot device from the resulting menu. You can also disable certain boot devices by selecting **Disabled**.



Note Only one device of a given type will be shown in this list. If more than one device of the same type exists, use the *Device BBS Priorities* submenus to re-order the priority of devices of the same type.

The following submenus will be displayed if one or more bootable devices of the corresponding type is present:

- **Hard Drive BBS Priorities**—Use this setting to access the **Hard Drive BBS Priorities** submenu to re-order or disable bootable hard drive devices. Refer to the *Hard Drive BBS Priorities Submenu* section for more information.
- **CD/DVD ROM Drive BBS Priorities**—Use this setting to access the **CD/DVD ROM Drive BBS Priorities** submenu to re-order or disable bootable CD/DVD ROM drive devices. Refer to the *CD/DVD ROM Drive BBS Priorities Submenu* section for more information.
- **Floppy Drive BBS Priorities**—Use this setting to access the **Floppy Drive BBS Priorities** submenu to re-order or disable bootable floppy drive devices. Refer to the *Floppy Drive BBS Priorities Submenu* section for more information.
- **Network Device BBS Priorities**—Use this setting to access the **Network Device BBS Priorities** submenu to re-order or disable bootable network devices. Refer to the *Network Device BBS Priorities Submenu* section for more information.

Boot Settings Configuration Submenu

Use this submenu to apply alternate configurations to boot settings. Normally, you do not need to modify these settings, as the factory default settings provide the most compatible and optimal configuration.

- **Setup Prompt Timeout**—This setting specifies the number of seconds the system will wait for a BIOS Setup menu keypress (the <Delete> key). The default value is **2**.
- **Bootup NumLock State**—This setting specifies the power-on state of the keyboard NumLock setting. The default value is **On**.

Hard Drive BBS Priorities Submenu

- **Boot Option #1, Boot Option #2, Boot Option #3**—These settings specify the boot priority of hard drive devices. The highest priority device is displayed on the main **Boot Option Priorities** list. Optionally, each device can also be **Disabled** if the device should never be used as a boot device.

CD/DVD ROM Drive BBS Priorities Submenu

- **Boot Option #1, Boot Option #2, Boot Option #3**—These settings specify the boot priority of CD/DVD ROM drive devices. The highest priority device is displayed on the main **Boot Option Priorities** list. Optionally, each device can also be **Disabled** if the device should never be used as a boot device.

Floppy Drive BBS Priorities Submenu

- **Boot Option #1, Boot Option #2, Boot Option #3**—These settings specify the boot priority of floppy drive devices. The highest priority device is displayed on the main **Boot Option Priorities** list. Optionally, each device can also be **Disabled** if the device should never be used as a boot device.

Network Device BBS Priorities Submenu

- **Boot Option #1, Boot Option #2, Boot Option #3**—These settings specify the boot priority of network devices. The highest priority device is displayed on the main **Boot Option Priorities** list. Optionally, each device can also be **Disabled** if the device should never be used as a boot device.

Security Menu

Use this menu to enable BIOS security options.

- **Administrator Password**—This setting specifies a password that must be entered to access the BIOS Setup Utility. If only the Administrator's password is set, then this only limits access to the BIOS setup program and is only asked for when entering the BIOS setup program. By default, no password is specified.
- **User Password**—This setting specifies a password that must be entered to access the BIOS Setup Utility or to boot the system. If only the User's password is set, then this is a power on password and must be entered to boot or enter the BIOS setup program. In the BIOS setup program, the User will have Administrator rights. By default, no password is specified.

Save & Exit Menu

The **Save & Exit** setup menu includes all available options for exiting, saving, and loading the BIOS default configuration. As an alternative to this screen, press <F9> to load optimal BIOS default settings and <F10> to save changes and exit setup.

The **Exit** setup menu includes the following settings:

- **Save Changes and Reset**—Any changes made to BIOS settings are stored in NVRAM. The setup program then exits and reboots the controller. The <F10> key can also be used to select this option.
- **Discard Changes and Reset**—Any changes made to BIOS settings during this session of the BIOS setup program are discarded. The setup program then exits and reboots the controller. The <Esc> key can also be used to select this option.
- **Save Changes**—Changes made to BIOS settings during this session are committed to NVRAM. The setup program remains active, allowing further changes.
- **Discard Changes**—Any changes made to BIOS settings during this session of the BIOS setup program are discarded. The BIOS setup continues to be active.
- **Restore Factory Defaults**—This option restores all BIOS settings to the factory default. This option is useful if the controller exhibits unpredictable behavior due to an incorrect or

inappropriate BIOS setting. Notice that any nondefault settings such as boot order, passwords, and so on, are also restored to their factory defaults. The <F9> key can also be used to select this option.

- **Save As User Defaults**—This option saves a copy of the current BIOS settings as the User Defaults. This option is useful for preserving custom BIOS setup configurations.
- **Restore User Defaults**—This option restores all BIOS settings to the user defaults. This option is useful for restoring previously preserved custom BIOS setup configurations.
- **Boot Override**—This option lists all possible bootable devices and allows the user to override the **Boot Option Priorities** list for the current boot. If no changes have been made to the BIOS setup options, the system will continue booting to the selected device without first rebooting. If BIOS setup options have been changed and saved, a reboot will be required and the boot override selection will not be valid.

BIOS Diagnostic Utilities

You can test the hard drive and memory of your controller with the included BIOS diagnostic utilities.

Accessing BIOS Diagnostic Utilities

Complete the following steps to start the BIOS Diagnostic Utility.

1. Power on or reboot your controller.
2. When the message **<F2> to run diagnostics** appears, press the <F2> key. The first diagnostic utility loads after a short delay.

Hard Drive Diagnostic Utility

The hard drive is tested first upon entry into the BIOS Diagnostic Utilities. A quick test is performed initially, and a more comprehensive test is performed second. The user may abort and skip any test by pressing the <Esc> key at any time during that test. After both tests have finished or been skipped, the user is presented with the testing results. If both tests have succeeded or been skipped, **Press any key to continue** is displayed. In order to continue with testing, user interaction is required to press a key on the keyboard.



Note If either hard drive test fails, the controller is not permitted to boot, and the user is instructed to turn off the controller and replace the hard drive.

Memory Diagnostic Utility

The memory diagnostic utility is started immediately after the user presses a key to exit the hard drive diagnostic utility. The user may abort and skip the memory test by pressing the <Esc> key at any time during this test. After the memory utility has finished or been skipped, the user is presented with the testing result. If the memory test was successful or skipped, **Press any key to continue** is displayed. In order to continue to boot the controller, user interaction is required to press a key on the keyboard.



Note If the memory test fails, the controller is not permitted to boot, and the user is instructed to turn off the controller and replace the memory.

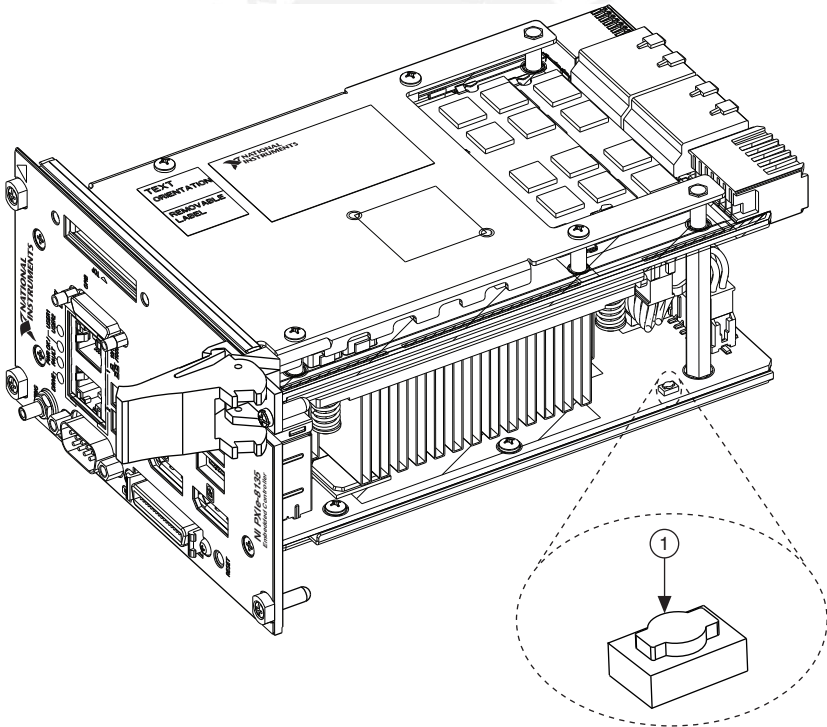
System CMOS

The NI PXIe-8135 contains memory backed up by a battery to store BIOS configuration information.

Complete the following steps to clear the CMOS contents:

1. Power off the chassis.
2. Remove the controller from the chassis.
3. Press the push-button switch, as shown in Figure 2-3.
4. Wait ten seconds.
5. Reinstall the controller in the chassis.

Figure 2-3. Clearing the CMOS Contents



1 Push-Button Switch SW2

LabVIEW RT Installation

This section explains software installation and switch configuration for LabVIEW RT on your PXI Express controller.

LabVIEW RT Software Installation

The following section describes the necessary steps to get your PXI Express embedded controller setup to run LabVIEW Real-Time. In this section you will configure the boot mode of the controller, verify or change IP settings, and install LabVIEW Real-Time software.

Complete the following steps to install the LabVIEW RT software.

1. Boot the NI PXI Express embedded controller into the real-time operating system. Refer to the [LabVIEW RT Configuration Switches](#) section or the [LabVIEW RT Setup Menu](#) section in this manual to configure the controller for booting into LabVIEW RT.

The PXI Express controller will automatically boot into LabVIEW RT Safe Mode when no software is installed. LabVIEW RT Safe Mode loads with the basic real-time operating system and will automatically attempt to connect to the network using DHCP. If DHCP is not available, it will then connect to the network with a link-local IP address.



Tip You can connect a monitor to the desktop PC to display startup messages such as the IP address and MAC address.

2. Open Measurement & Automation Explorer (MAX) on another computer in the same subnet and expand the **Remote Systems** branch. MAX lists the PXI Express controller as the model name of the controller followed by the MAC address (for example, **NI-PXIe-8135 00802f108562**).



Note The other computer must have LabVIEW, LabVIEW RT, and any desired drivers installed.



Tip Record the PXI Express controller MAC address, located on the side of the controller, for use in identifying the controller. The label also can be removed and placed on the front of the controller for easier access.

3. Click on the appropriate PXI Express controller entry to access the **Network Settings** tab in the right pane view.
4. (Optional) Enter a name for the RT target in the **Name** text box.
5. (Optional) Set the network configuration options of the RT target in the **IP Settings** section and click the **Apply** button.

For information about configuring network settings, refer to the *Configuring Network Settings* book, accessible by browsing to **MAX Remote Systems Help»LabVIEW Real-Time Target Configuration»Configuring Network Settings** from the **Contents** tab of *MAX Help*.



Note When any IP or identification settings are changed, you will be prompted to reboot the controller for the changes to take effect. Click **Yes** to automatically reboot the RT target. You may also reboot the controller by right-clicking on the target name under **Remote Systems** and selecting **Reboot**.

After rebooting the PXI Express controller it will appear in the **Remote Systems** category with the assigned name.

6. Expand the PXI Express controller view in the **Remote Systems** branch and select **Software**.
7. Click the **Add/Remove Software** button in the toolbar to launch the LabVIEW Real-Time Software Wizard.
8. Install the LabVIEW Real-Time software and device drivers that you require on the RT target. Refer to the NI Web site at ni.com/info and enter the Info Code `et_spc` for the latest information about supported software.

After installation of the software the controller will automatically reboot and you will now be able to program it using LabVIEW Real-Time.



Note Refer to the *RT Getting Started Guide* available on your host computer for more information about setting up your RT target.

LabVIEW RT Configuration Switches

Use the LabVIEW RT configuration switches to configure LabVIEW RT if it is installed on the controller. If you are not using LabVIEW RT, these switches should remain in the OFF position. The controller reads these switches only after a system reset.

The NI PXIe-8135 controller includes the following LabVIEW RT configuration switches:

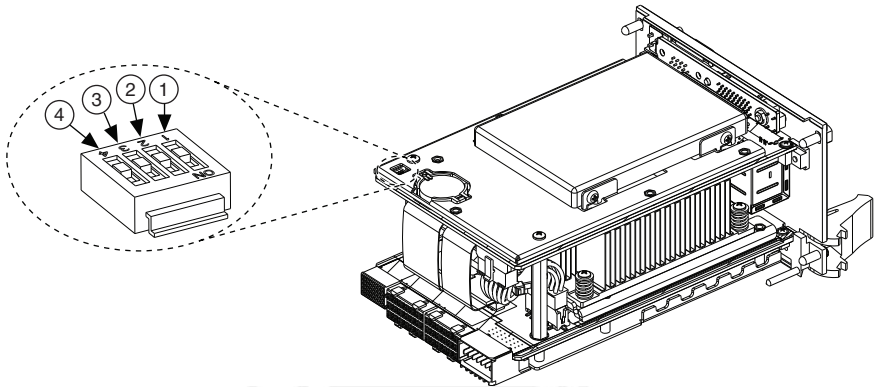
- Switch 1—**Boot LabVIEW RT**: Set this switch to ON to boot LabVIEW RT.
- Switch 2—**Boot Safe Mode**: Set this switch to ON to boot LabVIEW RT into safe mode to reconfigure TCP/IP settings and to download or update software from a host computer. This switch overrides the behavior of Switch 1. Booting the controller into safe mode does not start the embedded LabVIEW RT engine. After changing the settings or software, reboot the controller with this switch OFF to resume normal operation.
- Switch 3—**Disable Startup VI**: Set this switch to ON to prevent VIs from automatically running at startup if the controller becomes inaccessible because of a startup VI.
- Switch 4—**Reset IP Address**: Set this switch to ON to reset the IP address and other TCP/IP settings to their factory defaults. Use this switch if moving the controller to a different subnet or if the current TCP/IP settings are valid.



Note By default, the target will automatically attempt to connect to the network using DHCP. If the target is unable to initiate a DHCP connection, the target connects to the network with a link-local IP address or `169.254.x.x`.

Figure 2-4 shows the location of the LabVIEW RT configuration switches. The switches are shown in the OFF position.

Figure 2-4. LabVIEW RT Configuration Switches



1 Switch 1—Boot LabVIEW RT
2 Switch 2—Boot Safe Mode

3 Switch 3—Disable Startup VI
4 Switch 4—Reset IP Address

Drivers and Software

Your hard drive includes a directory called `images` in its root that contains software and soft copies of manuals for the peripherals. The directory structure under the `images` directory is logically organized into several levels.

In the `images` directory, you will find a `manuals` directory, an `os` directory, and a `drivers` directory.

The `manuals` directory contains quick reference guides, technical reference manuals, and National Instruments software manuals, all in Adobe Acrobat format. To access any manual, change your directory to `c:\images\manuals` and list the contents of that directory.

The `os` directory contains a subdirectory corresponding to the operating system installed on your computer.

The `drivers` directory contains driver installers for the system peripherals. These files and directories are copied exactly from the manufacturer distribution disks, so the naming conventions vary from peripheral to peripheral.

PXI Express Features

PXI Express Trigger Connectivity

The SMB connector on the NI PXIe-8135 front panel can connect to or from any PXI Express backplane trigger line. A trigger allocation process is needed to prevent two resources from connecting to the same trigger line, resulting in the trigger being double-driven and possibly damaging the hardware. At the time of this manual's publication, this software is not yet available for Windows. Contact National Instruments for more information.

PXI Express Chassis Configuration

The PXI Express Platform Services software installed on your controller and available on the *National Instruments Driver DVD* or *PXI Platform Services CD* included with your kit automatically identifies your PXI Express system components to generate a `pxiesys.ini` and `pxisys.ini` file. You can configure your entire PXI Express system through Measurement & Automation Explorer (MAX), included with your controller. MAX creates the `pxiesys.ini` and `pxisys.ini` file, which define your PXI Express system parameters. MAX also provides an interface to route and reserve triggers so dynamic routing, through drivers such as DAQmx, avoids double-driving and potentially damaging trigger lines. For more information about routing and reserving PXI Express triggers, refer to KnowledgeBase 3TJDOND8, *Using PXI Timing and Triggering Functionality*, at ni.com/support.

The configuration steps for single or multiple-chassis systems are the same.

PXI Express System Configuration

1. Launch Measurement & Automation Explorer (MAX).
2. In the **Configuration** tree, expand **Devices and Interfaces**.
3. In the **Devices and Interfaces** tree, expand **PXI System**. Your PXI Express chassis is already identified and appears in the **PXI System** tree.
4. For each unidentified PXI Express chassis in the **PXI System** tree, right-click on the chassis and select the appropriate chassis model through the **Identify As** submenu. Further expanding the **PXI System** branch shows all devices in the system that NI-VISA can recognize.

The PXI Express specification allows for many combinations of PXI Express chassis and system modules. To assist system integrators, PXI Express chassis and system module manufacturers must document their products' capabilities. PXI Express devices must provide a driver and/or `.ini` file for identification. For NI PXI Express chassis and controllers, these files are provided as part of the NI PXI Platform Services software included with your controller. System integrators, configuration utilities, and device drivers can use these `.ini` files.

The NI PXI Platform Services software uses the system module driver, chassis driver, and `chassis.ini` files to generate the PXI/PXI Express system description files (`pxisys.ini`

and `pxiesys.ini`). Device drivers and other utility software read the `pxiesys.ini` and `pxisys.ini` files to obtain system information. For detailed information about initialization files, refer to the PXI Express specification at www.pxisa.org.

Upgrading RAM

You can change the amount of installed RAM on the NI PXIe-8135 by upgrading the SO-DIMMs.

To upgrade the RAM, remove the NI PXIe-8135 from the PXI Express chassis. To optimize both memory capacity and system performance, use the same size and speed memory module in each of the two module slots. The use of different size modules in each slot is supported, but system performance will be slower than using two matched modules. However, two mismatched modules could result in better performance than using a single module.

National Instruments offers the following SO-DIMM for use with the NI PXIe-8135 controller.

- PC3-12800 (DDR3 1600) 4 GB, 256 MB × 64, CL 9, 1.18 in. max (NI part number 782341-4096)
- PC3-12800 (DDR3 1600) 8 GB, 512 MB × 64, CL 9, 1.18 in. max (NI part number 782341-8192)

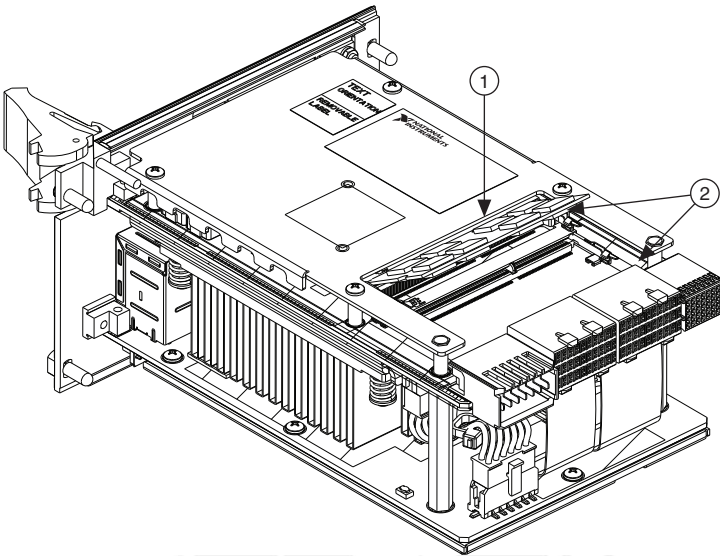


Note National Instruments has tested and verified that the DDR3 SO-DIMMs we sell work with the NI PXIe-8135. We recommend you purchase your DDR3 SO-DIMM modules from National Instruments. Other off-the-shelf DDR3 SO-DIMM modules are not guaranteed to work properly.

When installing memory modules into the memory sockets, the lower socket must be populated first, followed by the upper socket. If a single memory module is used, it must be installed in the lower socket.

The NI PXIe-8135 removable hard drive variant has a single module slot that supports up to an 8 GB DDR3 SO-DIMM module.

Figure 2-5. Installing a DDR3 SO-DIMM in an NI PXIe-8135 Controller



1 DDR3 SO-DIMM Module in Upper Socket

2 DDR3 SO-DIMM Sockets

Hard Drive Recovery

NI PXIe-8135 controllers include two methods of restoring the original factory condition of your hard drive. Hard drive-based recovery stores a factory backup on a separate portion of your hard drive allowing you to restore your controller without additional media. The NI PXIe-8135 controller also ships with an *OS Recovery* CD that allows you to reinstall your operating system onto your hard drive through an external USB CD/DVD-ROM. For more information on these tools, refer to KnowledgeBase 2ZKC02OK, *Hard Drive Recovery and OS Installation for PXI and VXI Controllers*, at ni.com/support.



Note The hard drive recovery hot key is <F4>. To access the hard drive-based recovery tool, press and hold <F4> when video first appears during the boot process.

If you need to recover your factory-installed operating system from a CD, you can use the included OS re-installation CD with an external USB CD/DVD-ROM drive. Boot the PXI Express controller using the OS re-installation CD to recover the OS. You also may need to reinstall other software after using the CD to recover the OS.



Note Recovering the OS erases the contents of your hard disk. Back up any files you want to keep.

Installing an OS

NI PXIe-8135 controllers include a preinstalled OS. In some cases, you may want to install a different OS. When doing so, consider the following guidelines.

Installing from a USB CD/DVD-ROM

The NI PXIe-8135 supports the installation of Windows 7 or Windows XP from a USB CD/DVD-ROM. As an alternative to a USB CD/DVD-ROM drive, you can use an external SCSI CD-ROM with a PXI-SCSI adapter.



Note For additional assistance with installing or changing an operating system, refer to KnowledgeBase 2ZKC02OK, *Hard Drive Recovery and OS Installation for PXI and VXI Controllers*, at ni.com/support.

ExpressCard

This section provides information on the installation and removal of ExpressCard™ modules.

Installing an ExpressCard

You can install an ExpressCard module while the NI PXIe-8135 is running. The NI PXIe-8135 will automatically detect the card. ExpressCards are generally marked with a symbol or a label to indicate which end to insert into the slot. The cards are keyed to prevent incorrect insertion.

To install an ExpressCard, complete the following steps.

1. Hold the card so the top side is facing left.
2. Insert the card until it is completely seated in its connector. The connector has an automatic eject mechanism. If you insert the card and it is ejected, simply re-insert the card until it is seated.

If you encounter too much resistance, do not force the card. Check the card orientation and try again.

The NI PXIe-8135 will automatically recognize the ExpressCard and load the appropriate driver(s). Third-party cards may require that you install additional drivers. Contact your ExpressCard vendor for more information.

Removing an ExpressCard

To remove the ExpressCard module push in the module and then release to eject the card. Slide the card out of the slot.



Caution To avoid data loss and other potential issues, stop communication with your ExpressCard device before removing it from the NI PXIe-8135. In Windows, use the **Safely Remove Hardware** tool to safely stop the ExpressCard.

Removable Hard Drive

This section provides information on the installation and removal of the removable hard drive.



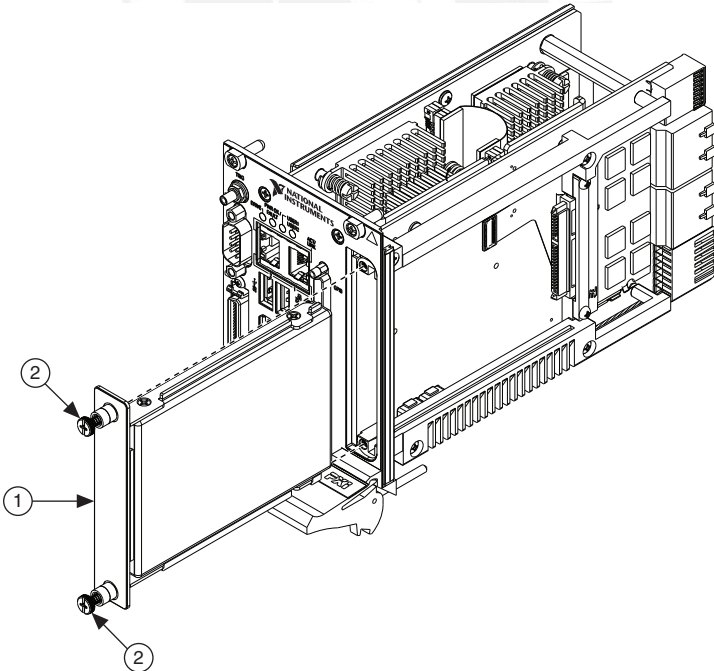
Caution The removable hard drive must be installed before powering on the NI PXIe-8135 and should not be removed during operation.

Installing the Removable Hard Drive

To install the removable hard drive, complete the following steps:

1. Hold the removable hard drive so that the top side is facing right, as shown in Figure 2-6.
2. Insert the removable hard drive so that it is completely seated in its connector. The insertion resistance will increase for the final connector mate.
3. If the removable hard drive does not easily insert, do *not* force the drive. Check the alignment and try again. The removable hard drive may not be flush with the front of the NI PXIe-8135 when fully inserted.
4. Tighten the thumb screws. If the thumb screws do not thread, the removable hard drive may not be fully inserted. Try removing and completely inserting the removable hard drive.

Figure 2-6. Installing the Removable Hard Drive in an NI PXIe-8135 Controller



1 Removable Hard Drive

2 Thumb Screws (2x)

Removing the Removable Hard Drive

To remove the removable hard drive, complete the following steps:

1. Power off the chassis.
2. Loosen the thumb screws.
3. Unseat the removable hard drive from the connector and remove it from the slot.

Store the hard drive in the original antistatic packaging when not in use to avoid damage.



I/O Information

Front Panel Connectors

Table 3-1 lists various peripherals and their corresponding NI PXIe-8135 external connectors, bus interfaces, and functions.

Table 3-1. NI PXIe-8135 Peripherals Overview

Peripheral	External Connector	Description
Video	DisplayPort (2 connectors)	ATI Radeon E4690 Embedded GPU
Serial	COM1 (9-pin DSUB)	16550 RS-232 serial port
Ethernet Port 1	LAN (RJ45, dual stacked)	10/100/1000 Ethernet Intel 82579 WOL capable
Ethernet Port 2	LAN (RJ45, dual stacked)	10/100/1000 Ethernet Intel 82574 Not WOL capable
Parallel	Parallel Port (36-pin champ)	IEEE 1284
USB 2.0	USB 4-pin Series A stacked receptacle (4 ports)	USB 2.0 capable
USB 3.0	USB 9-pin Series A stacked receptacle (2 ports)	USB 3.0 and USB 2.0 capable
PXI Express trigger	Trigger (SMB)	Routing PXI Express triggers to or from the backplane trigger bus
GPIB device	GPIB (25-pin Micro D)	General-Purpose Interface Bus, IEEE 488.2
ExpressCard Variant		
ExpressCard/34 module	ExpressCard/34 slot	ExpressCard/34 expansion

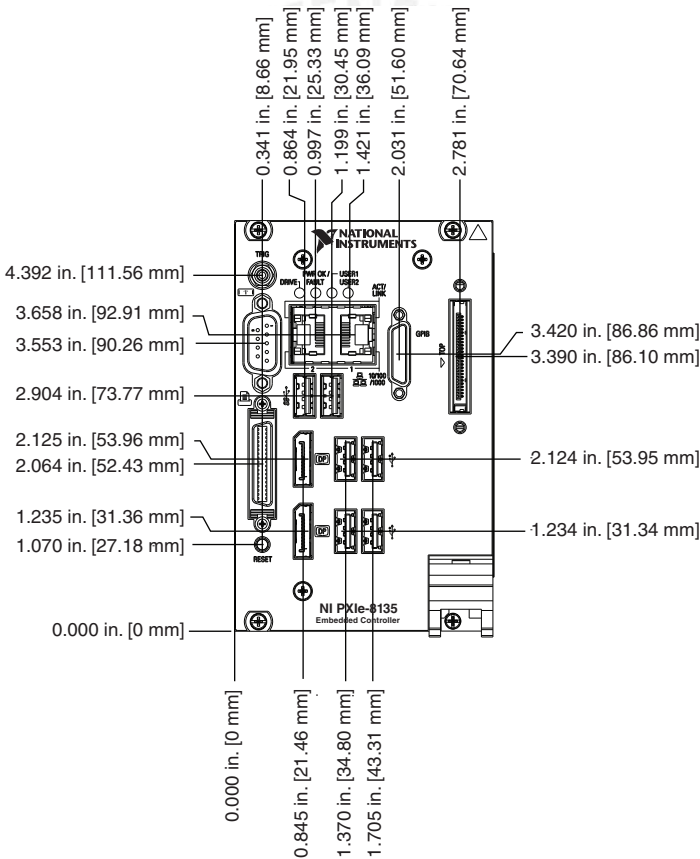
Table 3-1. NI PXIe-8135 Peripherals Overview (Continued)

Peripheral	External Connector	Description
Removable Hard Drive Variant		
Removable Hard Drive	Removable HDD	Removable Hard Disk Drive

Front Panel

Figures 3-1 and 3-2 show the front panel layout and dimensions of the NI PXIe-8135. Dimensions are in inches [millimeters].

Figure 3-1. NI PXIe-8135 Front Panel Layout and Dimensions (ExpressCard Variant)



DisplayPort

Figure 3-3 shows the location and pinouts for the DisplayPort connectors on the NI PXIe-8135. Table 3-2 lists and describes the DisplayPort connector signals.

Figure 3-3. DisplayPort Connector Location and Pinout

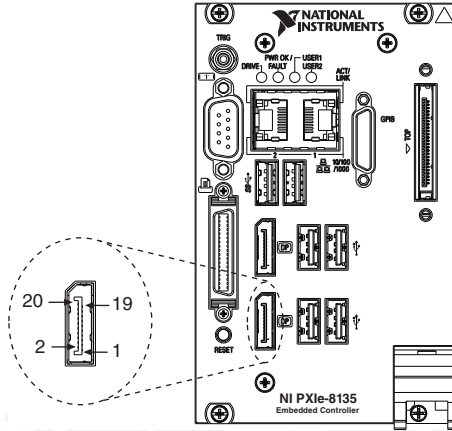


Table 3-2. DisplayPort Connector Signals

Pin	Signal Name
1	ML_Lane0(p)
2	GND
3	ML_Lane0(n)
4	ML_Lane1(p)
5	GND
6	ML_Lane1(n)
7	ML_Lane2(p)
8	GND
9	ML_Lane2(n)
10	ML_Lane3(p)
11	GND
12	ML_Lane3(n)
13	CONFIG1

Table 3-2. DisplayPort Connector Signals (Continued)

Pin	Signal Name
14	CONFIG2
15	AUX CH (p)
16	GND
17	AUX CH (n)
18	Hot Plug Detect
19	Return
20	DP_PWR

COM1

Figure 3-4 shows the location and pinouts for the COM1 connector on the NI PXIe-8135. Table 3-3 lists and describes the COM1 connector signal.

AMP manufactures a serial port mating connector, part number 745491-5.

Figure 3-4. COM1 Connector Location and Pinout

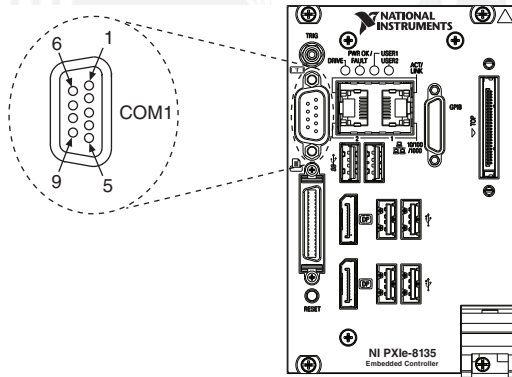


Table 3-3. COM1 Connector Signals

Pin	Signal Name	Signal Description
1	DCD#	Data Carrier Detect
2	RXD#	Receive Data
3	TXD#	Transmit Data
4	DTR#	Data Terminal Ready
5	GND	Ground
6	DSR#	Data Set Ready
7	RTS#	Ready to Send
8	CTS#	Clear to Send
9	RI#	Ring Indicator

Note: The pound symbol (#) indicates an active low signal.

Ethernet

Figure 3-5 shows the location and pinouts for the dual stacked Ethernet connector on the NI PXIe-8135. Table 3-4 lists and describes the Ethernet connector signals.

AMP manufactures a mating connector, part number 554739-1.

Figure 3-5. Ethernet Connector Location and Pinout

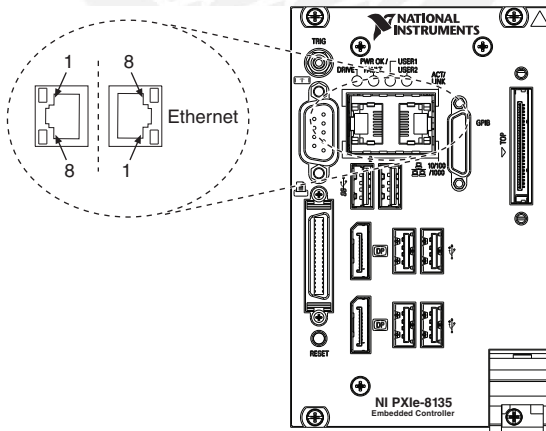


Table 3-4. Ethernet Connector Signals

Pin	Fast Ethernet	Gigabit Ethernet
1	TX+	TX_A+
2	TX-	TX_A-
3	RX+	RX_B+
4	NC	TX_C+
5	NC	TX_C-
6	RX-	RX_B-
7	NC	RX_D+
8	NC	RX_D-



Note The Ethernet controllers can perform an automatic crossover, thus eliminating the need for crossover cables.

Table 3-5. 10/100/1000 LAN Connector LED States

LED	Color	LED State	Condition
ACT/ LINK	Green	Off	LAN link is not established.
		On (steady state)	LAN link is established.
		On (brighter and pulsing)	The controller is communicating with another computer on the LAN.
10/100/ 1000	(None)	Off	10 Mbit/sec data rate is selected.
	Green	On	100 Mbit/sec data rate is selected.
	Amber	On	1000 Mbit/sec data rate is selected.

Parallel Port

Figure 3-6 shows the location and pinouts for the IEEE 1284 (parallel) connector on the NI PXIe-8135. Table 3-6 lists and describes the IEEE 1284 connector signals.

Parallel port adapter cables are available from National Instruments, part number 777169-01.

Figure 3-6. Parallel Port Connector Location and Pinout

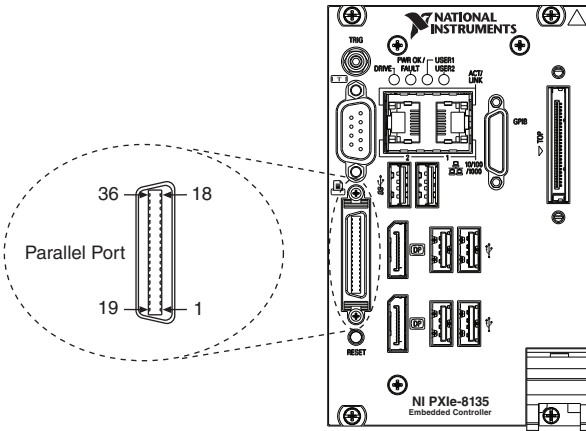


Table 3-6. Parallel Port Connector Signals

Pin	Default Configuration (LPT)	
	Signal Name	Signal Description
1	BUSY	Device Busy
2	SLCT	Select
3	ACK#	Acknowledge
4	FAULT#(ERROR#)	Fault
5	PAPEREND	Paper End
6	PD0	Data Bit 0
7	PD1	Data Bit 1
8	PD 2	Data Bit 2
9	PD3	Data Bit 3
10	PD4	Data Bit 4
11	PD5	Data Bit 5

Table 3-6. Parallel Port Connector Signals (Continued)

Pin	Default Configuration (LPT)	
	Signal Name	Signal Description
12	PD6	Data Bit 6
13	PD7	Data Bit 7
14	INIT#	Initialize Printer
15	STROBE#	Strobe
16	SLCTIN#	Select Input
17	AUTOFD#	Auto Line Feed
18	+5V	+5 V
19 to 35	GND	Ground
36	NC	Not Connected

Note: The pound symbol (#) indicates an active low signal.

Universal Serial Bus

Figure 3-7 shows the location and pinouts for the Universal Serial Bus (USB) connectors on the NI PXIe-8135. Each controller has 4 USB ports on the front panel. Table 3-7 lists and describes the USB connector signals.

Figure 3-7. USB Connector Location and Pinout

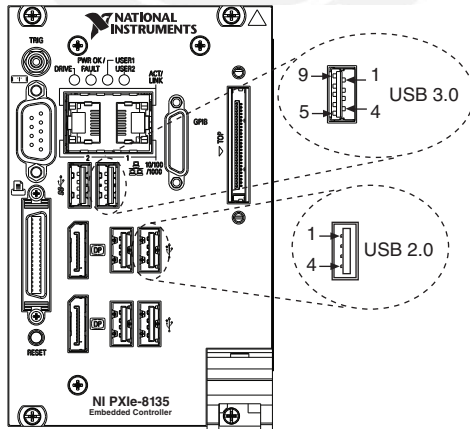


Table 3-7. USB 2.0 Connector Signals

Pin	Signal Name	Signal Description
1	VCC	Cable Power (+5 V)
2	-Data	USB Data -
3	+Data	USB Data +
4	GND	Ground

Table 3-8. USB 3.0 Connector Signals

Pin	Signal Name	Signal Description
1	VCC	Cable Power (+5 V)
2	-Data	USB Data -
3	+Data	USB Data +
4	GND	Ground
5	StdA_SSRX-	USB Data Receive-
6	StdA_SSRX+	USB Data Receive+
7	GND_DRAIN	Ground
8	StdA_SSTX-	USB Data Transmit-
9	StdA_SSTX+	USB Data Transmit+

GPIO (IEEE 488.2)

Figure 3-9 shows the location and pinouts for the GPIO connector on the NI PXIe-8135. Table 3-10 lists and describes the GPIO connector signals.

ITT Canon manufactures a GPIO mating connector, part number MDSM-25SC-Z11-V51.

Figure 3-9. GPIO Connector Location and Pinout

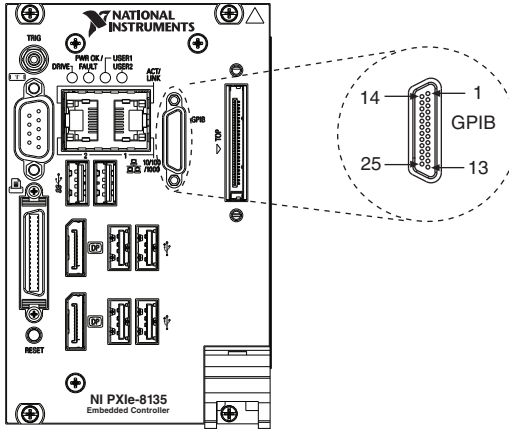


Table 3-10. GPIO Connector Signals

Pin	Signal Name	Signal Description
1	DIO1#	Data Bit 1
2	DIO2#	Data Bit 2
3	DIO3#	Data Bit 3
4	DIO4#	Data Bit 4
5	EOI#	End or Identify
6	DAV#	Data Valid
7	NRFD#	Not Ready for Data
8	NDAC#	Not Data Accepted
9	IFC#	Interface Clear
10	SRQ#	Service Request
11	ATN#	Attention
12	SHIELD	Chassis ground

Table 3-10. GPIB Connector Signals (Continued)

Pin	Signal Name	Signal Description
13	DIO5#	Data Bit 5
14	DIO6#	Data Bit 6
15	DIO7#	Data Bit 7
16	DIO8#	Data Bit 8
17	REN#	Remote Enable
18 to 25	GND	Logic Ground

Note: The pound symbol (#) indicates an active low signal.

ExpressCard/34 Slot (Optional)

The NI PXIe-8135 controller can be equipped with an optional ExpressCard/34 slot on the front panel, providing I/O expansion and options for removable storage.

Figure 3-10 shows the location and pinouts for the ExpressCard/34 slot on the NI PXIe-8135. Table 3-11 lists and describes the ExpressCard connector signals.

Figure 3-10. ExpressCard/34 Slot Location and Pinout

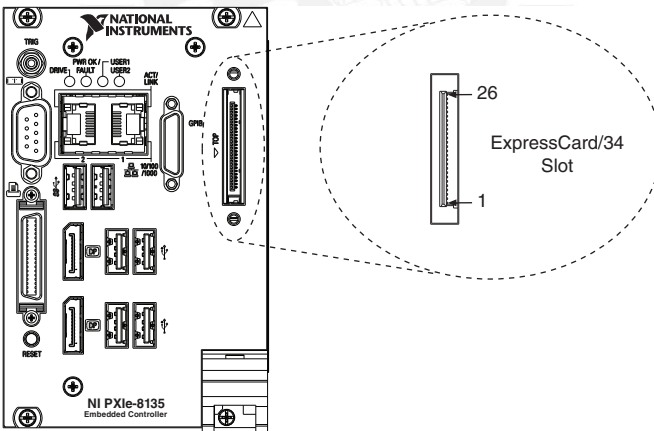


Table 3-11. ExpressCard Connector Signals

Pin	Signal Name	Signal Description
1	GND	Ground
2	USBD-	USB Data -
3	USBD+	USB Data +
4	CPUSB#	USB Presence
5	RESERVED	Reserved by spec for future use
6	RESERVED	Reserved by spec for future use
7	SMBCLK	SMBus Clock
8	SMBDATA	SMBus Data
9	+1.5V	Power
10	+1.5V	Power
11	WAKE#	PE Wake
12	+3.3VAUX	Power
13	PERST#	PE Reset
14	+3.3V	Power
15	+3.3V	Power
16	CLKREQ#	Clock Request
17	CPPE#	PE Presence
18	REFCLK-	Reference Clock -
19	REFCLK+	Reference Clock +
20	GND	Ground
21	PERn0	PE Data Receive -
22	PERp0	PE Data Receive +
23	GND	Ground
24	PETn0	PE Data Transmit -

Table 3-11. ExpressCard Connector Signals (Continued)

Pin	Signal Name	Signal Description
25	PETp0	PE Data Transmit +
26	GND	Ground

Note: The pound symbol (#) indicates an active low signal.

Removable Hard Drive (Optional)

The NI PXIe-8135 controller can be equipped with an optional removable hard drive on the front panel, providing an option for removable storage.

Figure 3-11 shows the location and pinouts for the removable hard drive on the NI PXIe-8135. Table 3-11 lists and describes the removable hard drive connector signals.

Figure 3-11. Removable Hard Drive Location and Pinout

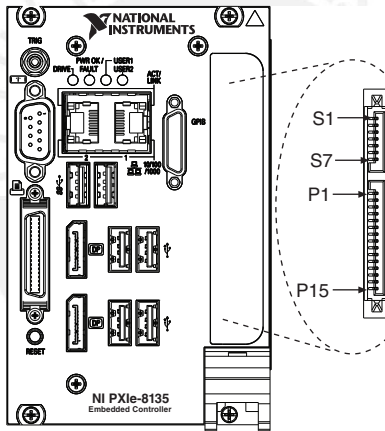


Table 3-12. Removable Hard Drive Connector Signals

Pin	Signal Name	Signal Description
S1	GND	Ground
S2	A+	SATA Transmit
S3	A-	SATA Transmit
S4	GND	Ground
S5	B+	SATA Receive
S6	B-	SATA Receive

Table 3-12. Removable Hard Drive Connector Signals (Continued)

Pin	Signal Name	Signal Description
S7	GND	Ground
P1	3.3 V	Power
P2	3.3 V	Power
P3	3.3 V	Power
P4	GND	Ground
P5	GND	Ground
P6	GND	Ground
P7	5 V	Power
P8	5 V	Power
P9	5 V	Power
P10	GND	Ground
P11	GND/Optional	Ground/Act/Staggerd Spinup
P12	GND	Ground
P13	NC	No Connect
P14	NC	No Connect
P15	NC	No Connect

Front Panel Features

The NI PXIe-8135 has the following front-panel features:

- A system reset pushbutton (press the button to generate a reset to the controller)
- Two front panel LEDs that show PC status
 - The **PWR OK/FAULT** LED indicates the status of the controller. The LED will indicate one of the following states:
 - Green ON steady—PXI Express and onboard power is on and within regulation limits.
 - Green BLINKING—The controller has entered the soft off state and is safe to power down.
 - OFF—The controller is powered off.
 - Red BLINKING—The controller detected a power rail fault when trying to boot.
 - Red Solid—The controller detected a thermal fault and has shut down to protect the system.
 - The **DRIVE** LED indicates when an access to the internal hard disk is occurring.
 - The **USER1** LED is a bi-color green/yellow LED. You can define the USER1 LED to meet the needs of your LabVIEW application.
 - The **USER2** LED is a bi-color green/yellow LED. You can define the USER2 LED to meet the needs of your LabVIEW application.

Data Storage

The NI PXIe-8135 has the following data storage features:

- Internal Serial ATA hard drive
 - 250 GB or larger 2.5 in. notebook hard drive
 - Supports Native Command Queuing
 - Supports transfer rates up to 600 MB/s
- Removable Serial ATA hard drive (Removable hard drive variant only)
 - 250 GB or larger 2.5 in. notebook hard drive
 - Supports Native Command Queuing
 - Supports transfer rates up to 300 MB/s
- USB storage support—USB CD/DVD-ROM, mass storage device, or floppy drive

Common Configuration Questions

This chapter answers common configuration questions you may have when using a NI PXIe-8135 embedded controller.

General Questions

What do the LEDs on the NI PXIe-8135 front panel mean?

Refer to the LED status descriptions in the *Removable Hard Drive (Optional)* section of Chapter 3, *I/O Information*.

After shutting down my NI PXIe-8135 controller, the Port 1 Ethernet LEDs continue to blink. Is it safe to remove my controller or disconnect power?

The NI PXIe-8135's port 1 Intel 82579 Ethernet device remains powered even after shutdown. It is safe to remove your controller or disconnect power.

How do I check the configuration of the memory, hard drive, time/date, and so on?

You can view these parameters in the BIOS setup. To enter the BIOS setup, reboot the NI PXIe-8135 and press <Delete> during the memory tests. Refer to the *Accessing BIOS Setup Utility* section of Chapter 2, *Installation and Configuration*, for more information.

Can I use the internal Serial ATA drive and an external hard drive at the same time?

Yes. Refer to the *BIOS Setup Utility* section of Chapter 2, *Installation and Configuration*, for more information.

Boot Options

What devices can I boot from?

The NI PXIe-8135 can boot from the following devices:

- The internal Serial ATA hard drive
- An external SCSI hard drive or SCSI CD/DVD-ROM if a SCSI adapter, such as the PXI-8214, is used
- A network PXE server on the same subnet

- An external USB mass storage device such as a USB hard drive, USB CD/DVD-ROM, or USB flash drive
- An external USB floppy drive
- Most PCI or PCIe-based devices that provide an Option ROM



Note There are some limitations when booting from a USB device. Windows 7 and Windows XP can be installed from a USB CD/DVD-ROM, but earlier versions of Windows cannot. The NI PXIe-8135 BIOS configures the USB devices so that they will work in a DOS environment.

How do I configure the controller to boot from these devices?

There are two methods.

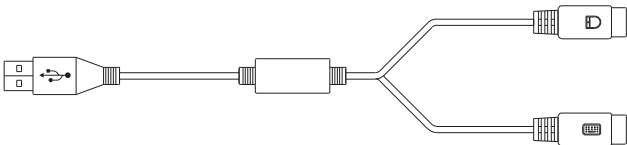
- Enter the BIOS setup by rebooting the controller and pressing <Delete> during the memory tests. Select the **Boot** menu. You will see a list of all bootable devices, ordered by device type. You can set the boot order by altering the **1st Boot Device**, **2nd Boot Device**, and **3rd Boot Device** settings.
- To boot from a different device without permanently changing the boot order, press <F10> during POST. After the BIOS completes the POST and just before the controller boots the OS, the **Boot** menu is displayed. You can select the device type you want to boot from.

Cables and Connections

How do I plug both a PS/2 mouse and PS/2 keyboard into the controller?

The NI PXIe-8135 has no PS/2 connector, and you need to use a USB Y-splitter cable as shown in Figure 4-1, or a similar device, to connect both a PS/2 mouse and PS/2 keyboard. National Instruments part number 778713-01 is such a cable and is available through the online catalog at ni.com/products.

Figure 4-1. Y-Splitter Cable



What if I don't have a Y-splitter cable? Can I still use a mouse and keyboard?

If you do not have a Y-splitter cable, plug a USB keyboard into any USB connector. You can also plug a USB mouse into any USB connector.

How do I connect a standard 25-pin LPT cable to the NI PXIe-8135?

The NI PXIe-8135 uses a type C LPT connector. Most parallel port devices use a type A connector. To use a device with a standard type A LPT connector, you need to use a type C-to-type A LPT adapter. Parallel port adapter cables, part number 777169-01, are available through the online catalog at ni.com/products.

Software Driver Installation

How do I install or reinstall the video driver?

Refer to KnowledgeBase 3H3COSD8, *What Peripheral Drivers Should I Use with My PXI or VXI Controller?*, at ni.com/support.

How do I install or reinstall the Ethernet driver?

Refer to KnowledgeBase 3H3COSD8, *What Peripheral Drivers Should I Use with My PXI or VXI Controller?*, at ni.com/support.

How do I install or reinstall the GPIB driver?

The NI-488.2 driver for your GPIB port is installed by default when your controller is first shipped from the factory. To change the default installed driver, complete the following steps:

1. Download the latest GPIB driver from ni.com/downloads.
2. Install the driver and verify that the driver has properly detected the GPIB driver in the Device Manager. If you need more assistance, refer to ni.com/support/install.

How do I install software from a CD?

The compact size of the NI PXIe-8135 does not allow for an integrated USB CD/DVD-ROM drive. If you are using Windows 7 or Windows XP, you have the following options:

- **USB CD/DVD-ROM**—Windows 7 and Windows XP support installing from a USB CD/DVD-ROM using a bootable installation CD.
- **SCSI CD-ROM**—Windows 7 and Windows XP supports installing from a SCSI CD-ROM using a bootable installation CD.
- **Mapped network drive**—You can use the Ethernet to connect to another computer. If you share the USB CD/DVD-ROM drive on the other computer, you can map the shared USB CD/DVD-ROM drive to a drive letter on the NI PXIe-8135.

A USB CD/DVD-ROM drive is available from National Instruments, part number 778492-01.

Upgrade Information

How do I upgrade system memory?

You can change the amount of installed RAM on the NI PXIe-8135 by upgrading the DDR3 SO-DIMMs.

To upgrade the RAM, remove the NI PXIe-8135 from the PXI Express chassis. To optimize both memory capacity and system performance, use the same size and speed memory module in each of the two module slots. The use of different size modules in each slot is supported, but system performance will be slower than using two matched modules. However, two mismatched modules will result in better performance than using a single module.

National Instruments offers the following types of SO-DIMMs for use with the NI PXIe-8135 controller.

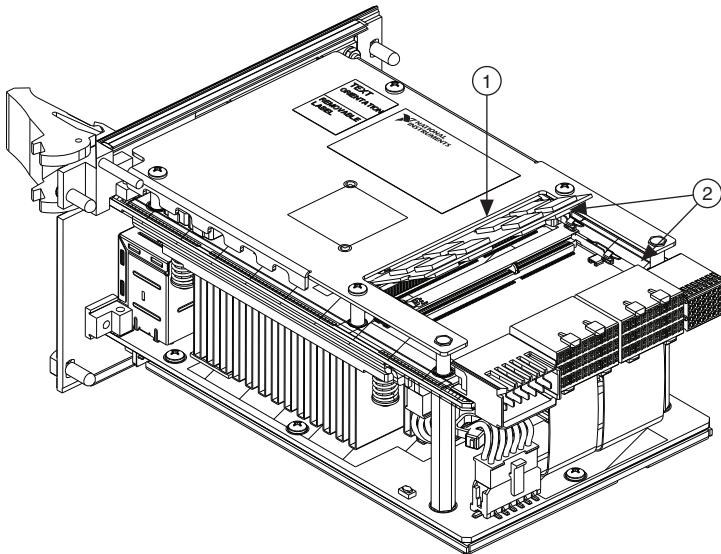
- PC3-12800 (DDR3 1600) 4 GB, 256 MB × 64, CL 9, 1.18 in. max (NI part number 782341-4096)
- PC3-12800 (DDR3 1600) 8 GB, 512 MB × 64, CL 9, 1.18 in. max (NI part number 782341-8192)



Note National Instruments has tested and verified that the DDR3 SO-DIMMs we sell work with the NI PXIe-8135. We recommend you purchase your DDR3 SO-DIMM modules from National Instruments. Other off-the-shelf DDR3 SO-DIMM modules are not guaranteed to work properly.

When installing memory modules into the memory sockets, the lower socket must be populated first, followed by the upper socket. If a single memory module is used, it must be installed in the lower socket.

The NI PXIe-8135 removable hard drive variant has a single module slot that supports up to an 8 GB DDR3 SO-DIMM module.

Figure 4-2. Installing a DDR3 SO-DIMM in an NI PXIe-8135 Controller

1 DDR3 SO-DIMM Module in Upper Socket

2 DDR3 SO-DIMM Sockets

How do I flash a new BIOS?

You can download the new BIOS from ftp.ni.com/support/pxi. For more information, refer to KnowledgeBase 2GIGKD0Z, *Determining and Upgrading PXI and VXI Embedded Controller BIOS Versions*.

Where do I get the latest software drivers?

The latest National Instruments software is available from ni.com/downloads. For peripheral drivers, refer to KnowledgeBase 3H3COSD8, *What Peripheral Drivers Should I Use with My PXI or VXI Controller?*, at ni.com.

My NI PXIe-8135 does not have an internal floppy drive. Is there a way to use an external drive?

Yes. The NI PXIe-8135 controller supports and can boot from USB floppy drives. Refer to the [Boot Options](#) section for more information.

A USB floppy drive is available from National Instruments, part number 778492-02.

PXI Express Configuration

How do I use the SMB trigger on the front panel?

For details, refer to the *PXI Express Features* section of Chapter 2, *Installation and Configuration*.

Why doesn't the NI PXIe-8135 work with the PXI-8220 or PXI-8221?

The serialized IRQ line is not routed to the Intel 7 Series chipset on the NI PXIe-8135. This prevents PC cards using ISA interrupts from working with the NI PXIe-8135.



Troubleshooting

This chapter answers common troubleshooting questions you may have when using the NI PXIe-8135 embedded computer.

What if the NI PXIe-8135 does not boot?

Several problems can cause a controller not to boot. Here are some things to look for and possible solutions.

Things to Notice:

- Which LEDs come on? The **PWROK/FAULT** LED should stay lit green. The **Drive** LED should blink during boot as the disk is accessed.
- What appears on the display? Does it hang at some particular point (BIOS, Operating System, and so on)? If nothing appears on the screen, try a different monitor. Does your monitor work with a different PC? If it hangs, note the last screen output that you saw for reference when consulting National Instruments technical support.
- What has changed about the system? Did you recently move the system? Was there electrical storm activity? Did you recently add a new module, memory chip, or piece of software?
- Refer to your chassis user manual for additional troubleshooting steps.

Things to Try:

- Make sure the chassis is plugged in to a working power source.
- Check any fuses or circuit breakers in the chassis or other power supply (possibly a UPS).
- Make sure the controller module is firmly seated in the chassis.
- Remove all other modules from the chassis.
- Remove any nonessential cables or devices.
- Try the controller in a different chassis.
- Try a similar controller in this same chassis.
- Clear the CMOS. (Refer to the *System CMOS* section of Chapter 2, *Installation and Configuration*.)
- Recover the hard drive on the controller. (Refer to the *Hard Drive Recovery* section of Chapter 2, *Installation and Configuration*.)
- Make sure the RAM is properly seated.
- For the removable hard drive variant, ensure the HDD shuttle is properly seated.

My controller boots fine until I get to Windows, at which point I cannot read the screen. This may include garbled output, white screen, black screen, or an out of synch message from the monitor.

This problem usually results from having the video card output set past the limits of the monitor. You will need to boot Windows in Safe Mode. To do this, reboot the controller. As Windows begins to boot, hold down <F8>. You should now be able to reset the video driver to lower settings. Try setting the resolution to 800 × 600 and the refresh rate to 60 Hz. Once you reboot, you can raise these values again, using the test option in Windows. These settings are accessible through the **Advanced** tab of the **Display** item in the **Control Panel**. Alternately, you can try a different monitor, preferably a newer and larger one.

My system boots fine as long as a particular module is not in my chassis.

The most common cause of this is a damaged module. Try the module in a different chassis or with a different controller. Also, remove any external cables or terminal blocks connected to the system. If the module does not work in these cases, it is likely damaged. Contact the module manufacturer for further troubleshooting.

Refer to the KnowledgeBase or product manuals section at ni.com for more information specific to the chassis and controller with which you are having difficulties.

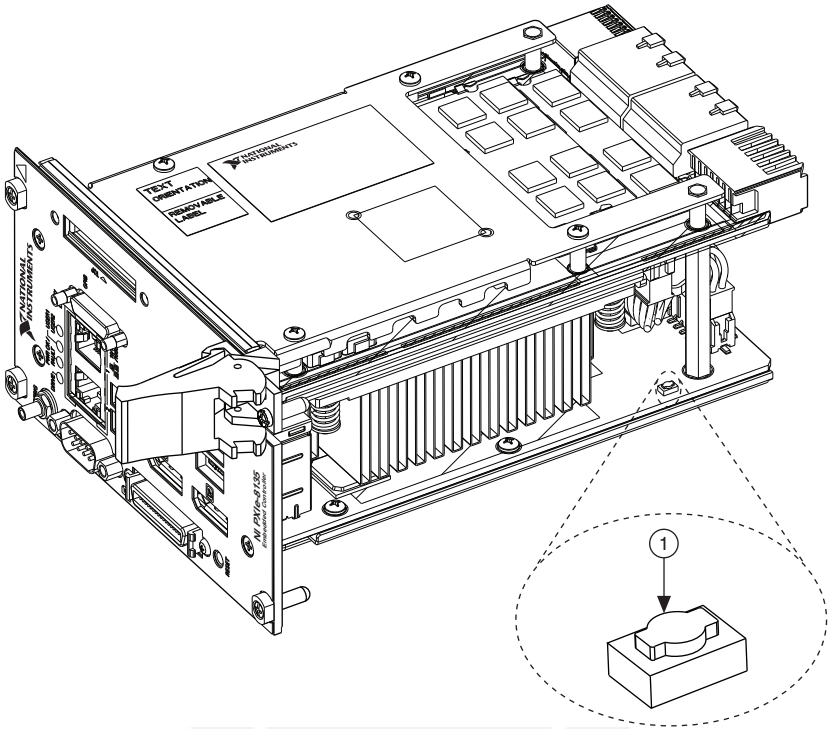
My CMOS is corrupted. How do I set it back to default?

1. Enter the BIOS setup program as described in the *Accessing BIOS Setup Utility* section of Chapter 2, *Installation and Configuration*.
2. Press <F9> to load BIOS defaults.
3. Answer **Y** (Yes) to the verification prompt.
4. Select **Save and Exit Setup**.

As an alternative method, complete the following steps:

1. Power off the chassis.
2. Remove the controller from the chassis.
3. Press the Clear CMOS button (SW2) as shown in Figure 5-1.
4. Wait ten seconds.
5. Reinstall the controller in the chassis.

Figure 5-1. Clearing the CMOS Contents



- 1 Push-Button Switch SW2

Specifications

This appendix lists the electrical, mechanical, and environmental specifications of the NI PXIe-8135 embedded controller.

Features

NI PXIe-8135	
CPU	Intel Core i7 3610 QE
CPU Frequency	2.3 GHz (base), 3.3 GHz (single-core Turbo mode)
On-die L2 cache	256 KB x4 (256 KB per core)
Dual-Channel DDR3 RAM, PC3 12800	4 GB Standard 16 GB Maximum
Single-Channel DDR3 RAM, PC3 12800*	4 GB Standard 8 GB Maximum
Hard Drive	250 GB or larger Serial ATA†
Ethernet	10/100/1000 BaseTX, 2 ports
PXI Express 4 Link Configuration	x4, x4, x4, x4
PXI Express 2 Link Configuration	x8, x8
GPIB (IEEE 488 Controller)	Yes
Serial Ports (RS-232)	Yes (1)
Parallel Port	Yes (1)
Hi-Speed USB (2.0) Ports	Yes (4)
Hi-Speed USB (3.0) Ports	Yes (2)
ExpressCard/34 Slot	Yes
PS/2 Keyboard/Mouse Connector	No
PXI Express Trigger Bus Input/Output	Yes

NI PXIe-8135	
Removable Hard Drive	Yes (1)
Installed Operating System	Windows 7 Professional, Windows XP Professional SP3 for Embedded Systems
* Removable hard drive option.	
† Extended-temperature 24/7 option provides 80 GB minimum hard drive. Controllers configured for LabVIEW RT provide a 80 GB (minimum) SATA hard drive.	

Electrical

Voltage (V)	Current (Amps)	
	Typical	Maximum
+3.3 V	3.75 A	5.4 A
+5 V	1.5 A	2.0 A
+12 V	3.5 A	5.0 A
-12 V	0.00 A	0.00 A
+5 V Aux	0.3 A	0.4 A

Physical

Board dimensions	Four-wide 3U PXI Express module
Slot requirements	One system slot plus three controller expansion slots
Compatibility	Fully compatible with <i>PXI Express Specification 1.0</i>
Weight	1.30 kg (2.87 lb) typical

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2
Indoor use only.	



Caution Clean the NI PXIe-8135 with a soft nonmetallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Operating Environment

NI PXIe-8135

Ambient temperature range

Standard 5 to 50 °C¹
 (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 high temperature limit.)

Extended Temperature

Option 0 to 55 °C¹
 (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.)

Relative humidity range..... 10% to 90%, noncondensing
 (Tested in accordance with IEC-60068-2-56.)



Caution The operating temperature must not be exceeded, even when used in a chassis with a higher temperature range.

Storage Environment

NI PXIe-8135

Ambient temperature range

Standard -40 to 65 °C
 (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit.)

Extended Temperature

Option -40 to 71 °C
 (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 limits.)

Relative humidity range..... 5% to 95%, noncondensing
 (Tested in accordance with IEC-60068-2-56.)

Shock and Vibration

Operating Shock 30 g peak, half-sine, 11 ms pulse
 (Tested in accordance with IEC-60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)

¹ Processor should not throttle CPU frequency under reasonable, worst case processor work loads in high operating temperatures.

Random Vibration

- Operating 5 to 500 Hz, 0.3 g_{rms} (with solid-state hard drive)
- Nonoperating 5 to 500 Hz, 2.4 g_{rms}
(Tested in accordance with IEC-60068-2-64.
Nonoperating test profile exceeds the
requirements of MIL-PRF-28800F, Class 3.)



Note Specifications are subject to change without notice.

Safety

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1



Note For UL and other safety certifications, refer to the product label or the [Online Product Certification](#) section.



Caution Using the NI PXIe-8135 in a manner not described in this document may impair the protection the NI PXIe-8135 provides.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions



Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia and New Zealand (per CISPR 11) Class A equipment is intended for use only in heavy-industrial locations.



Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generates radio frequency energy for the treatment of material or inspection/analysis purposes.



Note For EMC declarations and certifications, and additional information, refer to the [Online Product Certification](#) section.

CE Compliance

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

To obtain product certifications and the Declaration of Conformity (DoC) for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* Web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)



EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit ni.com/environment/weee.

Battery Replacement and Disposal



Battery Directive This device contains a long-life coin cell battery. If you need to replace it, use the Return Material Authorization (RMA) process or contact an authorized National Instruments service representative. For more information about compliance with the EU Battery Directive 2006/66/EC about Batteries and Accumulators and Waste Batteries and Accumulators, visit ni.com/environment/batterydirective.

电子信息产品污染控制管理办法（中国 RoHS）



中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息, 请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

Technical Support and Professional Services

Log in to your National Instruments ni.com User Profile to get personalized access to your services. Visit the following sections of ni.com for technical support and professional services:

- **Support**—Technical support at ni.com/support includes the following resources:
 - **Self-Help Technical Resources**—For answers and solutions, visit ni.com/support for software drivers and updates, a searchable KnowledgeBase, product manuals, step-by-step troubleshooting wizards, thousands of example programs, tutorials, application notes, instrument drivers, and so on. Registered users also receive access to the NI Discussion Forums at ni.com/forums. NI Applications Engineers make sure every question submitted online receives an answer.
 - **Standard Service Program Membership**—This program entitles members to direct access to NI Applications Engineers via phone and email for one-to-one technical support, as well as exclusive access to self-paced online training modules at ni.com/self-paced-training. All customers automatically receive a one-year membership in the Standard Service Program (SSP) with the purchase of most software products and bundles including NI Developer Suite. NI also offers flexible extended contract options that guarantee your SSP benefits are available without interruption for as long as you need them. Visit ni.com/ssp for more information.
For information about other technical support options in your area, visit ni.com/services, or contact your local office at ni.com/contact.
- **Training and Certification**—Visit ni.com/training for training and certification program information. You can also register for instructor-led, hands-on courses at locations around the world.
- **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, National Instruments Alliance Partner members can help. To learn more, call your local NI office or visit ni.com/alliance.
- **Declaration of Conformity (DoC)**—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer’s declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting ni.com/certification.
- **Calibration Certificate**—If your product supports calibration, you can obtain the calibration certificate for your product at ni.com/calibration.

You also can visit the Worldwide Offices section of ni.com/niglobal to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.



Glossary

Symbol	Prefix	Value
n	nano	10^{-9}
μ	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^3
M	mega	10^6
G	giga	10^9
T	tera	10^{12}

Symbols

° Degrees.

Ω Ohms.

% Percent.

A

A Amperes.

AC Alternating Current.

B

B Bytes.

backplane An assembly, typically a printed circuit board, with connectors and signal paths that bus the connector pins.

BIOS Basic Input/Output System—BIOS functions are the fundamental level of any PC or compatible computer. BIOS functions embody the basic operations needed for successful use of the computer's hardware resources.

C

C

Celsius.

cache

Small portion of high-speed memory used for temporary storage of frequently used data.

CMOS

Complementary Metal Oxide Semiconductor—A process used in making chips.

CompactPCI Express

An adaptation of the PCI specification for industrial and/or embedded applications that require a more robust mechanical form factor than desktop PCI. CompactPCI Express provides a standard form factor for those applications requiring the high performance of PCI as well as the small size and ruggedness of a rack-mount system.

D

DC

Direct Current.

DDR

Double Data Rate.

DMA

Direct Memory Access—A method by which data is transferred between devices and internal memory without intervention of the central processing unit.

DVI

Digital Visual Interface—A video connector designed to maximize the visual quality of digital display devices such as flat panel LCD computer displays and digital projectors. It was developed by an industry consortium, the Digital Display Working Group (DDWG).

E

ECP

Extended Capabilities Parallel.

EEPROM

Electrically Erasable Programmable Read Only Memory.

EMC

Electromagnetic Compatibility.

EMI

Electromagnetic interference.

EPP	Enhanced Parallel Port.
expansion ROM	An onboard EEPROM that may contain device-specific initialization and system boot functionality.
F	
FCC	Federal Communications Commission.
G	
g	<ol style="list-style-type: none"> 1. Grams. 2. A measure of acceleration equal to 9.8 m/s².
GPIB	General Purpose Interface Bus (IEEE 488).
g _{rms}	A measure of random vibration—The root mean square of acceleration levels in a random vibration test profile.
H	
Hz	Hertz—Cycles per second.
I	
I/O	Input/Output—The techniques, media, and devices used to achieve communication between machines and users.
IDE	Integrated Drive Electronics—Hard disk and built-in controller.
IEEE	Institute of Electrical and Electronics Engineers.
in.	Inches.
instrument driver	A set of routines designed to control a specific instrument or family of instruments, and any necessary related files for LabWindows/CVI or LabVIEW.
interrupt	A means for a device to request service from another device.
interrupt level	The relative priority at which a device can interrupt.

Glossary

IRQ#	Interrupt signal.
ISA	Industry Standard Architecture—The original PC bus architecture, specifically the 16-bit AT bus.
K	
KB	Kilobytes of memory.
L	
LAN	Local Area Network—Communications network that serves users within a confined geographical area. It is made up of servers, workstations, a network operating system, and a communications link.
LED	Light-emitting diode.
M	
m	Meters.
master	A functional part of a PXI Express device that initiates data transfers on the PXI Express backplane. A transfer can be either a read or a write.
MB	Megabytes of memory.
MTBF	Mean time between failure.
N	
NI-488 or NI-488.2	The National Instruments software for GPIB systems.
NI-DAQ	The National Instruments software for data acquisition instruments.
NI-VISA	The National Instruments implementation of the VISA standard—An interface-independent software that provides a unified programming interface for VXI, GPIB, and serial instruments.

P

PCI	Peripheral Component Interconnect—The PCI bus is a high-performance 32-bit or 64-bit bus with multiplexed address and data lines.
PCMCIA	Personal Computer Memory Card International Association.
peripheral	Any hardware device connected to a computer, such as a monitor, keyboard, printer, plotter, disk or tape drive, graphics tablet, scanner, mouse, and so on.
PXI Express	PCI eXtensions for Instrumentation—An open implementation of CompactPCI Express that adds electrical features that meet the high-performance requirements of instrumentation applications by providing triggering, local buses, and system clock capabilities. PXI Express also offers two-way interoperability with CompactPCI Express products.

R

RAM	Random Access Memory—The computer's primary workspace.
resource	Hardware settings used by devices in a computer system, including ISA interrupt level, DMA channel, and I/O address.
RMS	Root mean squared. <i>See also σ_{rms}.</i>

S

s	Seconds.
SDRAM	Synchronous Dynamic RAM (Random Access Memory)—Storage that the computer must refresh at frequent intervals.
SO-DIMM	Small Outline Dual In-line Memory Module.
SPI Bus	Serial Peripheral Interface—A standard for controlling most any digital electronics that accept a clocked serial stream of bits.

U

USB Universal Serial Bus.

V

V Volts.

VGA Video Graphics Array—The minimum video display standard for all PCs.

W

W Watts.



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