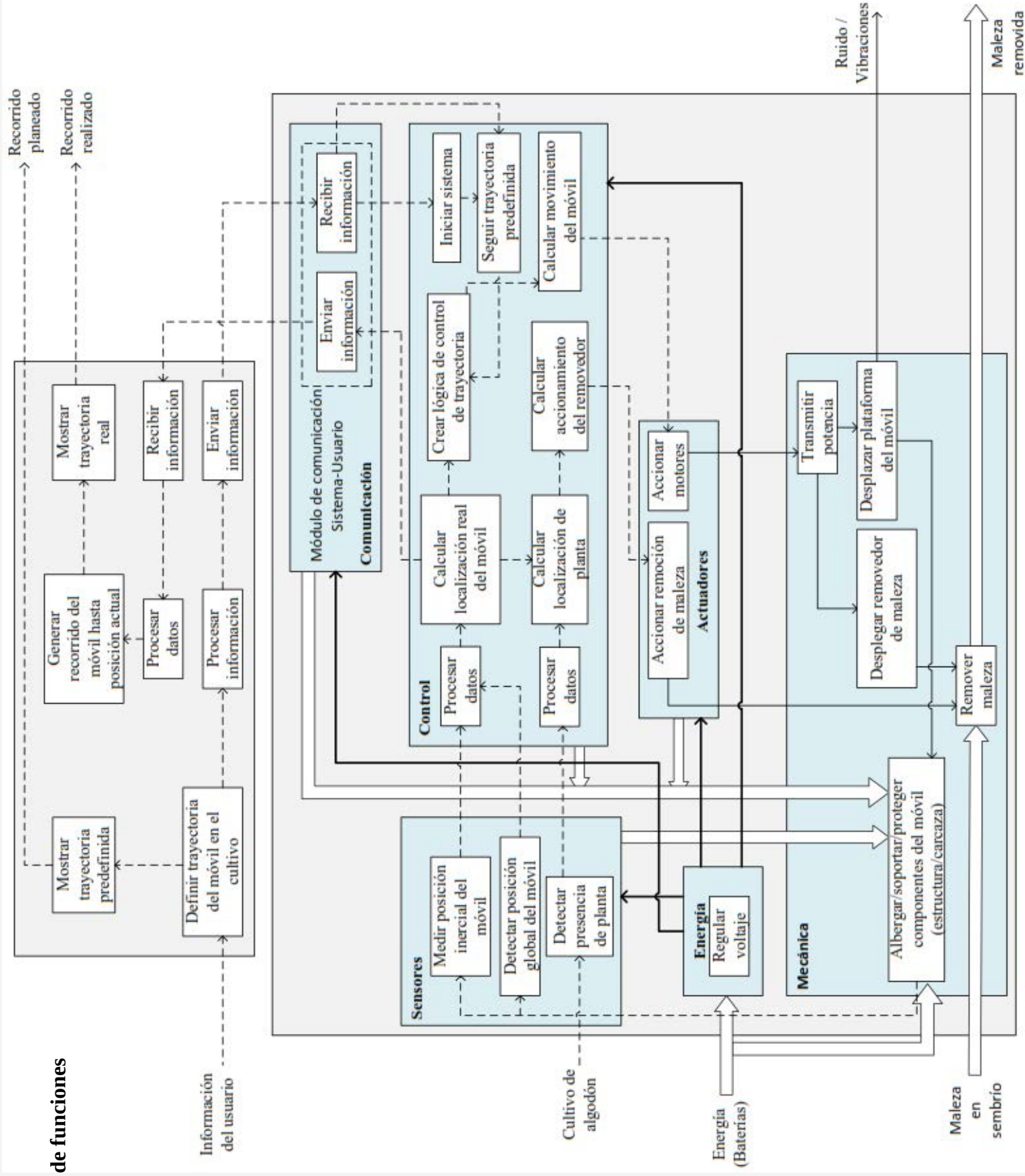


Estructura de funciones



Evaluación técnico – económica

Tabla A.2.
Fuente: Elaboración propia.

EVALUACIÓN DEL PROYECTO VALOR TÉCNICO (Xi)							Área de Diseño			
Proyecto: Diseño de un sistema de control mecánico de maleza en cultivos de algodón										
p: Puntaje de 0 a 4 (Escala de valores VDI2225) 0 = No satisface, 1 = Apenas aceptable, 2 = Suficiente, 3 = Bien, 4 = Excelente (Ideal) g: Peso ponderado en función de la importancia de los criterios de evaluación.										
Criterios de evaluación para diseños en fase de concepto										
Variantes de Concepto			Solución 1		Solución 2		Solución 3		Solución Ideal	
			S1		S2		S3		Sideal	
Nº	Criterio de evaluación	g	p	gp	p	gp	P	gp	p	gp
1	Función principal	4	4	16	4	16	3	12	4	16
2	Operación	4	3	12	3	12	2	8	4	16
3	Control	3	3	9	3	9	2	6	4	12
4	Energía	2	2	4	2	4	3	6	4	8
5	Seguridad	4	3	12	2	8	3	12	4	16
Puntaje máximo Sp ó Sgp			15	53	14	49	13	44	20	68
Valor técnico Xi			0.75	0.779	0.7	0.721	0.65	0.647	1	1

Tabla A.3.
Fuente: Elaboración propia.

EVALUACIÓN DEL PROYECTO VALOR ECONÓMICO (Yi)							Área de Diseño				
Proyecto: Diseño de un sistema de control mecánico de maleza en cultivos de algodón											
p: Puntaje de 0 a 4 (Escala de valores VDI2225) 0 = No satisface, 1 = Apenas aceptable, 2 = Suficiente, 3 = Bien, 4 = Excelente (Ideal) g: Peso ponderado en función de la importancia de los criterios de evaluación.											
Variantes de Concepto			Solución 1		Solución 2		Solución 3		Solución Ideal		
			S1		S2		S3		Sideal		
Nº	Criterio de evaluación		g	p	gp	p	gp	p	gp	p	gp
1	Costo		3	3	9	3	9	2	9	4	12
Puntaje máximo Sp ó Sgp				3	9	3	9	2	6	4	12
Valor económico Yi				0.75	0.75	0.75	0.75	0.5	0.5	1	1

Lista de exigencias

Tabla A.1.
Fuente: Elaboración propia.

LISTA DE EXIGENCIAS		
PROYECTO:	DISEÑO DE UN SISTEMA AUTOMÁTICO DE CONTROL MECÁNICO DE MALEZAS EN CULTIVOS DE ALGODÓN	
CAMBIOS	D/E	REQUERIMIENTOS
		FUNCIÓN PRINCIPAL
04/09/2015	E	Control mecánico de malezas entre plantas en cultivos de algodón sin la ayuda de un operario.
		GEOMETRÍA
06/09/2015	E	Ancho <1.20 m.
	E	Alto >15 cm.
	E	Largo <1.00 m.
	D	Distancia de operación de actuadores flexible.
		CINEMÁTICA
04/09/2015	E	Movimiento a través de hileras de cultivo.
	E	Velocidad máxima: 2 km/h.
		ENERGÍA
04/09/2015	E	Uso de baterías.
	E	Baterías recargables.
	E	Duración de 1.5 horas.
	D	Recarga con luz solar.
		SEGURIDAD
06/09/2015	D	Circuitos eléctricos aislados del usuario.
	D	Apagado de emergencia.
	D	Elementos mecánicos aislados del usuario.
		FABRICACIÓN
04/09/2015	E	Material: Aluminio.
	D	Piezas: Mercado Local.
		ENSAMBLAJE
06/09/2015	D	Sistema desmontable en 2 partes.
		FUERZAS
06/09/2015	E	Peso máximo: 20 kg.
		OPERACIÓN
04/09/2015	E	Sistema autónomo.
	D	Movilización en terrenos no uniformes.
		MANTENIMIENTO
04/09/2015	D	Mínimo cada 5 hectáreas.
		ERGONOMÍA
06/09/2015	D	Transportable por una persona.
	D	Diseño estético.

06/09/2015		ELECTRÓNICA
	E	Circuito de protección de las baterías.
	D	Aislamiento entre circuito de potencia y control.
	D	Sensor de alarma de emergencia.
06/09/2015	E	Movilización vía sensor de visión (cámara).
		CONTROL
	E	Navegación paralela a cada surco.
	E	Giro paralelo hacia siguiente surco.
06/09/2015	E	Movilización vía GPS.
		SEÑALES
	E	Entrada:
	D	Imágenes por cámara.
06/09/2015	E	Comando de usuario.
	E	Salida:
	E	Movimiento.
	E	Planta detectada.
06/09/2015		COSTO
	E	Costo Máximo: 3000 dólares.
06/09/2015		TERRENO
	E	Plantas distribuidas en surcos.
	E	Distancia entre surcos de 120 cm.
	E	Distancia entre plantas de 40 cm.
	E	Malezas con altura entre 0 y 2.5 cm (ya sea hoja ancha o corta).
	E	Plantas con altura entre 0 y 15 cm.
	E	Terreno libre de obstáculos (rocas).
	E	Suelo arenoso y húmedo.

Cálculos electrónicos

B.2.1. Cálculo de consumo de corriente:

- Para la parte de control:

Dado que los pines de Arduino pueden proporcionar hasta 20 mA, para calcular la corriente necesaria se multiplicará la cantidad de pines en ambos Arduinos por la corriente máxima (20 mA).

$$40 \text{ pines} \times 20 \text{ mA} = 0.8 \text{ A.}$$

Para el PandaBoard se sabe que consume alrededor de 1.5 A cuando solo se está usando un puerto USB (el que se comunica con la cámara).

Finalmente, el módulo XBee consume 215 mA de acuerdo a sus especificaciones, el módulo GPS e IMU consumen poca corriente por lo que forman parte de los pines que usa el Arduino.

Corriente total:

$$0.8 + 1.5 + 0.215 = 2.515 \text{ A.}$$

Escogiendo una batería de 5000 mAh, se tiene una autonomía de aproximadamente 2 horas, lo cual cumple con los requerimientos propuestos.

- Para la parte de potencia:

Para calcular la corriente de los actuadores, se hará uso de la conversión de potencia eléctrica a mecánica, por lo que se asumirá un factor de eficiencia de 0.8.

Dynamixel:

Torque: 1 Nm.

Velocidad: $1.047 \text{ rad} / 0.169 \text{ s} = 6.2 \text{ rad/s}$.

Potencia: $T \times \omega = 0.8 \times V \times I$.

$$1 \times 6.2 = 0.8 \times 12 \times I$$

$$I = 0.646 \text{ A.}$$

Como son dos Dynamixel, la corriente es de 1.292 A.

Motor DC:

Torque: 1 Nm.

Velocidad: 7.33 rad/s.

Potencia: $T \times \omega = 0.8 \times V \times I$.

$$1 \times 7.33 = 0.8 \times 12 \times I$$

$$I = 0.763 \text{ A.}$$

Como son cuatro motores, la corriente es de 3.052 A.

Servomotor de la Rueda:

Torque: 0.2 Nm.

Velocidad: $1.047 \text{ rad}/0.17 \text{ s} = 6.16 \text{ rad/s}$.

Potencia: $T \times \omega = 0.8 \times V \times I$.

$$0.22 \times 6.16 = 0.8 \times 6 \times I$$

$$I = 0.282 \text{ A}.$$

Como son cuatro servomotores, la corriente es de 1.13 A.

Corriente total:

$$1.13 + 3.052 + 1.292 = 5.473 \text{ A}.$$

Escogiendo una batería de 12000 mAh, se tiene una autonomía de aproximadamente 2.19 h, lo cual cumple con los requerimientos propuestos.

B.2.2. Cálculo del regulador a 3.3 V (XBee):

Corriente: 215 mA.

Voltaje de salida: 3.3 V.

Inductor:

Del datasheet del integrado LM2576, se obtiene el valor recomendado del inductor.

$$L = 680 \text{ uH @ } 1 \text{ A}.$$

Condensador:

$C_{in} = 100 \text{ uF}$ (por recomendación del fabricante).

$$C_{out} \geq 7.785 \times \frac{V_{in}}{V_{out} \times L} = 7.785 \times \frac{11.1}{3.3 \times 680} = 0.04 \text{ uF}.$$

$$C_{out} = 47 \text{ nF}.$$

Diodo:

$$I_{diodo} = 1.25 \times I_{load-max} = 1.25 \times 0.215 = 0.26875 \text{ A}$$

Diodo Shottky 1 A.

B.2.3. Cálculo del regulador a 5 V (PandaBoard):

Corriente: 1.5 A.

Voltaje de salida: 5 V.

Inductor:

Del datasheet del integrado LM2576, se obtiene el valor recomendado del inductor.

$$L = 150 \text{ uH @ } 2 \text{ A}.$$

Condensador:

$C_{in} = 100 \text{ uF}$ (por recomendación del fabricante).

$$C_{out} \geq 7.785 \times \frac{V_{in}}{V_{out} \times L} = 7.785 \times \frac{11.1}{5 \times 150} = 0.115 \text{ uF}.$$

$$C_{out} = 0.12 \text{ uF}.$$

Diodo:

$$I_{\text{diodo}} = 1.25 \times I_{\text{load-max}} = 1.25 \times 1.5 = 1.875 \text{ A}$$

Diodo Shottky 2 A.

B.2.4. Cálculo del regulador a 12 V (Dynamixel):

Corriente: 0.646 A.

Voltaje de salida: 12 V.

Inductor:

Del datasheet del integrado LM2576, se obtiene el valor recomendado del inductor.

$$L = 680 \text{ uH @ } 1 \text{ A.}$$

Condensador:

Cin = 100 uF (por recomendación del fabricante).

$$C_{\text{out}} \geq 7.785 \times \frac{V_{\text{in}}}{V_{\text{out}} \times L} = 7.785 \times \frac{22.8}{12 \times 680} = 0.022 \text{ uF.}$$

$$C_{\text{out}} = 0.47 \text{ nF.}$$

Diodo:

$$I_{\text{diodo}} = 1.25 \times I_{\text{load-max}} = 1.25 \times 0.646 = 0.8 \text{ A}$$

Diodo Shottky 1 A.

B.2.5. Cálculo del regulador a 12 V (motor DC):

Corriente: 0.763 A.

Voltaje de salida: 12 V.

Inductor:

Del datasheet del integrado LM2576, se obtiene el valor recomendado del inductor.

$$L = 470 \text{ uH @ } 1 \text{ A.}$$

Condensador:

Cin = 100 uF (por recomendación del fabricante).

$$C_{\text{out}} \geq 7.785 \times \frac{V_{\text{in}}}{V_{\text{out}} \times L} = 7.785 \times \frac{22.8}{12 \times 470} = 0.031 \text{ uF.}$$

$$C_{\text{out}} = 47 \text{ nF.}$$

Diodo:

$$I_{\text{diodo}} = 1.25 \times I_{\text{load-max}} = 1.25 \times 0.763 = 0.954 \text{ A}$$

Diodo Shottky 1 A.

B.2.6. Cálculo del regulador a 6 V (servomotores de las ruedas):

Corriente: 0.282 A.

Voltaje de salida: 6 V.

Inductor:

$$E \times T = (V_{\text{in}} - V_{\text{out}}) \times \frac{V_{\text{out}}}{V_{\text{in}}} \times \frac{1000}{52} = (22.8 - 6) \times \frac{6}{22.8} \times \frac{1000}{52} = 85 \text{ Vx}\mu\text{s.}$$

Con el valor de E x T y tablas del datasheet del integrado LM2576, se obtiene el valor recomendado del inductor.

$L = 1000 \text{ uH @ } 1\text{A}.$

Condensador:

$C_{in} = 100 \text{ uF}$ (por recomendación del fabricante).

$$C_{out} \geq 7.785 \times \frac{V_{in}}{V_{out} \times L} = 7.785 \times \frac{22.8}{6 \times 1000} = 0.03 \text{ uF}.$$

$C_{out} = 47 \text{ nF}.$

Diodo:

$$I_{\text{diodo}} = 1.25 \times I_{\text{load-max}} = 1.25 \times 0.282 = 0.35 \text{ A}$$

Diodo Shottky 1 A.

Resistencias:

$$V_{out} = 1.23 \times (1 + \frac{R_2}{R_1}).$$

$$R_1 = 1 \text{ k}\Omega.$$

$$6 = 1.23 \times (1 + \frac{R_2}{1}).$$

$$R_2 = 3.878.$$

Se escoge $R_2 = 3.9 \text{ k}\Omega.$

B.2.7. Cálculo de disipación de potencia de los reguladores:

Del datasheet (se asumirá temperatura ambiente de 25°C):

Temperatura máxima de operación: 125°C

Resistencia térmica juntura ambiente (R_{ja}): 45°C/W

Resistencia térmica juntura carcasa (R_{jc}): 2°C/W

Regulador a 3.3 V (Xbee):

$$P_{\text{disipada}} = (V_{in} - V_{out}) \times I = (11.1 - 3.3) \times 0.215 = 1.677 \text{ W}$$

Temp. de trabajo = $R_{ja} \times P_{\text{disipada}} + T_{amb} = 45 \times 1.677 + 25 = 100.5^\circ\text{C}$ (No supera T_{max} , no necesita disipador)

Regulador a 5 V (PandaBoard):

$$P_{\text{disipada}} = (V_{in} - V_{out}) \times I = (11.1 - 5) \times 1.5 = 9.15 \text{ W}$$

Temp. de trabajo = $R_{ja} \times P_{\text{disipada}} + T_{amb} = 45 \times 9.15 + 25 = 436.75^\circ\text{C}$ (Supera T_{max} , necesita disipador)

Resistencia térmica de disipador = $(T_{max} - T_{amb}) / P_{\text{disipada}} - R_{jc} = 100 / 9.15 - 2 = 8.8^\circ\text{C/W}$ (Se redondea hacia un valor comercial inferior por precaución).

Regulador a 12 V (Dynamixel):

$$P_{\text{disipada}} = (V_{in} - V_{out}) \times I = (22.8 - 12) \times 0.646 = 7 \text{ W (aproximadamente)}$$

Temp. de trabajo = $R_{ja} \times P_{\text{disipada}} + T_{amb} = 45 \times 7 + 25 = 340^\circ\text{C}$ (Supera T_{max} , necesita disipador)

Resistencia térmica de disipador = $(T_{max} - T_{amb}) / P_{\text{disipada}} - R_{jc} = 100 / 7 - 2 = 12^\circ\text{C/W}$ (Se redondea hacia un valor comercial inferior por precaución).

Regulador a 12 V (Motores DC):

$$P_{\text{disipada}} = (V_{in} - V_{out}) \times I = (22.8 - 12) \times 0.763 = 8.24 \text{ W}$$

Temp. de trabajo = $R_{ja} \times P_{\text{disipada}} + T_{amb} = 45 \times 8.24 + 25 = 395.8^\circ\text{C}$ (Supera T_{max} , necesita disipador)

Resistencia térmica de disipador = $(T_{\text{max}} - T_{\text{amb}})/P_{\text{disipada}} - R_{\text{jc}} = 100/8.24 - 2 = 10^{\circ}\text{C/W}$ (Se redondea hacia un valor comercial inferior por precaución).

Regulador a 6 V (Servomotores de ruedas):

$P_{\text{disipada}} = (V_{\text{in}} - V_{\text{out}}) * I = (22.8 - 6) * 0.282 = 4.74 \text{ W}$ (aproximadamente)

Temp. de trabajo = $R_{\text{ja}} * P_{\text{disipada}} + T_{\text{amb}} = 45 * 4.74 + 25 = 238.3^{\circ}\text{C}$ (Supera T_{max} , necesita disipador)

Resistencia térmica de disipador = $(T_{\text{max}} - T_{\text{amb}})/P_{\text{disipada}} - R_{\text{jc}} = 100/4.74 - 2 = 18^{\circ}\text{C/W}$ (Se redondea hacia un valor comercial inferior por precaución).



Cálculos mecánicos

B.1.1. Resistencia de la viga:

Las ruedas se acoplan a ambos extremos de una viga de tubo cuadrado y pared delgada, Para simplificar los cálculos de resistencia, se asumen fuerzas puntuales en la viga.

Asimismo, el peso del chasis y los componentes que soportan las vigas es de 6.6 kg, pero asumiendo un factor de seguridad de 1.5, se tiene una carga de 10 kg aproximadamente.

Masa del chasis: 10 kg

Material del tubo: Aluminio

Densidad: 2700 kg/m^3

Resistencia a la fluencia: 240 MPa

Esfuerzo máximo de corte: 140 MPa

Módulo de elasticidad: 69 GPa

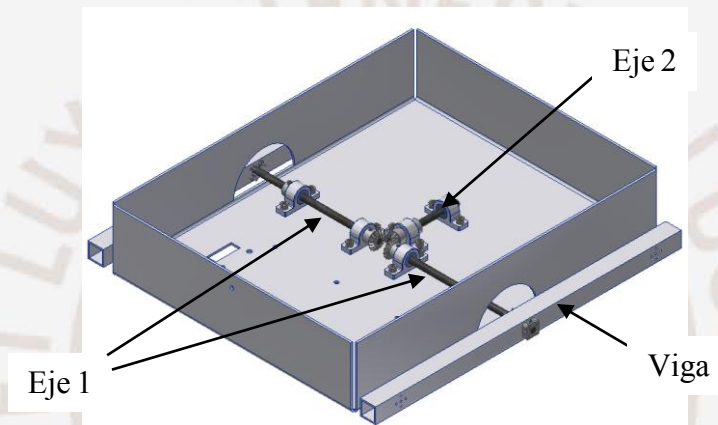


Figura B.1.
Fuente: Elaboración propia.

Se analiza solo una viga, por lo que se considera solo la mitad de la carga (49.05 N), equivalente a 5 kg.

DCL:

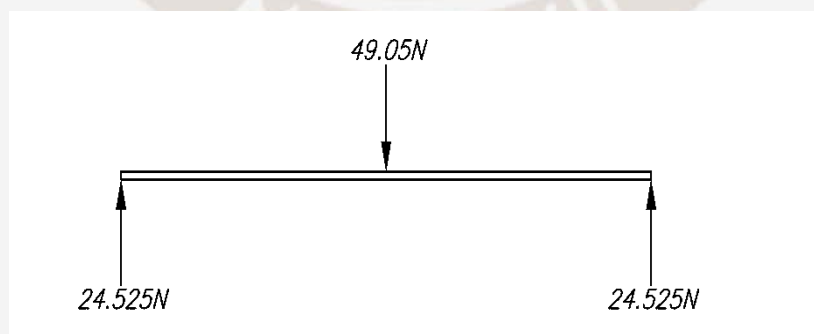


Figura B.2.
Fuente: Elaboración propia.

DFC:

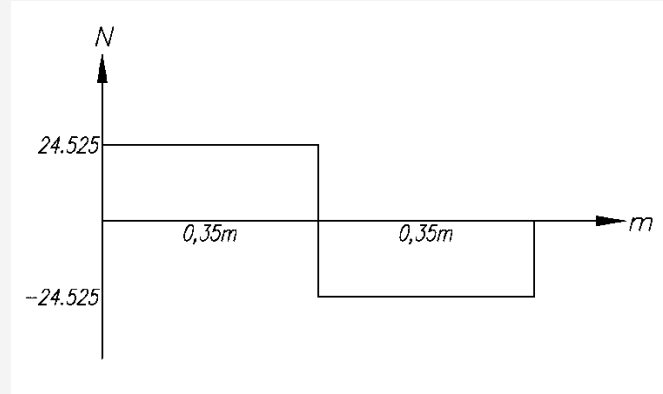


Figura B.3.
Fuente: Elaboración propia.

DMF:

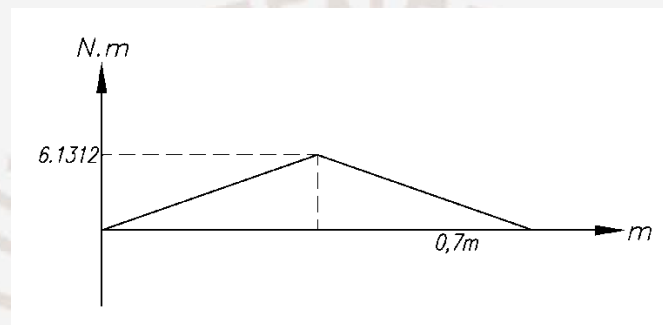


Figura B.4.
Fuente: Elaboración propia.

Con el diagrama de fuerza cortante (ver figura B.3) y el diagrama de momento flector (ver figura B.4) se tiene la fuerza y el momento (así como la distancia) crítico a la que va estar sometida la viga.

- Resistencia por flexión de la viga:

$$\text{Esfuerzo} = \frac{M}{S}$$

Donde: M: Momento flector.

$$S_{\min} = \frac{M_{\max}}{\text{Esfuerzo}}$$

S: Módulo de sección

$$S_{\min} = \frac{6.1312 \text{ Nm}}{240\,000\,000 \text{ N/m}^2} = 0.026 \text{ cm}^3$$

Smin: Módulo de sección mínimo

Mmax: Momento flector máximo

Sección viga:

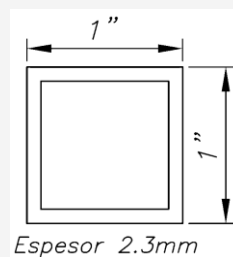


Figura B.5.
Fuente: Elaboración propia.

$$S = \frac{C^4 - C'^4}{C} = 9.018 \text{ cm}^3 \quad (\text{Cumple con el mínimo hallado, no falla por flexión}).$$

Donde:

c: lado externo (1 pulgada).

c': lado interno (lado externo menos dos veces el espesor).

- Resistencia al esfuerzo de corte de la viga:

Como la viga es de pared delgada, para hallar el esfuerzo cortante, se simplifica a:

$$\tau = \frac{2V}{A} = \frac{2 \times 49.05}{2.1252 \times 10^{-4}} = 461.6 \text{ KPa} \text{ (Menor a 140 MPa, no falla por esfuerzo cortante).}$$

B.1.2. Resistencia del eje 1:

Para verificar que el eje soporte las cargas se analiza su DCL, donde el momento torsor de 6.1312 Nm y la fuerza de 49.05 N en el extremo derecho provienen como reacciones de la viga ya analizada. Este momento torsor se transmitirá con igual magnitud a los demás ejes debido a que los engranajes cónicos presentan igual diámetro y número de dientes.

DCL:

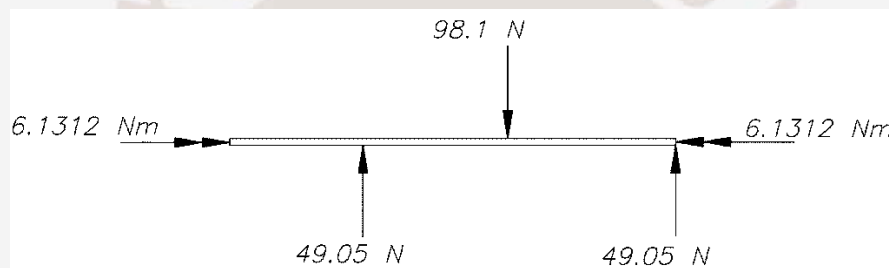


Figura B.6.

Fuente: Elaboración propia.

A partir del DCL, se obtienen los diagramas de fuerza cortante y momento flector.

DFC:

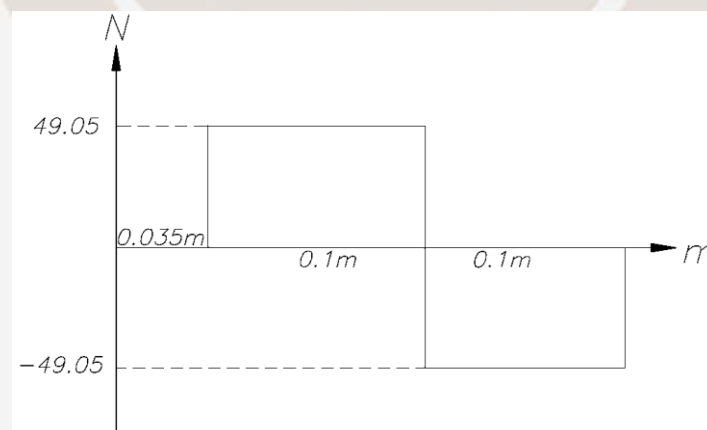


Figura B.7.

Fuente: Elaboración propia.

DMF:

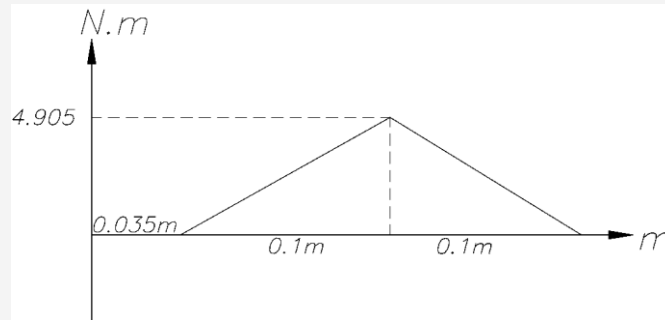


Figura B.8.
Fuente: Elaboración propia.

- Resistencia por flexión del eje 1:

Se recuerda que el eje es de acero estructural, por lo que:

Resistencia a la fluencia: 250 MPa

$$\text{Esfuerzo} = \frac{M}{S}$$

Donde: M: Momento flector.

$$S_{\min} = \frac{M_{\max}}{\text{Esfuerzo}}$$

S: Módulo de sección

$$S_{\min} = \frac{4.905 \text{ Nm}}{250\,000\,000 \text{ N/m}^2} = 0.0196 \text{ cm}^3.$$

Smin: Módulo de sección mínimo

Mmax: Momento flector máximo

Sección del eje:

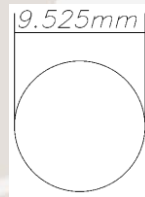


Figura B.9.
Fuente: Elaboración propia.

$$S = 0.0982d^3 = 0.0848 \text{ cm}^3 \quad (\text{Cumple con el mínimo hallado, no falla por flexión}).$$

Donde:

d: diámetro del eje.

B.1.3. Resistencia del eje 2:

El momento torsor del eje 1 se transmite a través de una fuerza en el engranaje cónico del eje 2. Esta fuerza se compensa con la reacción que ejerce el engranaje cónico del otro eje 1 (ver figura B.10), por lo que el eje 2 solo estaría soportando la carga de su propio peso (ver figura B.11). El eje no falla por flexión.

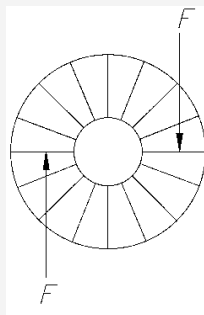


Figura B.10.
Fuente: Elaboración propia.

Se verifica en el DCL que el eje 2 solo soporta su propio peso (R_1 y R_2 son las reacciones provenientes de las chumaceras y W es el peso del eje).

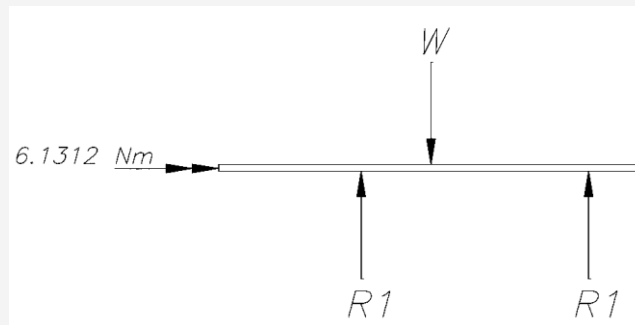


Figura B.11.
Fuente: Elaboración propia.

B.1.4. Cálculo de torque del motor:

Si se tienen los siguientes datos:

Velocidad deseada: 0.55 m/s (2 km/h)

Radio de rueda: 7.5 cm

La velocidad angular deseada será:

$$\omega = \frac{0.55}{0.075} = 7.33 \times 60 \times \frac{1}{2\pi} = 70 \text{ rpm.}$$

Se asume un coeficiente de fricción del suelo:

$$\mu = 0.5.$$

Entonces la fuerza de fricción:

$$F_f = \mu \times N = 0.5 \times 24.525 = 12.2625 \text{ N.}$$

Cabe recordar que la reacción N se calculó durante el análisis de resistencia de la viga.

Para la inercia de la rueda se asume como anillo para tomar el peor de los casos.

$$I = MR^2 = 1 \times 0.075^2 = 5.625 \times 10^{-3} \text{ kg. m}^2.$$

Entonces el torque necesario será (se asume $\alpha = 7.33 \frac{\text{rad}}{\text{s}^2}$):

$$T = I \times \alpha + r \times F_f = 5.625 \times 10^{-3} \times 7.33 + 0.075 \times 12.2625 = 0.96 \text{ Nm.}$$

Potencia:

$$P = T \times \omega = 0.96 \times 7.33 = 7.044 \text{ W.}$$

B.1.5. Cálculo de torque del servomotor:

Para calcular el torque necesario se usó la siguiente fórmula:

$$T = W_u \sqrt{\frac{B^2}{8} + E^2}.$$

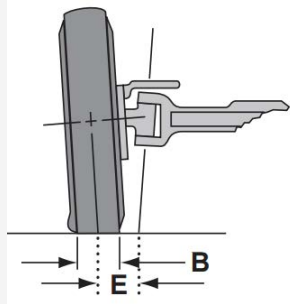


Figura B.5. Rueda vista de sección.

Fuente: <http://www.brevini.co.nz/wp-content/uploads/calculators/PowerSteeringCalc.pdf>.

Donde:

T: torque del servomotor.

W: peso sobre la rueda.

u: coeficiente de fricción.

B: ancho de la rueda.

E: offset del centro de la rueda con el punto de aplicación de torque.

Se sabe que el peso sobre la rueda es de 24.525 N (calculada anteriormente) y que el “offset” es cero debido a que el servomotor se encuentra sobre la rueda. Se asume un coeficiente de fricción de 1 para tomar el peor de los casos; asimismo, el ancho de la rueda es de 1 pulgada.

$$T = 24.525 \times 1 \sqrt{\frac{0.0254^2}{8} + 0^2} = 0.22 \text{ Nm.}$$

B.1.6. Cálculo de torque del servomotor del removedor:

A pesar que el disco removedor va a girar libremente por el suelo, se asumirá que está fijo y que el servomotor debe soportar la reacción del suelo. Para esto se emplea la siguiente fórmula [18]:

$$F_t = a \cdot b \left(13,30 \cdot \gamma \cdot a + 3,06 \cdot \gamma \cdot \frac{v^2}{g} \right),$$

Donde:

γ : densidad del suelo (kg/m^3).

a: profundidad de la herramienta (m).

b: ancho de la herramienta (m).

v: velocidad de la herramienta (m/s).

g: gravedad (m/s^2).

F_t : fuerza en daN.

Dadas las condiciones del suelo se asumirá una densidad de 1290 kg/m^3 , la profundidad de trabajo es de 0.04 m, el ancho del disco es de 0.015 m y la velocidad es de 0.55 m/s.

$$F_t = 0.04 \times 0.015 \times \left(13,30 \times 1290 \times 0.04 + 3,06 \times 1290 \times \frac{0.55^2}{9.81} \right) = 0.4848 \text{ daN}$$

$$= 4.848 \text{ N.}$$

Con la distancia de 4 cm de profundidad y de 20 cm del suelo al chasis del móvil se tiene 24 cm de distancia a la fuerza calculada. Lo que genera un torque de 1.16 Nm, el cual debe soportar el servomotor.

Lista de planos

Tabla B.1. Lista de planos.
Fuente: Elaboración propia.

Planos Mecánicos		
Número	Sobre	Nombre
L1 – A0	1	Ensamble general del sistema removedor de malezas
L2 – A2	2	Chasis con mecanismo diferencial
L3 – A1	3	Subsistema rueda
L4 – A1	4	Removedor completo
L5 – A2	5	Subsistema removedor
L6 – A1	6	Chasis
L7 – A2	7	Placa de unión rueda con servo
L8 – A3	8	Brida
L9 – A3	9	Cubo de unión con eje
L10 – A3	10	Disco removedor
L11 – A3	11	Eje corto del diferencial
L12 – A3	12	Eje de disco removedor
L13 – A3	13	Eje de mecanismo diferencial
L14 – A3	14	Eje removedor
L15 – A3	15	Placa de unión removedor con chasis
L16 – A3	16	Placa de unión servo con viga
L17 – A3	17	Placa soporte de disco removedor
L18 – A3	18	Placa soporte de servo
L19 – A3	19	Placa soporte
L20 – A3	20	Viga
Planos Eléctricos		
Número	Sobre	Nombre
L1 - A2	21	Diagrama General
L2 - A3	22	Reguladores de Voltaje

SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

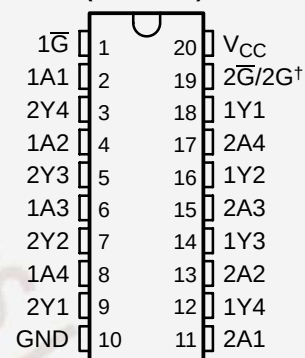
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- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- Hysteresis at Inputs Improves Noise Margins

description

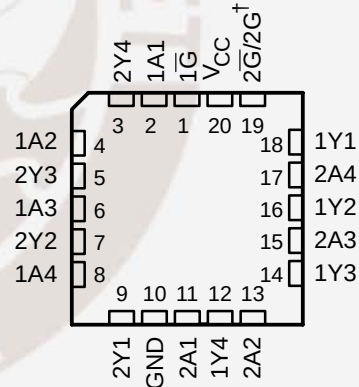
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical, active-low output-control ($\overline{G}$) inputs, and complementary output-control (G and $\overline{G}$) inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise margin. The SN74LS' and SN74S' devices can be used to drive terminated lines down to 133 Ω .

SN54LS', SN54S' ... J OR W PACKAGE
SN74LS240, SN74LS244 ... DB, DW, N, OR NS PACKAGE
SN74LS241 ... DW, N, OR NS PACKAGE
SN74S' ... DW OR N PACKAGE
(TOP VIEW)



† 2G for 'LS241 and 'S241 or 2 $\overline{G}$ for all other drivers.

SN54LS', SN54S' ... FK PACKAGE
(TOP VIEW)



† 2G for 'LS241 and 'S241 or 2 $\overline{G}$ for all other drivers.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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ORDERING INFORMATION[†]

T_A	PACKAGE[‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS240N	SN74LS240N
			SN74LS241N	SN74LS241N
			SN74LS244N	SN74LS244N
			SN74S240N	SN74S240N
			SN74S241N	SN74S241N
			SN74S244N	SN74S244N
	SOIC – DW	Tube	SN74LS240DW	LS240
		Tape and reel	SN74LS240DWR	
		Tube	SN74LS241DW	LS241
		Tape and reel	SN74LS241DWR	
		Tube	SN74LS244DW	LS244
		Tape and reel	SN74LS244DWR	
		Tube	SN74S240DW	S240
		Tape and reel	SN74S240DWR	
		Tube	SN74S241DW	S241
		Tape and reel	SN74S241DWR	
		Tube	SN74S244DW	S244
		Tape and reel	SN74S244DWR	
	SOP – NS	Tape and reel	SN74LS240NSR	74LS240
			SN74LS241NSR	74LS241
			SN74LS244NSR	74LS244
	SSOP – DB	Tape and reel	SN74LS240DBR	LS240
			SN74LS244DBR	LS244

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

[‡] Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



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**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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ORDERING INFORMATION[†] (CONTINUED)

T_A	PACKAGE[‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CDIP – J	Tube	SN54LS240J	SN54LS240J
			SNJ54LS240J	SNJ54LS240J
			SN54LS241J	SN54LS241J
			SNJ54LS241J	SNJ54LS241J
			SN54LS244J	SN54LS244J
			SNJ54LS244J	SNJ54LS244J
			SN54S240J	SN54S240J
			SNJ54S240J	SNJ54S240J
			SN54S241J	SN54S241J
			SNJ54S241J	SNJ54S241J
			SN54S244J	SN54S244J
			SNJ54S244J	SNJ54S244J
	CFP – W	Tube	SNJ54LS240W	SNJ54LS240W
			SNJ54LS241W	SNJ54LS241W
			SNJ54LS244W	SNJ54LS244W
			SNJ54S240W	SNJ54S240W
			SNJ54S241W	SNJ54S241W
			SNJ54S244W	SNJ54S244W
	LCCC – FK	Tube	SNJ54LS240FK	SNJ54LS240FK
			SNJ54LS241FK	SNJ54LS241FK
			SNJ54LS244FK	SNJ54LS244FK
			SNJ54S240FK	SNJ54S240FK
			SNJ54S241FK	SNJ54S241FK
			SNJ54S244FK	SNJ54S244FK

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

[‡] Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



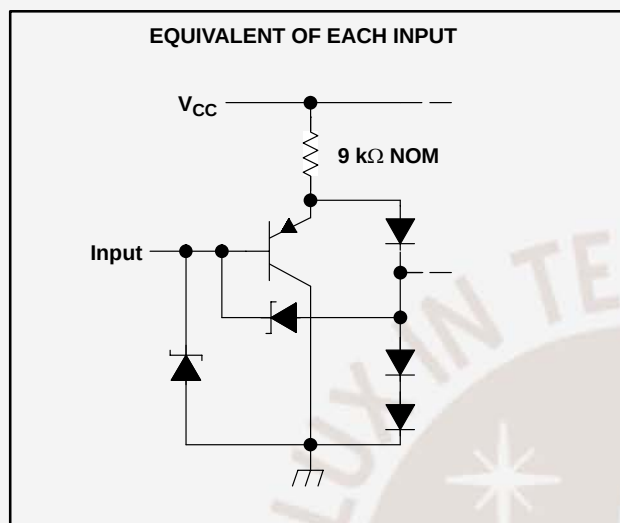
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SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

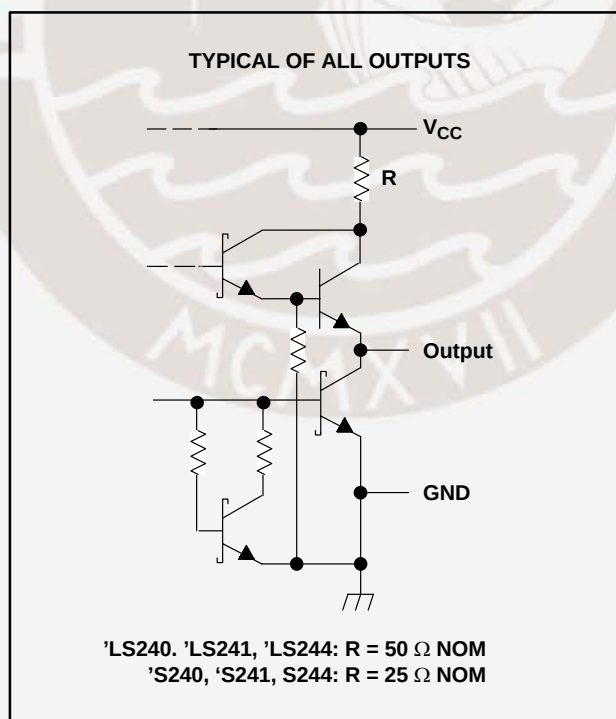
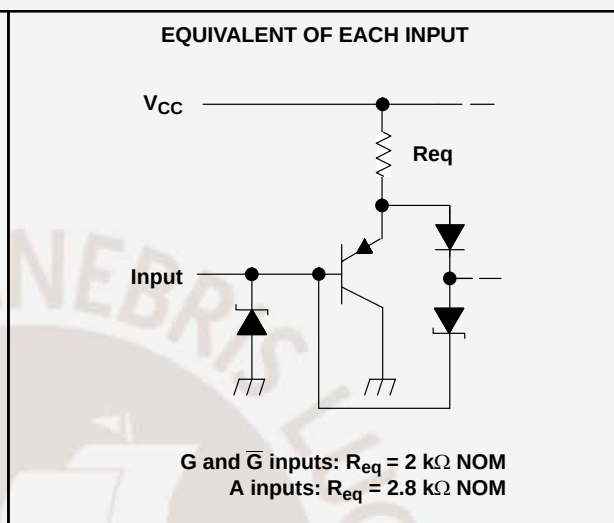
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schematics of inputs and outputs

'LS240, 'LS241, 'LS244



'S240, 'S241, 'S244



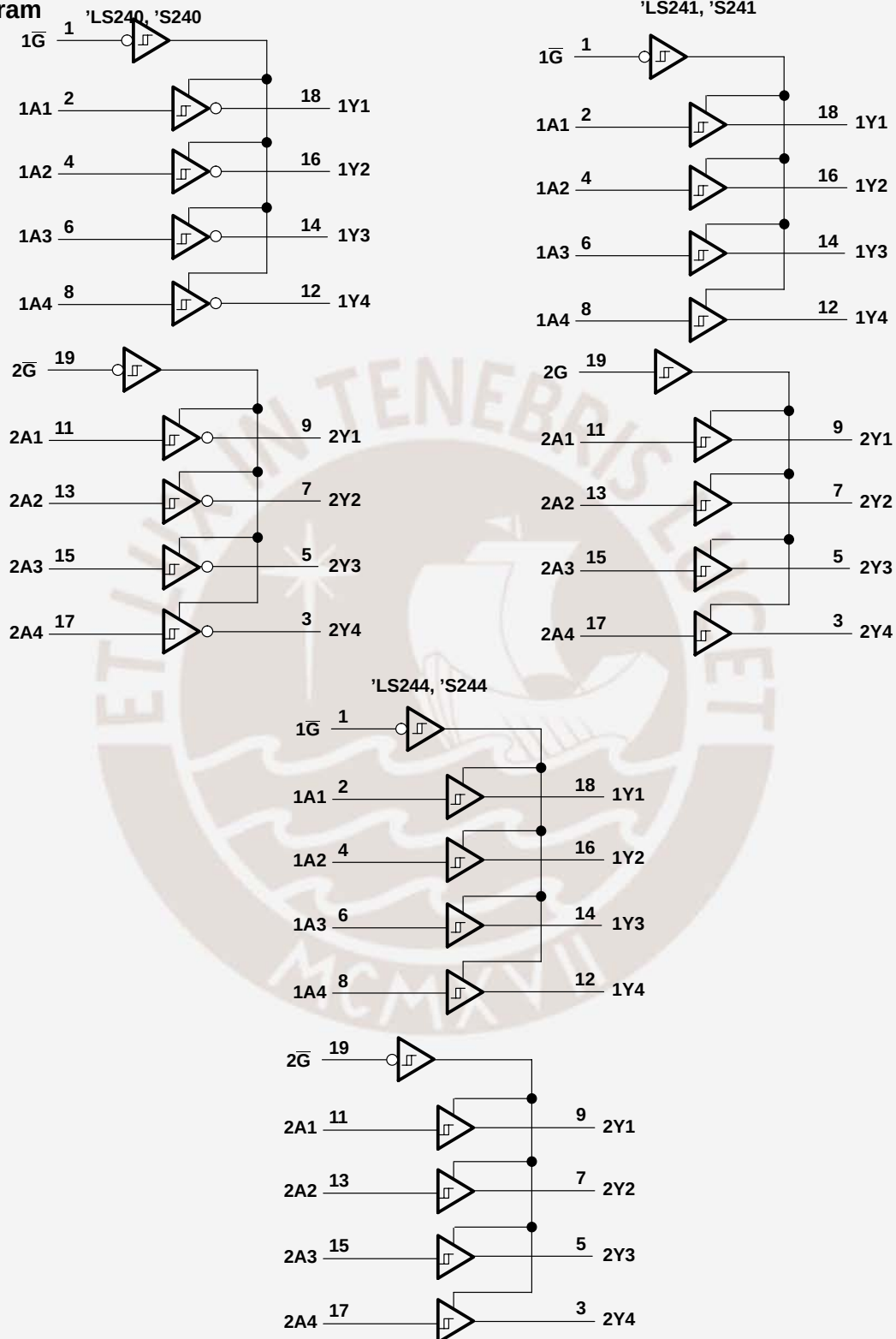
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**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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logic diagram



Pin numbers shown are for DB, DW, J, N, NS, and W packages.



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SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244 **SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244** **OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I : 'LS	7 V
'S	5.5 V
Off-state output voltage	5.5 V
Package thermal impedance, θ_{JA} (see Note 2): DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			–12			–15	mA
I_{OL} Low-level output current			12			24	mA
T_A Operating free-air temperature	–55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.



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**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]			SN54LS [†]			SN74LS [†]			UNIT
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = \text{MIN},$ $I_I = -18 \text{ mA}$					-1.5			-1.5	V
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$			0.2	0.4		0.2	0.4		V
V_{OH}	$V_{CC} = \text{MIN},$ $I_{OH} = -3 \text{ mA}$	$V_{IH} = 2 \text{ V},$	$V_{IL} = \text{MAX},$	2.4	3.4		2.4	3.4		V
	$V_{CC} = \text{MIN},$ $I_{OH} = \text{MAX}$	$V_{IH} = 2 \text{ V},$	$V_{IL} = 0.5 \text{ V},$	2			2			
V_{OL}	$V_{CC} = \text{MIN},$ $V_{IL} = \text{MAX}$	$V_{IH} = 2 \text{ V},$	$I_{OL} = 12 \text{ mA}$			0.4			0.4	V
			$I_{OL} = 24 \text{ mA}$						0.5	
I_{OZH}	$V_{CC} = \text{MAX},$ $V_{IL} = \text{MAX}$	$V_{IH} = 2 \text{ V},$	$V_O = 2.7 \text{ V}$			20			20	μA
I_{OZL}	$V_{CC} = \text{MAX},$ $V_{IL} = \text{MAX}$	$V_{IH} = 2 \text{ V},$	$V_O = 0.4 \text{ V}$			-20			-20	μA
I_I	$V_{CC} = \text{MAX},$	$V_I = 7 \text{ V}$				0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX},$	$V_I = 2.7 \text{ V}$				20			20	μA
I_{IL}	$V_{CC} = \text{MAX},$	$V_{IL} = 0.4 \text{ V}$				-0.2			-0.2	mA
$I_{OS}^{\S}$	$V_{CC} = \text{MAX},$			-40		-225	-40		-225	mA
I_{CC}	$V_{CC} = \text{MAX},$ Output open	Outputs high	All			17			17	mA
		Outputs low	'LS240			26			26	
			'LS241, 'LS244			27			27	
		Outputs disabled	'LS240			29			29	
			'LS241, 'LS244			32			32	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see Figure 1)

PARAMETER	TEST CONDITIONS		'LS240			'LS241, 'LS244			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	$R_L = 667 \Omega,$	$C_L = 45 \text{ pF}$		9	14		12	18	ns
t_{PHL}				12	18		12	18	
t_{PZL}	$R_L = 667 \Omega,$	$C_L = 45 \text{ pF}$		20	30		20	30	ns
t_{PZH}				15	23		15	23	
t_{PLZ}	$R_L = 667 \Omega,$	$C_L = 5 \text{ pF}$		10	20		10	20	ns
t_{PHZ}				15	25		15	25	



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SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions

		SN54S'			SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-12			-15	mA
I _{OL}	Low-level output current			48			64	mA
	External resistance between any input and V _{CC} or ground			40			40	kΩ
T _A	Operating free-air temperature (see Note 3)	-55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.

3. An SN54S241J operating at free-air temperature above 116°C requires a heat sink that provides a thermal resistance from case to free air, R_{θCA}, of not more than 40°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54S'		SN74S'		UNIT
				MIN	TYP‡	MAX	MIN	
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.2		-1.2		V
Hysteresis (V _{T+} - V _{T-})	V _{CC} = MIN			0.2	0.4	0.2	0.4	V
V _{OH}	V _{CC} = MIN I _{OH} = -1 mA	V _{IH} = 2 V,	V _{IL} = 0.8 V,			2.7		V
	V _{CC} = MIN, I _{OH} = -3 mA	V _{IH} = 2 V,	V _{IL} = 0.8 V,	2.4	3.4	2.4	3.4	
	V _{CC} = MIN, I _{OH} = MAX	V _{IH} = 2 V,	V _{IL} = 0.5 V,	2		2		
V _{OL}	V _{CC} = MIN, I _{OL} = MAX	V _{IH} = 2 V,	V _{IL} = 0.8 V,	0.55		0.55		V
I _{OZH}	V _{CC} = MAX, V _{IL} = 0.8 V	V _{IH} = 2 V,	V _O = 2.4 V	50		50		μA
I _{OZL}	V _{CC} = MAX, V _{IL} = 0.8 V	V _{IH} = 2 V,	V _O = 0.5 V	-50		-50		μA
I _I	V _{CC} = MAX,	V _I = 5.5 V		1		1		mA
I _{IH}	V _{CC} = MAX,	V _I = 2.7 V		50		50		μA
I _{IL}	V _{CC} = MAX,	V _I = 0.5 V	Any A	-400		-400		μA
			Any G	-2		-2		mA
I _{OS} §	V _{CC} = MAX			-50	-225	-50	-225	mA
I _{CC}	V _{CC} = MAX, Output open	Outputs high	'S240	80	123	80	135	mA
			'S241, 'S244	95	147	95	160	
		Outputs low	'S240	100	145	100	150	
			'S241, 'S244	120	170	120	180	
		Outputs disabled	'S240	100	145	100	150	
			'S241, 'S244	120	170	120	180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.



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**SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS**

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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 2)

PARAMETER	TEST CONDITIONS	'S240			'S241, 'S244			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	$R_L = 90\ \Omega$, $C_L = 50\text{ pF}$		4.5	7		6	9	ns
t_{PHL}			4.5	7		6	9	
t_{PZL}	$R_L = 90\ \Omega$, $C_L = 50\text{ pF}$		10	15		10	15	ns
t_{PZH}			6.5	10		8	12	
t_{PLZ}	$R_L = 90\ \Omega$, $C_L = 5\text{ pF}$		10	15		10	15	ns
t_{PHZ}			6	9		6	9	

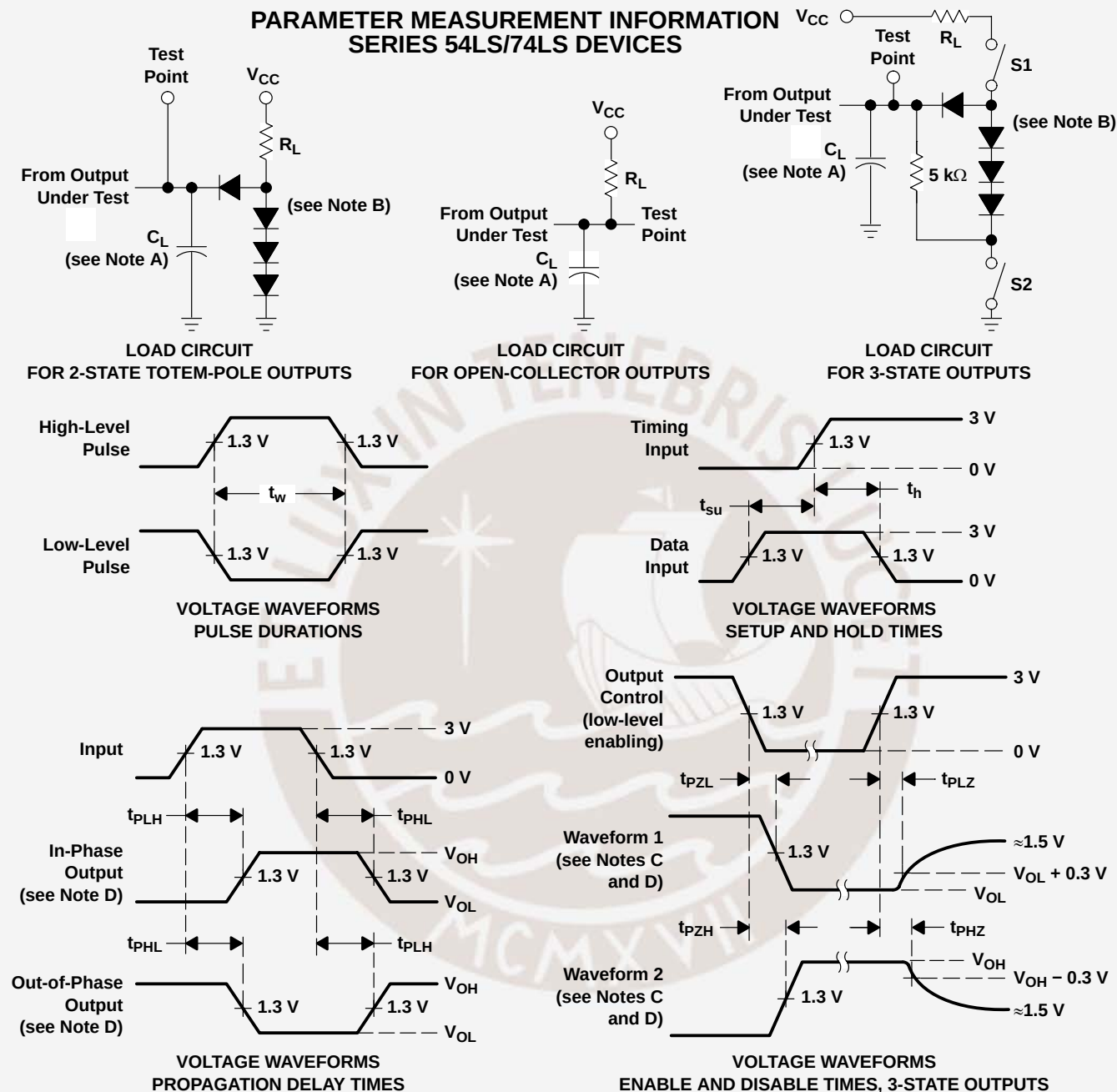


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SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION SERIES 54LS/74LS DEVICES

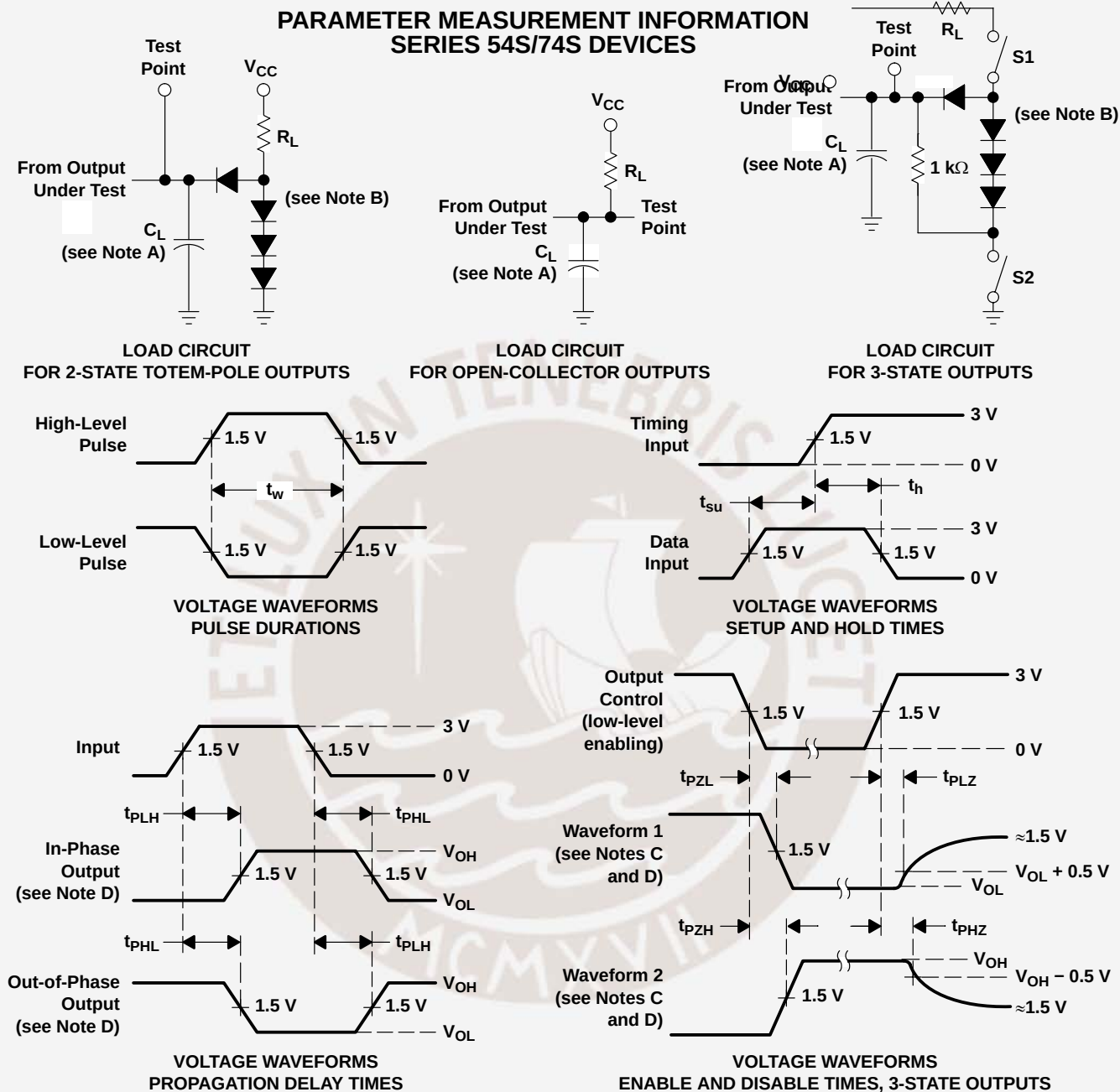


- NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
G. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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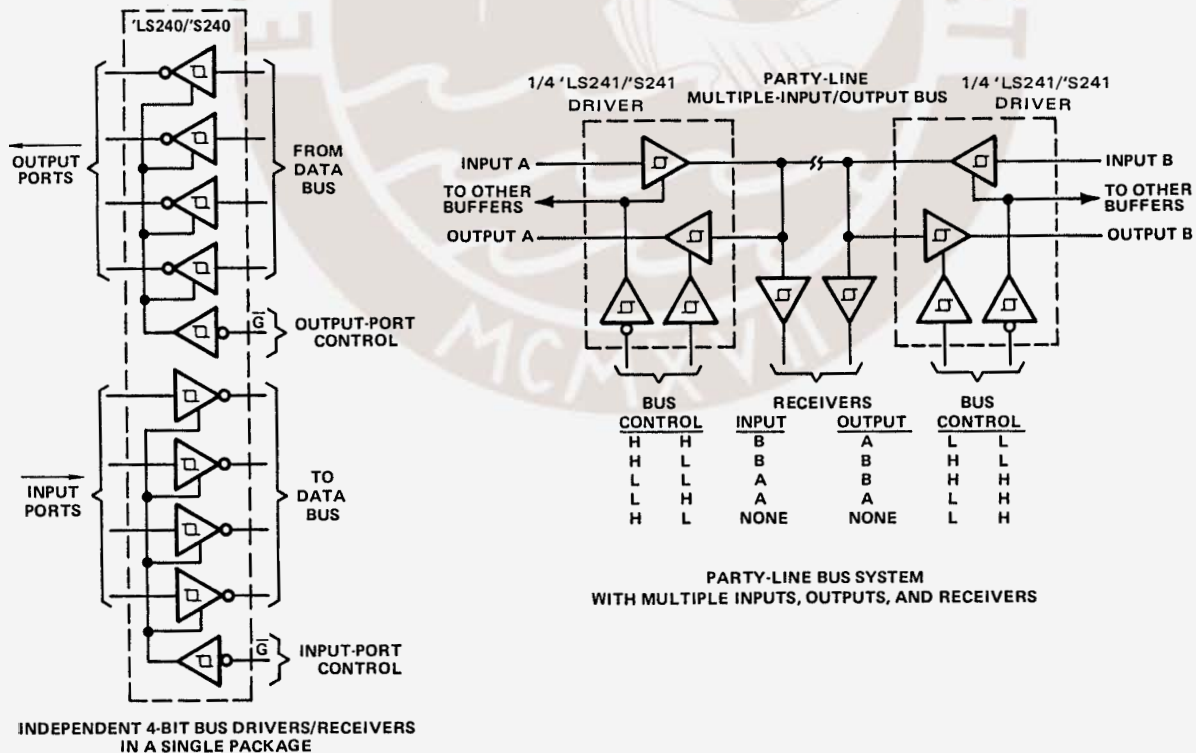
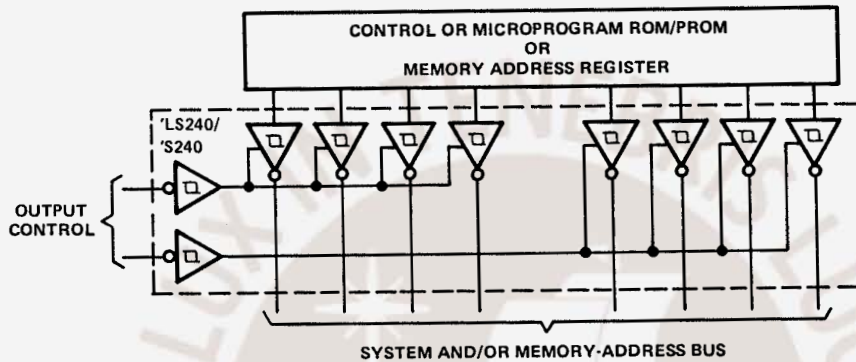
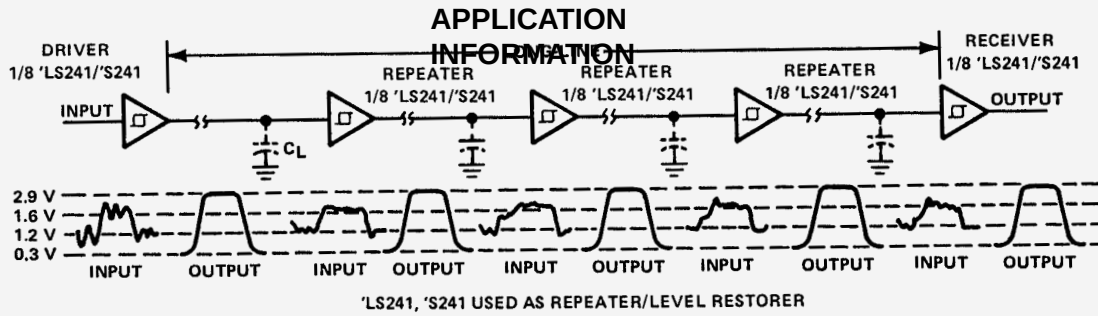
- NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
E. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$; t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
F. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244 SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S244 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SDLS144C -

APRIL 1985 - REVISED MAY 2010



PACKAGE OPTION ADDENDUM



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-7801201VRA	ACTIVE	CDIP	J	20	20	TBD	A42	N / A for Pkg Type	-55 to 125	5962-7801201VR A SNV54LS240J	Samples
5962-7801201VSA	ACTIVE	CFP	W	20	25	TBD	A42	N / A for Pkg Type	-55 to 125	5962-7801201VS A SNV54LS240W	Samples
7705701RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7705701RA SNJ54LS244J	Samples
7705701SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7705701SA SNJ54LS244W	Samples
78012012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	78012012A SNJ54LS 240FK	Samples
7801201RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7801201RA SNJ54LS240J	Samples
7801201SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7801201SA SNJ54LS240W	Samples
JM38510/32401B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32401B2A	Samples
JM38510/32401BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32401BRA	Samples
JM38510/32401BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32401BSA	Samples
JM38510/32402B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32402B2A	Samples
JM38510/32402BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32402BRA	Samples
JM38510/32402BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32402BSA	Samples
JM38510/32403B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32403B2A	Samples
JM38510/32403BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32403BRA	Samples
JM38510/32403BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32403BSA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/32403SRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32403SRA	Samples
JM38510/32403SSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32403SSA	Samples
M38510/32401B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32401B2A	Samples
M38510/32401BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32401BRA	Samples
M38510/32401BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32401BSA	Samples
M38510/32402B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32402B2A	Samples
M38510/32402BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32402BRA	Samples
M38510/32402BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32402BSA	Samples
M38510/32403B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32403B2A	Samples
M38510/32403BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32403BRA	Samples
M38510/32403BSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32403BSA	Samples
M38510/32403SRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32403SRA	Samples
M38510/32403SSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32403SSA	Samples
SN54LS240J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS240J	Samples
SN54LS241J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS241J	Samples
SN54LS244J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS244J	Samples
SN54S240J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S240J	Samples
SN54S241J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S241J	Samples
SN54S244J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S244J	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS240DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS240	Samples
SN74LS240DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS240	Samples
SN74LS240DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS240	Samples
SN74LS240DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS240	Samples
SN74LS240DWRG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		Samples
SN74LS240J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	0 to 70		
SN74LS240N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS240N	Samples
SN74LS240N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74LS240NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS240N	Samples
SN74LS240NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS240	Samples
SN74LS240NSRE4	ACTIVE	SO	NS	20		TBD	Call TI	Call TI	0 to 70		Samples
SN74LS240NSRG4	ACTIVE	SO	NS	20		TBD	Call TI	Call TI	0 to 70		Samples
SN74LS241DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS241	Samples
SN74LS241DWE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		Samples
SN74LS241DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS241	Samples
SN74LS241DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS241	Samples
SN74LS241DWRE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		Samples
SN74LS241DWRG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		Samples
SN74LS241J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	0 to 70		
SN74LS241N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS241N	Samples
SN74LS241N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS241NE4	ACTIVE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		Samples
SN74LS241NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS241	Samples
SN74LS241NSRE4	ACTIVE	SO	NS	20		TBD	Call TI	Call TI	0 to 70		Samples
SN74LS241NSRG4	ACTIVE	SO	NS	20		TBD	Call TI	Call TI	0 to 70		Samples
SN74LS244DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS244	Samples
SN74LS244DBRE4	ACTIVE	SSOP	DB	20		TBD	Call TI	Call TI	0 to 70		Samples
SN74LS244DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS244	Samples
SN74LS244DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS244	Samples
SN74LS244DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS244	Samples
SN74LS244DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS244	Samples
SN74LS244DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS244	Samples
SN74LS244DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS244	Samples
SN74LS244DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS244	Samples
SN74LS244J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	0 to 70		
SN74LS244N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS244N	Samples
SN74LS244N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74LS244NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS244N	Samples
SN74LS244NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS244	Samples
SN74LS244NSRE4	ACTIVE	SO	NS	20		TBD	Call TI	Call TI	0 to 70		Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS244NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS244	Samples
SN74S240DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S240	Samples
SN74S240DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S240	Samples
SN74S240DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S240	Samples
SN74S240N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S240N	Samples
SN74S240N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74S240NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S240N	Samples
SN74S241DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S241	Samples
SN74S241DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S241	Samples
SN74S241J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	0 to 70		
SN74S241N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S241N	Samples
SN74S241N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74S244DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S244	Samples
SN74S244DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S244	Samples
SN74S244DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	S244	Samples
SN74S244J	OBSOLETE	CDIP	J	20		TBD	Call TI	Call TI	0 to 70		
SN74S244N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S244N	Samples
SN74S244N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SNJ54LS240FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	78012012A SNJ54LS 240FK	Samples
SNJ54LS240J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7801201RA SNJ54LS240J	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LS240W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7801201SA SNJ54LS240W	Samples
SNJ54LS241FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 241FK	Samples
SNJ54LS241J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS241J	Samples
SNJ54LS241W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS241W	Samples
SNJ54LS244FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 244FK	Samples
SNJ54LS244J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7705701RA SNJ54LS244J	Samples
SNJ54LS244W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	7705701SA SNJ54LS244W	Samples
SNJ54S240FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 240FK	Samples
SNJ54S240J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S240J	Samples
SNJ54S240W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S240W	Samples
SNJ54S241FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 241FK	Samples
SNJ54S241J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S241J	Samples
SNJ54S241W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S241W	Samples
SNJ54S244FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 244FK	Samples
SNJ54S244J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S244J	Samples
SNJ54S244W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S244W	Samples

⁽¹⁾ The marketing status values are defined as follows:

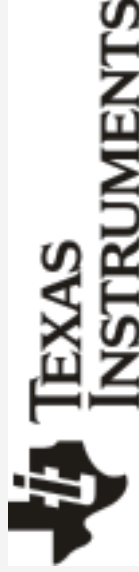
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.



(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS240, SN54LS240-SP, SN54LS241, SN54LS244, SN54LS244-SP, SN54LS244, SN54S240, SN54S241, SN54S244, SN74LS240, SN74LS241, SN74LS244, SN74S244 :

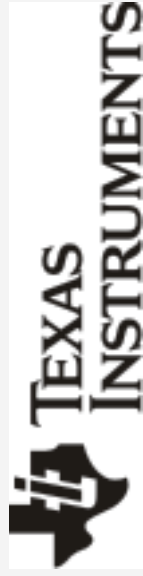
• Catalog: [SN74LS240, SN54LS240, SN74LS241, SN74LS244, SN54LS244, SN74S240, SN74S241, SN74S244](#)

• Military: [SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S244](#)

• Space: [SN54LS240-SP, SN54LS244-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



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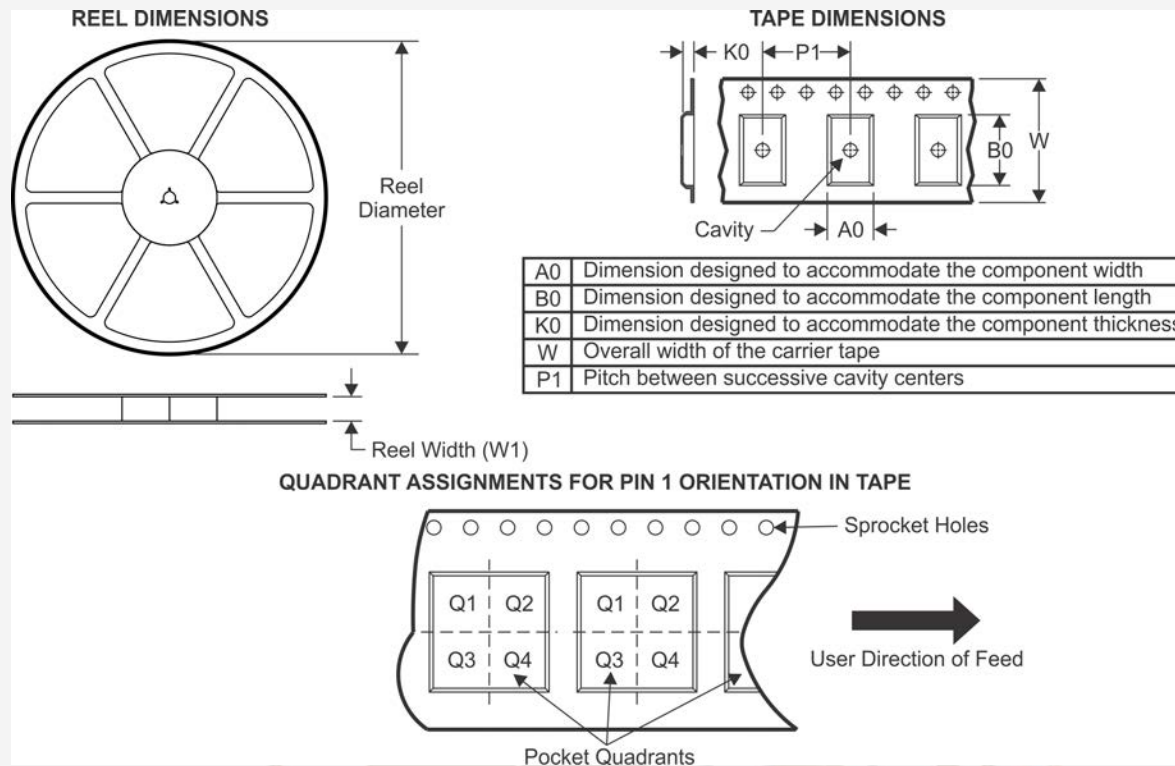
- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application



10-Jun-2014

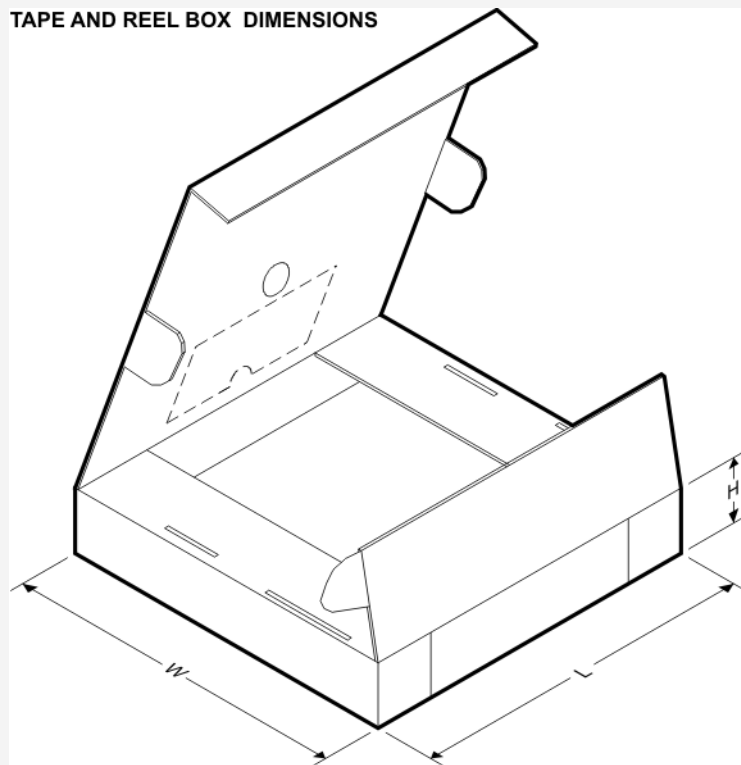
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS240DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LS240NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LS241DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LS241NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LS244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LS244DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LS244NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74S240DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74S241DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74S244DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



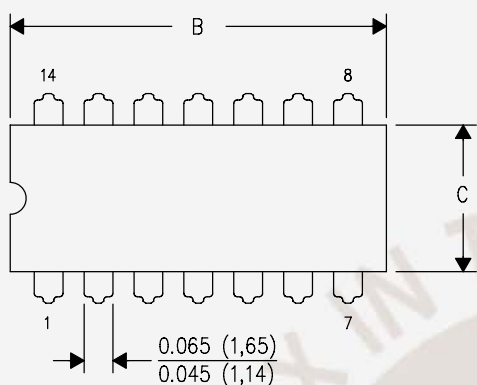
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS240DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS240NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LS241DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS241NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LS244DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LS244DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LS244NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74S240DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74S241DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74S244DWR	SOIC	DW	20	2000	367.0	367.0	45.0

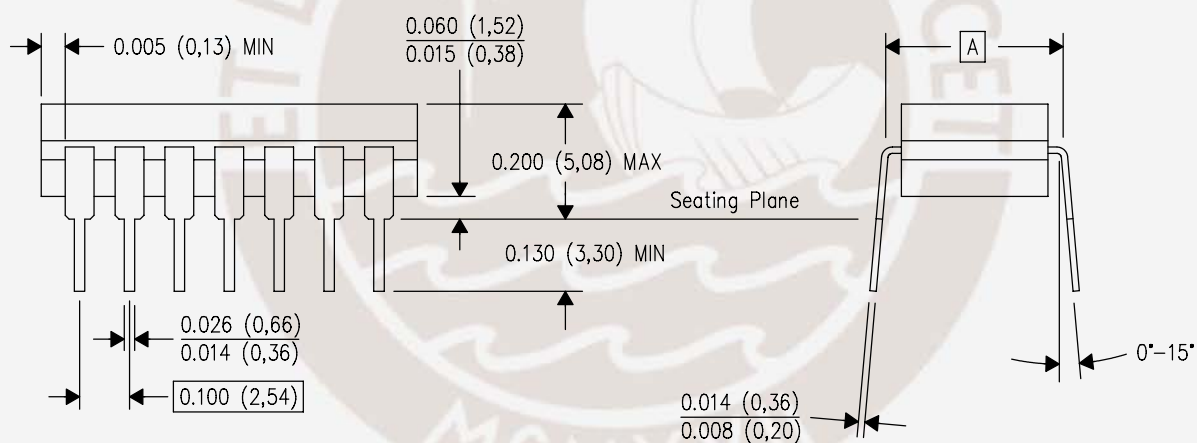
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



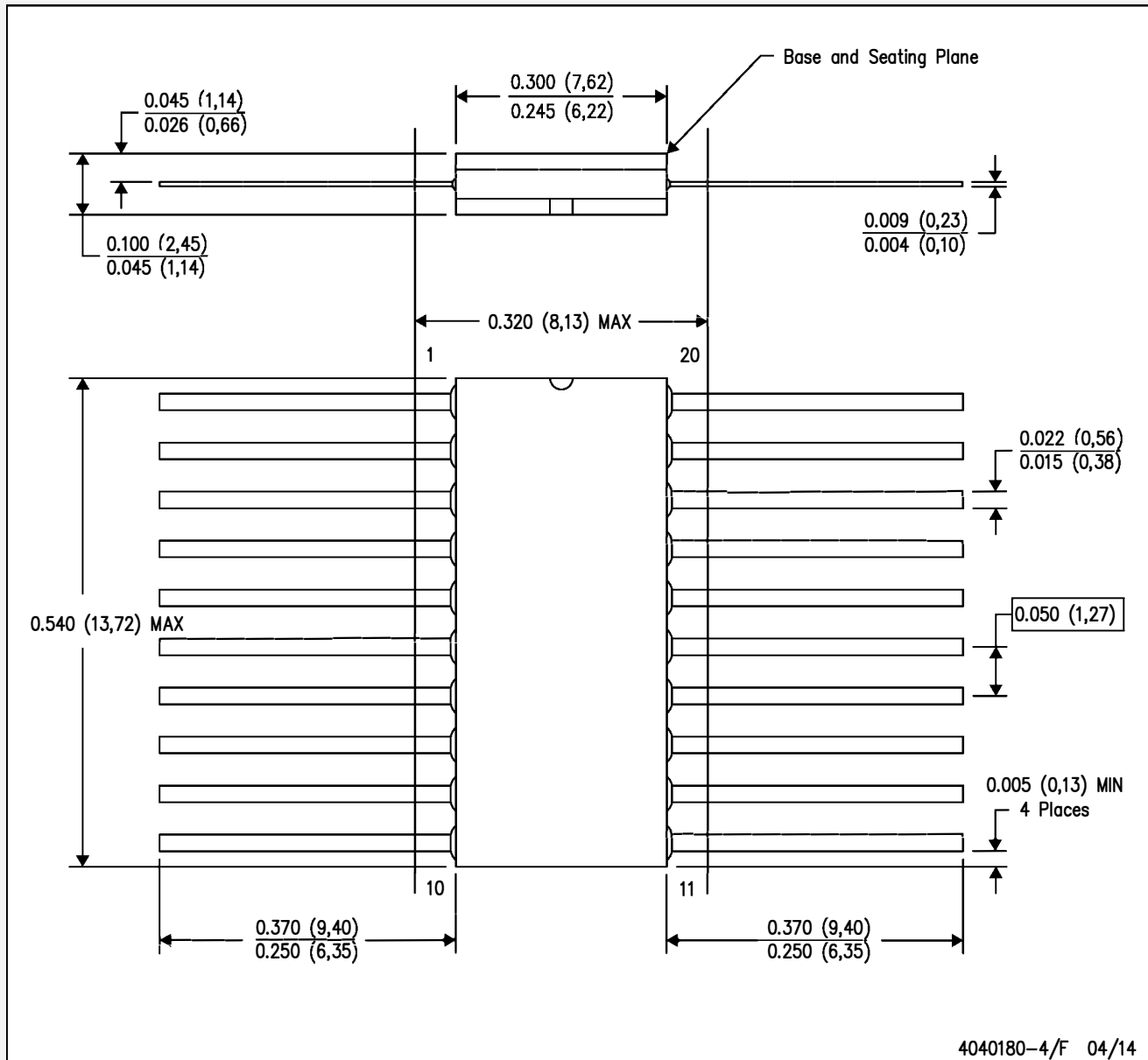
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



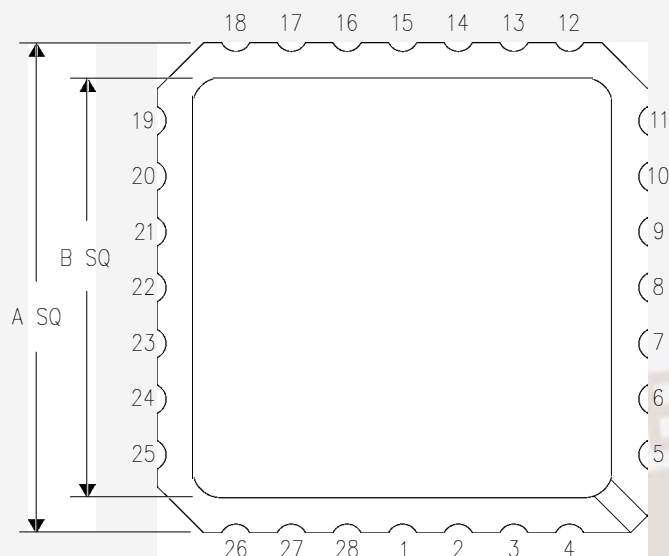
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within Mil-Std 1835 GDFP2-F20

MECHANICAL DATA

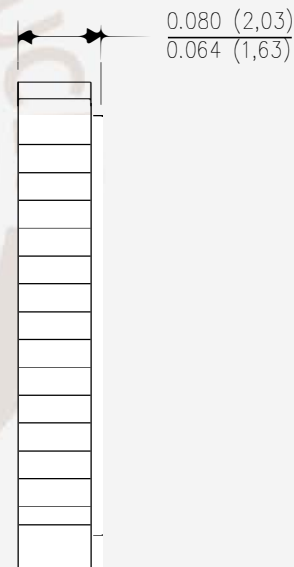
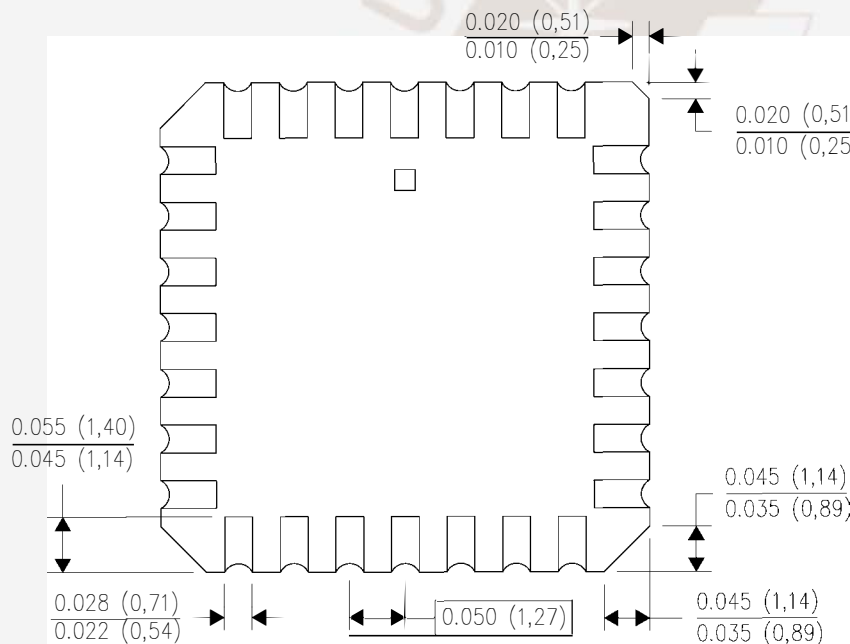
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



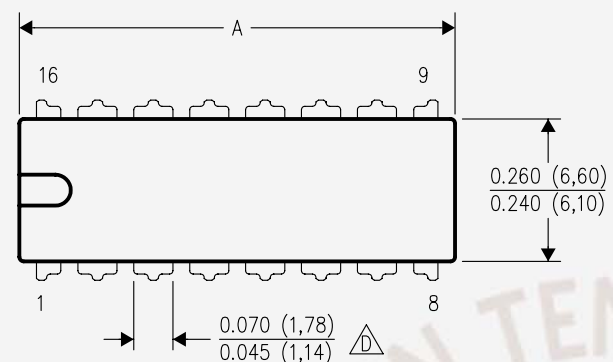
4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

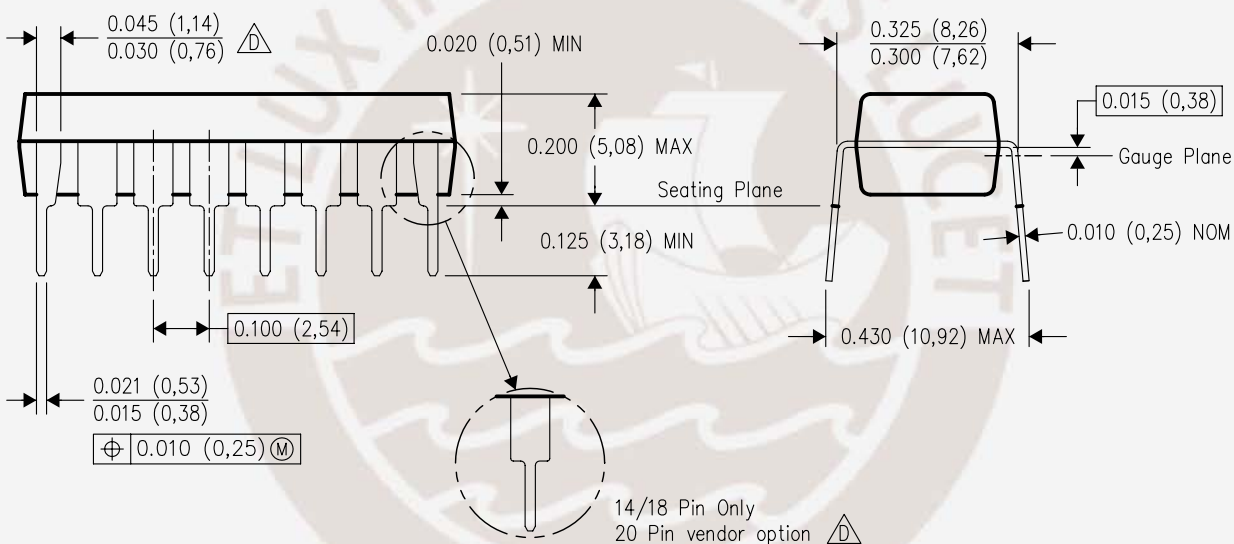
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



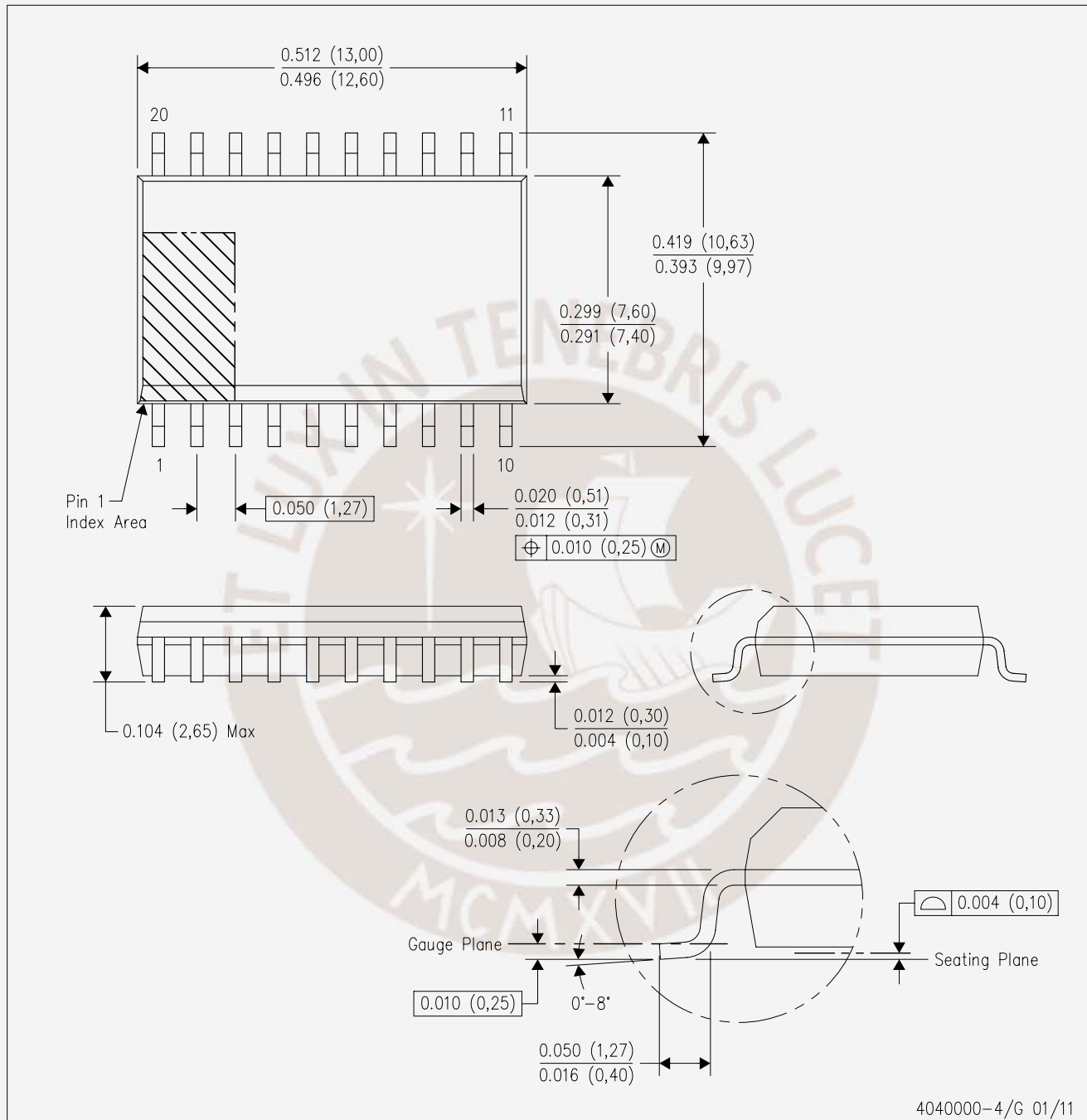
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 D The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

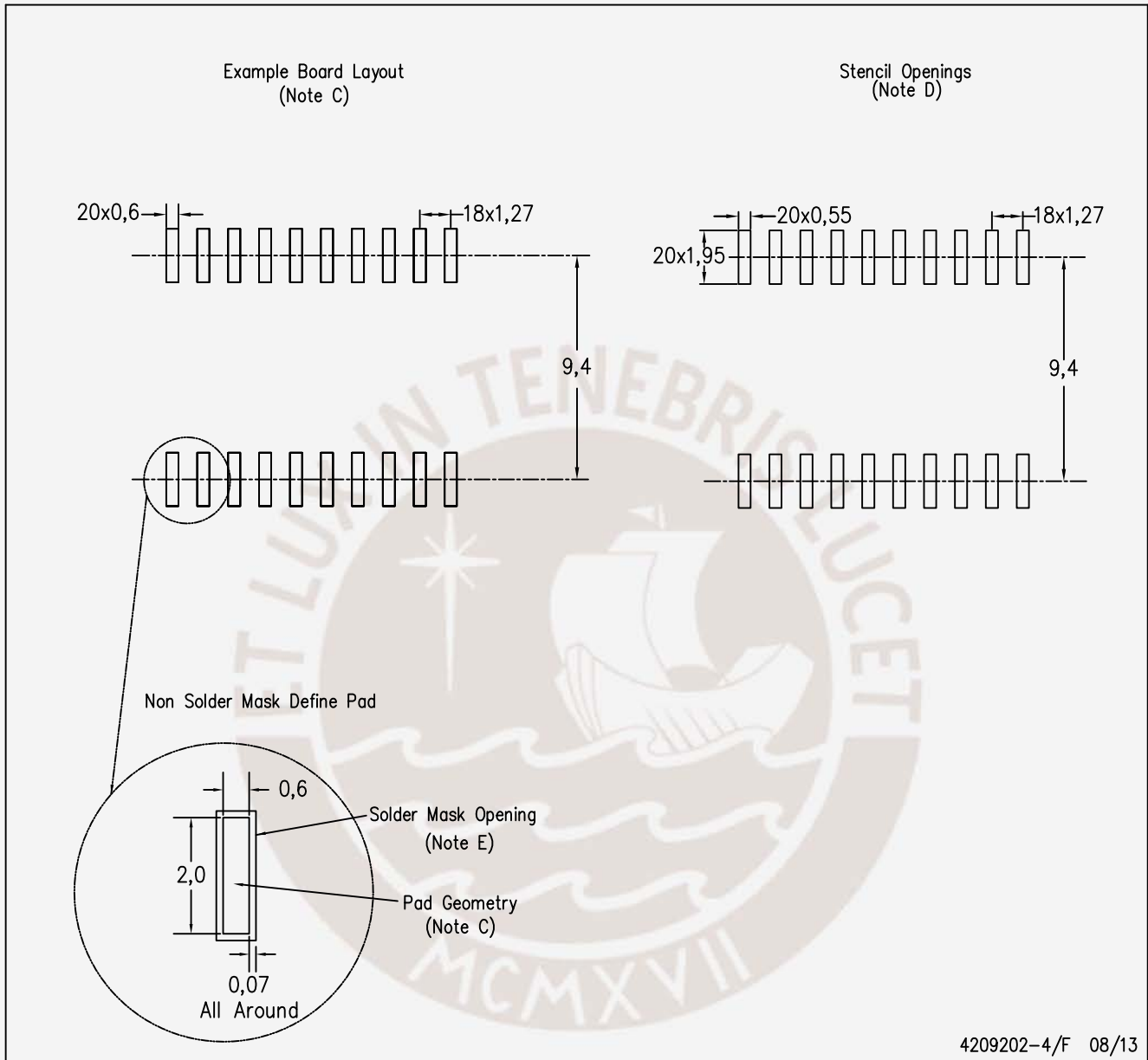
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

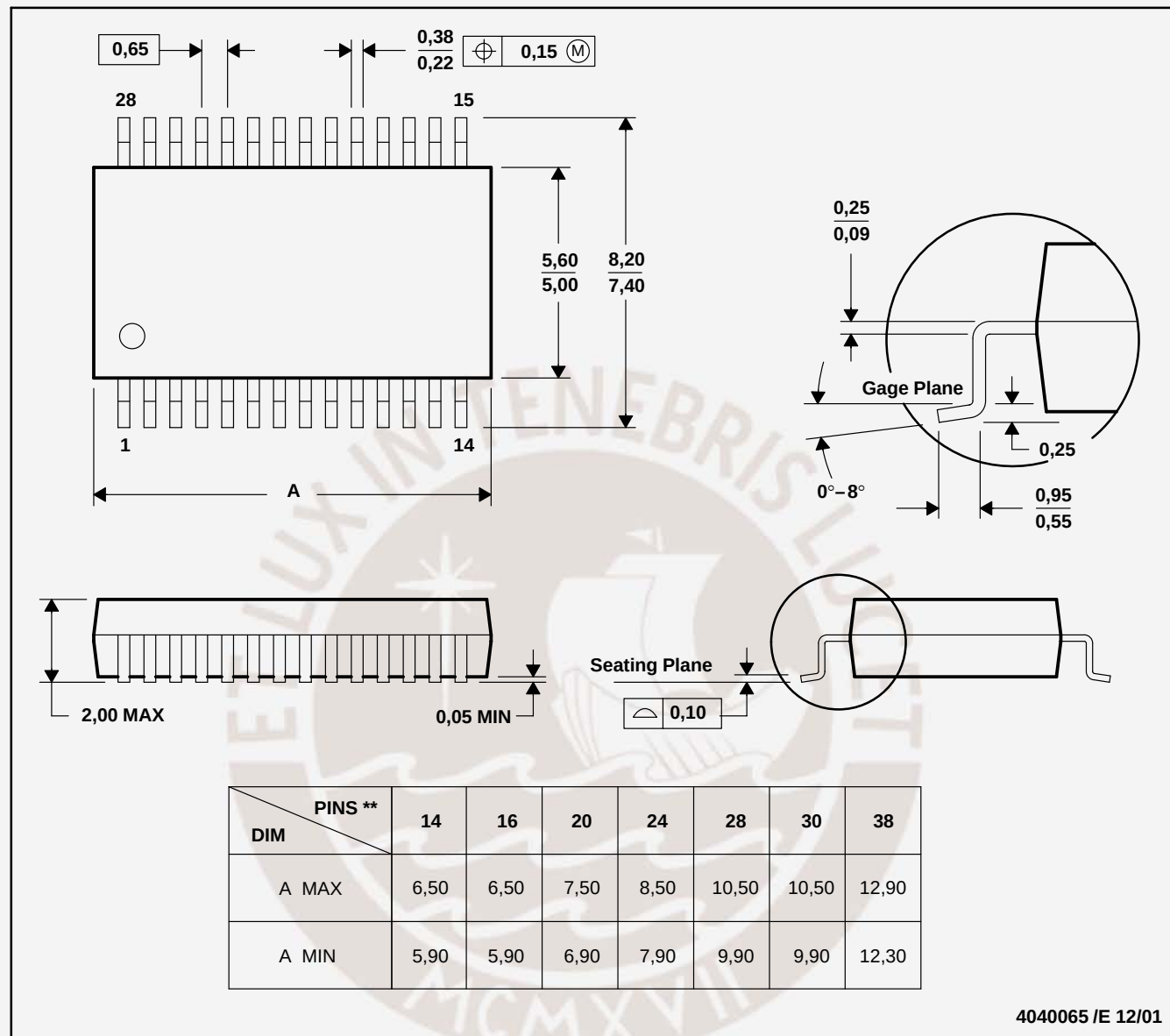


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



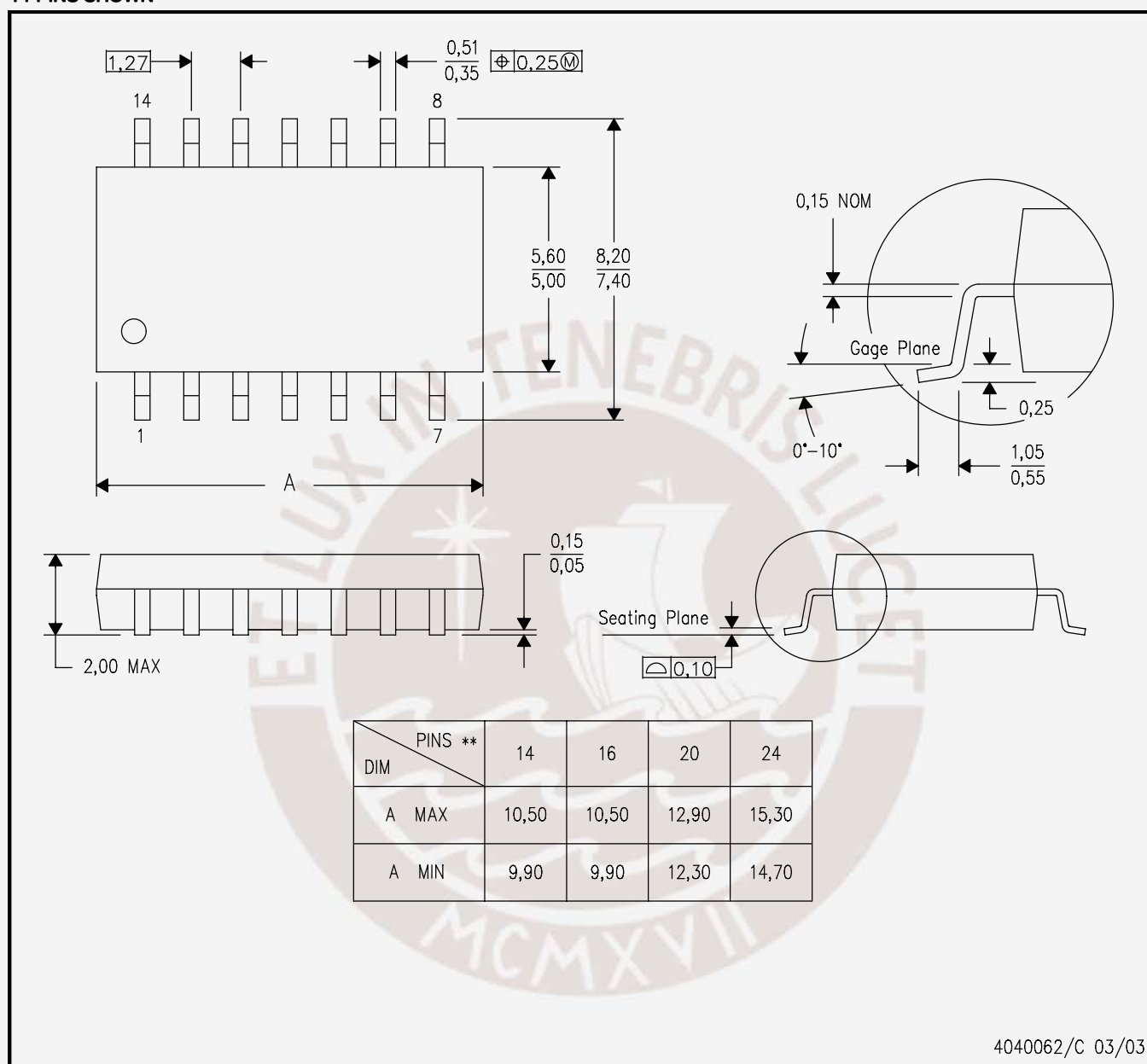
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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5.0 A Throttle Control H-Bridge

The 33926 is a SMARTMOS monolithic H-Bridge Power IC designed primarily for automotive electronic throttle control, but is applicable to any low-voltage DC servo motor control application within the current and voltage limits stated in this specification.

The 33926 is able to control inductive loads with currents up to 5.0 A peak. RMS current capability is subject to the degree of heatsinking provided to the device package. Internal peak-current limiting (regulation) is activated at load currents above 6.5 A ± 1.5 A. Output loads can be pulse width modulated (PWM'ed) at frequencies up to 20 kHz. A load current feedback feature provides a proportional (0.24% of the load current) current output suitable for monitoring by a microcontroller's A/D input. A Status Flag output reports undervoltage, overcurrent, and overtemperature fault conditions.

Two independent inputs provide polarity control of two half-bridge totem-pole outputs. Two independent disable inputs are provided to force the H-Bridge outputs to tri-state (high-impedance off state). An inverted input changes the IN1 and IN2 inputs to LOW = true logic.

Features

- 5.0 to 28 V continuous operation (transient operation from 5.0 to 40 V)
- 225 m Ω maximum $R_{DS(on)}$ at 150 °C (each H-Bridge MOSFET)
- 3.0 V and 5.0 V TTL / CMOS logic compatible inputs
- Overcurrent limiting (Regulation) via an internal constant-off-time PWM
- Output short-circuit protection (short to V_{PWR} or ground)
- Temperature dependent current limit threshold reduction
- All Inputs have an internal source/sink to define the default (floating input) states
- Sleep mode with current draw < 50 μ A (with inputs floating or set to match default logic states)



Applications

- Electronic Throttle Control (ETC)
- Exhaust Gas Recirculation (EGR)
- Turbo Flap Control
- Industrial and Medical pumps and motor control

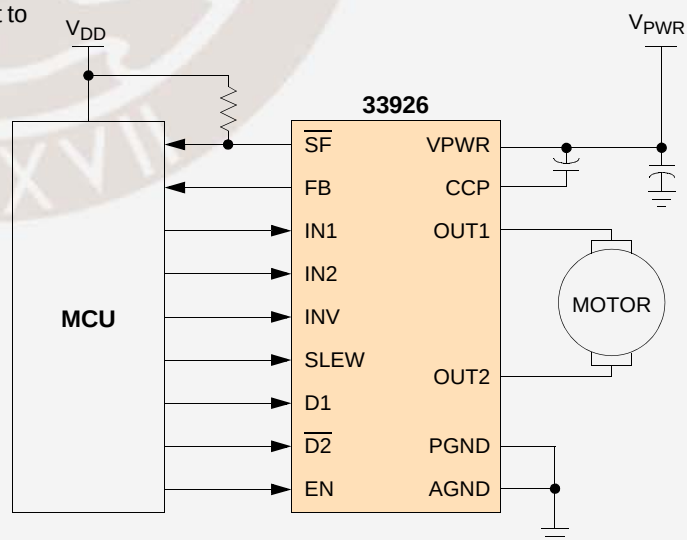


Figure 1. 33926 Simplified Application Diagram

ORDERABLE PARTS

ORDERABLE PARTS

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to <http://www.freescale.com> and perform a part number search for the following device numbers.

Table 1. Orderable Part Variations

Part Number	Notes	Temperature (T _A)	Package
MC33926PNB	(1)	-40 to 125 °C	32 PQFN

Notes

1. To order parts in Tape & Reel, add the R2 suffix to the part number.



INTERNAL BLOCK DIAGRAM

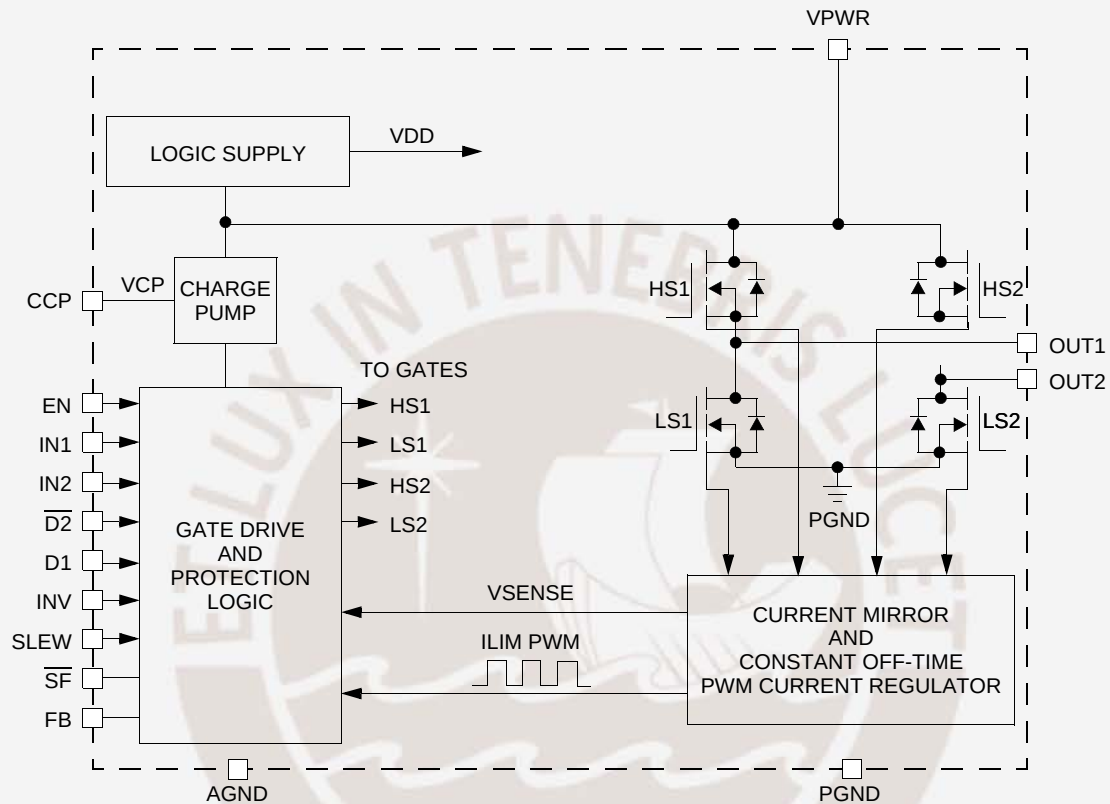


Figure 2. 33926 Simplified Internal Block Diagram

PIN CONNECTIONS

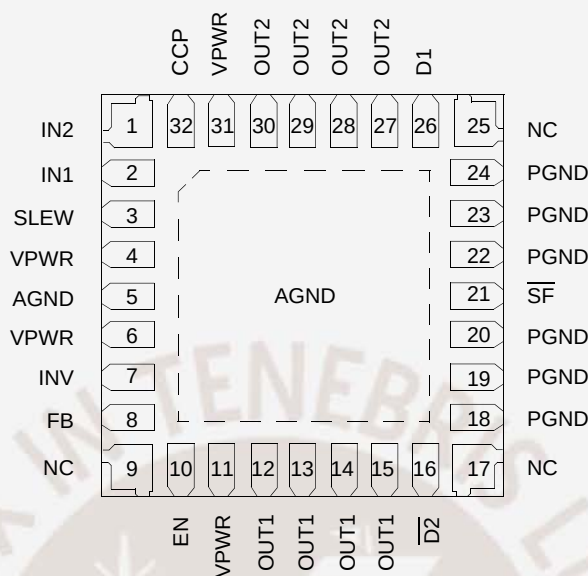
Transparent Top
View of Package

Figure 3. 33926 Pin Connections

A functional description of each pin can be found in the Functional Description section beginning on [page 13](#).

Table 2. 33926 Pin Definitions

Pin	Pin Name	Pin Function	Formal Name	Definition
1	IN2	Logic Input	Input 2	Logic input control of OUT2; e.g., when IN2 is logic HIGH, OUT2 is set to V_{PWR} , and when IN2 is logic LOW, OUT2 is set to PGND. (Schmitt trigger input with $\sim 80\ \mu\text{A}$ source so default condition = OUT2 HIGH.)
2	IN1	Logic Input	Input 1	Logic input control of OUT1; e.g., when IN1 is logic HIGH, OUT1 is set to V_{PWR} , and when IN1 is logic LOW, OUT1 is set to PGND. (Schmitt trigger Input with $\sim 80\ \mu\text{A}$ source so default condition = OUT1 HIGH.)
3	SLEW	Logic Input	Slew Rate	Logic input to select fast or slow slew rate. (Schmitt trigger input with $\sim 80\ \mu\text{A}$ sink so default condition = slow.)
4, 6, 11, 31	VPWR	Power Input	Positive Power Supply	These pins must be connected together physically as close as possible and directly soldered down to a wide, thick, low resistance supply plane on the PCB.
5, Exposed Pad	AGND	Analog Ground	Analog Signal Ground	The low current analog signal ground must be connected to PGND via low impedance path ($\ll 10\ \text{m}\Omega$, 0 Hz to 20 kHz). Exposed copper pad is also the main heatsinking path for the device.
7	INV	Logic Input	Input Invert	Sets IN1 and IN2 to logic LOW = TRUE. (Schmitt trigger input with $\sim 80\ \mu\text{A}$ sink so default condition = non-inverted.)
8	FB	Analog Output	Feedback	Load current feedback output provides ground referenced 0.24% of H-Bridge high-side output current. (Tie pin to GND through a resistor if not used.)
9, 17, 25	NC		No Connect	No internal connection is made to this pin.
10	EN	Logic Input	Enable Input	When EN is logic HIGH, the device is operational. When EN is logic LOW, the device is placed in Sleep mode. (logic input with $\sim 80\ \mu\text{A}$ sink so default condition = Sleep mode.)

Table 2. 33926 Pin Definitions (continued)

Pin	Pin Name	Pin Function	Formal Name	Definition
12, 13, 14, 15	OUT1	Power Output	H-Bridge Output 1	Source of high-side MOSFET1 and drain of low-side MOSFET1.
16	$\overline{D2}$	Logic Input	Disable Input 2 (Active Low)	When $\overline{D2}$ is logic LOW, both OUT1 and OUT2 are tri-stated. (Schmitt trigger input with $\sim 80\ \mu\text{A}$ sink so default condition = disabled.)
18–20, 22–24	PGND	Power Ground	Power Ground	High-current power ground pins must be connected together physically as close as possible and directly soldered down to a wide, thick, low resistance ground plane on the PCB.
21	SF	Logic Output - Open Drain	Status Flag (Active Low)	Open drain active LOW status flag output (requires an external pull-up resistor to V_{DD} . Maximum permissible load current $< 0.5\ \text{mA}$. Maximum $V_{CESAT} < 0.4\ \text{V}$ at $0.3\ \text{mA}$. Maximum permissible pull-up voltage $< 7.0\ \text{V}$.)
26	D1	Logic Input	Disable Input 1 (Active High)	When D1 is logic HIGH, both OUT1 and OUT2 are tri-stated. Schmitt trigger input with $\sim 80\ \mu\text{A}$ source so default condition = disabled.
27, 28, 29, 30	OUT2	Power Output	H-Bridge Output 2	Source of high-side MOSFET2 and drain of low-side MOSFET2.
32	CCP	Analog Output	Charge Pump Capacitor	External reservoir capacitor connection for internal charge pump; connected to VPWR. Allowable values are 30 to $100\ \mu\text{F}$. Note: This capacitor is required for the proper performance of the device.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device. These parameters are not production tested.

Symbol	Ratings	Value	Unit	Notes
ELECTRICAL RATINGS				
$V_{PWR(SS)}$ $V_{PWR(T)}$	Power Supply Voltage Normal Operation (Steady-state) Transient Overvoltage	-0.3 to 28 -0.3 to 40	V	(1)
V_{IN}	Logic Input Voltage	-0.3 to 7.0	V	(2)
$V_{\overline{SF}}$	$\overline{SF}$ Output	-0.3 to 7.0	V	(3)
$I_{OUT(CONT)}$	Continuous Output Current	5.0	A	(4)
V_{ESD1} V_{ESD2}	ESD Voltage Human Body Model Machine Model Charge Device Model Corner Pins (1,9,17,25) All Other Pins	± 2000 ± 200 ± 750 ± 500	V	(5)
THERMAL RATINGS				
T_{STG}	Storage Temperature	-65 to 150	°C	
T_A T_J	Operating Temperature Ambient Junction	-40 to 125 -40 to 150	°C	(6)

Notes

- Device will survive repetitive transient overvoltage conditions for durations not to exceed 500 ms at duty cycle not to exceed 10%. External protection is required to prevent device damage in case of a reverse battery condition.
- Exceeding the maximum input voltage on IN1, IN2, EN, INV, SLEW, D1, or D2 may cause a malfunction or permanent damage to the device.
- Exceeding the pull-up resistor voltage on the open drain $\overline{SF}$ pin may cause permanent damage to the device.
- Continuous output current capability is dependent on sufficient package heatsinking to keep junction temperature ≤ 150 °C.
- ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP} = 100$ pF, $R_{ZAP} = 1500$ Ω), ESD2 testing is performed in accordance with the Machine Model ($C_{ZAP} = 200$ pF, $R_{ZAP} = 0$ Ω), and the Charge Device Model (CDM), Robotic ($C_{ZAP} = 4.0$ pF).
- The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking provided. Brief non-repetitive excursions of junction temperature above 150 °C can be tolerated provided the duration does not exceed 30 seconds maximum. (Non-repetitive events are defined as not occurring more than once in 24 hours.)

Table 3. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device. These parameters are not production tested.

Symbol	Ratings	Value	Unit	Notes
T_{PPRT}	Peak Package Reflow Temperature During Reflow	250	°C	(7) (8)
$R_{\theta JC}$	Approximate Junction-to-Case Thermal Resistance	<1.0	°C/W	(9)

Notes

- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescall's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C for Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL).
- Exposed heatsink pad plus the power and ground pins comprise the main heat conduction paths. The actual $R_{\theta JB}$ (junction-to-PC board) values will vary depending on solder thickness and composition and copper trace thickness and area. Maximum current at maximum die temperature represents ~16 W of conduction loss heating in the diagonal pair of output MOSFETs. Therefore, the $R_{\theta JA}$ must be <5.0 °C/W for maximum current at 70 °C ambient. Module thermal design must be planned accordingly.

ELECTRICAL CHARACTERISTICS
 STATIC ELECTRICAL CHARACTERISTICS
STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Characteristics noted under conditions $5.0\text{ V} \leq V_{PWR} \leq 28\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$, $\text{GND} = 0\text{ V}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
POWER INPUTS (VPWR)						
$V_{PWR(SS)}$ $V_{PWR(T)}$	Operating Voltage Range Steady-state Transient ($t < 500\text{ ms}$)	5.0 –	– –	28 40	V	(10) (11)
$I_{PWR(SLEEP)}$	Sleep State Supply Current $\text{EN}, \overline{\text{D2}}, \text{INV}, \text{SLEW} = \text{Logic [0]}, \text{IN1}, \text{IN2}, \text{D1} = \text{Logic [1]}, \text{and}$ $I_{OUT} = 0\text{ A}$	–	–	50	μA	(12)
$I_{PWR(STANDBY)}$	Standby Supply Current (Part Enabled) $I_{OUT} = 0\text{ A}, V_{EN} = 5.0\text{ V}$	–	–	20	mA	
$V_{UVLO(ACTIVE)}$ $V_{UVLO(INACTIVE)}$ $V_{UVLO(HYS)}$	Undervoltage Lockout Thresholds $V_{PWR(FALLING)}$ $V_{PWR(RISING)}$ Hysteresis	4.15 – 150	– – 200	– 5.0 350	V V mV	
CHARGE PUMP						
$V_{CP} - V_{PWR}$	Charge Pump Voltage (CP Capacitor = 33 nF) $V_{PWR} = 5.0\text{ V}$ $V_{PWR} = 28\text{ V}$	3.5 –	– –	– 12	V	
CONTROL INPUTS						
V_I	Operating Input Voltage ($\text{EN}, \text{IN1}, \text{IN2}, \text{D1}, \overline{\text{D2}}, \text{INV}, \text{SLEW}$)	–	–	5.5	V	
V_{IH} V_{IL} V_{HYS}	Input Voltage ($\text{IN1}, \text{IN2}, \text{D1}, \overline{\text{D2}}, \text{INV}, \text{SLEW}$) Logic Threshold HIGH Logic Threshold LOW Hysteresis	2.0 – 250	– – 400	– 1.0 –	V V mV	(13)
V_{TH}	Input Voltage (EN) Threshold	1.0	–	2.0	V	
I_{IN}	Logic Input Currents, $V_{PWR} = 5.0\text{ V}$ Inputs $\text{EN}, \overline{\text{D2}}, \text{INV}, \text{SLEW}$ (internal pull-downs), $V_{IH} = 5.0\text{ V}$ Inputs $\text{IN1}, \text{IN2}, \text{D1}$ (internal pull-ups), $V_{IL} = 0\text{ V}$	20 –200	80 –80	200 –20	μA	

Notes

- Device specifications are characterized over the range of $8.0\text{ V} \leq V_{PWR} \leq 28\text{ V}$. Continuous operation above 28 V may degrade device reliability. Device is operational down to 5.0 V, but below 8.0 V the output resistance may increase by 50 percent.
- Device will survive the transient overvoltage indicated for a maximum duration of 500 ms. Transient not to be repeated more than once every 10 seconds.
- $I_{PWR(SLEEP)}$ is with Sleep mode activated and $\text{EN}, \overline{\text{D2}}, \text{INV}, \text{SLEW} = \text{logic [0]}$, and $\text{IN1}, \text{IN2}, \text{D1} = \text{logic [1]}$ or with these inputs left floating.
- SLEW input voltage hysteresis is guaranteed by design.

ELECTRICAL CHARACTERISTICS
STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions $5.0\text{ V} \leq V_{PWR} \leq 28\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$, $GND = 0\text{ V}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
POWER OUTPUTS OUT1, OUT2						
$R_{DS(ON)}$	Output-ON Resistance, $I_{LOAD} = 3.0\text{ A}$ $V_{PWR} = 8.0\text{ V}$, $T_J = 25\text{ }^{\circ}\text{C}$ $V_{PWR} = 8.0\text{ V}$, $T_J = 150\text{ }^{\circ}\text{C}$ $V_{PWR} = 5.0\text{ V}$, $T_J = 150\text{ }^{\circ}\text{C}$	— — —	120 — —	— 225 325	m Ω	(15)
I_{LIM}	Output Current Regulation Threshold $T_J < T_{FB}$ $T_J \geq T_{FB}$ (Fold back Region - see Figure 9 and Figure 11)	5.2 —	6.5 4.2	8.0 —	A	(14)
I_{SCH}	High-side Short-circuit Detection Threshold (Short-circuit to GND)	11	13	16	A	(14)
I_{SCL}	Low-side Short-circuit Detection Threshold (Short-circuit to VPWR)	9.0	11	14	A	(14)
$I_{OUTLEAK}$	Output Leakage Current, Outputs off, $V_{PWR} = 28\text{ V}$ $V_{OUT} = V_{PWR}$ $V_{OUT} = \text{Ground}$	— —60	— —	100 —	μA	(16)
V_F	Output MOSFET Body Diode Forward Voltage Drop $I_{OUT} = 3.0\text{ A}$	—	—	2.0	V	
T_{LIM} T_{HYS}	Overtemperature Shutdown Thermal Limit at T_J Hysteresis at T_J	175 —	— 12	200 —	$^{\circ}\text{C}$	(14)
T_{FB}	Current Foldback at T_J (14)	165	—	185	$^{\circ}\text{C}$	
T_{SEP}	Current Foldback to Thermal Shutdown Separation (14)	10	—	15	$^{\circ}\text{C}$	

HIGH-SIDE CURRENT SENSE FEEDBACK

I_{FB}	Feedback Current (pin FB sourcing current) (17)					
	$I_{OUT} = 0\text{ mA}$	0.0	—	50	μA	
	$I_{OUT} = 300\text{ mA}$	0.0	270	750	μA	
	$I_{OUT} = 500\text{ mA}$	0.35	0.775	1.56	mA	
	$I_{OUT} = 1.5\text{ A}$	2.86	3.57	4.28	mA	
	$I_{OUT} = 3.0\text{ A}$	5.71	7.14	8.57	mA	
	$I_{OUT} = 6.0\text{ A}$	11.43	14.29	17.15	mA	

STATUS FLAG (18)

I_{SFLEAK}	Status Flag Leakage Current $V_{SF} = 5.0\text{ V}$	—	—	5.0	μA	(19)
V_{SFLOW}	Status Flag SET Voltage $I_{SF} = 300\text{ }\mu\text{A}$	—	—	0.4	V	(20)

Notes

14. This parameter is guaranteed by design.
15. Output-ON resistance as measured from output to VPWR and from output to GND.
16. Outputs switched OFF via D1 or D2.
17. Accuracy is better than 20% from 0.5 to 6.0 A. Recommended terminating resistor value: $R_{FB} = 270\text{ }\Omega$.
18. Status Flag output is an open drain output requiring a pull-up resistor to logic V_{DD} .
19. Status Flag Leakage Current is measured with Status Flag HIGH and *not* SET.
20. Status Flag Set Voltage measured with Status Flag LOW and SET with $I_{SF} = 300\text{ }\mu\text{A}$. Maximum allowable sink current from this pin is $< |500\text{ }\mu\text{A}|$. Maximum allowable pull-up voltage $< 7.0\text{ V}$.

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ELECTRICAL CHARACTERISTICS
 DYNAMIC ELECTRICAL CHARACTERISTICS
DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions $5.0\text{ V} \leq V_{PWR} \leq 28\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$, $GND = 0\text{ V}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
TIMING CHARACTERISTICS						
f_{PWM}	PWM Frequency	–	–	20	kHz	(21)
f_{MAX}	Maximum Switching Frequency During Current Limit Regulation	–	–	20	kHz	(22)
t_{DON}	Output ON Delay $V_{PWR} = 14\text{ V}$	–	–	18	μs	(23)
t_{DOFF}	Output OFF Delay $V_{PWR} = 14\text{ V}$	–	–	12	μs	(23)
t_A	I_{LIM} Output Constant-OFF Time	15	20.5	32	μs	(24)
t_B	I_{LIM} Blanking Time	12	16.5	27	μs	(25)
$t_{DDISABLE}$	Disable Delay Time	–	–	8.0	μs	(26)
t_F, t_R	Output Rise and Fall Time SLEW = SLOW SLEW = FAST	1.5 0.2	3.0 –	6.0 1.45	μs	(27)
t_{FAULT}	Short-circuit/Overtemperature Turn-OFF (Latch-OFF) Time	–	–	8.0	μs	(28) (29)
t_{POD}	Power-ON Delay Time	–	1.0	5.0	ms	(29)
t_{RR}	Output MOSFET Body Diode Reverse Recovery Time	75	100	150	ns	(29)
f_{CP}	Charge Pump Operating Frequency	–	7.0	–	MHz	(29)

Notes

21. The maximum PWM frequency is obtained when the device is set to Fast Slew Rate via the SLEW pin. PWM-ing when SLEW is set to SLOW should be limited to frequencies < 11 kHz in order to allow the internal high-side driver circuitry time to fully enhance the high-side MOSFETs.
22. The internal current limit circuitry produces a constant-OFF-time Pulse Width Modulation of the output current. The output load's inductance, capacitance, and resistance characteristics affect the total switching period (OFF-time + ON-time), and thus the PWM frequency during current limit.
23. Output Delay is the time duration from 1.5 V on the IN1 or IN2 input signal to the 20% or 80% point (dependent on the transition direction) of the OUT1 or OUT2 signal. If the output is transitioning HIGH-to-LOW, the delay is from 1.5 V on the input signal to the 80% point of the output response signal. If the output is transitioning LOW-to-HIGH, the delay is from 1.5 V on the input signal to the 20% point of the output response signal. See [Figure 4](#), page 11.
24. The time during which the internal constant-OFF time PWM current regulation circuit has tri-stated the output bridge.
25. The time during which the current regulation threshold is ignored so that the short-circuit detection threshold comparators may have time to act.
26. Disable Delay Time measurement is defined in [Figure 5](#), page 11.
27. Rise Time is from the 10% to the 90% level and Fall Time is from the 90% to the 10% level of the output signal with $V_{PWR} = 14\text{ V}$, $R_{LOAD} = 3.0\text{ ohm}$. See [Figure 6](#), page 11.
28. Load currents ramping up to the current regulation threshold become limited at the I_{LIM} value (see [Figure 7](#)). The short-circuit currents possess a di/dt that ramps up to the I_{SCH} or I_{SCL} threshold during the I_{LIM} blanking time, registering as a short-circuit event detection and causing the shutdown circuitry to force the output into an immediate tri-state latch-OFF (see [Figure 8](#)). Operation in Current Limit mode may cause junction temperatures to rise. Junction temperatures above $\sim 160^{\circ}\text{C}$ will cause the output current limit threshold to "fold back", or decrease, until $\sim 175\text{ }^{\circ}\text{C}$ is reached, after which the T_{LIM} thermal latch-OFF will occur. Permissible operation within this fold back region is limited to non-repetitive transient events of duration not to exceed 30 seconds (see [Figure 9](#)).
29. Parameter is guaranteed by design.

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TIMING DIAGRAMS

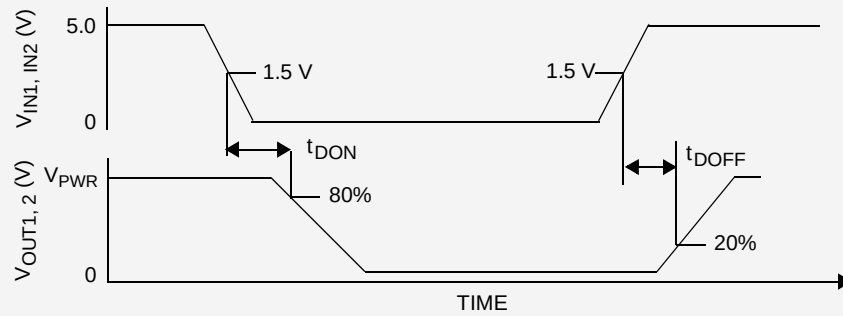


Figure 4. Output Delay Time

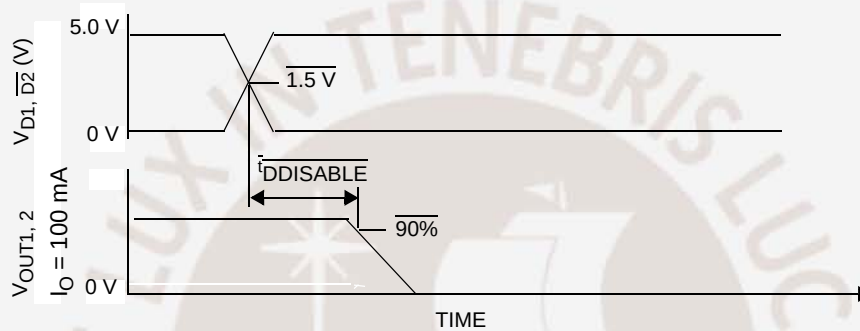


Figure 5. Disable Delay Time

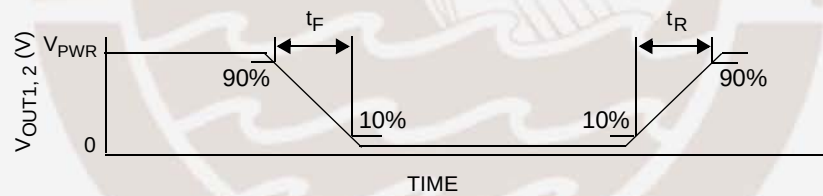


Figure 6. Output Switching Time

Overload Condition

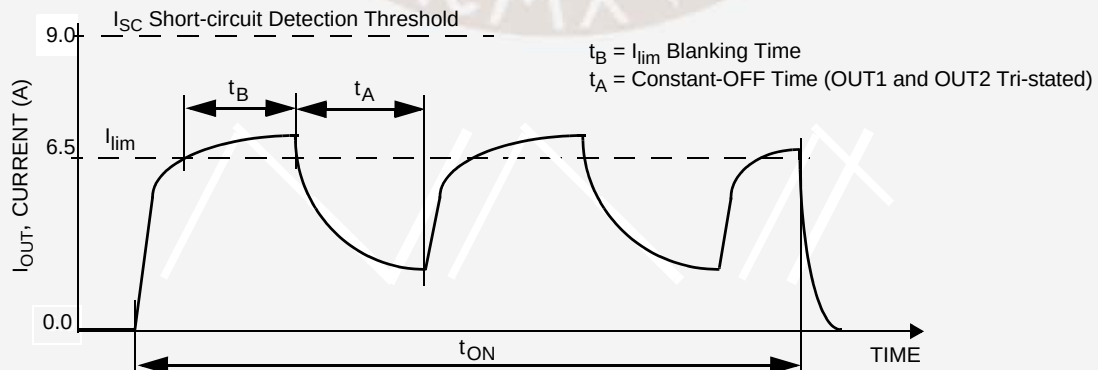


Figure 7. Current Limit Blanking Time and Constant-OFF Time

33926

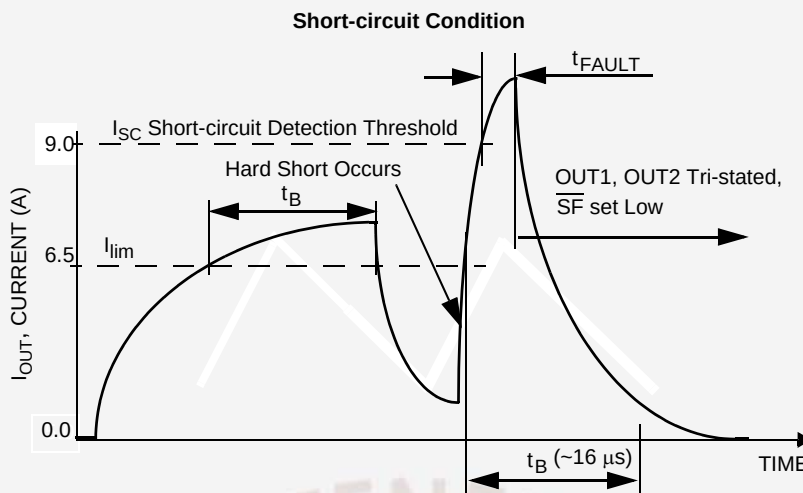


Figure 8. Short-circuit Detection Turn-OFF Time t_{FAULT}

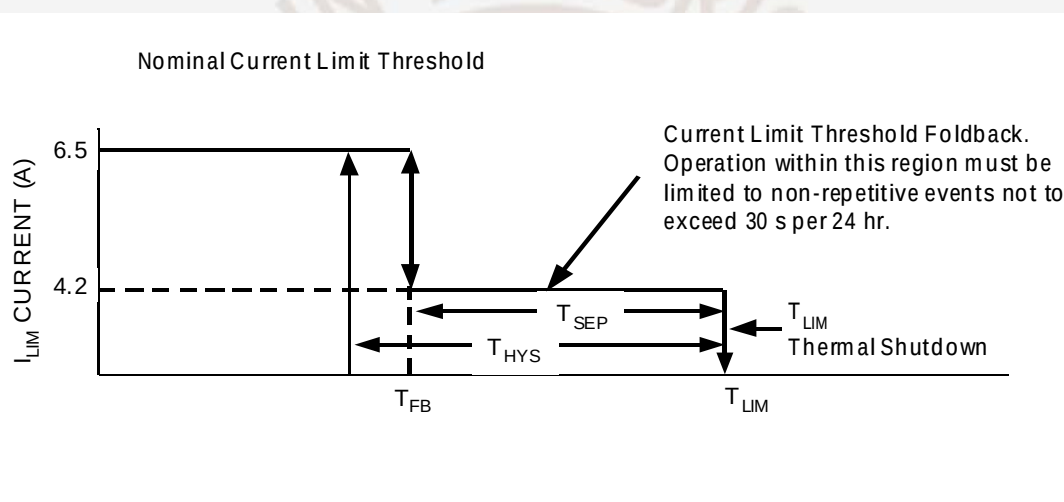


Figure 9. Output Current Limiting Foldback Region

FUNCTIONAL DESCRIPTION

INTRODUCTION

Numerous protection and operational features (speed, torque, direction, dynamic braking, PWM control, and closed-loop control) make the 33926 a very attractive, cost-effective solution for controlling a broad range of small DC motors. The 33926 outputs are capable of supporting peak DC load currents of up to 5.0 A from a 28 V_{PWR} source. An internal charge pump and gate drive circuitry are provided that can support external PWM frequencies up to 20 kHz.

The 33926 has an analog feedback (current mirror) output pin (the FB pin) that provides a constant-current source ratioed to the active high-side MOSFETs' current. This can be used to provide "real time" monitoring of output current to facilitate closed-loop operation for motor speed/torque control, or for the detection of open load conditions.

Two independent inputs, IN1 and IN2, provide control of the two totem-pole half-bridge outputs. An input invert, INV, changes IN1 and IN2 to LOW = true logic. Two different output slew rates are selectable via the SLEW input. Two independent disable inputs, D1 and D2, provide the means to force the H-Bridge outputs to a high-impedance state (all H-Bridge switches OFF). An EN pin controls an enable function that allows the IC to be placed in a power-conserving Sleep mode.

The 33926 has Output Current Limiting (via Constant OFF-Time PWM Current Regulation), Output Short-circuit Detection with Latch-OFF, and Overtemperature Detection with Latch-OFF. Once the device is latched-OFF due to a fault condition, either of the Disable inputs (D1 or D2), V_{PWR}, or EN must be "toggled" to clear the status flag.

Current limiting (Load Current Regulation) is accomplished by a constant-OFF time PWM method using current limit threshold triggering. The current limiting scheme is unique in that it incorporates a junction temperature-dependent current limit threshold. This means that the current limit threshold is "reduced to around 4.2 A" as the junction temperature increases above 160 °C. When the temperature is above 175 °C, overtemperature shutdown (latch-OFF) will occur. This combination of features allows the device to continue operating for short periods of time (<30 seconds) with unexpected loads, while still retaining adequate protection for both the device and the load.

FUNCTIONAL PIN DESCRIPTION

POWER GROUND AND ANALOG GROUND (PGND AND AGND)

The power and analog ground pins should be connected together with a very low-impedance connection.

POSITIVE POWER SUPPLY (VPWR)

VPWR pins are the power supply inputs to the device. All VPWR pins must be connected together on the printed circuit board with as short as possible traces, offering as low-impedance as possible between pins.

Transients on V_{PWR} which go below the undervoltage threshold will result in the protection activating. It is essential to use an input filter capacitor of sufficient size and low ESR to sustain a V_{PWR} greater than V_{UVLO} when the load is switched (See [33926 Typical Application Schematic on page 19](#)).

STATUS FLAG ($\overline{\text{SF}}$)

This pin is the device fault status output. This output is an active LOW open drain structure requiring a pull-up resistor to V_{DD}. The maximum V_{DD} is <7.0 V. Refer to [Table 6, Truth Table](#), page [17](#) for the SF Output status definition.

INPUT INVERT (INV)

The Input Invert Control pin sets IN1 and IN2 to LOW = TRUE. This is a Schmitt trigger input with ~80 µA sink; the default condition is non-inverted. If IN1 and IN2 are set so that the current is being commanded to flow through the load attached between OUT1 and OUT2, changing the logic level at INV will have the effect of reversing the direction of current commanded. Thus, the INV input may be used as a "forward/reverse" command input. If both IN1 and IN2 are the same logic level, then changing the logic level at INV will have the effect of changing the bridge's output from freewheeling high to freewheeling low or vice versa.

SLEW RATE (SLEW)

The SLEW pin is the logic input that selects fast or slow slew rate. Schmitt trigger input with ~80 µA sink so the default condition is SLOW. When SLEW is set to SLOW, PWM-ing should be limited to frequencies less than 11 kHz in order to allow the internal high-side driver circuitry time to fully enhance the high-side MOSFETs.

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INPUT 1,2 AND DISABLE INPUT 1,2 (IN1, IN2, AND D1, $\overline{D2}$)

These pins are input control pins used to control the outputs. These pins are 3.0 V/5.0 V CMOS-compatible inputs with hysteresis. IN1 and IN2 independently control OUT1 and OUT2, respectively. D1 and $\overline{D2}$ are complementary inputs used to tri-state disable the H-Bridge outputs.

When either D1 or $\overline{D2}$ is SET (D1 = logic HIGH or $\overline{D2}$ = logic LOW) in the disable state, outputs OUT1 and OUT2 are both tri-state disabled; however, the rest of the device circuitry is fully operational and the supply $I_{PWR(Standby)}$ current is reduced to a few mA. Refer to [Table 4, Static Electrical Characteristics](#), [page 8](#).

H-BRIDGE OUTPUT (OUT1, OUT2)

These pins are the outputs of the H-Bridge with integrated freewheeling diodes. The bridge output is controlled using the IN1, IN2, D1, and $\overline{D2}$ inputs. The outputs have PWM current limiting above the I_{LIM} threshold. The outputs also have thermal shutdown (tri-state latch-OFF) with hysteresis as well as short-circuit latch-OFF protection.

A disable timer (time t_B) is incorporated to distinguish between load currents that are higher than the I_{LIM} threshold and short-circuit currents. This timer is activated at each output transition.

CHARGE PUMP CAPACITOR (CCP)

This pin is the charge pump output pin and connection for the external charge pump reservoir capacitor. The allowable value is from 30 to 100 nF. This capacitor must be connected from the CCP pin to the VPWR pin. The device cannot operate properly without the external reservoir capacitor.

ENABLE INPUT (EN)

The EN pin is used to place the device in a Sleep mode so as to consume very low currents. When the EN pin voltage is a logic LOW state, the device is in Sleep mode. The device is enabled and fully operational when the EN pin voltage is in logic HIGH. An internal pulldown resistor maintains the device in Sleep mode in the event EN is driven through a high-impedance I/O, or an unpowered microcontroller, or the EN input becomes disconnected.

FEEDBACK (FB)

The 33926 has a feedback output (FB) for “real time” monitoring of H-Bridge high-side output currents to facilitate closed-loop operation for motor speed and torque control.

The FB pin provides current sensing feedback of the H-Bridge high-side drivers. When running in the forward or reverse direction, a ground-referenced 0.24% of load current is output to this pin. Through the use of an external resistor to ground, the proportional feedback current can be converted to a proportional voltage equivalent and the controlling microcontroller can “read” the current proportional voltage with its analog-to-digital converter (ADC). This is intended to provide the user with only first-order motor current feedback for motor torque control. The resistance range for the linear operation of the FB pin is $100 < R_{FB} < 300 \Omega$.

If PWM-ing is implemented using the disable pin inputs (either D1 or $\overline{D2}$), a small filter capacitor ($\sim 1.0 \mu F$) may be required in parallel with the R_{FB} resistor to ground for spike suppression.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

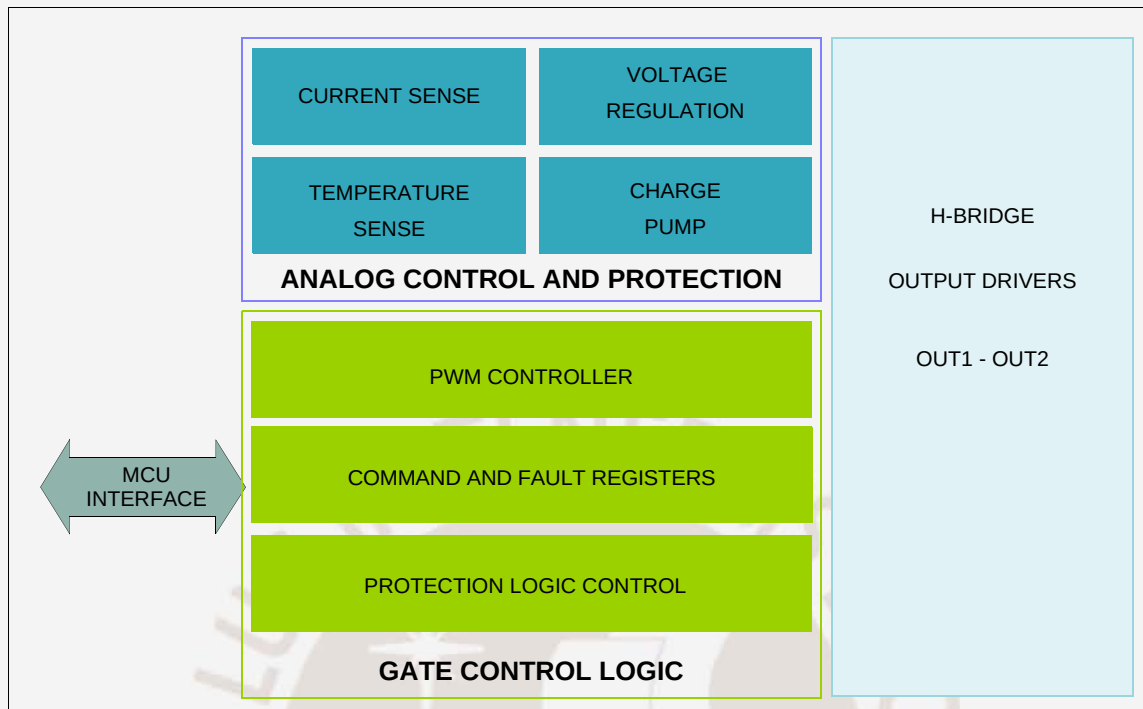


Figure 10. 33926 Functional Internal Block Diagram

ANALOG CONTROL AND PROTECTION CIRCUITRY

The on-chip voltage regulator supplies 3.3 V to the internal logic. The charge pump provides gate drive for the H-Bridge MOSFETs. The current and temperature sense circuitry provides detection and protection for the output drivers. Output undervoltage protection shuts down the MOSFETS.

GATE CONTROL LOGIC

The 33926 is a monolithic H-Bridge Power IC designed primarily for any low voltage DC servo motor control application within the current and voltage limits stated for the device. Two independent inputs provide polarity control of two half-bridge totem-pole outputs. Two independent disable inputs are provided to force the H-Bridge outputs to tri-state (high-impedance off-state).

H-BRIDGE OUTPUT DRIVERS: OUT1 AND OUT2

The H-Bridge is the power output stage. The current flow from OUT1 to OUT2 is reversible and under full control of the user by way of the Input Control Logic. The output stage is designed to produce full load control under all system conditions. All protective and control features are integrated into the control and protection blocks. The sensors for current and temperature are integrated directly into the output MOSFET for maximum accuracy and dependability.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

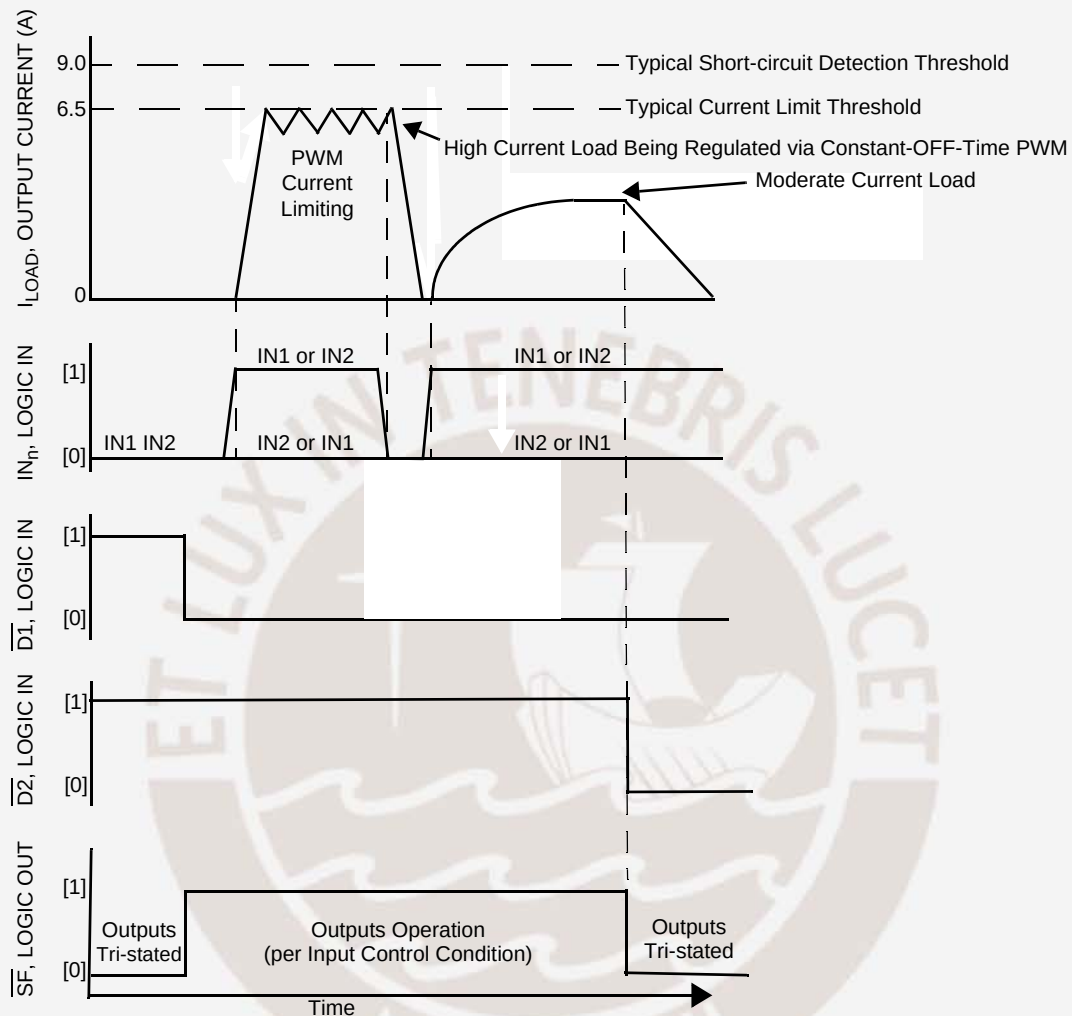


Figure 11. Operating States

LOGIC COMMANDS AND REGISTERS

Table 6. Truth Table

The tri-state conditions and the status flag are reset using D1 or $\overline{D2}$. The truth table uses the following notations: L = LOW, H = HIGH, X = HIGH or LOW, and Z = High-impedance. All output power transistors are switched off.

Device State	Input Conditions					Status	Outputs	
	EN	D1	$\overline{D2}$	IN1	IN2	$\overline{SF}$	OUT1	OUT2
Forward	H	L	H	H	L	H	H	L
Reverse	H	L	H	L	H	H	L	H
Free Wheeling Low	H	L	H	L	L	H	L	L
Free Wheeling High	H	L	H	H	H	H	H	H
Disable 1 (D1)	H	H	X	X	X	L	Z	Z
Disable 2 ($\overline{D2}$)	H	X	L	X	X	L	Z	Z
IN1 Disconnected	H	L	H	Z	X	H	H	X
IN2 Disconnected	H	L	H	X	Z	H	X	H
D1 Disconnected	H	Z	X	X	X	L	Z	Z
$\overline{D2}$ Disconnected	H	X	Z	X	X	L	Z	Z
Undervoltage Lockout ⁽³⁰⁾	H	X	X	X	X	L	Z	Z
Overttemperature ⁽³¹⁾	H	X	X	X	X	L	Z	Z
Short-circuit ⁽³¹⁾	H	X	X	X	X	L	Z	Z
Sleep Mode EN	L	X	X	X	X	H	Z	Z
EN Disconnected	Z	X	X	X	X	H	Z	Z

Notes

30. In the event of an undervoltage condition, the outputs tri-state and status flag is SET logic LOW. Upon undervoltage recovery, status flag is reset automatically or automatically cleared and the outputs are restored to their original operating condition.
31. When a short-circuit or overtemperature condition is detected, the power outputs are tri-state latched-OFF, independent of the input signals, and the status flag is latched to logic LOW. To reset from this condition requires the toggling of either D1, $\overline{D2}$, EN, or V_{PWR} .

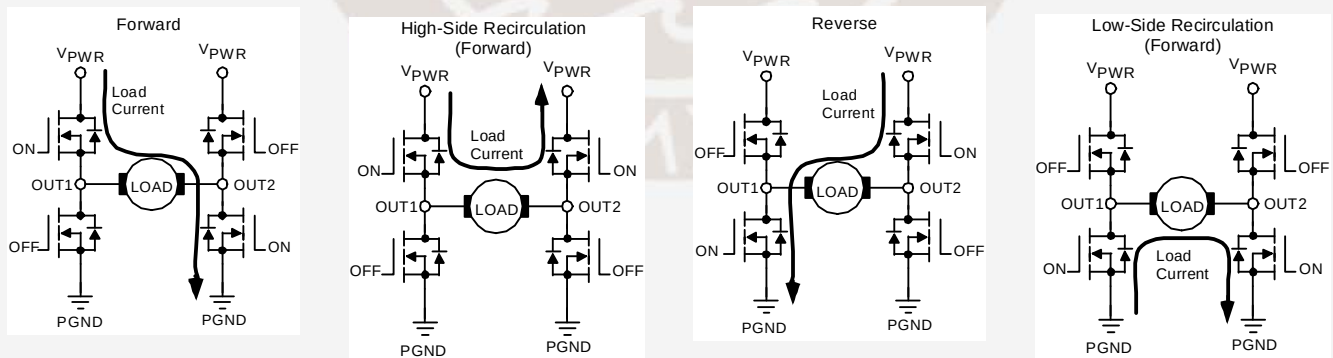


Figure 12. 33926 Power Stage Operation

PROTECTION AND DIAGNOSTIC FEATURES

SHORT-CIRCUIT PROTECTION

If an output short-circuit condition is detected, the power outputs tri-state (latch-OFF) independent of the input (IN1 and IN2) states, and the fault status output flag (SF) is SET to a logic LOW. If the D1 input changes from a logic HIGH to logic LOW, or if the D2 input changes from a logic LOW to logic HIGH, the output bridge will become operational again, and the fault status flag will be reset (cleared) to a logic HIGH state.

The output stage will always switch into the mode defined by the input pins (IN1, IN2, D1, and $\overline{D2}$), provided the device junction temperature is within the specified operating temperature range.

INTERNAL PWM CURRENT LIMITING

The maximum current flow under normal operating conditions should be less than 5.0 A. The instantaneous load currents will be limited to I_{LIM} via the internal PWM current limiting circuitry. When the I_{LIM} threshold current value is reached, the output stages are tri-stated for a fixed time (T_A) of 20 μ s typical. Depending on the time constant associated with the load characteristics, the output current decreases during the tri-state duration until the next output ON cycle occurs.

The PWM current limit threshold value is dependent on the device junction temperature. When $-40^\circ\text{C} < T_J < 160^\circ\text{C}$, I_{LIM} is between the specified minimum/maximum values. When T_J exceeds 160°C , the I_{LIM} threshold decreases to 4.2 A. Shortly above 175°C the device overtemperature circuit will detect T_{LIM} and an overtemperature shutdown will occur. This feature implements a graceful degradation of operation before thermal shutdown occurs, thus allowing for intermittent unexpected mechanical loads on the motor's gear-reduction train to be handled.

Important Die temperature excursions above 150°C are permitted only for non-repetitive durations < 30 seconds. Provision must be made at the system level to prevent prolonged operation in the current-foldback region.

OVERTEMPERATURE SHUTDOWN AND HYSTERESIS

If an overtemperature condition occurs, the power outputs are tri-stated (latched-OFF), and the fault status flag ($\overline{SF}$) is SET to a logic LOW.

To reset from this condition, D1 must change from a logic HIGH to logic LOW, or $\overline{D2}$ must change from a logic LOW to logic HIGH. When reset, the output stage switches ON again, provided that the junction temperature is now below the overtemperature threshold limit minus the hysteresis.

Important Resetting from the fault condition will clear the fault status flag. Powering down and powering up the device will also reset the 33926 from the fault condition.

OUTPUT AVALANCHE PROTECTION

If VPWR were to become an open circuit, the outputs would likely tri-state simultaneously due to the disable logic. This could result in an unclamped inductive discharge. The VPWR input to the 33926 should not exceed 40 V during this transient condition, to prevent electrical overstress of the output drivers. This can be accomplished with a zener clamp or MOV, and/or an appropriately valued input capacitor with sufficiently low ESR (see Figure 13).

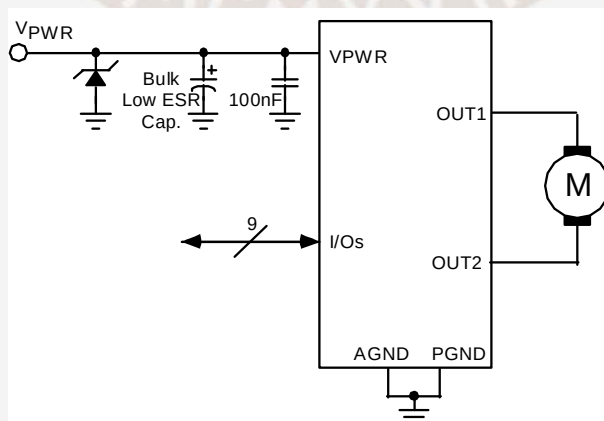


Figure 13. Avalanche Protection

TYPICAL APPLICATIONS

INTRODUCTION

A typical application schematic is shown in [Figure 14](#). For precision high current applications in harsh, noisy environments, the V_{PWR} by-pass capacitor may need to be substantially larger.

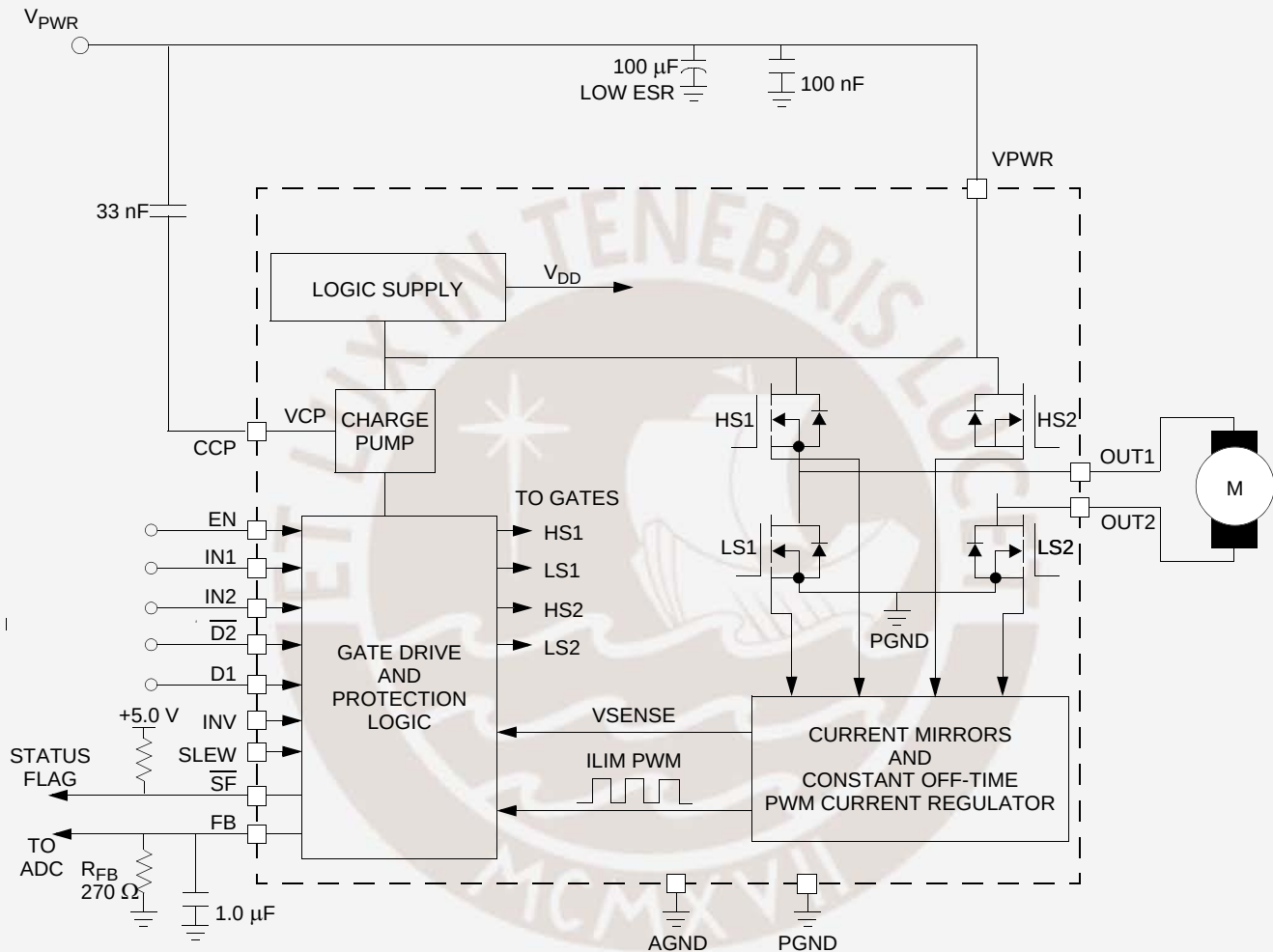
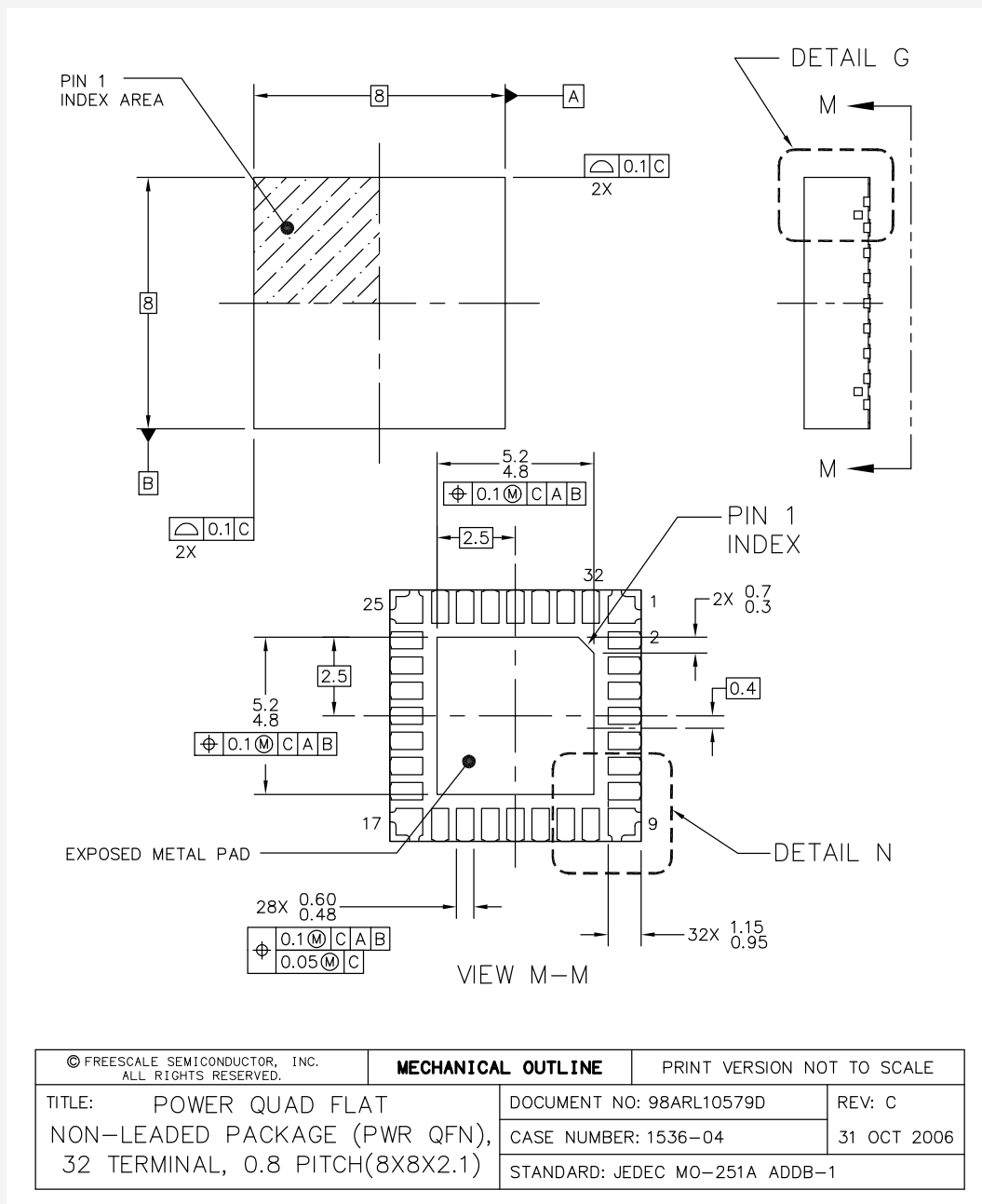


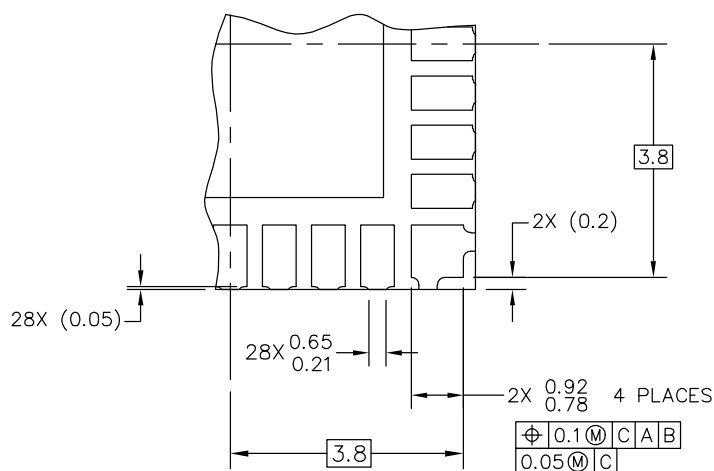
Figure 14. 33926 Typical Application Schematic

PACKAGING

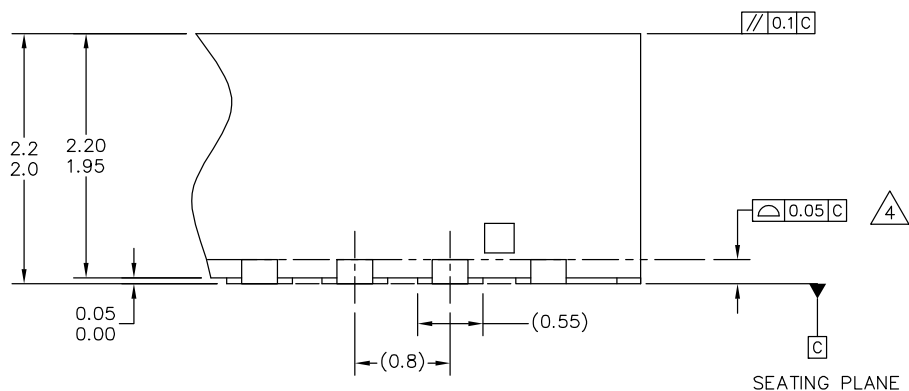
PACKAGE DIMENSIONS

For the most current package revision, visit www.freescale.com and perform a keyword search using the 98Axxxxxxx listed below.





DETAIL N
CORNER CONFIGURATION



DETAIL G
VIEW ROTATED 90° CW

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: POWER QUAD FLAT NON-LEADED PACKAGE (PWR QFN), 32 TERMINAL, 0.8 PITCH(8X8X2.1)		DOCUMENT NO: 98ARL10579D		REV: C	
		CASE NUMBER: 1536-04		31 OCT 2006	
		STANDARD: JEDEC MO-251A AADB-1			

ADDITIONAL DOCUMENTATION

THERMAL ADDENDUM (REV 2.0)

Introduction

This thermal addendum is provided as a supplement to the 33926 technical datasheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the datasheet.

Packaging and Thermal Considerations

The 33926 is offered in a 32 pin PQFN, single die package. There is a single heat source (P), a single junction temperature (T_J), and thermal resistance ($R_{\theta JA}$).

$$\{ T_J \} = [R_{\theta JA}] \cdot \{ P \}$$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to, and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

STANDARDS

Table 7. Thermal Performance Comparison

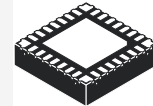
Thermal Resistance	[°C/W]
$R_{\theta JA}$ (1),(2)	28
$R_{\theta JB}$ (2),(3)	12
$R_{\theta JA}$ (1), (4)	80
$R_{\theta JC}$ (5)	1.0

Notes

1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-5 and JESD51-7.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the center lead.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad surface; cold plate attached to the package bottom side, remaining surfaces insulated.

33926

**32-PIN
PQFN**



**PNB SUFFIX
98ARL10579D
32-PIN PQFN
8.0 mm x 8.0 mm**

Note For package dimensions, refer to the 33926 data sheet.

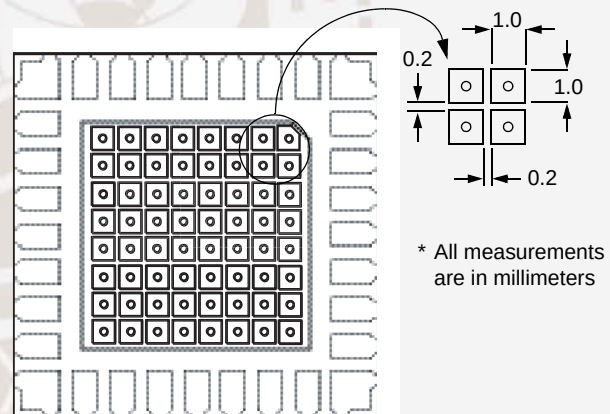


Figure 15. Surface Mount for Power PQFN with Exposed Pads

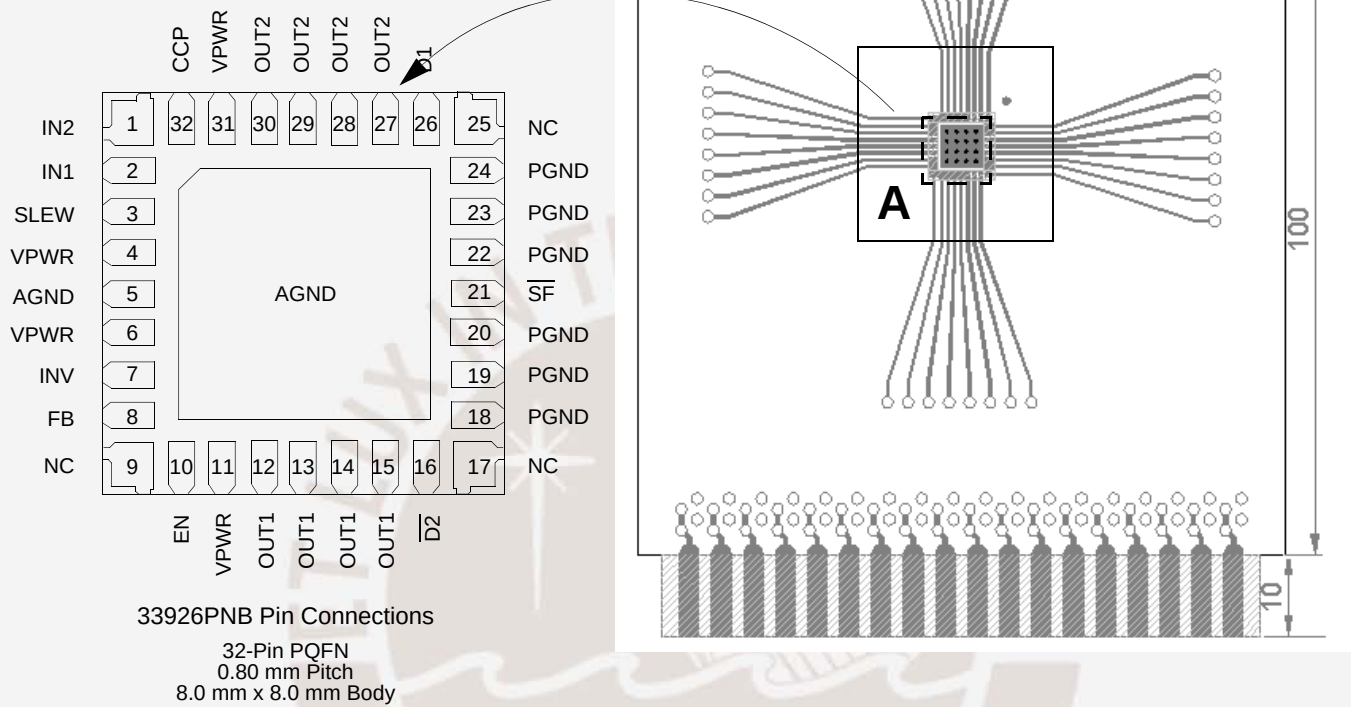


Figure 16. Thermal Test Board

Device on Thermal Test Board

- Material: Single layer printed circuit board
FR4, 1.6 mm thickness
Cu traces, 0.07 mm thickness
- Outline: 80 mm x 100 mm board area,
including edge connector for thermal
testing
- Area A: Cu heat-spreading areas on board
surface
- Ambient Conditions: Natural convection, still air

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

Table 8. Thermal Resistance Performance

A [mm ²]	$R_{\theta JA}$ [°C/W]
0	81
300	49
600	40

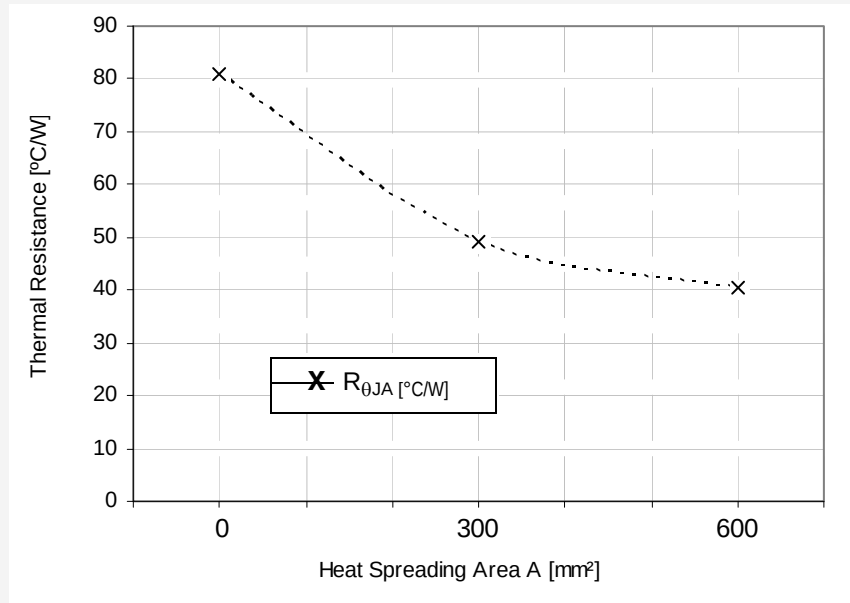


Figure 17. Device on Thermal Test Board $R_{\theta JA}$

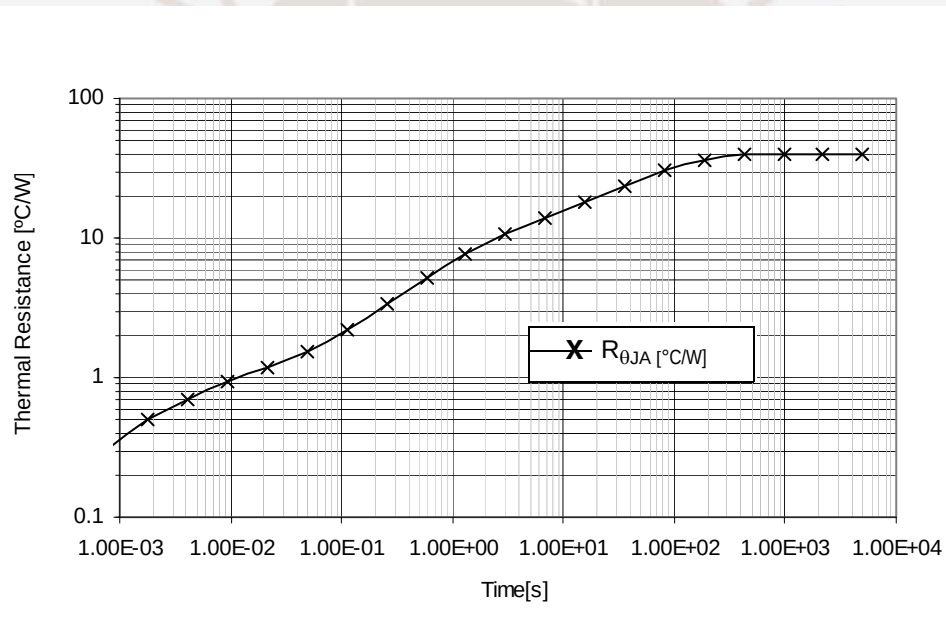


Figure 18. Transient Thermal Resistance $R_{\theta JA}$,
1.0 W Step response, Device on Thermal Test Board Area A = 600 (mm²)

REVISION HISTORY

Revision	Date	Description
1.0	3/2006	• Updated formatting and technical content throughout entire document.
2.0	6/2007	• Updated formatting and technical content throughout entire document
3.0	10/2006	• Updated formatting and technical content throughout entire document
4.0	12/2006	• Updated formatting and technical content throughout entire document
5.0	2/2007	• Updated formatting and technical content throughout entire document
6.0	3/2007	• Changed Human Body Model, Charge Pump Voltage (CP Capacitor = 33 nF), No PWM and PWM = 20kHz, Slew Rate = Fast, Output Rise and Fall Time ⁽²⁷⁾ • Added second paragraph to Positive Power Supply (VPWR) • Added "Low ESR" to 100μF on 33926 Typical Application Schematic
7.0	6/2007	• Changed status to Advance Information
8.0	4/2009	• Minor corrections and clarifications.
9.0	12/2009	• Changed minimum Operating Voltage range from 8.0 to 5.0.
10.0	8/2014	• Updated the overall format to new standards with no change to document content • Added SMARTMOS to the page 1 description. Added application. Moved the ordering information to page 2 • Updated the back page





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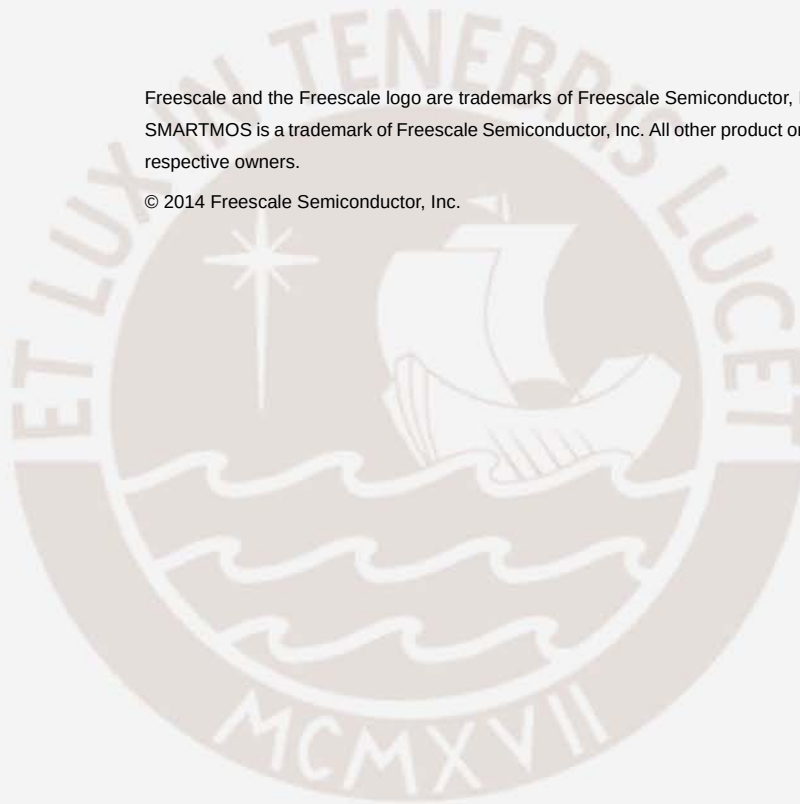
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GLOBALSAT GPS Module

Hardware Data Sheet

Product No : EM-506

User Manual Version 1.4



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Issue Date	APPR	CHECK	PREPARE
2013/10/08	Ray		Mason

Product Description

Product Description

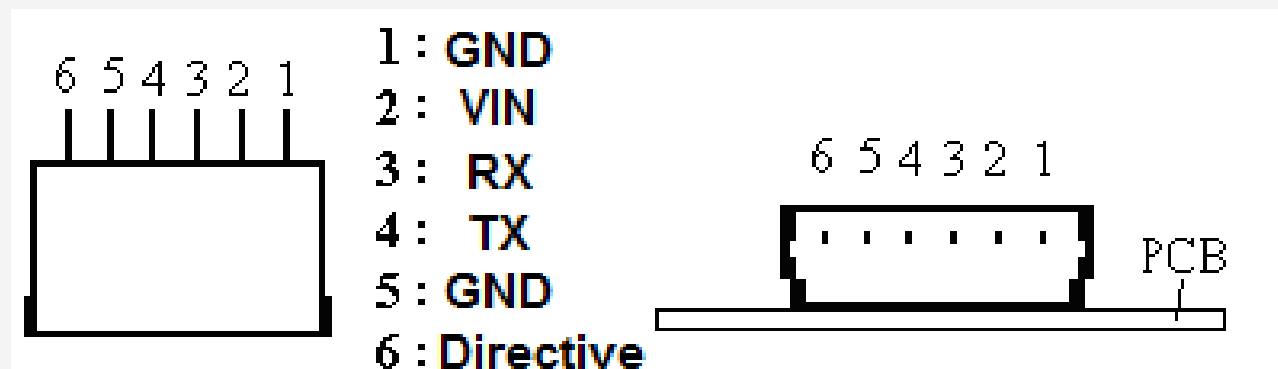
EM-506 GPS module features high sensitivity, low power and ultra small form factor. This GPS module is powered by SiRF Star IV, it can provide you with superior sensitivity and performance even in urban canyon and dense foliage environment. With SiRF CGEE (Client Generated Extended Ephemeris) technology, it predicts satellite positions for up to 3 days and delivers CGEE-start time of less than 15 seconds under most conditions, without any network assistance. Besides, MicroPower Mode allows GPS module to stay in a hot-start condition nearly continuously while consuming very little power. EM-506 is suitable for the following applications:

- Automotive navigation
- Fleet management
- Marine navigation

Product Features

- SiRF Star IV high performance GPS Chipset
- Very high sensitivity (Tracking Sensitivity: -163 dBm)
- Extremely fast TTFF (Time To First Fix) at low signal level
- Support UART interface.
- Built-in LNA(with in CHIP)
- Compact size (30.0mm x 30.0 mm x 10.7mm) suitable for space-sensitive application
- Support NMEA 0183 V3.0 (GGA, GSA, GSV, RMC, VTG, GLL, ZDA)
- Support OSP protocol
- Support SBAS (WASS, EGNOS, MSAS, GAGAN)

Product Pin Description



PIN Number(s)	Name	Type	Description	Note
1,5	GND	P	Ground.	
2	VIN	P	This is the main power supply to the engine board. (4.5Vdc to 6.5Vdc)	
3	RXD	I	This is the main receive channel for receiving software commands to the engine board from SiRFdemo software or from user written software. Baud rate based on flash memory setting.	
4	TXD	O	This is the main transmits channel for outputting navigation and measurement data to user's navigation software or user written software. Output 3.3V level.	
6	Directive	O	This pin indicates the GPS states.	

Electrical Specification

Absolute Maximums Ratings

Parameter	Min.	Typ.	Max.	Conditions	Unit
POWER Supply					
Main power supply(VCC)	4.5	5.0	6.5		V
Main power supply Current	45	50	55	GPS is not 3D Fixed.	mA
	33	34	38	GPS is 3D Fixed.	mA
RF					
Operating Frequency		1.575			Ghz

DC Electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Conditions	Units
I/O Low Level Output Voltage	V _{OL}			0.4		V
I/O High Level Output Voltage	V _{OH}		3.3			V
I/O Low Level Input Voltage	V _{IL}	-0.4		0.45		V
I/O High Level Input Voltage	V _{IH}	1.26		3.6		V
High Level Output Current	I _{OH}		2			mA
Low Level Output Current	I _{OL}		2			mA

Receiver Performance

Sensitivity	Tracking : Autonomous acquisition :	-163dBm -160 dBm
Time-To-First-Fix ¹	Cold Start – Autonomous	< 35s <15s (with CGEE)
	Warm Start – Autonomous ²	< 35s < 15s(with CGEE)
	Hot Start – Autonomous ³	< 1s
Horizontal Position Accuracy ⁴	Autonomous	< 2.5m
Velocity Accuracy ⁵	Speed	< 0.01 m/s
	Heading	< 0.01 degrees
Reacquisition	0.1 second, average	
Update Rate	1 Sec / 5 Sec	
Maximum Altitude	< 18,000 meter	
Maximum Velocity	< 515 meter/ second	
Maximum Acceleration	< 4G	

<Note>

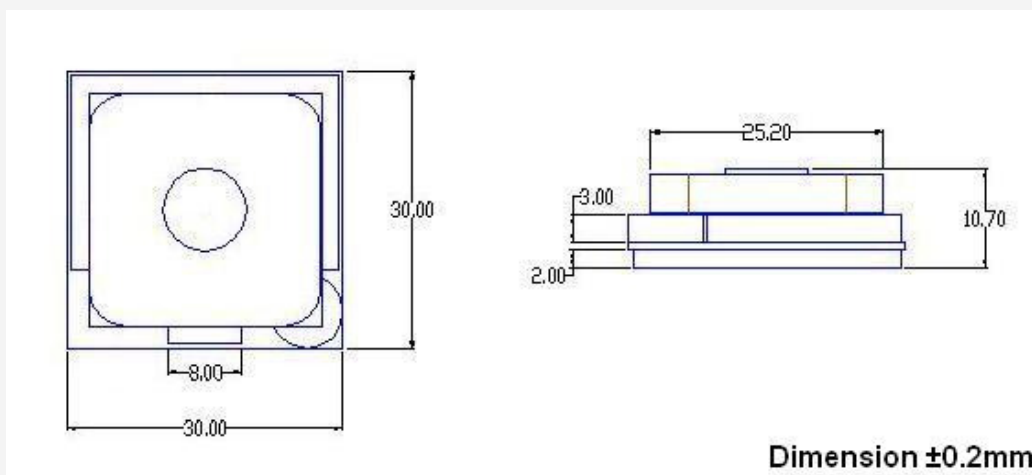
1. 50% -130dBm Fu 0.5ppm Tu ±2s Pu 30Km
2. Commanded **Warm START**
3. Commanded **Hot START**
4. 50% 24hr static, -130dBm
5. 50% @ 30m/s

Environmental Characteristics

Parameter	Min	Typ	Max	Unit
Humidity Range	5		95	% non-condensing
Operation Temperature	-40	25	85	°C
Storage Temperature	-40		85	°C



Physical Characteristic



OPERATING Description

GND

This is Ground pin for the baseband circuit.

VIN

This is the main power supply to the engine board. (4.5Vdc to 6.5Vdc)

RXD

This is the main channel for receiving software commands from SiRFdemo software or from your proprietary software.

TXD

This is the main transmits channel for outputting navigation and measurement data to user's navigation software or user written software. Output is TTL level, 0V ~ 3.3V.

Directive

This pin exports signal to indicate the GPS states.

GPS unfix: always low level.

GPS fixed: one second high level, one second low level.

LED

LED indicator for GPS fix or not fix

LEDOFF: Receiver switch off

LED ON: No fixed, Signal searching

LED Flashing: Position Fixed

SOFTWARE COMMAND

NMEA Output Command

GGA - Global Positioning System Fixed Data

Note – Fields marked in italic **red** apply only to NMEA version 2.3 (and later) in this NMEA message description

Table B-2 contains the values for the following example:

\$GPGGA,161229.487,3723.2475,N,12158.3416,W,1,07,1.0,9.0,M,-34.2,M,,0000*18

Table B-2 GGA Data Format

Name	Example	Units	Description
Message ID	\$GPGGA		GGA protocol header
UTC Time	161229.487		hhmmss.sss
Latitude	3723.2475		ddmm.mmmm
N/S Indicator	N		N=north or S=south
Longitude	12158.3416		dddmm.mmmm
E/W Indicator	W		E=east or W=west
Position Fix Indicator	1		See Table B-3
Satellites Used	07		Range 0 to 12
HDOP	1.0		Horizontal Dilution of Precision
MSL Altitude	9.0	meters	
Units	M	meters	
Geoid Separation ¹	-34.2	meters	Geoid-to-ellipsoid separation. Ellipsoid altitude=MSL Altitude + Geoid Separation
Units	M	meters	
Age of Diff. Corr.		second	Null fields when DGPS is not used
Diff. Ref. Station ID	0000		
Checksum	*18		
<CR><LF>			End of message termination

Table B-3 Position Fix Indicator

Value	Description
0	Fix not available or invalid
1	GPS SPS Mode, fix valid
2	Differential GPS, SPS Mode , fix valid
3	Not supported
6	Dead Reckoning Mode, fix valid

Note:

A valid status is derived from all the parameters set in the software. This includes the minimum

number of satellites required, any DOP mask setting, presence of DGPS corrections, etc. If the default or current software setting requires that a factor is met, then if that factor is not met the solution will be marked as invalid.

GLL - Geographic Position-Latitude/Longitude

Note – Fields marked in italic **red** apply only to NMEA version 2.3 (and later) in this NMEA message description

Table B-4 contains the values for the following example:

\$GPGLL,3723.2475,N,12158.3416,W,161229.487,A,A*41

Table B-4 GLL Data Format

Name	Example	Units	Description
Message ID	\$GPGLL		GLL protocol header
Latitude	3723.2475		ddmm.mmmm
N/S Indicator	n		N=north or S=south
Longitude	12158.3416		dddmm.mmmm
E/W Indicator	W		E=east or W=west
UTC Position	161229.487		hhmmss.sss
Status	A		A=data valid or V=data not valid
Mode	A		A=Autonomous, D=DGPS, E=DR N=Output Data Not Valid R= Coarse Position¹ S=Simulator
Checksum	*41		
<CR><LF>			End of message termination

1. Position was calculated based on one or more of the SVs having their states derived from almanac parameters, as opposed to ephemerides.

GSA - GNSS DOP and Active Satellites

Table B-5 contains the values for the following example:

\$GPGSA,A,3,07,02,26,27,09,04,15,,,,,1.8,1.0,1.5*33

Table B-5 GSA Data Format

Name	Example	Units	Description
Message ID	\$GPGSA		GSA protocol header
Mode 1	A		See Table B-6
Mode 2	3		See Table B-7
Satellite Used ¹	07		Sv on Channel 1
Satellite Used ¹	02		Sv on Channel 2
.....			
Satellite Used ¹			Sv on Channel 12
PDOP ²	1.8		Position dilution of Precision
HDOP ²	1.0		Horizontal dilution of Precision
VDOP ²	1.5		Vertical dilution of Precision
Checksum	*33		
<CR><LF>			End of message termination

1. Satellite used in solution.
2. Maximum DOP value reported is 50. When 50 is reported, the actual DOP may be much larger.

Table B-6 Mode1

Value	Description
M	Manual-forced to operate in 2D or 3D mode
A	2D automatic-allowed to automatically switch 2

Table B-7 Mode 2

Value	Description
1	Fix Not Available
2	2D (<4 SVs used)
3	3D (>3 SVs used)

GSV - GNSS Satellites in View

Table B-8 contains the values for the following example:

\$GPGSV,2,1,07,07,79,048,42,02,51,062,43,26,36,256,42,27,27,138,42*71

\$GPGSV,2,2,07,09,23,313,42,04,19,159,41,15,12,041,42*41

Table B-8 GSV Data Format

Name	Example	Units	Description
Message ID	\$GPGSV		GSV protocol header
Number of Messages ¹	2		Range 1 to 3
Message Number ¹	1		Range 1 to 3
Satellites in View ¹	07		
Satellite ID	07		Channel 1(Range 1 to 32)
Elevation	79	degrees	Channel 1(Maximum90)
Azimuth	048	degrees	Channel 1(True, Range 0 to 359)
SNR(C/No)	42	dBHz	Range 0 to 99,null when not tracking
.....			
Satellite ID	27		Channel 4 (Range 1 to 32)
Elevation	27	Degrees	Channel 4(Maximum90)
Azimuth	138	Degrees	Channel 4(True, Range 0 to 359)
SNR(C/No)	42	dBHz	Range 0 to 99,null when not tracking
Checksum	*71		
<CR><LF>			End of message termination

1. Depending on the number of satellites tracked, multiple messages of GSV data may be required. In some software versions, the maximum number of satellites reported as visible is limited to 12, even though more may be visible.

RMC - Recommended Minimum Specific GNSS Data

Note – Fields marked in italic **red** apply only to NMEA version 2.3 (and later) in this NMEA message description

Table B-9 contains the values for the following example:

\$GPRMC,161229.487,A,3723.2475,N,12158.3416,W,0.13,309.62,120598,,,A*10

Table B-9 RMC Data Format

Name	Example	Units	Description
Message ID	\$GPRMC		RMC protocol header
UTC Time	161229.487		hhmmss.sss
Status ¹	A		A=data valid or V=data not valid
Latitude	3723.2475		ddmm.mmmm
N/S Indicator	N		N=north or S=south
Longitude	12158.3416		dddmm.mmmm
E/W Indicator	W		E=east or W=west
Speed Over Ground	0.13	knots	
Course Over Ground	309.62	degrees	True
Date	120598		ddmmyy
Magnetic Variation ²		degrees	E=east or W=west
East/West Indicator ²	E		E=east
Mode	A		A=Autonomous, D=DGPS, E=DR N=Output Data Not Valid R= Coarse Position³ S=Simulator
Checksum	*10		
<CR><LF>			End of message termination

1. A valid status is derived from all the parameters set in the software. This includes the minimum number of satellites required, any DOP mask setting, presence of DGPS corrections, etc. If the default or current software setting requires that a factor is met, then if that factor is not met the solution will be marked as invalid.
2. SiRF Technology Inc. does not support magnetic declination. All “course over ground” data are geodetic WGS84 directions relative to true North.
3. Position was calculated based on one or more of the SVs having their states derived from almanac parameters, as opposed to ephemerides.

VTG - Course Over Ground and Ground Speed

Note – Fields marked in italic **red** apply only to NMEA version 2.3 (and later) in this NMEA message description

Table B-10 contains the values for the following example:

\$GPVTG,309.62,T,,M,0.13,N,0.2,K,A*23

Table B-10 VTG Data Format

Name	Example	Units	Description
Message ID	\$GPVTG		VTG protocol header
Course	309.62	degrees	Measured heading
Reference	T		True
Course		degrees	Measured heading
Reference	M		Magnetic ¹
Speed	0.13	knots	Measured horizontal speed
Units	N		Knots
Speed	0.2	Km/hr	Measured horizontal speed
Units	K		Kilometers per hour
Mode	A		A=Autonomous, D=DGPS, E=DR N=Output Data Not Valid R= Coarse Position² S=Simulator
Checksum	*23		
<CR><LF>			End of message termination

1. SiRF Technology Inc. does not support magnetic declination. All “course over ground” data are geodetic WGS84 directions.
2. Position was calculated based on one or more of the SVs having their states derived from almanac parameters, as opposed to ephemerides.

ZDA - Time and Date

This message is included only with systems which support a time-mark output pulse identified as "1PPS". Outputs the time associated with the current 1PPS pulse. Each message is output within a few hundred ms after the 1PPS pulse is output and tells the time of the pulse that just occurred.

Table B-11 contains the values for the following example:

\$GPZDA,181813,14,10,2003,,*4F<CR><LF>

Table B-11: ZDA Data Format

Name	Example	Unit	Description
Message ID	\$GPZDA		ZDA protocol header
UTC Time	181813	hhmmss	The UTC time units are: hh=UTC hours from 00 to 23 mm=UTC minutes from 00 to 59 ss=UTC seconds from 00 to 59 Either using valid IONO/UTC or estimated from default leap seconds
Day	14		Day of the month, range 1 to 31
Month	10		Month of the year, range 1 to 12
Year	2003		Year
Local zone hour ¹		hour	Offset from UTC (set to 00)
Local zone minutes ¹		minute	Offset from UTC (set to 00)
Checksum	*4F		
<CR><LF>			End of message termination

1. Not supported by CSR, reported as 00.

NMEA Input Command

A). Set Serial Port ID: 100 Set PORTA parameters and protocol

This command message is used to set the protocol (SiRF Binary, NMEA, or USER1) and/or the communication parameters (baud, data bits, stop bits, parity). Generally, this command would be used to switch the module back to SiRF Binary protocol mode where a more extensive command message set is available. For example, to change navigation parameters. When a valid message is received, the parameters will be stored in battery backed SRAM and then the receiver will restart using the saved parameters.

Format:

\$PSRF100,<protocol>,<baud>,<DataBits>,<StopBits>,<Parity>*CKSUM<CR><LF>

<protocol>	0=SiRF Binary, 1=NMEA, 4=USER1
<baud>	1200, 2400, 4800, 9600, 19200, 38400
<DataBits>	8,7. Note that SiRF protocol is only valid f8 Data bits
<StopBits>	0,1
<Parity>	0=None, 1=Odd, 2=Even

Example 1: Switch to SiRF Binary protocol at 9600,8,N,1

\$PSRF100,0,9600,8,1,0*0C<CR><LF>

Example 2: Switch to User1 protocol at 38400,8,N,1

\$PSRF100,4,38400,8,1,0*38<CR><LF>

****Checksum Field:** The absolute value calculated by exclusive-OR the 8 data bits of each character in the Sentence, between, but excluding "\$" and "**". The hexadecimal value of the most significant and least significant 4 bits of the result are converted to two ASCII characters (0-9, A-F) for transmission. The most significant character is transmitted first.

****<CR><LF>** : Hex 0D 0A

B). Navigation Initialization ID : 101 Parameters required for start

This command is used to initialize the module for a warm start, by providing current position (in X, Y, Z coordinates), clock offset, and time. This enables the receiver to search for the correct satellite signals at the correct signal parameters. Correct initialization parameters will enable the receiver to acquire signals more quickly, and thus, produce a faster navigational solution.

When a valid Navigation Initialization command is received, the receiver will restart using the input parameters as a basis for satellite selection and acquisition.

Format :

\$PSRF101,<X>,<Y>,<Z>,<ClkOffset>,<TimeOfWeek>,<WeekNo>,<chnlCount>,<ResetCfg>*CK
SUM<CR><LF>

<X>	X coordinate position INT32
<Y>	Y coordinate position INT32
<Z>	Z coordinate position INT32
<ClkOffset>	Clock offset of the receiver in Hz, Use 0 for last saved value if available. If this is unavailable, a default value of 75000 for GSP1, 95000 for GSP 1/LX will be used. INT32
<TimeOf Week>	GPS Time Of Week UINT32
<WeekNo>	GPS Week Number UINT16 (Week No and Time Of Week calculation from UTC time)
<chnlCount>	Number of channels to use.1-12. If your CPU throughput is not high enough, you could decrease needed throughput by reducing the number of active channels UBYTE
<ResetCfg>	bit mask 0x01=Data Valid warm/hot start=1 0x02=clear ephemeris warm start=1 0x04=clear memory. Cold start=1 UBYTE

Example: Start using known position and time.

\$PSRF101,-2686700,-4304200,3851624,96000,497260,921,12,3*7F

C). Set DGPS Port ID: 102 Set PORT B parameters for DGPS input

This command is used to control Serial Port B that is an input only serial port used to receive RTCM differential corrections.

Differential receivers may output corrections using different communication parameters. The default communication parameters for PORT B are 9600Baud, 8data bits, 0 stop bits, and no parity. If a DGPS receiver is used which has different communication parameters, use this command to allow the receiver to correctly decode the data. When a valid message is received, the parameters will be stored in battery backed SRAM and then the receiver will restart using the saved parameters.

Format:

\$ PSRF102,<Baud>,<DataBits>,<StopBits>,<Parity>*CKSUM<CR><LF>

<baud>	1200,2400,4800,9600,19200,38400
<DataBits>	8
<StopBits>	0,1
<Parity>	0=None, Odd=1,Even=2

Example: Set DGPS Port to be 9600,8,N,1

\$ PSRF102,9600,8,1.0*12

D). Query/Rate Control ID: 103 Query standard NMEA message and/or set output rate

This command is used to control the output of standard NMEA message GGA, GLL, GSA, GSV, RMC, VTG. Using this command message, standard NMEA message may be polled once, or setup for periodic output. Checksums may also be enabled or disabled depending on the needs of the receiving program. NMEA message settings are saved in battery backed memory for each entry when the message is accepted.

Format:

\$ PSRF103,<msg>,<mode>,<rate>,<cksumEnable>*CKSUM<CR><LF>

<msg>	0=GGA, 1=GLL, 2=GSA, 3=GSV, 4=RMC, 5=VTG 6=MSS(if internal beacon is supported) 7=Not defined 8=ZDA(if 1PPS output supported) 9=Not defined
<mode>	0=SetRate 1=Query 2=ABP On 3=ABP Off
<rate>	Output every <rate>seconds, off=0,max=255
<cksumEnable>	0=disable Checksum,1=Enable checksum for specified message

Example 1: Query the GGA message with checksum enabled

\$ PSRF103,00,01,00,01*25

Example 2: Enable VTG message for a 1Hz constant output with checksum enabled

\$ PSRF103,05,00,01,01*20

Example 3: Disable VTG message

\$ PSRF103,05,00,00,01*21

E). LLA Navigation Initialization ID: 104 Parameters required to start using Lat/Lon/Alt

This command is used to initialize the module for a warm start, by providing current position (in Latitude, Longitude, Altitude coordinates), clock offset, and time. This enables the receiver to search for the correct satellite signals at the correct signal parameters. Correct initialization parameters will enable the receiver to acquire signals more quickly, and thus, will produce a faster navigational solution.

When a valid LLA Navigation Initialization command is received, the receiver will restart using the input parameters as a basis for satellite selection and acquisition.

Format:

\$ PSRF104,<Lat>,<Lon>,<Alt>,<ClkOffset>,<TimeOfWeek>,<WeekNo>,<ChannelCount>,<ResetCfg>*CKSUM<CR><LF>

<Lat>	Latitude position, assumed positive north of equator and negative south of equator float, possibly signed
<Lon>	Longitude position, it is assumed positive east of Greenwich and negative west of Greenwich Float, possibly signed
<Alt>	Altitude position float, possibly signed
<ClkOffset>	Clock Offset of the receiver in Hz, use 0 for last saved value if available. If this is unavailable, a default value of 75000 for GSP1, 95000 for GSP1/LX will be used. INT32
<TimeOfWeek>	GPS Time Of Week UINT32
<WeekNo>	GPS Week Number UINT16
<ChannelCount>	Number of channels to use. 1-12 UBYTE
<ResetCfg>	bit mask 0x01=Data Valid warm/hot starts=1 0x02=clear ephemeris warm start=1 0x04=clear memory. Cold start=1 UBYTE

Example: Start using known position and time.

\$ PSRF104,37.3875111,-121.97232,0,96000,237759,922,12,3*37

F). Development Data On/Off ID: 105 Switch Development Data Messages On/Off

Use this command to enable development debug information if you are having trouble getting commands accepted. Invalid commands will generate debug information that should enable the user to determine the source of the command rejection. Common reasons for input command rejection are invalid checksum or parameter out of specified range. This setting is not preserved across a module reset.

Format: \$PSRF105,<debug>*CKSUM<CR><LF>

<debug> 0=Off, 1=On

Example: Debug On \$PSRF105,1*3E

Example: Debug Off \$PSRF105,0*3F

G). Select Datum ID: 106 Selection of datum to be used for coordinate Transformations

GPS receivers perform initial position and velocity calculations using an earth-centered earth-fixed (ECEF) coordinate system. Results may be converted to an earth model (geoid) defined by the selected datum. The default datum is WGS 84 (World Geodetic System 1984) which provides a worldwide common grid system that may be translated into local coordinate systems or map datums. (Local map datums are a best fit to the local shape of the earth and not valid worldwide.)

Examples:

Datum select TOKYO_MEAN

\$PSRF106,178*32

Name	Example	Unit	Description
Message ID	\$PSRF106		PSRF106 protocol header
Datum	178		21=WGS84 178=TOKYO_MEAN 179=TOKYO_JAPAN 180=TOKYO_KOREA 181=TOKYO_OKINAWA Debug
Checksum	*32		
<CR><LF>			End of message termination

RoHS / Lead Free Compliance



Globalsat WorldCom Corporation

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RoHS / Lead Free Compliance

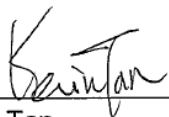
Dear Sales:

This letter is intended to answer questions you may come across regarding the compliance of Globalsat WorldCom Corporation products with the following European Directive 2011/65/EU (RoHS) :

- Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) .

This Directive aim is to avoid or limit the use of hazardous material compliant and meet the Standard by July.16,2011 of less than "0.1% by weight per homogeneous material for lead,hexavalent chromium,mercury, PBB and PBDE and 0.01% by weight and per homogeneous material for cadmium".

Globalsat has incorporated the requirement of 2011/65/EU into the product / technology development roadmaps and is committed to make lead free / RoHS fully compliant product available for shipment by July.16,2011.



Kevin Tan
Quality Assurance Manager



Prince Cheng
Chief Executive Officer (CEO)

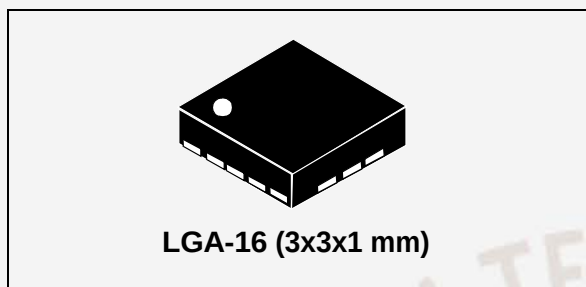
Reversion history

Reversion	Date	Name	Status / Comments
V1.1	20120320	Luwalk	Initial Version
V1.2	20130521	Mason	Modify VCC range
V1.3	20130724	Mason	1.Modify Pin define 2.Modify DC electrical characteristics
V1.4	20131008	Mason	Modify pin 1PPS to Directive



MEMS motion sensor: three-axis digital output gyroscope

Datasheet - production data



Features

- Wide supply voltage, 2.2 V to 3.6 V
- Wide extended operating temperature range (from -40 °C to 85 °C)
- Low voltage compatible IOs, 1.8 V
- Low power consumption
- Embedded power-down
- Sleep mode
- Fast turn-on and wake-up
- Three selectable full scales up to 2000 dps
- 16 bit rate value data output
- 8 bit temperature data output
- I²C/SPI digital output interface
- 2 dedicated lines (1 interrupt, 1 data ready)
- User enable integrated high-pass filters
- Embedded temperature sensor
- Embedded 32 levels of 16 bit data output FIFO
- High shock survivability
- ECOPACK[®] RoHS and "Green" compliant

Applications

- Gaming and virtual reality input devices
- Motion control with MMI (man-machine interface)
- GPS navigation systems
- Appliances and robotics

Description

The L3GD20H is a low-power three-axis angular rate sensor.

It includes a sensing element and an IC interface able to provide the measured angular rate to the external world through digital interface (I²C/SPI).

The sensing element is manufactured using a dedicated micromachining process developed by ST to produce inertial sensors and actuators on silicon wafers.

The IC interface is manufactured using a CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The L3GD20H has a full scale of $\pm 245/\pm 500/\pm 2000$ dps and is capable of measuring rates with a user selectable bandwidth.

The L3GD20H is available in a plastic land grid array (LGA) package and can operate within a temperature range from -40 °C to +85 °C.

Table 1. Device summary

Order code	Temperature range (°C)	Package	Packing
L3GD20H	-40 to +85	LGA-16 (3x3x1)	Tray
L3GD20HTR	-40 to +85	LGA-16 (3x3x1)	Tape and reel

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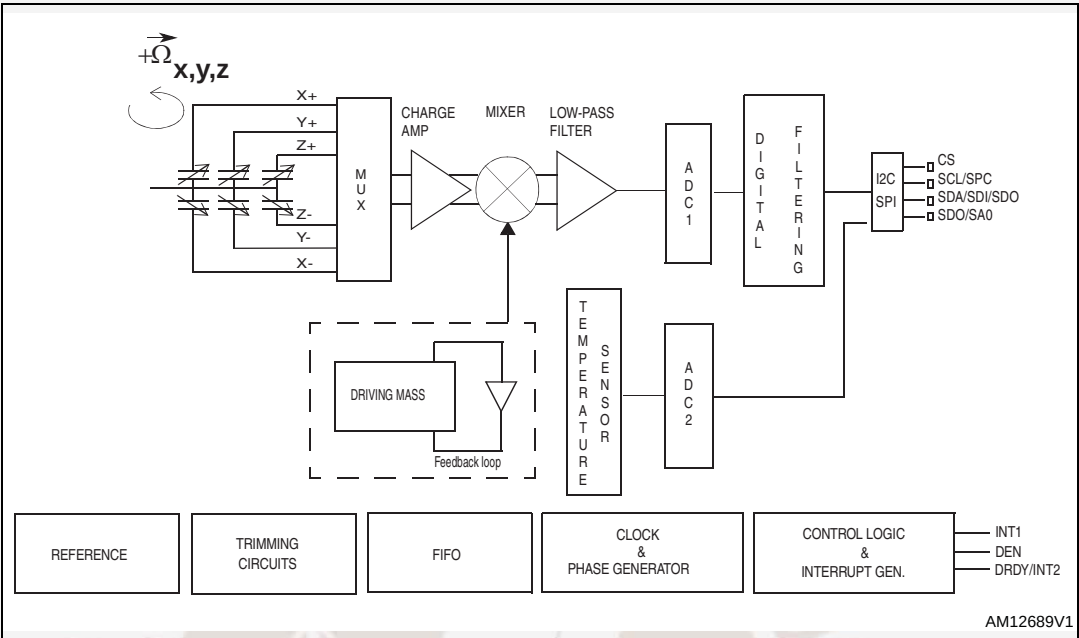


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1 Block diagram and pin description

Figure 1. Block diagram



The vibration of the structure is maintained by a drive circuitry in a feedback loop. The sensing signal is filtered and appears as digital signal at the output.

1.1 Pin description

Figure 2. Pin connection

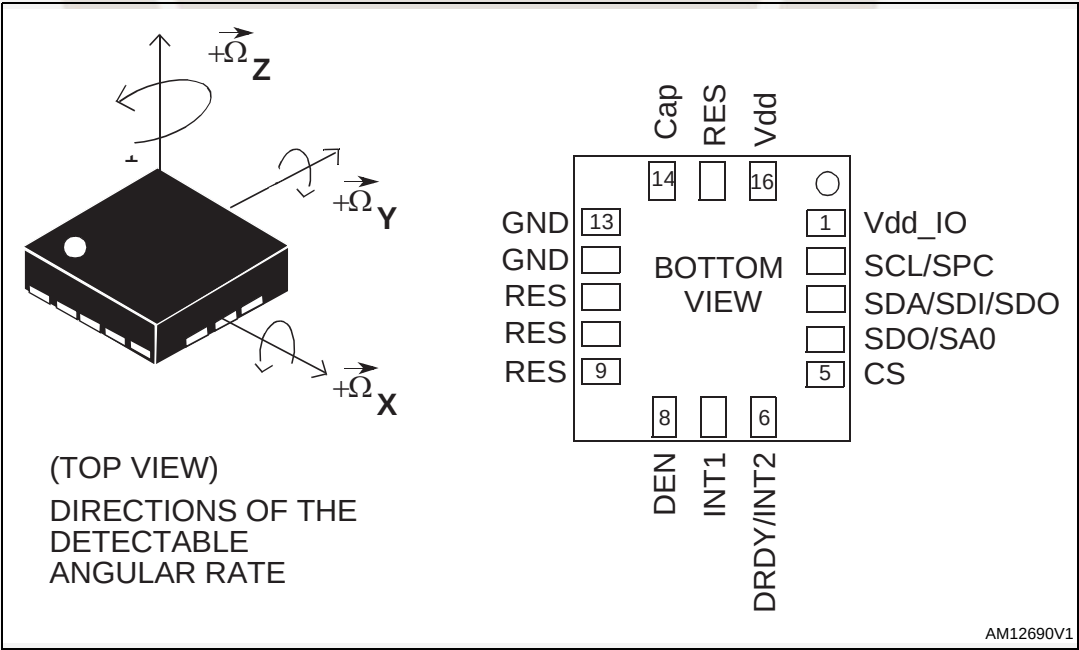


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO ⁽¹⁾	Power supply for I/O pins
2	SCL SPC	I ² C serial clock (SCL) SPI serial port clock (SPC)
3	SDA SDI SDO	I ² C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
4	SDO SA0	SPI serial data output (SDO) I ² C less significant bit of the device address (SA0)
5	CS	I ² C/SPI mode selection (1: SPI idle mode / I ² C communication enabled; 0: SPI communication mode / I ² C disabled)
6	DRDY/INT2	Data ready/fifo interrupt (FIFO threshold/overflow/empty)
7	INT1	Programmable interrupt
8	DEN ⁽²⁾	Gyroscope data enable
9	Reserved	Connect to GND
10	Reserved	Connect to GND
11	Reserved	Connect to GND or VDD
12	GND	0 V supply
13	GND	0 V supply
14	Cap	Connect to GND with ceramic capacitor ⁽³⁾
15	Reserved	Connect to GND or VDD
16	Vdd ⁽⁴⁾	Power supply

1. Recommended 100 nF filter capacitor.

2. Connected to GND if DEN is not used.

3. 10 nF (+/-10%), 25 V. 1 nF minimum value has to be guaranteed under 12 V bias condition.

4. Recommended 100 nF plus 10 µF capacitors.

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

@ Vdd = 3.0 V, T = 25 °C unless otherwise noted^(a).

Table 3. Mechanical characteristics

Symbol	Parameter	Test condition	Min.	Typ. ⁽¹⁾	Max.	Unit
FS	Measurement range	User selectable		±245 ±500 ±2000		dps
So	Sensitivity			8.75 17.50 70.00		mdps/digit
SoDr	Sensitivity change vs. temperature ⁽²⁾	From -40 °C to +85 °C Delta from T = 25 °C		±2		%
DVoff	Digital Zero-rate level	FS = 2000 dps		±25		dps
OffDr	Zero-rate level change vs temperature ⁽³⁾	FS = 2000 dps		±0.04		dps/°C
NL	Non linearity ⁽³⁾	Best fit straight line		0.2		% FS
Rn	Rate noise density ⁽³⁾	BW = 50 Hz		0.011		dps/(√Hz)
ODR	Digital output data rate ⁽³⁾			11.9/23.7/ 47.3/94.7/ 189.4/ 378.8/ 757.6		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.

2. Guaranteed by design.

3. The period (1/ODR), length of time between two consecutive sampling, must be derived by the reciprocal of the maximum. and minimum ODR limits: for example for ODR = 189.4 Hz, sampling period range will be within [4591 μs, 6211 μs] (where ODR minimum and maximum have been approximated at 162 Hz, 219 Hz respectively).

a. The product is factory calibrated at 3.0 V. The operational power supply range is specified in [Table 4](#).

2.2 Electrical characteristics

@ Vdd = 3.0 V, T = 25 °C unless otherwise noted^(b).

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ. ⁽¹⁾	Max.	Unit
Vdd	Supply voltage		2.2	3.0	3.6	V
Vdd_IO	I/O pins supply voltage ⁽²⁾		1.71		Vdd+0.1	V
Idd	Supply current			5.0		mA
IddSL	Supply current in sleep mode ⁽³⁾	Selectable by digital interface		2.5		mA
IddPdn	Supply current in power-down mode	Selectable by digital interface		1		μA
VIH	Digital high level input voltage		0.8*Vdd_IO			V
VIL	Digital low level input voltage				0.2*Vdd_IO	V
Ton	Turn-on time ⁽⁴⁾	LPF2 disabled ODR = 190 Hz		50		ms
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses, in this condition the measurement chain is powered off.
3. Sleep mode introduces a faster turn-on time related to power down mode.
4. Time to obtain stable sensitivity (within ±5% of final value) after exiting power-down mode. It is guaranteed by design.

b. The product is factory calibrated at 3.0 V.

2.3 Temperature sensor characteristics

@ Vdd =3.0 V, T=25 °C unless otherwise noted^(c).

Table 5. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ. ⁽¹⁾	Max.	Unit
TSDr	Temperature sensor output change vs temperature	-		-1		°C/digit
TODR	Temperature refresh rate			1		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.



c. The product is factory calibrated at 3.0 V.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

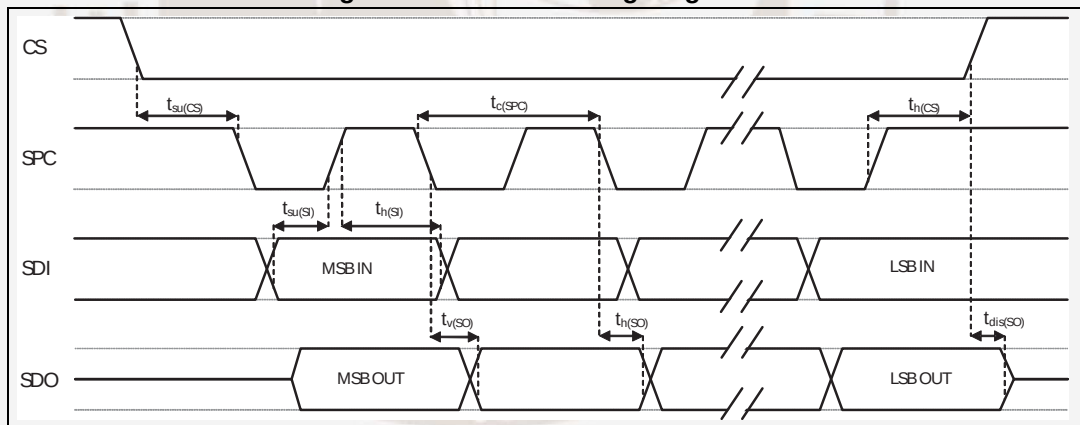
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value ⁽¹⁾		Unit
		Min.	Max.	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	5		ns
th(CS)	CS hold time	20		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	5		
tdis(SO)	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram^(d)



- d. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both Input and Output port.

2.4.2 I²C - Inter IC control interface

Subject to general operating conditions for V_{DD} and T_{OP}.

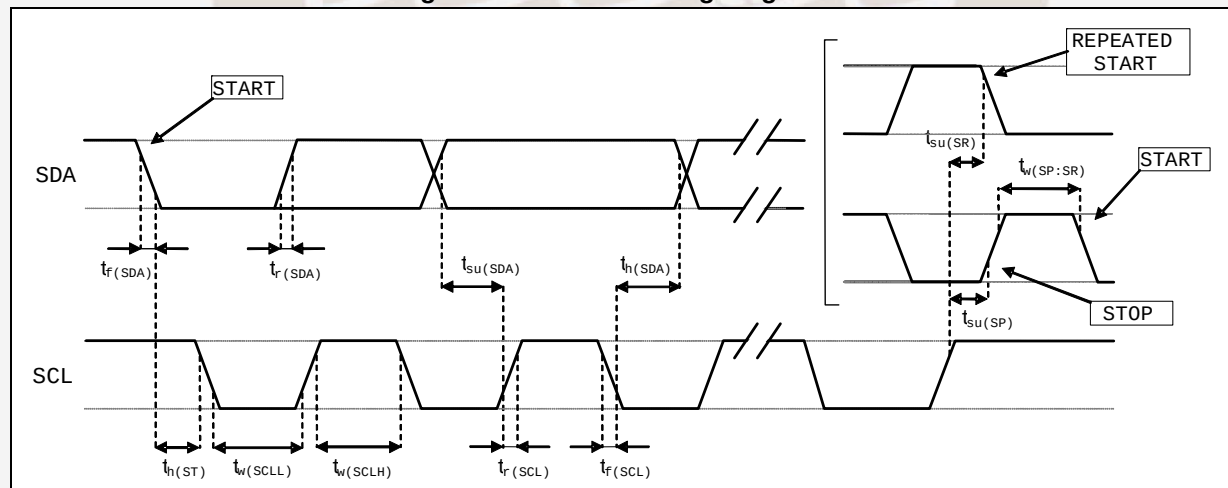
Table 7. I²C slave timing values

Symbol	Parameter	I ² C standard mode ⁽¹⁾		I ² C fast mode ⁽¹⁾		Unit
		Min.	Max.	Min.	Max.	
f _(SCL)	SCL clock frequency	0	100	0	400	kHz
t _{w(SCLL)}	SCL clock low time	4.7		1.3		μs
t _{w(SCLH)}	SCL clock high time	4.0		0.6		
t _{su(SDA)}	SDA setup time	250		100		ns
t _{h(SDA)}	SDA data hold time	0	3.45	0	0.9	μs
t _{r(SDA)} t _{r(SCL)}	SDA and SCL rise time		1000	20 + 0.1C _b ⁽²⁾	300	ns
t _{f(SDA)} t _{f(SCL)}	SDA and SCL fall time		300	20 + 0.1C _b ⁽²⁾	300	
t _{h(ST)}	START condition hold time	4		0.6		μs
t _{su(SR)}	Repeated START condition setup time	4.7		0.6		
t _{su(SP)}	STOP condition setup time	4		0.6		
t _{w(SP:SR)}	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.

2. C_b = total capacitance of one bus line, in pF.

Figure 4. I²C slave timing diagram^(e)



e. Measurement points are done at 0.2·V_{DD_IO} and 0.8·V_{DD_IO}, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
T _{STG}	Storage temperature range	-40 to +125	°C
Sg	Acceleration g for 0.1 ms	10,000	g
ESD	Electrostatic discharge protection	2 (HBM)	kV
Vin	Input voltage on any control pin (including CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0, DEN)	0.3 to Vdd_IO +0.3	V

Note: Supply voltage on any pin should never exceed 4.8 V.



This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part.



This is an ESD sensitive device, improper handling can cause permanent damage to the part.

2.6 Terminology

2.6.1 Sensitivity

An angular rate gyroscope is a device that produces a positive-going analog output for counterclockwise rotation around the sensitive axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

2.6.2 Zero-rate level

Zero-rate level describes the actual output signal if there is no angular rate present. Zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress.

2.7 Soldering information

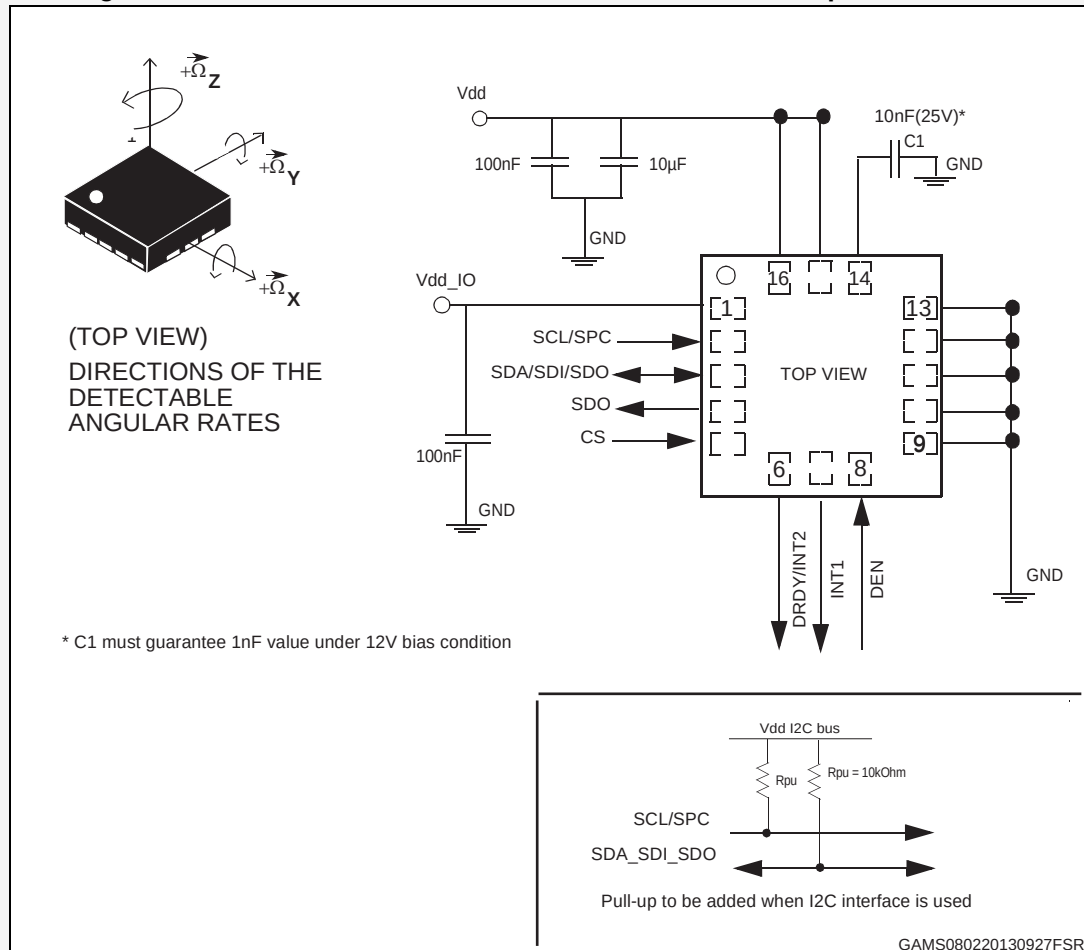
The LGA package is compliant with the ECOPACK[®], RoHS and “Green” standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

3 Application hints

Figure 5. L3GD20H electrical connections and external components values



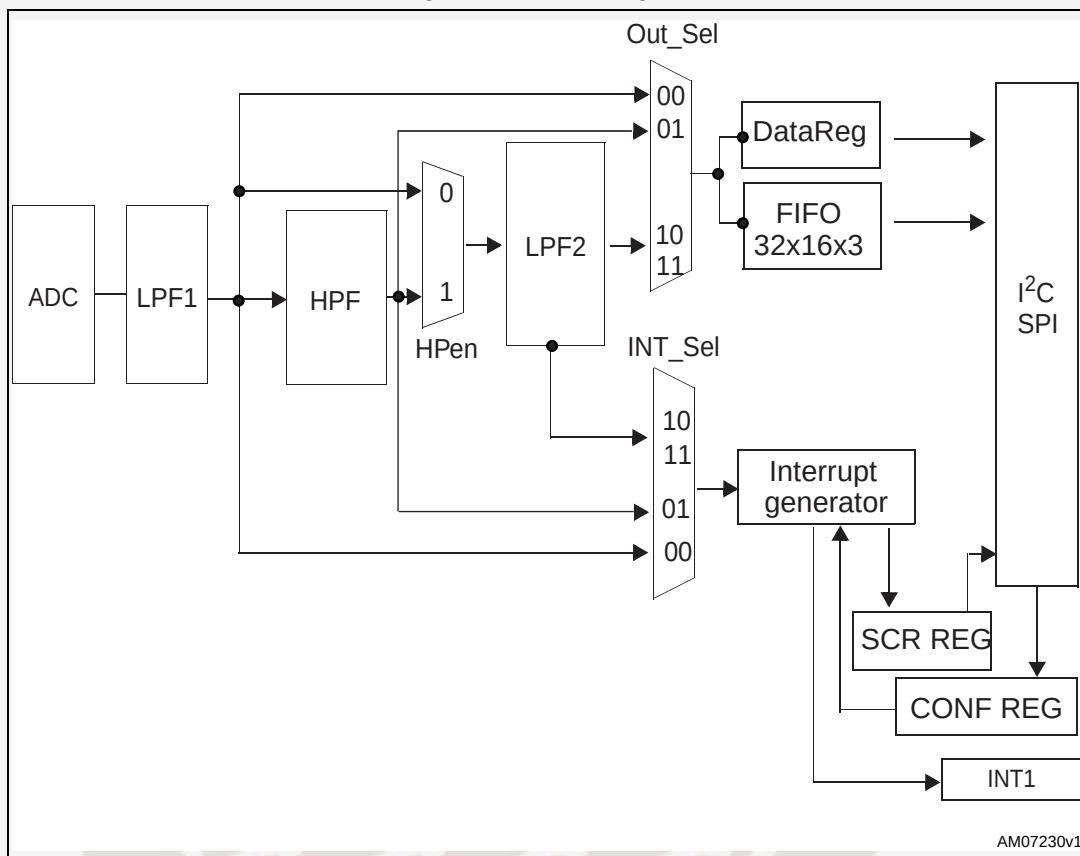
Power supply decoupling capacitors (100 nF + 10 μ F) should be placed as near as possible to the device (common design practice).

If Vdd and Vdd_IO are not connected together, 100 nF and 10 μ F decoupling capacitors must be placed between Vdd and common ground while 100 nF between Vdd_IO and common ground. Capacitors should be placed as near as possible to the device (common design practice).

4 Digital main blocks

4.1 Block diagram

Figure 6. Block diagram



4.2 FIFO

L3GD20H embeds 32 slots of 16-bit data FIFO for each of the three output channels: yaw, pitch and roll. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wakeup only when needed and burst the significant data out from the FIFO. This buffer can work accordingly to seven different modes: Bypass mode, FIFO-mode, Stream mode, Stream-to-FIFO mode, Bypass-to-Stream, Dynamic-Stream, Bypass-to-FIFO. Each mode is selected by the FM2:0 bits in FIFO_CTRL register. Programmable FIFO threshold level, FIFO empty or FIFO overrun events are available on FIFO_SRC register and can be set to generate dedicated interrupts on DRDY/INT2 pin.

FIFO_SRC(EMPTY) is equal to '1' when no samples are available.

FIFO_SRC(FTH) goes to '1' if a new data arrives and FIFO_SRC(FSS4:0) is greater than or equal to FIFO Threshold configured to FTH4:0 into FIFO_CTRL (2Eh). FIFO_SRC(FTH) goes to '0' if reading Yaw, Pitch and Roll data slot from FIFO and FIFO_SRC(FSS4:0) is minor than or equal to FIFO_CTRL(FTH4:0).

FIFO_SRC(OVRN) is equal to '1' if a FIFO slot is overwritten.

FIFO feature is enabled writing to '1' CTRL5(FIFO_EN).

To guarantee the switching into and out of FIFO mode discard the first sample acquired.

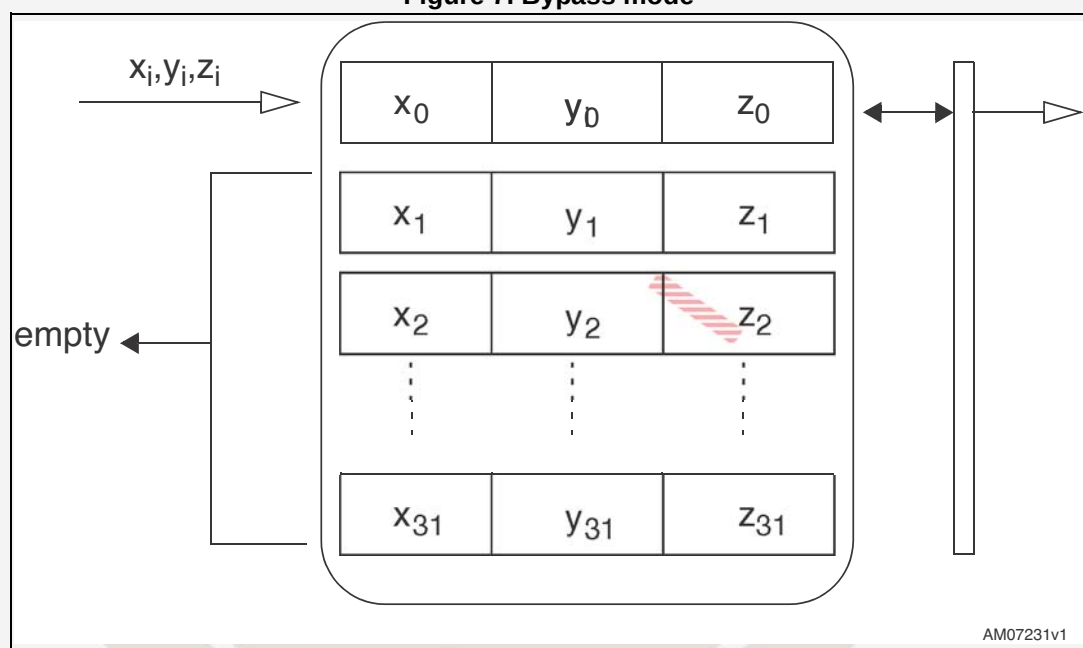
4.2.1 Bypass mode

In bypass mode (FIFO_CTRL(FM2:0) = 000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO-mode.

As described in the next figure, for each channel only the first address is used. When a new data is available the old one is overwritten.

Figure 7. Bypass mode



4.2.2 FIFO mode

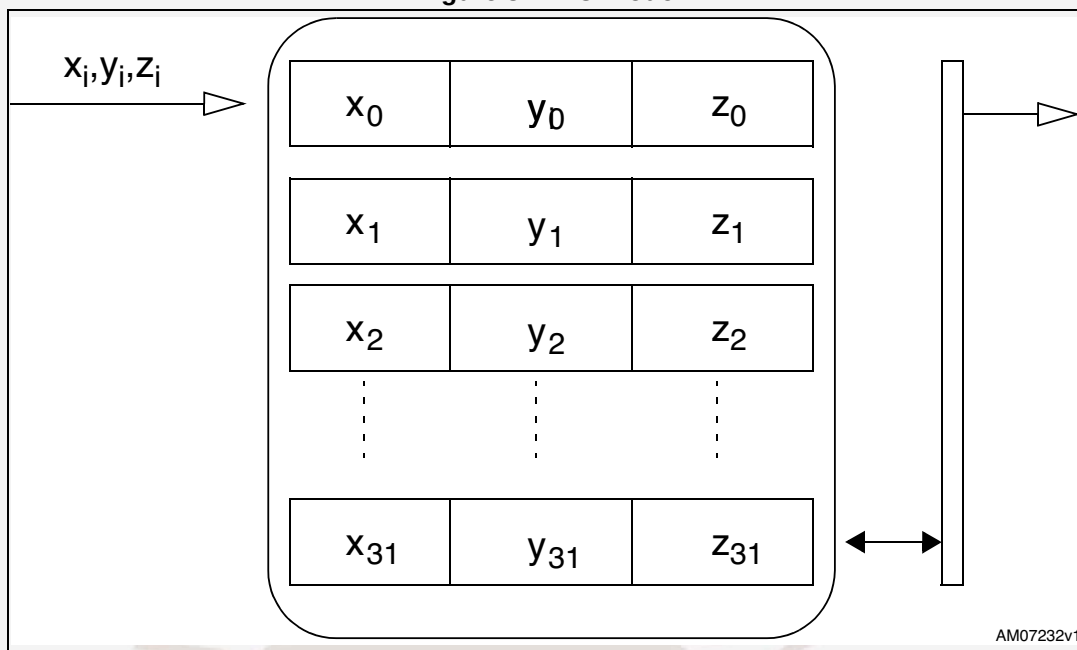
In FIFO mode (FIFO_CTRL(FM2:0) = 001) data from Yaw, Pitch and Roll channels are stored into the FIFO until it is full.

To reset FIFO content Bypass mode should be written in FIFO_CTRL(FM2:0) '000' value. After this reset command it is possible to restart FIFO mode writing FIFO_CTRL(FM2:0) the value '001'.

FIFO buffer can memorize 32 Yaw, Pitch and Roll data, but the depth of the FIFO can be reduced by means of CTRL5(StopOnFTH) bit setting to '1' StopOnFTH bit, FIFO depth is limited to FIFO_CTRL(FTH4:0) - 1.

A FIFO Threshold interrupt can be enabled (INT2_ORun bit into CTRL3 (22h)) in order to be raised when the FIFO is filled to the level specified into the FTH4:0 bits of FIFO_CTRL (2Eh). When FIFO Threshold interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input channels.

Figure 8. FIFO mode

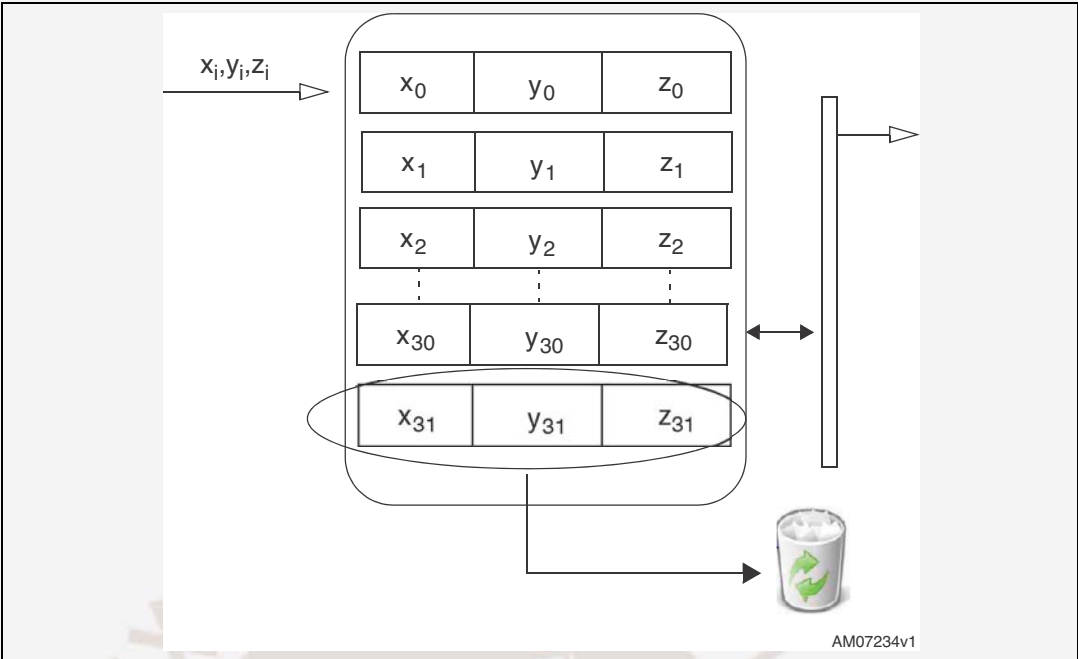


4.2.3 Stream mode - dynamic stream

Stream mode (FIFO_CTRL(FM2:0) = 010) provides continuous FIFO update: as new data arrives the older is discarded.

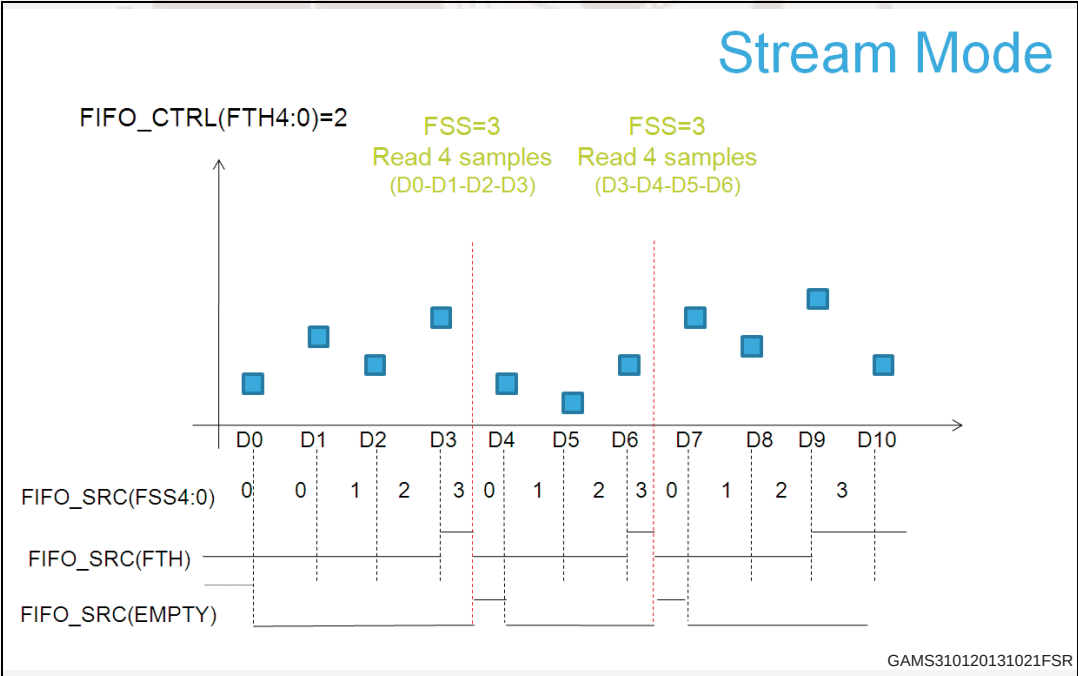
An overrun interrupt can be enabled, CTRL3(INT2_ORun)= '1', in order to read the whole FIFO content at once. If in the application no data can be lost and it is not possible to read at least one sample for each axis within one ODR period, a FIFO Threshold interrupt can be enabled in order to read partially the FIFO and let free memory slots for data incoming. Setting the FIFO_CTRL(FTH4:0) to N value, the number of Yaw, Pitch and Roll data samples that should be read at FIFO Threshold interrupt rising is up to (N+1).

Figure 9. Stream mode



In the latter case reading all FIFO content before an overrun interrupt has occurred, the first data read is equal to the last already read in previous burst, so the number of new data available in FIFO depends on previous reading (see FIFO_SRC behavior depicted in next figures).

Figure 10. Stream mode with threshold interrupt enable



In dynamic-stream mode (FIFO_CTRL(FM2:0) = 110) after emptying the FIFO the first new sample that arrives becomes the first to be read in subsequent read burst. In this way in

dynamic-stream mode (FIFO_CTRL(FM2:0) = 110) the number of new data available in FIFO does not depend on previous reading.

In dynamic-stream mode FIFO_SRC(FSS4:0) + 1 is the number of new X, Y and Z samples available in the FIFO buffer.

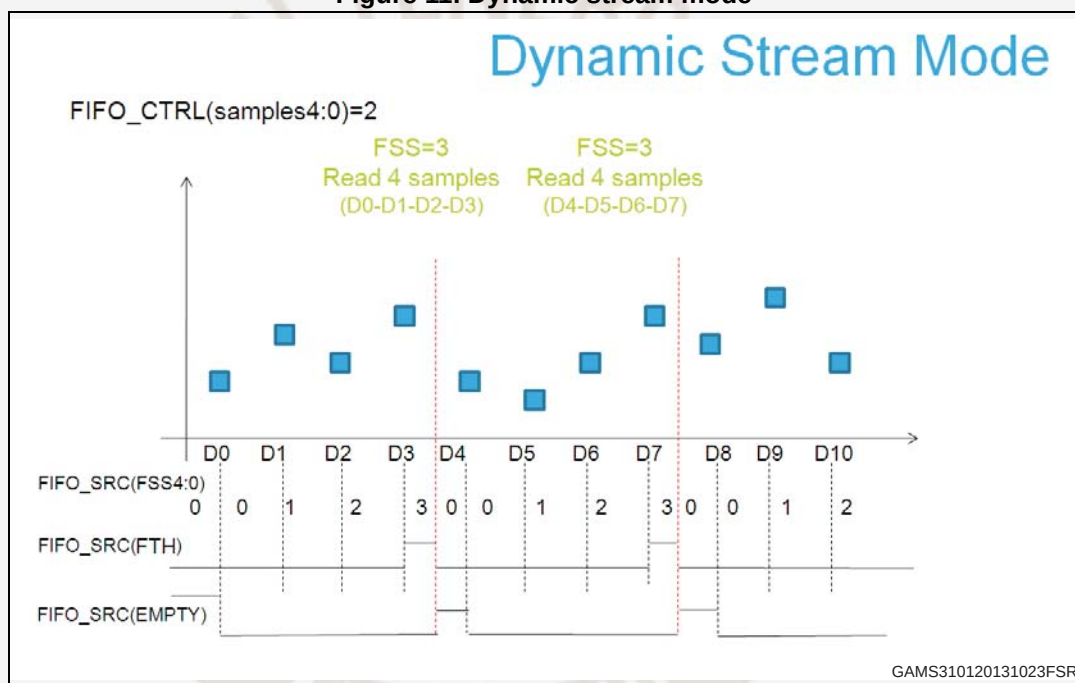
Stream mode is intended to be used reading all 32 samples of FIFO within an ODR after receiving an overrun signal.

Dynamic-stream is intended to be used to read FIFO_SRC(FSS4:0) + 1 samples when it is not possible to guarantee data reading within an ODR.

In dynamic-stream mode FIFO_CTRL(FTH4:0) setting should be between 1 and 30.

Also a FIFO Threshold interrupt CTRL3(INT2_FTH) can be enabled in order to read data from the FIFO and let free memory slot for data incoming. Setting the FIFO_CTRL(FTH4:0) to N value, the number of X, Y and Z data samples that should be read at FIFO Threshold interrupt rising, in order to read the whole FIFO content, is N + 2.

Figure 11. Dynamic stream mode



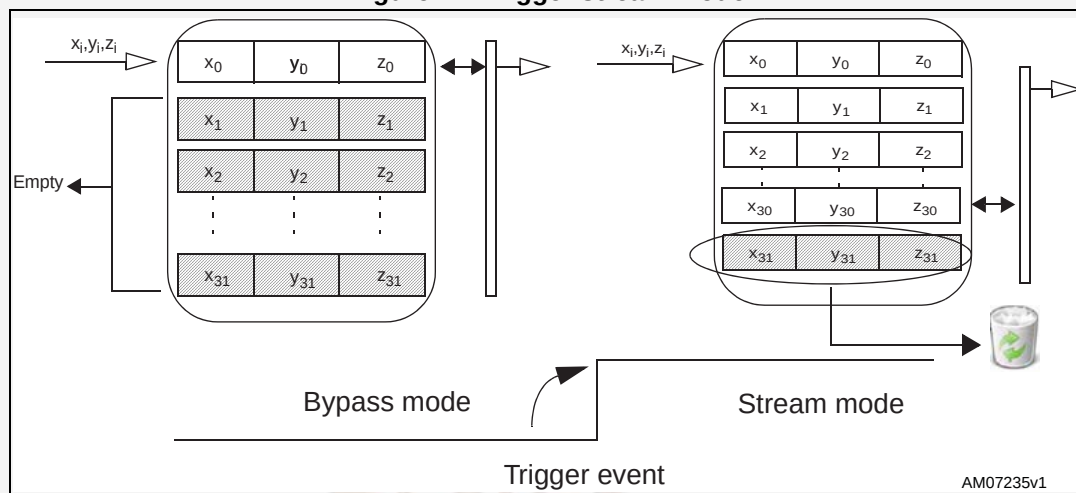
4.2.4 Stream-to-FIFO mode

In stream-to-FIFO mode (FIFO_CTRL(FM2:0) = 011), FIFO behavior changes according to IG_SRC(IA) bit. When IG_SRC(IA) bit is equal to '1' FIFO operates in FIFO-mode, when IG_SRC(IA) bit is equal to '0' FIFO operates in Stream mode.

Interrupt generator should be set to the desired configuration by means of IG_CFG, IG_THS_XH, IG_THS_XL, IG_THS_YH, IG_THS_YL, IG_THS_ZH and IG_THS_ZL.

IG_CFG(LIR) bit should be put to '1' in order to have latched interrupt.

Figure 12. Trigger stream mode



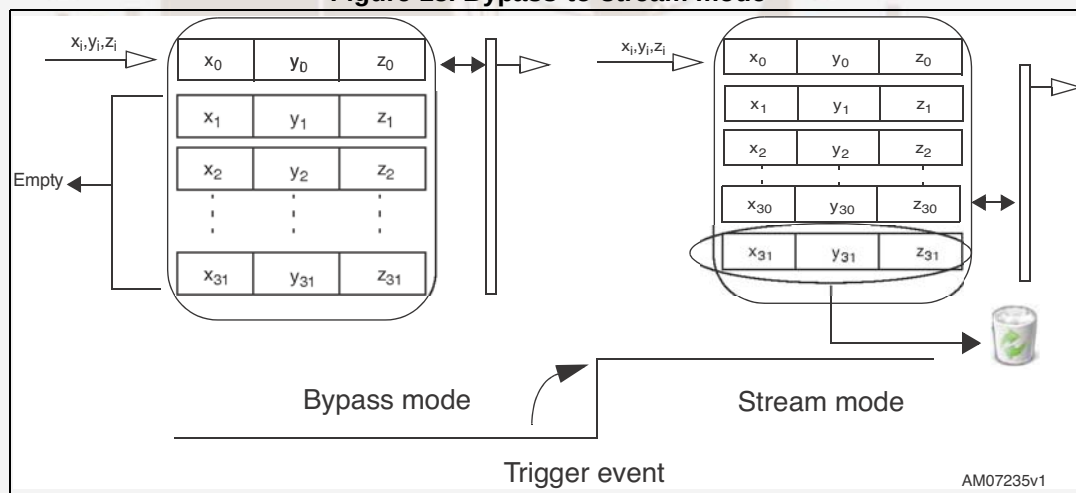
4.2.5 Bypass-to-stream mode

In bypass-to-stream mode ($\text{FIFO\_CTRL}(\text{FM2:0}) = '100'$), Yaw, Pitch and Roll measurement storage inside FIFO operates in Stream mode when IG_SRC (IA) is equal to '1', otherwise FIFO content is reset (bypass mode) .

Interrupt generator should be set to the desired configuration by means of IG_CFG , IG_THS_XH , IG_THS_XL , IG_THS_YH , IG_THS_YL , IG_THS_ZH and IG_THS_ZL .

$\text{IG\_CFG}(\text{LIR})$ bit should be put to '1' in order to have latched interrupt.

Figure 13. Bypass-to-stream mode



4.2.6 Bypass-to-FIFO mode

In bypass-to-FIFO mode (FIFO_CTRL(FM2:0) = '111', FIFO behavior changes according to IG_SRC(IA) bit. When IG_SRC(IA) bit is equal to '1' FIFO operates in FIFO-mode, when IG_SRC(IA) bit is equal to '0' FIFO operates in bypass mode (FIFO content reset). If a latched interrupt is generated FIFO starts collecting data until the first data into the FIFO-buffer is overwritten. Interrupt generator should be set to the desired configuration by means of IG_CFG, IG_THS_XH, IG_THS_XL, IG_THS_YH, IG_THS_YL, IG_THS_ZH and IG_THS_ZL.

IG_CFG (LIR) bit should be put to '1' in order to have latched interrupt.

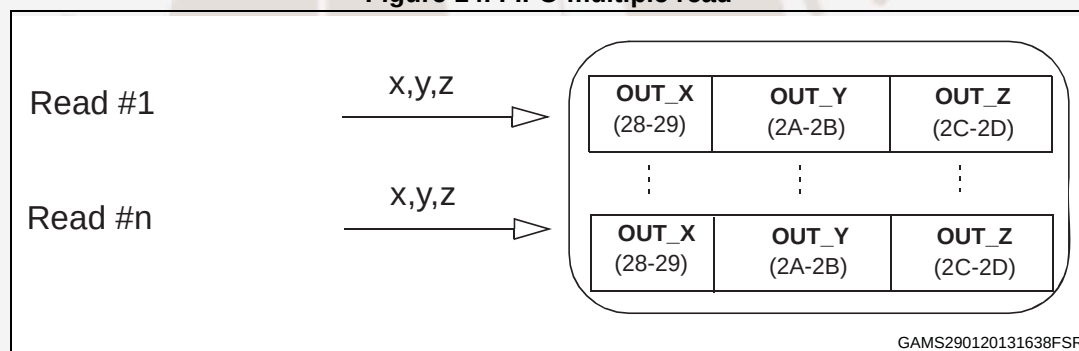
4.2.7 Retrieve data from FIFO

FIFO data is read through OUT_X_L and OUT_X_H (Addr reg 28h and 29h), OUT_Y_L and OUT_Y_H (Addr reg 2Ah and 2Bh) and OUT_Z_L and OUT_Z_H (Addr reg 2Ch and 2Dh) registers. A read operation by means of serial interface of OUT_X, OUT_Y or OUT_Z output registers provides the data stored into the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed into the OUT_X, OUT_Y and OUT_Z registers and both single read and read_burst operations can be used.

4.2.8 FIFO multiple read (burst)

Starting from the Addr 28h multiple read can be performed. Once the reading reaches the Addr 2Dh the system automatically restarts from the Addr. 28h.

Figure 14. FIFO multiple read



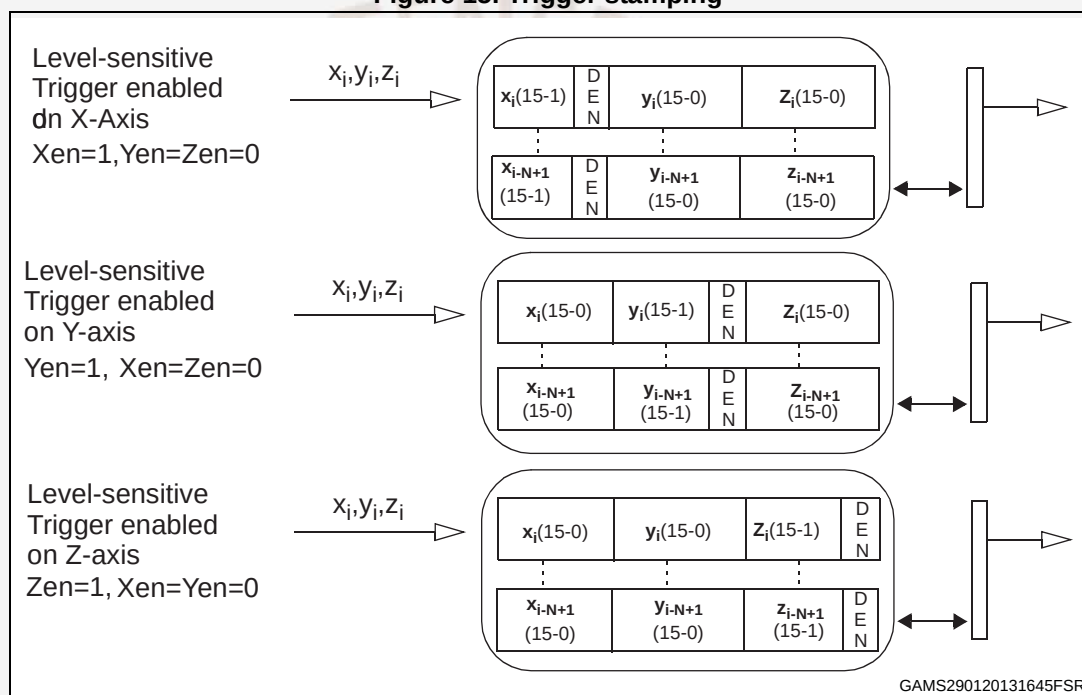
4.3 Level-sensitive/edge sensitive/impulse sensitive data enable

L3GD20H allows external trigger level recognition through enabling EXTRen and LVLen bits into CTRL2 (21h) and IMPEn bit into CTRL4 (23h). Three different modes can be used: level, edge or impulse sensitive trigger.

Table 9. Trigger stamping mode

LVLen	EXTRen	IMPEn	Trigger stamping mode
1	0	0	Level sensitive trigger
0	1	0	Edge sensitive trigger
1	0	1	Impulse sensitive trigger

Figure 15. Trigger stamping



4.3.1 Level sensitive trigger stamping

Level sensitive trigger can be enabled by setting to '1' the LVLen bit into CTRL2 (21h) while EXTRen bit into CTRL2 (21h) and IMPEn bit into CTRL4 (23h) have to be set to '0'.

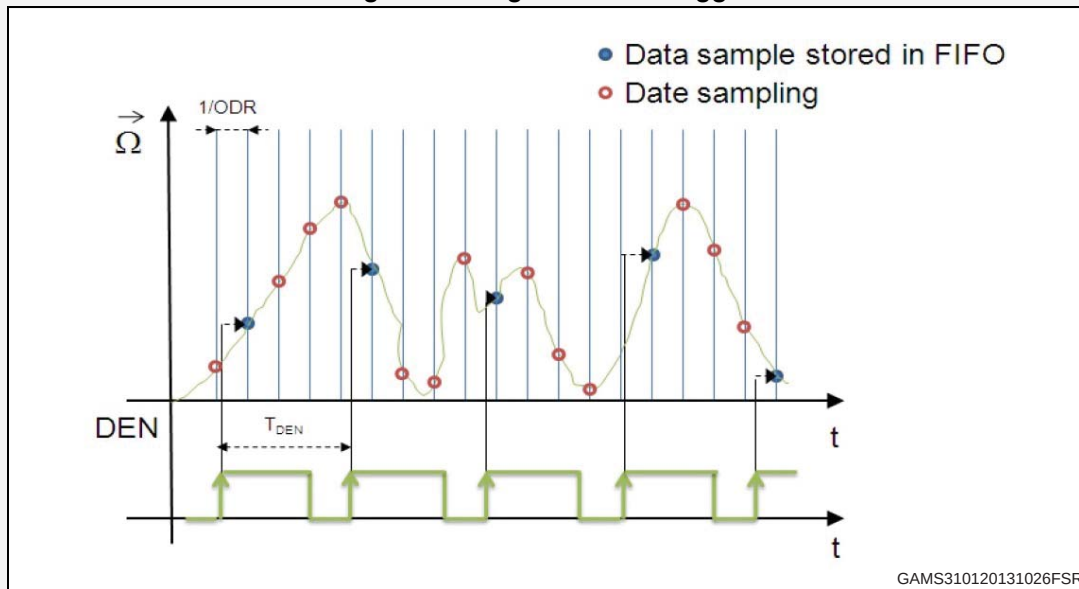
Once enabled, DEN level replaces the LSB of X, Y or Z axes configurable through Xen, Yen, Zen bits into CTRL1 (20h). Data is stored inside the FIFO with the internal selected ODR.

4.3.2 Edge sensitive trigger

Edge sensitive trigger can be enabled by setting to '1' the EXTRen bit into CTRL2 (21h) while LVLen bit into CTRL2 (21h) and IMPEn bit into CTRL4 (23h) have to be set to '0'.

Once enabled, FIFO is filled with the Pitch, Roll and Yaw data on the rising edge of DEN input signal. When ODR selected is 800 Hz, maximum DEN sample frequency is $f_{\text{DEN}} = 1/T_{\text{DEN}} = 400 \text{ Hz}$.

Figure 16. Edge-sensitive trigger



4.3.3 Impulse sensitive trigger

Impulse sensitive trigger can be enabled by setting to '1' LVLEn bit into CTRL2 (21h) and IMPEn bit into CTRL4 (23h) while the EXTren bit into CTRL2 (21h) has to be set to '0'.

If the duration of the DEN pulse is shorter than the selected ODR, the Impulse sensitive trigger functionality has to be enabled.

5 Digital interfaces

The registers embedded inside the L3GD20H may be accessed through both the I²C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the I²C interface, CS line must be tied high (i.e connected to Vdd_IO).

Table 10. Serial interface pin description

Pin name	Pin description
CS	SPI enable I ² C/SPI mode selection (1: I ² C mode; 0: SPI enabled)
SCL/SPC	I ² C Serial Clock (SCL) SPI Serial Port Clock (SPC)
SDA/SDI/SDO	I ² C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
SDO/SA0	SPI Serial Data Output (SDO) I ² C less significant bit of the device address

5.1 I²C serial interface

The L3GD20H I²C is a bus slave. The I²C is employed to write data into registers whose content can also be read back.

The relevant I²C terminology is given in the table below.

Table 11. I²C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through external pull-up resistor. When the bus is free both the lines are high.

The I²C interface is compliant with fast mode (400 kHz) I²C standards as well as with the normal mode.

5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the Master.

The Slave Address (SAD) associated to the L3GD20H is 110101xb. SDO/SA0 pin can be used to modify less significant bit of the device address. If SDO/SA0 pin is connected to voltage supply LSb is '1' (address 1101011b) else if SDO/SA0 pin is connected to ground LSb value is '0' (address 1101010b). This solution permits to connect and address two different gyroscopes to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the L3GD20H behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, a 8-bit sub-address will be transmitted: the 7 LSb represent the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is 1, the SUB (register address) will be automatically incremented to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition will have to be issued after the two sub-address bytes; if the bit is '0' (Write) the Master will transmit to the slave with direction unchanged. [Table 12](#) explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 12. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SDO	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

Table 13. Transfer when Master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 14. Transfer when Master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 15. Transfer when Master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 16. Transfer when Master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real time function) the data line must be left HIGH by the slave. The Master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of first register to be read.

In the presented communication format MAK is Master Acknowledge and NMAK is No Master Acknowledge.

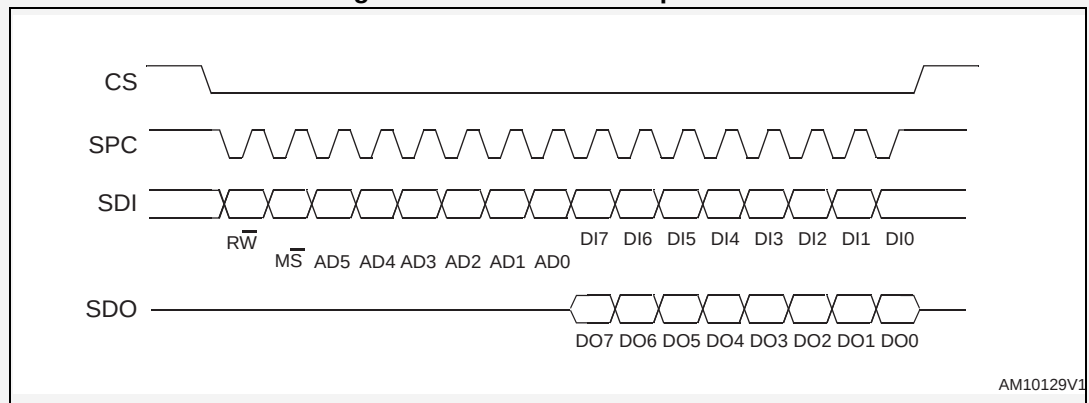
In order to disable the I2C block it is needed to write '1' in bit 3 of register located in address 39h.

5.2 SPI bus interface

The SPI is a bus slave. The SPI allows to write and read the registers of the device.

The Serial Interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 17. Read and write protocol



CS is the Serial Port Enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the Serial Port Data Input and Output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the Read Register and Write Register commands are completed in 16 clock pulses or in multiple of 8 in case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

bit 0: $\overline{RW}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

bit 1: $\overline{MS}$ bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address will be auto incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written into the device (MSb first).

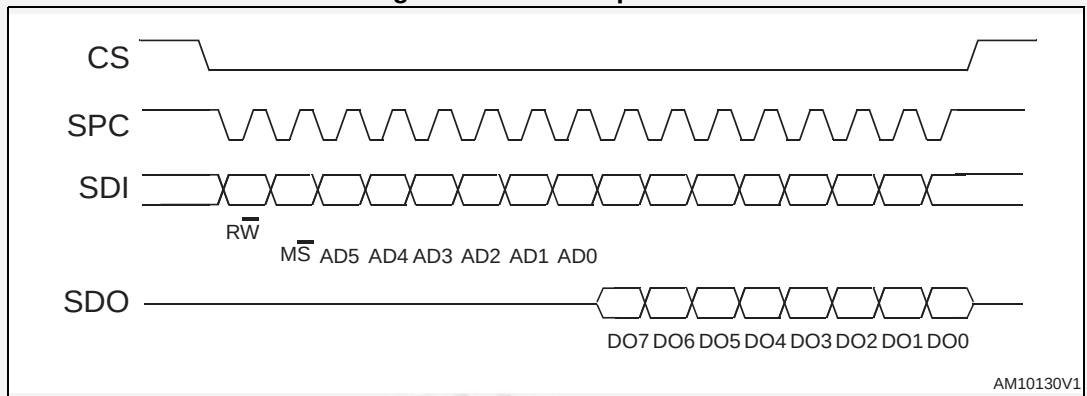
bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When $\overline{MS}$ bit is 0 the address used to read/write data remains the same for every block. When $\overline{MS}$ bit is 1 the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.2.1 SPI read

Figure 18. SPI read protocol



The SPI Read command is performed with 16 clock pulses. Multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: READ bit. The value is 1.

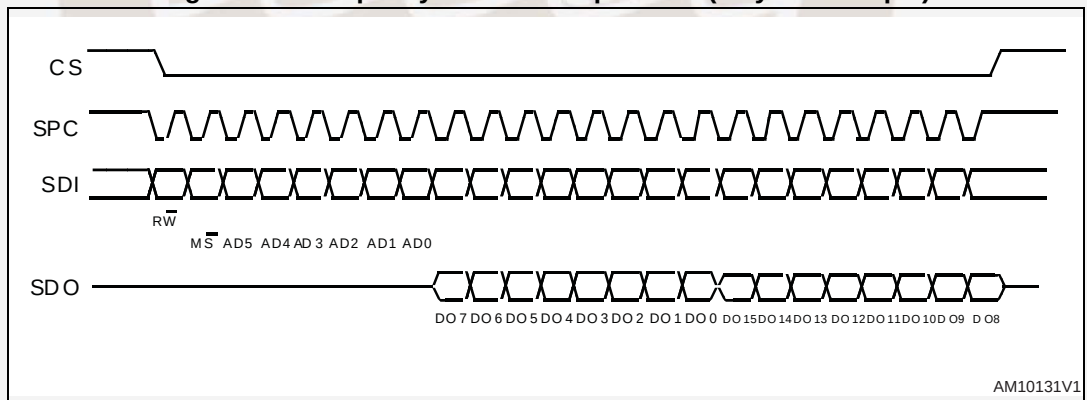
bit 1: $\overline{MS}$ bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

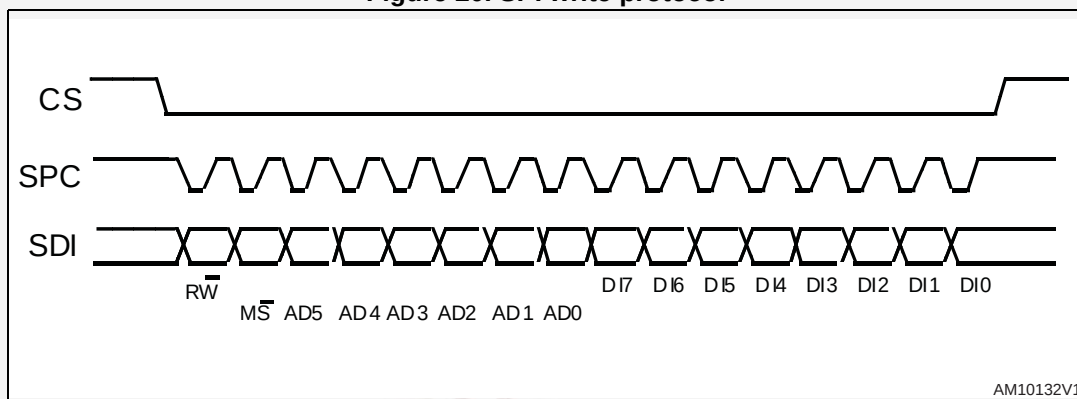
bit 16-... : data DO(...-8). Further data in multiple byte reading.

Figure 19. Multiple bytes SPI read protocol (2 bytes example)



5.2.2 SPI write

Figure 20. SPI write protocol



The SPI Write command is performed with 16 clock pulses. Multiple byte write command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: WRITE bit. The value is 0.

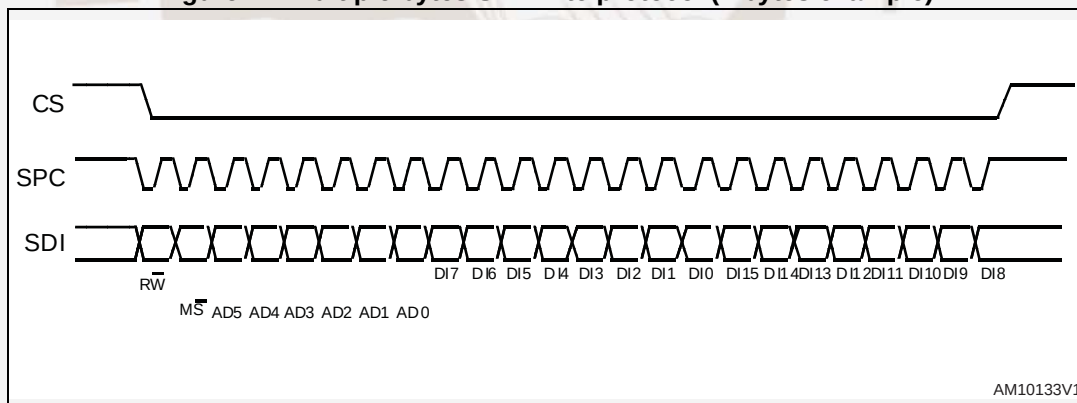
bit 1: $\overline{MS}$ bit. When 0 do not increment address, when 1 increment address in multiple writing.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written inside the device (MSb first).

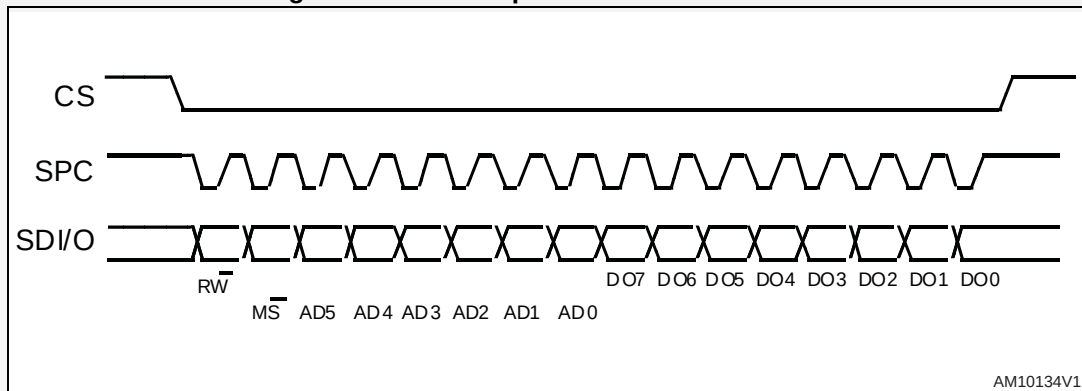
bit 16-... : data DI(...-8). Further data in multiple byte writing.

Figure 21. Multiple bytes SPI write protocol (2 bytes example)



5.2.3 SPI read in 3-wires mode

Figure 22. SPI read protocol in 3-wires mode



The SPI Read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: $\overline{MS}$ bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD[5:0]. This is the address field of the indexed register.

bit 8-15: data DO[7:0] (read mode). This is the data that will be read from the device (MSb first).

Multiple read command is also available in 3-wires mode.

6 Output register mapping

The table given below provides a listing of the 8 bit registers embedded in the device and the related addresses:

Table 17. Register address map

Name	Type	Register address		Default
		Hex	Binary	
Reserved	-	00-0E	-	-
WHO_AM_I	r	0F	000 1111	11010111
Reserved	-	10-1F	-	-
CTRL1	rw	20	010 0000	00000111
CTRL2	rw	21	010 0001	00000000
CTRL3	rw	22	010 0010	00000000
CTRL4	rw	23	010 0011	00000000
CTRL5	rw	24	010 0100	00000000
REFERENCE	rw	25	010 0101	00000000
OUT_TEMP	r	26	010 0110	Output
STATUS	r	27	010 0111	Output
OUT_X_L	r	28	010 1000	Output
OUT_X_H	r	29	010 1001	Output
OUT_Y_L	r	2A	010 1010	Output
OUT_Y_H	r	2B	010 1011	Output
OUT_Z_L	r	2C	010 1100	Output
OUT_Z_H	r	2D	010 1101	Output
FIFO_CTRL	rw	2E	010 1110	00000000
FIFO_SRC	r	2F	010 1111	Output
IG_CFG	rw	30	011 0000	00000000
IG_SRC	r	31	011 0001	Output
IG_THS_XH	rw	32	011 0010	00000000
IG_THS_XL	rw	33	011 0011	00000000
IG_THS_YH	rw	34	011 0100	00000000
IG_THS_YL	rw	35	011 0101	00000000
IG_THS_ZH	rw	36	011 0110	00000000
IG_THS_ZL	rw	37	011 0111	00000000
IG_DURATION	rw	38	011 1000	00000000
LOW_ODR	rw	39	011 1001	00000000

Registers marked as *Reserved* must not be changed. The writing to those registers may cause permanent damages to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered-up.



7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve angular rate data. The registers address, made of 7 bits, is used to identify them and to write the data through serial interface.

7.1 WHO_AM_I (0Fh)

Table 18. WHO_AM_I register

1	1	0	1	0	1	1	1

Device identification register.

7.2 CTRL1 (20h)

Table 19. CTRL1 register⁽¹⁾

DR1	DR0	BW1	BW0	PD	Zen	Xen	Yen

1. Xen, Yen, Zen enable X, Y or Z register in level sensitive trigger mode. Once LVLen bit = 1, DEN level replaces the LSB of X, Y or Z axes and all axis are available for reading.

Table 20. CTRL1 description

DR1-DR0	Output data rate selection. Refer to Table 21
BW1-BW0	Bandwidth selection. Refer to Table 21
PD	Power mode. Default value: 0. Refer to Table 0= Power Down 1= Normal Mode (For Sleep Mode set {PD:Zen:Yen:Xen} to {1000})
Zen	Z axis enable. Default value: 1 (0: Z axis disabled; 1: Z axis enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled; 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

DR<1:0> is used to set ODR selection. **BW <1:0>** is used to set bandwidth selection.

In the following table are reported all frequency resulting in combination of DR / BW bits.

Table 21. DR and BW configuration setting

Low_ODR ⁽¹⁾	DR <1:0>	BW <1:0>	ODR [Hz]	Cut-Off [Hz] ⁽²⁾
1	00	00	12.5	n.a.
1	00	01	12.5	n.a.
1	00	10	12.5	n.a.
1	00	11	12.5	n.a.
1	01	00	25	n.a.
1	01	01	25	n.a.
1	01	10	25	n.a.
1	01	11	25	n.a.
1	1X	00	50	16.6
1	1X	01	50	16.6
1	1X	10	50	16.6
1	1X	11	50	16.6
0	00	00	100	12.5
0	00	01	100	25
0	00	10	100	25
0	00	11	100	25
0	01	00	200	12.5
0	01	01	200	-
0	01	10	200	-
0	01	11	200	70
0	10	00	400	20
0	10	01	400	25
0	10	10	400	50
0	10	11	400	110
0	11	00	800	30
0	11	01	800	35
0	11	10	800	-
0	11	11	800	100

1. this bit is described in register LOW_ODR (39h register).

2. values in the table are indicative and they can vary proportionally with the specific ODR value.

Combination of **PD**, **Zen**, **Yen**, **Xen** are used to set device in different modes (power down / normal / sleep mode) according with the following table.

Table 22. Power mode selection configuration

Mode	PD	Zen	Yen	Xen
Power down	0	-	-	-
Normal	1	-	-	-
Sleep	1	0	0	0

7.3 CTRL2 (21h)

Table 23. CTRL2 register

EXTRen	LVLen	HPM1	HPM0	HPCF3	HPCF2	HPCF1	HPCF0

Table 24. CTRL2 description

EXTRen	Edge sensitive trigger Enable: Default value: 0 (0: external trigger disabled; 1: External trigger enabled)
LVLen	Level sensitive trigger Enable: Default value: 0 (0: level sensitive trigger disabled; 1: level sensitive trigger enabled)
HPM1- HPM0	High Pass filter Mode Selection. Default value: 00 Refer to Table 25
HPCF3- HPCF0	High Pass filter Cut Off frequency selection. Default value: 0000 Refer to Table 26

Table 25. High pass filter mode configuration

HPM1	HPM0	High pass filter mode
0	0	Normal mode (reset reading REFERENCE 25h register)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset on interrupt event

Table 26. High pass filter cut off frequency configuration [Hz]⁽¹⁾

HPCF3-0	ODR=12.5 Hz	ODR=25 Hz	ODR=50 Hz	ODR =100 Hz	ODR =200 Hz	ODR =400 Hz	ODR =800 Hz
0000	1	2	4	8	15	30	56
0001	0.5	1	2	4	8	15	30
0010	0.2	0.5	1	2	4	8	15
0011	0.1	0.2	0.5	1	2	4	8

Table 26. High pass filter cut off frequency configuration [Hz]⁽¹⁾ (continued)

HPCF3-0	ODR=12.5 Hz	ODR=25 Hz	ODR=50 Hz	ODR =100 Hz	ODR =200 Hz	ODR =400 Hz	ODR =800 Hz
0100	0.05	0.1	0.2	0.5	1	2	4
0101	0.02	0.05	0.1	0.2	0.5	1	2
0110	0.01	0.02	0.05	0.1	0.2	0.5	1
0111	0.005	0.01	0.02	0.05	0.1	0.2	0.5
1000	0.002	0.005	0.01	0.02	0.05	0.1	0.2
1001	0.001	0.002	0.005	0.01	0.02	0.05	0.1

1. values in the table are indicative and they can vary proportionally with the specific ODR value

7.4 CTRL3 (22h)

Table 27. CTRL3 register

INT1_IG	INT1_Boot	H_Lactive	PP_OD	INT2_DRDY	INT2_FTH	INT2_ORun	INT2_Empty

Table 28. CTRL3 description

INT1_IG	Interrupt enable on INT1 pin. Default value 0. (0: disable; 1: enable)
INT1_Boot	Boot status available on INT1 pin. Default value 0. (0: disable; 1: enable)
H_Lactive	Interrupt active configuration on INT. Default value 0. (0: high; 1: low)
PP_OD	Push- Pull / Open drain. Default value: 0. (0: push-pull; 1: open drain)
INT2_DRDY	Date Ready on DRDY/INT2 pin. Default value 0. (0: disable; 1: enable)
INT2_FTH	FIFO Threshold interrupt on DRDY/INT2 pin. Default value: 0. (0: disable; 1: enable)
INT2_ORun	FIFO Overrun interrupt on DRDY/INT2 pin. Default value: 0. (0: disable; 1: enable)
INT2_Empty	FIFO Empty interrupt on DRDY/INT2 pin. Default value: 0. (0: disable; 1: enable)

7.5 CTRL4 (23h)

Table 29. CTRL4 register

BDU	BLE	FS1	FS0	IMPen	ST2	ST1	SIM

Table 30. CTRL4 description

BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB reading)
BLE	Big/little endian data selection. Default value 0. (0: Data LSB @ lower address; 1: Data MSB @ lower address)

Table 30. CTRL4 description (continued)

FS1-FS0	Full scale selection. Default value: 00 (00: 245 dps; 01: 500 dps; 1x: 2000 dps)
IMPen	Level sensitive latched enable. Default value: 0 (0: level sensitive latched disabled; 1: level sensitive latched enabled)
ST2-ST1	Self-test enable. Default value: 00 00 = normal mode (default) 01 = self-test 0 (+) 10 = unused 11 = self-test 1(-)
SIM	SPI Serial Interface Mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface).

7.6 CTRL5 (24h)

Table 31. CTRL5 register

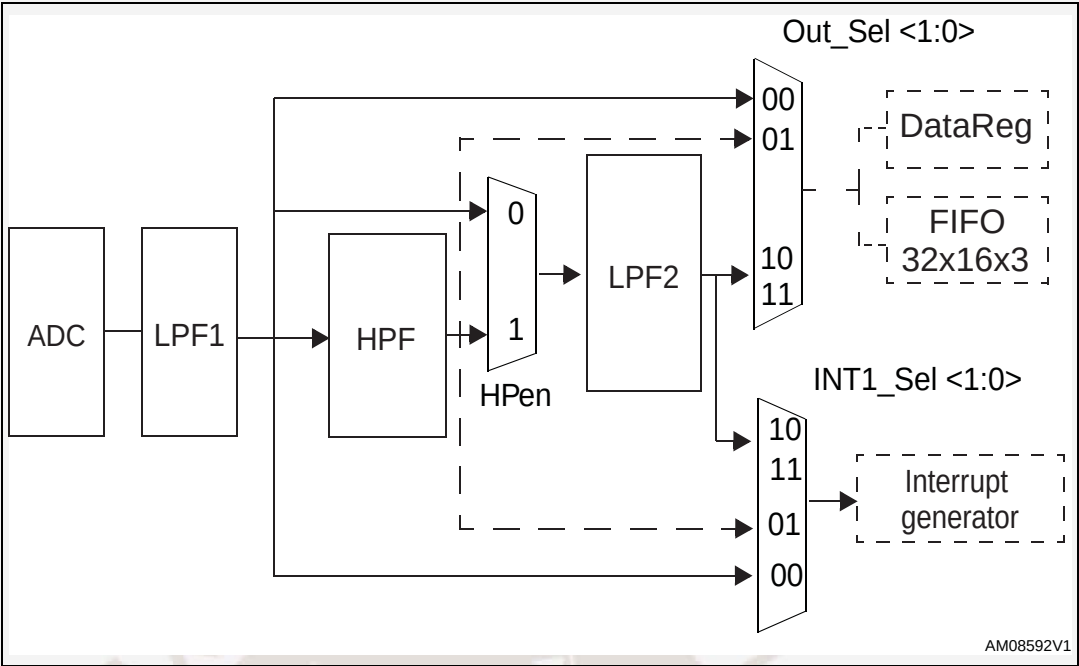
BOOT	FIFO_EN	StopOnFTH	HPen	IG_Sel1	IG_Sel0	Out_Sel1	Out_Sel0

Table 32. CTRL5 description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content ⁽¹⁾)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO Enable)
StopOnFTH	Sensing chain FIFO stop values memorization at FIFO Threshold. Default value: 0 0 = FIFO depth is not limited (32 digital words per axis) 1 = FIFO depth is limited to FIFO Threshold which is defined in FIFO_CTRL (2Eh Register)
HPen	High Pass filter Enable. Default value: 0 (0: HPF disabled; 1: HPF enabled see Figure 23.)
IG_Sel1-IG_Sel0	INT Generator selection configuration. Default value: 00 (See Figure 23.)
Out_Sel1-Out_Sel0	Out selection configuration. Default value: 00 (See Figure 23.)

1. Boot request is executed as soon as internal oscillator is turned-on. It is possible to set bit while in Power-down mode, in this case it will be served at the next normal mode or sleep mode.

Figure 23. IG_Sel and Out_Sel configuration block diagram



7.7 REFERENCE (25h)

Table 33. REFERENCE register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0

Table 34. REFERENCE register description

Ref 7-Ref0	Digital high pass filter reference value. Default value: 0

7.8 OUT_TEMP (26h)

Table 35. OUT_TEMP register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 36. OUT_TEMP register description

Temp7-Temp0	Temperature data (-1LSB/deg with 8 bit resolution). The value is expressed as two's complement.

7.9 STATUS (27h)

Table 37. STATUS register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 38. STATUS description

ZYXOR	X, Y, Z -axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data has overwritten the previous one before it was read)
ZOR	Z axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the Z-axis has overwritten the previous one)
YOR	Y axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the Y-axis has overwritten the previous one)
XOR	X axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the X-axis has overwritten the previous one)
ZYXDA	X, Y, Z -axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z axis new data available. Default value: 0 (0: a new data for the Z-axis is not yet available; 1: a new data for the Z-axis is available)
YDA	Y axis new data available. Default value: 0 (0: a new data for the Y-axis is not yet available; 1: a new data for the Y-axis is available)
XDA	X axis new data available. Default value: 0 (0: a new data for the X-axis is not yet available; 1: a new data for the X-axis is available)

7.10 OUT_X_L (28h), OUT_X_H (29h)

X-axis angular rate data. The value is expressed as two's complement.

7.11 OUT_Y_L (2Ah), OUT_Y_H (2Bh)

Y-axis angular rate data. The value is expressed as two's complement.

7.12 OUT_Z_L (2Ch), OUT_Z_H (2Dh)

Z-axis angular rate data. The value is expressed as two's complement.

7.13 FIFO_CTRL (2Eh)

Table 39. FIFO_CTRL register

FM2	FM1	FM0	FTH4	FTH3	FTH2	FTH1	FTH0

Table 40. FIFO_CTRL register description

FM2-FM0	FIFO mode selection. Default value: 000 (see Table 41)
FTH4-FTH0	FIFO threshold setting. Default value: 0

Table 41. FIFO mode configuration

FM2	FM1	FM0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-stream mode
1	1	0	Dynamic stream mode
1	1	1	Bypass-to-FIFO mode

7.14 FIFO_SRC (2Fh)

Table 42. FIFO_SRC register

FTH	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 43. FIFO_SRC register description

FTH	FIFO threshold status. (0: FIFO filling is lower than FTH level; 1: FIFO filling is equal or higher than FTH level)
OVRN	Overflow bit status. (0: FIFO is not completely filled; 1: FIFO is completely filled)
EMPTY	FIFO empty bit. (0: FIFO not empty; 1: FIFO empty)
FSS4-FSS0	FIFO stored data level of the unread samples

7.15 IG_CFG (30h)

Table 44. IG_CFG register

AND/OR	LIR	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 45. IG_CFG description

AND/OR	AND/OR combination of Interrupt events. Default value: 0 (0: OR combination of interrupt events 1: AND combination of interrupt events)
LIR	Latch Interrupt Request. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched) Cleared by reading IG_SRC reg.
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured angular rate value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured angular rate value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured angular rate value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured angular rate value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured angular rate value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured angular rate value lower than preset threshold)

Configuration register for Interrupt source.

7.16 IG_SRC (31h)

Table 46. IG_SRC register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 47. IG_SRC description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z High event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z Low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y High event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y Low event has occurred)

Table 47. IG_SRC description

XH	X high. Default value: 0 (0: no interrupt, 1: X High event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X Low event has occurred)

Interrupt source register. Read only register.

Reading at this address clears IG_SRC IA bit (and eventually the interrupt signal on INT1 pin) and allows the refresh of data in the IG_SRC register if the latched option was chosen.

7.17 IG_THS_XH (32h)

Table 48. IG_THS_XH register

DCRM	THSX14	THSX13	THSX12	THSX11	THSX10	THSX9	THSX8

Table 49. IG_THS_XH description

DCRM	Interrupt generation counter mode selection. Default value: 0 0 = Reset 1 = Decrement
THSX14 - THSX8	Interrupt threshold on X axis. Default value: 000 0000

7.18 IG_THS_XL (33h)

Table 50. IG_THS_XL register

THSX7	THSX6	THSX5	THSX4	THSX3	THSX2	THSX1	THSX0

Table 51. IG_THS_XL description

THSX7 - THSX0	Interrupt threshold on X axis. Default value: 0000 0000

7.19 IG_THS_YH (34h)

Table 52. IG_THS_YH register

-	THSY14	THSY13	THSY12	THSY11	THSY10	THSY9	THSY8

Table 53. IG_THS_YH description

THSY14 - THSY8	Interrupt threshold on Y axis. Default value: 000 0000

7.20 IG_THS_YL (35h)

Table 54. IG_THS_YL register

THSY7	THSY6	THSY5	THSY4	THSY3	THSY2	THSY1	THSY0

Table 55. IG_THS_YL description

THSY7 - THSY0	Interrupt threshold on Y axis. Default value: 0000 0000

7.21 IG_THS_ZH (36h)

Table 56. IG_THS_ZH register

-	THSZ14	THSZ13	THSZ12	THSZ11	THSZ10	THSZ9	THSZ8

Table 57. IG_THS_ZH description

THSZ14 - THSZ8	Interrupt threshold on Z axis. Default value: 000 0000

7.22 IG_THS_ZL (37h)

Table 58. IG_THS_ZL register

THSZ7	THSZ6	THSZ5	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0

Table 59. IG_THS_ZL description

THSZ7 - THSZ0	Interrupt threshold on Z axis. Default value: 0000 0000

7.23 IG_DURATION (38h)

Table 60. IG_DURATION register

WAIT	D6	D5	D4	D3	D2	D1	D0

Table 61. IG_DURATION description

WAIT	WAIT enable. Default value: 0 (0: disable; 1: enable)
D6 - D0	Duration value. Default value: 000 0000

D6 - D0 bits set the minimum duration of the Interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

WAIT bit has the following meaning:

Wait = '0': the interrupt falls immediately if signal crosses the selected threshold

Wait = '1': if signal crosses the selected threshold, the interrupt falls after a number of samples equal to the duration counter register value.

Figure 24. Wait disabled

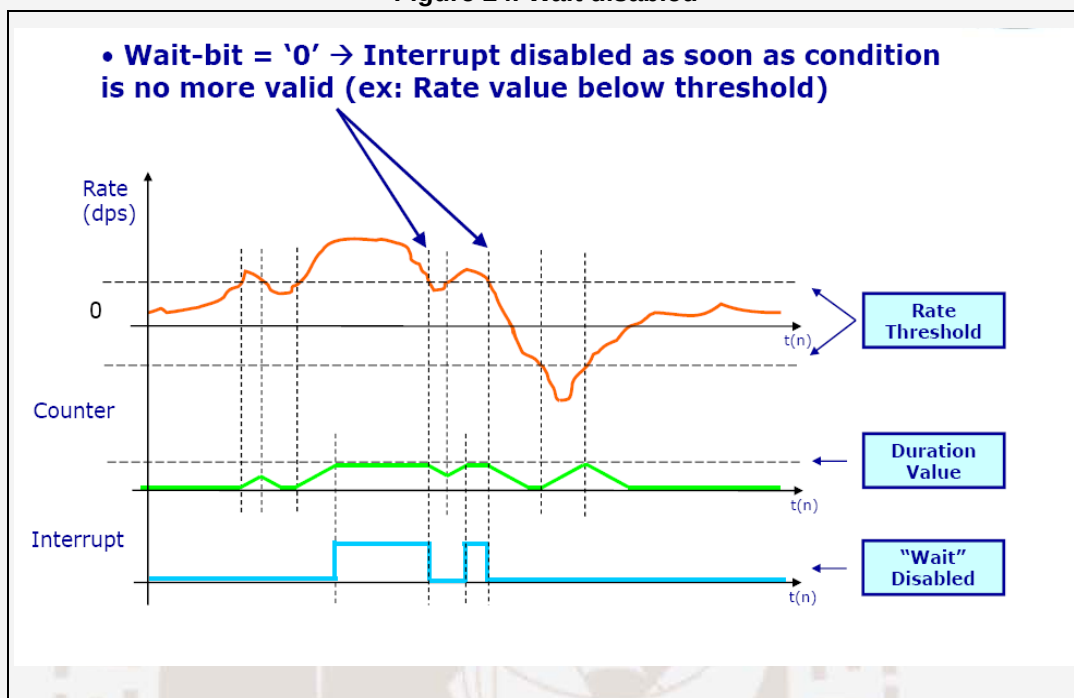
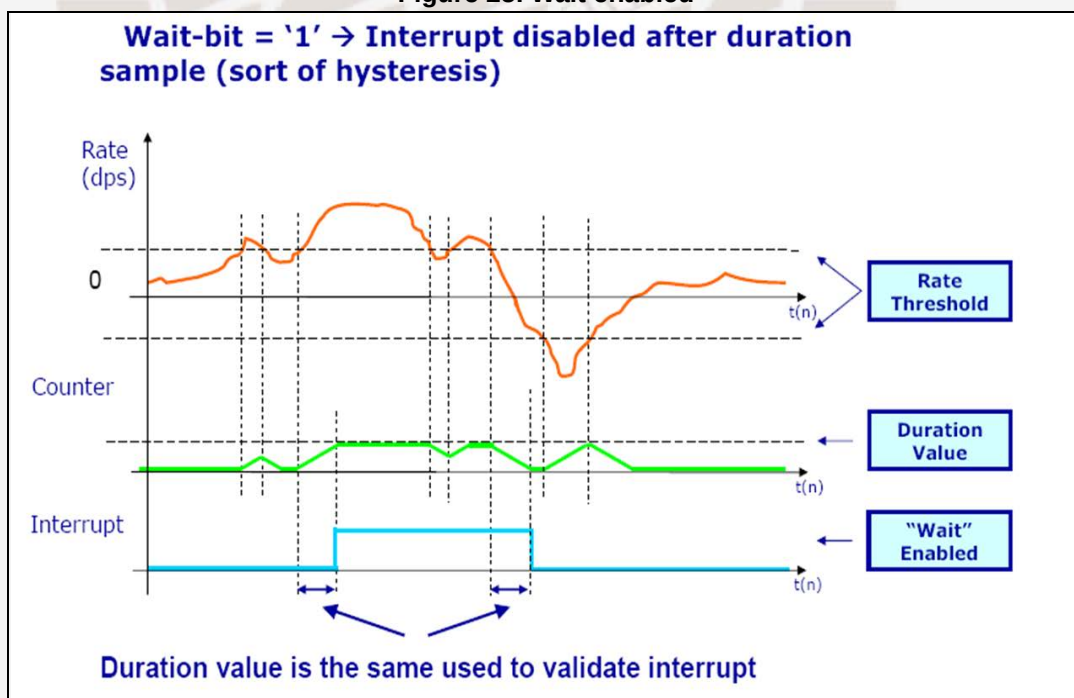


Figure 25. Wait enabled



7.24 LOW_ODR (39h)

Table 62. LOW_ODR register

--	--	DRDY_HL	0 ⁽¹⁾	I2C_dis	SW_RES	0 ⁽¹⁾	Low_ODR

1. These bits must be set to '0' for proper working of the device.

Table 63. LOW_ODR description

DRDY_HL	DRDY/INT2 pin active level. Default value: 0 0 = DRDY active high 1 = DRDY active low
I2C_dis	0 = both the I2C and SPI interfaces enabled (default) 1 = SPI only
SW_RES	Software reset. Default value: 0 0 = Normal Mode 1 = Reset Device (this bit is cleared by hardware after next flash boot)
Low_ODR	Low speed ODR. Default value: 0 Refer to Table 21 DR and BW configuration setting: for ODR and Bandwidth configuration on CTRL1 register 0 = Low Speed ODR disabled 1 = Low Speed ODR enabled

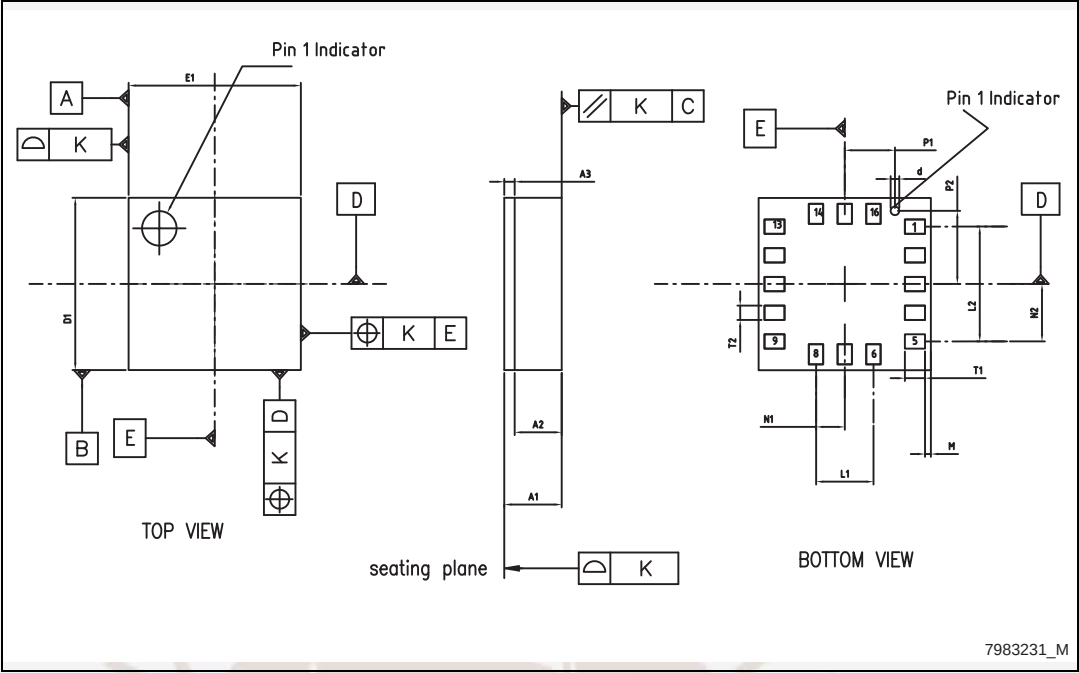
8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 64. LGA 3x3x1.0 16L mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A1			1
A2		0.785	
A3		0.200	
D1	2.850	3.000	3.150
E1	2.850	3.000	3.150
L1		1.000	1.060
L2		2.000	2.060
N1		0.500	
N2		1.000	
M	0.040	0.100	
P1		0.875	
P2		1.275	
T1	0.290	0.350	0.410
T2	0.190	0.250	0.310
d		0.150	
k		0.050	

Figure 26. LGA 3x3x1.0 16L mechanical drawing



9 Revision history

Table 65. Document revision history

Date	Revision	Changes
20-Jul-2012	1	Initial release.
05-Mar-2013	2	Added Chapter 3: Application hints , Chapter 6: Output register mapping and Chapter 7: Register description Updated Chapter 4.2: FIFO .



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LSM303DLHC

Ultra compact high performance e-compass 3D accelerometer and 3D magnetometer module

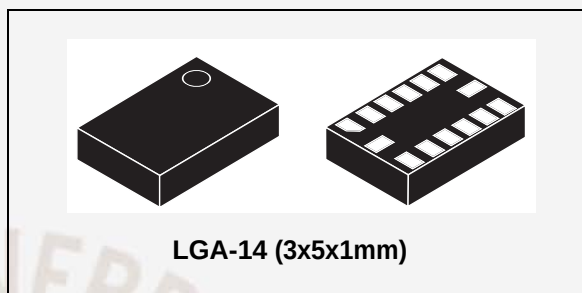
Preliminary data

Features

- 3 magnetic field channels and 3 acceleration channels
- From ± 1.3 to ± 8.1 gauss magnetic field full-scale
- $\pm 2g / \pm 4g / \pm 8g / \pm 16g$ selectable full-scale
- 16 bit data output
- I²C serial interface
- Analog supply voltage 2.16 V to 3.6 V
- Power-down mode/ low-power mode
- 2 independent programmable interrupt generators for free-fall and motion detection
- Embedded temperature sensor
- Embedded FIFO
- 6D/4D orientation detection
- ECOPACK[®] RoHS and "Green" compliant

Applications

- Compensated compass
- Map rotation
- Position detection
- Motion-activated functions
- Free-fall detection
- Click/double click recognition
- Pedometer
- Intelligent power-saving for handheld devices
- Display orientation
- Gaming and virtual reality input devices
- Impact recognition and logging
- Vibration monitoring and compensation



LGA-14 (3x5x1mm)

Description

The LSM303DLHC is a system-in-package featuring a 3D digital linear acceleration sensor and a 3D digital magnetic sensor.

LSM303DLHC has linear acceleration full-scales of $\pm 2g / \pm 4g / \pm 8g / \pm 16g$ and a magnetic field full-scale of $\pm 1.3 / \pm 1.9 / \pm 2.5 / \pm 4.0 / \pm 4.7 / \pm 5.6 / \pm 8.1$ gauss. All full-scales available are fully selectable by the user.

LSM303DLHC includes an I²C serial bus interface that supports standard and fast mode 100 kHz and 400kHz. The system can be configured to generate interrupt signals by inertial wake-up/free-fall events as well as by the position of the device itself. Thresholds and timing of interrupt generators are programmable by the end user on the fly. Magnetic and accelerometer parts can be enabled or put into power-down mode separately.

The LSM303DLHC is available in a plastic land grid array package (LGA) and is guaranteed to operate over an extended temperature range from -40°C to $+85^{\circ}\text{C}$.

Table 1. Device summary

Part number	Temperature range [°C]	Package	Packing
LSM303DLHC	-40 to +85	LGA-14	Tray
LSM303DLHCTR	-40 to +85	LGA-14	Tape and reel

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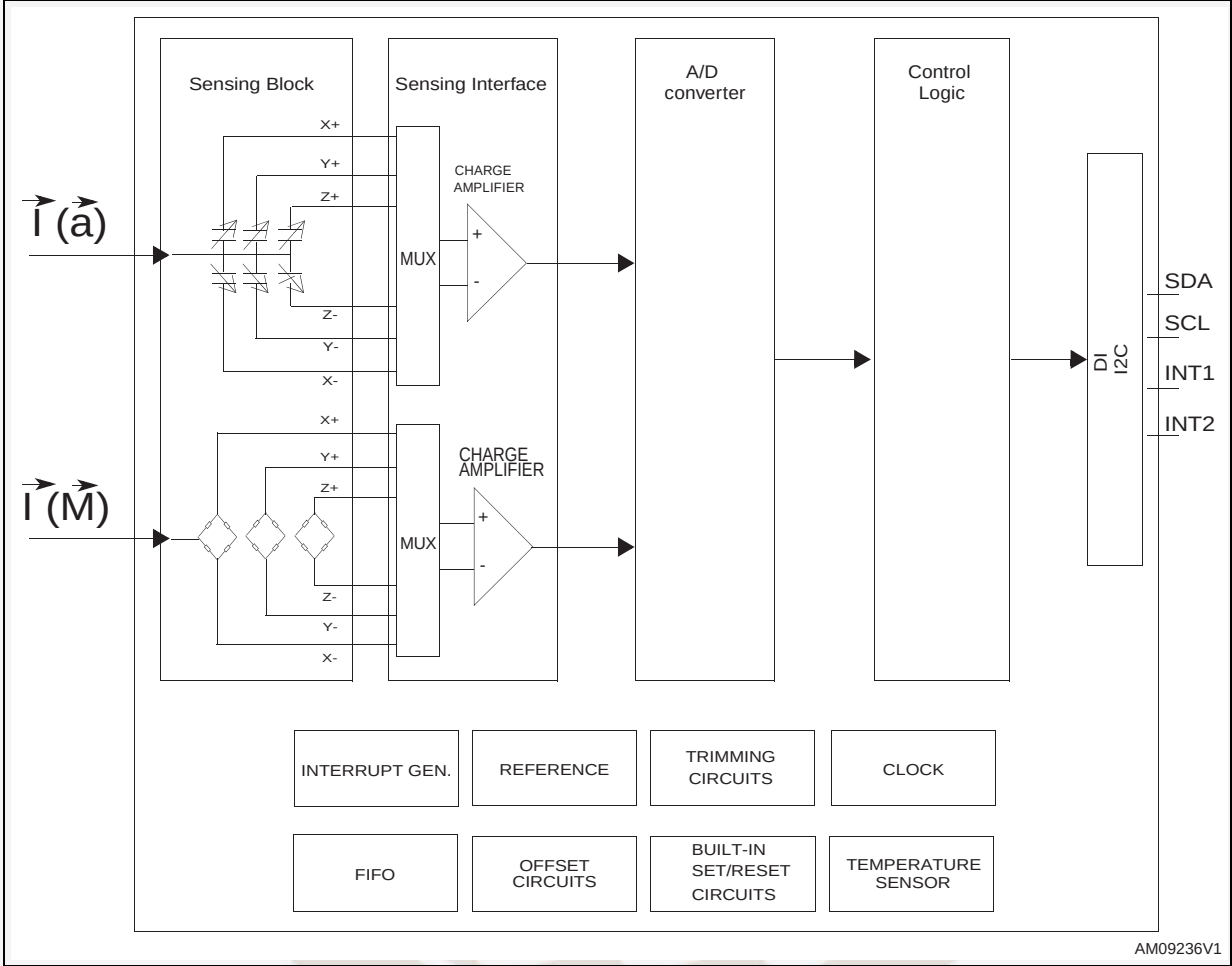
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1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connection

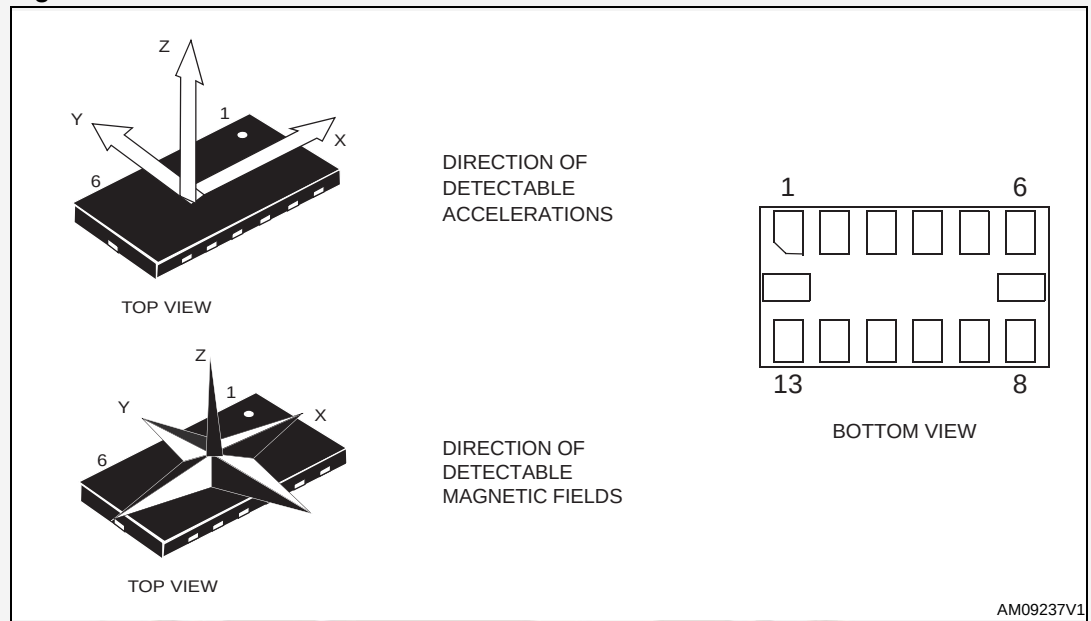


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	SCL	Signal interface I ² C serial clock (SCL)
3	SDA	Signal interface I ² C serial data (SDA)
4	INT2	Inertial Interrupt 2
5	INT1	Inertial Interrupt 1
6	C1	Reserved capacitor connection (C1)
7	GND	0 V supply
8	Reserved	Leave unconnected
9	DRDY	Data ready
10	Reserved	Connect to GND
11	Reserved	Connect to GND
12	SETP	S/R capacitor connection (C2)
13	SETC	S/R capacitor connection (C2)
14	Vdd	Power supply

2 Module specifications

2.1 Sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted^(a).

Table 3. Sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ. ⁽¹⁾	Max.	Unit
LA_FS	Linear acceleration measurement range ⁽²⁾	FS bit set to 00		±2		g
		FS bit set to 01		±4		
		FS bit set to 10		±8		
		FS bit set to 11		±16		
M_FS	Magnetic measurement range	GN bits set to 001		±1.3		gauss
		GN bits set to 010		±1.9		
		GN bits set to 011		±2.5		
		GN bits set to 100		±4.0		
		GN bits set to 101		±4.7		
		GN bits set to 110		±5.6		
		GN bits set to 111		±8.1		
LA_So	Linear acceleration sensitivity	FS bit set to 00		1		mg/LSB
		FS bit set to 01		2		
		FS bit set to 10		4		
		FS bit set to 11		12		
M_GN	Magnetic gain setting	GN bits set to 001 (X,Y)		1100		LSB/ gauss
		GN bits set to 001 (Z)		980		
		GN bits set to 010 (X,Y)		855		
		GN bits set to 010 (Z)		760		
		GN bits set to 011 (X,Y)		670		
		GN bits set to 011 (Z)		600		
		GN bits set to 100 (X,Y)		450		
		GN bits set to 100 (Z)		400		
		GN bits set to 101 (X,Y)		400		
		GN bits set to 101 (Z)		355		
		GN bits set to 110 (X,Y)		330		
		GN bits set to 110 (Z)		295		
		GN bits set to 111 ⁽²⁾ (X,Y)		230		
		GN bits set to 111 ⁽²⁾ (Z)		205		

a. The product is factory calibrated at 2.5 V. The operational power supply range is from 2.16 V to 3.6 V.

Table 3. Sensor characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ. ⁽¹⁾	Max.	Unit
LA_TCS0	Linear acceleration sensitivity change vs. temperature	FS bit set to 00		±0.01		%/°C
LA_TyOff	Linear acceleration typical Zero- <i>g</i> level offset accuracy ^{(3),(4)}	FS bit set to 00		±60		mg
LA_TCOff	Linear acceleration Zero- <i>g</i> level change vs. temperature	Max. delta from 25 °C		±0.5		mg/°C
LA_An	Acceleration noise density	FS bit set to 00, normal mode(Table 8.), ODR bit set to 1001		220		ug/ sqrt(Hz)
M_R	Magnetic resolution			2		mgauss
M_CAS	Magnetic cross-axis sensitivity	Cross field = 0.5 gauss H applied = ±3 gauss		±1		%FS/ gauss
M_EF	Maximum exposed field	No permitting effect on zero reading			10000	gauss
M_DF	Disturbing field	Sensitivity starts to degrade. Use S/R pulse to restore sensitivity			20	gauss
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.

2. Verified by wafer level test and measurement of initial offset and sensitivity.

3. Typical Zero-*g* level offset value after MSL3 preconditioning.

4. Offset can be eliminated by enabling the built-in high pass filter.

2.2 Temperature sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted ^(b).

Table 4. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ. ⁽¹⁾	Max.	Unit
TSDr	Temperature sensor output change vs. temperature	-		8		LSB/°C ⁽²⁾
TODR	Temperature refresh rate			ODR ⁽³⁾		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.

2. 12-bit resolution.

3. For ODR configuration refer to [Table 72](#).

b. The product is factory calibrated at 2.5 V.

2.3 Electrical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ. ⁽¹⁾	Max.	Unit
Vdd	Supply voltage	-	2.16		3.6	V
Vdd_IO	Module power supply for I/O		1.71	1.8	Vdd+0.1	
Idd	Current consumption in normal mode ⁽²⁾			110		μA
IddSL	Current consumption in sleep-mode ⁽³⁾			1		μA
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.

2. Magnetic sensor setting ODR = 7.5 Hz, Accelerometer sensor ODR = 50 Hz.

3. Linear accelerometer in sleep-mode and magnetic sensor in power-down mode.

2.4 Communication interfaces characteristics

External pull-up resistors are required to support I²C standard and fast speed modes.

2.4.1 Sensor I²C - inter IC control interface

Subject to general operating conditions for Vdd and Top.

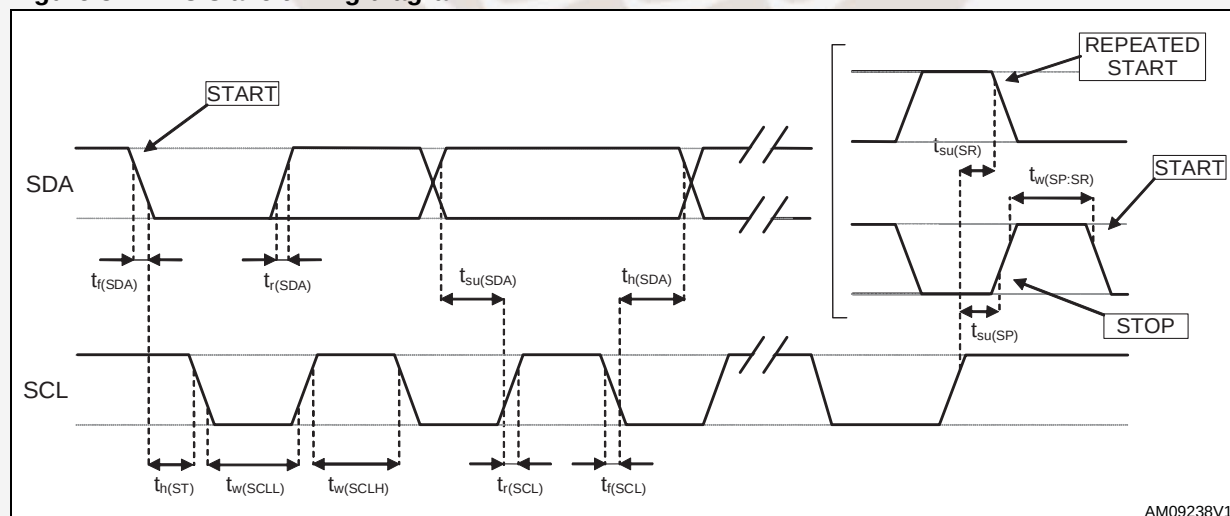
Table 6. I²C slave timing values

Symbol	Parameter	I ² C standard mode ⁽¹⁾		I ² C fast mode ⁽¹⁾		Unit
		Min.	Max.	Min.	Max.	
f _(SCL)	SCL clock frequency	0	100	0	400	KHz
t _{w(SCLL)}	SCL clock low time	4.7		1.3		μs
t _{w(SCLH)}	SCL clock high time	4.0		0.6		
t _{su(SDA)}	SDA setup time	250		100		ns
t _{h(SDA)}	SDA data hold time	0.01	3.45	0.01	0.9	μs
t _{r(SDA)} t _{r(SCL)}	SDA and SCL rise time		1000	20 + 0.1C _b ⁽²⁾	300	ns
t _{f(SDA)} t _{f(SCL)}	SDA and SCL fall time		300	20 + 0.1C _b ⁽²⁾	300	
t _{h(ST)}	START condition hold time	4		0.6		μs
t _{su(SR)}	Repeated START condition setup time	4.7		0.6		
t _{su(SP)}	STOP condition setup time	4		0.6		
t _{w(SP:SR)}	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.

2. C_b = total capacitance of one bus line, in pF.

Figure 3. I²C slave timing diagram ^(c)



AM09238V1

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (SCL, SDA)	-0.3 to Vdd_IO +0.3	V
A _{POW}	Acceleration (any axis, powered, Vdd = 2.5 V)	3,000 for 0.5 ms	g
		10,000 for 0.1 ms	g
A _{UNP}	Acceleration (any axis, unpowered)	3,000 for 0.5 ms	g
		10,000 for 0.1 ms	g
T _{OP}	Operating temperature range	-40 to +85	°C
T _{STG}	Storage temperature range	-40 to +125	°C



This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part.



This is an ESD sensitive device, improper handling can cause permanent damage to the part.

c. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.6 Terminology

2.6.1 Linear acceleration sensitivity

Linear acceleration sensitivity describes the gain of the accelerometer sensor and can be determined by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations, this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ± 1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and also very little over time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

2.6.2 Zero-g level

Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady-state on a horizontal surface measures 0 *g* in the X axis and 0 *g* in the Y axis whereas the Z axis measures 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from the ideal value in this case is called Zero-*g* offset. Offset is, to some extent, a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* level change vs. temperature". The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

3 Functionality

The LSM303DLHC is a system-in-package featuring a 3D digital linear acceleration and 3D digital magnetic field detection sensor.

The system includes specific sensing elements and an IC interface capable of measuring both the linear acceleration and magnetic field applied on it and to provide a signal to the external world through an I²C serial interface with separated digital output.

The sensing system is manufactured using specialized micromachining processes, while the IC interfaces are realized using a CMOS technology that allows to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LSM303DLHC features two data-ready signals (RDY) which indicate when a new set of measured acceleration data and magnetic data are available, therefore simplifying data synchronization in the digital system that uses the device.

The LSM303DLHC may also be configured to generate a free-fall interrupt signal according to a programmed acceleration event along the enabled axes.

Linear acceleration operating mode

LSM303DLHC provides two different acceleration operating modes, respectively reported as "normal mode" and "low-power mode". While normal mode guarantees high resolution, low-power mode reduces further the current consumption.

[Table 8](#) summarizes how to select the operating mode.

Table 8. Accelerometer operating mode selection

Operating mode	CTRL_REG1[3] (LPen bit)	CTRL_REG4[3] (HR bit)	BW [Hz]	Turn-on time [ms]
Low-power mode	1	0	ODR/2	1
Normal mode	0	1	ODR/9	7/ODR

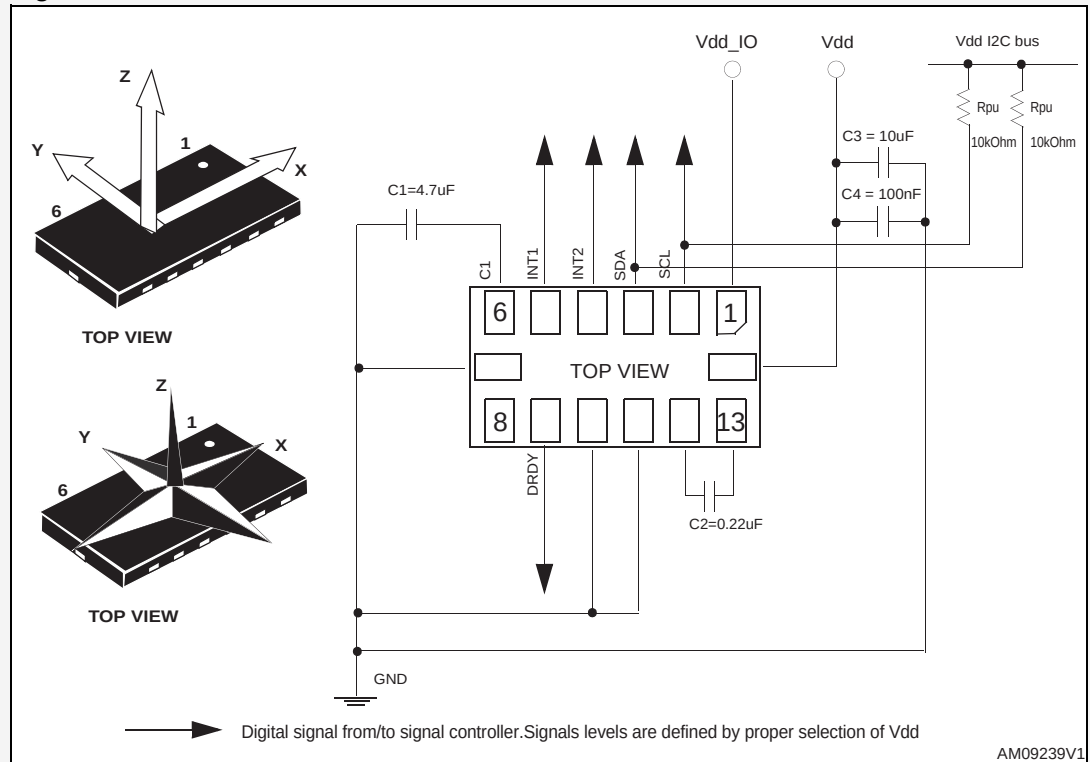
3.1 Factory calibration

The IC interface is factory calibrated for linear acceleration sensitivity (LA_So), and linear acceleration Zero-g level (LA_TyOff).

The trimming values are stored inside the device by a non-volatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during the normal operation. This allows the user to use the device without further calibration.

4 Application hints

Figure 4. LSM303DLHC electrical connection



4.1 capacitors

The C1 and C2 external capacitors should be low SR value ceramic type constructions (typ. suggested value 200 mOhm). Reservoir capacitor C1 is nominally 4.7 μF in capacitance, with the set/reset capacitor C2 nominally 0.22 μF in capacitance.

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C4=100 nF ceramic, C3=10 μF Al) should be placed as near as possible to the supply pin of the device (common design practice). All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to [Figure 4](#)).

The functionality of the device and the measured acceleration/magnetic field data is selectable and accessible through the I²C interface.

The functions, the threshold, and the timing of the two interrupt pins (INT 1 and INT 2) can be completely programmed by the user through the I²C interface.

4.2 Pull-up resistors

Pull-up resistors (suggested value 10 kOhm) are placed on the two I²C bus lines.

4.3 Digital interface power supply

This digital interface, dedicated to the linear acceleration and to the magnetic field signal, is capable of operating with a standard power supply (Vdd) or using a dedicated power supply (Vdd_IO).

4.4 Soldering information

The LGA package is compliant with the ECOPACK[®], RoHS, and "Green" standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave "Pin 1 Indicator" unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

4.5 High current wiring effects

High current in the wiring and printed circuit trace can be culprits in causing errors in magnetic field measurements for compassing.

Conductor generated magnetic fields add to the Earth's magnetic field, causing errors in compass heading computation.

Keep currents higher than 10 mA a few millimeters further away from the sensor IC.

5 Digital interfaces

The registers embedded inside the LSM303DLHC are accessible through two separate I²C serial interfaces, one for the accelerometer core and one for the magnetometer core.

Table 9. Serial interface pin description

PIN Name	PIN Description
SCL	I ² C serial clock (SCL)
SDA	I ² C serial data (SDA)

5.1 I²C serial interface

The LSM303DLHC I²C is a bus slave. The I²C is employed to write the data into the registers when also be read back.

The relevant I²C terminology is given in the table below.

Table 10. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals, and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus, the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface.

5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and bit 8 tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM303DLHC behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted; the 7 LSBs represent the actual register address while the MSB enables address auto-increment. If the MSB of the SUB field is '1', the SUB (register address) is automatically increased to allow multiple data Read/Write.

Table 11. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 12. Transfer when master is writing multiple bytes to slave:

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 13. Transfer when master is receiving (reading) one byte of data from slave:

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSB) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

5.1.2 Linear acceleration digital interface

For linear acceleration the default (factory) 7-bit slave address is 0011001b.

The slave address is completed with a Read/Write bit. If the bit is '1' (read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (write) the master transmits to the slave with the direction unchanged. [Table 14](#) explains how the read/write bit pattern is composed, listing all the possible configurations.

Table 14. SAD+Read/Write patterns

Command	SAD[7:1]	R/W	SAD+R/W
Read	0011001	1	00110011 (33h)
Write	0011001	0	00110010 (32h)

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

In the presented communication format, MAK is master acknowledge and NMAK is no master acknowledge.

Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK		SAK	DATA		DATA		DATA			

5.1.3 Magnetic field digital interface

For magnetic sensors the default (factory) 7-bit slave address is 0011110xb.

The slave address is completed with a Read/Write bit. If the bit is '1' (read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (write) the master transmits to the slave with the direction unchanged. [Table 16](#) explains how the SAD is composed.

Table 16. SAD

Command	SAD[6:0]	R/W	SAD+R/W
Read	0011110	1	00111101 (3Dh)
Write	0011110	0	00111100 (3Ch)

Magnetic signal interface reading/writing

The interface uses an address pointer to indicate which register location is to be read from or written to. These pointer locations are sent from the master to this slave device and succeed the 7-bit address plus 1 bit Read/Write identifier.

To minimize the communication between the master and magnetic digital interface of LSM303DLHC, the address pointer updates automatically without master intervention.

This automatic address pointer update has two additional features. First, when address 12 or higher is accessed, the pointer updates to address 00, and secondly, when address 08 is reached, the pointer rolls back to address 03. Logically, the address pointer operation functions as shown below.

If (address pointer = 08) then the address pointer = 03

Or else, if (address pointer >= 12) then the address pointer = 0

Or else, (address pointer) = (address pointer) + 1

The address pointer value itself cannot be read via the I²C bus.

Any attempt to read an invalid address location returns 0, and any write to an invalid address location, or an undefined bit within a valid address location, is ignored by this device.

6 Register mapping

[Table 17](#) provides a listing of the 8-bit registers embedded in the device and the related addresses:

Table 17. Register address map

Name	Slave address	Type	Register address		Default	Comment
			Hex	Binary		
Reserved (do not modify)	Table 14		00 - 1F	--	--	Reserved
CTRL_REG1_A	Table 14	rw	20	010 0000	00000111	
CTRL_REG2_A	Table 14	rw	21	010 0001	00000000	
CTRL_REG3_A	Table 14	rw	22	010 0010	00000000	
CTRL_REG4_A	Table 14	rw	23	010 0011	00000000	
CTRL_REG5_A	Table 14	rw	24	010 0100	00000000	
CTRL_REG6_A	Table 14	rw	25	010 0101	00000000	
REFERENCE_A	Table 14	rw	26	010 0110	00000000	
STATUS_REG_A	Table 14	r	27	010 0111	00000000	
OUT_X_L_A	Table 14	r	28	010 1000	output	
OUT_X_H_A	Table 14	r	29	010 1001	output	
OUT_Y_L_A	Table 14	r	2A	010 1010	output	
OUT_Y_H_A	Table 14	r	2B	010 1011	output	
OUT_Z_L_A	Table 14	r	2C	010 1100	output	
OUT_Z_H_A	Table 14	r	2D	010 1101	output	
FIFO_CTRL_REG_A	Table 14	rw	2E	010 1110	00000000	
FIFO_SRC_REG_A	Table 14	r	2F	010 1111		
INT1_CFG_A	Table 14	rw	30	011 0000	00000000	
INT1_SOURCE_A	Table 14	r	31	011 0001	00000000	
INT1_THS_A	Table 14	rw	32	011 0010	00000000	
INT1_DURATION_A	Table 14	rw	33	011 0011	00000000	
INT2_CFG_A	Table 14	rw	34	011 0100	00000000	
INT2_SOURCE_A	Table 14	r	35	011 0101	00000000	
INT2_THS_A	Table 14	rw	36	011 0110	00000000	
INT2_DURATION_A	Table 14	rw	37	011 0111	00000000	
CLICK_CFG_A	Table 14	rw	38	011 1000	00000000	
CLICK_SRC_A	Table 14	rw	39	011 1001	00000000	
CLICK_THS_A	Table 14	rw	3A	011 1010	00000000	
TIME_LIMIT_A	Table 14	rw	3B	011 1011	00000000	

Table 17. Register address map (continued)

Name	Slave address	Type	Register address		Default	Comment
			Hex	Binary		
TIME_LATENCY_A	Table 14	rw	3C	011 1100	00000000	
TIME_WINDOW_A	Table 14	rw	3D	011 1101	00000000	
Reserved (do not modify)	Table 14		3E-3F	--	--	Reserved
CRA_REG_M	Table 16	rw	00	00000000	0001000	
CRB_REG_M	Table 16	rw	01	00000001	0010000	
MR_REG_M	Table 16	rw	02	00000010	00000011	
OUT_X_H_M	Table 16	r	03	00000011	output	
OUT_X_L_M	Table 16	r	04	00000100	output	
OUT_Z_H_M	Table 16	r	05	00000101	output	
OUT_Z_L_M	Table 16	r	06	00000110	output	
OUT_Y_H_M	Table 16	r	07	00000111	output	
OUT_Y_L_M	Table 16	r	08	00001000	output	
SR_REG_Mg	Table 16	r	09	00001001	00000000	
IRA_REG_M	Table 16	r	0A	00001010	01001000	
IRB_REG_M	Table 16	r	0B	00001011	00110100	
IRC_REG_M	Table 16	r	0C	00001100	00110011	
Reserved (do not modify)	Table 16		0D-30	--	--	Reserved
TEMP_OUT_H_M	Table 16		31	00000000	output	
TEMP_OUT_L_M	Table 16		32	00000000	output	
Reserved (do not modify)	Table 16		33-3A	--	--	Reserved

Registers marked as “reserved” must not be changed. The writing to these registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibrated values. Their content is automatically restored when the device is powered up.

7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve acceleration data. The register address, made up of 7 bits, is used to identify them and to write the data through the serial interface.

7.1 Linear acceleration register description

7.1.1 CTRL_REG1_A (20h)

Table 18. CTRL_REG1_A register

ODR3	ODR2	ODR1	ODR0	LPen	Zen	Yen	Xen

Table 19. CTRL_REG1_A description

ODR3-0	Data rate selection. Default value: 0 (0000: power-down, others: refer to Table 20 .)
LPen	Low-power mode enable. Default value: 0 (0: normal mode, 1: low-power mode)
Zen	Z axis enable. Default value: 1 (0: Z axis disabled, 1: Z axis enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled, 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled, 1: X axis enabled)

ODR<3:0> is used to set the power mode and ODR selection. In [Table 20](#) all frequencies resulting in a combination of ODR<3:0> are listed.

Table 20. Data rate configuration

ODR3	ODR2	ODR1	ODR0	Power mode selection
0	0	0	0	Power-down mode
0	0	0	1	Normal / low-power mode (1 Hz)
0	0	1	0	Normal / low-power mode (10 Hz)
0	0	1	1	Normal / low-power mode (25 Hz)
0	1	0	0	Normal / low-power mode (50 Hz)
0	1	0	1	Normal / low-power mode (100 Hz)
0	1	1	0	Normal / low-power mode (200 Hz)
0	1	1	1	Normal / low-power mode (400 Hz)

Table 20. Data rate configuration (continued)

ODR3	ODR2	ODR1	ODR0	Power mode selection
1	0	0	0	Low-power mode (1.620 KHz)
1	0	0	1	Normal (1.344 kHz) / low-power mode (5.376 KHz)

7.1.2 CTRL_REG2_A (21h)

Table 21. CTRL_REG2_A register

HPM1	HPM0	HPCF2	HPCF1	FDS	HPCLICK	HPIS2	HPIS1

Table 22. CTRL_REG2_A description

HPM1 -HPM0	High pass filter mode selection. Default value: 00 (refer to Table 23)
HPCF2 - HPCF1	High pass filter cut-off frequency selection
FDS	Filtered data selection. Default value: 0 (0: internal filter bypassed, 1: data from internal filter sent to output register and FIFO)
HPCLICK	High pass filter enabled for CLICK function. (0: filter bypassed, 1: filter enabled)
HPIS2	High pass filter enabled for AOI function on Interrupt 2, (0: filter bypassed, 1: filter enabled)
HPIS1	High pass filter enabled for AOI function on Interrupt 1, (0: filter bypassed, 1: filter enabled)

Table 23. High pass filter mode configuration

HPM1	HPM0	High pass filter mode
0	0	Normal mode (reset reading HP_RESET_FILTER)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset on interrupt event

7.1.3 CTRL_REG3_A (22h)

Table 24. CTRL_REG3_A register

I1_CLICK	I1_AOI1	I1_AOI2	I1_DRDY1	I1_DRDY2	I1_WTM	I1_OVERRUN	--

Table 25. CTRL_REG3_A description

I1_CLICK	CLICK interrupt on INT1. Default value 0. (0: disable, 1: enable)
I1_AOI1	AOI1 interrupt on INT1. Default value 0. (0: disable, 1: enable)
I1_AOI2	AOI2 interrupt on INT1. Default value 0. (0: disable, 1: enable)
I1_DRDY1	DRDY1 interrupt on INT1. Default value 0. (0: disable, 1: enable)
I1_DRDY2	DRDY2 interrupt on INT1. Default value 0. (0: disable, 1: enable)
I1_WTM	FIFO watermark interrupt on INT1. Default value 0. (0: disable, 1: enable)
I1_OVERRUN	FIFO overrun interrupt on INT1. Default value 0. (0: disable, 1: enable)

7.1.4 CTRL_REG4_A (23h)

Table 26. CTRL_REG4_A register

BDU	BLE	FS1	FS0	HR	0 ⁽¹⁾	0 ⁽¹⁾	SIM

1. This bit must be set to '0' for correct working of the device.

Table 27. CTRL_REG4_A description

BDU	Block data update. Default value: 0 (0: continuous update, 1: output registers not updated until MSB and LSB reading)
BLE	Big/little endian data selection. Default value 0. (0: data LSB @ lower address, 1: data MSB @ lower address)
FS1-FS0	Full-scale selection. Default value: 00 (00: +/- 2G, 01: +/- 4G, 10: +/- 8G, 11: +/- 16G)
HR	High resolution output mode: Default value: 0 (0: high resolution disable, 1: high resolution enable)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface, 1: 3-wire interface).

7.1.5 CTRL_REG5_A (24h)

Table 28. CTRL_REG5_A register

BOOT	FIFO_EN	--	--	LIR_INT1	D4D_INT1	LIR_INT2	D4D_INT2

Table 29. CTRL_REG5_A description

BOOT	Reboot memory content. Default value: 0 (0: normal mode, 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable, 1: FIFO enable)
LIR_INT1	Latch interrupt request on INT1_SRC register, with INT1_SRC register cleared by reading INT1_SRC itself. Default value: 0. (0: interrupt request not latched, 1: interrupt request latched)
D4D_INT1	4D enable: 4D detection is enabled on INT1 when 6D bit on INT1_CFG is set to 1.
LIR_INT2	Latch interrupt request on INT2_SRC register, with INT2_SRC register cleared by reading INT2_SRC itself. Default value: 0. (0: interrupt request not latched, 1: interrupt request latched)
D4D_INT2	4D enable: 4D detection is enabled on INT2 when 6D bit on INT2_CFG is set to 1.

7.1.6 CTRL_REG6_A (25h)

Table 30. CTRL_REG6_A register

I2_CLICKen	I2_INT1	I2_INT2	BOOT_I1	P2_ACT	--	H_LACTIVE	--

Table 31. CTRL_REG6_A description

I2_CLICKen	CLICK interrupt on PAD2. Default value 0. (0: disable, 1: enable)
I2_INT1	Interrupt 1 on PAD2. Default value 0. (0: disable, 1: enable)
I2_INT2	Interrupt 2 on PAD2. Default value 0. (0: disable, 1: enable)
BOOT_I1	Reboot memory content on PAD2. Default value: 0 (0: disable, 1: enable)
P2_ACT	Active function status on PAD2. Default value 0. (0: disable, 1: enable)
H_LACTIVE	Interrupt active high, low. Default value 0. (0: active high, 1: active low)

7.1.7 REFERENCE/DATACAPTURE_A (26h)

Table 32. REFERENCE_A register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0

Table 33. REFERENCE_A register description

Ref 7-Ref0	Reference value for interrupt generation. Default value: 0

7.1.8 STATUS_REG_A (27h)

Table 34. STATUS_A register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 35. STATUS_A register description

ZYXOR	X, Y, and Z axis data overrun. Default value: 0 (0: no overrun has occurred, 1: a new set of data has overwritten the previous ones)
ZOR	Z axis data overrun. Default value: 0 (0: no overrun has occurred, 1: a new data for the Z-axis has overwritten the previous one)
YOR	Y axis data overrun. Default value: 0 (0: no overrun has occurred, 1: a new data for the Y-axis has overwritten the previous one)
XOR	X axis data overrun. Default value: 0 (0: no overrun has occurred, 1: a new data for the X-axis has overwritten the previous one)
ZYXDA	X, Y, and Z axis new data available. Default value: 0 (0: a new set of data is not yet available, 1: a new set of data is available)
ZDA	Z axis new data available. Default value: 0 (0: a new data for the Z-axis is not yet available, 1: a new data for the Z-axis is available)
YDA	Y axis new data available. Default value: 0 (0: a new data for the Y-axis is not yet available, 1: a new data for the Y-axis is available)
XDA	X axis new data available. Default value: 0 (0: a new data for the X-axis is not yet available, 1: a new data for the X-axis is available)

7.1.9 OUT_X_L_A (28h), OUT_X_H_A (29h)

X-axis acceleration data. The value is expressed in 2's complement.

7.1.10 OUT_Y_L_A (2Ah), OUT_Y_H_A (2Bh)

Y-axis acceleration data. The value is expressed in 2's complement.

7.1.11 OUT_Z_L_A (2Ch), OUT_Z_H_A (2Dh)

Z-axis acceleration data. The value is expressed in 2's complement.

7.1.12 FIFO_CTRL_REG_A (2Eh)

Table 36. REFERENCE_A register

FM1	FM0	TR	FTH4	FTH3	FTH2	FTH1	FTH0

Table 37. REFERENCE_A register description

FM1-FM0	FIFO mode selection. Default value: 00 (see Table 38)
TR	Trigger selection. Default value: 0 0: trigger event linked to trigger signal on INT1 1: trigger event linked to trigger signal on INT2
FTH4:0	Default value: 0

Table 38. FIFO mode configuration

FM1	FM0	FIFO mode configuration
0	0	Bypass mode
0	1	FIFO mode
1	0	Stream mode
1	1	Trigger mode

7.1.13 FIFO_SRC_REG_A (2Fh)

Table 39. FIFO_SRC_A register

WTM	OVNR_FIFO	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

7.1.14 INT1_CFG_A (30h)

Table 40. INT1_CFG_A register

AOI	6D	ZHIE/ ZUPE	ZLIE/ ZDOWNE	YHIE/ YUPE	YLIE/ YDOWNE	XHIE/ XUPE	XLIE/ XDOWNE

Table 41. INT1_CFG_A description

AOI	AND/OR combination of interrupt events. Default value: 0 (refer to Table 42)
6D	6-direction detection function enabled. Default value: 0 (refer to Table 42)
ZHIE/ ZUPE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request, 1: enable interrupt request)
ZLIE/ ZDOWNE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request, 1: enable interrupt request)

Table 41. INT1_CFG_A description (continued)

YHIE/ YUPE	Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request, 1: enable interrupt request.)
YLIE/ YDOWNE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request, 1: enable interrupt request.)
XHIE/ XUPE	Enable interrupt generation on X high event or on direction recognition. Default value: 0 (0: disable interrupt request, 1: enable interrupt request.)
XLIE/XDOWNE	Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request, 1: enable interrupt request.)

Content of this register is loaded at boot. Write operation at this address is possible only after system boot.

Table 42. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

Difference between AOI-6D = '01' and AOI-6D = '11'.

AOI-6D = '01' is movement recognition. An interrupt is generated when orientation moves from unknown zone to known zone. The interrupt signal stays for a duration ODR.

AOI-6D = '11' is direction recognition. An interrupt is generated when orientation is inside a known zone. The interrupt signal stays until orientation is inside the zone.

7.1.15 INT1_SRC_A (31h)

Table 43. INT1_SRC_A register

0 ⁽¹⁾	IA	ZH	ZL	YH	YL	XH	XL

1. This bit must be set to '0' for correct working of the device.

Table 44. INT1_SRC_A description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated, 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt, 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)

Table 44. INT1_SRC_A description (continued)

YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Interrupt 1 source register. Read only register.

Reading at this address clears the INT1_SRC IA bit (and the interrupt signal on the INT 1 pin) and allows the refreshing of data in the INT1_SRC register if the latched option was chosen.

7.1.16 INT1_THS_A (32h)

Table 45. INT1_THS_A register

0 ⁽¹⁾	THS6	THS5	THS4	THS3	THS2	THS1	THS0

1. This bit must be set to '0' for correct working of the device.

Table 46. INT1_THS_A description

THS6 - THS0	Interrupt 1 threshold. Default value: 000 0000

7.1.17 INT1_DURATION_A (33h)

Table 47. INT1_DURATION_A register

0 ⁽¹⁾	D6	D5	D4	D3	D2	D1	D0

1. This bit must be set to '0' for correct working of the device.

Table 48. INT1_DURATION_A description

D6 - D0	Duration value. Default value: 000 0000

D6 - D0 bits set the minimum duration of the Interrupt 1 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

7.1.18 INT2_CFG_A (34h)

Table 49. INT2_CFG_A register

AOI	6D	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 50. INT2_CFG_A description

AOI	AND/OR combination of interrupt events. Default value: 0 (see Table 51)
6D	6-direction detection function enabled. Default value: 0 (refer to Table 51)
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request, 1: enable interrupt request on measured accel. value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request, 1: enable interrupt request on measured accel. value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request, 1: enable interrupt request on measured accel. value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request, 1: enable interrupt request on measured accel. value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request, 1: enable interrupt request on measured accel. value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request, 1: enable interrupt request on measured accel. value lower than preset threshold)

Table 51. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

Difference between AOI-6D = '01' and AOI-6D = '11'.

AOI-6D = '01' is movement recognition. An interrupt is generated when orientation moves from unknown zone to known zone. The interrupt signal stays for a duration ODR.

AOI-6D = '11' is direction recognition. An interrupt is generated when orientation is inside a known zone. The interrupt signal stays until orientation is inside the zone.

7.1.19 INT2_SRC_A (35h)

Table 52. INT2_SRC_A register

0 ⁽¹⁾	IA	ZH	ZL	YH	YL	XH	XL

1. This bit must be set to '0' for correct working of the device.

Table 53. INT2_SRC_A description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated, 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt, 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X Low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Interrupt 2 source register. Read only register.

Reading at this address clears INT2_SRC IA bit (and the interrupt signal on the INT 2 pin) and allows the refreshing of data in the INT2_SRC register if the latched option was chosen.

7.1.20 INT2_THS_A (36h)

Table 54. INT2_THS_A register

0 ⁽¹⁾	THS6	THS5	THS4	THS3	THS2	THS1	THS0

1. This bit must be set to '0' for correct working of the device

Table 55. INT2_THS_A description

THS6 - THS0	Interrupt 1 threshold. Default value: 000 0000

7.1.21 INT2_DURATION_A (37h)

Table 56. INT2_DURATION_A register

0 ⁽¹⁾	D6	D5	D4	D3	D2	D1	D0

1. This bit must be set to '0' for correct working of the device

Table 57. INT2_DURATION_A description

D6-D0	Duration value. Default value: 000 0000

D6 - D0 bits set the minimum duration of the Interrupt 2 event to be recognized. Duration time steps and maximum values depend on the ODR chosen.

7.1.22 CLICK_CFG_A (38h)

Table 58. CLICK_CFG_A register

--	--	ZD	ZS	YD	YS	XD	XS

Table 59. CLICK_CFG_A description

ZD	Enable interrupt double CLICK on Z axis. Default value: 0 (0: disable interrupt request, 1: enable interrupt request on measured accel. value higher than preset threshold)
ZS	Enable interrupt single CLICK on Z axis. Default value: 0 (0: disable interrupt request, 1: enable interrupt request on measured accel. value higher than preset threshold)
YD	Enable interrupt double CLICK on Y axis. Default value: 0 (0: disable interrupt request, 1: enable interrupt request on measured accel. value higher than preset threshold)
YS	Enable interrupt single CLICK on Y axis. Default value: 0 (0: disable interrupt request, 1: enable interrupt request on measured accel. value higher than preset threshold)
XD	Enable interrupt double CLICK on X axis. Default value: 0 (0: disable interrupt request, 1: enable interrupt request on measured accel. value higher than preset threshold)
XS	Enable interrupt single CLICK on X axis. Default value: 0 (0: disable interrupt request, 1: enable interrupt request on measured accel. value higher than preset threshold)

7.1.23 CLICK_SRC_A (39h)

Table 60. CLICK_SRC_A register

--	IA	DCLICK	SCLICK	Sign	Z	Y	X

Table 61. CLICK_SRC_A description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated, 1: one or more interrupts have been generated)
DCLICK	Double CLICK-CLICK enable. Default value: 0 (0:double CLICK-CLICK detection disable, 1: double CLICK-CLICK detection enable)
SCLICK	Single CLICK-CLICK enable. Default value: 0 (0:Single CLICK-CLICK detection disable, 1: single CLICK-CLICK detection enable)
Sign	CLICK-CLICK Sign. 0: positive detection, 1: negative detection

Table 61. CLICK_SRC_A description (continued)

Z	Z CLICK-CLICK detection. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
Y	Y CLICK-CLICK detection. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
X	X CLICK-CLICK detection. Default value: 0 (0: no interrupt, 1: X high event has occurred)

7.1.24 CLICK_THS_A (3Ah)**Table 62. CLICK_THS_A register**

--	Ths6	Ths5	Ths4	Ths3	Ths2	Ths1	Ths0

Table 63. CLICK_SRC_A description

Ths6-Ths0	CLICK-CLICK threshold. Default value: 000 0000

1 LSB = full-scale / 128. THS6 through THS0 define the threshold which is used by the system to start the click detection procedure. The threshold value is expressed over 7 bits as an unsigned number.

7.1.25 TIME_LIMIT_A (3Bh)**Table 64. TIME_LIMIT_A register**

--	TLI6	TLI5	TLI4	TLI3	TLI2	TLI1	TLI0

Table 65. TIME_LIMIT_A description

TLI7-TLI0	CLICK-CLICK time limit. Default value: 000 0000

1 LSB = 1/ODR. TLI7 through TLI0 define the maximum time interval that can elapse between the start of the click detection procedure (the acceleration on the selected channel exceeds the programmed threshold) and when the acceleration goes back below the threshold.

7.1.26 TIME_LATENCY_A (3Ch)**Table 66. TIME_LATENCY_A register**

TLA7	TLA6	TLA5	TLA4	TLA3	TLA2	TLA1	TLA0

Table 67. TIME_LATENCY_A description

TLA7-TLA0	CLICK-CLICK time latency. Default value: 000 0000

1 LSB = 1/ODR. TLA7 through TLA0 define the time interval that starts after the first click detection where the click detection procedure is disabled, in cases where the device is configured for double click detection.

7.1.27 TIME_WINDOW_A (3Dh)

Table 68. TIME_WINDOW_A register

TW7	TW6	TW5	TW4	TW3	TW2	TW1	TW0

Table 69. TIME_WINDOW_A description

TW7-TW0	CLICK-CLICK time window

1 LSB = 1/ODR. TW7 through TW0 define the maximum interval of time that can elapse after the end of the latency interval in which the click detection procedure can start, in cases where the device is configured for double click detection.

7.2 Magnetic field sensing register description

7.2.1 CRA_REG_M (00h)

Table 70. CRA_REG_M register

TEMP_EN	0 ⁽¹⁾	0 ⁽¹⁾	DO2	DO1	DO0	0 ⁽¹⁾	0 ⁽¹⁾

1. This bit must be set to '0' for correct working of the device

Table 71. CRA_REG_M description

TEMP_EN	Temperature sensor enable. 0: temperature sensor disabled (default), 1: temperature sensor enabled
DO2 to DO0	Data output rate bits. These bits set the rate at which data is written to all three data output registers (refer to Table 72). Default value: 100

Table 72. Data rate configurations

DO2	DO1	DO0	Minimum data output rate (Hz)
0	0	0	0.75
0	0	1	1.5
0	1	0	3.0
0	1	1	7.5
1	0	0	15
1	0	1	30

Table 72. Data rate configurations (continued)

DO2	DO1	DO0	Minimum data output rate (Hz)
1	1	0	75
1	1	1	220

7.2.2 CRB_REG_M (01h)

Table 73. CRA_REG register

GN2	GN1	GN0	0 ⁽¹⁾	0 ⁽¹⁾	0 ⁽¹⁾	0 ⁽¹⁾	0 ⁽¹⁾

1. This bit must be set to '0' for correct working of the device.

Table 74. CRA_REG description

GN1-0	Gain configuration bits. The gain configuration is common for all channels (refer to Table 75)

Table 75. Gain setting

GN2	GN1	GN0	Sensor input field range [Gauss]	Gain X, Y, and Z [LSB/Gauss]	Gain Z [LSB/Gauss]	Output range
0	0	1	±1.3	1100	980	0xF800–0x07FF (-2048–2047)
0	1	0	±1.9	855	760	
0	1	1	±2.5	670	600	
1	0	0	±4.0	450	400	
1	0	1	±4.7	400	355	
1	1	0	±5.6	330	295	
1	1	1	±8.1	230	205	

7.2.3 MR_REG_M (02h)

Table 76. MR_REG

0 ⁽¹⁾	0 ⁽¹⁾	0 ⁽¹⁾	0 ⁽¹⁾	0 ⁽¹⁾	0 ⁽¹⁾	MD1	MD0

1. This bit must be set to '0' for correct working of the device.

Table 77. MR_REG description

MD1-0	Mode select bits. These bits select the operation mode of this device (refer to Table 78)

Table 78. Magnetic sensor operating mode

MD1	MD0	Mode
0	0	Continuous-conversion mode
0	1	Single-conversion mode
1	0	Sleep-mode. Device is placed in sleep-mode
1	1	Sleep-mode. Device is placed in sleep-mode

7.2.4 OUT_X_H_M (03), OUT_X_LH_M (04h)

X-axis magnetic field data. The value is expressed as 2's complement.

7.2.5 OUT_Z_H_M (05), OUT_Z_L_M (06h)

Z-axis magnetic field data. The value is expressed as 2's complement.

7.2.6 OUT_Y_H_M (07), OUT_Y_L_M (08h)

Y-axis magnetic field data. The value is expressed as 2's complement.

7.2.7 SR_REG_M (09h)**Table 79. SR register**

--	--	--	--	--	--	LOCK	DRDY

Table 80. SR register description

LOCK	Data output register lock. Once a new set of measurements is available, this bit is set when the first magnetic field data register has been read.
DRDY	Data ready bit. This bit is set when a new set of measurements are available.

7.2.8 IR_REG_M (0Ah/0Bh/0Ch)**Table 81. IRA_REG_M**

0	1	0	0	1	0	0	0

Table 82. IRB_REG_M

0	0	1	1	0	1	0	0

Table 83. IRC_REG_M

0	0	1	1	0	0	1	1

7.2.9 TEMP_OUT_H_M (31h), TEMP_OUT_L_M (32h)

Table 84. TEMP_OUT_H_M register

TEMP11	TEMP10	TEMP9	TEMP8	TEMP7	TEMP6	TEMP5	TEMP4

Table 85. TEMP_OUT_L_M register

TEMP3	TEMP2	TEMP1	TEMP0	--	--	--	--

Table 86. TEMP_OUT resolution

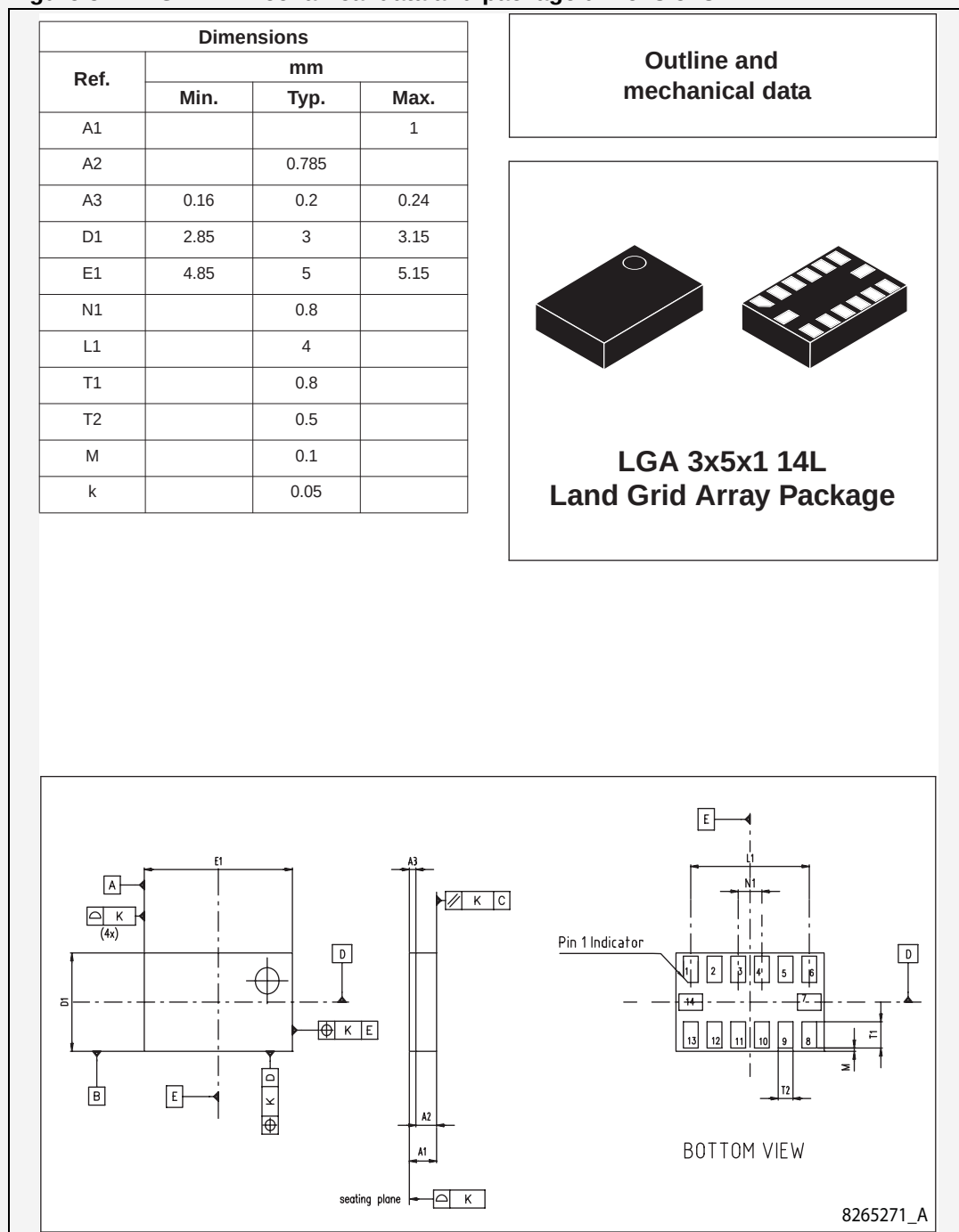
TEMP11-0	Temperature data (8LSB/deg - 12-bit resolution). The value is expressed as 2's complement.



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 5. LGA-14: mechanical data and package dimensions



9 Revision history

Table 87. Document revision history

Date	Revision	Changes
21-Apr-2011	1	Initial release.



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Preface

Read This First

About This Manual

This manual should be used by software and hardware developers of applications based on the OMAP4460 chipset. This document describes the OMAP4460 Pandaboard ES hardware. This document also gives the user information about the different interfaces on the OMAP4460 Pandaboard ES.

Related Documentation

- OMAP4460 Technical Reference Manual
- OMAP4460 Pandaboard ES Schematic (750-2170-002-SCH)
- OMAP4460 Pandaboard ES Gerber Files (720-2170-004)
- OMAP4460 Pandaboard ES Bill-of-Materials (750-2170-002-EBOM)

Revision History

Revision History

Rev	Changes	Date
0.1	Preliminary Release	29 Sept. 2011

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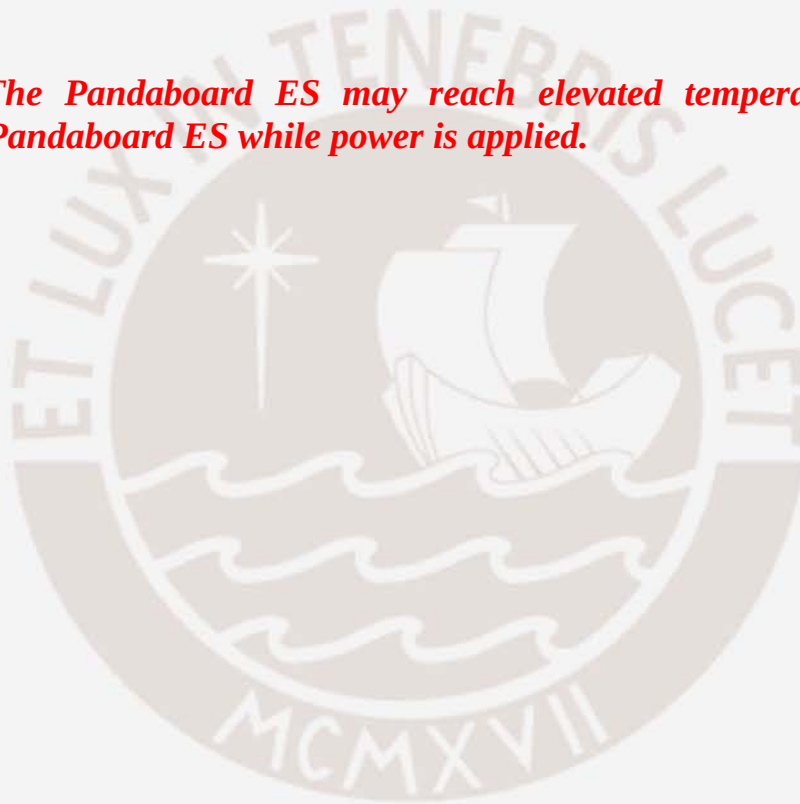
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1 Introduction

This document is the System Reference Manual for the Pandaboard ES, a low cost OMAP4460 based board supported through <http://Pandaboard.org>. This includes system setup and debugging. This document provides detailed information on the overall design and usage of the Pandaboard ES from the System perspective.

CAUTION: The Pandaboard ES may reach elevated temperatures. Avoid handling the Pandaboard ES while power is applied.



1.1 OMAP4460 Pandaboard ES Overview

Pandaboard ES is an OMAP4460 platform designed to provide access to as many of the powerful features of the OMAP4460 Multimedia Processor as possible, while maintaining a low cost. This will allow the user to develop software to utilize the features of the powerful OMAP4460 processor. In addition, by providing expandability via onboard connectors, the Pandaboard ES supports development of additional capabilities/functionality. See Table 1 for a listing of the Pandaboard ES features.

Feature		
Processor	OMAP4460	
POP Memory	Elpida 8Gb LPDDR2 (EDB8064B1PB-8D-F)	
PMIC	TI (TWL6030 Power Management Companion IC)	
Debug Support	14-pin JTAG	GPIO Pins
	UART via DB-9 connector	LEDs
PCB	4.5" x 4.0" (114.3 x 101.6 mm)	8 layers
Indicators	3 LEDs (two user-controlled, one overvoltage indicator)	
HS USB 2.0 OTG Port	Mini-AB USB connector, sourced from OMAP USB Transceiver	
HS USB Host Port	Four USB HS Ports, up to 500mA current out on each, two to onboard connectors, two to expansion connectors	
Audio Connectors	3.5mm, L+R out	3.5mm, Stereo In
SD/MMC Connector	6 in 1 SD/MMC/SDIO	4/8 bit support, Dual voltage
User Interface	1-User defined button	Reset Button
	SYSBOOT3 switch	
Video	DVI-D or HDMI	Optional user provided plug-in display
Power Connector	USB Power	DC Power
Camera	Not included, but supported via camera expansion connector	
Expansion Connectors (not populated)	See Paragraph 2.17 on page 41	
Parallel LCD Expansion Connectors (not populated)	See Paragraph 2.13.1 on page 32	
DSI LCD Expansion Connector (not populated)	See Paragraph 2.13.2 on page 34	

Table 1: Pandaboard ES Features

1.2 Overview of the OMAP4460 Pandaboard ES Kit Contents

The OMAP4460 Pandaboard ES kit contains the following items:

- 1 Pandaboard ES
- Board packing material
- 1 Shipping Box

The following items can be used with the Pandaboard ES, but are NOT included in the kit.

- USB Cable (mini-AB to Type A)
- HDMI Cable (Type A)
- DB-9 Male-to-female cable (straight-through)
- HDMI-A Male to DVI-D Cable
- DC wall supply (+5Vdc, 2.0mm center pin diameter/6.5mm outer hole diameter jack)

2 OMAP4460 Pandaboard ES Architecture

This chapter explains the architecture of the OMAP4460 Pandaboard ES.

2.1 Overview of the Pandaboard ES Architecture

Shown in Figure 1 is the Architectural Block Diagram of the OMAP4460 Pandaboard ES.

Listed below are the major components used on the Pandaboard ES.

- OMAP4460 Processor
- TWL6030 (Phoenix) Power Management Companion Device
- TWL6040 (Phoenix) Audio Companion Device
- TPS62361 Switching Power Supply
- POP Mobile LPDDR2 SDRAM Memory
- HDMI Connector (Type A) – for OMAP4460 HDMI Transmitter output
- HDMI Connector (Type A) – for DVI-D output sourced via OMAP4 parallel display output
- Audio Input & Output Connectors (3.5mm)
- SD/SDIO/MMC Media Card Cage
- UART via RS-232 interface via 9-pin D-Sub Connector
- LS Research Module – 802.11b/g/n, Bluetooth

The Platform also includes connectors that can be used for additional functionality and/or expansion purposes. These connectors are not populated on the platform, but can be installed by the user. They are indicated by the blue blocks in Figure 1, and include:

- Camera Connector (J17)
- Parallel LCD Expansion Connectors (J1 and J4)
- Generic Expansion Connectors (J3 and J6)
- DSI Display Expansion Connector (J7)

See Figure 2 on page 16 for a top side view of the Panda Platform.

The core components of the Pandaboard ES will be discussed in this section of the document. This would include the OMAP4460 Processor and its POP LPDDR2 memory, the input clock circuitry, the TWL6030 Power Companion IC, and the TWL6040 Audio Companion IC. The functional interfaces will be discussed in later sections of the document.

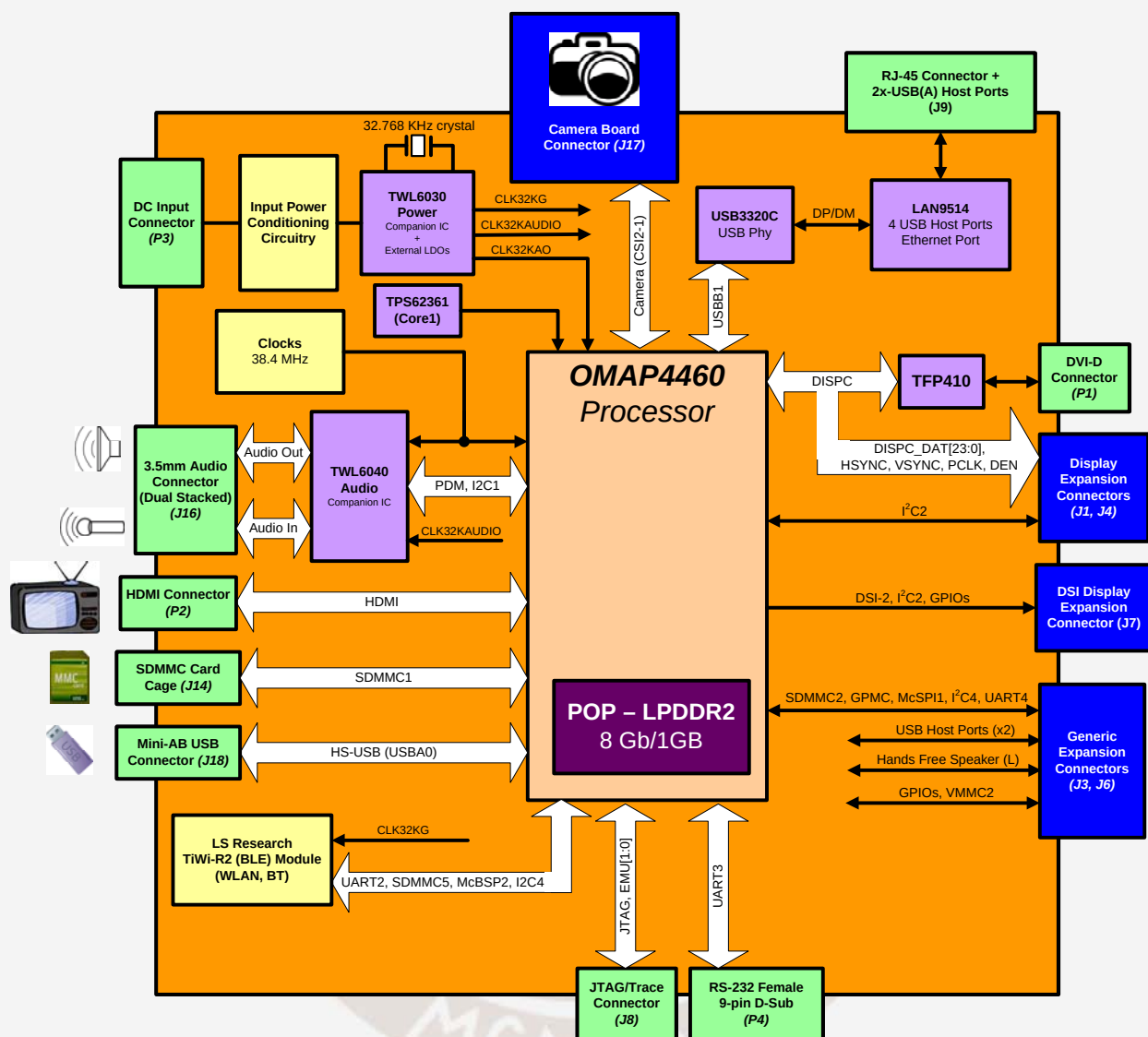


Figure 1 – OMAP4460 Pandaboard ES Architectural Block Diagram

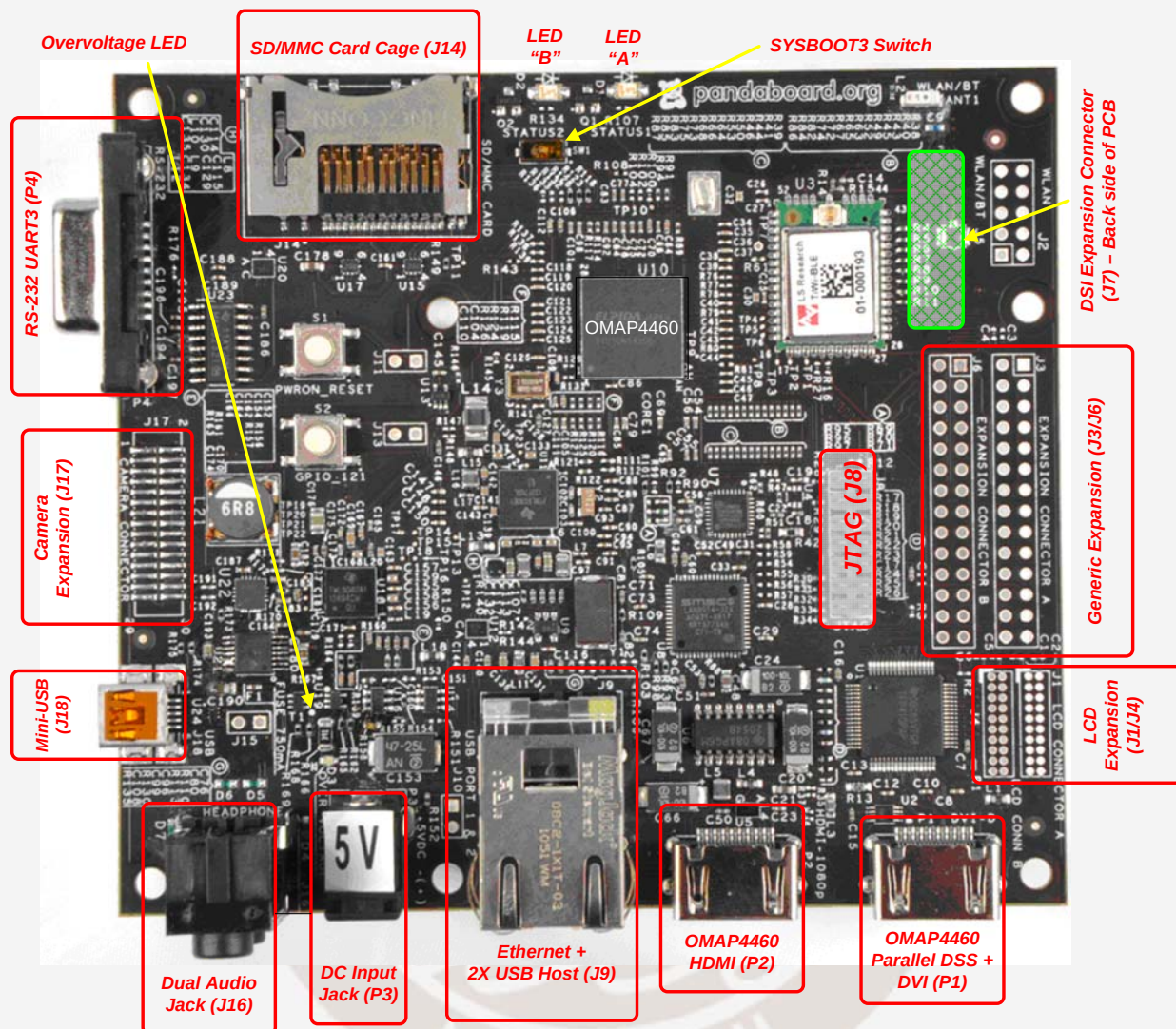


Figure 2 – OMAP4460 Pandaboard ES (Top View)

2.2 System Clock Distribution

The OMAP4460 Pandaboard ES implements a 38.4 MHz 1.8V CMOS square-wave oscillator that directly drives the FREF_SLICER_IN input (ball AG8) of the OMAP4460 processor and the MCLK input to the TWL6040 Audio Companion IC. This clock is used as an input to the PLLs within the OMAP4460 processor so that it can generate all the internal clock frequencies required for system operation.

2.3 OMAP4460 Processor

The heart of Pandaboard ES is the OMAP4460 processor. The OMAP4460 high-performance multimedia application device is based on enhanced OMAP™ architecture and uses 45-nm technology. For more information, refer to the OMAP4460 Technical Reference Manual (TRM). The architecture is designed to provide best-in-class video, image, and graphics processing sufficient to various applications. The device supports the following functions:

- Streaming video up to full high definition (HD) (1920 × 1080 p, 30 fps)
- 2-dimensional (2D)/3-dimensional (3D) mobile gaming
- Video conferencing
- High-resolution still image (up to 16 Mp)

The device supports high-level operating systems (OSs) such as:

- Windows™ CE, WinMobile™
- Symbian OS™
- Linux®
- Palm OS™

The device is composed of the following subsystems:

- Cortex™-A9 microprocessor unit (MPU) subsystem, including two ARM® Cortex-A9 cores capable of operation at 1.2GHz
- Digital signal processor (DSP) subsystem
- Image and video accelerator high-definition (IVA-HD) subsystem
- Cortex™-M3 MPU subsystem, including two ARM Cortex-M3 microprocessors
- Display subsystem
- Audio back-end (ABE) subsystem
- Imaging subsystem (ISS), consisting of image signal processor (ISP) and still image coprocessor (SIMCOP) block
- 2D/3D graphic accelerator (SGX) subsystem
- Emulation (EMU) subsystem

The device includes state-of-art power-management techniques required for high-performance mobile products. Comprehensive power management is integrated into the device. The device also integrates:

- On-chip memory
- External memory interfaces
- Memory management
- Level 3 (L3) and level 4 (L4) interconnects

- System and connecting peripherals

2.4 TPS62361 External Power Supply (VDD_MPU)

The VDD_MPU balls on the OMAP4460 processor that power the ARM cores are supplied by an external switch mode supply at U25. This device is a Texas Instruments TPS62361 switch mode supply that is controllable via the smart reflex I2C interface of the OMAP4460 processor. Additionally, the VSEL0 ball of the converter is controlled by an OMAP GPIO (GPIO_WK7). This part may be found on sheet 2 of the schematics.

2.5 TWL6030 Power Companion IC

The TWL6030 device is a small (7 x 7 mm, 0.4mm pitch) 256 ball FBGA that provides many functions used on the Platform. Shown below is a feature list of the major functions/interfaces provided by the TWL6030 device that are utilized on the Panda platform. This list below doesn't include all device functionality, just that which is used on the Pandaboard ES.

- A power management system (FSM)
- 1 HS-I2C interface ($\leq 2.4\text{Mbits/s}$) for all Phoenix Power IC GP control commands (CTL-I2C)
- 1 HS-I2C interface ($\leq 2.4\text{Mbits/s}$) for all Smart-Reflex Class 3 control commands (SR-I2C)
- MMC card detection mechanism
- A 24MHz RC oscillator
- A 32kHz RC oscillator for a fast device start-up
- A high-performance crystal oscillator, for 32.768kHz external crystal
- A Real Time Clock (RTC) resource
- Power supply resources:
 - 11 Low Drop Out (LDO) regulators
 - 1 for internal purposes only (VRTC)
 - 1 for internal and platform needs (VANA)
 - 9 for platform needs (VAUX1, VAUX2, VAUX3, VCXIO, VDAC, VMMC, VPP, VUSB, VUSIM)
 - 7 buck SMPS with:
 - DVS capability Smart-Reflex Class 3 compatible (VCORE1, VCORE2, VCORE3)
 - 1 for I/O supply (V1V8), with specific PWMFORCE input control
 - 1 for LDOs pre-regulation (V2V1) and Phoenix Audio features
 - 1 for memory supply (VMEM)
 - 1 for external modem, RF transceiver or I/Os (V1V29)
- 3 general-purpose enables for possible platform upgrades (REGEN1, REGEN2, SYSEN)

2.5.1 TWL6030 Core SMPS Outputs

The TWL6030 implements three Switch Mode Power Supplies (SMPS) that source two of the three main core voltage rails for the OMAP4460 processor. The default voltage of all of these supplies is 0.95V, and each should be adjusted as required by S/W for the desired processor OPP.

VCORE1 is a 1200mA SMPS that is used to power the VDD_CORE balls on the OMAP4460 processor (net name VDD_VCORE3, (34 balls total) and the VDDA_DLLn_LPDDR21 and VDDA_DLLn_LPDDR22 balls, where n=0/1 (4 balls total). VCORE2 is a 600mA SMPS that is used to power the VDD_IVA_AUDIO balls on the processor (net name VDD_VCORE2, 10 balls total). VCORE3 is a 600mA SMPS that is not used on the OMAP4460 Pandaboard ES.

2.5.2 TWL6030 V1V8 SMPS Output

The TWL6030 V1V8 SMPS provides the I/O voltage for the Pandaboard ES (net name VIO_1v8). This is a 1200mA SMPS that provides a 1.8V output that is used to power many balls on the OMAP4460 processor that set the I/O voltage for the device. It also sources onboard peripherals that require an operating voltage referenced to processor I/Os.

2.5.3 TWL6030 V2V1 SMPS Output

The TWL6030 V2V1 SMPS output is used by the TWL6040 Audio Companion IC as an input for some of its internal power supplies (specifically the high side and low side LDOs and the negative charge pump). It is also connected to the TWL6030 as the input voltage to the VCXIO and VDAC LDOs (net name VDD_2V1). It is a 600mA SMPS with a default output value of 2.10V.

2.5.4 TWL6030 VMEM SMPS Output

The TWL6030 VMEM SMPS is not used on the OMAP4460 Pandaboard ES. The LPDDR2 power balls on the OMAP4460 that were previously connected to this rail for the OMAP4430 are connected to the V1V29 SMPS.

2.5.5 TWL6030 V1V29 SMPS Output

The TWL6030 V1V29 output is a 600mA SMPS used to provide the operating voltage for the VDD2 LPDDR2 balls on the OMAP4460 processor (net name VDD_VMEM). These OMAP balls are feed-throughs to the top POP footprint on the OMAP package, where they directly connect to the LPDDR2 VDD2 balls. This SMPS is a 600mA max capacity rail. The Micron LPDDR2 device used is an S4B type device, so VDD2 is required to be 1.2V. This is set in the TWL6030 companion chip by connecting the BOOT1 input to VRTC, which causes V1V29 to be set to a default of 1.225V.

2.5.6 TWL6030 LDO Power Resources

The VAUX2 LDO is a programmable LDO that is only connected to pin 1 of the LCD Expansion Connector J4. Its possible output voltage settings include 1.2V, 1.8V, 2.5V, 2.75V, and 2.8V, and its maximum output current is 200mA. The voltage to be programmed will be dependent on the board plugged into the LCD Expansion connectors, but will most likely be 2.8V.

The VAUX2 LDO is a programmable LDO that is only connected to pin 1 of the LCD Expansion Connector J4. Its possible output voltage settings include 1.2V, 1.8V, 2.5V, 2.75V, and 2.8V, and its maximum output current is 200mA. The voltage to be programmed will be dependent on the board plugged into the LCD Expansion connectors, but will most likely be 2.8V.

The VAUX3 LDO is a programmable LDO that is only connected to pin 30 of the Camera Expansion Connector, J17. Its possible output voltage settings include 1.0V, 1.2V, 1.3V, 1.8V, 2.5V, 2.8V, 3.0V, and its maximum output current is 200mA. The output voltage to be utilized would depend on the implementation of the camera module.

The VCXIO LDO is a fixed 1.8V, 200mA LDO that provides a 1.8V input to certain noise sensitive OMAP4460 balls. The balls powered by this LDO include the VDDA_CSI2 balls (V28 and W28), the VDDA_DPLL balls (G13, P9 and Y16), and on this revision of the Pandaboard ES, the VDDS_DV_BANK7 ball (M28). This LDO also provides power for the onboard 38.4 MHz oscillator.

The VDAC LDO is a fixed 1.8V, 50mA LDO that provides a 1.8V input to certain noise sensitive OMAP4460 balls. The balls powered by this LDO include the VDDA_HDMI_VDAC balls (A11 and G12).

The VMMC LDO is a programmable LDO that provides the voltage to the VDDS_MMC1 balls on the OMAP processor (pins G7 and H7) as well as the SDMMC cardcage. This LDO is off when the board is powered on, but is turned on and set to 1.8V or 3.0V depending on card capabilities detected.

The VRTC LDO is an adjustable LDO that provides internal voltages to the TWL6030 device. Its possible output voltage settings are 1.8V and 2.5V and its maximum output current is 25mA. In normal operation, it should always be set to 1.8V.

The VUSB LDO is a fixed 3.3V, 35mA LDO that provides voltage to the OMAP4460 that it uses for its internal USB transceiver. The only ball powered by this LDO is the VDDA_USBA00TG_3P3V ball (ball A5).

The VPP LDO is adjustable LDO that powers the VPP_CUST and VPP_STD balls on OMAP (balls J8 and Y22). This LDO is only needed for eFuse operations and can be left disabled for normal Pandaboard ES operation.

2.5.7 TWL6030 Clock Circuitry

The TWL6030 has an 32.768 KHz crystal connected across its OSC32KIN and OSC32KOUT balls. This crystal is used by the TWL6030 to generate three output 32.768 KHz, 1.8V square wave clock outputs. These outputs are:

CLK32KAO: always on clock connected to the SYS32K input of the OMAP4460 processor.

CLK32KAUDIO: clock connected to the CLK32K input of the TWL6040 Audio Companion IC.

CLK32KG: a gated 32.768 clock connected to the SLOW_CLK input of the LS Research module. This clock will be off by default at reset, and must be enabled by software.

2.6 TWL6040 Audio Companion IC

The TWL6040 device is a small (6 x 6 mm, 0.5mm pitch) 120 ball PBGA that provides many functions, primarily audio, used on the Platform. Shown below is a feature list of the major functions/interfaces provided by the TWL6040 device.

- A audio management system
 - PDM Interface for Audio and control
 - Analog Microphone Interface
 - Headset – speaker (32 ohm) and microphone
 - Earpiece Output
 - Aux Output
 - Hands-free 8 ohm driver
 - Dual Vibrator
- Misc Control
 - GPO
 - I2C (high speed)
 - Power on/off
- Power
 - Internal LDOs
 - Internal negative charge pump

2.7 SYSBOOT Configuration

The OMAP4460 Processor has eight SYSBOOT inputs. These inputs are sampled after a board reset, and determine the booting and operating mode of the OMAP4460 Processor. The upper two inputs (SYSBOOT[7:6]) control the clocking modes of the part (i.e. enabling/disabling the internal oscillator to allow using a crystal input or oscillator). They are currently set to “11” and should not be changed.

The lower six inputs, SYSBOOT[5:0] determine the type and order of memory or peripheral booting. SYSBOOT[5] determines whether memory or peripheral booting is preferred. The SYSBOOT definitions may be found in the OMAP4460 TRM, but are included here for convenience. See Table 2 on page 24 for the SYSBOOT definitions for peripheral preferred booting, and Table 3 on page 25 for memory preferred booting SYSBOOT definitions. The shaded row(s) in Table 2 are the default configuration of the Pandaboard ES, depending on the setting of SW1.

If it is desired to change the SYSBOOT configuration, resistors may be added or removed from the SYSBOOT[5:0] lines (except for SYSBOOT3, which may be changed by changing the position of switch SW1). The SYSBOOT[5:0] lines have weak internal pull-down resistors inside the OMAP4460, so removing the onboard resistor will result in the line being sampled as a ‘0’ at reset, and installing a 3.3K

or lower value resistor will result in the line being sampled as a '1' at reset. See Figure 3 on page 23 for the location of the resistors on SYSBOOT[5:0]. These resistors are connected to OMAP4460 as follows:

- SYSBOOT0: R123
- SYSBOOT1: R138
- SYSBOOT2: R128
- SYSBOOT3: N/A (controlled by switch SW1)
- SYSBOOT4: R137
- SYSBOOT5: R139

NOTE: Do not use pull-up resistance values higher than 3.3Kohm on the SYSBOOT lines. This would create a voltage divider with the internal OMAP pulldown, potentially causing an invalid value to be internally latched for SYSBOOT.





SYSBOOT[5:0]	Booting Devices Order			
	1 st	2 nd	3 rd	4 th
000000	USB	MMC2(1)		
000001	USB	XIP		
000010	USB	XIPWAIT		
000011	USB	NAND		
000100	USB	EMIF		
000101	USB	MMC1		
000110	USB	OneNAND		
000111	USB	OneNAND	MMC2(1)	
001000	UART	MMC2(1)		
001001	UART	XIP		
001010	UART	XIPWAIT		
001011	UART	NAND		
001100	UART	EMIF		
001101	UART	MMC1		
001110	UART	OneNAND		
001111	USB-ULPI	MMC2(1)		
010000	USB-ULPI	XIP		
010001	USB-ULPI	XIPWAIT		
010010	USB-ULPI	NAND		
010011	USB-ULPI	EMIF		
010100	USB-ULPI	MMC1		
010101	USB-ULPI	OneNAND		
010110	USB	UART	MMC1	MMC2(1)
010111	USB	UART	MMC1	XIP
011000	USB-ULPI	UART	MMC2(2)	
011001	USB	UART	MMC1	NAND
011010	UART	MMC2(2)		
011011	USB	UART	MMC1	
011100	USB	MMC2(2)		
011101	Reserved			
011110	Reserved			
011111 ⁽¹⁾	Fast XIP booting. Wait monitoring off		USB	UART

⁽¹⁾ Only on GP devices

Table 2: SYSBOOT[5:0] Definitions – Peripheral Preferred Booting

SYSBOOT[5:0]	Booting Devices Order			
	1 st	2 nd	3 rd	4 th
100000	MMC2(1)	USB		
100001	XIP	USB		
100010	XIPWAIT	USB		
100011	NAND	USB		
100100	EMIF	USB		
100101	MMC1	USB		
100110	OneNAND	USB		
100111	OneNAND	MMC2(1)	USB	
101000	MMC2(1)	UART		
101001	XIP	UART		
101010	XIPWAIT	UART		
101011	NAND	UART		
101100	EMIF	UART		
101101	MMC1	UART		
101110	OneNAND	UART		
101111	MMC2(1)	USB-ULPI		
110000	XIP	USB-ULPI		
110001	XIPWAIT	USB-ULPI		
110010	NAND	USB-ULPI		
110011	EMIF	USB-ULPI		
110100	MMC1	USB-ULPI		
110101	OneNAND	USB-ULPI		
110110	MMC2(1)	USB	UART	MMC1
110111	XIP	USB	UART	MMC1
111000	MMC2(2)	USB-ULPI	UART	
111001	NAND	USB	UART	MMC1
111010	MMC2(2)	UART		
111011	MMC1	USB	UART	
111100	MMC2(2)	USB		
111101	Reserved			
111110	Reserved			
111111 ⁽¹⁾	Fast XIP booting. Wait monitoring off		USB	UART

⁽¹⁾ Only on GP devices

Table 3: SYSBOOT[5:0] Definitions – Memory Preferred Booting

2.8 Miscellaneous Power Circuitry

2.8.1 Input Power Circuitry

The input power circuitry may be found on sheet 2 of the board schematic. A block diagram of this circuitry is shown in Figure 4 below. The Pandaboard ES may be run either with or without a DC wall supply plugged into the input power jack at P3.

Without an external power supply plugged in, the 5Vdc input power is supplied from the mini-AB USBOTG connector at J18. This supply is only capable of providing 500mA of output current (1A if operating via a USB cable with a “Y” connection to the host), so board operations will be limited in this mode (e.g. operations could be limited, depending on current requirements). The path of current flow in this mode is designated below by the red arrow. The 5V from VBUS will be routed through the switch at U21, to the TPS54320 switching power supply at U22, which provides a 3.7V “battery” voltage for the TWL6030 and TWL6040 Companion ICs.

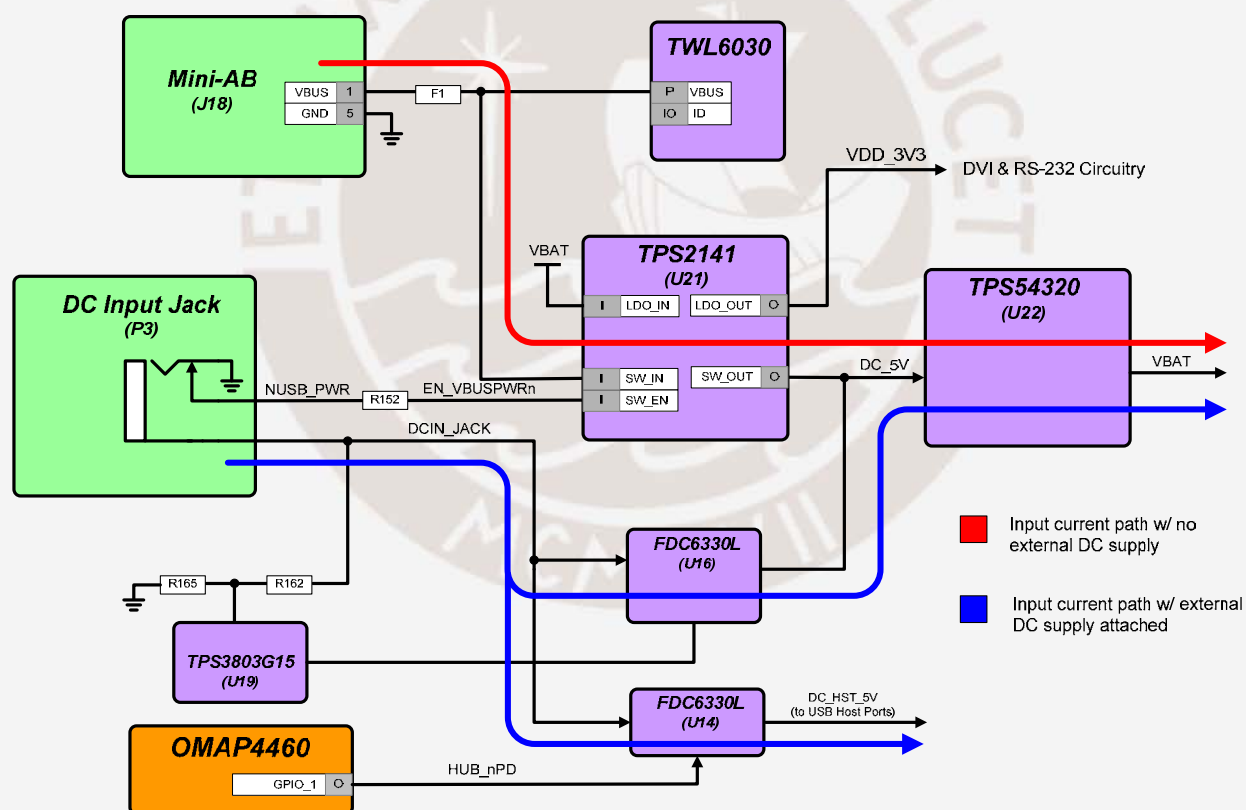


Figure 4 – Pandaboard ES Input Power Circuitry Block Diagram

With an external power supply plugged in, the 5Vdc input power is supplied from the input DC jack at P3. The current capability in this mode is only limited by the particular DC supply being used. The path of current flow in this mode is designated below by the blue arrows. The switch at U21 will be disabled by the insertion of the DC input jack in this mode, and the regulated 5Vdc from the wall supply will be connected to the input of the TPS54320 switching power supply at U22, which provides a 3.7V “battery” voltage for the TWL6030 and TWL6040 Companion ICs.

CAUTION: only use a 5Vdc regulated power supply to power the PandaBoard ES. Connecting a supply with an output higher than +5Vdc could cause possible board damage.

The supervisor IC at U19 has the DC input power tied to its VDD pin through a voltage divider. When the voltage at the VDD input of this IC exceeds 1.40V (i.e. $DCIN\_JACK \geq 5.64V$), the reset output of the supervisor is negated. This will enable the two FETs at T1A and T1B, which will illuminate the red overvoltage indicator, and disable the load switch at U16, which removes input power to the onboard circuitry. The load switch at U14 that provides 5V USB Host power is enabled and disabled manually by writing GPIO_1 to a ‘1’, or a ‘0’, respectively. This load switch powers up disabled.

2.8.2 USB/Ethernet Power Circuitry

There is a fixed 3.3V LDO (U11) that provides power for the LAN9514 Ethernet/USB Hub device. This device is a Texas Instruments TPS73633DBVR device which can provide up to 400mA of output current. This device may be controlled via S/W by writing OMAP4460 GPIO_1. Writing this GPIO high will enable this LDO, while writing it low will disable it (see Table 10 on page 41). This device is shown on sheet 11 of the schematic.

2.9 Standard Volatile Memory

The OMAP4460 processor supports two LPDDR2 channels, accessible only via a POP memory device soldered on the 216-ball, 12x12 mm footprint on top of the OMAP4460 processor. Each channel supports up to two chip-selects, so up to four LPDDR2 memory dies are supported. The two stacked memory packages are directly connected to the two LPDDR2 EMIF4D interfaces of the OMAP4460 die. The base address for the LPDDR2 is 0x8000 0000.

An 8Gb/1GB POP LPDDR2 DRAM device (Elpida P/N EDB8064B1PB-8D-F) is provided on the PandaBoard ES. The memory device has four dies, with each die being a separate 2Gb LPDDR2.

2.10 Debug UART Interface

A single RS-232 port is provided on the Pandaboard ES via 9-pin D-sub female connector at location P4. It provides access to the UART3 interface of the OMAP4460. See Figure 5 for the implementation of the RS232 port.

The TXS0104EZXR device at U20 is a voltage translator that translates between the 1.8V logic levels required by the OMAP4460 processor to the 3.3V logic levels required by the SN75C3232EDR. The SN75C3232EDR @ U23 is an RS-232 transceiver that converts the 3.3V logic signals to/from the voltage translator to the RS-232 signal levels required (-5V to +5V).

The UART port at P4 can be accessed by using Teraterm or other terminal emulation program. To use this UART interface, the serial port settings should be applied as follows:

- BAUD RATE: 115200
- DATA: 8 bit
- PARITY: none
- STOP: 1bit
- FLOW CONTROL: none

This port requires the use of a 9-pin D-sub Male to Female cable.

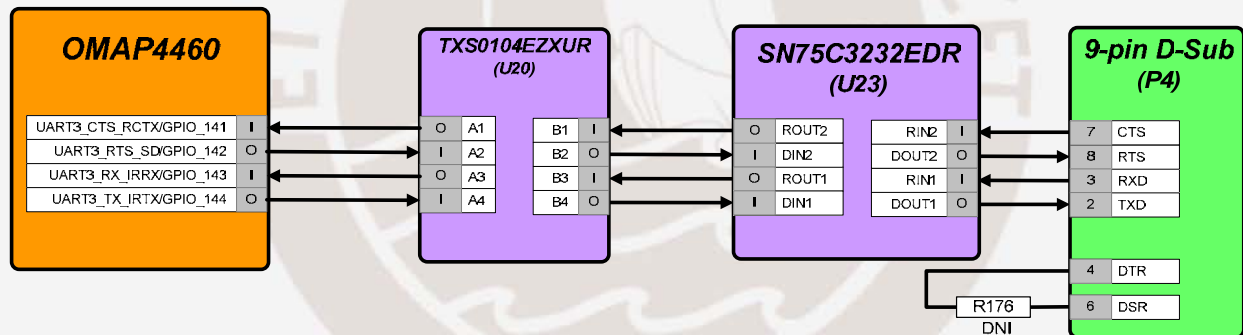


Figure 5 – Panda UART3/RS-232 Block Diagram

2.11 SD/MMC Connector

The OMAP4460 Pandaboard ES supports removable memory storage via onboard SD/MMC card cage. It is an eight-bit card cage that supports 1.8V or 3.0V cards. Card detect functionality is supported via the TWL6030 power companion IC. See Figure 6 for a block diagram of the interface signaling to the card cage. The resistors shown in Figure 6 below are 33 ohm series termination resistors.

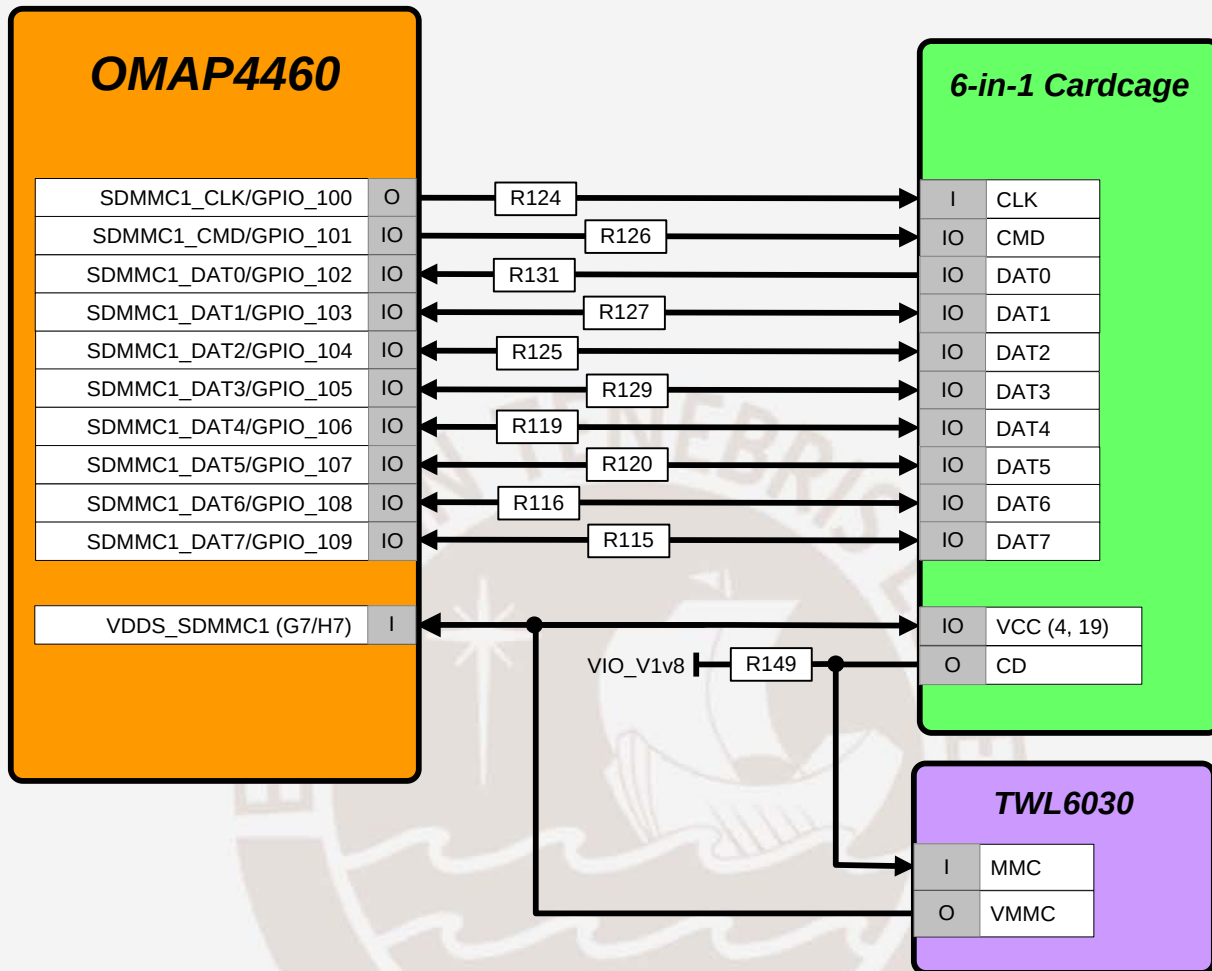


Figure 6 – Panda SDMMC1 Card Cage Block Diagram

2.12 HDMI Interface

The OMAP4460 Pandaboard ES provides a High-Definition Multimedia Interface (HDMI) via an industry-standard Type A connector at location P2. The interface is provided using the internal HDMI module provided by the OMAP4460. See Figure 7 for a block diagram of the Pandaboard ES HDMI circuitry. This interface includes a Texas Instruments TPD12S015A HDMI Port Protection/Interface device. The high-speed differential clock and data lines are connected straight from OMAP to the ESD protection device, to the connector, so that any ESD event experienced at the connector will be absorbed before damaging the OMAP4460 device I/Os.

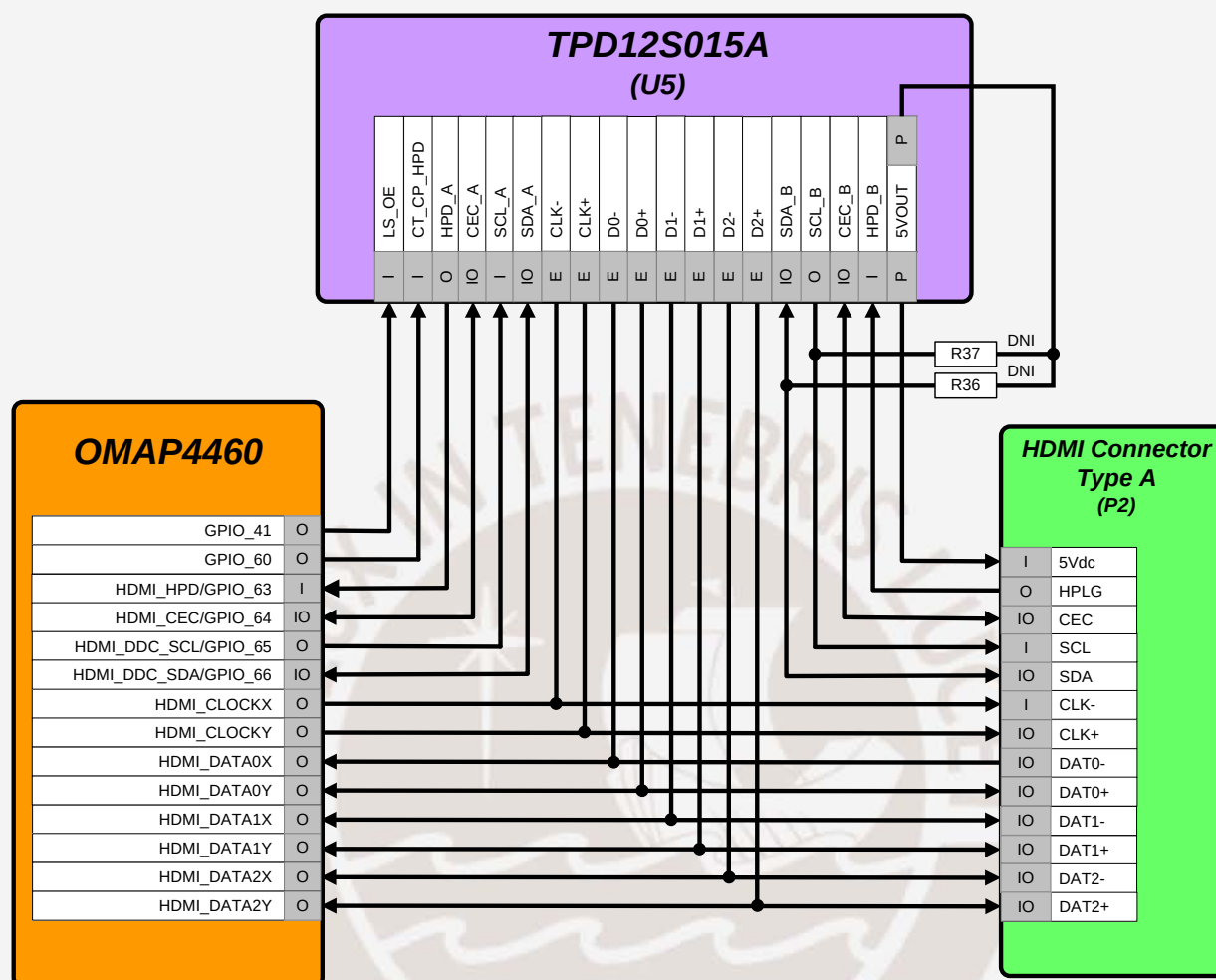


Figure 7 – Panda HDMI Interface Block Diagram

In addition to providing ESD protection on the signals coming from the connector, this device performs voltage translation on the control signals in the HDMI interface (SCL, SDA, CEC, and HPD) from the 1.8V levels of the OMAP4460 to the 5V levels required by a TV set. It also implements a DC/DC boost converter that operates from the “battery” voltage, VBAT, and outputs a 5Vdc output that is capable of sourcing up to 55mA of current. See Table 4 for the GPIOs used on the HDMI interface and a description of their function. The direction column in this table indicates whether this device is an output from OMAP (O) or an input to OMAP (I).

GPIO	Dir	Signal Name	Description
GPIO_41	O	HDMI_LS_OE	TPD12S015A Level Shifter and internal LDO Enable 1 = Enabled, 0 = Disabled
GPIO_60	O	HDMI_CT_CP_HPD	TPD12S015A DC/DC Converter and Hot-Plug Detect Enable 1 = Enabled, 0 = Disabled

Table 4: HDMI GPIO Definitions

2.13 Display Interface

The Pandaboard ES provides two possible options for the usage of the OMAP4460 parallel display signals. The first option is to use the onboard TFP410 DVI transmitter, whose output feeds an onboard DVI-D connector. The second option is to use a Display Board plugged into a pair of 20-pin LCD expansion connectors (J1 and J4). Both of these possible options are discussed in the following paragraphs. Additionally, a third display option has been added to the OMAP4460 Pandaboard ES. This option is using a DSI Display Board plugged into connector J7 on the back side of the PCB. See Figure 8 for a diagram of the Pandaboard ES Display Interface options.

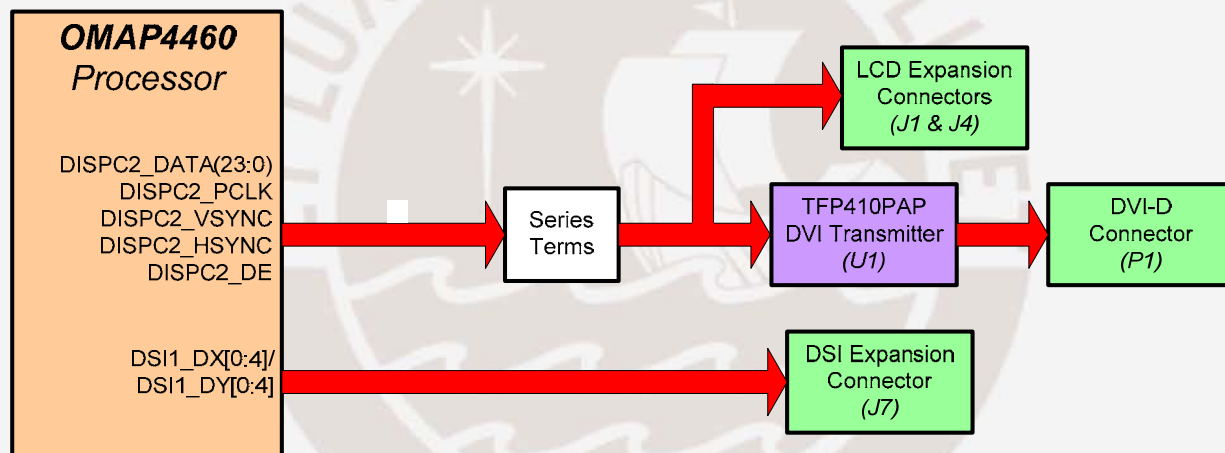


Figure 8 – Panda Display Interface Block Diagram

2.13.1 Parallel Display Interface

See Figure 9 for a detailed block diagram of the OMAP4460 Pandaboard ES parallel display interface. (NOTE: J1/J4 are pin-compatible with the OMAP3530 BeagleBoard, so display boards designed for it may be used with the OMAP4460 Pandaboard ES).

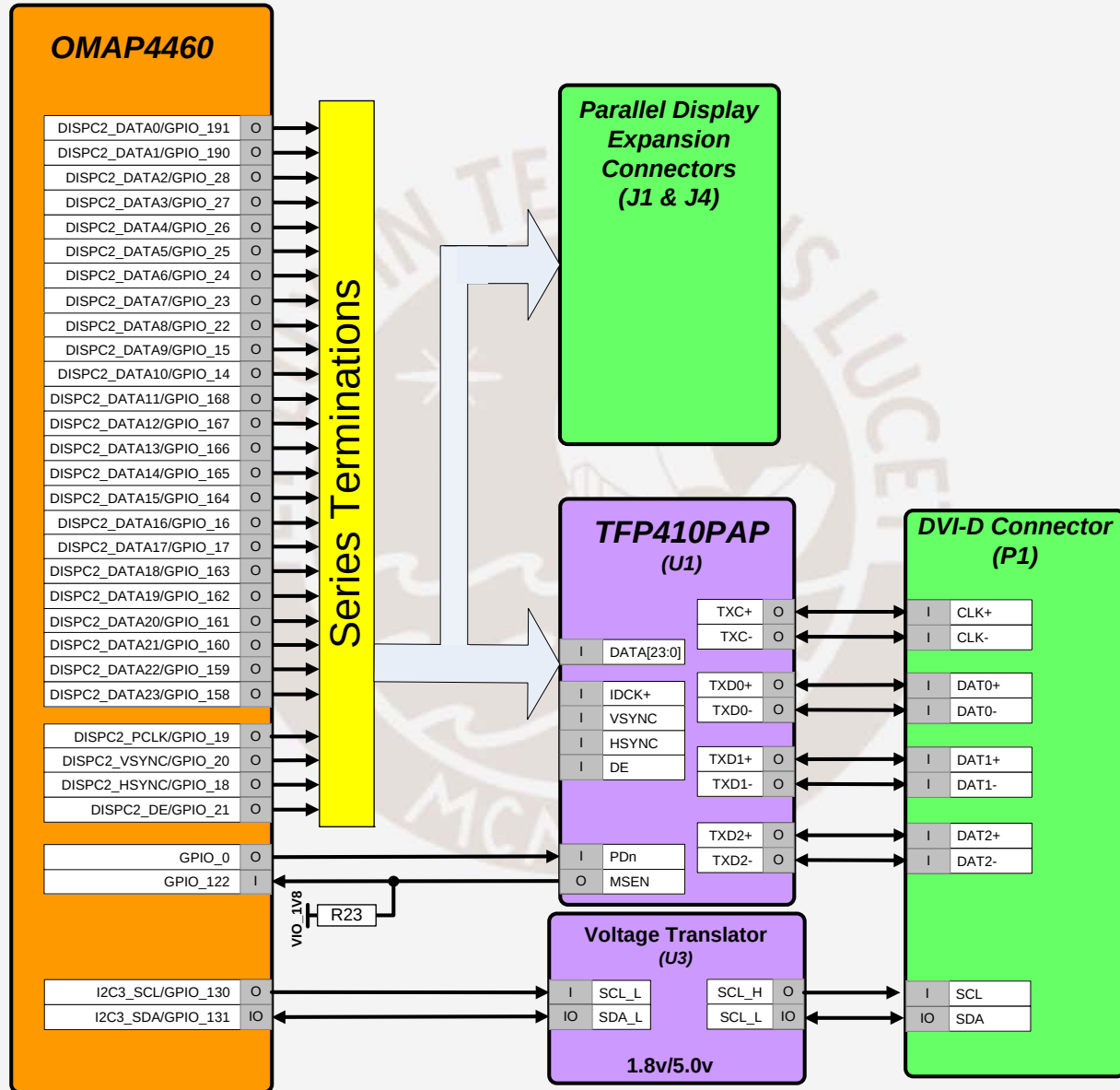


Figure 9 – Pandaboard ES DSS Output Block Diagram

See Table 5 for the GPIOs used on the Parallel display interface and a description of their function. This table does not include the 28 parallel display signals (DATA[23:0], PCLK, VSYNC, HSYNC, and DE).

NOTE: no configuration changes are required to switch between usage of the onboard DVI connector or an external display plugged into the display expansion connectors.

GPIO	Signal Name	Description
GPIO_0	H_GPIO_0/ TFP410_NPD	TFP410 Device Power down (<i>note: this GPIO goes through a voltage translator to meet the 3.3V I/O requirement of the TFP410 on this pin</i>) 1 = Normal Operation, 0 = Power Down
GPIO_122	DVI_MSEN	TFP410 Monitor Sense 0 = Powered on receiver sensed at the differential outputs 1 = No powered on receiver detected. (<i>note: this output from the TFP410 is open-drain and has a pull-up to 1.8V, so it is connected directly to OMAP</i>)

Table 5: DVI-D Display GPIO Definitions

See Table 6 and Table 7 for the pinout of the display expansion connectors.

Pin#	Signal	I/O	Description
1	DCIN_JACK	PWR	DC rail from the Main DC supply
2	DCIN_JACK	PWR	DC rail from the Main DC supply
3	h_DSS_DAT1	I	LCD Pixel Data bit 1
4	h_DSS_DAT0	I	LCD Pixel Data bit 0
5	h_DSS_DAT3	I	LCD Pixel Data bit 3
6	h_DSS_DAT2	I	LCD Pixel Data bit 2
7	h_DSS_DAT5	I	LCD Pixel Data bit 5
8	h_DSS_DAT4	I	LCD Pixel Data bit 4
9	h_DSS_DAT12	I	LCD Pixel Data bit 12
10	h_DSS_DAT10	I	LCD Pixel Data bit 10
11	h_DSS_DAT23	I	LCD Pixel Data bit 23
12	h_DSS_DAT14	I	LCD Pixel Data bit 14
13	h_DSS_DAT19	I	LCD Pixel Data bit 19
14	h_DSS_DAT22	I	LCD Pixel Data bit 22
15	H_I2C2_SDA	I/O	I2C2 Serial Data
16	h_DSS_DAT11	I	LCD Pixel Data bit 11
17	h_DSS_VSYNC	I	LCD Vertical Sync Signal
18	H_DPM_EMU2	I	DPM_EMU2/GPIO_13
19	GND	PWR	Ground bus
20	GND	PWR	Ground bus

Table 6: LCD Expansion Connector “A” Pin Definitions (J1)

Pin#	Signal	I/O	Description
1	VDD_VAUX2	PWR	Power rail (adjustable from 1.2V to 2.8V)
2	VIO_1V8	PWR	1.8V system I/O voltage
3	h_DSS_DAT20	I	LCD Pixel Data bit 20
4	h_DSS_DAT21	I	LCD Pixel Data bit 21
5	h_DSS_DAT17	I	LCD Pixel Data bit 17
6	h_DSS_DAT18	I	LCD Pixel Data bit 18
7	h_DSS_DAT15	I	LCD Pixel Data bit 15
8	h_DSS_DAT16	I	LCD Pixel Data bit 16
9	h_DSS_DAT7	I	LCD Pixel Data bit 7
10	h_DSS_DAT13	I	LCD Pixel Data bit 13
11	h_DSS_DAT8	I	LCD Pixel Data bit 8
12	NUSB_PWR	O	Input Power Enable
13	h_DSS_DAT9	I	LCD Pixel Data bit 9
14	H_I2C2_SCL	I	I2C2 Serial Clock
15	h_DSS_DAT6	I	LCD Pixel Data bit 6
16	h_DSS_PCLK	I	LCD Pixel Clock
17	h_DSS_DEN	I	LCD Data Enable
18	h_DSS_HSYNC	I	LCD Horizontal Sync
19	GND	PWR	Ground bus
20	GND	PWR	Ground bus

Table 7: LCD Expansion Connector “B” Pin Definitions (J4)

2.13.2 DSI Display Expansion Connector Interface

A third display option for the Pandaboard ES is to plug an external display module into the DSI display expansion connector J7. This connector is a 40-pin, 0.8mm pitch connector (Hirose P/N FX6A-40P-0.8SV91), and is mounted on the back side of the Pandaboard ES PCB. See Figure 10 below for the orientation/pin numbering of this connector as viewed from the back side of the PCB.

A block diagram of the Pandaboard ES Display Expansion interface is shown in Figure 11 on page 36.

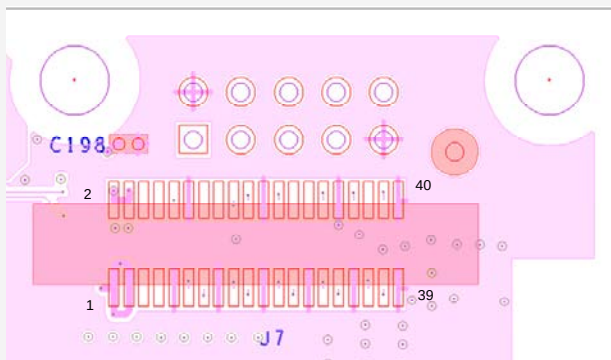


Figure 10 – Panda DSI Display Connector Orientation

See Table 8 for the pinout of J7 and a description of the signals on the connector. Any pin not shown in Table 8 is not connected.

J7 Pin #	OMAP Ball #	Signal Name	Signal Description
1,3	---	VIO_1V8	VIO from TWL6030
2,4	---	VBAT	Battery input voltage
Multiple	---	DGND	Signal Ground (connected on pins 9, 12, 15, 21, 22, 27, 32, 33, 39, and 40)
10	---	PHO_PWM1	PWM1 output of TWL6030 device
11	P3	DSI1_DX0	DSI Signal Lane 0 Data X
13	P4	DSI1_DY0	DSI Signal Lane 0 Data Y
17	N3	DSI1_DX1	DSI Signal Lane 1 Data X
18	C26	h_I2C2_SCL	I ² C Clock In
19	N4	DSI1_DY1	DSI Signal Lane 1 Data Y
20	D26	h_I2C2_SDA	I ² C Data I/O
23	M3	DSI1_DX2	DSI Signal Lane 2 Data X
24	D21	TSC_nINT	Touchscreen Interrupt Out (GPIO_52)
25	M4	DSI1_DY2	DSI Signal Lane 2 Data Y
29	L3	DSI1_DX3	DSI Signal Lane 3 Data X
30	AG24	h_DMTIMER11_PWM	Display PWM (GPIO_121)
31	L4	DSI1_DY3	DSI Signal Lane 3 Data Y
34	B24	h_GPIO_102	LCD Reset (GPIO_102)
35	K3	DSI1_DX4	DSI Signal Lane 4 Data X
37	K4	DSI1_DY4	DSI Signal Lane 4 Data Y
38	A24	H_DSI1_TE0	Display Tearing Effect (GPIO_101)

Table 8: DSI Display Expansion Connector Pin Definitions (J7)

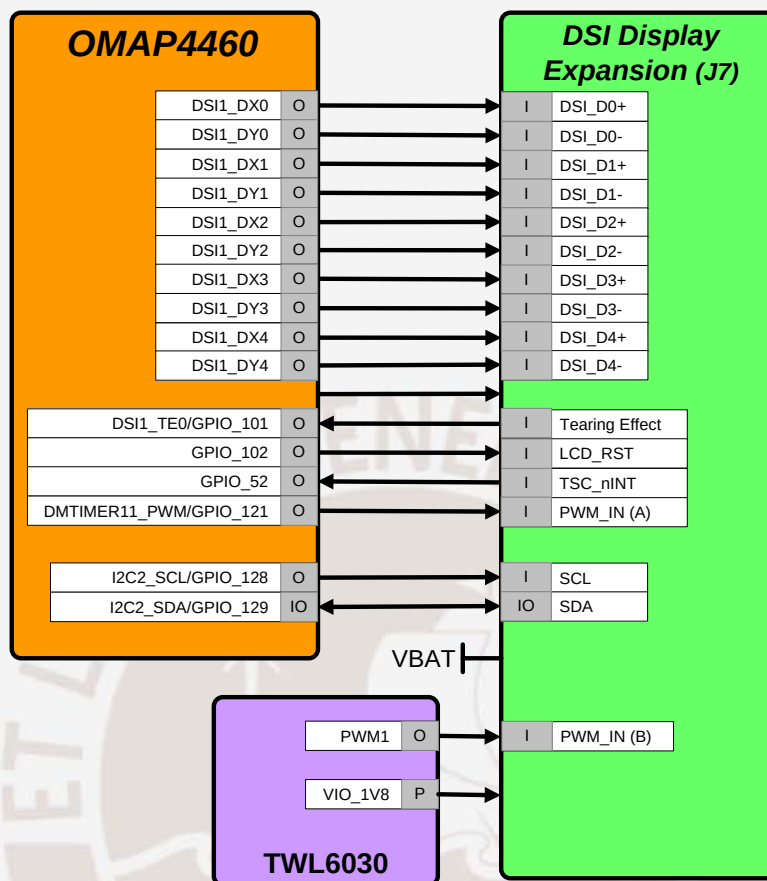


Figure 11 – Panda DSI Display Expansion Block Diagram

2.14 Bluetooth/WLAN Interfaces

The Pandaboard ES provides a module (LS Research Inc. P/N TiWi-BLE) that provides a Bluetooth interface, and a 2.4 GHz 802.11b/g/n interface. This module may be found on sheet 14 of the schematics (reference designator U3). It uses Texas Instruments' WiLink™ 6.0 solution. Information for this module may be found at: <http://www.lsr.com>.

See Figure 12 for a diagram of the Pandaboard ES connectivity to this module. See Table 9 on page 38 for a description of the GPIOs used to interface to the module and their function.

The OMAP4460 interfaces are connected to the LS Research WiLink™ module as follows:

- SDMMC5: WLAN SDIO interface
- UART2: Bluetooth Host Control Interface
- McBSP1: Audio Digital PCM Path

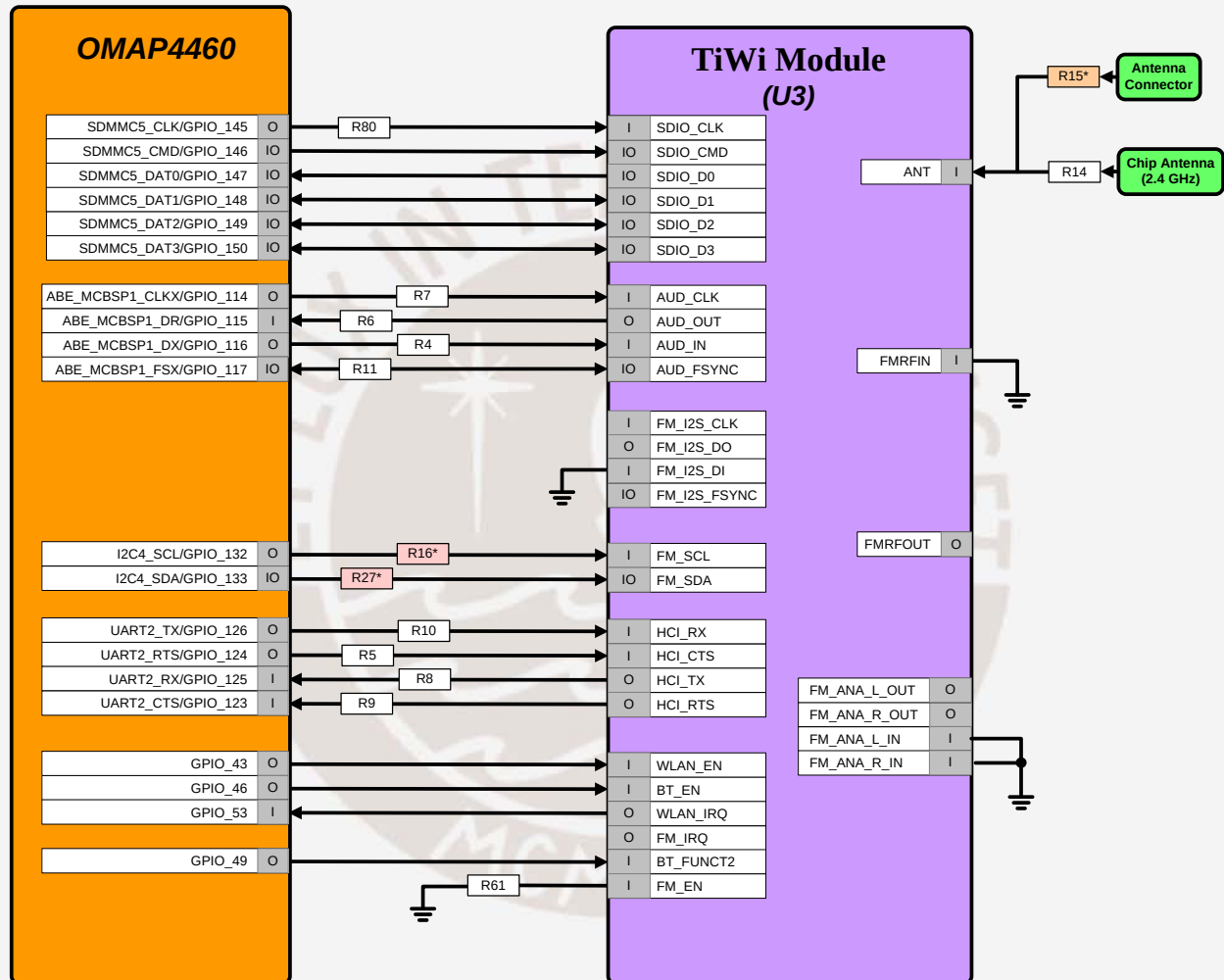


Figure 12 – Pandaboard ES WLAN/Bluetooth Interface Block Diagram

GPIO	Dir.	Signal Name	Description
GPIO_43	O	WLAN_EN	802.11b/g Enable 1 = Enabled, 0 = Disabled
GPIO_46	O	BT_EN	Bluetooth Enable 1 = Enabled, 0 = Disabled
GPIO_49	I	BT_WAKEUP	Bluetooth Wakeup
GPIO_53	I	WLAN_nIRQ	WLAN Interrupt Input

Table 9: WLAN/Bluetooth Module GPIO Definitions

2.15 Audio Interfaces

See Figure 13 for a block diagram of the audio connectivity on the OMAP4460 Pandaboard ES. In this block diagram, the signals with a red background in the box specifying their direction are analog I/Os while all others are 1.8V digital I/Os.

The OMAP4460 Pandaboard ES provides a stacked audio connector, which provides two 3.5mm audio jack connections. The upper jack on this stacked connector (J16A in Figure 13 below), is connected to FM Audio Left and Right inputs of the TWL6040 Audio Companion IC (AFML/AFMR). The lower jack on this stacked connector (J16B in Figure 13 below) is connected to the Headset Right and Left outputs of the TWL6040. Additionally, there is a 2nd possible connection to the TWL6040 Auxiliary outputs (AUXLP/AUXRP). To enable this alternate path, resistors R181 and R182 would need to be removed, and zero ohm, 0402 resistors should be installed at locations R160 and R164.

The digital path for this audio back to the OMAP4460 processor is through the PDM interface. For expansion purposes, the left Hands-Free speaker outputs of the TWL6040 are connected to the Expansion Connector J6 (see Paragraph 2.17 on page 41 for further details).

The Pandaboard ES also provisions a digital PCM path for Bluetooth audio from the module to OMAP4460 via McBSP1.

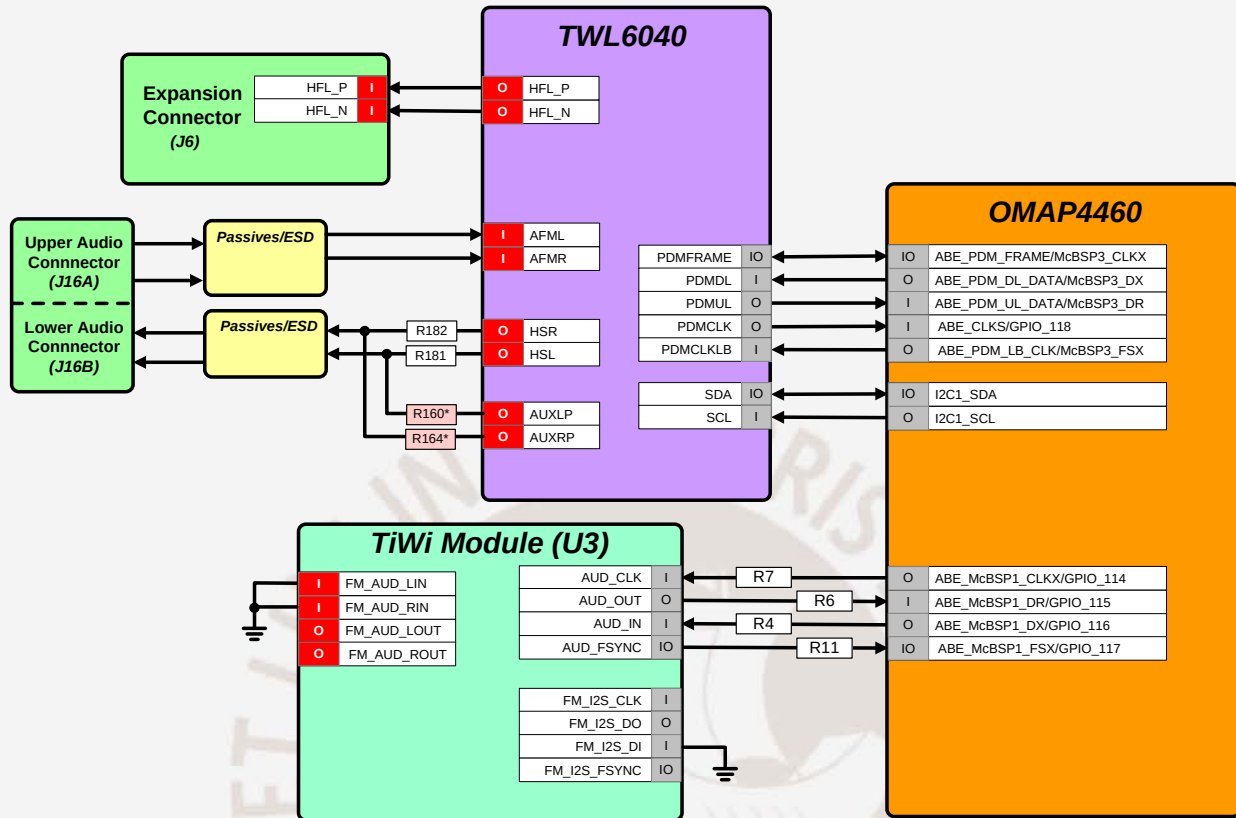


Figure 13 – Panda Audio Interface Block Diagram

2.16 USB Interfaces

The Pandaboard ES utilizes two USB interfaces. The first is a DP/DM interface from the internal transceiver within OMAP to the mini-AB connector J18. The second interface utilizes the 12-wire ULPI interface (USBB1) to an onboard USB phy, whose DP/DM I/Os are interfaced to a Hub IC which provides four downstream USB Host ports, and an Ethernet interface. Each of these interfaces will be discussed in more detail in the following paragraphs.

2.16.1 USBOTG Interface

The Pandaboard ES uses the USB OTG transceiver within the OMAP4460 that is connected to an industry-standard mini-AB connector (J18) as shown in Figure 14. The VBUS from the connector is connected to the TWL6030 companion Power IC, which can provide up to 100mA in host mode (i.e. when a client device is connected). The Pandaboard ES may only be used in host mode if a +5Vdc power supply is installed in power jack P3.

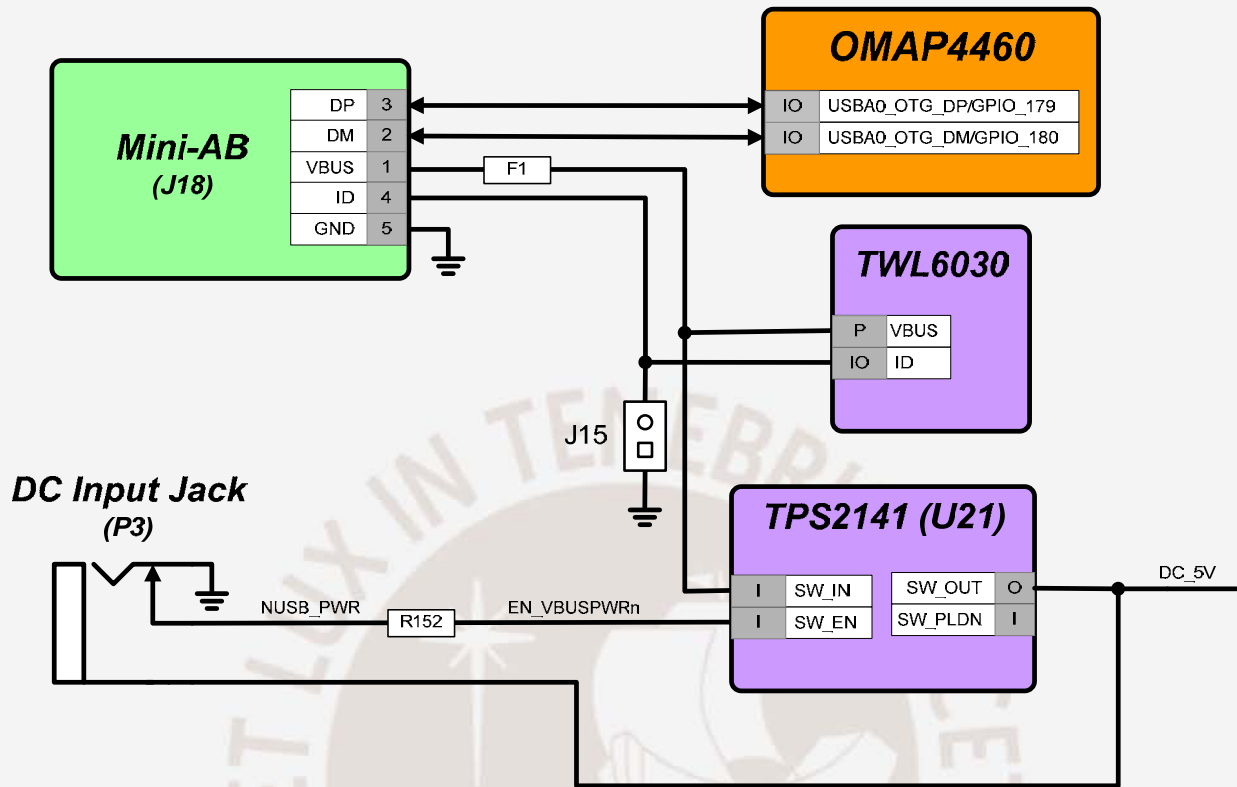


Figure 14 – Panda USBOTG Interface Block Diagram

2.16.2 USBB1 Phy Interface

The Pandaboard ES uses the 12-wire OMAP4460 USBB1 ULPI interface connected to an SMSC USB3320C-EZK phy. This Phy converts the 12-wire ULPI interface to a DP/DM pair that is used as the upstream USB interface to the LAN9514 USB/Ethernet Hub IC. The Hub IC provides four downstream Host USB ports, and an Ethernet interface. Two of the USB Host Ports are available via the combo connector J9, while the other two ports are available via Expansion Connector J6. The Ethernet interface is available via a tab-up RJ-45 connector at J9. See Figure 15 for a block diagram of the Pandaboard ES USBB1 interface connectivity.

- *Note that the reference clock to the USB3320C is sourced from the FREF_CLK3_OUT output of OMAP4460, and this OMAP output must be programmed for a clock frequency of 19.2 MHz for proper operation*

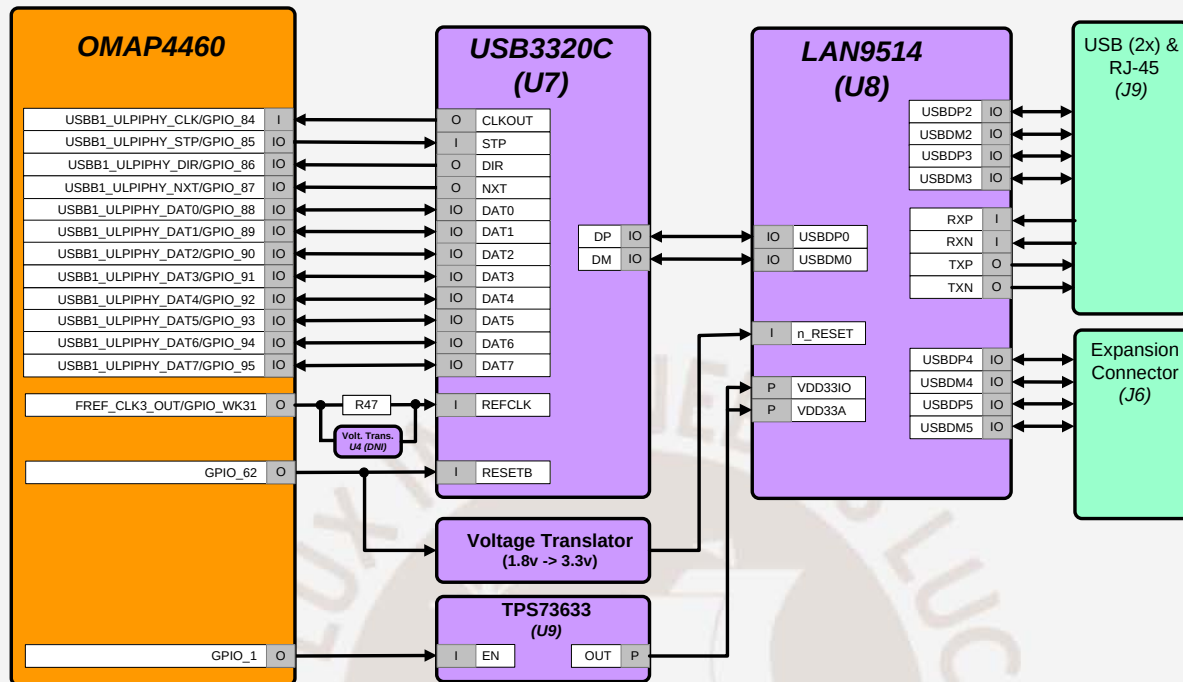


Figure 15 – Panda USBB1 Interface Block Diagram

See Table 10 for the definition of the GPIOs used to provide USB Host Port/Ethernet functions.

GPIO	Dir.	Signal Name	Description
GPIO_1	O	HUB_NPD/ HUB_LDO_EN	Enable to the Hub 3.3V LDO @ U9 (note: this GPIO goes through a voltage translator to provide adequate V_{ih} margin on the LDO enable input). 1 = Enable Hub LDO 0 = Power Down Hub LDO
GPIO_62	O	HUB_NRESET/ HUB_NRESET_3V3	USB/Ethernet Hub Reset 0 = Hub & Phy held in reset 1 = Normal operation.
GPIO_WK31	O	USBB1_PHY_REFCLK	This pin needs to be used as FREF_CLK3_OUT, and programmed to output 19.2 MHz

Table 10: USB Host Port/Ethernet GPIO Definitions

2.17 Expansion Connectors (J3 & J6)

The Pandaboard ES provides locations for two 28-pin, 0.1" through-hole expansion connectors, J3 and J6, to support platform expansion (these connectors are not mounted on the current Pandaboard ES). The placement of these connectors on the Panda PCB is shown below. On both connectors, the top left pin is pin 1 and odd numbered pins are on the top row of the connector, and even numbered pins are on the bottom row. See Figure 16 for the placement and orientation of these two connectors on the Pandaboard ES. The distance between pin 1 of the two connectors is 300 mils or 7.62mm. Note that since these are through-hole connectors, boards can be designed to plug into the Pandaboard ES from either top or bottom, depending on user preference.

See Table 11 for the pinout of expansion connector "A" and Table 12 for the pinout of expansion connector "B". These tables show the primary function that is available on the connector pin, along with the alternate function that can be selected by changing the OMAP4460 pin multiplexing. Some of the OMAP I/Os have more than two possible functions, see Table 22 on page 55 for a complete list of the functions available.

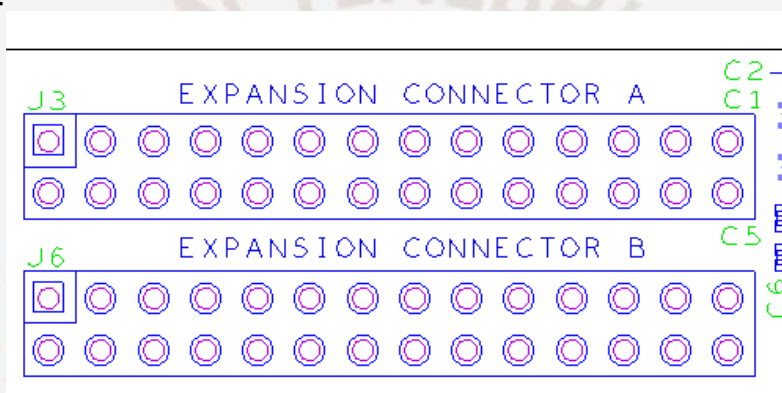


Figure 16 – Expansion Connector PCB Placement/Orientation

J3 Pin #	OMAP Ball #	Primary Function	Secondary Function	Description of Pandaboard ES Usage
1	---	VIO_1V8	---	1.8V I/O Power
2	---	DCIN_JACK	---	5Vdc Input Power
3	B16	GPMC_AD7	SDMMC2_DAT7	GPMC Address/Data Bit 7
4	AH23	MCSP1_CS3	GPIO_140	SPI1 Chip Select 3 (also UART1_RTS)
5	A16	GPMC_AD6	SDMMC2_DAT6	GPMC Address/Data Bit 6
6	AH19	UART4_TX	GPIO_156	UART4 Transmit Data
7	D15	GPMC_AD5	SDMMC2_DAT5	GPMC Address/Data Bit 5
8	AG20	UART4_RX	GPIO_155	UART4 Receive Data
9	C15	GPMC_AD4	SDMMC2_DAT4	GPMC Address/Data Bit 4
10	AF23	MCSP1_CS1	GPIO_138	SPI1 Chip Select 1 (also UART1_RX)
11	D13	GPMC_AD3	SDMMC2_DAT3	GPMC Address/Data Bit 3
12	AG22	MCSP1_SIMO	GPIO_136	SPI1 Slave In Master Out
13	C13	GPMC_AD2	SDMMC2_DAT2	GPMC Address/Data Bit 2
14	AG23	MCSP1_CS2	GPIO_139	SPI1 Chip Select 2 (also UART1_CTS)
15	D12	GPMC_AD1	SDMMC2_DAT1	GPMC Address/Data Bit 1
16	AE23	MCSP1_CS0	GPIO_137	SPI1 Chip Select 0
17	C12	GPMC_AD0	SDMMC2_DAT0	GPMC Address/Data Bit 0
18	AE22	MCSP1_SOMI	GPIO_135	SPI1 Slave Out Master In
19	B12	GPMC_NWE	SDMMC2_CMD	GPMC Write Enable
20	AF22	MCSP1_CLK	GPIO_134	SPI1 Clock Out
21	B11	GPMC_NOE	SDMMC2_CLK	GPMC Output Enable
22	D19	GPMC_AD15	GPIO_39	GPMC Address/Data Bit 15
23	AH22	I2C4_SDA	GPIO_133	I2C4 Serial Data
24	AG21	I2C4_SCL	GPIO_132	I2C4 Serial Clock
25	---	REGEN1	---	TWL6030 REGEN1
26	E7	SYS_NRESPWRON	---	Power On Reset
27	---	DGND	---	Digital Ground
28	---	DGND	---	Digital Ground

Table 11: Expansion Connector “A” Pin Definitions (J3)

J6 Pin #	OMAP Ball #	Primary Function	Secondary Function	Description of Pandaboard ES Usage
1	---	VBUS_3	---	VBUS out from USB Host Port #3
2	---	VBUS_4	---	VBUS out from USB Host Port #4
3	---	USBH3_DM	---	USB Host Port #3 Data Minus
4	---	USBH4_DM	---	USB Host Port #4 Data Minus
5	---	USBH3_DP	---	USB Host Port #3 Data Plus
6	---	USBH4_DP	---	USB Host Port #4 Data Plus
7	---	DGND	---	Digital Ground
8	---	DGND	---	Digital Ground
9	C19	GPMC_AD14	GPIO_38	GPMC Address/Data Bit 14
10	D18	GPMC_AD13	GPIO_37	GPMC Address/Data Bit 13
11	AF7	SYS_NRESWARM	---	Warm Reset
12	---	PB_POWER_ON	---	Power on input to TWL6030 (ref. to VBAT)
13	---	HFL_P	---	Hands Free Left Speaker Out (+)
14	AG24	H_DMTIMER11_PWM	GPIO_121	Display PWM Control
15	---	HFL_N	---	Hands Free Left Speaker Out (-)
16	---	VDD_VAUX1	---	VAUX1 from TWL6030
17	C18	GPMC_AD12	GPIO_36	GPMC Address/Data Bit 13
18	C16	GPMC_AD8	GPIO_32	GPMC Address/Data Bit 8
19	B26	GPMC_WAIT0	GPIO_61	GPMC Wait input 0
20	D16	GPMC_AD9	GPIO_33	GPMC Address/Data Bit 9
21	C25	GPMC_NWP	GPIO_54	GPMC Write Protect
22	C17	GPMC_AD10	GPIO_34	GPMC Address/Data Bit 10
23	B22	GPMC_CLK	GPIO_55	GPMC Clock Out
24	D17	GPMC_AD11	GPIO_35	GPMC Address/Data Bit 11
25	B25	GPMC_NCS0	GPIO_50	GPMC Chip Select 0
26	D25	GPMC_NADV_ALE	GPIO_56	GPMC Address Valid/Address Latch Enable
27	C21	GPMC_NCS1	GPIO_51	GPMC Chip Select 1
28	C23	GPMC_NBE0_CLE	GPIO_59	GPMC Byte Enable 0/Command Latch Enable

Table 12: Expansion Connector “B” Pin Definitions (J6)

2.18 Camera Expansion Connector (J17)

The Pandaboard ES does not provide an onboard camera sensor, but does provision for a 30-pin camera connector. This camera connector receives the five CSI-2 lanes of the OMAP4460 CSI21 camera interface as well as GPIOs for use on a plug-in camera module.

See Table 13 below for the pinout of the camera expansion connector.

NOTE: the GPIOs listed below don’t have specific functions defined yet, as there has been no camera module designed. These GPIOs will be user-definable per the camera module implementation.

J17 Pin #	OMAP Ball #	Signal Name	Signal Description
1	---	DGND	Signal Ground
2	---	DGND	Signal Ground
3	R26	CSI21_DX0	CSI Signal Lane 0 Data X
4	V26	CSI21_DX3	CSI Signal Lane 3 Data X
5	R25	CSI21_DY0	CSI Signal Lane 0 Data Y
6	V25	CSI21_DY3	CSI Signal Lane 3 Data Y
7	---	DGND	Signal Ground
8	---	DGND	Signal Ground
9	T26	CSI21_DX1	CSI Signal Lane 1 Data X
10	W26	CSI21_DX4	CSI Signal Lane 4 Data X
11	T25	CSI21_DY1	CSI Signal Lane 1 Data Y
12	W25	CSI21_DY4	CSI Signal Lane 4 Data Y
13	---	DGND	Signal Ground
14	---	DGND	Signal Ground
15	U26	CSI21_DX2	CSI Signal Lane 2 Data X
16	B17	H_GPIO_40	OMAP GPIO_40
17	U25	CSI21_DY2	CSI Signal Lane 2 Data Y
18	B20	H_GPIO_45	OMAP GPIO_45
19	---	DGND	Signal Ground
20	V27	H_CAM_GLB_RESET	Camera Global Reset or GPIO_83
21	W27	H_I2C3_SCL	I2C3 Serial Clock
22	T27	H_CAM_SHUTTER	Camera Shutter or GPIO_81
23	Y27	H_I2C3_SDA	I2C3 Serial Data
24	U27	H_CAM_STROBE	Camera Strobe or GPIO_82
25	B21	H_GPIO_47	OMAP GPIO_47
26	B19	H_GPIO_44	OMAP GPIO_44
27	AA28	H_FREF_CLK1_OUT	OMAP Camera Clock In
28	B18	H_GPIO_42	OMAP GPIO_42
29	---	VBAT	Battery Voltage In
30	---	VDD_VAUX3	TWL6030 VAUX3 LDO (adjustable from 1.0V to 3.0V)

Table 13: Camera Expansion Connector Pin Definitions (J17)

2.19 JTAG Connector (J8)

The Pandaboard ES provides a 14-pin 0.1" (2.54mm) pitch through-hole connector at J8 as shown in Figure 17 below. In the figure below, pin 1 is the lower left pin and pin 2 is directly above it. Odd number pins are on the bottom side of the connector, and even numbered pins are along the top. Pin 6 is removed to comply with the keying on the JTAG pods.

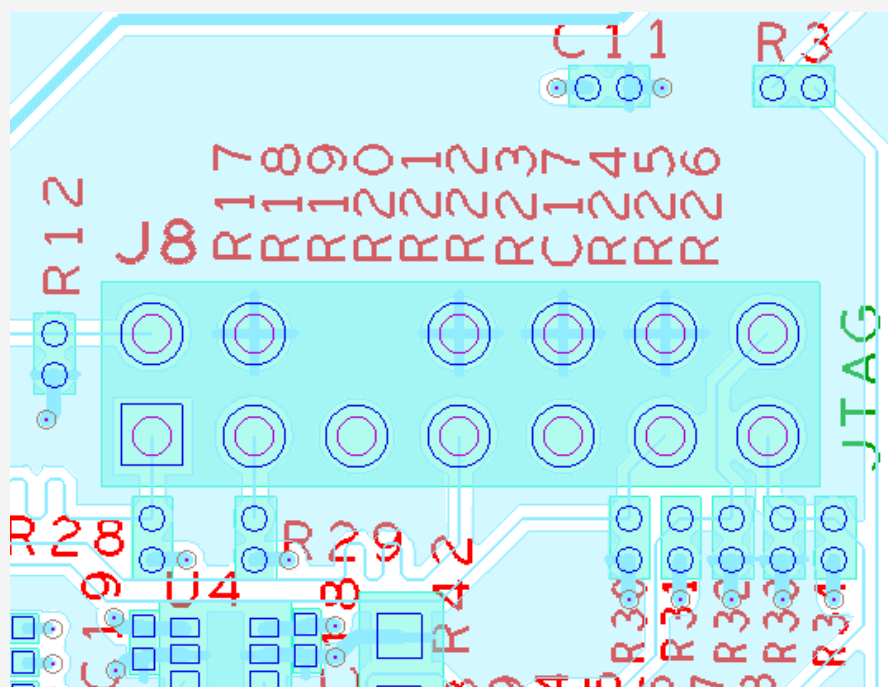


Figure 17 – 14-pin JTAG Connector (J8)

See Table 14 for a description of the pins their connectivity to OMAP4460, and their function on this connector.

J8 Pin #	OMAP Ball #	Signal Name	Signal Description
1	AH1	H_JTAG_TMS	JTAG Test Mode Select
2	AH2	H_JTAG_NTRST	JTAG Test Reset (Active low)
3	AE1	H_JTAG_TDI	JTAG Test Data In
4,8,10,12	----	DGND	Signal Ground
5	---	VIO_1V8	1.8V JTAG Power
6	---	----	N/A
7	AE2	H_JTAG_TDO	JTAG Test Data Out
9	AE3	H_JTAG_RTCK	JTAG Return Clock Out
11	AG1	H_JTAG_TCK	JTAG Clock In
13	M2	H_DPM_EMU0	Emulator I/O 0
14	N2	H_DPM_EMU1	Emulator I/O 1

Table 14: JTAG Connector Pinout (J8)

2.20 LED Indicators

The Pandaboard ES provides three LED indicators. See Figure 18 for the location of these three LEDs on the Panda PCB.

LEDs D1 and D2 are green LEDs. D1 is controlled via OMAP4460 GPIO_110 (ball AD27), while D2 is controlled via OMAP4460 GPIO_WK8 (ball AC3). For both of these LEDs, writing the GPIO high will turn on the LED, while writing it low will turn off the LED.

LED D3 is a red LED that is controlled automatically via onboard circuitry. This LED being illuminated indicates an overvoltage condition on the input DC supply (i.e. a supply of greater than 5V has been plugged into P3). The supervisor IC at U19 on sheet 2 of the schematics monitors the voltage from the DC input jack (through a voltage divider to set the appropriate threshold). If a DC supply of more than 5V is plugged into the Pandaboard ES, the U19 output reset will be negated, which will turn on the red LED at D3 and disable load switch U16 on sheet 2 of the schematic, which will remove 5V power to the remainder of the Pandaboard ES circuitry. This is intended to prevent damage to onboard circuitry.

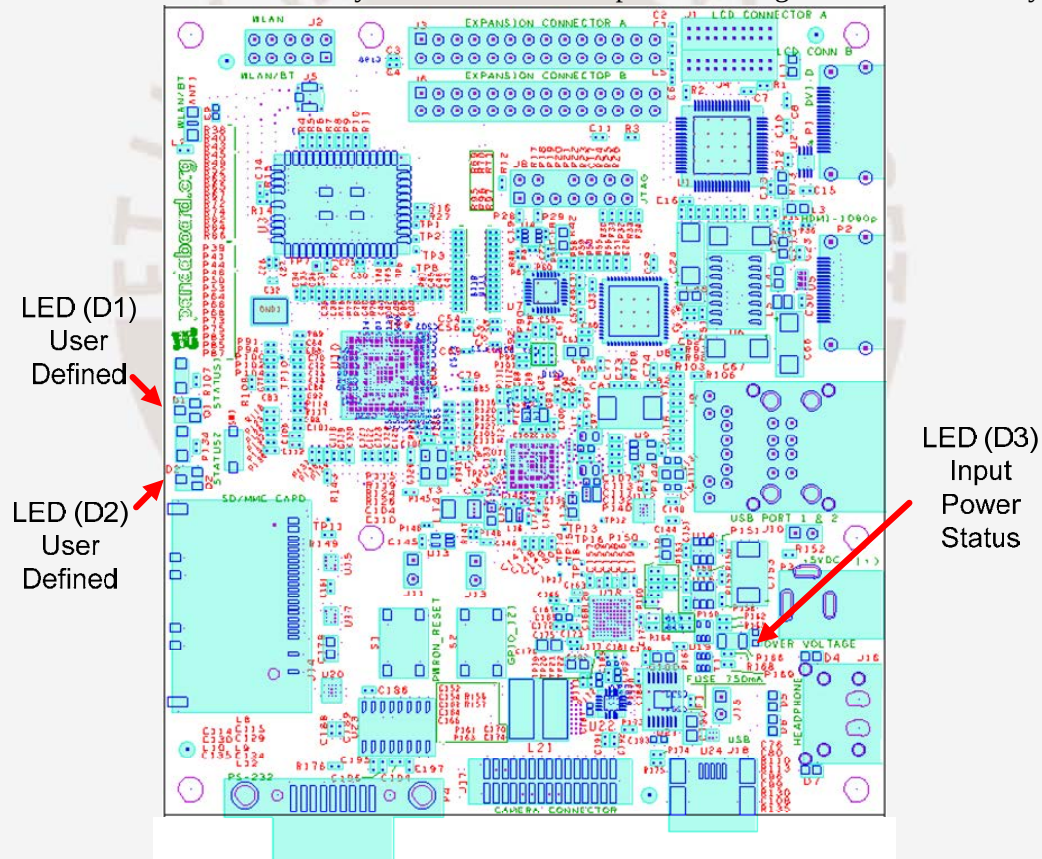


Figure 18 – Pandaboard ES LED Locations

2.21 User Interface Features

Described below are the user features that are incorporated in the OMAP4460 Pandaboard ES.

2.21.1 S1 – Push Button Switch

S1 is a momentary push-button switch that may be depressed to initiate a power-on reset of the Pandaboard ES. The normal power-on output from the TWL6030 is driven through an open-collector driver, and the output of this switch is tied to the output of the output of the open-collector gate.

2.21.2 S2 - Push Button Switch

S2 is a momentary push-button switch whose output is tied to GPIO_113 on the Pandaboard ES. Depressing this switch will momentarily ground GPIO_113. For proper operation of this switch, the internal pull on this signal must be enabled, and it must be set to a pull-up NOT a pull-down.

2.21.3 SW1 – Dip/Slide Switch

SW1 is slide switch that is used to provide the Pandaboard ES user with the desired value on the SYSBOOT3 input into the OMAP4460. Having this switch in the open position will cause SYSBOOT3 to be sampled as a logic '1' at reset, while having it in the closed position will cause SYSBOOT3 to be sampled low at reset.

2.22 I²C Device Mapping

The OMAP4460 Pandaboard ES contains four different I²C busses that are provided by the OMAP4460 (I²C1, I²C2, I²C3, and I²C4). The paragraphs below detail the seven bit I²C addresses for each device on the different I²C busses. The write and read addresses are derived by adding a '0' or '1' respectively, to the LSB of the address given below.

2.22.1 OMAP I²C1

Device	Function	I2C Address
TWL6030	Phoenix Power IC	0x48, 0x49, 0x4A
TWL6040	Phoenix Audio IC	0x4B

Table 15: OMAP I²C1 Device Addresses

2.22.2 OMAP I²C2

<i>Device</i>	<i>Function</i>	<i>I2C Address</i>
Display Expansion Connector (J1/J4)	External LCD Control (e.g. touchscreen)	TBD
DSI Expansion Connector (J7)	DSI Connector Touchscreen I/F Control	TBD

Table 16: OMAP I²C2 Device Addresses

2.22.3 OMAP I²C3

<i>Device</i>	<i>Function</i>	<i>I2C Address</i>
DVI-D connector (P1)	Control of television set connected via P1	TBD
Camera Expansion connector (J17)	Camera Module Control	TBD

Table 17: OMAP I²C3 Device Addresses

2.22.4 OMAP I²C4

<i>Device</i>	<i>Function</i>	<i>I2C Address</i>
Expansion Connectors (J6)	Future expansion	TBD

Table 18: OMAP I²C4 Device Addresses

3 Pandaboard ES S/W Interface

This chapter provides details of interest regarding the SW interface of the Pandaboard ES implementation.

3.1 Readable Board Revision

The OMAP4460 Panda Board provides a readable PCB revision that may be read by Software to determine what board is being used. These board ID bits are shown below for the OMAP4460 and OMAP4430 Pandaboard ESs. BOARD_ID2 and BOARD_ID0 stayed on the same GPIOs (GPIO_171 and GPIO_182, respectively), but BOARD_ID1 changed from GPIO_101 on the 4430 Pandaboard ES to GPIO_48 on the OMAP4460 Pandaboard ES. This was necessary because GPIO_101 was utilized as the tearing effect signal to the new DSI Display Expansion connector at J7. Values are as shown in Table 19 below.

BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
OMAP4460 Pandaboard ES				
GPIO_2	GPIO_3	GPIO_171	GPIO_48	GPIO_182
0	0	0	1	1
OMAP4430 Pandaboard ES				
N/A ¹	N/A ¹	GPIO_171	GPIO_101	GPIO_182
1	1	0	1	1

Table 19: Board ID Read Values

¹ – GPIO_2 and GPIO_3 are unused on the OMAP4430 Pandaboard ES, and if read, will both be read back as '1'

3.2 Pandaboard ES Pin Multiplexing

3.2.1 Panda Base Platform Pin Multiplexing

See Table 20 for a listing of the OMAP pin multiplexing required for the OMAP4460 processor on the Pandaboard ES. This table only includes the GPIOs that are connected and required for operation of the as-shipped configuration of the Pandaboard ES. Unused pins are not included here as well as any GPIOs that go to the onboard connectors. GPIOs that are connected to the Camera Expansion connector at J17 are listed in Table 21 on page 54, while the signals connected to the Generic Expansion connectors at J3 and J6 may be found in Table 22 on page 55.

GPIO	OMAP Ball #	Mux Mode	Signal Name	Description of Pandaboard ES Usage
0	J27	3	H_GPIO_0	DVI-D Transmitter (TFP410) Power Down

GPIO	OMAP Ball #	Mux Mode	Signal Name	Description of Pandaboard ES Usage
1	H27	3	HUB_NPD	Ethernet/USB Hub LDO Power Enable
2	L27	3	GPIO_2	Board ID Bit 4
3	K27	3	GPIO_3	Board ID Bit 3
11	M2	0	DPM_EMU0	JTAG Emulator 0 I/O
12	N2	0	DPM_EMU1	JTAG Emulator 1 I/O
14	V1	5	DISPC2_DATA10	Parallel Display Data Bit 10
15	V2	5	DISPC2_DATA9	Parallel Display Data Bit 9
16	W1	5	DISPC2_DATA16	Parallel Display Data Bit 16
17	W2	5	DISPC2_DATA17	Parallel Display Data Bit 17
18	W3	5	DISPC2_HSYNC	Parallel Display Horizontal Sync
19	W4	5	DISPC2_PCLK	Parallel Display Pixel Clock
20	Y2	5	DISPC2_VSYNC	Parallel Display Vertical Sync
21	Y3	5	DISPC2_DE	Parallel Display Data Enable
22	Y4	5	DISPC2_DATA8	Parallel Display Data Bit 8
23	AA1	5	DISPC2_DATA7	Parallel Display Data Bit 7
24	AA2	5	DISPC2_DATA6	Parallel Display Data Bit 6
25	AA3	5	DISPC2_DATA5	Parallel Display Data Bit 5
26	AA4	5	DISPC2_DATA4	Parallel Display Data Bit 4
27	AB2	5	DISPC2_DATA3	Parallel Display Data Bit 3
28	AB3	5	DISPC2_DATA2	Parallel Display Data Bit 2
41	A18	3	GPIO_41	HDMI Transceiver Level Shifter Output Enable
43	A19	3	GPIO_43	Wireless LAN Enable
46	A21	3	GPIO_46	Bluetooth Enable
48	C20	3	GPIO_48	Board ID Bit 1
49	D20	3	GPIO_49	Bluetooth Wakeup
53	C22	3	GPIO_53	WLAN Interrupt In
60	D22	3	GPIO_60	HDMI DC/DC-Hot Plug Enable
62	B23	3	GPIO_62	Ethernet/USB Hub Reset
63	B9	0	HDMI_HPD	HDMI Hot Plug Detect
64	B10	0	HDMI_CEC	HDMI Consumer Electronic Control
65	A8	0	HDMI_DDC_SCL	Display Data Channel Serial Clock
66	B8	0	HDMI_DDC_SDA	Display Data Channel Serial Data
84	AE18	4	ULPIPHY_CLK	USBB1 ULPI Clock (Hub)
85	AG19	4	ULPIPHY_STP	USBB1 ULPI Stop (Hub)
86	AF19	4	ULPIPHY_DIR	USBB1 ULPI Direction (Hub)
87	AE19	4	ULPIPHY_NXT	USBB1 ULPI Next (Hub)
88	AF18	4	ULPIPHY_DAT0	USBB1 ULPI Data Bit 0 (Hub)
89	AG18	4	ULPIPHY_DAT1	USBB1 ULPI Data Bit 1 (Hub)
90	AE17	4	ULPIPHY_DAT2	USBB1 ULPI Data Bit 2 (Hub)

GPIO	OMAP Ball #	Mux Mode	Signal Name	Description of Pandaboard ES Usage
91	AF17	4	ULPIPHY_DAT3	USBB1 ULPI Data Bit 3 (Hub)
92	AH17	4	ULPIPHY_DAT4	USBB1 ULPI Data Bit 4 (Hub)
93	AE16	4	ULPIPHY_DAT5	USBB1 ULPI Data Bit 5 (Hub)
94	AF16	4	ULPIPHY_DAT6	USBB1 ULPI Data Bit 6 (Hub)
95	AG16	4	ULPIPHY_DAT7	USBB1 ULPI Data Bit 7 (Hub)
100	D2	0	SDMMC1_CLK	SDMMC Card Cage Clock (1.8v/3.0V)
101	E3	0	SDMMC1_CMD	SDMMC Card Cage Command (1.8v/3.0V)
101	A24	3	GPIO_101	Board ID Input Bit 1
102	E4	0	SDMMC1_DAT0	SDMMC Card Cage Data Bit 0 (1.8v/3.0V)
103	E2	0	SDMMC1_DAT1	SDMMC Card Cage Data Bit 1 (1.8v/3.0V)
104	E1	0	SDMMC1_DAT2	SDMMC Card Cage Data Bit 2 (1.8v/3.0V)
105	F4	0	SDMMC1_DAT3	SDMMC Card Cage Data Bit 3 (1.8v/3.0V)
106	F3	0	SDMMC1_DAT4	SDMMC Card Cage Data Bit 4 (1.8v/3.0V)
107	F1	0	SDMMC1_DAT5	SDMMC Card Cage Data Bit 5 (1.8v/3.0V)
108	G4	0	SDMMC1_DAT6	SDMMC Card Cage Data Bit 6 (1.8v/3.0V)
109	G3	0	SDMMC1_DAT7	SDMMC Card Cage Data Bit 7 (1.8v/3.0V)
110	AD27	3	GPIO_110	LED D1 On/Off Control
113	AC28	3	GPIO_113	Input from push-button switch S2
114	AC26	0	MCBSP1_CLKX	BT Audio I2S Clock
115	AC25	0	MCBSP1_DR	BT Audio I2S Data Out
116	AB25	0	MCBSP1_DX	BT Audio I2S Data In
117	AC27	0	MCBSP1_FSX	BT Audio I2S Frame Sync
118	AH26	0	ABE_CLKS	Clock input from TWL6030 Audio Companion IC
121	AG24	5	DMTIMER11_PWM_EVT	Display Expansion Connector(s) PWM Control
122	AH24	3	GPIO_122	DVI-D Monitor Sense Input
123	AB26	0	UART2_CTS	Bluetooth Host Control Interface Request to Send
124	AB27	0	UART2_RTS	Bluetooth Host Control Interface Clear to Send
125	AA25	0	UART2_RX	Bluetooth Host Control Interface Transmit Data
126	AA26	0	UART2_TX	Bluetooth Host Control Interface Receive Data
127	AA27	3	GPIO_127	TWL6040 Audio Power On
128	C26	0	I2C2_SCL	I2C2 Serial Clock
129	D26	0	I2C2_SDA	I2C2 Serial Data
130	W27	0	I2C3_SCL	I2C3 Serial Clock
131	Y27	0	I2C3_SDA	I2C3 Serial Data
132	AG21	0	I2C4_SCL	I2C4 Serial Clock
133	AH22	0	I2C4_SDA	I2C4 Serial Data
141	F27	0	UART3_CTS	Debug Terminal RS-232 Clear to Send
142	F28	0	UART3_RTS	Debug Terminal RS-232 Request to Send
143	G27	0	UART3_RX	Debug Terminal RS-232 Receive Data

GPIO	OMAP Ball #	Mux Mode	Signal Name	Description of Pandaboard ES Usage
144	G28	0	UART3_TX	Debug Terminal RS-232 Transmit Data
145	AE5	0	SDMMC5_CLK	WLAN SDIO Clock Line
146	AF5	0	SDMMC5_CMD	WLAN SDIO Command Line
147	AE4	0	SDMMC5_DAT0	WLAN SDIO Data Bit 0
148	AF4	0	SDMMC5_DAT1	WLAN SDIO Data Bit 1
149	AG3	0	SDMMC5_DAT2	WLAN SDIO Data Bit 2
150	AF3	0	SDMMC5_DAT3	WLAN SDIO Data Bit 3
158	AF12	5	DISPC_DATA23	Parallel Display Data Bit 23
159	AE12	5	DISPC_DATA22	Parallel Display Data Bit 22
160	AG13	5	DISPC_DATA21	Parallel Display Data Bit 21
161	AE11	5	DISPC_DATA20	Parallel Display Data Bit 20
162	AF11	5	DISPC_DATA19	Parallel Display Data Bit 19
163	AG11	5	DISPC_DATA18	Parallel Display Data Bit 18
164	AH11	5	DISPC_DATA15	Parallel Display Data Bit 15
165	AE10	5	DISPC_DATA14	Parallel Display Data Bit 14
166	AF10	5	DISPC_DATA13	Parallel Display Data Bit 13
167	AG10	5	DISPC_DATA12	Parallel Display Data Bit 12
168	AE9	5	DISPC_DATA11	Parallel Display Data Bit 11
171	G26	3	GPIO_171	Board ID Bit 2
179	B5	0	USBA0_OTG_DP	Internal USB Transceiver Data Plus
180	B4	0	USBA0_OTG_DM	Internal USB Transceiver Data Minus
181	AA28	0	FREF_CLK1_OUT	Camera Expansion Connector
182	Y28	0	GPIO_182	Board ID Bit 0
183	AF6	0	SYS_NIRQ2	System Interrupt from TWL6040 Audio IC
184	F26	0	SYS_BOOT0	SYSBOOT Input 0
185	E27	0	SYS_BOOT1	SYSBOOT Input 1
186	E26	0	SYS_BOOT2	SYSBOOT Input 2
187	E25	0	SYS_BOOT3	SYSBOOT Input 3
188	D28	0	SYS_BOOT4	SYSBOOT Input 4
189	D27	0	SYS_BOOT5	SYSBOOT Input 5
190	AB4	5	DISPC2_DATA1	Parallel Display Data Bit 1
191	AC4	5	DISPC2_DATA0	Parallel Display Data Bit 0
WK5	AG8	0	FREF_SLICER_IN	38.4MHz Clock Input
WK6	AD2	2	GPIO_WK6	MSECURE output to TWL6030 (RTC related)
WK7	AC2	3	GPIO_WK7	TPS62361 VSEL0 control
WK8	AC3	3	GPIO_WK8	LED D2 On/Off Control
WK9	AF8	0	SYS_BOOT6	SYSBOOT Input 6
WK10	AE8	0	SYS_BOOT7	SYSBOOT Input 7
WK31	AD4	0	FREF_CLK3_OUT	USBB1 Phy Reference Clock (19.2 MHz)

Table 20: Pandaboard ES OMAP4460 Pin Multiplexing

3.2.2 Camera Expansion Connector Pin Multiplexing

See Table 21 for a description of the pin multiplexing possibilities for the camera expansion board signals.

GPIO	OMAP Ball #	Mux Mode	Signal Name	Description of Pandaboard ES Usage
40	B17	3	GPIO_40	Camera Expansion Connector (pin 16)
42	B18	3	GPIO_42	Camera Expansion Connector (pin 28)
44	B19	3	GPIO_44	Camera Expansion Connector (pin 26)
45	B20	3	GPIO_45	Camera Expansion Connector (pin 18)
47	B21	3	GPIO_47	Camera Expansion Connector (pin 25)
67	R26	0	CSI21_DX0	Camera Expansion Connector (pin 3)
68	R25	0	CSI21_DY0	Camera Expansion Connector (pin 5)
69	T26	0	CSI21_DX1	Camera Expansion Connector (pin 9)
70	T25	0	CSI21_DY1	Camera Expansion Connector (pin 11)
71	U26	0	CSI21_DX2	Camera Expansion Connector (pin 15)
72	U25	0	CSI21_DY2	Camera Expansion Connector (pin 17)
73	V26	0	CSI21_DX3	Camera Expansion Connector (pin 4)
74	V25	0	CSI21_DY3	Camera Expansion Connector (pin 6)
75	W26	0	CSI21_DX4	Camera Expansion Connector (pin 10)
76	W25	0	CSI21_DY4	Camera Expansion Connector (pin 12)
81	T27	0/3	CAM_SHUTTER	Camera shutter or GPIO_81 (pin 22)
82	U27	0/3	CAM_STROBE	Camera strobe or GPIO_82 (pin 24)
83	V27	0	CAM_GLOBALRESET	Camera Expansion Connector (pin 20)
130	W27	0	I2C3_SCL	I2C3 Serial Clock (pin 21)
131	Y27	0	I2C3_SDA	I2C3 Serial Data (pin 23)
181	AA28	0	FREF_CLK1_OUT	Camera Expansion Connector (pin 27)

Table 21: Camera Expansion Connector (J17) Pin Multiplexing Options

3.2.3 Expansion Connector (J3 & J6) Pin Multiplexing

See Table 22 below for a listing of the IOs connected to the expansion connectors at J3 and J6. GPIOs with multiple mux modes listed have multiple functions that can be supported, depending on the requirements of the particular expansion board being utilized.

GPIO	OMAP Ball #	Mux Mode	Function1	Function2	Function3	Function4
32	C16	0/1/3/5	GPMC_AD8	KPD_ROW0	GPIO_32	SDMMC1_DAT0
33	D16	0/1/3/5	GPMC_AD9	KPD_ROW1	GPIO_33	SDMMC1_DAT1
34	C17	0/1/3/5	GPMC_AD10	KPD_ROW2	GPIO_34	SDMMC1_DAT2
35	D17	0/1/3/5	GPMC_AD11	KPD_ROW3	GPIO_35	SDMMC1_DAT3
36	C18	0/1/3/5	GPMC_AD12	KPD_COL0	GPIO_36	SDMMC1_DAT4
37	D18	0/1/3/5	GPMC_AD13	KPD_COL1	GPIO_37	SDMMC1_DAT5
38	C19	0/1/3/5	GPMC_AD14	KPD_COL2	GPIO_38	SDMMC1_DAT6
39	D19	0/1/3/5	GPMC_AD15	KPD_COL3	GPIO_39	SDMMC1_DAT7
50	B25	0/3	GPMC_NCS0	GPIO_50	----	----
51	C21	0/3	GPMC_NCS1	GPIO_51	----	----
54	C25	0/3/4	GPMC_NWP	GPIO_54	SYS_NDMAREQ1	----
55	B22	0/3/4/5	GPMC_CLK	GPIO_55	SYS_NDMAREQ2	SDMMC1_CMD
56	D25	0/3/4/5	GPMC_NADV_ALE	GPIO_56	SYS_NDMAREQ3	SDMMC1_CLK
59	C23	0/3	GPMC_NBE0_CLE	GPIO_59	----	----
61	B26	0/3	GPMC_WAIT0	GPIO_61	----	----
132	AG21	0/3	I2C4_SCL	GPIO_132	----	----
133	AH22	0/3	I2C4_SDA	GPIO_133	----	----
134	AF22	0/3	MCSP11_CLK	GPIO_134	----	----
135	AE22	0/3	MCSP11_SOMI	GPIO_135	----	----
136	AG22	0/3	MCSP11_SIMO	GPIO_136	----	----
137	AE23	0/3	MCSP11_CS0	GPIO_137	----	----
138	AF23	0/3	MCSP11_CS1	GPIO_138	----	----
139	AG23	0/2/3	MCSP11_CS2	SLIMBUS2_CLOCK	GPIO_139	----
140	AH23	0/2/3	MCSP11_CS3	SLIMBUS2_DATA	GPIO_140	----
155	AG20	0/2/3	UART4_RX	KPD_ROW8	GPIO_155	----
156	AH19	0/2/3	UART4_TX	KPD_COL8	GPIO_156	----
None	C12	0/1	GPMC_AD0	SDMMC2_DAT0	----	----
None	D12	0/1	GPMC_AD1	SDMMC2_DAT1	----	----
None	C13	0/1	GPMC_AD2	SDMMC2_DAT2	----	----
None	D13	0/1	GPMC_AD3	SDMMC2_DAT3	----	----
None	C15	0/1	GPMC_AD4	SDMMC2_DAT4	----	----
None	D15	0/1	GPMC_AD5	SDMMC2_DAT5	----	----
None	A16	0/1	GPMC_AD6	SDMMC2_DAT6	----	----
None	B16	0/1	GPMC_AD7	SDMMC2_DAT0	----	----
None	B11	0/1	GPMC_NOE	SDMMC2_CLK	----	----
None	B12	0/1	GPMC_NWE	SDMMC2_CMD	----	----

Table 22: Expansion Connector (J3 & J6) Pin Multiplexing Options

3.3 OMAP4460 Pandaboard ES Key Components

See Table 23 for a listing of the manufacturers and manufacturer part numbers for some of the key components used on the OMAP4460 Pandaboard ES.

Device / Interface	Under NDA?	Manufacture P/N
Application Processor		
Processor	Yes	TI OMAP4460
Memories/Storage		
DDR	Yes	Elpida 8Gb (POP, S4B) EDB8064B1PB-8D-F
Removable card support	No	KingConn 6-in-One SD/MMC (8 bit Cardcage) SDMM-B0-0016
Removable card ESD protection	No	Texas Instruments TPD6E001RSER
Power		
Power Management (U12)	Yes	Texas Instruments TWL6030
DC Input Connector (P3)	No	CUI, Inc. PJ-002A
USB Power Switch/LDO (U21)	No	Texas Instruments TPS2141PWP
Input Power SMPS (U22)	No	Texas Instruments TPS54320RHL
Input Voltage Supervisor (U19)	No	Texas Instruments TPS3803G15DCKR
USB/Ethernet Hub Power (U9)	No	Texas Instruments TPS73633DBVR
Clocking		
38.4 MHz oscillator	No	TXC 7X-38.400MBB-T
Video/Display		
HDMI Transceiver + ESD protection	No	Texas Instruments TPD12S015AYFFR
HDMI Connector & DVI-D Connector	No	FCI Connectors 10029449-001RLF

DVI-D Transmitter	No	Texas Instruments TFP410PAP
Audio		
Audio Management	Yes	TI TWL6040
Dual Stacked Audio Jack	No	Kycon STX-4235-3/3-N
MCS		
Wilink™6 Module	No	LS Research, Inc. LS240-WI-01-A20
USB/Ethernet		
Ethernet + 2x USB Host Port Connector	No	Tyco (6620004-1) Belfuse (08C2-1X1T-03)
ULPI USB Phy	No	SMSC USB3320C-EZK
USB/Ethernet Hub Controller	No	SMSC LAN9514-JZX
USB OTG ESD Protection	No	Texas Instruments TPD4S012DRYR
Camera Expansion		
30-pin Camera Expansion Connector	No	Samtec TFM-115-32-S-D-A
Display Expansion		
DSI Display Expansion (40 pin SMT, 0.8mm pitch)	No	Hirose FX6A-40P-0.8SV91
Parallel Display Expansion (2x 20 pin TH, 0.050" pitch)	No	Samtec SFMC-110-T1-F-D
Generic Expansion		
Generic Expansion (2x 28 pin TH, 0.050" pitch)	No	Major League Electronics LSWSS-114-D-02-T-LF

Table 23: OMAP4460 Pandaboard ES Key H/W Components

3.4 OMAP4460 Pandaboard ES Key Component Datasheet URLs

Shown below for convenience are links to datasheets for key Pandaboard ES components.

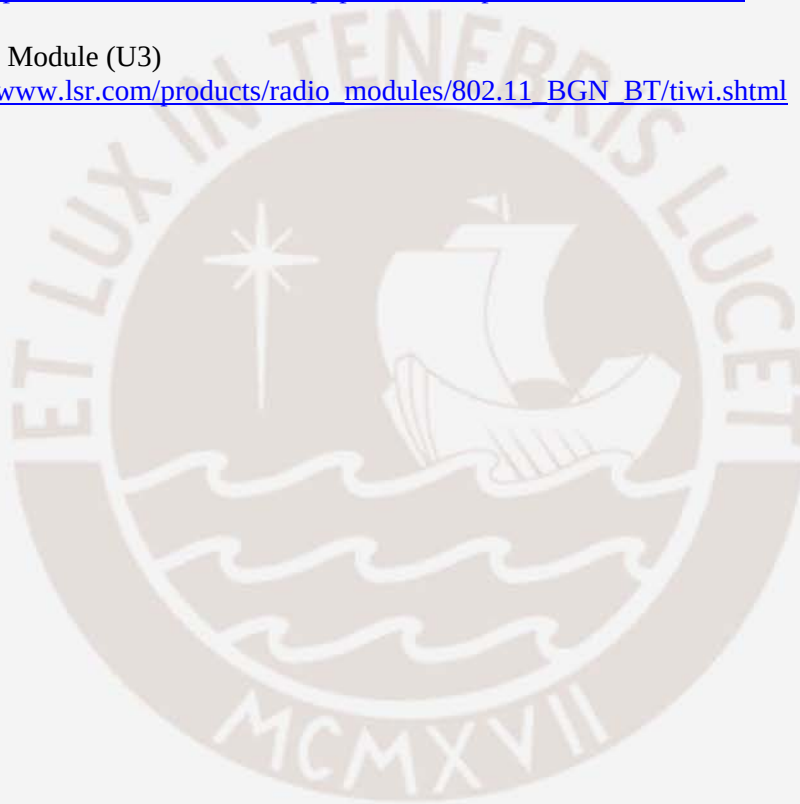
3.4.1 Connector Datasheets

- Combo Ethernet/2x USB Host Port Connector (J9)
 - <http://www.tycoelectronics.com/catalog/products/en?q=6620004-1>
- Power Input Connector (P3)
 - <http://products.cui.com/adtemplate.asp?brand=electronic-components&invky=7106&catky=619701&subcatky1=447353&subcatky2=632366&subcatky3=405514>
- Dual Audio Jack (J16)
 - http://domino2.kycon.com/catalog_PDF/STX4235.pdf
- DVI-D & HDMI Connectors (P1 & P2)
 - http://portal.fciconnect.com/portal/page/portal/FcicntPublic/Product_Type?appname=catLanding
- Camera Expansion Connector (J17)
 - http://www.samtec.com/documents/webfiles/pdf/TFM_SM.PDF
- DSI Display Expansion Connector (J7)
 - <http://www.hirose-connectors.com/connectors/H205SeriesGaiyou.aspx?c1=FX6&c3=3>

3.4.2 Key Electronic Component Datasheets

- DVI Transmitter (U1)
 - <http://focus.ti.com/docs/prod/folders/print/tfp410.html>
- HDMI Companion Chip – ESD, Level Translator, Charge Pump (U5)
 - <http://www.ti.com/product/tpd12s015a>
- USB Power Switch w/ Integrated LDO (U21)
 - <http://focus.ti.com/docs/prod/folders/print/tps2141.html>
- Switching Power Supply, 3A (U22)
 - <http://www.ti.com/product/tps54320>

- Single Output LDO, 400mA (U9)
 - <http://www.ti.com/product/tps73633>
- Single Voltage Detector, (U19)
 - <http://www.ti.com/product/tps3803g15>
- USB ULPI Phy (U7)
 - <http://www.smsc.com/index.php?tid=143&pid=211>
- USB/Ethernet Hub Controller (U9)
 - <http://www.smsc.com/index.php?tid=300&pid=135&cid=&tab=5>
- Wilink™6 Module (U3)
http://www.lsr.com/products/radio_modules/802.11_BGN_BT/tiwi.shtml



4 Test/Debug Information

This chapter contains information to allow easier debug access to signals on the OMAP4460 Pandaboard ES.

4.1 Pandaboard ES Clock Signal Access

The following sections show where various clock signals on the Pandaboard ES may be accessed.

4.1.1 H_FREF_ALTCLK_IN_OMAP Probe Point

This signal is the input clock to OMAP and the TWL6040 Audio Companion IC from the onboard 38.4 MHz oscillator. It may be probed at TP9 in the area above OMAP as shown in Figure 19 below.

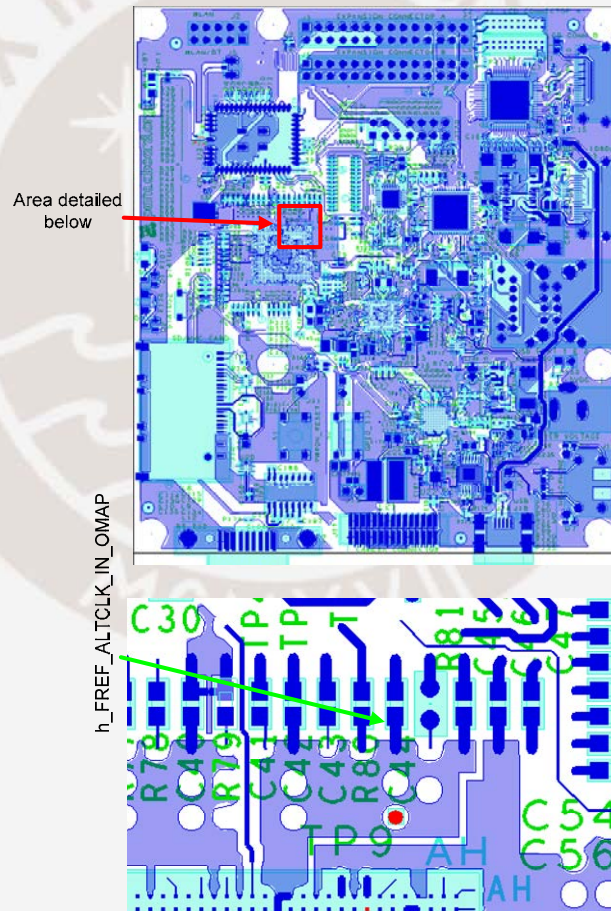
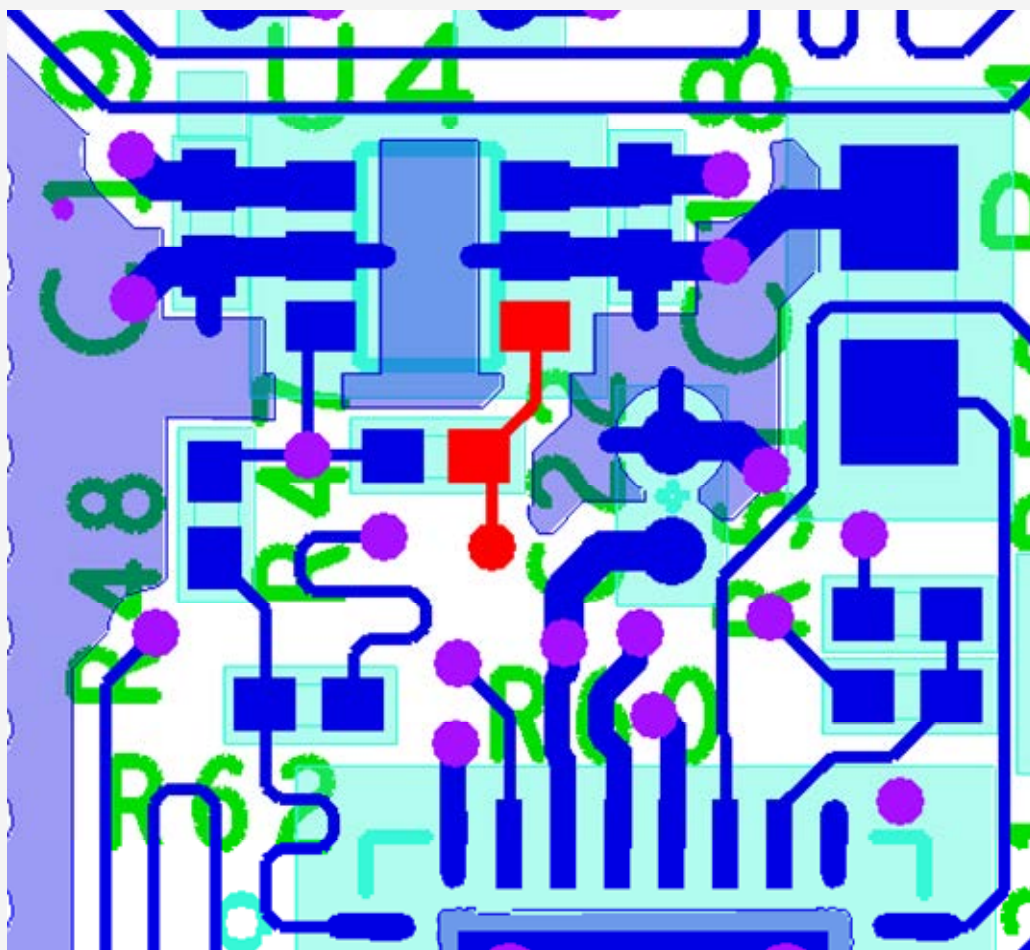


Figure 19 – 38.4 MHz Input Clock Probe Point (h_FREF_ALTCLK_IN_OMAP)**4.1.2 USBB1_PHY_REFCLK Probe Point**

The 19.2 MHz reference input clock to the USBB1 Phy device may be probed at R47-1 or U4-4 as shown below in red. These parts are located directly below the 14-pin JTAG connector J8.

**Figure 20 – USB Phy Ref Clock In Probe Point (USBB1_PHY_REFCLK)**

4.1.3 CLK32K_AUD Probe Point

The 32.768KHz input clock to the TWL6040 Audio Companion IC may be probed at TP14 as shown in Figure 21. This testpoint may be located between the TWL6040 device at U19 and the TWL6030 Power Companion device at U12.

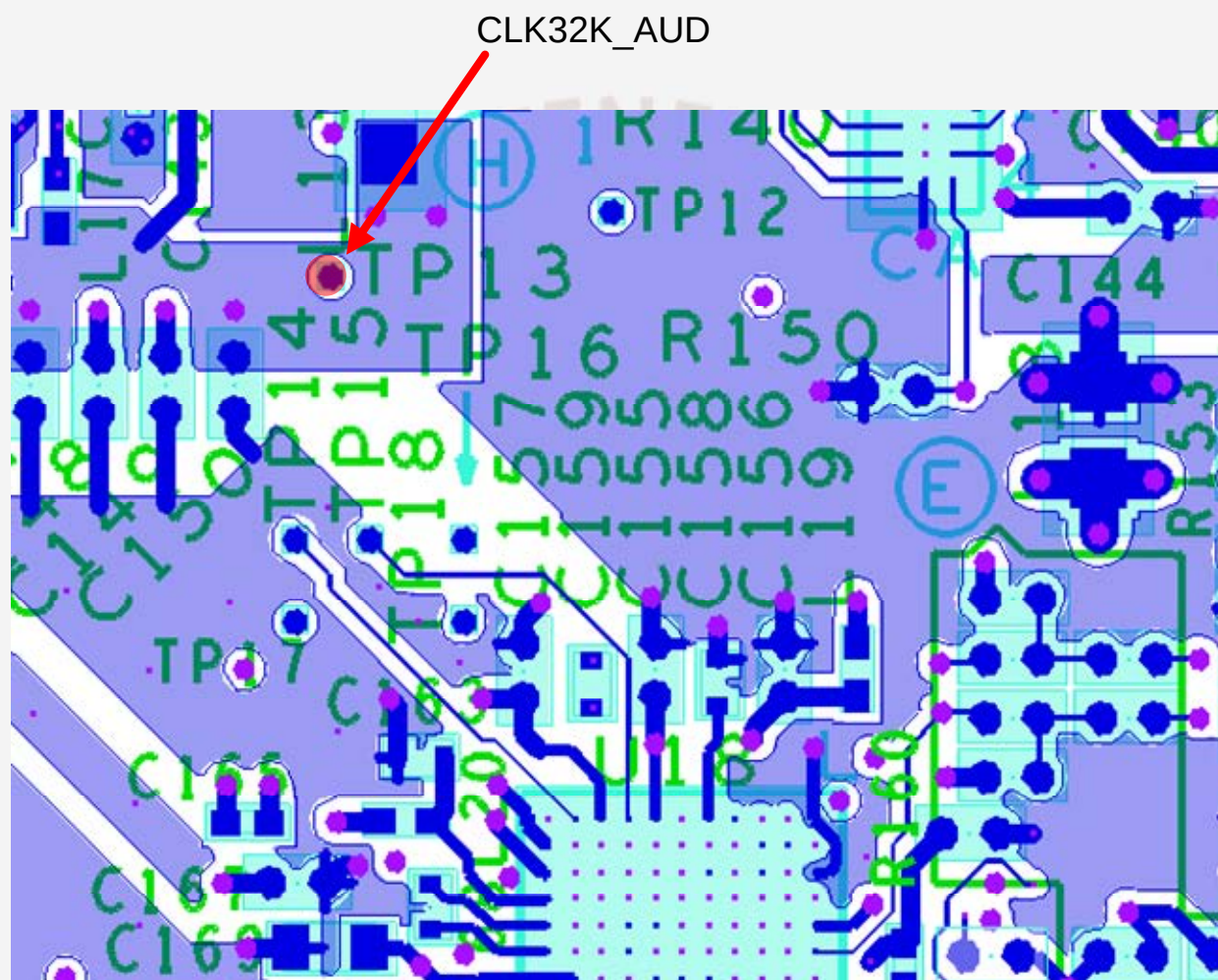


Figure 21 – 32KHz Audio Clock Probe Point (CLK32K_AUD)

4.2 Pandaboard ES Power Rail Signal Access

4.2.1 TWL6030 SMPS Output Probe Points

The outputs of the seven Phoenix SMPS output supplies may be probed around the TWL6030 IC at U11 as shown in Figure 22 below.

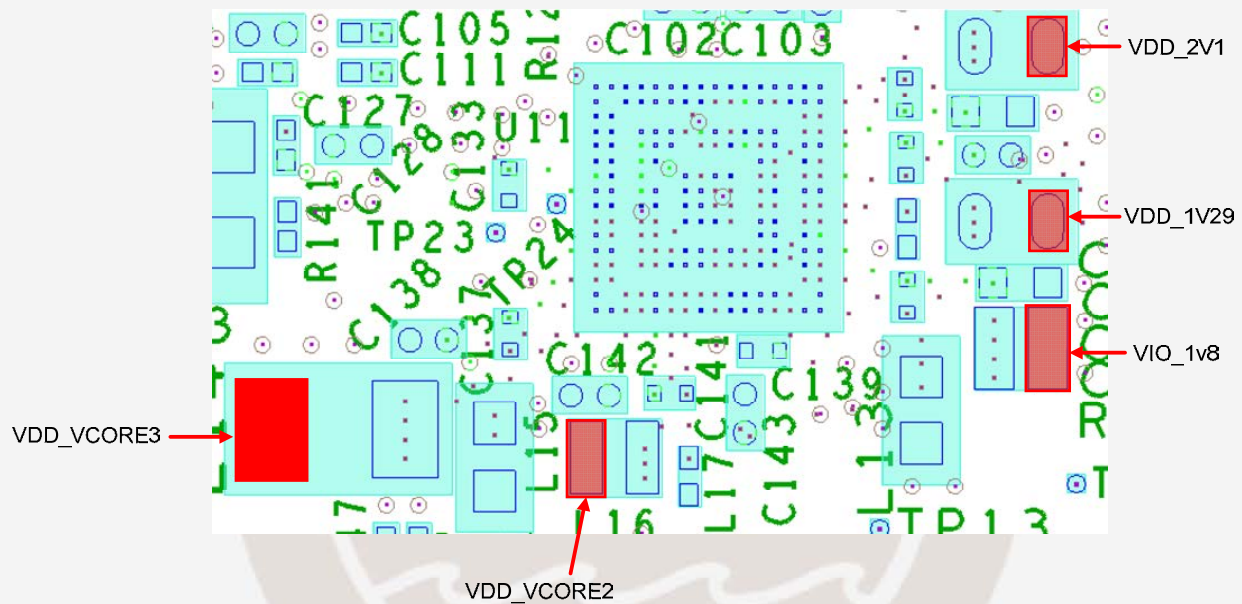


Figure 22 – TWL6030 SMPS Output Probe Points

4.2.2 VDD_CORE1 Output Probe Point

The output of the TPS62361 external supply used to power the VDD_MPU inputs of the OMAP4460 may be probed on the back side of the PCB at L23-1 as shown in Figure 23 below.



Figure 23 – VDD_CORE1 Output Probe Point

4.2.3 VCXIO LDO Output Probe Point

The outputs of the TWL6030 VCXIO LDO may be probed around the bottom of the OMAP4460 and near the oscillator Y3 as shown in Figure 24 below. The possible probe points are at C123-2, C125-2, R145-1, C109-2, C86-2, C127-2, or C105-2 as shown highlighted in red from left to right in Figure 24.

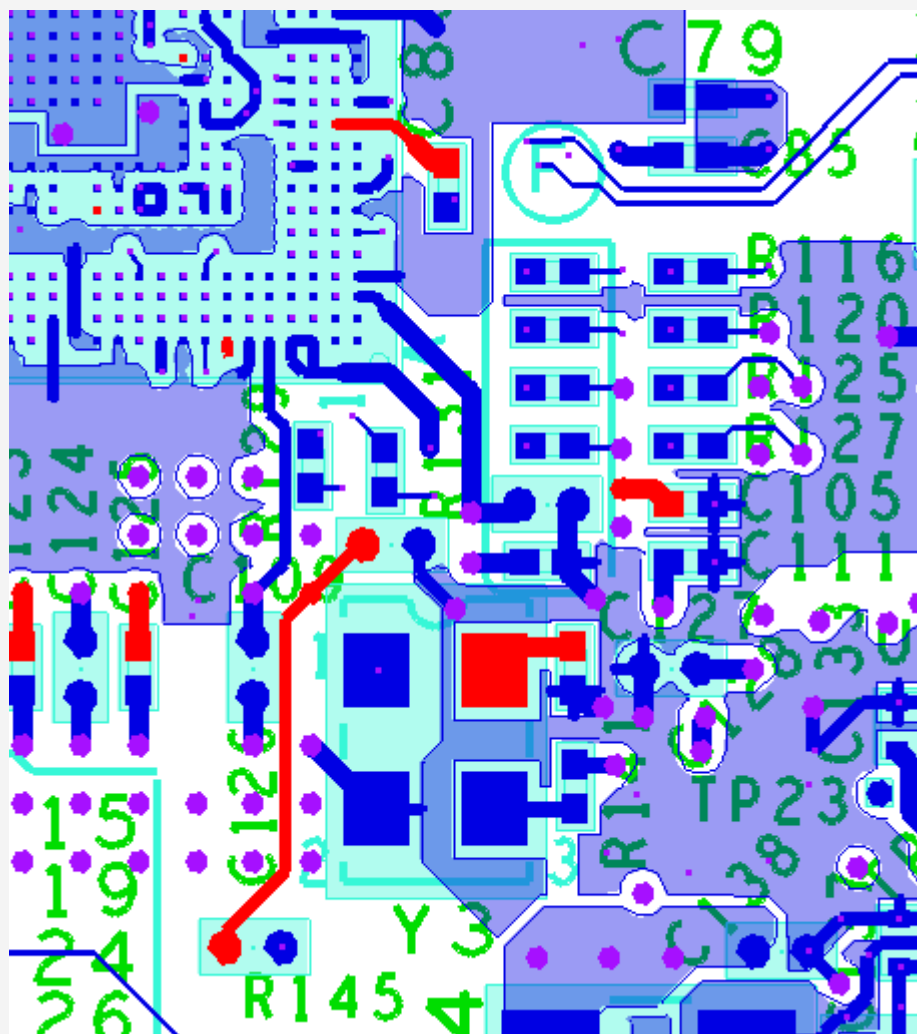


Figure 24 – TWL6030 VCXIO LDO Output Probe Points

4.3 Pandaboard ES Interface Signal Access

4.3.1 TWL6040 PDM Interface Probe Points

The PDM interface which is the digital audio interface between the OMAP4460 and the TWL6040 Audio Companion IC, may be probed at testpoints above the TWL6040 IC at U18 as shown in Figure 25 below.

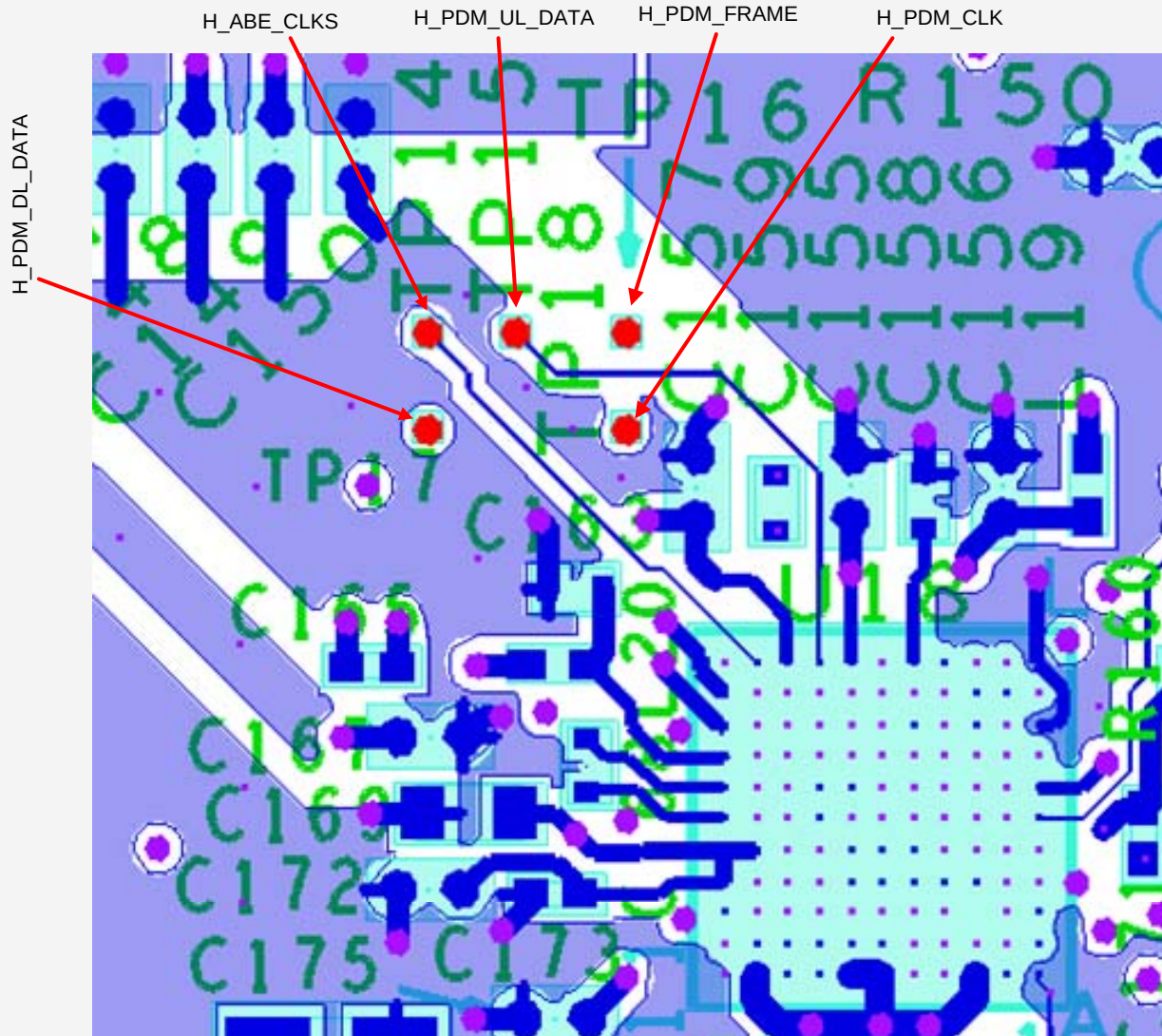


Figure 25 – TWL6040 PDM Interface Probe Points

4.4 Pandaboard ES Schematic

The following pages contain the PDF schematics for the production Pandaboard ES. The schematics are included in this document for convenience, and this manual will be periodically updated, but for the latest information be sure and check on the Pandaboard.org website. OrCAD 16.3 source files are provided for the Pandaboard ES at the following URL:

<http://Pandaboard.org/content/resources/references>

*These design materials are ***NOT SUPPORTED*** and **DO NOT** constitute a reference design. Only “community” support is allowed via resources at <http://Pandaboard.org/content/community/home>. THERE IS NO WARRANTY FOR THE DESIGN MATERIALS, TO THE EXTENT PERMITTED BY APPLICABLE LAW. EXCEPT WHEN OTHERWISE STATED IN WRITING THE COPYRIGHT HOLDERS AND/OR OTHER PARTIES PROVIDE THE DESIGN MATERIALS “AS IS” WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. THE ENTIRE RISK AS TO THE QUALITY AND PERFORMANCE OF THE DESIGN MATERIALS IS WITH YOU. SHOULD THE DESIGN MATERIALS PROVE DEFECTIVE, YOU ASSUME THE COST OF ALL NECESSARY SERVICING, REPAIR OR CORRECTION.*

We mean it; these design materials may be totally unsuitable for any purposes.

Rev	Date	Notes
A	8/29/2011	Created from 750-2170-001 rev. D schematic (input power and antenna matching component changes). Added resistor on VBAT to allow overall current measurement.

Table of Contents

Pg# – Schematic Page Name

1 – Title Page

2 – Input Power

3 – Phoenix Power Component

4 – Phoenix Audio Component

5 – OMAP4460 Symbol A

6 – OMAP4460 Symbol B

7 – OMAP4460 Symbol C

8 – OMAP4460 Debug Interface

9 – SDMMC Card Interface + USB Phy (Hub)

10 – DVI & HDMI Connector

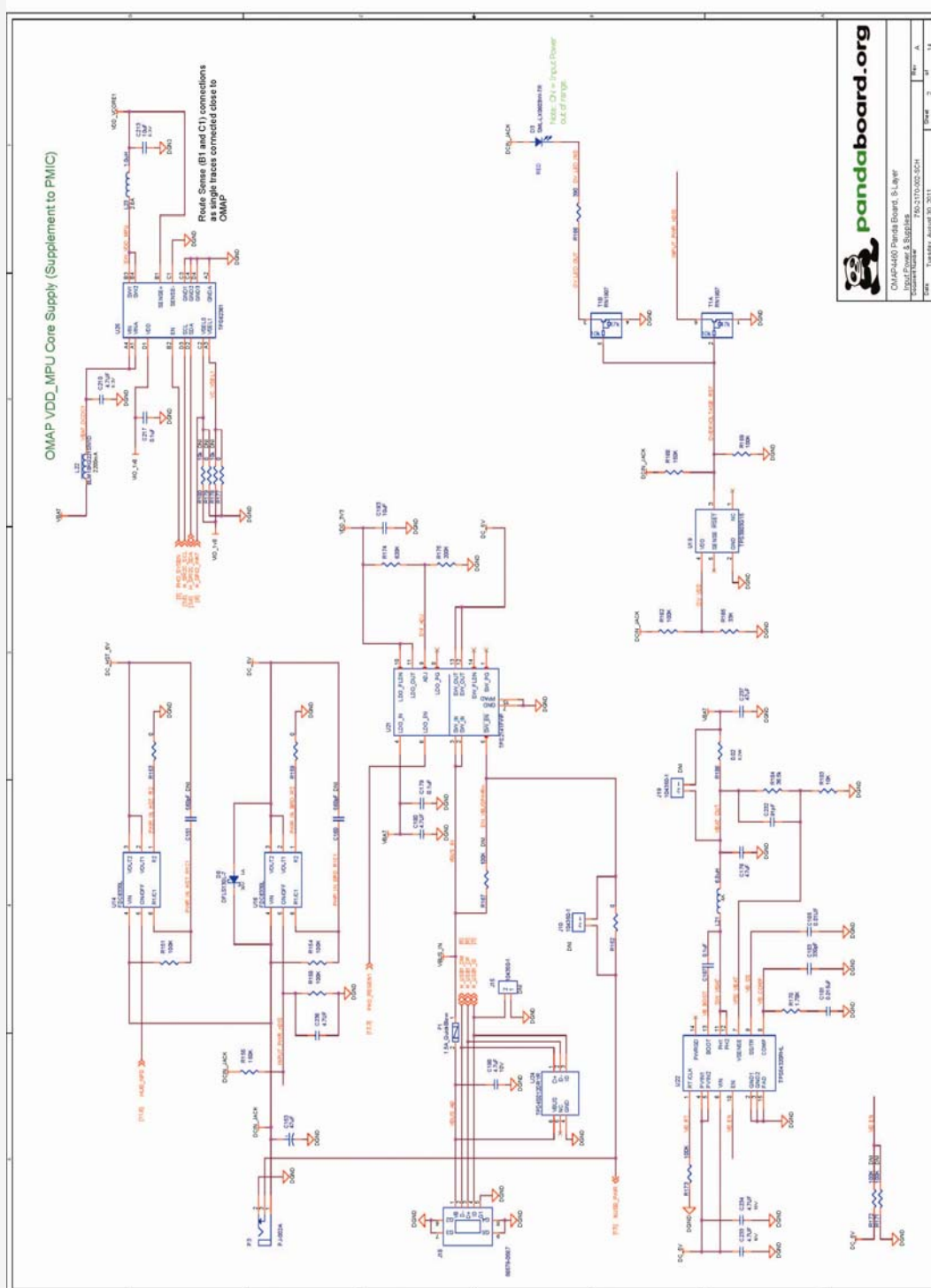
11 – Debug Ethernet

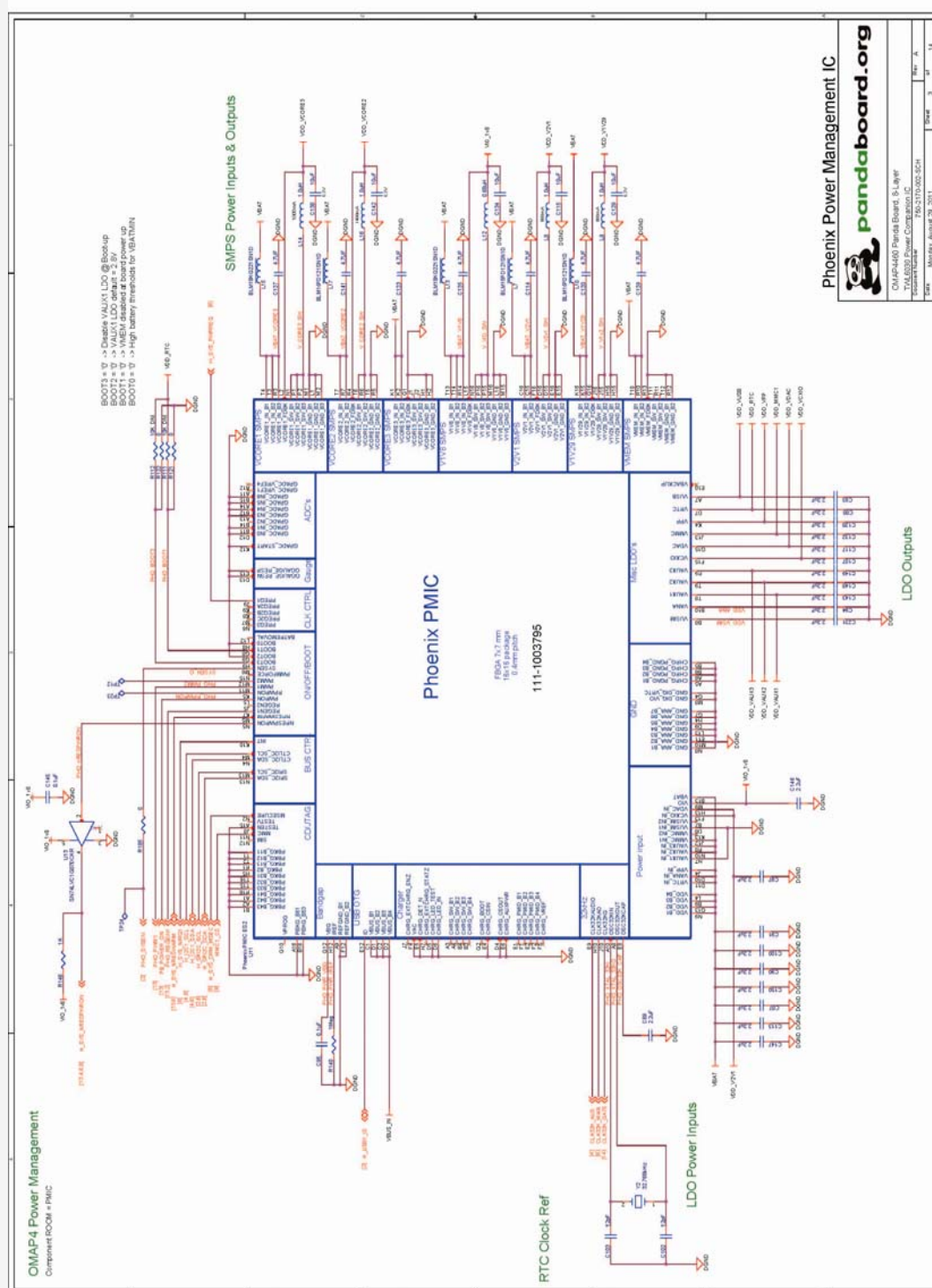
12 – Audio Jack/RS-232 Connection

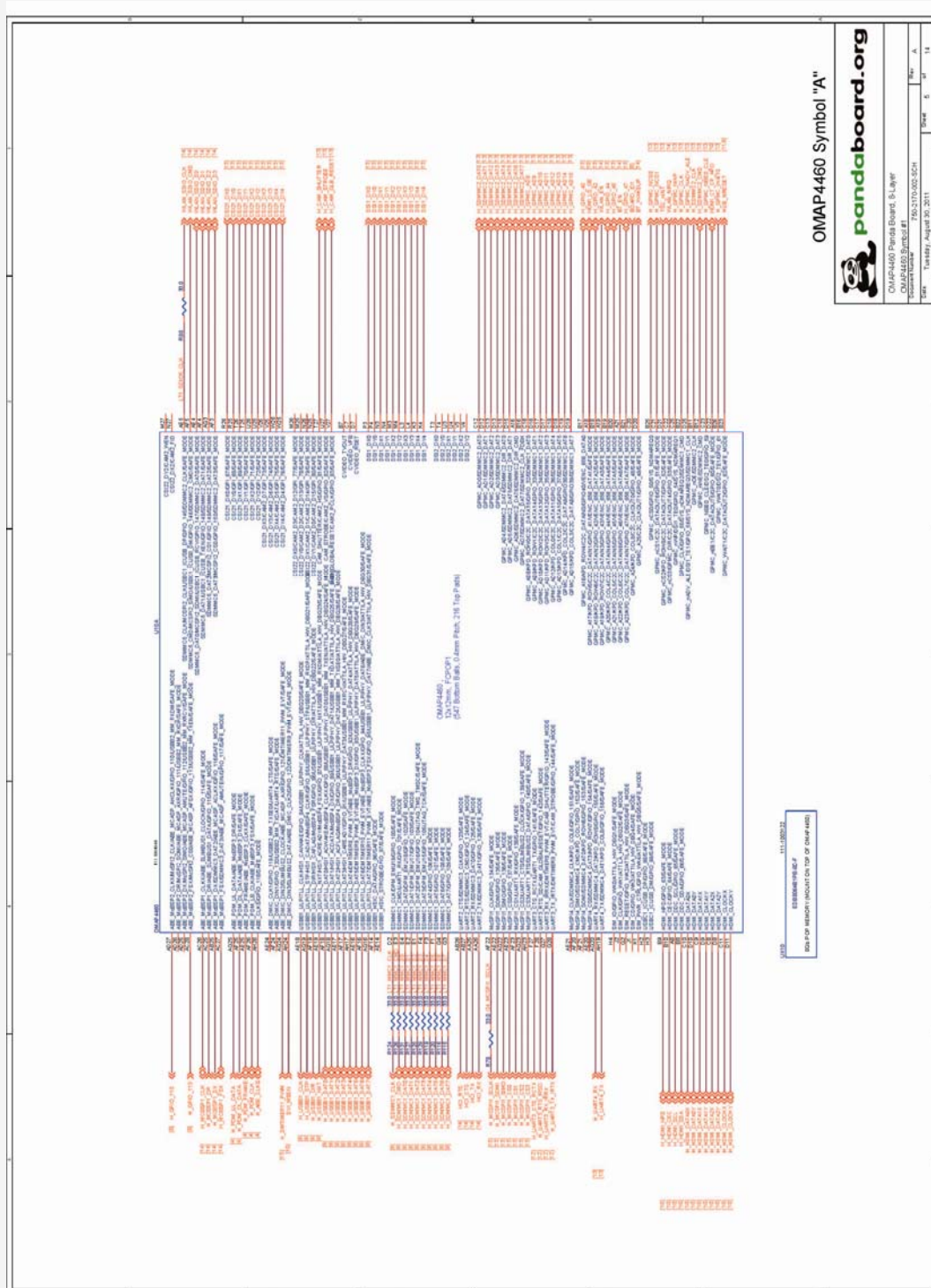
13 – Expansion Connectors

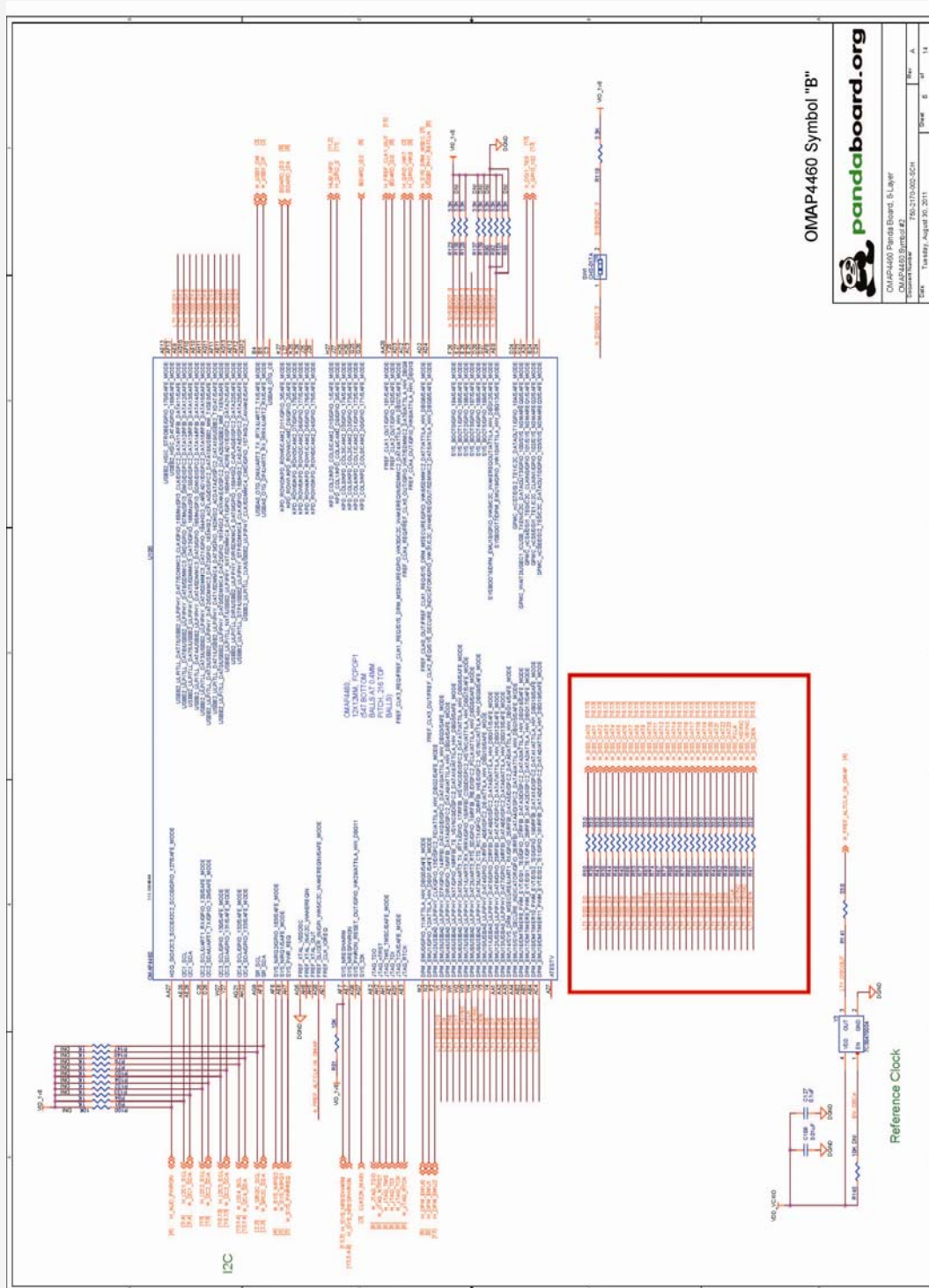
14 – WLAN Subsystem

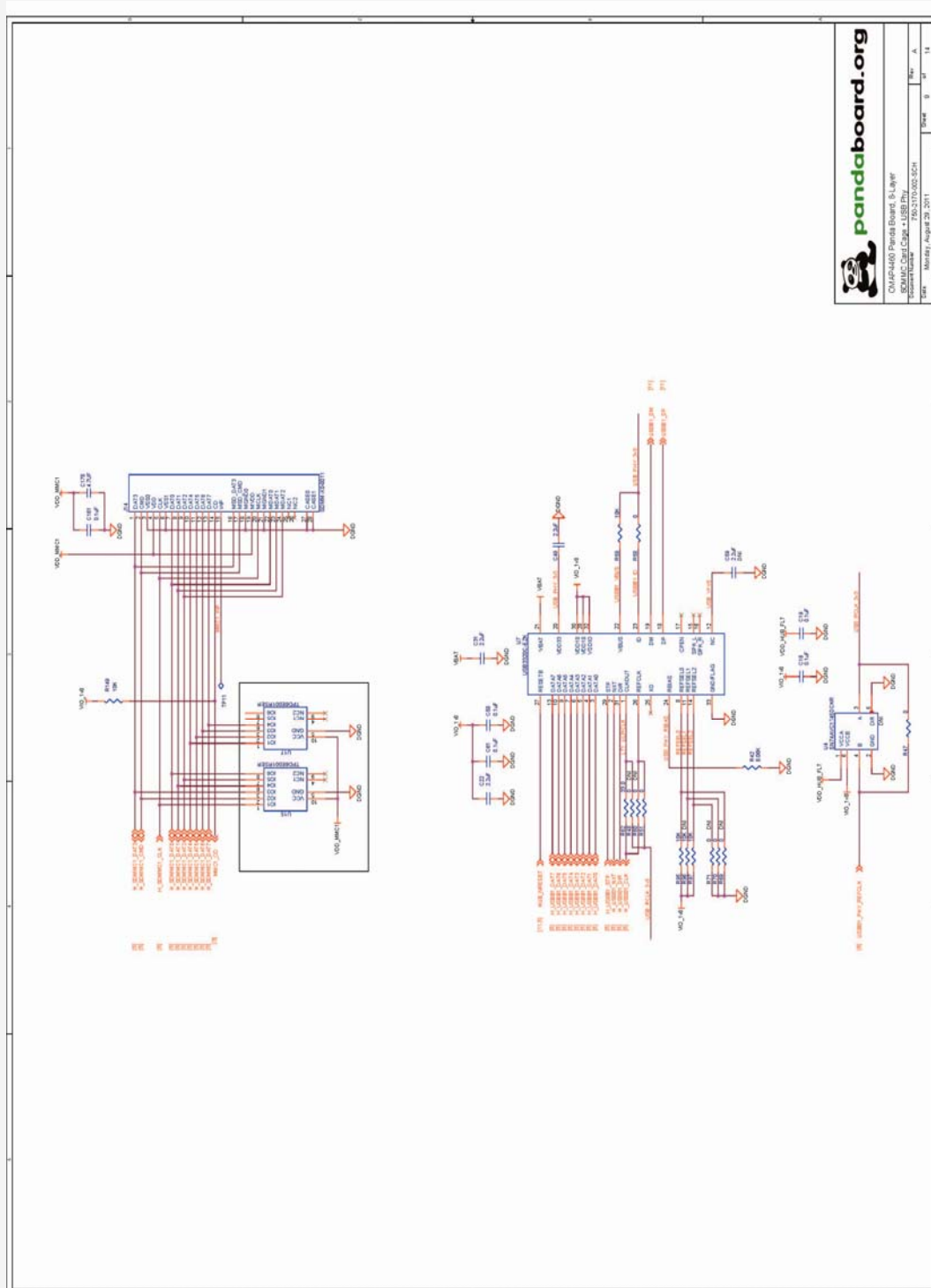
**pandaboard.org**
OMAP4460 Pandaboard ES Layer
750-2170-001 Rev. D
Created from 750-2170-001 Rev. D
Date: September 29, 2011
Page: 1 of 14

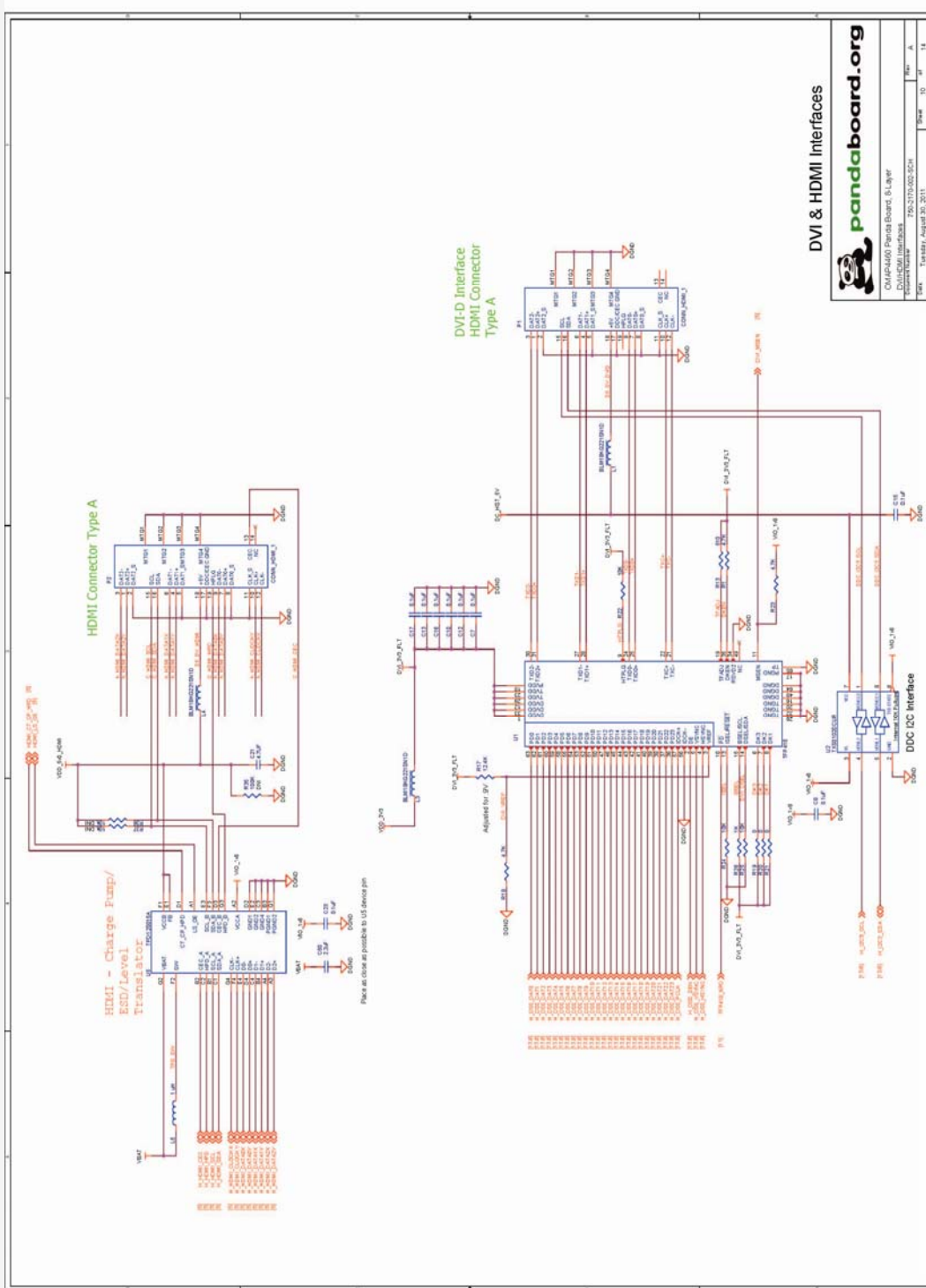


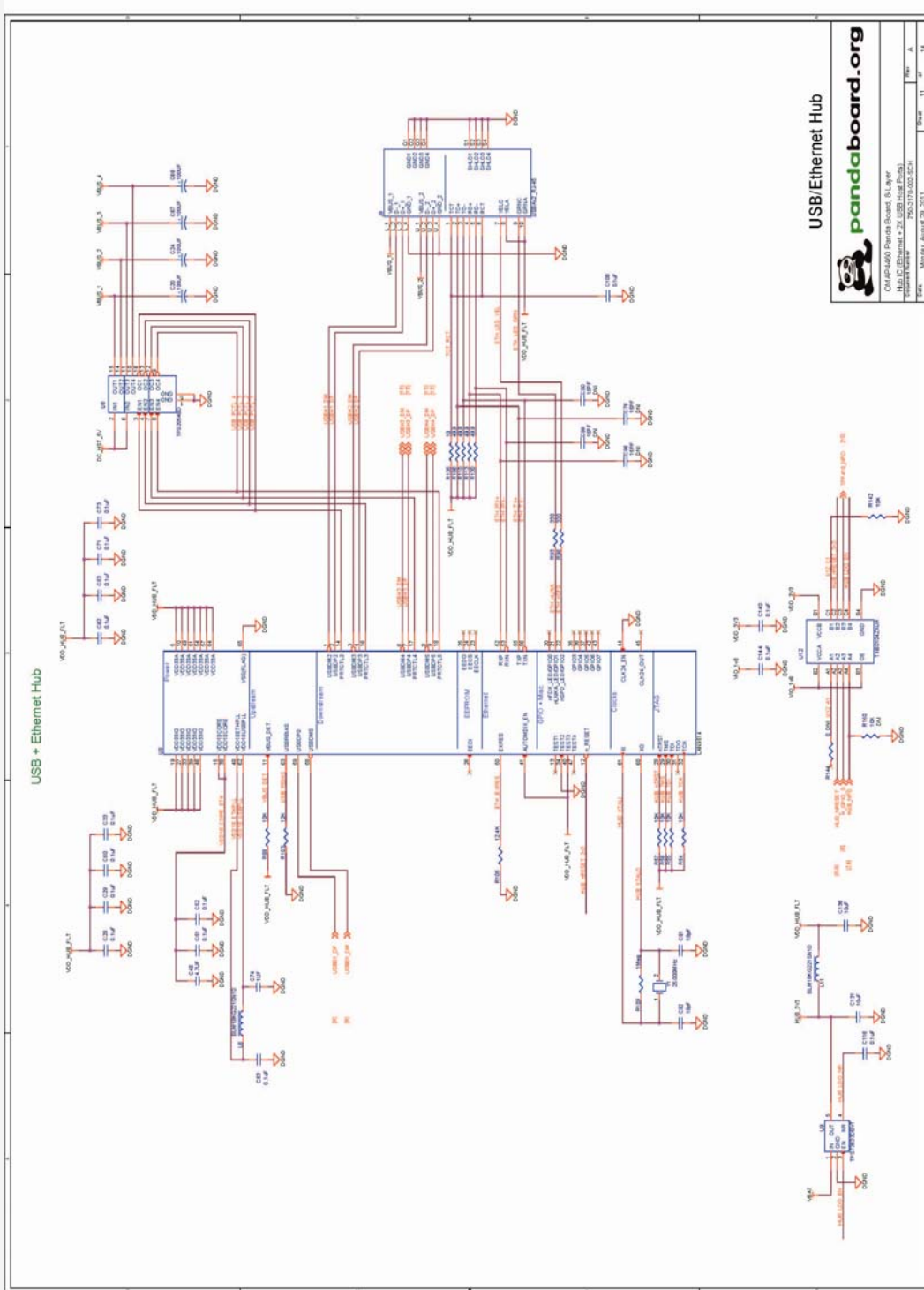


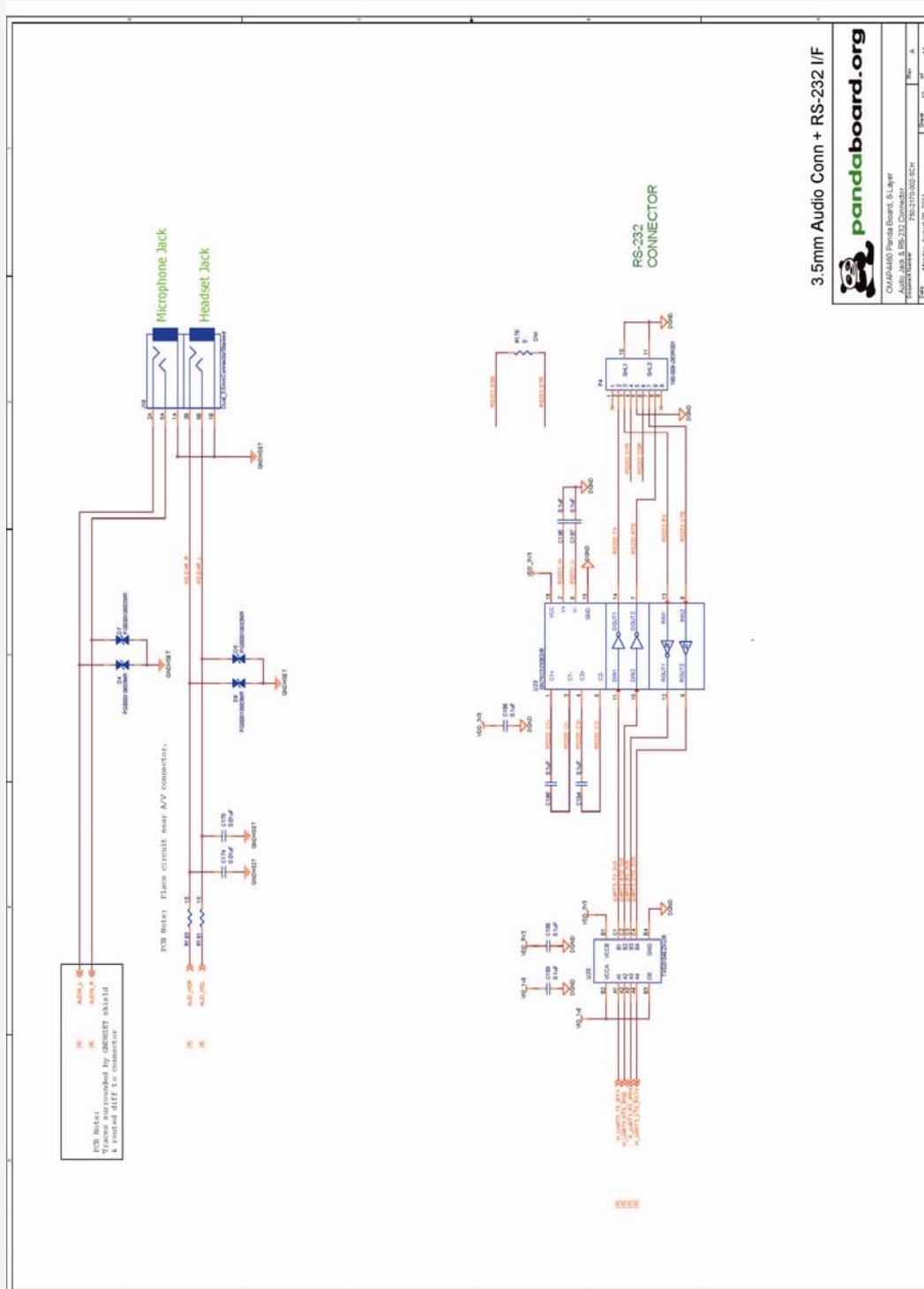


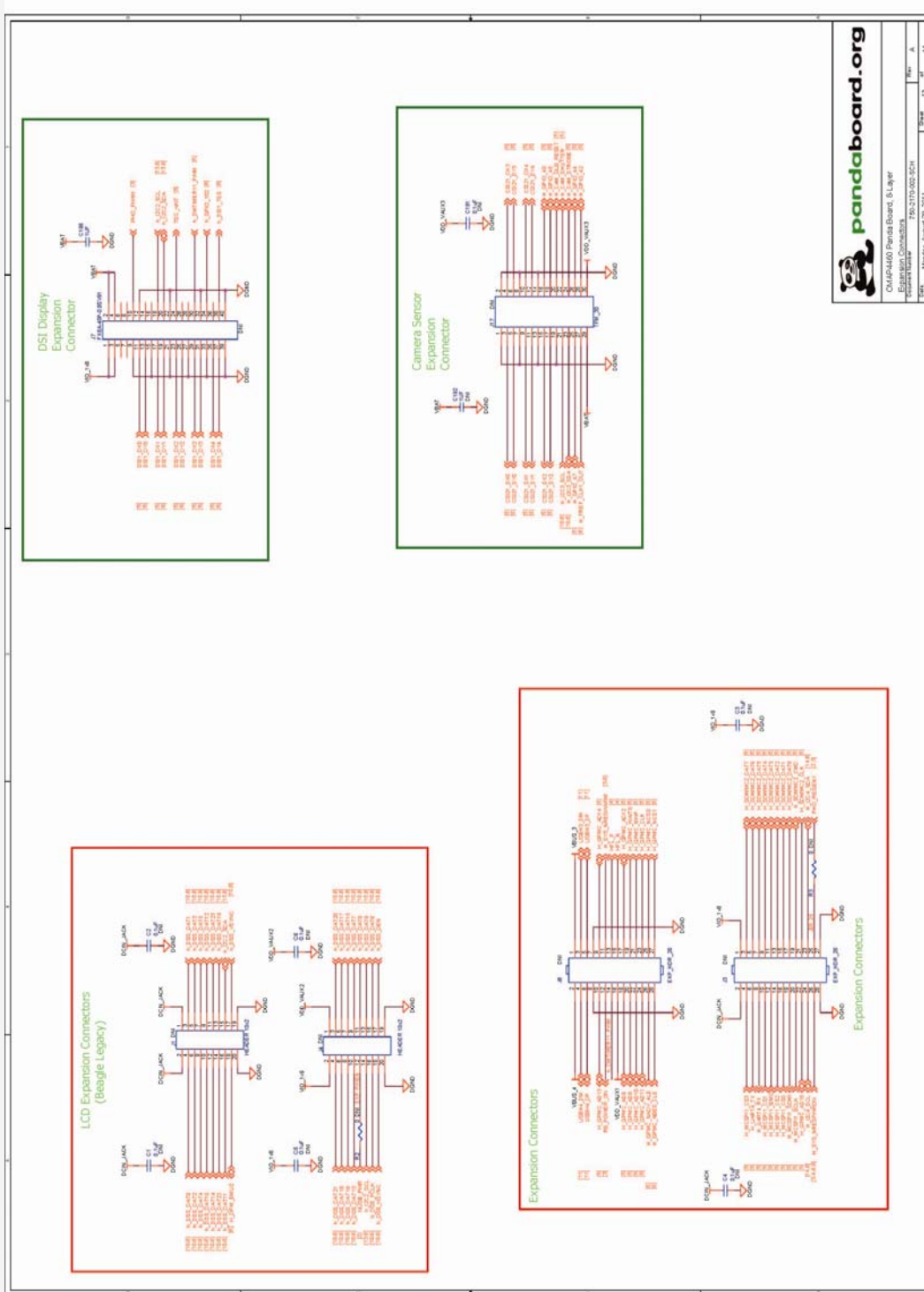












4.5 Pandaboard ES Bill of Materials

The Bill of Material for the OMAP4460 Pandaboard ES is provided at the following location:

<http://Pandaboard.org/content/resources/references>

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We mean it; these design materials may be totally unsuitable for any purposes.

4.6 Pandaboard ES PCB Design Information

The PCB Design information (including the Cadence Allegro 16.3 Board file (.brd file) and PCB Gerber design files) are provided at the following location:

<http://Pandaboard.org/content/resources/references>

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LM2576/LM2576HV Series SIMPLE SWITCHER® 3A Step-Down Voltage Regulator

Check for Samples: [LM2576](#), [LM2576HV](#)

FEATURES

- 3.3V, 5V, 12V, 15V, and Adjustable Output Versions
- Adjustable Version Output Voltage Range, 1.23V to 37V (57V for HV Version) $\pm 4\%$ Max Over Line and Load Conditions
- Specified 3A Output Current
- Wide Input Voltage Range, 40V Up to 60V for HV Version
- Requires Only 4 External Components
- 52 kHz Fixed Frequency Internal Oscillator
- TTL Shutdown Capability, Low Power Standby Mode
- High Efficiency
- Uses Readily Available Standard Inductors
- Thermal Shutdown and Current Limit Protection
- P+ Product Enhancement Tested

APPLICATIONS

- Simple High-Efficiency Step-Down (Buck) Regulator
- Efficient Pre-Regulator for Linear Regulators
- On-Card Switching Regulators
- Positive to Negative Converter (Buck-Boost)

DESCRIPTION

The LM2576 series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving 3A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5V, 12V, 15V, and an adjustable output version.

Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensation and a fixed-frequency oscillator.

The LM2576 series offers a high-efficiency replacement for popular three-terminal linear regulators. It substantially reduces the size of the heat sink, and in some cases no heat sink is required.

A standard series of inductors optimized for use with the LM2576 are available from several different manufacturers. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a specified $\pm 4\%$ tolerance on output voltage within specified input voltages and output load conditions, and $\pm 10\%$ on the oscillator frequency. External shutdown is included, featuring 50 μ A (typical) standby current. The output switch includes cycle-by-cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

TYPICAL APPLICATION

(Fixed Output Voltage Versions)

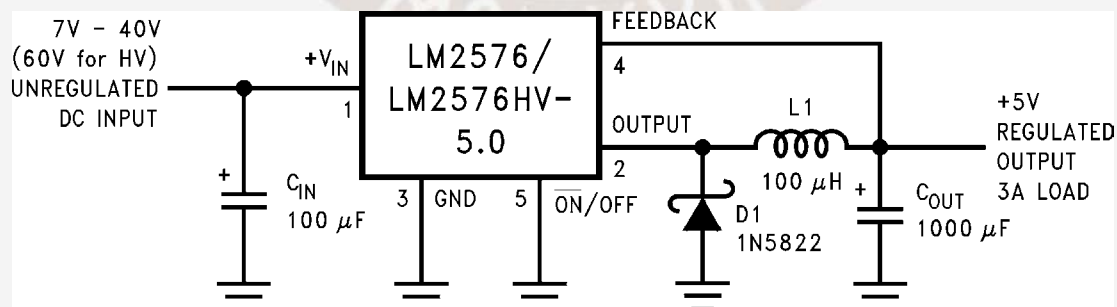


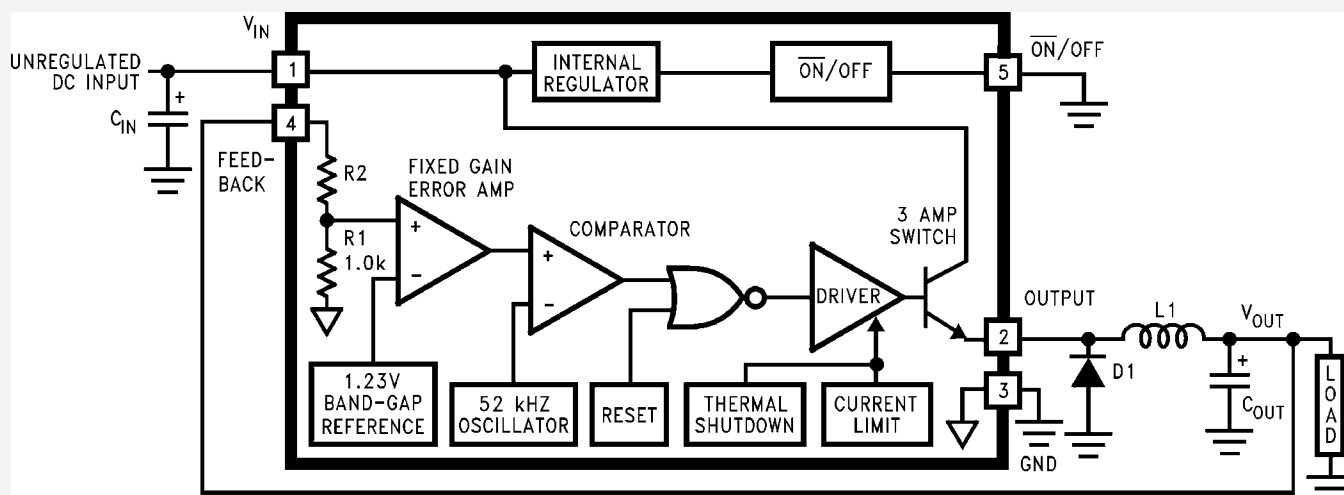
Figure 1.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SIMPLE SWITCHER is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

Block Diagram



3.3V $R2 = 1.7k$
 5V, $R2 = 3.1k$
 12V, $R2 = 8.84k$
 15V, $R2 = 11.3k$
 For ADJ. Version
 $R1 = \text{Open}$, $R2 = 0\Omega$
 Patent Pending



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾⁽²⁾

Maximum Supply Voltage	LM2576	45V
	LM2576HV	63V
ON /OFF Pin Input Voltage		$-0.3V \leq V \leq +V_{IN}$
Output Voltage to Ground	(Steady State)	-1V
Power Dissipation		Internally Limited
Storage Temperature Range		-65°C to +150°C
Maximum Junction Temperature		150°C
Minimum ESD Rating	(C = 100 pF, R = 1.5 kΩ)	2 kV
Lead Temperature	(Soldering, 10 Seconds)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see [ELECTRICAL CHARACTERISTICS ALL OUTPUT VOLTAGE VERSIONS](#).

(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

OPERATING RATINGS

Temperature Range	LM2576/LM2576HV	$-40^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$
Supply Voltage	LM2576	40V
	LM2576HV	60V

ELECTRICAL CHARACTERISTICS LM2576-3.3, LM2576HV-3.3

Specifications with standard type face are for $T_J = 25^{\circ}\text{C}$, and those with **boldface type** apply over full Operating Temperature Range.

Symbol	Parameter	Conditions	LM2576-3.3 LM2576HV-3.3		Units (Limits)
			Typ	Limit ⁽¹⁾	
SYSTEM PARAMETERS Test Circuit Figure 21 and Figure 22 ⁽²⁾					
V _{OUT}	Output Voltage	V _{IN} = 12V, I _{LOAD} = 0.5A Circuit of Figure 21 and Figure 22	3.3	3.234 3.366	V V(Min) V(Max)
V _{OUT}	Output Voltage LM2576	6V ≤ V _{IN} ≤ 40V, 0.5A ≤ I _{LOAD} ≤ 3A Circuit of Figure 21 and Figure 22	3.3	3.168/ 3.135 3.432/ 3.465	V V(Min) V(Max)
V _{OUT}	Output Voltage LM2576HV	6V ≤ V _{IN} ≤ 60V, 0.5A ≤ I _{LOAD} ≤ 3A Circuit of Figure 21 and Figure 22	3.3	3.168/ 3.135 3.450/ 3.482	V V(Min) V(Max)
η	Efficiency	V _{IN} = 12V, I _{LOAD} = 3A	75		%

(1) All limits specified at room temperature (standard type face) and at temperature extremes (bold type face). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods.

(2) External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2576/LM2576HV is used as shown in [Figure 21](#) and [Figure 22](#), system performance will be as shown in [ELECTRICAL CHARACTERISTICS ALL OUTPUT VOLTAGE VERSIONS](#).

ELECTRICAL CHARACTERISTICS LM2576-5.0, LM2576HV-5.0

Specifications with standard type face are for $T_J = 25^\circ\text{C}$, and those with [Figure 21](#) and [Figure 22](#) **boldface type** apply over full Operating Temperature Range.

Symbol	Parameter	Conditions	LM2576-5.0 LM2576HV-5.0		Units (Limits)
			Typ	Limit ⁽¹⁾	
SYSTEM PARAMETERS Figure 21 and Figure 22 ⁽²⁾					
V _{OUT}	Output Voltage	V _{IN} = 12V, I _{LOAD} = 0.5A Circuit of Figure 21 and Figure 22	5.0	4.900 5.100	V V(Min) V(Max)
V _{OUT}	Output Voltage LM2576	0.5A ≤ I _{LOAD} ≤ 3A, 8V ≤ V _{IN} ≤ 40V Circuit of Figure 21 and Figure 22	5.0	4.800/ 4.750 5.200/ 5.250	V V(Min) V(Max)
V _{OUT}	Output Voltage LM2576HV	0.5A ≤ I _{LOAD} ≤ 3A, 8V ≤ V _{IN} ≤ 60V Circuit of Figure 21 and Figure 22	5.0	4.800/ 4.750 5.225/ 5.275	V V(Min) V(Max)
η	Efficiency	V _{IN} = 12V, I _{LOAD} = 3A	77		%

- (1) All limits specified at room temperature (standard type face) and at temperature extremes (bold type face). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods.
- (2) External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2576/LM2576HV is used as shown in [Figure 21](#) and [Figure 22](#), system performance will be as shown in [ELECTRICAL CHARACTERISTICS ALL OUTPUT VOLTAGE VERSIONS](#).

ELECTRICAL CHARACTERISTICS LM2576-12, LM2576HV-12

Specifications with standard type face are for $T_J = 25^\circ\text{C}$, and those with **boldface type** apply over full Operating Temperature Range.

Symbol	Parameter	Conditions	LM2576-12 LM2576HV-12		Units (Limits)
			Typ	Limit ⁽¹⁾	
SYSTEM PARAMETERS Test Circuit <i>Figure 21 and Figure 22</i> ⁽²⁾					
V _{OUT}	Output Voltage	V _{IN} = 25V, I _{LOAD} = 0.5A Circuit of <i>Figure 21</i> and <i>Figure 22</i>	12	11.76 12.24	V V(Min) V(Max)
V _{OUT}	Output Voltage LM2576	0.5A ≤ I _{LOAD} ≤ 3A, 15V ≤ V _{IN} ≤ 40V Circuit of <i>Figure 21</i> and <i>Figure 22</i> and	12	11.52/ 11.40 12.48/ 12.60	V V(Min) V(Max)
V _{OUT}	Output Voltage LM2576HV	0.5A ≤ I _{LOAD} ≤ 3A, 15V ≤ V _{IN} ≤ 60V Circuit of <i>Figure 21</i> and <i>Figure 22</i>	12	11.52/ 11.40 12.54/ 12.66	V V(Min) V(Max)
η	Efficiency	V _{IN} = 15V, I _{LOAD} = 3A	88		%

- (1) All limits specified at room temperature (standard type face) and at temperature extremes (bold type face). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods.
- (2) External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2576/LM2576HV is used as shown in [Figure 21](#) and [Figure 22](#), system performance will be as shown in [ELECTRICAL CHARACTERISTICS ALL OUTPUT VOLTAGE VERSIONS](#).

ELECTRICAL CHARACTERISTICS LM2576-15, LM2576HV-15

Specifications with standard type face are for $T_J = 25^\circ\text{C}$, and those with **boldface type** apply over full Operating Temperature Range.

Symbol	Parameter	Conditions	LM2576-15 LM2576HV-15		Units (Limits)
			Typ	Limit ⁽¹⁾	
SYSTEM PARAMETERS Test Circuit Figure 21 and Figure 22 ⁽²⁾					
V _{OUT}	Output Voltage	V _{IN} = 25V, I _{LOAD} = 0.5A Circuit of Figure 21 and Figure 22	15	14.70 15.30	V V(Min) V(Max)
V _{OUT}	Output Voltage LM2576	0.5A ≤ I _{LOAD} ≤ 3A, 18V ≤ V _{IN} ≤ 40V Circuit of Figure 21 and Figure 22	15	14.40/ 14.25 15.60/ 15.75	V V(Min) V(Max)
V _{OUT}	Output Voltage LM2576HV	0.5A ≤ I _{LOAD} ≤ 3A, 18V ≤ V _{IN} ≤ 60V Circuit of Figure 21 and Figure 22	15	14.40/ 14.25 15.68/ 15.83	V V(Min) V(Max)
η	Efficiency	V _{IN} = 18V, I _{LOAD} = 3A	88		%

- (1) All limits specified at room temperature (standard type face) and at temperature extremes (bold type face). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods.
- (2) External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2576/LM2576HV is used as shown in [Figure 21](#) and [Figure 22](#), system performance will be as shown in [ELECTRICAL CHARACTERISTICS ALL OUTPUT VOLTAGE VERSIONS](#).

ELECTRICAL CHARACTERISTICS LM2576-ADJ, LM2576HV-ADJ

Specifications with standard type face are for $T_J = 25^\circ\text{C}$, and those with **boldface type** apply over full Operating Temperature Range.

Symbol	Parameter	Conditions	LM2576-ADJ LM2576HV-ADJ		Units (Limits)
			Typ	Limit ⁽¹⁾	
SYSTEM PARAMETERS Test Circuit Figure 21 and Figure 22 ⁽²⁾					
V _{OUT}	Feedback Voltage	V _{IN} = 12V, I _{LOAD} = 0.5A V _{OUT} = 5V, Circuit of Figure 21 and Figure 22	1.230	1.217 1.243	V V(Min) V(Max)
V _{OUT}	Feedback Voltage LM2576	0.5A ≤ I _{LOAD} ≤ 3A, 8V ≤ V _{IN} ≤ 40V V _{OUT} = 5V, Circuit of Figure 21 and Figure 22	1.230	1.193/ 1.180 1.267/ 1.280	V V(Min) V(Max)
V _{OUT}	Feedback Voltage LM2576HV	0.5A ≤ I _{LOAD} ≤ 3A, 8V ≤ V _{IN} ≤ 60V V _{OUT} = 5V, Circuit of Figure 21 and Figure 22	1.230	1.193/ 1.180 1.273/ 1.286	V V(Min) V(Max)
η	Efficiency	V _{IN} = 12V, I _{LOAD} = 3A, V _{OUT} = 5V	77		%

- (1) All limits specified at room temperature (standard type face) and at temperature extremes (bold type face). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods.
- (2) External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2576/LM2576HV is used as shown in [Figure 21](#) and [Figure 22](#), system performance will be as shown in [ELECTRICAL CHARACTERISTICS ALL OUTPUT VOLTAGE VERSIONS](#).

ELECTRICAL CHARACTERISTICS ALL OUTPUT VOLTAGE VERSIONS

Specifications with standard type face are for $T_J = 25^\circ\text{C}$, and those with **boldface type** apply over full Operating Temperature Range. Unless otherwise specified, $V_{IN} = 12\text{V}$ for the 3.3V, 5V, and Adjustable version, $V_{IN} = 25\text{V}$ for the 12V version, and $V_{IN} = 30\text{V}$ for the 15V version. $I_{LOAD} = 500\text{ mA}$.

Symbol	Parameter	Conditions	LM2576-XX LM2576HV-XX		Units (Limits)
			Typ	Limit ⁽¹⁾	
DEVICE PARAMETERS					
I _b	Feedback Bias Current	V _{OUT} = 5V (Adjustable Version Only)	50	100/ 500	nA
f _O	Oscillator Frequency	See ⁽²⁾	52	47/ 42 58/ 63	kHz kHz (Min) kHz (Max)
V _{SAT}	Saturation Voltage	I _{OUT} = 3A ⁽³⁾	1.4	1.8/2.0	V V(Max)
DC	Max Duty Cycle (ON)	See ⁽⁴⁾	98	93	% %(Min)
I _{CL}	Current Limit	See ⁽³⁾⁽²⁾	5.8	4.2/ 3.5 6.9/ 7.5	A A(Min) A(Max)
I _L	Output Leakage Current	Output = 0V Output = -1V Output = -1V ⁽⁵⁾⁽⁶⁾	7.5	2 30	mA(Max) mA mA(Max)
I _Q	Quiescent Current	See ⁽⁵⁾	5	10	mA mA(Max)
I _{STBY}	Standby Quiescent Current	$\overline{\text{ON}}$ /OFF Pin = 5V (OFF)	50	200	μA μA(Max)
θ _{JA} θ _{JA} θ _{JC} θ _{JA}	Thermal Resistance	T Package, Junction to Ambient ⁽⁷⁾ T Package, Junction to Ambient ⁽⁸⁾ T Package, Junction to Case S Package, Junction to Ambient ⁽⁹⁾	65 45 2 50		°C/W
$\overline{\text{ON}}$ /OFF CONTROL Test Circuit Figure 21 and Figure 22					
V _{IH}	$\overline{\text{ON}}$ /OFF Pin	V _{OUT} = 0V	1.4	2.2/ 2.4	V(Min)
V _{IL}	Logic Input Level	V _{OUT} = Nominal Output Voltage	1.2	1.0/ 0.8	V(Max)
I _{IH}	$\overline{\text{ON}}$ /OFF Pin Input Current	$\overline{\text{ON}}$ /OFF Pin = 5V (OFF)	12	30	μA μA(Max)
I _{IL}		$\overline{\text{ON}}$ /OFF Pin = 0V (ON)	0	10	μA μA(Max)

- (1) All limits specified at room temperature (standard type face) and at temperature extremes (bold type face). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods.
- (2) The oscillator frequency reduces to approximately 11 kHz in the event of an output short or an overload which causes the regulated output voltage to drop approximately 40% from the nominal output voltage. This self protection feature lowers the average power dissipation of the IC by lowering the minimum duty cycle from 5% down to approximately 2%.
- (3) Output pin sourcing current. No diode, inductor or capacitor connected to output.
- (4) Feedback pin removed from output and connected to 0V.
- (5) Feedback pin removed from output and connected to +12V for the Adjustable, 3.3V, and 5V versions, and +25V for the 12V and 15V versions, to force the output transistor OFF.
- (6) $V_{IN} = 40\text{V}$ (60V for high voltage version).
- (7) Junction to ambient thermal resistance (no external heat sink) for the 5 lead TO-220 package mounted vertically, with $\frac{1}{2}$ inch leads in a socket, or on a PC board with minimum copper area.
- (8) Junction to ambient thermal resistance (no external heat sink) for the 5 lead TO-220 package mounted vertically, with $\frac{1}{4}$ inch leads soldered to a PC board containing approximately 4 square inches of copper area surrounding the leads.
- (9) If the DPAK/TO-263 package is used, the thermal resistance can be reduced by increasing the PC board copper area thermally connected to the package. Using 0.5 square inches of copper area, θ_{JA} is 50°C/W , with 1 square inch of copper area, θ_{JA} is 37°C/W , and with 1.6 or more square inches of copper area, θ_{JA} is 32°C/W .

TYPICAL PERFORMANCE CHARACTERISTICS

(Circuit of [Figure 21](#) and [Figure 22](#))

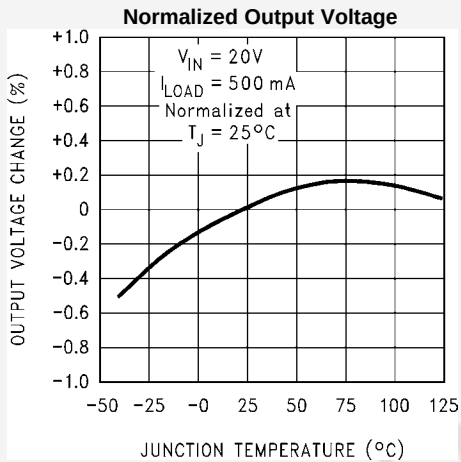


Figure 2.

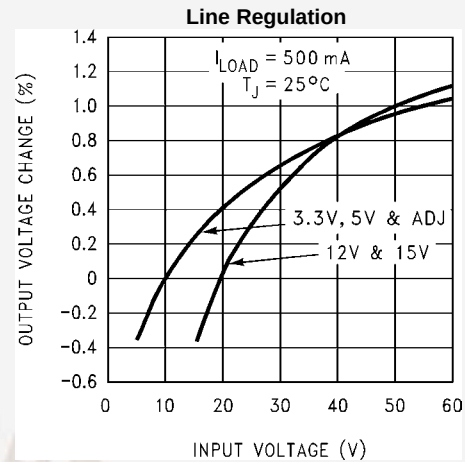


Figure 3.

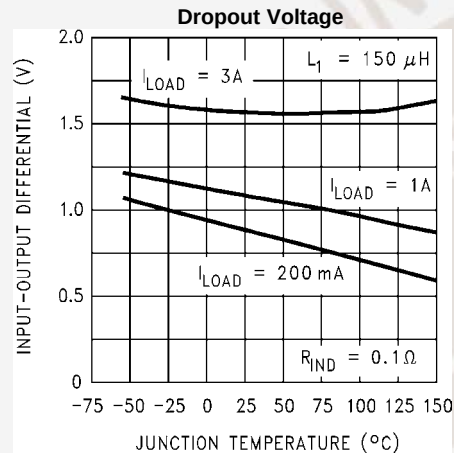


Figure 4.

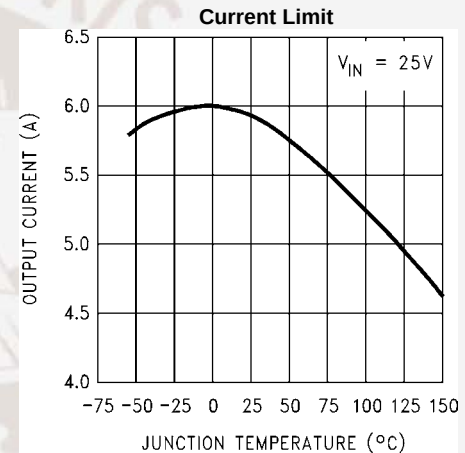


Figure 5.

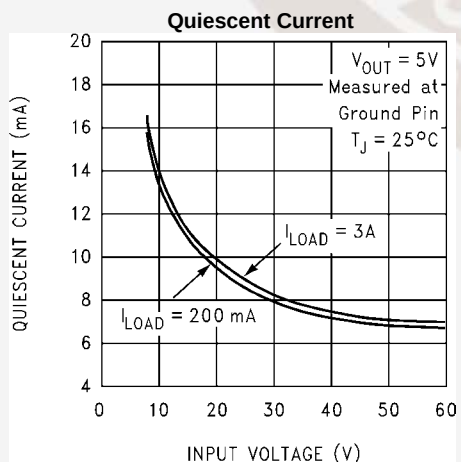


Figure 6.

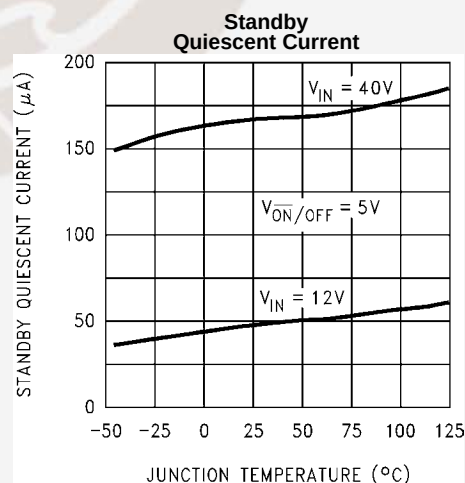
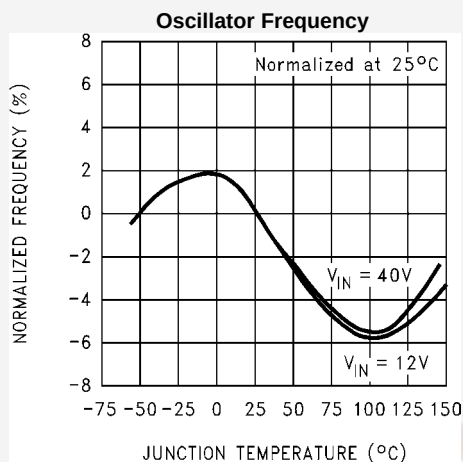
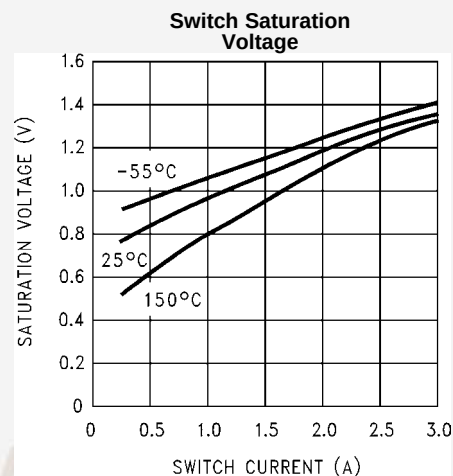
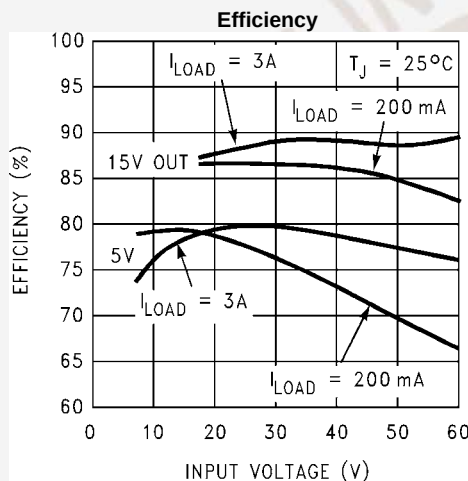
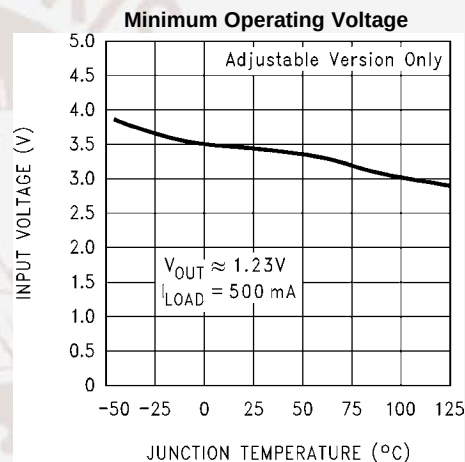
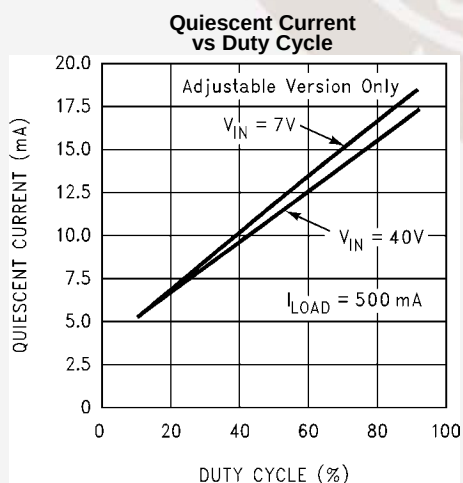
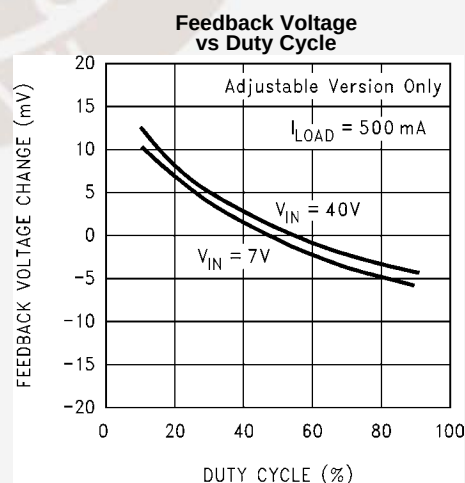


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)(Circuit of [Figure 21](#) and [Figure 22](#))**Figure 8.****Figure 9.****Figure 10.****Figure 11.****Figure 12.****Figure 13.**

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Circuit of [Figure 21](#) and [Figure 22](#))

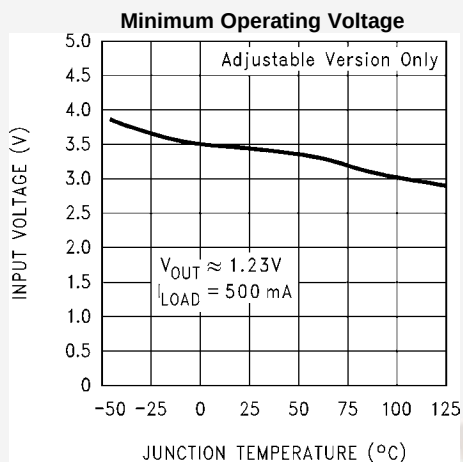


Figure 14.

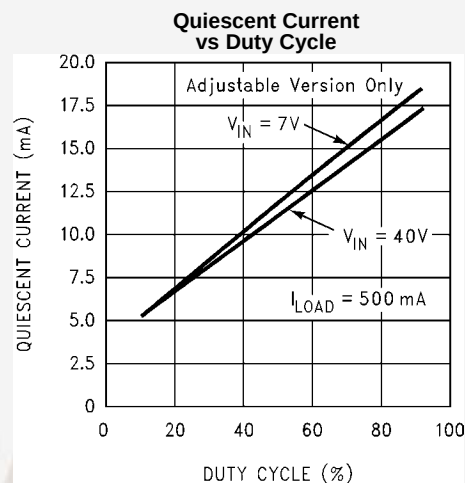


Figure 15.

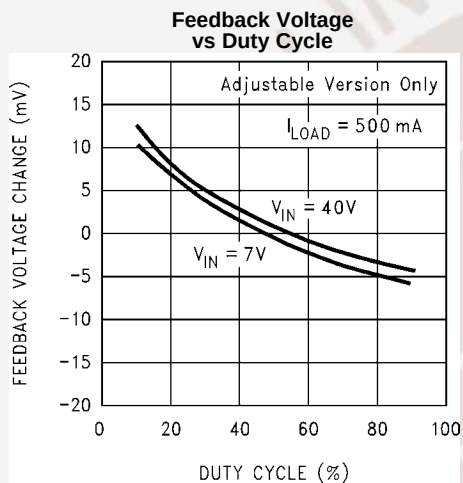


Figure 16.

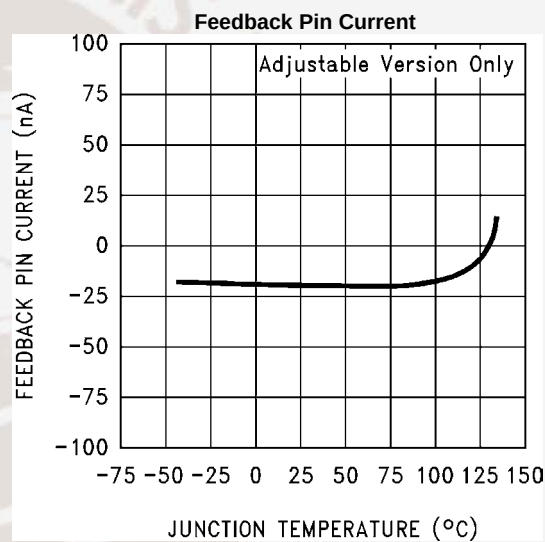
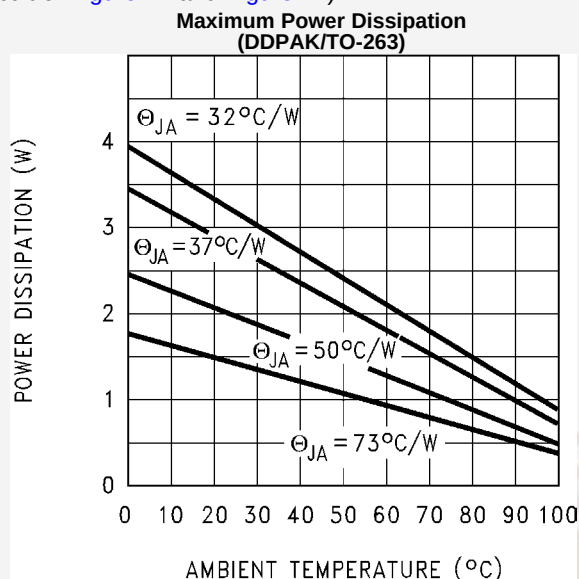
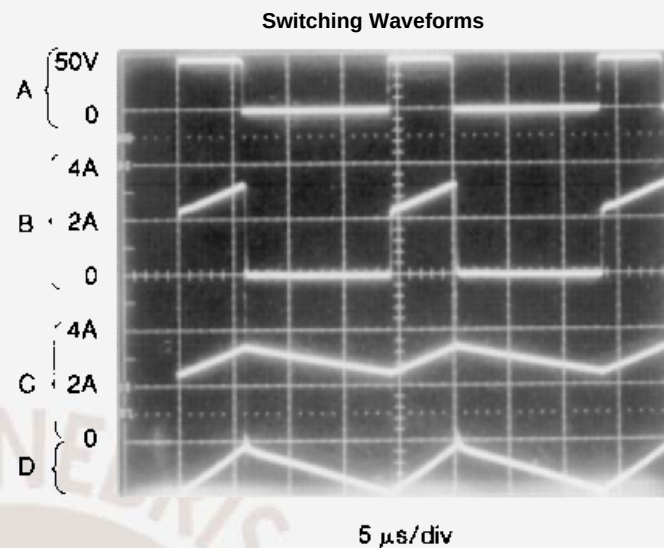


Figure 17.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)(Circuit of [Figure 21](#) and [Figure 22](#))

If the DDPak/TO-263 package is used, the thermal resistance can be reduced by increasing the PC board copper area thermally connected to the package. Using 0.5 square inches of copper area, θ_{JA} is 50°C/W , with 1 square inch of copper area, θ_{JA} is 37°C/W , and with 1.6 or more square inches of copper area, θ_{JA} is 32°C/W .

Figure 18.

 $V_{OUT} = 15\text{V}$

A: Output Pin Voltage, 50V/div

B: Output Pin Current, 2A/div

C: Inductor Current, 2A/div

D: Output Ripple Voltage, 50 mV/div,
AC-CoupledHorizontal Time Base: 5 $\mu\text{s/div}$

Figure 19.

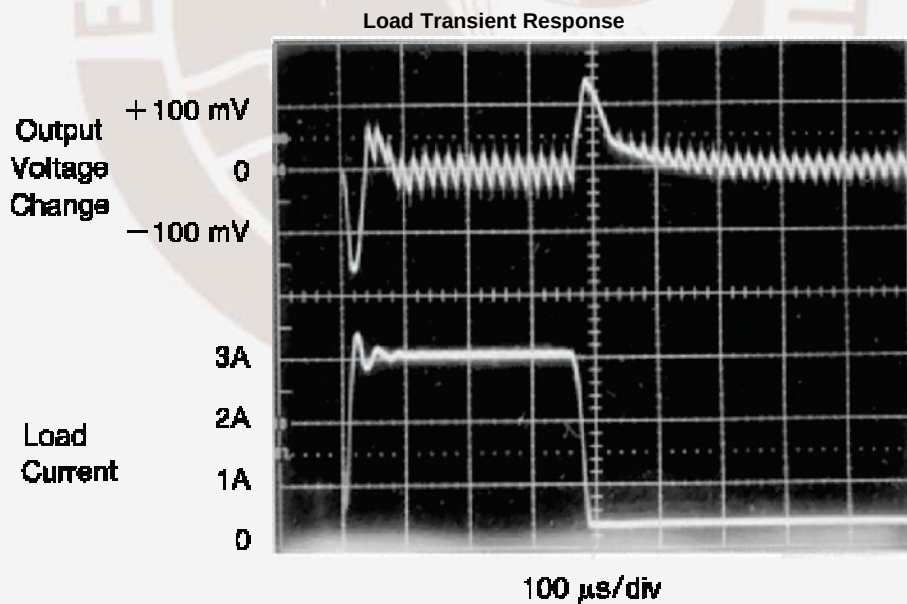
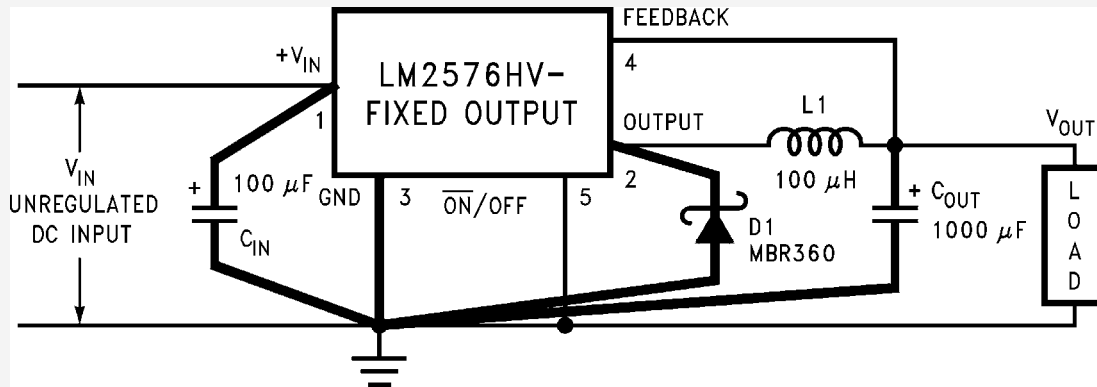


Figure 20.

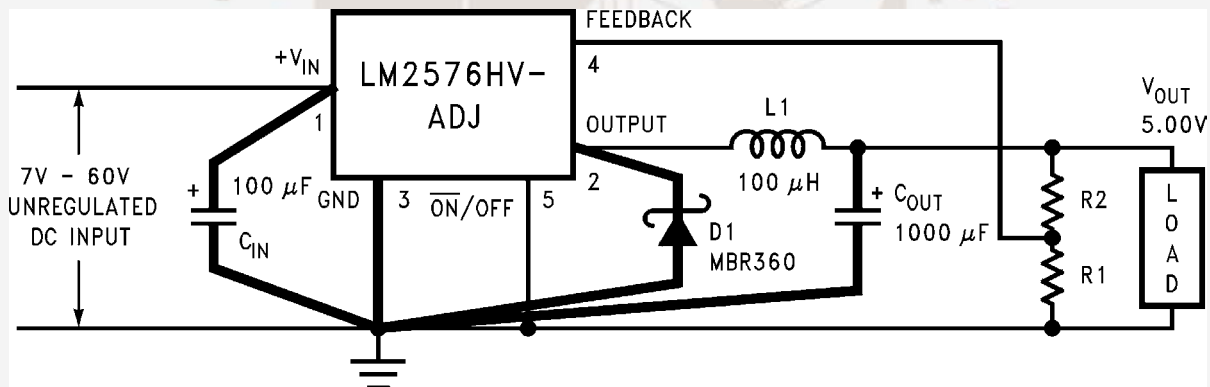
TEST CIRCUIT AND LAYOUT GUIDELINES

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance generate voltage transients which can cause problems. For minimal inductance and ground loops, the length of the leads indicated by heavy lines should be kept as short as possible. Single-point grounding (as indicated) or ground plane construction should be used for best results. When using the Adjustable version, physically locate the programming resistors near the regulator, to keep the sensitive feedback wiring short.



C_{IN} — 100 μ F, 75V, Aluminum Electrolytic
 C_{OUT} — 1000 μ F, 25V, Aluminum Electrolytic
 D_1 — Schottky, MBR360
 L_1 — 100 μ H, Pulse Eng. PE-92108
 R_1 — 2k, 0.1%
 R_2 — 6.12k, 0.1%

Figure 21. Fixed Output Voltage Versions



$$V_{OUT} = V_{REF} \left(1 + \frac{R_2}{R_1} \right)$$

$$R_2 = R_1 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

where

$V_{REF} = 1.23V$, R_1 between 1k and 5k

Figure 22. Adjustable Output Voltage Version

LM2576 Series Buck Regulator Design Procedure

PROCEDURE (Fixed Output Voltage Versions)	EXAMPLE (Fixed Output Voltage Versions)
Given: V_{OUT} = Regulated Output Voltage (3.3V, 5V, 12V, or 15V) $V_{IN(Max)}$ = Maximum Input Voltage $I_{LOAD(Max)}$ = Maximum Load Current	Given: V_{OUT} = 5V $V_{IN(Max)}$ = 15V $I_{LOAD(Max)}$ = 3A
1. Inductor Selection (L1) A. Select the correct Inductor value selection guide from Figure 23 , Figure 24 , Figure 25 , or Figure 26 . (Output voltages of 3.3V, 5V, 12V or 15V respectively). For other output voltages, see the design procedure for the adjustable version. B. From the inductor value selection guide, identify the inductance region intersected by $V_{IN(Max)}$ and $I_{LOAD(Max)}$, and note the inductor code for that region. C. Identify the inductor value from the inductor code, and select an appropriate inductor from the table shown in Figure 23 . Part numbers are listed for three inductor manufacturers. The inductor chosen must be rated for operation at the LM2576 switching frequency (52 kHz) and for a current rating of $1.15 \times I_{LOAD}$. For additional inductor information, see INDUCTOR SELECTION .	1. Inductor Selection (L1) A. Use the selection guide shown in Figure 24 . B. From the selection guide, the inductance area intersected by the 15V line and 3A line is L100. C. Inductor value required is 100 μ H. From the table in Figure 23 . Choose AIE 415-0930, Pulse Engineering PE92108, or Renco RL2444.
2. Output Capacitor Selection (C_{OUT}) A. The value of the output capacitor together with the inductor defines the dominate pole-pair of the switching regulator loop. For stable operation and an acceptable output ripple voltage, (approximately 1% of the output voltage) a value between 100 μ F and 470 μ F is recommended. B. The capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5V regulator, a rating of at least 8V is appropriate, and a 10V or 15V rating is recommended. Higher voltage electrolytic capacitors generally have lower ESR numbers, and for this reason it may be necessary to select a capacitor rated for a higher voltage than would normally be needed.	2. Output Capacitor Selection (C_{OUT}) A. C_{OUT} = 680 μ F to 2000 μ F standard aluminum electrolytic. B. Capacitor voltage rating = 20V.
3. Catch Diode Selection (D1) A. The catch-diode current rating must be at least 1.2 times greater than the maximum load current. Also, if the power supply design must withstand a continuous output short, the diode should have a current rating equal to the maximum current limit of the LM2576. The most stressful condition for this diode is an overload or shorted output condition. B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.	3. Catch Diode Selection (D1) A. For this example, a 3A current rating is adequate. B. Use a 20V 1N5823 or SR302 Schottky diode, or any of the suggested fast-recovery diodes shown in Table 1 .
4. Input Capacitor (C_{IN}) An aluminum or tantalum electrolytic bypass capacitor located close to the regulator is needed for stable operation.	4. Input Capacitor (C_{IN}) A 100 μ F, 25V aluminum electrolytic capacitor located near the input and ground pins provides sufficient bypassing.

INDUCTOR VALUE SELECTION GUIDES

(For Continuous Mode Operation)

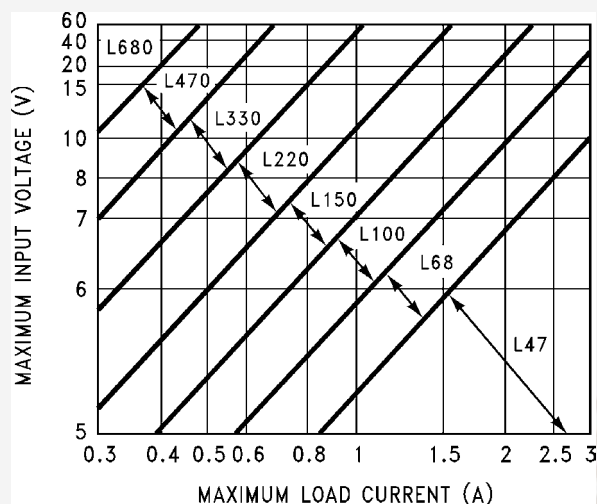


Figure 23. LM2576(HV)-3.3

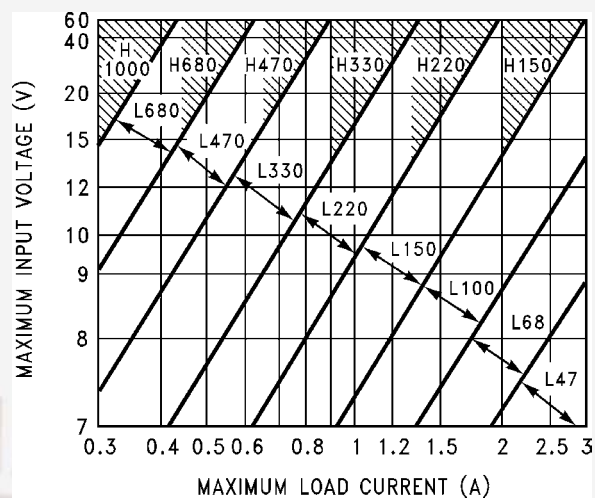


Figure 24. LM2576(HV)-5.0

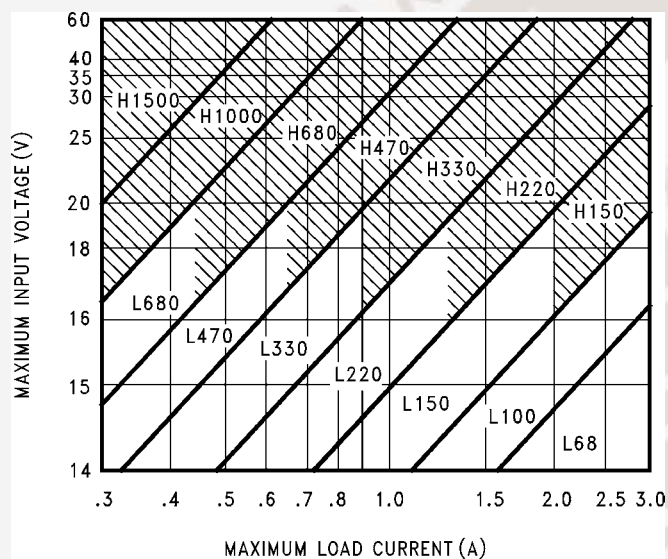


Figure 25. LM2576(HV)-12

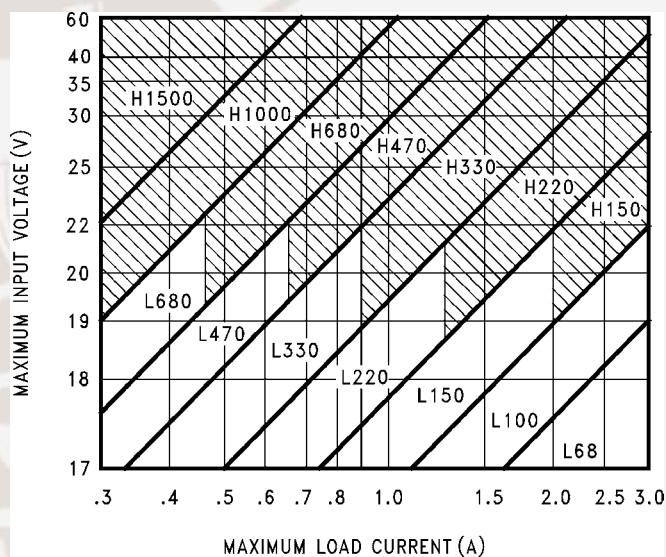


Figure 26. LM2576(HV)-15

(For Continuous Mode Operation)

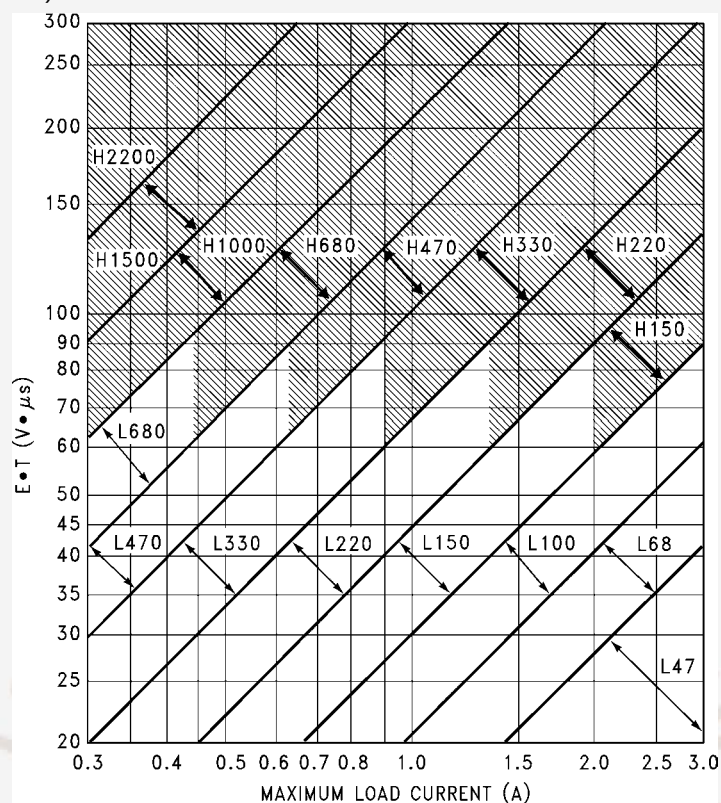


Figure 27. LM2576(HV)-ADJ

PROCEDURE (Adjustable Output Voltage Versions)	EXAMPLE (Adjustable Output Voltage Versions)
Given: V_{OUT} = Regulated Output Voltage $V_{IN(Max)}$ = Maximum Input Voltage $I_{LOAD(Max)}$ = Maximum Load Current F = Switching Frequency (Fixed at 52 kHz)	Given: $V_{OUT} = 10V$ $V_{IN(Max)} = 25V$ $I_{LOAD(Max)} = 3A$ $F = 52 \text{ kHz}$
1. Programming Output Voltage (Selecting R_1 and R_2 , as shown in Figure 21 and Figure 22) Use the following formula to select the appropriate resistor values. $V_{OUT} = V_{REF} \left(1 + \frac{R_2}{R_1} \right) \quad \text{where } V_{REF} = 1.23V$ R_1 can be between 1k and 5k. (For best temperature coefficient and stability with time, use 1% metal film resistors) $R_2 = R_1 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$	1. Programming Output Voltage (Selecting R_1 and R_2) $V_{OUT} = 1.23 \left(1 + \frac{R_2}{R_1} \right) \quad \text{Select } R_1 = 1k$ $R_2 = R_1 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) = 1k \left(\frac{10V}{1.23V} - 1 \right)$ $R_2 = 1k (8.13 - 1) = 7.13k$, closest 1% value is 7.15k

(For Continuous Mode Operation)

PROCEDURE (Adjustable Output Voltage Versions)	EXAMPLE (Adjustable Output Voltage Versions)
2. Inductor Selection (L1) A. Calculate the inductor Volt • microsecond constant, $E \cdot T$ ($V \cdot \mu s$), from the following formula: $E \cdot T = (V_{IN} - V_{OUT}) \frac{V_{OUT}}{V_{IN}} \cdot \frac{1000}{F \text{ (in kHz)}} (V \cdot \mu s)$ B. Use the $E \cdot T$ value from the previous formula and match it with the $E \cdot T$ number on the vertical axis of the Inductor Value Selection Guide shown in Figure 27. C. On the horizontal axis, select the maximum load current. D. Identify the inductance region intersected by the $E \cdot T$ value and the maximum load current value, and note the inductor code for that region. E. Identify the inductor value from the inductor code, and select an appropriate inductor from the table shown in Table 2. Part numbers are listed for three inductor manufacturers. The inductor chosen must be rated for operation at the LM2576 switching frequency (52 kHz) and for a current rating of $1.15 \times I_{LOAD}$. For additional inductor information, see INDUCTOR SELECTION.	2. Inductor Selection (L1) A. Calculate $E \cdot T$ ($V \cdot \mu s$) $E \cdot T = (25 - 10) \cdot \frac{10}{25} \cdot \frac{1000}{52} = 115 V \cdot \mu s$ B. $E \cdot T = 115 V \cdot \mu s$ C. $I_{LOAD}(\text{Max}) = 3A$ D. Inductance Region = H150 E. Inductor Value = 150 μH Choose from AIE part #415-0936 Pulse Engineering part #PE-531115, or Renco part #RL2445.
3. Output Capacitor Selection (C_{OUT}) A. The value of the output capacitor together with the inductor defines the dominate pole-pair of the switching regulator loop. For stable operation, the capacitor must satisfy the following requirement: $C_{OUT} \geq 13,300 \frac{V_{IN}(\text{Max})}{V_{OUT} \cdot L(\mu H)} (\mu F)$ The above formula yields capacitor values between 10 μF and 2200 μF that will satisfy the loop requirements for stable operation. But to achieve an acceptable output ripple voltage, (approximately 1% of the output voltage) and transient response, the output capacitor may need to be several times larger than the above formula yields. B. The capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 10V regulator, a rating of at least 15V or more is recommended. Higher voltage electrolytic capacitors generally have lower ESR numbers, and for this reason it may be necessary to select a capacitor rate for a higher voltage than would normally be needed.	3. Output Capacitor Selection (C_{OUT}) $C_{OUT} > 13,300 \frac{25}{10 \cdot 150} = 22.2 \mu F$ However, for acceptable output ripple voltage select $C_{OUT} \geq 680 \mu F$ $C_{OUT} = 680 \mu F$ electrolytic capacitor
4. Catch Diode Selection (D1) A. The catch-diode current rating must be at least 1.2 times greater than the maximum load current. Also, if the power supply design must withstand a continuous output short, the diode should have a current rating equal to the maximum current limit of the LM2576. The most stressful condition for this diode is an overload or shorted output. See Table 1. B. The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.	4. Catch Diode Selection (D1) A. For this example, a 3.3A current rating is adequate. B. Use a 30V 31DQ03 Schottky diode, or any of the suggested fast-recovery diodes in Table 1.
5. Input Capacitor (C_{IN}) An aluminum or tantalum electrolytic bypass capacitor located close to the regulator is needed for stable operation.	5. Input Capacitor (C_{IN}) A 100 μF aluminum electrolytic capacitor located near the input and ground pins provides sufficient bypassing.

To further simplify the buck regulator design procedure, TI is making available computer design software to be used with the **SIMPLE SWITCHER** line of switching regulators. **Switchers Made Simple** (Version 3.3) is available on a (3½") diskette for IBM compatible computers from a TI office in your area.

Table 1. Diode Selection Guide

V_R	Schottky		Fast Recovery	
	3A	4A–6A	3A	4A–6A
20V	1N5820 MBR320P SR302	1N5823	The following diodes are all rated to 100V 31DF1 HER302	The following diodes are all rated to 100V 50WF10 MUR410 HER602
30V	1N5821 MBR330 31DQ03 SR303	50WQ03 1N5824		
40V	1N5822 MBR340 31DQ04 SR304	MBR340 50WQ04 1N5825		
50V	MBR350 31DQ05 SR305	50WQ05		
60V	MBR360 DQ06 SR306	50WR06 50SQ060		

Table 2. Inductor Selection by Manufacturer's Part Number

Inductor Code	Inductor Value	Schott ⁽¹⁾	Pulse Eng. ⁽²⁾	Renco ⁽³⁾
L47	47 μ H	671 26980	PE-53112	RL2442
L68	68 μ H	671 26990	PE-92114	RL2443
L100	100 μ H	671 27000	PE-92108	RL2444
L150	150 μ H	671 27010	PE-53113	RL1954
L220	220 μ H	671 27020	PE-52626	RL1953
L330	330 μ H	671 27030	PE-52627	RL1952
L470	470 μ H	671 27040	PE-53114	RL1951
L680	680 μ H	671 27050	PE-52629	RL1950
H150	150 μ H	671 27060	PE-53115	RL2445
H220	220 μ H	671 27070	PE-53116	RL2446
H330	330 μ H	671 27080	PE-53117	RL2447
H470	470 μ H	671 27090	PE-53118	RL1961
H680	680 μ H	671 27100	PE-53119	RL1960
H1000	1000 μ H	671 27110	PE-53120	RL1959
H1500	1500 μ H	671 27120	PE-53121	RL1958
H2200	2200 μ H	671 27130	PE-53122	RL2448

(1) Schott Corporation, (612) 475-1173, 1000 Parkers Lake Road, Wayzata, MN 55391.

(2) Pulse Engineering, (619) 674-8100, P.O. Box 12235, San Diego, CA 92112.

(3) Renco Electronics Incorporated, (516) 586-5566, 60 Jeffryn Blvd. East, Deer Park, NY 11729.

APPLICATION HINTS

INPUT CAPACITOR (C_{IN})

To maintain stability, the regulator input pin must be bypassed with at least a 100 μ F electrolytic capacitor. The capacitor's leads must be kept short, and located near the regulator.

If the operating temperature range includes temperatures below -25°C , the input capacitor value may need to be larger. With most electrolytic capacitors, the capacitance value decreases and the ESR increases with lower temperatures and age. Paralleling a ceramic or solid tantalum capacitor will increase the regulator stability at cold temperatures. For maximum capacitor operating lifetime, the capacitor's RMS ripple current rating should be greater than

$$1.2 \times \left(\frac{t_{ON}}{T} \right) \times I_{LOAD}$$

$$\text{where } \frac{t_{ON}}{T} = \frac{V_{OUT}}{V_{IN}} \text{ for a buck regulator}$$

$$\text{and } \frac{t_{ON}}{T} = \frac{|V_{OUT}|}{|V_{OUT}| + V_{IN}} \text{ for a buck-boost regulator.}$$

(1)

INDUCTOR SELECTION

All switching regulators have two basic modes of operation: continuous and discontinuous. The difference between the two types relates to the inductor current, whether it is flowing continuously, or if it drops to zero for a period of time in the normal switching cycle. Each mode has distinctively different operating characteristics, which can affect the regulator performance and requirements.

The LM2576 (or any of the SIMPLE SWITCHER family) can be used for both continuous and discontinuous modes of operation.

The inductor value selection guides in [Figure 23](#) through [Figure 27](#) were designed for buck regulator designs of the continuous inductor current type. When using inductor values shown in the inductor selection guide, the peak-to-peak inductor ripple current will be approximately 20% to 30% of the maximum DC current. With relatively heavy load currents, the circuit operates in the continuous mode (inductor current always flowing), but under light load conditions, the circuit will be forced to the discontinuous mode (inductor current falls to zero for a period of time). This discontinuous mode of operation is perfectly acceptable. For light loads (less than approximately 300 mA) it may be desirable to operate the regulator in the discontinuous mode, primarily because of the lower inductor values required for the discontinuous mode.

The selection guide chooses inductor values suitable for continuous mode operation, but if the inductor value chosen is prohibitively high, the designer should investigate the possibility of discontinuous operation. The computer design software **Switchers Made Simple** will provide all component values for discontinuous (as well as continuous) mode of operation.

Inductors are available in different styles such as pot core, toriod, E-frame, bobbin core, and so on, as well as different core materials, such as ferrites and powdered iron. The least expensive, the bobbin core type, consists of wire wrapped on a ferrite rod core. This type of construction makes for an inexpensive inductor, but since the magnetic flux is not completely contained within the core, it generates more electromagnetic interference (EMI). This EMI can cause problems in sensitive circuits, or can give incorrect scope readings because of induced voltages in the scope probe.

The inductors listed in the selection chart include ferrite pot core construction for AIE, powdered iron toroid for Pulse Engineering, and ferrite bobbin core for Renco.

An inductor should not be operated beyond its maximum rated current because it may saturate. When an inductor begins to saturate, the inductance decreases rapidly and the inductor begins to look mainly resistive (the DC resistance of the winding). This will cause the switch current to rise very rapidly. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.

The inductor manufacturer's data sheets include current and energy limits to avoid inductor saturation.

INDUCTOR RIPPLE CURRENT

When the switcher is operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage). For a given input voltage and output voltage, the peak-to-peak amplitude of this inductor current waveform remains constant. As the load current rises or falls, the entire sawtooth current waveform also rises or falls. The average DC value of this waveform is equal to the DC load current (in the buck regulator configuration).

If the load current drops to a low enough level, the bottom of the sawtooth current waveform will reach zero, and the switcher will change to a discontinuous mode of operation. This is a perfectly acceptable mode of operation. Any buck switching regulator (no matter how large the inductor value is) will be forced to run discontinuous if the load current is light enough.

OUTPUT CAPACITOR

An output capacitor is required to filter the output voltage and is needed for loop stability. The capacitor should be located near the LM2576 using short pc board traces. Standard aluminum electrolytics are usually adequate, but low ESR types are recommended for low output ripple voltage and good stability. The ESR of a capacitor depends on many factors, some which are: the value, the voltage rating, physical size and the type of construction. In general, low value or low voltage (less than 12V) electrolytic capacitors usually have higher ESR numbers.

The amount of output ripple voltage is primarily a function of the ESR (Equivalent Series Resistance) of the output capacitor and the amplitude of the inductor ripple current (ΔI_{IND}). See [INDUCTOR RIPPLE CURRENT](#).

The lower capacitor values (220 μ F–1000 μ F) will allow typically 50 mV to 150 mV of output ripple voltage, while larger-value capacitors will reduce the ripple to approximately 20 mV to 50 mV.

$$\text{Output Ripple Voltage} = (\Delta I_{IND}) (\text{ESR of } C_{OUT}) \quad (2)$$

To further reduce the output ripple voltage, several standard electrolytic capacitors may be paralleled, or a higher-grade capacitor may be used. Such capacitors are often called “high-frequency,” “low-inductance,” or “low-ESR.” These will reduce the output ripple to 10 mV or 20 mV. However, when operating in the continuous mode, reducing the ESR below 0.03 Ω can cause instability in the regulator.

Tantalum capacitors can have a very low ESR, and should be carefully evaluated if it is the only output capacitor. Because of their good low temperature characteristics, a tantalum can be used in parallel with aluminum electrolytics, with the tantalum making up 10% or 20% of the total capacitance.

The capacitor's ripple current rating at 52 kHz should be at least 50% higher than the peak-to-peak inductor ripple current.

CATCH DIODE

Buck regulators require a diode to provide a return path for the inductor current when the switch is off. This diode should be located close to the LM2576 using short leads and short printed circuit traces.

Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best efficiency, especially in low output voltage switching regulators (less than 5V). Fast-Recovery, High-Efficiency, or Ultra-Fast Recovery diodes are also suitable, but some types with an abrupt turn-off characteristic may cause instability and EMI problems. A fast-recovery diode with soft recovery characteristics is a better choice. Standard 60 Hz diodes (e.g., 1N4001 or 1N5400, and so on) are also **not suitable**. See [Table 1](#) for Schottky and “soft” fast-recovery diode selection guide.

OUTPUT VOLTAGE RIPPLE AND TRANSIENTS

The output voltage of a switching power supply will contain a sawtooth ripple voltage at the switcher frequency, typically about 1% of the output voltage, and may also contain short voltage spikes at the peaks of the sawtooth waveform.

The output ripple voltage is due mainly to the inductor sawtooth ripple current multiplied by the ESR of the output capacitor. (See [INDUCTOR SELECTION](#))

The voltage spikes are present because of the the fast switching action of the output switch, and the parasitic inductance of the output filter capacitor. To minimize these voltage spikes, special low inductance capacitors can be used, and their lead lengths must be kept short. Wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all contribute to the amplitude of these spikes.

An additional small LC filter (20 μ H & 100 μ F) can be added to the output (as shown in [Figure 33](#)) to further reduce the amount of output ripple and transients. A 10 $\times$ reduction in output ripple voltage and transients is possible with this filter.

FEEDBACK CONNECTION

The LM2576 (fixed voltage versions) feedback pin must be wired to the output voltage point of the switching power supply. When using the adjustable version, physically locate both output voltage programming resistors near the LM2576 to avoid picking up unwanted noise. Avoid using resistors greater than 100 k Ω because of the increased chance of noise pickup.

ON /OFF INPUT

For normal operation, the $\overline{\text{ON}}$ /OFF pin should be grounded or driven with a low-level TTL voltage (typically below 1.6V). To put the regulator into standby mode, drive this pin with a high-level TTL or CMOS signal. The $\overline{\text{ON}}$ /OFF pin can be safely pulled up to +V_{IN} without a resistor in series with it. The $\overline{\text{ON}}$ /OFF pin should not be left open.

GROUNDING

To maintain output voltage stability, the power ground connections must be low-impedance (see [Figure 21](#) and [Figure 22](#)). For the 5-lead TO-220 and DPAK/TO-263 style package, both the tab and pin 3 are ground and either connection may be used, as they are both part of the same copper lead frame.

HEAT SINK/THERMAL CONSIDERATIONS

In many cases, only a small heat sink is required to keep the LM2576 junction temperature within the allowed operating range. For each application, to determine whether or not a heat sink will be required, the following must be identified:

1. Maximum ambient temperature (in the application).
2. Maximum regulator power dissipation (in application).
3. Maximum allowed junction temperature (125°C for the LM2576). For a safe, conservative design, a temperature approximately 15°C cooler than the maximum temperatures should be selected.
4. LM2576 package thermal resistances θ_{JA} and θ_{JC} .

Total power dissipated by the LM2576 can be estimated as follows:

$$P_D = (V_{IN})(I_Q) + (V_O/V_{IN})(I_{LOAD})(V_{SAT})$$

where

- I_Q (quiescent current) and V_{SAT} can be found in [TYPICAL PERFORMANCE CHARACTERISTICS](#) shown previously,
- V_{IN} is the applied minimum input voltage, V_O is the regulated output voltage,
- and I_{LOAD} is the load current.

(3)

The dynamic losses during turn-on and turn-off are negligible if a Schottky type catch diode is used.

When no heat sink is used, the junction temperature rise can be determined by the following:

$$\Delta T_J = (P_D) (\theta_{JA}) \quad (4)$$

To arrive at the actual operating junction temperature, add the junction temperature rise to the maximum ambient temperature.

$$T_J = \Delta T_J + T_A \quad (5)$$

If the actual operating junction temperature is greater than the selected safe operating junction temperature determined in step 3, then a heat sink is required.

When using a heat sink, the junction temperature rise can be determined by the following:

$$\Delta T_J = (P_D) (\theta_{JC} + \theta_{\text{interface}} + \theta_{\text{Heat sink}}) \quad (6)$$

The operating junction temperature will be:

$$T_J = T_A + \Delta T_J \quad (7)$$

As in [Equation 14](#), if the actual operating junction temperature is greater than the selected safe operating junction temperature, then a larger heat sink is required (one that has a lower thermal resistance).

Included on the **Switcher Made Simple** design software is a more precise (non-linear) thermal model that can be used to determine junction temperature with different input-output parameters or different component values. It can also calculate the heat sink thermal resistance required to maintain the regulators junction temperature below the maximum operating temperature.

Additional Applications

INVERTING REGULATOR

[Figure 28](#) shows a LM2576-12 in a buck-boost configuration to generate a negative 12V output from a positive input voltage. This circuit bootstraps the regulator's ground pin to the negative output voltage, then by grounding the feedback pin, the regulator senses the inverted output voltage and regulates it to -12V.

For an input voltage of 12V or more, the maximum available output current in this configuration is approximately 700 mA. At lighter loads, the minimum input voltage required drops to approximately 4.7V.

The switch currents in this buck-boost configuration are higher than in the standard buck-mode design, thus lowering the available output current. Also, the start-up input current of the buck-boost converter is higher than the standard buck-mode regulator, and this may overload an input power source with a current limit less than 5A. Using a delayed turn-on or an undervoltage lockout circuit (described in [NEGATIVE BOOST REGULATOR](#)) would allow the input voltage to rise to a high enough level before the switcher would be allowed to turn on.

Because of the structural differences between the buck and the buck-boost regulator topologies, the buck regulator design procedure section can not be used to select the inductor or the output capacitor. The recommended range of inductor values for the buck-boost design is between 68 μH and 220 μH , and the output capacitor values must be larger than what is normally required for buck designs. Low input voltages or high output currents require a large value output capacitor (in the thousands of micro Farads).

The peak inductor current, which is the same as the peak switch current, can be calculated from the following formula:

$$I_p \approx \frac{I_{\text{LOAD}} (V_{\text{IN}} + |V_O|)}{V_{\text{IN}}} + \frac{V_{\text{IN}} |V_O|}{V_{\text{IN}} + |V_O|} \times \frac{1}{2L_1 f_{\text{osc}}}$$

where

- $f_{\text{osc}} = 52 \text{ kHz}$ (8)

Under normal continuous inductor current operating conditions, the minimum V_{IN} represents the worst case. Select an inductor that is rated for the peak current anticipated.

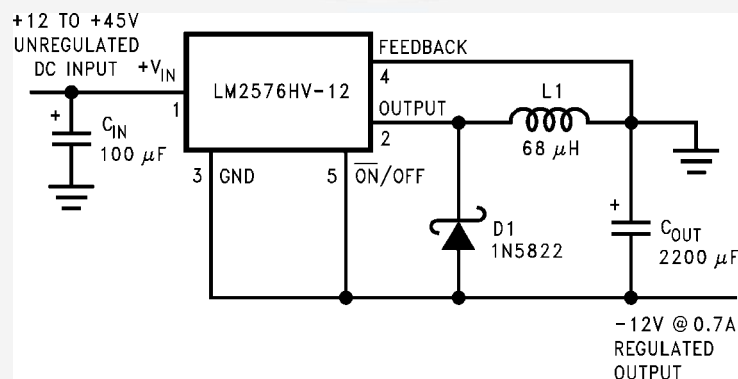


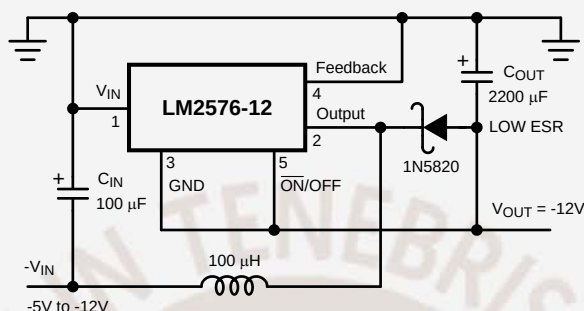
Figure 28. Inverting Buck-Boost Develops -12V

Also, the maximum voltage appearing across the regulator is the absolute sum of the input and output voltage. For a -12V output, the maximum input voltage for the LM2576 is +28V, or +48V for the LM2576HV.

The **Switchers Made Simple** (version 3.0) design software can be used to determine the feasibility of regulator designs using different topologies, different input-output parameters, different components, and so on.

NEGATIVE BOOST REGULATOR

Another variation on the buck-boost topology is the negative boost configuration. The circuit in Figure 29 accepts an input voltage ranging from -5V to -12V and provides a regulated -12V output. Input voltages greater than -12V will cause the output to rise above -12V, but will not damage the regulator.



Typical Load Current
400 mA for $V_{IN} = -5.2V$
750 mA for $V_{IN} = -7V$
Heat sink may be required.

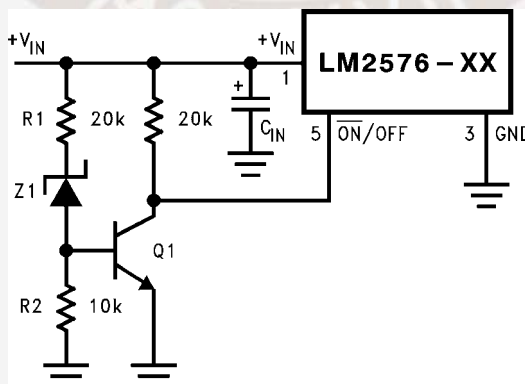
Figure 29. Negative Boost

Because of the boosting function of this type of regulator, the switch current is relatively high, especially at low input voltages. Output load current limitations are a result of the maximum current rating of the switch. Also, boost regulators can not provide current limiting load protection in the event of a shorted load, so some other means (such as a fuse) may be necessary.

UNDERVOLTAGE LOCKOUT

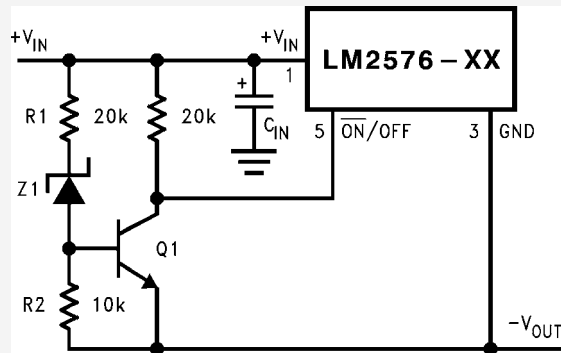
In some applications it is desirable to keep the regulator off until the input voltage reaches a certain threshold. An undervoltage lockout circuit which accomplishes this task is shown in Figure 30, while Figure 31 shows the same circuit applied to a buck-boost configuration. These circuits keep the regulator off until the input voltage reaches a predetermined level.

$$V_{TH} \approx V_{Z1} + 2V_{BE}(Q1)$$



Complete circuit not shown.

Figure 30. Undervoltage Lockout for Buck Circuit



Complete circuit not shown (see [Figure 28](#)).

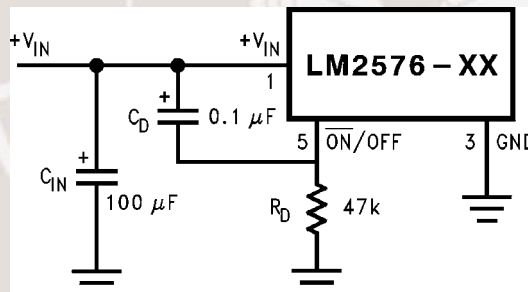
Figure 31. Undervoltage Lockout for Buck-Boost Circuit

DELAYED STARTUP

The $\overline{\text{ON}}/\text{OFF}$ pin can be used to provide a delayed startup feature as shown in [Figure 32](#). With an input voltage of 20V and for the part values shown, the circuit provides approximately 10 ms of delay time before the circuit begins switching. Increasing the RC time constant can provide longer delay times. But excessively large RC time constants can cause problems with input voltages that are high in 60 Hz or 120 Hz ripple, by coupling the ripple into the $\overline{\text{ON}}/\text{OFF}$ pin.

ADJUSTABLE OUTPUT, LOW-RIPPLE POWER SUPPLY

A 3A power supply that features an adjustable output voltage is shown in [Figure 33](#). An additional L-C filter that reduces the output ripple by a factor of 10 or more is included in this circuit.



Complete circuit not shown.

Figure 32. Delayed Startup

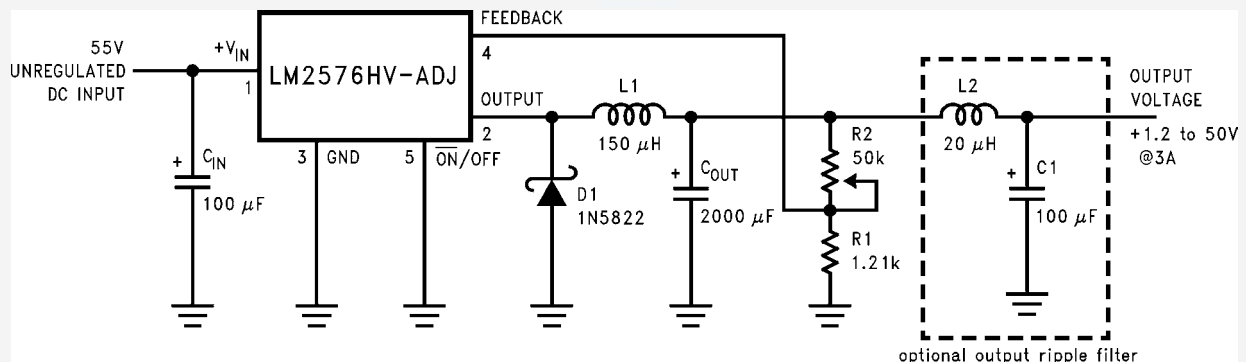


Figure 33. 1.2V to 55V Adjustable 3A Power Supply with Low Output Ripple

DEFINITION OF TERMS

BUCK REGULATOR A switching regulator topology in which a higher voltage is converted to a lower voltage. Also known as a step-down switching regulator.

BUCK-BOOST REGULATOR A switching regulator topology in which a positive voltage is converted to a negative voltage without a transformer.

DUTY CYCLE (D) Ratio of the output switch's on-time to the oscillator period.

$$\begin{aligned} \text{for buck regulator} \quad D &= \frac{t_{ON}}{T} = \frac{V_{OUT}}{V_{IN}} \\ \text{for buck-boost regulator} \quad D &= \frac{t_{ON}}{T} = \frac{|V_O|}{|V_O| + V_{IN}} \end{aligned} \quad (9)$$

CATCH DIODE OR CURRENT STEERING DIODE The diode which provides a return path for the load current when the LM2576 switch is OFF.

EFFICIENCY (η) The proportion of input power actually delivered to the load.

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \quad (10)$$

CAPACITOR EQUIVALENT SERIES RESISTANCE (ESR) The purely resistive component of a real capacitor's impedance (see [Figure 34](#)). It causes power loss resulting in capacitor heating, which directly affects the capacitor's operating lifetime. When used as a switching regulator output filter, higher ESR values result in higher output ripple voltages.



Figure 34. Simple Model of a Real Capacitor

Most standard aluminum electrolytic capacitors in the 100 μF –1000 μF range have 0.5 Ω to 0.1 Ω ESR. Higher-grade capacitors (“low-ESR”, “high-frequency”, or “low-inductance”) in the 100 μF –1000 μF range generally have ESR of less than 0.15 Ω .

EQUIVALENT SERIES INDUCTANCE (ESL) The pure inductance component of a capacitor (see [Figure 34](#)). The amount of inductance is determined to a large extent on the capacitor's construction. In a buck regulator, this unwanted inductance causes voltage spikes to appear on the output.

OUTPUT RIPPLE VOLTAGE The AC component of the switching regulator's output voltage. It is usually dominated by the output capacitor's ESR multiplied by the inductor's ripple current (ΔI_{IND}). The peak-to-peak value of this sawtooth ripple current can be determined by reading the [INDUCTOR RIPPLE CURRENT](#) section.

CAPACITOR RIPPLE CURRENT RMS value of the maximum allowable alternating current at which a capacitor can be operated continuously at a specified temperature.

STANDBY QUIESCENT CURRENT (I_{STBY}) Supply current required by the LM2576 when in the standby mode (ON /OFF pin is driven to TTL-high voltage, thus turning the output switch OFF).

INDUCTOR RIPPLE CURRENT (ΔI_{IND}) The peak-to-peak value of the inductor current waveform, typically a sawtooth waveform when the regulator is operating in the continuous mode (vs. discontinuous mode).

CONTINUOUS/DISCONTINUOUS MODE OPERATION Relates to the inductor current. In the continuous mode, the inductor current is always flowing and never drops to zero, vs. the discontinuous mode, where the inductor current drops to zero for a period of time in the normal switching cycle.

INDUCTOR SATURATION The condition which exists when an inductor cannot hold any more magnetic flux. When an inductor saturates, the inductor appears less inductive and the resistive component dominates. Inductor current is then limited only by the DC resistance of the wire and the available source current.

OPERATING VOLT MICROSECOND CONSTANT ($E \cdot T_{op}$) The product (in Volt $\cdot\mu\text{s}$) of the voltage applied to the inductor and the time the voltage is applied. This $E \cdot T_{op}$ constant is a measure of the energy handling capability of an inductor and is dependent upon the type of core, the core area, the number of turns, and the duty cycle.

Connection Diagrams

(XX indicates output voltage option.)

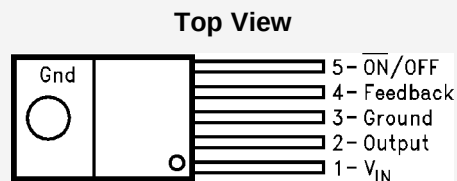


**Figure 35. Straight Leads
5-Lead TO-220 (T) Package
LM2576T-XX or LM2576HVT-XX
See Package Number KC0005A**

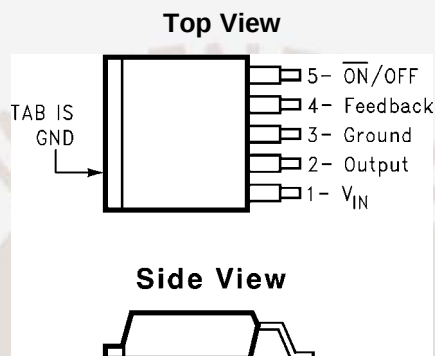


**Figure 36. DDPAK/TO-263 (S) Package
5-Lead Surface-Mount Package
LM2576S-XX or LM2576HVS-XX
See Package Number KTT0005B
LM2576SX-XX or LM2576HVSX-XX
See Package Number KTT0005B**

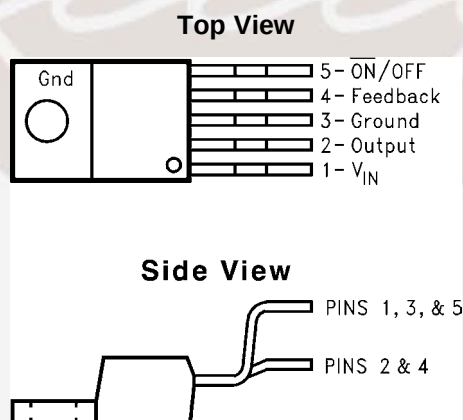


**Figure 37. Bent, Staggered Leads
5-Lead TO-220 (T) Package
LM2576T-XX Flow LB03
or LM2576HVT-XX Flow LB03
See Package Number NDH0005D**

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
Changed layout of National Data Sheet to TI format	24





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PACKAGE OPTION ADDENDUM

1-Nov-2015

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2576HVS-12	NRND	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LM2576 HVS-12 P+	
LM2576HVS-12/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2576 HVS-12 P+	Samples
LM2576HVS-3.3	NRND	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LM2576 HVS-3.3 P+	
LM2576HVS-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2576 HVS-3.3 P+	Samples
LM2576HVS-5.0	NRND	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LM2576 HVS-5.0 P+	
LM2576HVS-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2576 HVS-5.0 P+	Samples
LM2576HVS-ADJ	NRND	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LM2576 HVS-ADJ P+	
LM2576HVS-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2576 HVS-ADJ P+	Samples
LM2576HVSX-12	NRND	DDPAK/ TO-263	KTT	5	500	TBD	Call TI	Call TI	-40 to 125	LM2576 HVS-12 P+	
LM2576HVSX-12/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2576 HVS-12 P+	Samples
LM2576HVSX-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2576 HVS-3.3 P+	Samples
LM2576HVSX-5.0	NRND	DDPAK/ TO-263	KTT	5	500	TBD	Call TI	Call TI	-40 to 125	LM2576 HVS-5.0 P+	
LM2576HVSX-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2576 HVS-5.0 P+	Samples
LM2576HVSX-ADJ	NRND	DDPAK/ TO-263	KTT	5	500	TBD	Call TI	Call TI	-40 to 125	LM2576 HVS-ADJ P+	
LM2576HVSX-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2576 HVS-ADJ P+	Samples
LM2576HVT-12	NRND	TO-220	KC	5	45	TBD	Call TI	Call TI	-40 to 125	LM2576HVT -12 P+	
LM2576HVT-12/ILF03	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM2576HVT -12 P+	Samples



PACKAGE OPTION ADDENDUM

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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽⁶⁾	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking ^(4/5)	Samples
LM2576HVT-12/NOPB	ACTIVE	TO-220	KC	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2576HVT-12 P+	Samples
LM2576HVT-15	NRND	TO-220	KC	5	45	TBD	Call TI	Call TI	-40 to 125	LM2576HVT-15 P+	
LM2576HVT-15/LB03	NRND	TO-220	NDH	5	45	TBD	Call TI	Call TI		LM2576HVT-15 P+	
LM2576HVT-15/LF03	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM2576HVT-15 P+	Samples
LM2576HVT-15/NOPB	ACTIVE	TO-220	KC	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2576HVT-15 P+	Samples
LM2576HVT-5.0	NRND	TO-220	KC	5	45	TBD	Call TI	Call TI	-40 to 125	LM2576HVT-5.0 P+	
LM2576HVT-5.0/LB03	NRND	TO-220	NDH	5	45	TBD	Call TI	Call TI		LM2576HVT-5.0 P+	
LM2576HVT-5.0/LF02	ACTIVE	TO-220	NEB	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM2576HVT-5.0 P+	Samples
LM2576HVT-5.0/LF03	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM2576HVT-5.0 P+	Samples
LM2576HVT-5.0/NOPB	ACTIVE	TO-220	KC	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2576HVT-5.0 P+	Samples
LM2576HVT-ADJ	NRND	TO-220	KC	5	45	TBD	Call TI	Call TI	-40 to 125	LM2576HVT-ADJ P+	
LM2576HVT-ADJ/LB03	NRND	TO-220	NDH	5	45	TBD	Call TI	Call TI		LM2576HVT-ADJ P+	
LM2576HVT-ADJ/LF03	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM2576HVT-ADJ P+	Samples
LM2576HVT-ADJ/NOPB	ACTIVE	TO-220	KC	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2576HVT-ADJ P+	Samples
LM2576S-12	NRND	DDPAK/TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LM2576S-12 P+	
LM2576S-12/NOPB	ACTIVE	DDPAK/TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2576S-12 P+	Samples
LM2576S-3.3/NOPB	ACTIVE	DDPAK/TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2576S-3.3 P+	Samples
LM2576S-5.0	NRND	DDPAK/TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LM2576S-5.0 P+	



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Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽⁶⁾	MSL Peak Temp ⁽³⁾	Op Temp (°C)	Device Marking ^(4/5)	Samples
LM2576S-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2576S -5.0 P+	Samples
LM2576S-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2576S -ADJ P+	Samples
LM2576SX-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2576S -3.3 P+	Samples
LM2576SX-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2576S -5.0 P+	Samples
LM2576SX-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2576S -ADJ P+	Samples
LM2576T-12	NRND	TO-220	KC	5	45	TBD	Call TI	Call TI	-40 to 125	LM2576T -12 P+	
LM2576T-12/LB03	NRND	TO-220	NDH	5	45	TBD	Call TI	Call TI		LM2576T -12 P+	
LM2576T-12/LF03	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2576T -12 P+	Samples
LM2576T-12/NOPB	ACTIVE	TO-220	KC	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2576T -12 P+	Samples
LM2576T-15/LF03	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2576T -15 P+	Samples
LM2576T-15/NOPB	ACTIVE	TO-220	KC	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2576T -15 P+	Samples
LM2576T-3.3/LB03	NRND	TO-220	NDH	5		TBD	Call TI	Call TI		LM2576T -3.3 P+	
LM2576T-3.3/LF03	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM2576T -3.3 P+	Samples
LM2576T-3.3/NOPB	ACTIVE	TO-220	KC	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2576T -3.3 P+	Samples
LM2576T-5.0	NRND	TO-220	KC	5	45	TBD	Call TI	Call TI	-40 to 125	LM2576T -5.0 P+	
LM2576T-5.0/LB03	NRND	TO-220	NDH	5	45	TBD	Call TI	Call TI		LM2576T -5.0 P+	
LM2576T-5.0/LF02	ACTIVE	TO-220	NEB	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM2576T -5.0 P+	Samples
LM2576T-5.0/LF03	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM2576T -5.0 P+	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2576T-5.0/NOPB	ACTIVE	TO-220	KC	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2576T -5.0 P+	Samples
LM2576T-ADJ	NRND	TO-220	KC	5	45	TBD	Call TI	Call TI	-40 to 125	LM2576T -ADJ P+	
LM2576T-ADJ/LB03	NRND	TO-220	NDH	5	45	TBD	Call TI	Call TI		LM2576T -ADJ P+	
LM2576T-ADJ/LF02	ACTIVE	TO-220	NEB	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM2576T -ADJ P+	Samples
LM2576T-ADJ/LF03	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM2576T -ADJ P+	Samples
LM2576T-ADJ/NOPB	ACTIVE	TO-220	KC	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2576T -ADJ P+	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



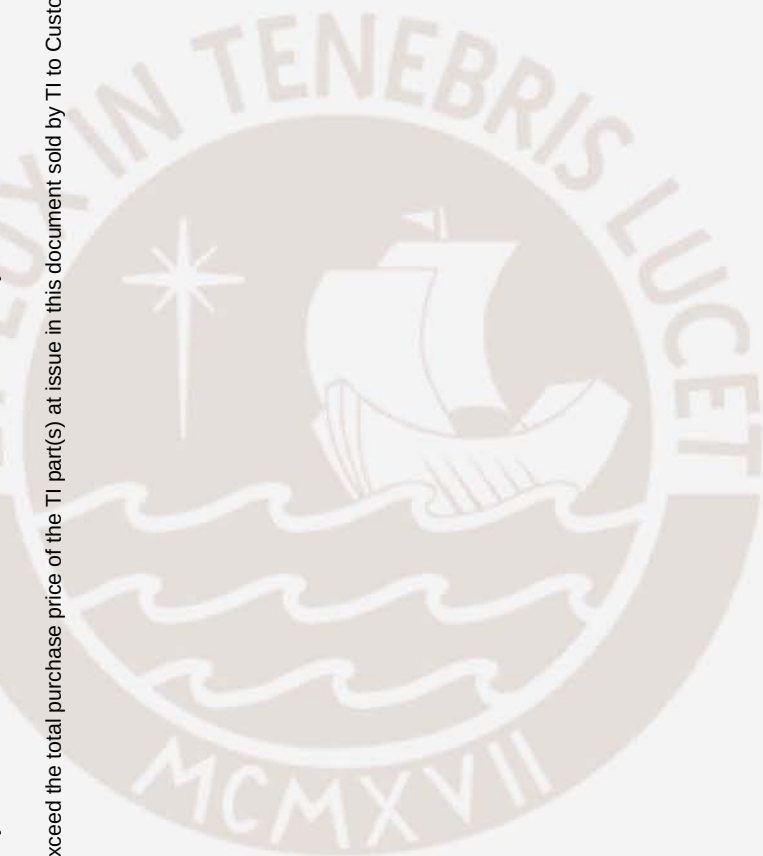
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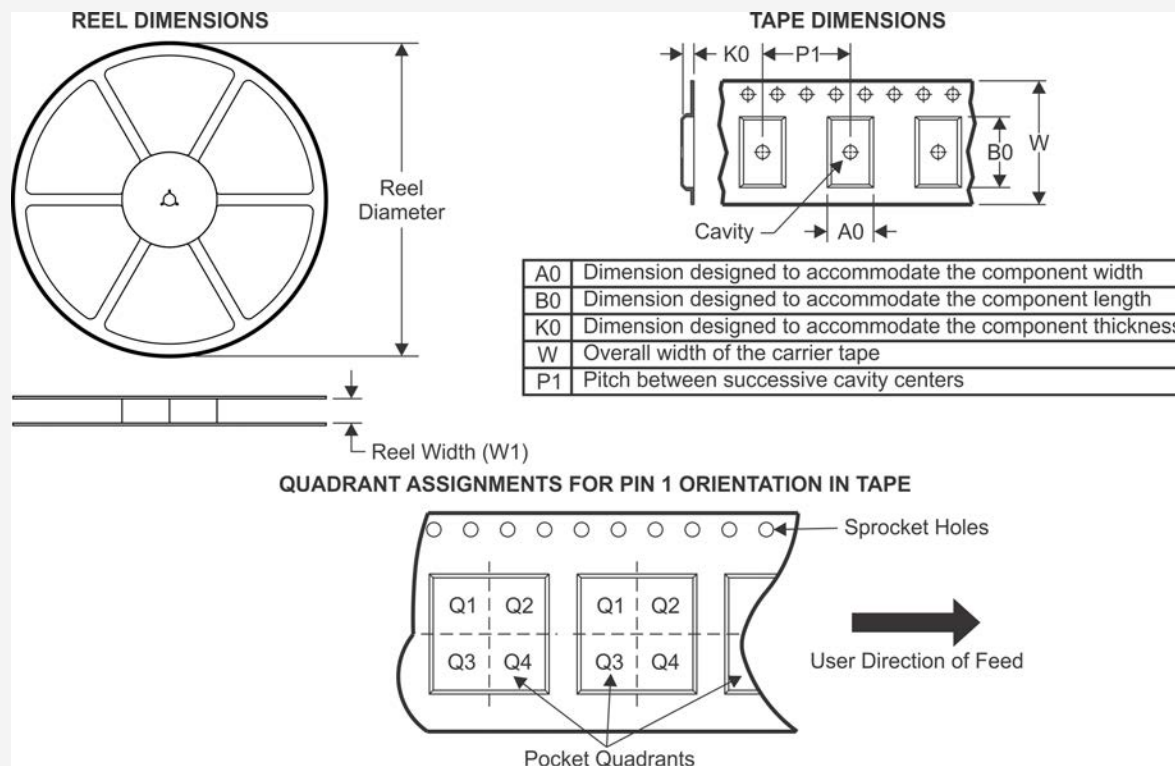
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(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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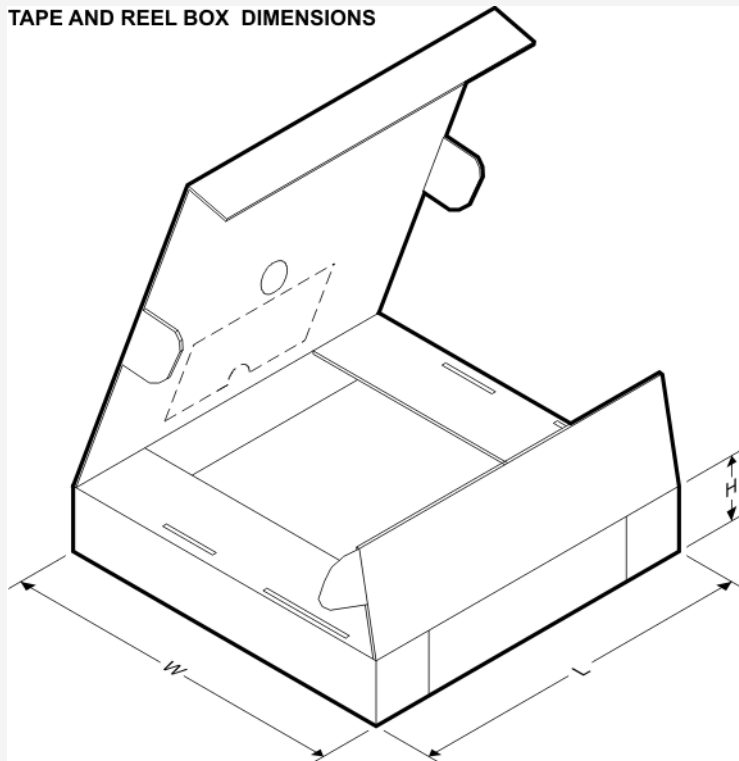


TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2576HVSX-12	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM2576HVSX-12/NOPB	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM2576HVSX-3.3/NOPB	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM2576HVSX-5.0	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM2576HVSX-5.0/NOPB	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM2576HVSX-ADJ	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM2576HVSX-ADJ/NOPB	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM2576SX-3.3/NOPB	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM2576SX-5.0/NOPB	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM2576SX-ADJ/NOPB	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

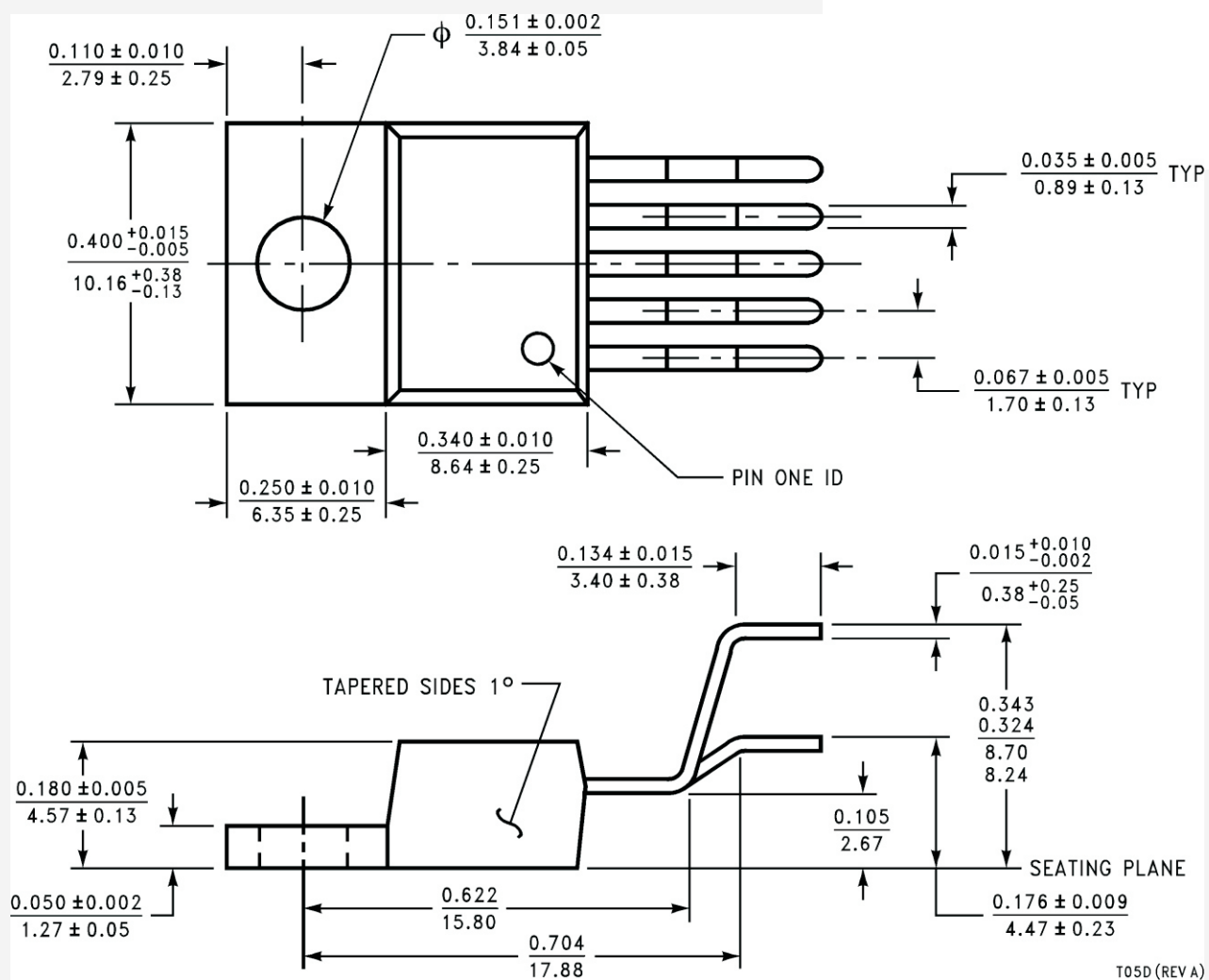
TAPE AND REEL BOX DIMENSIONS



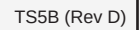
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2576HVSX-12	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LM2576HVSX-12/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LM2576HVSX-3.3/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LM2576HVSX-5.0	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LM2576HVSX-5.0/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LM2576HVSX-ADJ	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LM2576HVSX-ADJ/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LM2576SX-3.3/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LM2576SX-5.0/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LM2576SX-ADJ/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0

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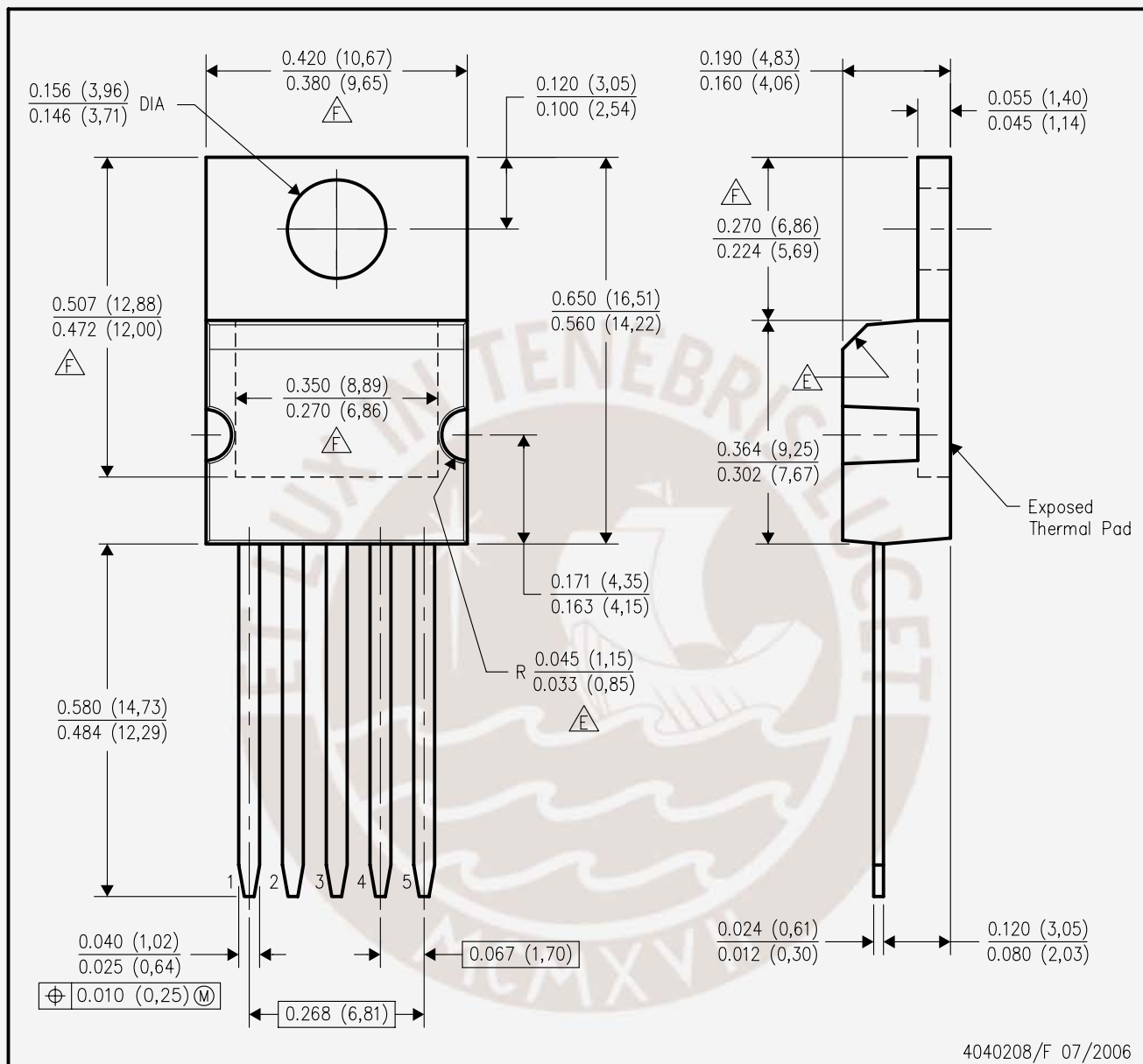
T05D (REV A)





KC (R-PSFM-T5)

PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. All lead dimensions apply before solder dip.
 - D. The center lead is in electrical contact with the mounting tab.
 - These features are optional.
 - Thermal pad contour optional within these dimensions.

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XBee[®] / XBee-PRO[®] RF Modules

XBee[®]/XBee-PRO[®] RF Modules

RF Module Operation

RF Module Configuration

Appendices



Product Manual v1.xEx - 802.15.4 Protocol

For RF Module Part Numbers: XB24-A...-001, XBP24-A...-001

IEEE[®] 802.15.4 RF Modules by Digi International



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<http://www.digi.com>

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1. XBee®/XBee-PRO® RF Modules

The XBee and XBee-PRO RF Modules were engineered to meet IEEE 802.15.4 standards and support the unique needs of low-cost, low-power wireless sensor networks. The modules require minimal power and provide reliable delivery of data between devices.

The modules operate within the ISM 2.4 GHz frequency band and are pin-for-pin compatible with each other.



Key Features

Long Range Data Integrity

XBee

- Indoor/Urban: up to 100' (30 m)
- Outdoor line-of-sight: up to 300' (90 m)
- Transmit Power: 1 mW (0 dBm)
- Receiver Sensitivity: -92 dBm

XBee-PRO

- Indoor/Urban: up to 300' (90 m), 200' (60 m) for International variant
- Outdoor line-of-sight: up to 1 mile (1600 m), 2500' (750 m) for International variant
- Transmit Power: 63mW (18dBm), 10mW (10dBm) for International variant
- Receiver Sensitivity: -100 dBm

RF Data Rate: 250,000 bps

Advanced Networking & Security

Retries and Acknowledgements
DSSS (Direct Sequence Spread Spectrum)
Each direct sequence channels has over 65,000 unique network addresses available
Source/Destination Addressing
Unicast & Broadcast Communications
Point-to-point, point-to-multipoint and peer-to-peer topologies supported

Low Power

XBee

- TX Peak Current: 45 mA (@3.3 V)
- RX Current: 50 mA (@3.3 V)
- Power-down Current: < 10 μ A

XBee-PRO

- TX Peak Current: 250mA (150mA for international variant)
- TX Peak Current (RPSMA module only): 340mA (180mA for international variant)
- RX Current: 55 mA (@3.3 V)
- Power-down Current: < 10 μ A

ADC and I/O line support

Analog-to-digital conversion, Digital I/O
I/O Line Passing

Easy-to-Use

No configuration necessary for out-of box RF communications
Free X-CTU Software (Testing and configuration software)
AT and API Command Modes for configuring module parameters
Extensive command set
Small form factor

Worldwide Acceptance

FCC Approval (USA) Refer to Appendix A [p64] for FCC Requirements.
Systems that contain XBee®/XBee-PRO® RF Modules inherit Digi Certifications.

ISM (Industrial, Scientific & Medical) **2.4 GHz frequency band**

Manufactured under **ISO 9001:2000** registered standards

XBee®/XBee-PRO® RF Modules are optimized for use in the United States, Canada, Australia, Japan, and Europe. Contact Digi for complete list of government agency approvals.



Specifications

Table 1-01. Specifications of the XBee®/XBee-PRO® RF Modules

Specification	XBee	XBee-PRO
Performance		
Indoor/Urban Range	Up to 100 ft (30 m)	Up to 300 ft. (90 m), up to 200 ft (60 m) International variant
Outdoor RF line-of-sight Range	Up to 300 ft (90 m)	Up to 1 mile (1600 m), up to 2500 ft (750 m) international variant
Transmit Power Output (software selectable)	1mW (0 dBm)	63mW (18dBm)* 10mW (10 dBm) for International variant
RF Data Rate	250,000 bps	250,000 bps
Serial Interface Data Rate (software selectable)	1200 bps - 250 kbps (non-standard baud rates also supported)	1200 bps - 250 kbps (non-standard baud rates also supported)
Receiver Sensitivity	-92 dBm (1% packet error rate)	-100 dBm (1% packet error rate)
Power Requirements		
Supply Voltage	2.8 – 3.4 V	2.8 – 3.4 V
Transmit Current (typical)	45mA (@ 3.3 V)	250mA (@3.3 V) (150mA for international variant) RPSMA module only: 340mA (@3.3 V) (180mA for international variant)
Idle / Receive Current (typical)	50mA (@ 3.3 V)	55mA (@ 3.3 V)
Power-down Current	< 10 μ A	< 10 μ A
General		
Operating Frequency	ISM 2.4 GHz	ISM 2.4 GHz
Dimensions	0.960" x 1.087" (2.438cm x 2.761cm)	0.960" x 1.297" (2.438cm x 3.294cm)
Operating Temperature	-40 to 85° C (industrial)	-40 to 85° C (industrial)
Antenna Options	Integrated Whip, Chip or U.FL Connector, RPSMA Connector	Integrated Whip, Chip or U.FL Connector, RPSMA Connector
Networking & Security		
Supported Network Topologies	Point-to-point, Point-to-multipoint & Peer-to-peer	
Number of Channels (software selectable)	16 Direct Sequence Channels	12 Direct Sequence Channels
Addressing Options	PAN ID, Channel and Addresses	PAN ID, Channel and Addresses
Agency Approvals		
United States (FCC Part 15.247)	OUR-XBEE	OUR-XBEEPRO
Industry Canada (IC)	4214A XBEE	4214A XBEEPRO
Europe (CE)	ETSI	ETSI (Max. 10 dBm transmit power output)*
Japan	R201WW07215214	R201WW08215111 (Max. 10 dBm transmit power output)*
Australia	C-Tick	C-Tick

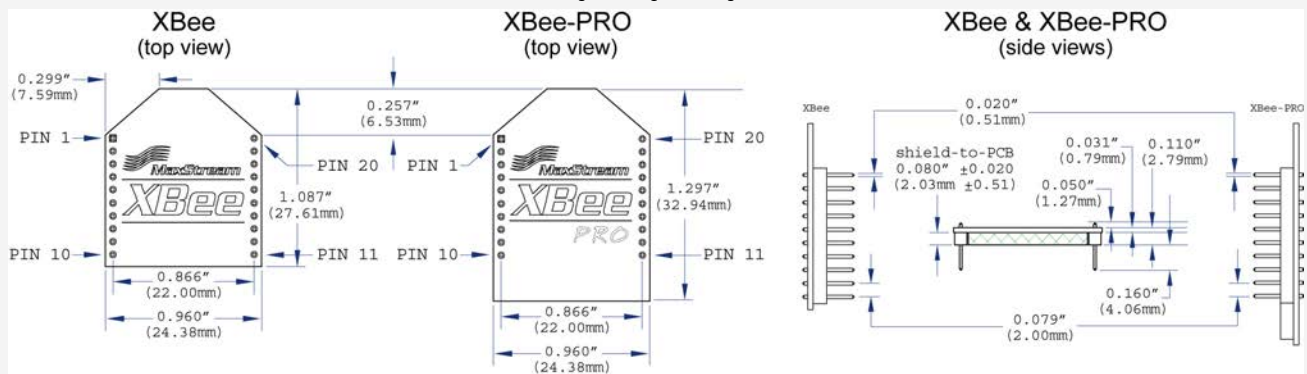
* See Appendix A for region-specific certification requirements.

Antenna Options: The ranges specified are typical when using the integrated Whip (1.5 dBi) and Dipole (2.1 dBi) antennas. The Chip antenna option provides advantages in its form factor; however, it typically yields shorter range than the Whip and Dipole antenna options when transmitting outdoors. For more information, refer to the "XBee Antennas" Knowledgebase Article located on Digi's Support Web site

Mechanical Drawings

Figure 1-01. Mechanical drawings of the XBee®/XBee-PRO® RF Modules (antenna options not shown)

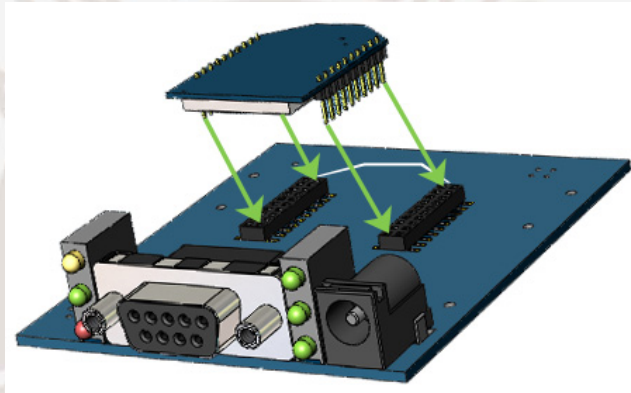
The XBee and XBee-PRO RF Modules are pin-for-pin compatible.



Mounting Considerations

The XBee®/XBee-PRO® RF Module was designed to mount into a receptacle (socket) and therefore does not require any soldering when mounting it to a board. The XBee Development Kits contain RS-232 and USB interface boards which use two 20-pin receptacles to receive modules.

Figure 1-02. XBee Module Mounting to an RS-232 Interface Board.



The receptacles used on Digi development boards are manufactured by Century Interconnect. Several other manufacturers provide comparable mounting solutions; however, Digi currently uses the following receptacles:

- Through-hole single-row receptacles -
Samtec P/N: MMS-110-01-L-SV (or equivalent)
- Surface-mount double-row receptacles -
Century Interconnect P/N: CPRMSL20-D-0-1 (or equivalent)
- Surface-mount single-row receptacles -
Samtec P/N: SMM-110-02-SM-S

Digi also recommends printing an outline of the module on the board to indicate the orientation the module should be mounted.

Pin Signals

Figure 1-03. XBee®/XBee-PRO® RF Module Pin Numbers

(top sides shown - shields on bottom)

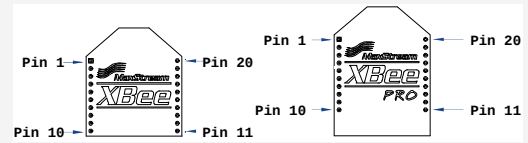


Table 1-02. Pin Assignments for the XBee and XBee-PRO Modules

(Low-asserted signals are distinguished with a horizontal line above signal name.)

Pin #	Name	Direction	Description
1	VCC	-	Power supply
2	DOUT	Output	UART Data Out
3	DIN / <u>CONFIG</u>	Input	UART Data In
4	DO8*	Output	Digital Output 8
5	<u>RESET</u>	Input	Module Reset (reset pulse must be at least 200 ns)
6	PWM0 / RSSI	Output	PWM Output 0 / RX Signal Strength Indicator
7	PWM1	Output	PWM Output 1
8	[reserved]	-	Do not connect
9	<u>DTR</u> / <u>SLEEP_RQ</u> / DI8	Input	Pin Sleep Control Line or Digital Input 8
10	GND	-	Ground
11	AD4 / DIO4	Either	Analog Input 4 or Digital I/O 4
12	<u>CTS</u> / DIO7	Either	Clear-to-Send Flow Control or Digital I/O 7
13	ON / <u>SLEEP</u>	Output	Module Status Indicator
14	VREF	Input	Voltage Reference for A/D Inputs
15	Associate / AD5 / DIO5	Either	Associated Indicator, Analog Input 5 or Digital I/O 5
16	RTS / AD6 / DIO6	Either	Request-to-Send Flow Control, Analog Input 6 or Digital I/O 6
17	AD3 / DIO3	Either	Analog Input 3 or Digital I/O 3
18	AD2 / DIO2	Either	Analog Input 2 or Digital I/O 2
19	AD1 / DIO1	Either	Analog Input 1 or Digital I/O 1
20	AD0 / DIO0	Either	Analog Input 0 or Digital I/O 0

* Function is not supported at the time of this release

Design Notes:

- Minimum connections: VCC, GND, DOUT & DIN
- Minimum connections for updating firmware: VCC, GND, DIN, DOUT, RTS & DTR
- Signal Direction is specified with respect to the module
- Module includes a 50k Ω pull-up resistor attached to RESET
- Several of the input pull-ups can be configured using the PR command
- Unused pins should be left disconnected

Electrical Characteristics

Table 1-03. DC Characteristics (VCC = 2.8 - 3.4 VDC)

Symbol	Characteristic	Condition	Min	Typical	Max	Unit
V _{IL}	Input Low Voltage	All Digital Inputs	-	-	0.35 * VCC	V
V _{IH}	Input High Voltage	All Digital Inputs	0.7 * VCC	-	-	V
V _{OL}	Output Low Voltage	I _{OL} = 2 mA, VCC ≥ 2.7 V	-	-	0.5	V
V _{OH}	Output High Voltage	I _{OH} = -2 mA, VCC ≥ 2.7 V	VCC - 0.5	-	-	V
I _{IN}	Input Leakage Current	V _{IN} = VCC or GND, all inputs, per pin	-	0.025	1	μA
I _{OZ}	High Impedance Leakage Current	V _{IN} = VCC or GND, all I/O High-Z, per pin	-	0.025	1	μA
TX	Transmit Current	VCC = 3.3 V	-	45 (XBee) 215, 140 (PRO, Int)	-	mA
RX	Receive Current	VCC = 3.3 V	-	50 (XBee) 55 (PRO)	-	mA
PWR-DWN	Power-down Current	SM parameter = 1	-	< 10	-	μA

Table 1-04. ADC Characteristics (Operating)

Symbol	Characteristic	Condition	Min	Typical	Max	Unit
V _{REFH}	VREF - Analog-to-Digital converter reference range		2.08	-	V _{DDAD} *	V
I _{REF}	VREF - Reference Supply Current	Enabled	-	200	-	μA
		Disabled or Sleep Mode	-	< 0.01	0.02	μA
V _{INDC}	Analog Input Voltage ¹		V _{SSAD} - 0.3	-	V _{DDAD} + 0.3	V

1. Maximum electrical operating range, not valid conversion range.

* V_{DDAD} is connected to VCC.

Table 1-05. ADC Timing/Performance Characteristics¹

Symbol	Characteristic	Condition	Min	Typical	Max	Unit
R _{AS}	Source Impedance at Input ²		-	-	10	kΩ
V _{AIN}	Analog Input Voltage ³		V _{REFL}		V _{REFH}	V
RES	Ideal Resolution (1 LSB) ⁴	2.08V ≤ V _{DDAD} ≤ 3.6V	2.031	-	3.516	mV
DNL	Differential Non-linearity ⁵		-	±0.5	±1.0	LSB
INL	Integral Non-linearity ⁶		-	±0.5	±1.0	LSB
E _{ZS}	Zero-scale Error ⁷		-	±0.4	±1.0	LSB
F _{FS}	Full-scale Error ⁸		-	±0.4	±1.0	LSB
E _{IL}	Input Leakage Error ⁹		-	±0.05	±5.0	LSB
E _{TU}	Total Unadjusted Error ¹⁰		-	±1.1	±2.5	LSB

1. All ACCURACY numbers are based on processor and system being in WAIT state (very little activity and no IO switching) and that adequate low-pass filtering is present on analog input pins (filter with 0.01 μF to 0.1 μF capacitor between analog input and VREFL). Failure to observe these guidelines may result in system or microcontroller noise causing accuracy errors which will vary based on board layout and the type and magnitude of the activity.

Data transmission and reception during data conversion may cause some degradation of these specifications, depending on the number and timing of packets. It is advisable to test the ADCs in your installation if best accuracy is required.

2. R_{AS} is the real portion of the impedance of the network driving the analog input pin. Values greater than this amount may not fully charge the input circuitry of the ATD resulting in accuracy error.

3. Analog input must be between V_{REFL} and V_{REFH} for valid conversion. Values greater than V_{REFH} will convert to \$3FF.

4. The resolution is the ideal step size or 1LSB = (V_{REFH} - V_{REFL})/1024

5. Differential non-linearity is the difference between the current code width and the ideal code width (1LSB). The current code width is the difference in the transition voltages to and from the current code.

6. Integral non-linearity is the difference between the transition voltage to the current code and the adjusted ideal transition voltage for the current code. The adjusted ideal transition voltage is (Current Code - 1/2) * (1 / ((V_{REFH} + E_{FS}) - (V_{REFL} + E_{ZS}))).

7. Zero-scale error is the difference between the transition to the first valid code and the ideal transition to that code. The Ideal transition voltage to a given code is (Code - 1/2) * (1 / (V_{REFH} - V_{REFL})).

8. Full-scale error is the difference between the transition to the last valid code and the ideal transition to that code. The ideal transition voltage to a given code is (Code - 1/2) * (1 / (V_{REFH} - V_{REFL})).

9. Input leakage error is error due to input leakage across the real portion of the impedance of the network driving the analog pin. Reducing the impedance of the network reduces this error.

10. Total unadjusted error is the difference between the transition voltage to the current code and the ideal straight-line transfer function. This measure of error includes inherent quantization error (1/2LSB) and circuit error (differential, integral, zero-scale, and full-scale) error. The specified value of E_{TU} assumes zero E_{IL} (no leakage or zero real source impedance).



2. RF Module Operation

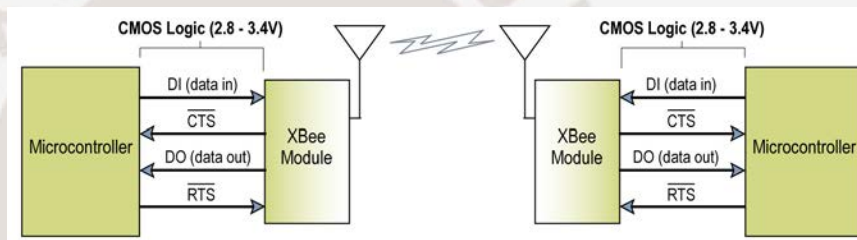
Serial Communications

The XBee®/XBee-PRO® RF Modules interface to a host device through a logic-level asynchronous serial port. Through its serial port, the module can communicate with any logic and voltage compatible UART; or through a level translator to any serial device (For example: Through a Digi proprietary RS-232 or USB interface board).

UART Data Flow

Devices that have a UART interface can connect directly to the pins of the RF module as shown in the figure below.

Figure 2-01. System Data Flow Diagram in a UART-interfaced environment
(Low-asserted signals distinguished with horizontal line over signal name.)

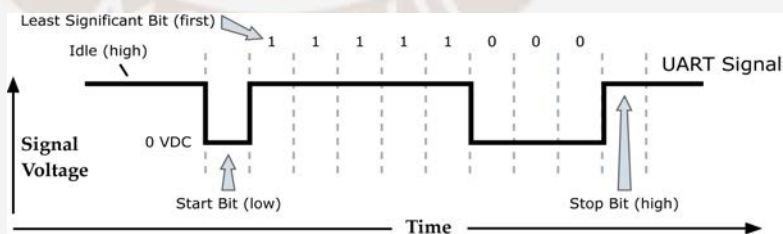


Serial Data

Data enters the module UART through the DI pin (pin 3) as an asynchronous serial signal. The signal should idle high when no data is being transmitted.

Each data byte consists of a start bit (low), 8 data bits (least significant bit first) and a stop bit (high). The following figure illustrates the serial bit pattern of data passing through the module.

Figure 2-02. UART data packet 0x1F (decimal number "31") as transmitted through the RF module
Example Data Format is 8-N-1 (bits - parity - # of stop bits)



Serial communications depend on the two UARTs (the microcontroller's and the RF module's) to be configured with compatible settings (baud rate, parity, start bits, stop bits, data bits).

The UART baud rate and parity settings on the XBee module can be configured with the BD and SB commands, respectively. See the command table in Chapter 3 for details.

Transparent Operation

By default, XBee®/XBee-PRO® RF Modules operate in Transparent Mode. When operating in this mode, the modules act as a serial line replacement - all UART data received through the DI pin is queued up for RF transmission. When RF data is received, the data is sent out the DO pin.

Serial-to-RF Packetization

Data is buffered in the DI buffer until one of the following causes the data to be packetized and transmitted:

1. No serial characters are received for the amount of time determined by the RO (Packetization Timeout) parameter. If RO = 0, packetization begins when a character is received.
2. The maximum number of characters that will fit in an RF packet (100) is received.
3. The Command Mode Sequence (GT + CC + GT) is received. Any character buffered in the DI buffer before the sequence is transmitted.

If the module cannot immediately transmit (for instance, if it is already receiving RF data), the serial data is stored in the DI Buffer. The data is packetized and sent at any RO timeout or when 100 bytes (maximum packet size) are received.

If the DI buffer becomes full, hardware or software flow control must be implemented in order to prevent overflow (loss of data between the host and module).

API Operation

API (Application Programming Interface) Operation is an alternative to the default Transparent Operation. The frame-based API extends the level to which a host application can interact with the networking capabilities of the module.

When in API mode, all data entering and leaving the module is contained in frames that define operations or events within the module.

Transmit Data Frames (received through the DI pin (pin 3)) include:

- RF Transmit Data Frame
- Command Frame (equivalent to AT commands)

Receive Data Frames (sent out the DO pin (pin 2)) include:

- RF-received data frame
- Command response
- Event notifications such as reset, associate, disassociate, etc.

The API provides alternative means of configuring modules and routing data at the host application layer. A host application can send data frames to the module that contain address and payload information instead of using command mode to modify addresses. The module will send data frames to the application containing status packets; as well as source, RSSI and payload information from received data packets.

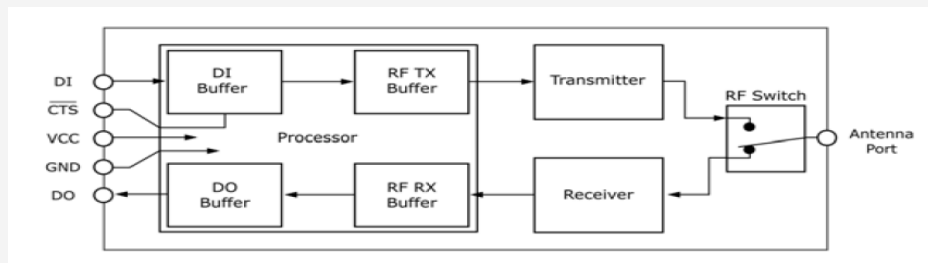
The API operation option facilitates many operations such as the examples cited below:

- > Transmitting data to multiple destinations without entering Command Mode
- > Receive success/failure status of each transmitted RF packet
- > Identify the source address of each received packet

To implement API operations, refer to API sections [p57].

Flow Control

Figure 2-03. Internal Data Flow Diagram



DI (Data In) Buffer

When serial data enters the RF module through the DI pin (pin 3), the data is stored in the DI Buffer until it can be processed.

Hardware Flow Control ($\overline{\text{CTS}}$). When the DI buffer is 17 bytes away from being full; by default, the module de-asserts $\overline{\text{CTS}}$ (high) to signal to the host device to stop sending data [refer to D7 (DIO7 Configuration) parameter]. $\overline{\text{CTS}}$ is re-asserted after the DI Buffer has 34 bytes of memory available.

How to eliminate the need for flow control:

1. Send messages that are smaller than the DI buffer size (202 bytes).
2. Interface at a lower baud rate [BD (Interface Data Rate) parameter] than the throughput data rate.

Case in which the DI Buffer may become full and possibly overflow:

If the module is receiving a continuous stream of RF data, any serial data that arrives on the DI pin is placed in the DI Buffer. The data in the DI buffer will be transmitted over-the-air when the module is no longer receiving RF data in the network.

Refer to the RO (Packetization Timeout), BD (Interface Data Rate) and D7 (DIO7 Configuration) command descriptions for more information.

DO (Data Out) Buffer

When RF data is received, the data enters the DO buffer and is sent out the serial port to a host device. Once the DO Buffer reaches capacity, any additional incoming RF data is lost.

Hardware Flow Control ($\overline{\text{RTS}}$). If $\overline{\text{RTS}}$ is enabled for flow control (D6 (DIO6 Configuration) Parameter = 1), data will not be sent out the DO Buffer as long as $\overline{\text{RTS}}$ (pin 16) is de-asserted.

Two cases in which the DO Buffer may become full and possibly overflow:

1. If the RF data rate is set higher than the interface data rate of the module, the module will receive data from the transmitting module faster than it can send the data to the host.
2. If the host does not allow the module to transmit data out from the DO buffer because of being held off by hardware or software flow control.

Refer to the D6 (DIO6 Configuration) command description for more information.

ADC and Digital I/O Line Support

The XBees®/XBee-PRO® RF Modules support ADC (Analog-to-digital conversion) and digital I/O line passing. The following pins support multiple functions:

Table 2-01. Pin functions and their associated pin numbers and commands

AD = Analog-to-Digital Converter, DIO = Digital Input/Output

Pin functions not applicable to this section are denoted within (parenthesis).

Pin Function	Pin#	AT Command
AD0 / DIO0	20	D0
AD1 / DIO1	19	D1
AD2 / DIO2	18	D2
AD3 / DIO3 / (COORD_SEL)	17	D3
AD4 / DIO4	11	D4
AD5 / DIO5 / (ASSOCIATE)	15	D5
DIO6 / (RTS)	16	D6
DIO7 / (CTS)	12	D7
DIO8 / (DTR) / (Sleep_RQ)	9	D8

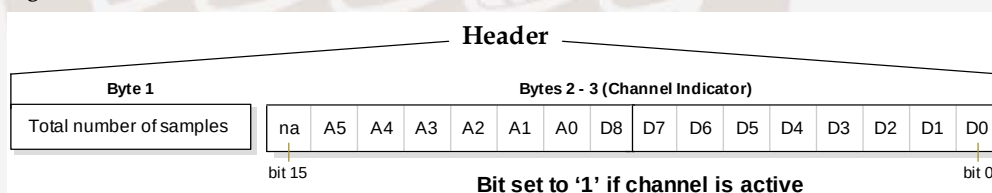
To enable ADC and DIO pin functions:

For ADC Support:	Set ATDn = 2
For Digital Input support:	Set ATDn = 3
For Digital Output Low support:	Set ATDn = 4
For Digital Output High support:	Set ATDn = 5

I/O Data Format

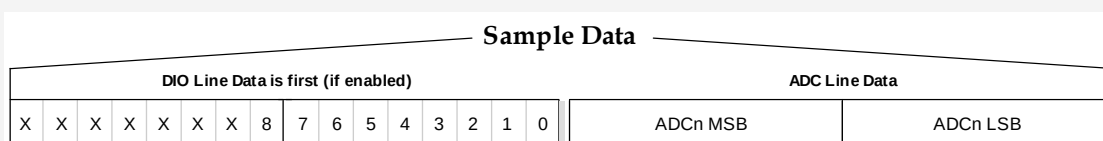
I/O data begins with a header. The first byte of the header defines the number of samples forthcoming. The last 2 bytes of the header (Channel Indicator) define which inputs are active. Each bit represents either a DIO line or ADC channel.

Figure 2-04. Header



Sample data follows the header and the channel indicator frame is used to determine how to read the sample data. If any of the DIO lines are enabled, the first 2 bytes are the DIO sample. The ADC data follows. ADC channel data is represented as an unsigned 10-bit value right-justified on a 16-bit boundary.

Figure 2-05. Sample Data



API Support

I/O data is sent out the UART using an API frame. All other data can be sent and received using Transparent Operation [refer to p11] or API framing if API mode is enabled (AP > 0).

API Operations support two RX (Receive) frame identifiers for I/O data (set 16-bit address to 0xFFFE and the module will do 64-bit addressing):

- 0x82 for RX (Receive) Packet: 64-bit address I/O
- 0x83 for RX (Receive) Packet: 16-bit address I/O

The API command header is the same as shown in the “RX (Receive) Packet: 64-bit Address” and “RX (Receive) Packet: 16-bit Address” API types [refer to p63]. RX data follows the format described in the I/O Data Format section [p13].

Applicable Commands: AP (API Enable)

Sleep Support

Automatic wakeup sampling can be suppressed by setting SO bit 1. When an RF module wakes, it will always do a sample based on any active ADC or DIO lines. This allows sampling based on the sleep cycle whether it be Cyclic Sleep (SM parameter = 4 or 5) or Pin Sleep (SM = 1 or 2). To gather more samples when awake, set the IR (Sample Rate) parameter.

For Cyclic Sleep modes: If the IR parameter is set, the module will stay awake until the IT (Samples before TX) parameter is met. The module will stay awake for ST (Time before Sleep) time.

Applicable Commands: IR (Sample Rate), IT (Samples before TX), SM (Sleep Mode), IC (DIO Change Detect), SO (Sleep Options)

DIO Pin Change Detect

When “DIO Change Detect” is enabled (using the IC command), DIO lines 0-7 are monitored. When a change is detected on a DIO line, the following will occur:

1. An RF packet is sent with the updated DIO pin levels. This packet will not contain any ADC samples.
2. Any queued samples are transmitted before the change detect data. This may result in receiving a packet with less than IT (Samples before TX) samples.

Note: Change detect will not affect Pin Sleep wake-up. The D8 pin (DTR/Sleep_RQ/DI8) is the only line that will wake a module from Pin Sleep. If not all samples are collected, the module will still enter Sleep Mode after a change detect packet is sent.

Applicable Commands: IC (DIO Change Detect), IT (Samples before TX)

NOTE: Change detect is only supported when the Dx (DIOx Configuration) parameter equals 3, 4 or 5.

Sample Rate (Interval)

The Sample Rate (Interval) feature allows enabled ADC and DIO pins to be read periodically on modules that are not configured to operate in Sleep Mode. When one of the Sleep Modes is enabled and the IR (Sample Rate) parameter is set, the module will stay awake until IT (Samples before TX) samples have been collected.

Once a particular pin is enabled, the appropriate sample rate must be chosen. The maximum sample rate that can be achieved while using one A/D line is 1 sample/ms or 1 KHz (Note that the modem will not be able to keep up with transmission when IR & IT are equal to “1” and that configuring the modem to sample at rates greater than once every 20ms is not recommended).

Applicable Commands: IR (Sample Rate), IT (Samples before TX), SM (Sleep Mode)

I/O Line Passing

Virtual wires can be set up between XBee®/XBee-PRO® Modules. When an RF data packet is received that contains I/O data, the receiving module can be setup to update any enabled outputs (PWM and DIO) based on the data it receives.

Note that I/O lines are mapped in pairs. For example: AD0 can only update PWM0 and DI5 can only update DO5. The default setup is for outputs not to be updated, which results in the I/O data being sent out the UART (refer to the IU (Enable I/O Output) command). To enable the outputs to be updated, the IA (I/O Input Address) parameter must be setup with the address of the module that has the appropriate inputs enabled. This effectively binds the outputs to a particular module's input. This does not affect the ability of the module to receive I/O line data from other modules - only its ability to update enabled outputs. The IA parameter can also be setup to accept I/O data for output changes from any module by setting the IA parameter to 0xFFFF.

When outputs are changed from their non-active state, the module can be setup to return the output level to its non-active state. The timers are set using the Tn (Dn Output Timer) and PT (PWM Output Timeout) commands. The timers are reset every time a valid I/O packet (passed IA check) is received. The IC (Change Detect) and IR (Sample Rate) parameters can be setup to keep the output set to their active output if the system needs more time than the timers can handle.

Note: DI8 cannot be used for I/O line passing.

Applicable Commands: IA (I/O Input Address), Tn (Dn Output Timeout), P0 (PWM0 Configuration), P1 (PWM1 Configuration), M0 (PWM0 Output Level), M1 (PWM1 Output Level), PT (PWM Output Timeout), RP (RSSI PWM Timer)

Configuration Example

As an example for a simple A/D link, a pair of RF modules could be set as follows:

Remote Configuration

DL = 0x1234
MY = 0x5678
D0 = 2
D1 = 2
IR = 0x14
IT = 5

Base Configuration

DL = 0x5678
MY = 0x1234
P0 = 2
P1 = 2
IU = 1
IA = 0x5678 (or 0xFFFF)

These settings configure the remote module to sample AD0 and AD1 once each every 20 ms. It then buffers 5 samples each before sending them back to the base module. The base should then receive a 32-Byte transmission (20 Bytes data and 12 Bytes framing) every 100 ms.

XBee® / XBee-PRO® Networks

The following terms will be used to explicate the network operations:

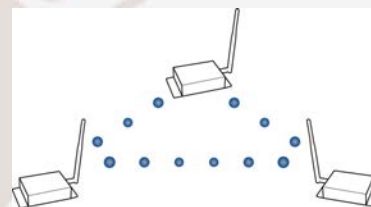
Table 2-02. Terms and definitions

Term	Definition
PAN	Personal Area Network - A data communication network that includes one or more End Devices and optionally a Coordinator.
Coordinator	A Full-function device (FFD) that provides network synchronization by polling nodes [NonBeacon (w/ Coordinator) networks only]
End Device	<i>When in the same network as a Coordinator</i> - RF modules that rely on a Coordinator for synchronization and can be put into states of sleep for low-power applications.
Association	The establishment of membership between End Devices and a Coordinator. Association is only applicable in NonBeacon (w/Coordinator) networks.

Peer-to-Peer

By default, XBee®/XBee-PRO RF Modules are configured to operate within a Peer-to-Peer network topology and therefore are not dependent upon Master/Slave relationships. NonBeacon systems operate within a Peer-to-Peer network topology and therefore are not dependent upon Master/Slave relationships. This means that modules remain synchronized without use of master/server configurations and each module in the network shares both roles of master and slave. Digi's peer-to-peer architecture features fast synchronization times and fast cold start times. This default configuration accommodates a wide range of RF data applications.

Figure 2-06. Peer-to-Peer Architecture



A peer-to-peer network can be established by configuring each module to operate as an End Device (CE = 0), disabling End Device Association on all modules (A1 = 0) and setting ID and CH parameters to be identical across the network.

NonBeacon (w / Coordinator)

A device is configured as a Coordinator by setting the CE (Coordinator Enable) parameter to "1". Coordinator power-up is governed by the A2 (Coordinator Association) parameter.

In a Coordinator system, the Coordinator can be configured to use direct or indirect transmissions. If the SP (Cyclic Sleep Period) parameter is set to "0", the Coordinator will send data immediately. Otherwise, the SP parameter determines the length of time the Coordinator will retain the data before discarding it. Generally, SP (Cyclic Sleep Period) and ST (Time before Sleep) parameters should be set to match the SP and ST settings of the End Devices.

Association

Association is the establishment of membership between End Devices and a Coordinator. The establishment of membership is useful in scenarios that require a central unit (Coordinator) to relay messages to or gather data from several remote units (End Devices), assign channels or assign PAN IDs.

An RF data network that consists of one Coordinator and one or more End Devices forms a PAN (Personal Area Network). Each device in a PAN has a PAN Identifier [ID (PAN ID) parameter]. PAN IDs must be unique to prevent miscommunication between PANs. The Coordinator PAN ID is set using the ID (PAN ID) and A2 (Coordinator Association) commands.

An End Device can associate to a Coordinator without knowing the address, PAN ID or channel of the Coordinator. The A1 (End Device Association) parameter bit fields determine the flexibility of an End Device during association. The A1 parameter can be used for an End Device to dynamically set its destination address, PAN ID and/or channel.

For example: If the PAN ID of a Coordinator is known, but the operating channel is not; the A1 command on the End Device should be set to enable the 'Auto_Associate' and 'Reassign_Channel' bits. Additionally, the ID parameter should be set to match the PAN ID of the associated Coordinator.

Coordinator / End Device Setup and Operation

To configure a module to operate as a Coordinator, set the CE (Coordinator Enable) parameter to '1'. Set the CE parameter of End Devices to '0' (default). Coordinator and End Devices should contain matching firmware versions.

NonBeacon (w/ Coordinator) Systems

The Coordinator can be configured to use direct or indirect transmissions. If the SP (Cyclic Sleep Period) parameter is set to '0', the Coordinator will send data immediately. Otherwise, the SP parameter determines the length of time the Coordinator will retain the data before discarding it. Generally, SP (Cyclic Sleep Period) and ST (Time before Sleep) parameters should be set to match the SP and ST settings of the End Devices.

Coordinator Start-up

Coordinator power-up is governed by the A2 (Coordinator Association) command. On power-up, the Coordinator undergoes the following sequence of events:

1. Check A2 parameter- Reassign_PANID Flag

Set (bit 0 = 1) - The Coordinator issues an Active Scan. The Active Scan selects one channel and transmits a request to the broadcast address (0xFFFF) and broadcast PAN ID (0xFFFF). It then listens on that channel for beacons from any Coordinator operating on that channel. The listen time on each channel is determined by the SD (Scan Duration) parameter value.

Once the time expires on that channel, the Active Scan selects another channel and again transmits the BeaconRequest as before. This process continues until all channels have been scanned, or until 5 PANs have been discovered. When the Active Scan is complete, the results include a list of PAN IDs and Channels that are being used by other PANs. This list is used to assign an unique PAN ID to the new Coordinator. The ID parameter will be retained if it is not found in the Active Scan results. Otherwise, the ID (PAN ID) parameter setting will be updated to a PAN ID that was not detected.

Not Set (bit 0 = 0) - The Coordinator retains its ID setting. No Active Scan is performed.

2. Check A2 parameter - Reassign_Channel Flag (bit 1)

Set (bit 1 = 1) - The Coordinator issues an Energy Scan. The Energy Scan selects one channel and scans for energy on that channel. The duration of the scan is specified by the SD (Scan Duration) parameter. Once the scan is completed on a channel, the Energy Scan selects the next channel and begins a new scan on that channel. This process continues until all channels have been scanned.

When the Energy Scan is complete, the results include the maximal energy values detected on each channel. This list is used to determine a channel where the least energy was detected. If an Active Scan was performed (Reassign_PANID Flag set), the channels used by the detected PANs are eliminated as possible channels. Thus, the results of the Energy Scan and the Active Scan (if performed) are used to find the best channel (channel with the least energy that is not used by any detected PAN). Once the best channel has been selected, the CH (Channel) parameter value is updated to that channel.

Not Set (bit 1 = 0) - The Coordinator retains its CH setting. An Energy Scan is not performed.

3. Start Coordinator

The Coordinator starts on the specified channel (CH parameter) and PAN ID (ID parameter). Note, these may be selected in steps 1 and/or 2 above. The Coordinator will only allow End Devices to associate to it if the A2 parameter "AllowAssociation" flag is set. Once the Coordinator has successfully started, the Associate LED will blink 1 time per second. (The LED is solid if the Coordinator has not started.)

4. Coordinator Modifications

Once a Coordinator has started:

Modifying the A2 (Reassign_Channel or Reassign_PANID bits), ID, CH or MY parameters will cause the Coordinator's MAC to reset (The Coordinator RF module (including volatile RAM) is not reset). Changing the A2 AllowAssociation bit will not reset the Coordinator's MAC. In a non-beaconing system, End Devices that associated to the Coordinator prior to a MAC reset will have knowledge of the new settings on the Coordinator. Thus, if the Coordinator were to change its ID, CH or MY settings, the End Devices would no longer be able to communicate with the non-beacon Coordinator. Once a Coordinator has started, the ID, CH, MY or A2 (Reassign_Channel or Reassign_PANID bits) should not be changed.

End Device Start-up

End Device power-up is governed by the A1 (End Device Association) command. On power-up, the End Device undergoes the following sequence of events:

1. Check A1 parameter - AutoAssociate Bit

Set (bit 2 = 1) - End Device will attempt to associate to a Coordinator. (refer to steps 2-3).

Not Set (bit 2 = 0) - End Device will not attempt to associate to a Coordinator. The End Device will operate as specified by its ID, CH and MY parameters. Association is considered complete and the Associate LED will blink quickly (5 times per second). When the AutoAssociate bit is not set, the remaining steps (2-3) do not apply.

2. Discover Coordinator (if Auto-Associate Bit Set)

The End Device issues an Active Scan. The Active Scan selects one channel and transmits a BeaconRequest command to the broadcast address (0xFFFF) and broadcast PAN ID (0xFFFF). It then listens on that channel for beacons from any Coordinator operating on that channel. The listen time on each channel is determined by the SD parameter.

Once the time expires on that channel, the Active Scan selects another channel and again transmits the BeaconRequest command as before. This process continues until all channels have been scanned, or until 5 PANs have been discovered. When the Active Scan is complete, the results include a list of PAN IDs and Channels that are being used by detected PANs.

The End Device selects a Coordinator to associate with according to the A1 parameter "Reassign_PANID" and "Reassign_Channel" flags:

Reassign_PANID Bit Set (bit 0 = 1)- End Device can associate with a PAN with any ID value.

Reassign_PANID Bit Not Set (bit 0 = 0) - End Device will only associate with a PAN whose ID setting matches the ID setting of the End Device.

Reassign_Channel Bit Set (bit 1 = 1) - End Device can associate with a PAN with any CH value.

Reassign_Channel Bit Not Set (bit 1 = 0)- End Device will only associate with a PAN whose CH setting matches the CH setting of the End Device.

After applying these filters to the discovered Coordinators, if multiple candidate PANs exist, the End Device will select the PAN whose transmission link quality is the strongest. If no valid Coordinator is found, the End Device will either go to sleep (as dictated by its SM (Sleep Mode) parameter) or retry Association.

Note - An End Device will also disqualify Coordinators if they are not allowing association (A2 - AllowAssociation bit); or, if the Coordinator is not using the same NonBeacon scheme as the End Device. (They must both be programmed with NonBeacon code.)

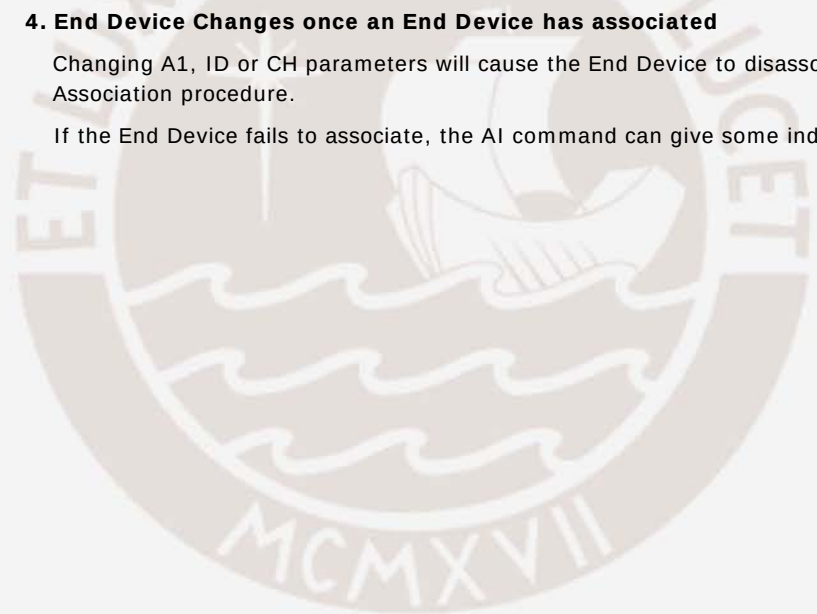
3. Associate to Valid Coordinator

Once a valid Coordinator is found (step 2), the End Device sends an AssociationRequest message to the Coordinator. It then waits for an AssociationConfirmation to be sent from the Coordinator. Once the Confirmation is received, the End Device is Associated and the Associate LED will blink rapidly (2 times per second). The LED is solid if the End Device has not associated.

4. End Device Changes once an End Device has associated

Changing A1, ID or CH parameters will cause the End Device to disassociate and restart the Association procedure.

If the End Device fails to associate, the AI command can give some indication of the failure.



XBee® /XBee-PRO® Addressing

Every RF data packet sent over-the-air contains a Source Address and Destination Address field in its header. The RF module conforms to the 802.15.4 specification and supports both short 16-bit addresses and long 64-bit addresses. A unique 64-bit IEEE source address is assigned at the factory and can be read with the SL (Serial Number Low) and SH (Serial Number High) commands. Short addressing must be configured manually. A module will use its unique 64-bit address as its Source Address if its MY (16-bit Source Address) value is "0xFFFF" or "0xFFFE".

To send a packet to a specific module using 64-bit addressing: Set the Destination Address (DL + DH) of the sender to match the Source Address (SL + SH) of the intended destination module.

To send a packet to a specific module using 16-bit addressing: Set DL (Destination Address Low) parameter to equal the MY parameter of the intended destination module and set the DH (Destination Address High) parameter to '0'.

Unicast Mode

By default, the RF module operates in Unicast Mode. Unicast Mode is the only mode that supports retries. While in this mode, receiving modules send an ACK (acknowledgement) of RF packet reception to the transmitter. If the transmitting module does not receive the ACK, it will re-send the packet up to three times or until the ACK is received.

Short 16-bit addresses. The module can be configured to use short 16-bit addresses as the Source Address by setting (MY < 0xFFFE). Setting the DH parameter (DH = 0) will configure the Destination Address to be a short 16-bit address (if DL < 0xFFFE). For two modules to communicate using short addressing, the Destination Address of the transmitter module must match the MY parameter of the receiver.

The following table shows a sample network configuration that would enable Unicast Mode communications using short 16-bit addresses.

Table 2-03. Sample Unicast Network Configuration (using 16-bit addressing)

Parameter	RF Module 1	RF Module 2
MY (Source Address)	0x01	0x02
DH (Destination Address High)	0	0
DL (Destination Address Low)	0x02	0x01

Long 64-bit addresses. The RF module's serial number (SL parameter concatenated to the SH parameter) can be used as a 64-bit source address when the MY (16-bit Source Address) parameter is disabled. When the MY parameter is disabled (MY = 0xFFFF or 0xFFFE), the module's source address is set to the 64-bit IEEE address stored in the SH and SL parameters.

When an End Device associates to a Coordinator, its MY parameter is set to 0xFFFE to enable 64-bit addressing. The 64-bit address of the module is stored as SH and SL parameters. To send a packet to a specific module, the Destination Address (DL + DH) on the sender must match the Source Address (SL + SH) of the desired receiver.

Broadcast Mode

Any RF module within range will accept a packet that contains a broadcast address. When configured to operate in Broadcast Mode, receiving modules do not send ACKs (Acknowledgements) and transmitting modules do not automatically re-send packets as is the case in Unicast Mode.

To send a broadcast packet to all modules regardless of 16-bit or 64-bit addressing, set the destination addresses of all the modules as shown below.

Sample Network Configuration (All modules in the network):

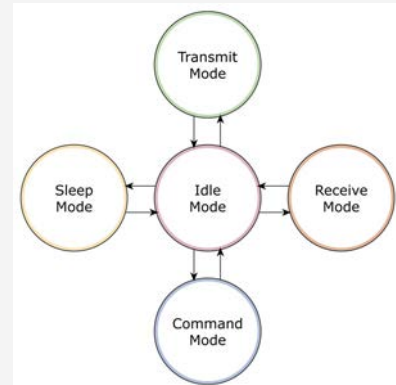
- DL (Destination Low Address) = 0x0000FFFF
- DH (Destination High Address) = 0x00000000 (default value)

NOTE: When programming the module, parameters are entered in hexadecimal notation (without the "0x" prefix). Leading zeros may be omitted.

Modes of Operation

XBee®/XBee-PRO® RF Modules operate in five modes.

Figure 2-07. Modes of Operation



Idle Mode

When not receiving or transmitting data, the RF module is in Idle Mode. The module shifts into the other modes of operation under the following conditions:

- Transmit Mode (Serial data is received in the DI Buffer)
- Receive Mode (Valid RF data is received through the antenna)
- Sleep Mode (Sleep Mode condition is met)
- Command Mode (Command Mode Sequence is issued)

Transmit/Receive Modes

RF Data Packets

Each transmitted data packet contains a Source Address and Destination Address field. The Source Address matches the address of the transmitting module as specified by the MY (Source Address) parameter (if MY $\geq$ 0xFFFE), the SH (Serial Number High) parameter or the SL (Serial Number Low) parameter. The <Destination Address> field is created from the DH (Destination Address High) and DL (Destination Address Low) parameter values. The Source Address and/or Destination Address fields will either contain a 16-bit short or long 64-bit long address.

The RF data packet structure follows the 802.15.4 specification.

[Refer to the XBee/XBee-PRO Addressing section for more information]

Direct and Indirect Transmission

There are two methods to transmit data:

- Direct Transmission - data is transmitted immediately to the Destination Address
- Indirect Transmission - A packet is retained for a period of time and is only transmitted after the destination module (Source Address = Destination Address) requests the data.

Indirect Transmissions can only occur on a Coordinator. Thus, if all nodes in a network are End Devices, only Direct Transmissions will occur. Indirect Transmissions are useful to ensure packet delivery to a sleeping node. The Coordinator currently is able to retain up to 2 indirect messages.

Direct Transmission

A Coordinator can be configured to use only Direct Transmission by setting the SP (Cyclic Sleep Period) parameter to "0". Also, a Coordinator using indirect transmissions will revert to direct transmission if it knows the destination module is awake.

To enable this behavior, the ST (Time before Sleep) value of the Coordinator must be set to match the ST value of the End Device. Once the End Device either transmits data to the Coordinator or polls the Coordinator for data, the Coordinator will use direct transmission for all subsequent data transmissions to that module address until ST time occurs with no activity (at which point it will revert to using indirect transmissions for that module address). "No activity" means no transmission or reception of messages with a specific address. Global messages will not reset the ST timer.

Indirect Transmission

To configure Indirect Transmissions in a PAN (Personal Area Network), the SP (Cyclic Sleep Period) parameter value on the Coordinator must be set to match the longest sleep value of any End Device. The sleep period value on the Coordinator determines how long (time or number of beacons) the Coordinator will retain an indirect message before discarding it.

An End Device must poll the Coordinator once it wakes from Sleep to determine if the Coordinator has an indirect message for it. For Cyclic Sleep Modes, this is done automatically every time the module wakes (after SP time). For Pin Sleep Modes, the A1 (End Device Association) parameter value must be set to enable Coordinator polling on pin wake-up. Alternatively, an End Device can use the FP (Force Poll) command to poll the Coordinator as needed.

CCA (Clear Channel Assessment)

Prior to transmitting a packet, a CCA (Clear Channel Assessment) is performed on the channel to determine if the channel is available for transmission. The detected energy on the channel is compared with the CA (Clear Channel Assessment) parameter value. If the detected energy exceeds the CA parameter value, the packet is not transmitted.

Also, a delay is inserted before a transmission takes place. This delay is settable using the RN (Backoff Exponent) parameter. If RN is set to "0", then there is no delay before the first CCA is performed. The RN parameter value is the equivalent of the "minBE" parameter in the 802.15.4 specification. The transmit sequence follows the 802.15.4 specification.

By default, the MM (MAC Mode) parameter = 0. On a CCA failure, the module will attempt to re-send the packet up to two additional times.

When in Unicast packets with RR (Retries) = 0, the module will execute two CCA retries. Broadcast packets always get two CCA retries.

Acknowledgement

If the transmission is not a broadcast message, the module will expect to receive an acknowledgement from the destination node. If an acknowledgement is not received, the packet will be resent up to 3 more times. If the acknowledgement is not received after all transmissions, an ACK failure is recorded.

Sleep Mode

Sleep Modes enable the RF module to enter states of low-power consumption when not in use. In order to enter Sleep Mode, one of the following conditions must be met (in addition to the module having a non-zero SM parameter value):

- Sleep_RQ (pin 9) is asserted and the module is in a pin sleep mode (SM = 1, 2, or 5)
- The module is idle (no data transmission or reception) for the amount of time defined by the ST (Time before Sleep) parameter. [NOTE: ST is only active when SM = 4-5.]

Table 2-04. Sleep Mode Configurations

Sleep Mode Setting	Transition into Sleep Mode	Transition out of Sleep Mode (wake)	Characteristics	Related Commands	Power Consumption
Pin Hibernate (SM = 1)	Assert (high) Sleep_RQ (pin 9)	De-assert (low) Sleep_RQ	Pin/Host-controlled / NonBeacon systems only / Lowest Power	(SM)	< 10 μ A (@3.0 VCC)
Pin Doze (SM = 2)	Assert (high) Sleep_RQ (pin 9)	De-assert (low) Sleep_RQ	Pin/Host-controlled / NonBeacon systems only / Fastest wake-up	(SM)	< 50 μ A
Cyclic Sleep (SM = 4)	Automatic transition to Sleep Mode as defined by the SM (Sleep Mode) and ST (Time before Sleep) parameters.	Transition occurs after the cyclic sleep time interval elapses. The time interval is defined by the SP (Cyclic Sleep Period) parameter.	RF module wakes in pre-determined time intervals to detect if RF data is present / When SM = 5	(SM), SP, ST	< 50 μ A when sleeping
Cyclic Sleep (SM = 5)	Automatic transition to Sleep Mode as defined by the SM (Sleep Mode) and ST (Time before Sleep) parameters or on a falling edge transition of the SLEEP_RQ pin.	Transition occurs after the cyclic sleep time interval elapses. The time interval is defined by the SP (Cyclic Sleep Period) parameter.	RF module wakes in pre-determined time intervals to detect if RF data is present. Module also wakes on a falling edge of SLEEP_RQ	(SM), SP, ST	< 50 μ A when sleeping

The SM command is central to setting Sleep Mode configurations. By default, Sleep Modes are disabled (SM = 0) and the module remains in Idle/Receive Mode. When in this state, the module is constantly ready to respond to serial or RF activity.

Pin / Host-controlled Sleep Modes

The transient current when waking from pin sleep (SM = 1 or 2) does not exceed the idle current of the module. The current ramps up exponentially to its idle current.

Pin Hibernate (SM = 1)

- Pin/Host-controlled
- Typical power-down current: < 10 μ A (@3.0 VCC)
- Wake-up time: 13.2 msec

Pin Hibernate Mode minimizes quiescent power (power consumed when in a state of rest or inactivity). This mode is voltage level-activated; when Sleep_RQ (pin 9) is asserted, the module will finish any transmit, receive or association activities, enter Idle Mode, and then enter a state of sleep. The module will not respond to either serial or RF activity while in pin sleep.

To wake a sleeping module operating in Pin Hibernate Mode, de-assert Sleep_RQ (pin 9). The module will wake when Sleep_RQ is de-asserted and is ready to transmit or receive when the CTS line is low. When waking the module, the pin must be de-asserted at least two 'byte times' after CTS goes low. This assures that there is time for the data to enter the DI buffer.

Pin Doze (SM = 2)

- Pin/Host-controlled
- Typical power-down current: < 50 μ A
- Wake-up time: 2 msec

Pin Doze Mode functions as does Pin Hibernate Mode; however, Pin Doze features faster wake-up time and higher power consumption.

To wake a sleeping module operating in Pin Doze Mode, de-assert Sleep_RQ (pin 9). The module will wake when Sleep_RQ is de-asserted and is ready to transmit or receive when the CTS line is

low. When waking the module, the pin must be de-asserted at least two 'byte times' after CTS goes low. This assures that there is time for the data to enter the DI buffer.

Cyclic Sleep Modes

Cyclic Sleep Remote (SM = 4)

- Typical Power-down Current: < 50 μ A (when asleep)
- Wake-up time: 2 msec

The Cyclic Sleep Modes allow modules to periodically check for RF data. When the SM parameter is set to '4', the module is configured to sleep, then wakes once a cycle to check for data from a module configured as a Cyclic Sleep Coordinator (SM = 0, CE = 1). The Cyclic Sleep Remote sends a poll request to the coordinator at a specific interval set by the SP (Cyclic Sleep Period) parameter. The coordinator will transmit any queued data addressed to that specific remote upon receiving the poll request.

If no data is queued for the remote, the coordinator will not transmit and the remote will return to sleep for another cycle. If queued data is transmitted back to the remote, it will stay awake to allow for back and forth communication until the ST (Time before Sleep) timer expires.

Also note that $\overline{\text{CTS}}$ will go low each time the remote wakes, allowing for communication initiated by the remote host if desired.

Cyclic Sleep Remote with Pin Wake-up (SM = 5)

Use this mode to wake a sleeping remote module through either the RF interface or by the de-assertion of Sleep_RQ for event-driven communications. The cyclic sleep mode works as described above (Cyclic Sleep Remote) with the addition of a pin-controlled wake-up at the remote module. The Sleep_RQ pin is edge-triggered, not level-triggered. The module will wake when a low is detected then set $\overline{\text{CTS}}$ low as soon as it is ready to transmit or receive.

Any activity will reset the ST (Time before Sleep) timer so the module will go back to sleep only after there is no activity for the duration of the timer. Once the module wakes (pin-controlled), further pin activity is ignored. The module transitions back into sleep according to the ST time regardless of the state of the pin.

[Cyclic Sleep Coordinator (SM = 6)]

- Typical current = Receive current
- Always awake

NOTE: The SM=6 parameter value exists solely for backwards compatibility with firmware version 1.x60. If backwards compatibility with the older firmware version is not required, always use the CE (Coordinator Enable) command to configure a module as a Coordinator.

This mode configures a module to wake cyclic sleeping remotes through RF interfacing. The Coordinator will accept a message addressed to a specific remote 16 or 64-bit address and hold it in a buffer until the remote wakes and sends a poll request. Messages not sent directly (buffered and requested) are called "Indirect messages". The Coordinator only queues one indirect message at a time. The Coordinator will hold the indirect message for a period 2.5 times the sleeping period indicated by the SP (Cyclic Sleep Period) parameter. The Coordinator's SP parameter should be set to match the value used by the remotes.

Command Mode

To modify or read RF Module parameters, the module must first enter into Command Mode - a state in which incoming characters are interpreted as commands. Two Command Mode options are supported: AT Command Mode [refer to section below] and API Command Mode [p57].

AT Command Mode

To Enter AT Command Mode:

Send the 3-character command sequence “+++” and observe guard times before and after the command characters. [Refer to the “Default AT Command Mode Sequence” below.]

Default AT Command Mode Sequence (for transition to Command Mode):

- No characters sent for one second [GT (Guard Times) parameter = 0x3E8]
- Input three plus characters (“+++”) within one second [CC (Command Sequence Character) parameter = 0x2B.]
- No characters sent for one second [GT (Guard Times) parameter = 0x3E8]

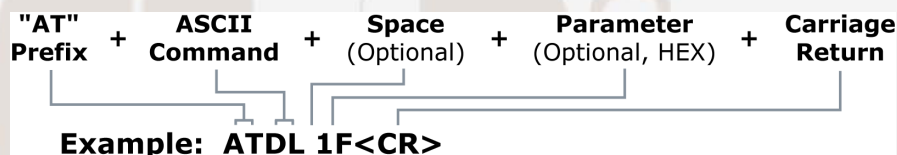
All of the parameter values in the sequence can be modified to reflect user preferences.

NOTE: Failure to enter AT Command Mode is most commonly due to baud rate mismatch. Ensure the ‘Baud’ setting on the “PC Settings” tab matches the interface data rate of the RF module. By default, the BD parameter = 3 (9600 bps).

To Send AT Commands:

Send AT commands and parameters using the syntax shown below.

Figure 2-08. Syntax for sending AT Commands



To read a parameter value stored in the RF module's register, omit the parameter field.

The preceding example would change the RF module Destination Address (Low) to “0x1F”. To store the new value to non-volatile (long term) memory, subsequently send the WR (Write) command.

For modified parameter values to persist in the module's registry after a reset, changes must be saved to non-volatile memory using the WR (Write) Command. Otherwise, parameters are restored to previously saved values after the module is reset.

System Response. When a command is sent to the module, the module will parse and execute the command. Upon successful execution of a command, the module returns an “OK” message. If execution of a command results in an error, the module returns an “ERROR” message.

To Exit AT Command Mode:

1. Send the ATCN (Exit Command Mode) command (followed by a carriage return).
[OR]
2. If no valid AT Commands are received within the time specified by CT (Command Mode Timeout) Command, the RF module automatically returns to Idle Mode.

For an example of programming the RF module using AT Commands and descriptions of each configurable parameter, refer to the RF Module Configuration chapter [p26].

3. RF Module Configuration

Programming the RF Module

Refer to the Command Mode section [p25] for more information about entering Command Mode, sending AT commands and exiting Command Mode. For information regarding module programming using API Mode, refer to the API Operation sections [p57].

Programming Examples

Setup

The programming examples in this section require the installation of Digi's X-CTU Software and a serial connection to a PC. (Digi stocks RS-232 and USB boards to facilitate interfacing with a PC.)

1. Install Digi's X-CTU Software to a PC by double-clicking the "setup_X-CTU.exe" file. (The file is located on the Digi CD and www.digi.com/xctu.)
2. Mount the RF module to an interface board, then connect the module assembly to a PC.
3. Launch the X-CTU Software and select the 'PC Settings' tab. Verify the baud and parity settings of the Com Port match those of the RF module.

NOTE: Failure to enter AT Command Mode is most commonly due to baud rate mismatch. Ensure the 'Baud' setting on the 'PC Settings' tab matches the interface data rate of the RF module. By default, the BD parameter = 3 (which corresponds to 9600 bps).

Sample Configuration: Modify RF Module Destination Address

Example: Utilize the X-CTU "Terminal" tab to change the RF module's DL (Destination Address Low) parameter and save the new address to non-volatile memory.

After establishing a serial connection between the RF module and a PC [refer to the 'Setup' section above], select the "Terminal" tab of the X-CTU Software and enter the following command lines ('CR' stands for carriage return):

Method 1 (One line per command)

Send AT Command	System Response
+++	OK <CR> (Enter into Command Mode)
ATDL <Enter>	{current value} <CR> (Read Destination Address Low)
ATDL1A0D <Enter>	OK <CR> (Modify Destination Address Low)
ATWR <Enter>	OK <CR> (Write to non-volatile memory)
ATCN <Enter>	OK <CR> (Exit Command Mode)

Method 2 (Multiple commands on one line)

Send AT Command	System Response
+++	OK <CR> (Enter into Command Mode)
ATDL <Enter>	{current value} <CR> (Read Destination Address Low)
ATDL1A0D,WR,CN <Enter>	OK<CR> OK<CR> OK<CR>

Sample Configuration: Restore RF Module Defaults

Example: Utilize the X-CTU "Modem Configuration" tab to restore default parameter values.

After establishing a connection between the module and a PC [refer to the 'Setup' section above], select the "Modem Configuration" tab of the X-CTU Software.

1. Select the 'Read' button.
2. Select the 'Restore' button.

Remote Configuration Commands

The API firmware has provisions to send configuration commands to remote devices using the Remote Command Request API frame (see API Operation). This API frame can be used to send commands to a remote module to read or set command parameters.

The API firmware has provisions to send configuration commands (set or read) to a remote module using the Remote Command Request API frame (see API Operations). Remote commands can be issued to read or set command parameters on a remote device.

Sending a Remote Command

To send a remote command, the Remote Command Request frame should be populated with values for the 64 bit and 16 bit addresses. If 64 bit addressing is desired then the 16 bit address field should be filled with 0xFFFF. If any value other than 0xFFFF is used in the 16 bit address field then the 64 bit address field will be ignored and 16 bit addressing will be used. If a command response is desired, the Frame ID should be set to a non-zero value.

Applying Changes on Remote

When remote commands are used to change command parameter settings on a remote device, parameter changes do not take effect until the changes are applied. For example, changing the BD parameter will not change the actual serial interface rate on the remote until the changes are applied. Changes can be applied using remote commands in one of three ways:

Set the apply changes option bit in the API frame

Issue an AC command to the remote device

Issue a WR + FR command to the remote device to save changes and reset the device.

Remote Command Responses

If the remote device receives a remote command request transmission, and the API frame ID is non-zero, the remote will send a remote command response transmission back to the device that sent the remote command. When a remote command response transmission is received, a device sends a remote command response API frame out its UART. The remote command response indicates the status of the command (success, or reason for failure), and in the case of a command query, it will include the register value.

The device that sends a remote command will not receive a remote command response frame if:

The destination device could not be reached

The frame ID in the remote command request is set to 0.

Command Reference Tables

XBee®/XBee-PRO® RF Modules expect numerical values in hexadecimal. Hexadecimal values are designated by a "0x" prefix. Decimal equivalents are designated by a "d" suffix. Commands are contained within the following command categories (listed in the order that their tables appear):

- Special
- Networking & Security
- RF Interfacing
- Sleep (Low Power)
- Serial Interfacing
- I/O Settings
- Diagnostics
- AT Command Options

All modules within a PAN should operate using the same firmware version.

Special**Table 3-01. XBee-PRO Commands - Special**

AT Command	Command Category	Name and Description	Parameter Range	Default
WR	Special	Write. Write parameter values to non-volatile memory so that parameter modifications persist through subsequent power-up or reset. Note: Once WR is issued, no additional characters should be sent to the module until after the response "OK\r" is received.	-	-
RE	Special	Restore Defaults. Restore module parameters to factory defaults.	-	-
FR (v1.x80*)	Special	Software Reset. Responds immediately with an OK then performs a hard reset ~100ms later.	-	-

* Firmware version in which the command was first introduced (firmware versions are numbered in hexadecimal notation.)

Networking & Security**Table 3-02. XBee®/XBee-PRO® Commands - Networking & Security** (Sub-categories designated within {brackets})

AT Command	Command Category	Name and Description	Parameter Range	Default
CH	Networking {Addressing}	Channel. Set/Read the channel number used for transmitting and receiving data between RF modules (uses 802.15.4 protocol channel numbers).	0x0B - 0x1A (XBee) 0x0C - 0x17 (XBee-PRO)	0x0C (12d)
ID	Networking {Addressing}	PAN ID. Set/Read the PAN (Personal Area Network) ID. Use 0xFFFF to broadcast messages to all PANs.	0 - 0xFFFF	0x3332 (13106d)
DH	Networking {Addressing}	Destination Address High. Set/Read the upper 32 bits of the 64-bit destination address. When combined with DL, it defines the destination address used for transmission. To transmit using a 16-bit address, set DH parameter to zero and DL less than 0xFFFF. 0x000000000000FFFF is the broadcast address for the PAN.	0 - 0xFFFFFFFF	0
DL	Networking {Addressing}	Destination Address Low. Set/Read the lower 32 bits of the 64-bit destination address. When combined with DH, DL defines the destination address used for transmission. To transmit using a 16-bit address, set DH parameter to zero and DL less than 0xFFFF. 0x000000000000FFFF is the broadcast address for the PAN.	0 - 0xFFFFFFFF	0
MY	Networking {Addressing}	16-bit Source Address. Set/Read the RF module 16-bit source address. Set MY = 0xFFFF to disable reception of packets with 16-bit addresses. 64-bit source address (serial number) and broadcast address (0x000000000000FFFF) is always enabled.	0 - 0xFFFF	0
SH	Networking {Addressing}	Serial Number High. Read high 32 bits of the RF module's unique IEEE 64-bit address. 64-bit source address is always enabled.	0 - 0xFFFFFFFF [read-only]	Factory-set
SL	Networking {Addressing}	Serial Number Low. Read low 32 bits of the RF module's unique IEEE 64-bit address. 64-bit source address is always enabled.	0 - 0xFFFFFFFF [read-only]	Factory-set
RR (v1.xA0*)	Networking {Addressing}	XBee Retries. Set/Read the maximum number of retries the module will execute in addition to the 3 retries provided by the 802.15.4 MAC. For each XBee retry, the 802.15.4 MAC can execute up to 3 retries.	0 - 6	0
RN	Networking {Addressing}	Random Delay Slots. Set/Read the minimum value of the back-off exponent in the CSMA-CA algorithm that is used for collision avoidance. If RN = 0, collision avoidance is disabled during the first iteration of the algorithm (802.15.4 - macMinBE).	0 - 3 [exponent]	0
MM (v1.x80*)	Networking {Addressing}	MAC Mode. MAC Mode. Set/Read MAC Mode value. MAC Mode enables/disables the use of a Digi header in the 802.15.4 RF packet. When Modes 0 or 3 are enabled (MM=0,3), duplicate packet detection is enabled as well as certain AT commands. Please see the detailed MM description on page 47 for additional information.	0 - 3 0 = Digi Mode 1 = 802.15.4 (no ACKs) 2 = 802.15.4 (with ACKs) 3 = Digi Mode (no ACKs)	0
NI (v1.x80*)	Networking {Identification}	Node Identifier. Stores a string identifier. The register only accepts printable ASCII data. A string can not start with a space. Carriage return ends command. Command will automatically end when maximum bytes for the string have been entered. This string is returned as part of the ND (Node Discover) command. This identifier is also used with the DN (Destination Node) command.	20-character ASCII string	-
ND (v1.x80*)	Networking {Identification}	Node Discover. Discovers and reports all RF modules found. The following information is reported for each module discovered (the example cites use of Transparent operation (AT command format) - refer to the long ND command description regarding differences between Transparent and API operation). MY<CR> SH<CR> SL<CR> DB<CR> NI<CR><CR> The amount of time the module allows for responses is determined by the NT parameter. In Transparent operation, command completion is designated by a <CR> (carriage return). ND also accepts a Node Identifier as a parameter. In this case, only a module matching the supplied identifier will respond. If ND self-response is enabled (NO=1) the module initiating the node discover will also output a response for itself.	optional 20-character NI value	
NT (v1.xA0*)	Networking {Identification}	Node Discover Time. Set/Read the amount of time a node will wait for responses from other nodes when using the ND (Node Discover) command.	0x01 - 0xFC [x 100 ms]	0x19

Table 3-02. XBee®/XBee-PRO® Commands - Networking & Security (Sub-categories designated within {brackets})

AT Command	Command Category	Name and Description	Parameter Range	Default
NO (v1xC5)	Networking {Identification}	Node Discover Options. Enables node discover self-response on the module.	0-1	0
DN (v1.x80*)	Networking {Identification}	Destination Node. Resolves an NI (Node Identifier) string to a physical address. The following events occur upon successful command execution: 1. DL and DH are set to the address of the module with the matching Node Identifier. 2. "OK" is returned. 3. RF module automatically exits AT Command Mode If there is no response from a module within 200 msec or a parameter is not specified (left blank), the command is terminated and an "ERROR" message is returned.	20-character ASCII string	-
CE (v1.x80*)	Networking {Association}	Coordinator Enable. Set/Read the coordinator setting.	0 - 1 0 = End Device 1 = Coordinator	0
SC (v1.x80*)	Networking {Association}	Scan Channels. Set/Read list of channels to scan for all Active and Energy Scans as a bitfield. This affects scans initiated in command mode (AS, ED) and during End Device Association and Coordinator startup: bit 0 - 0x0B bit 4 - 0x0F bit 8 - 0x13 bit12 - 0x17 bit 1 - 0x0C bit 5 - 0x10 bit 9 - 0x14 bit13 - 0x18 bit 2 - 0x0D bit 6 - 0x11 bit 10 - 0x15 bit14 - 0x19 bit 3 - 0x0E bit 7 - 0x12 bit 11 - 0x16 bit 15 - 0x1A	0 - 0xFFFF [bitfield] (bits 0, 14, 15 not allowed on the XBee-PRO)	0x1FFE (all XBee-PRO Channels)
SD (v1.x80*)	Networking {Association}	Scan Duration. Set/Read the scan duration exponent. End Device - Duration of Active Scan during Association. Coordinator - If 'ReassignPANID' option is set on Coordinator [refer to A2 parameter], SD determines the length of time the Coordinator will scan channels to locate existing PANs. If 'ReassignChannel' option is set, SD determines how long the Coordinator will perform an Energy Scan to determine which channel it will operate on. 'Scan Time' is measured as (# of channels to scan] * (2 ^ SD) * 15.36ms). The number of channels to scan is set by the SC command. The XBee can scan up to 16 channels (SC = 0xFFFF). The XBee PRO can scan up to 13 channels (SC = 0x3FFE). Example: The values below show results for a 13 channel scan: If SD = 0, time = 0.18 sec SD = 8, time = 47.19 sec SD = 2, time = 0.74 sec SD = 10, time = 3.15 min SD = 4, time = 2.95 sec SD = 12, time = 12.58 min SD = 6, time = 11.80 sec SD = 14, time = 50.33 min	0-0x0F [exponent]	4
A1 (v1.x80*)	Networking {Association}	End Device Association. Set/Read End Device association options. bit 0 - ReassignPanID 0 - Will only associate with Coordinator operating on PAN ID that matches module ID 1 - May associate with Coordinator operating on any PAN ID bit 1 - ReassignChannel 0 - Will only associate with Coordinator operating on matching CH Channel setting 1 - May associate with Coordinator operating on any Channel bit 2 - AutoAssociate 0 - Device will not attempt Association 1 - Device attempts Association until success Note: This bit is used only for Non-Beacon systems. End Devices in Beacon-enabled system must always associate to a Coordinator bit 3 - PollCoordOnPinWake 0 - Pin Wake will not poll the Coordinator for indirect (pending) data 1 - Pin Wake will send Poll Request to Coordinator to extract any pending data bits 4 - 7 are reserved	0 - 0x0F [bitfield]	0
A2 (v1.x80*)	Networking {Association}	Coordinator Association. Set/Read Coordinator association options. bit 0 - ReassignPanID 0 - Coordinator will not perform Active Scan to locate available PAN ID. It will operate on ID (PAN ID). 1 - Coordinator will perform Active Scan to determine an available ID (PAN ID). If a PAN ID conflict is found, the ID parameter will change. bit 1 - ReassignChannel - 0 - Coordinator will not perform Energy Scan to determine free channel. It will operate on the channel determined by the CH parameter. 1 - Coordinator will perform Energy Scan to find a free channel, then operate on that channel. bit 2 - AllowAssociation - 0 - Coordinator will not allow any devices to associate to it. 1 - Coordinator will allow devices to associate to it. bits 3 - 7 are reserved	0 - 7 [bitfield]	0

Table 3-02. XBee®/XBee-PRO® Commands - Networking & Security (Sub-categories designated within [brackets])

AT Command	Command Category	Name and Description	Parameter Range	Default
AI (v1.x80*)	Networking {Association}	Association Indication. Read errors with the last association request: 0x00 - Successful Completion - Coordinator successfully started or End Device association complete 0x01 - Active Scan Timeout 0x02 - Active Scan found no PANs 0x03 - Active Scan found PAN, but the CoordinatorAllowAssociation bit is not set 0x04 - Active Scan found PAN, but Coordinator and End Device are not configured to support beacons 0x05 - Active Scan found PAN, but the Coordinator ID parameter does not match the ID parameter of the End Device 0x06 - Active Scan found PAN, but the Coordinator CH parameter does not match the CH parameter of the End Device 0x07 - Energy Scan Timeout 0x08 - Coordinator start request failed 0x09 - Coordinator could not start due to invalid parameter 0x0A - Coordinator Realignment is in progress 0x0B - Association Request not sent 0x0C - Association Request timed out - no reply was received 0x0D - Association Request had an Invalid Parameter 0x0E - Association Request Channel Access Failure. Request was not transmitted - CCA failure 0x0F - Remote Coordinator did not send an ACK after Association Request was sent 0x10 - Remote Coordinator did not reply to the Association Request, but an ACK was received after sending the request 0x11 - [reserved] 0x12 - Sync-Loss - Lost synchronization with a Beaconing Coordinator 0x13 - Disassociated - No longer associated to Coordinator 0xFF - RF Module is attempting to associate	0 - 0x13 [read-only]	-
DA (v1.x80*)	Networking {Association}	Force Disassociation. End Device will immediately disassociate from a Coordinator (if associated) and reattempt to associate.	-	-
FP (v1.x80*)	Networking {Association}	Force Poll. Request indirect messages being held by a coordinator.	-	-
AS (v1.x80*)	Networking {Association}	Active Scan. Send Beacon Request to Broadcast Address (0xFFFF) and Broadcast PAN (0xFFFF) on every channel. The parameter determines the time the radio will listen for Beacons on each channel. A PanDescriptor is created and returned for every Beacon received from the scan. Each PanDescriptor contains the following information: CoordAddress (SH, SL)<CR> CoordPanID (ID)<CR> CoordAddrMode <CR> 0x02 = 16-bit Short Address 0x03 = 64-bit Long Address Channel (CH parameter) <CR> SecurityUse<CR> ACLEntry<CR> SecurityFailure<CR> SuperFrameSpec<CR> (2 bytes): bit 15 - Association Permitted (MSB) bit 14 - PAN Coordinator bit 13 - Reserved bit 12 - Battery Life Extension bits 8-11 - Final CAP Slot bits 4-7 - Superframe Order bits 0-3 - Beacon Order GtsPermit<CR> RSSI<CR> (RSSI is returned as -dBm) TimeStamp<CR> (3 bytes) <CR> A carriage return <CR> is sent at the end of the AS command. The Active Scan is capable of returning up to 5 PanDescriptors in a scan. The actual scan time on each channel is measured as Time = [(2 ^SD PARAM) * 15.36] ms. Note the total scan time is this time multiplied by the number of channels to be scanned (16 for the XBee and 13 for the XBee-PRO). Also refer to SD command description.	0 - 6	-
ED (v1.x80*)	Networking {Association}	Energy Scan. Send an Energy Detect Scan. This parameter determines the length of scan on each channel. The maximal energy on each channel is returned & each value is followed by a carriage return. An additional carriage return is sent at the end of the command. The values returned represent the detected energy level in units of -dBm. The actual scan time on each channel is measured as Time = [(2 ^ED) * 15.36] ms. Note the total scan time is this time multiplied by the number of channels to be scanned (refer to SD parameter).	0 - 6	-
EE (v1.xA0*)	Networking {Security}	AES Encryption Enable. Disable/Enable 128-bit AES encryption support. Use in conjunction with the KY command.	0 - 1	0 (disabled)
KY (v1.xA0*)	Networking {Security}	AES Encryption Key. Set the 128-bit AES (Advanced Encryption Standard) key for encrypting/decrypting data. The KY register cannot be read.	0 - (any 16-Byte value)	-

* Firmware version in which the command was first introduced (firmware versions are numbered in hexadecimal notation.)

RF Interfacing**Table 3-03. XBee/XBee-PRO Commands - RF Interfacing**

AT Command	Command Category	Name and Description	Parameter Range	Default
PL	RF Interfacing	Power Level. Select/Read the power level at which the RF module transmits conducted power.	0 - 4 (XBee / XBee-PRO) 0 = -10 / 10 dBm 1 = -6 / 12 dBm 2 = -4 / 14 dBm 3 = -2 / 16 dBm 4 = 0 / 18 dBm XBee-PRO International variant: PL=4: 10 dBm PL=3: 8 dBm PL=2: 2 dBm PL=1: -3 dBm PL=0: -3 dBm	4
CA (v1.x80*)	RF Interfacing	CCA Threshold. Set/read the CCA (Clear Channel Assessment) threshold. Prior to transmitting a packet, a CCA is performed to detect energy on the channel. If the detected energy is above the CCA Threshold, the module will not transmit the packet.	0x24 - 0x50 [-dBm]	0x2C (-44d dBm)

* Firmware version in which the command was first introduced (firmware versions are numbered in hexadecimal notation.)

Sleep (Low Power)**Table 3-04. XBee®/XBee-PRO® Commands - Sleep (Low Power)**

AT Command	Command Category	Name and Description	Parameter Range	Default
SM	Sleep (Low Power)	Sleep Mode. Set/Read Sleep Mode configurations.	0 - 5 0 = No Sleep 1 = Pin Hibernate 2 = Pin Doze 3 = Reserved 4 = Cyclic sleep remote 5 = Cyclic sleep remote w/ pin wake-up 6 = [Sleep Coordinator] for backwards compatibility w/ v1.x6 only; otherwise, use CE command.	0
SO	Sleep (Low Power)	Sleep Options Set/Read the sleep mode options. Bit 0 - Poll wakeup disable 0 - Normal operations. A module configured for cyclic sleep will poll for data on waking. 1 - Disable wakeup poll. A module configured for cyclic sleep will not poll for data on waking. Bit 1 - ADC/DIO wakeup sampling disable. 0 - Normal operations. A module configured in a sleep mode with ADC/DIO sampling enabled will automatically perform a sampling on wakeup. 1 - Suppress sample on wakeup. A module configured in a sleep mode with ADC/DIO sampling enabled will not automatically sample on wakeup.	0-4	0
ST	Sleep (Low Power)	Time before Sleep. <NonBeacon firmware> Set/Read time period of inactivity (no serial or RF data is sent or received) before activating Sleep Mode. ST parameter is only valid with Cyclic Sleep settings (SM = 4 - 5). Coordinator and End Device ST values must be equal. Also note, the GT parameter value must always be less than the ST value. (If GT > ST, the configuration will render the module unable to enter into command mode.) If the ST parameter is modified, also modify the GT parameter accordingly.	1 - 0xFFFF [x 1 ms]	0x1388 (5000d)
SP	Sleep (Low Power)	Cyclic Sleep Period. <NonBeacon firmware> Set/Read sleep period for cyclic sleeping remotes. Coordinator and End Device SP values should always be equal. To send Direct Messages, set SP = 0. End Device - SP determines the sleep period for cyclic sleeping remotes. Maximum sleep period is 268 seconds (0x68B0). Coordinator - If non-zero, SP determines the time to hold an indirect message before discarding it. A Coordinator will discard indirect messages after a period of (2.5 * SP).	0 - 0x68B0 [x 10 ms]	0
DP (1.x80*)	Sleep (Low Power)	Disassociated Cyclic Sleep Period. <NonBeacon firmware> End Device - Set/Read time period of sleep for cyclic sleeping remotes that are configured for Association but are not associated to a Coordinator. (i.e. If a device is configured to associate, configured as a Cyclic Sleep remote, but does not find a Coordinator, it will sleep for DP time before reattempting association.) Maximum sleep period is 268 seconds (0x68B0). DP should be > 0 for NonBeacon systems.	1 - 0x68B0 [x 10 ms]	0x3E8 (1000d)

* Firmware version in which the command was first introduced (firmware versions are numbered in hexadecimal notation.)

Serial Interfacing

Table 3-05. XBee-PRO Commands - Serial Interfacing

AT Command	Command Category	Name and Description	Parameter Range	Default
BD	Serial Interfacing	Interface Data Rate. Set/Read the serial interface data rate for communications between the RF module serial port and host. Request non-standard baud rates with values above 0x80 using a terminal window. Read the BD register to find actual baud rate achieved.	0 - 7 (standard baud rates) 0 = 1200 bps 1 = 2400 2 = 4800 3 = 9600 4 = 19200 5 = 38400 6 = 57600 7 = 115200 0x80 - 0x3D090 (non-standard baud rates up to 250 Kbps)	3
RO	Serial Interfacing	Packetization Timeout. Set/Read number of character times of inter-character delay required before transmission. Set to zero to transmit characters as they arrive instead of buffering them into one RF packet.	0 - 0xFF [x character times]	3
AP (v1.x80*)	Serial Interfacing	API Enable. Disable/Enable API Mode.	0 - 2 0 = Disabled 1 = API enabled 2 = API enabled (w/escaped control characters)	0
NB	Serial Interfacing	Parity. Set/Read parity settings.	0 - 4 0 = 8-bit no parity 1 = 8-bit even 2 = 8-bit odd 3 = 8-bit mark 4 = 8-bit space	0
PR (v1.x80*)	Serial Interfacing	Pull-up Resistor Enable. Set/Read bitfield to configure internal pull-up resistor status for I/O lines Bitfield Map: bit 0 - AD4/DIO4 (pin11) bit 1 - AD3 / DIO3 (pin17) bit 2 - AD2/DIO2 (pin18) bit 3 - AD1/DIO1 (pin19) bit 4 - AD0 / DIO0 (pin20) bit 5 - RTS / AD6 / DIO6 (pin16) bit 6 - DTR / SLEEP_RQ / DI8 (pin9) bit 7 - DIN/CONFIG (pin3) Bit set to "1" specifies pull-up enabled; "0" specifies no pull-up	0 - 0xFF	0xFF

* Firmware version in which the command was first introduced (firmware versions are numbered in hexadecimal notation.)

I/O Settings

Table 3-06. XBee-PRO Commands - I/O Settings (sub-category designated within {brackets})

AT Command	Command Category	Name and Description	Parameter Range	Default
D8	I/O Settings	DI8 Configuration. Select/Read options for the DI8 line (pin 9) of the RF module.	0 - 1 0 = Disabled 3 = DI (1,2,4 & 5 n/a)	0
D7 (v1.x80*)	I/O Settings	DIO7 Configuration. Select/Read settings for the DIO7 line (pin 12) of the RF module. Options include CTS flow control and I/O line settings.	0 - 1 0 = Disabled 1 = CTS Flow Control 2 = (n/a) 3 = DI 4 = DO low 5 = DO high 6 = RS485 Tx Enable Low 7 = RS485 Tx Enable High	1
D6 (v1.x80*)	I/O Settings	DIO6 Configuration. Select/Read settings for the DIO6 line (pin 16) of the RF module. Options include RTS flow control and I/O line settings.	0 - 1 0 = Disabled 1 = RTS flow control 2 = (n/a) 3 = DI 4 = DO low 5 = DO high	0

Table 3-06. XBee-PRO Commands - I/O Settings (sub-category designated within [brackets])

AT Command	Command Category	Name and Description	Parameter Range	Default
D5 (v1.x80*)	I/O Settings	DIO5 Configuration. Configure settings for the DIO5 line (pin 15) of the RF module. Options include Associated LED indicator (blinks when associated) and I/O line settings.	0 - 1 0 = Disabled 1 = Associated indicator 2 = ADC 3 = DI 4 = DO low 5 = DO high	1
D0 - D4 (v1.xA0*)	I/O Settings	(DIO4 - DIO4) Configuration. Select/Read settings for the following lines: AD0/DIO0 (pin 20), AD1/DIO1 (pin 19), AD2/DIO2 (pin 18), AD3/DIO3 (pin 17), AD4/DIO4 (pin 11). Options include: Analog-to-digital converter, Digital Input and Digital Output.	0 - 1 0 = Disabled 1 = (n/a) 2 = ADC 3 = DI 4 = DO low 5 = DO high	0
IU (v1.xA0*)	I/O Settings	I/O Output Enable. Disables/Enables I/O data received to be sent out UART. The data is sent using an API frame regardless of the current AP parameter value.	0 - 1 0 = Disabled 1 = Enabled	1
IT (v1.xA0*)	I/O Settings	Samples before TX. Set/Read the number of samples to collect before transmitting data. Maximum number of samples is dependent upon the number of enabled inputs.	1 - 0xFF	1
IS (v1.xA0*)	I/O Settings	Force Sample. Force a read of all enabled inputs (DI or ADC). Data is returned through the UART. If no inputs are defined (DI or ADC), this command will return error.	8-bit bitmap (each bit represents the level of an I/O line setup as an output)	-
IO (v1.xA0*)	I/O Settings	Digital Output Level. Set digital output level to allow DIO lines that are setup as outputs to be changed through Command Mode.	-	-
IC (v1.xA0*)	I/O Settings	DIO Change Detect. Set/Read bitfield values for change detect monitoring. Each bit enables monitoring of DIO0 - DIO7 for changes. If detected, data is transmitted with DIO data only. Any samples queued waiting for transmission will be sent first.	0 - 0xFF [bitfield]	0 (disabled)
IR (v1.xA0*)	I/O Settings	Sample Rate. Set/Read sample rate. When set, this parameter causes the module to sample all enabled inputs at a specified interval.	0 - 0xFFFF [x 1 msec]	0
IA (v1.xA0*)	I/O Settings {I/O Line Passing}	I/O Input Address. Set/Read addresses of module to which outputs are bound. Setting all bytes to 0xFF will not allow any received I/O packet to change outputs. Setting address to 0xFFFF will allow any received I/O packet to change outputs.	0 - 0xFFFFFFFFFFFFFFFF	0xFFFFFFFFFFFFFFFF
T0 - T7 (v1.xA0*)	I/O Settings {I/O Line Passing}	(D0 - D7) Output Timeout. Set/Read Output timeout values for lines that correspond with the D0 - D7 parameters. When output is set (due to I/O line passing) to a non-default level, a timer is started which when expired will set the output to its default level. The timer is reset when a valid I/O packet is received.	0 - 0xFF [x 100 ms]	0xFF
P0	I/O Settings {I/O Line Passing}	PWM0 Configuration. Select/Read function for PWM0 pin.	0 - 2 0 = Disabled 1 = RSSI 2 = PWM Output	1
P1 (v1.xA0*)	I/O Settings {I/O Line Passing}	PWM1 Configuration. Select/Read function for PWM1 pin.	0 - 2 0 = Disabled 1 = RSSI 2 = PWM Output	0
M0 (v1.xA0*)	I/O Settings {I/O Line Passing}	PWM0 Output Level. Set/Read the PWM0 output level.	0 - 0x03FF	-
M1 (v1.xA0*)	I/O Settings {I/O Line Passing}	PWM1 Output Level. Set/Read the PWM1 output level.	0 - 0x03FF	-
PT (v1.xA0*)	I/O Settings {I/O Line Passing}	PWM Output Timeout. Set/Read output timeout value for both PWM outputs. When PWM is set to a non-zero value: Due to I/O line passing, a time is started which when expired will set the PWM output to zero. The timer is reset when a valid I/O packet is received.]	0 - 0xFF [x 100 ms]	0xFF
RP	I/O Settings {I/O Line Passing}	RSSI PWM Timer. Set/Read PWM timer register. Set the duration of PWM (pulse width modulation) signal output on the RSSI pin. The signal duty cycle is updated with each received packet and is shut off when the timer expires.]	0 - 0xFF [x 100 ms]	0x28 (40d)

* Firmware version in which the command was first introduced (firmware versions are numbered in hexadecimal notation.)

Diagnostics

Table 3-07. XBee®/XBee-PRO® Commands - Diagnostics

AT Command	Command Category	Name and Description	Parameter Range	Default
VR	Diagnostics	Firmware Version. Read firmware version of the RF module.	0 - 0xFFFF [read-only]	Factory-set
VL (v1.x80*)	Diagnostics	Firmware Version - Verbose. Read detailed version information (including application build date, MAC, PHY and bootloader versions). The VL command has been deprecated in version 10C9. It is not supported in firmware versions after 10C8	-	-

Table 3-07. XBee®/XBee-PRO® Commands - Diagnostics

AT Command	Command Category	Name and Description	Parameter Range	Default
HV (v1.x80*)	Diagnostics	Hardware Version. Read hardware version of the RF module.	0 - 0xFFFF [read-only]	Factory-set
DB	Diagnostics	Received Signal Strength. Read signal level [in dB] of last good packet received (RSSI). Absolute value is reported. (For example: 0x58 = -88 dBm) Reported value is accurate between -40 dBm and RX sensitivity.	0x17-0x5C (XBee) 0x24-0x64 (XBee-PRO) [read-only]	-
EC (v1.x80*)	Diagnostics	CCA Failures. Reset/Read count of CCA (Clear Channel Assessment) failures. This parameter value increments when the module does not transmit a packet because it detected energy above the CCA threshold level set with CA command. This count saturates at its maximum value. Set count to "0" to reset count.	0 - 0xFFFF	-
EA (v1.x80*)	Diagnostics	ACK Failures. Reset/Read count of acknowledgment failures. This parameter value increments when the module expires its transmission retries without receiving an ACK on a packet transmission. This count saturates at its maximum value. Set the parameter to "0" to reset count.	0 - 0xFFFF	-
ED (v1.x80*)	Diagnostics	Energy Scan. Send 'Energy Detect Scan'. ED parameter determines the length of scan on each channel. The maximal energy on each channel is returned and each value is followed by a carriage return. Values returned represent detected energy levels in units of -dBm. Actual scan time on each channel is measured as $\text{Time} = [2^{\text{ED}} \times 15.36]$ ms. Total scan time is this time multiplied by the number of channels to be scanned.	0 - 6	-

* Firmware version in which the command was first introduced (firmware versions are numbered in hexadecimal notation.)



AT Command Options**Table 3-08. XBee®/XBee-PRO® Commands - AT Command Options**

AT Command	Command Category	Name and Description	Parameter Range	Default
CT	AT Command Mode Options	Command Mode Timeout. Set/Read the period of inactivity (no valid commands received) after which the RF module automatically exits AT Command Mode and returns to Idle Mode.	2 - 0xFFFF [x 100 ms]	0x64 (100d)
CN	AT Command Mode Options	Exit Command Mode. Explicitly exit the module from AT Command Mode.	--	--
AC (v1.xA0*)	AT Command Mode Options	Apply Changes. Explicitly apply changes to queued parameter value(s) and re-initialize module.	--	--
GT	AT Command Mode Options	Guard Times. Set required period of silence before and after the Command Sequence Characters of the AT Command Mode Sequence (GT+ CC + GT). The period of silence is used to prevent inadvertent entrance into AT Command Mode.	2 - 0x0CE4 [x 1 ms]	0x3E8 (1000d)
CC	AT Command Mode Options	Command Sequence Character. Set/Read the ASCII character value to be used between Guard Times of the AT Command Mode Sequence (GT+CC+GT). The AT Command Mode Sequence enters the RF module into AT Command Mode.	0 - 0xFF	0x2B ('+' ASCII)

* Firmware version in which the command was first introduced (firmware versions are numbered in hexadecimal notation.)



Command Descriptions

Command descriptions in this section are listed alphabetically. Command categories are designated within "< >" symbols that follow each command title. XBee®/XBee-PRO® RF Modules expect parameter values in hexadecimal (designated by the "0x" prefix).

All modules operating within the same network should contain the same firmware version.

A1 (End Device Association) Command

<Networking {Association}> The A1 command is used to set and read association options for an End Device.

Use the table below to determine End Device behavior in relation to the A1 parameter.

AT Command: ATA1

Parameter Range: 0 – 0x0F [bitfield]

Default Parameter Value: 0

Related Commands: ID (PAN ID), NI (Node Identifier), CH (Channel), CE (Coordinator Enable), A2 (Coordinator Association)

Minimum Firmware Version Required: v1.x80

Bit number	End Device Association Option
0 - ReassignPanID	0 - Will only associate with Coordinator operating on PAN ID that matches Node Identifier
	1 - May associate with Coordinator operating on any PAN ID
1 - ReassignChannel	0 - Will only associate with Coordinator operating on Channel that matches CH setting
	1 - May associate with Coordinator operating on any Channel
2 - AutoAssociate	0 - Device will not attempt Association
	1 - Device attempts Association until success Note: This bit is used only for Non-Beacon systems. End Devices in a Beaconsing system must always associate to a Coordinator
3 - PollCoordOnPinWake	0 - Pin Wake will not poll the Coordinator for pending (indirect) Data
	1 - Pin Wake will send Poll Request to Coordinator to extract any pending data
4 - 7	[reserved]

A2 (Coordinator Association) Command

<Networking {Association}> The A2 command is used to set and read association options of the Coordinator.

Use the table below to determine Coordinator behavior in relation to the A2 parameter.

AT Command: ATA2

Parameter Range: 0 – 7 [bitfield]

Default Parameter Value: 0

Related Commands: ID (PAN ID), NI (Node Identifier), CH (Channel), CE (Coordinator Enable), A1 (End Device Association), AS (Active Scan), ED (Energy Scan)

Minimum Firmware Version Required: v1.x80

Bit number	End Device Association Option
0 - ReassignPanID	0 - Coordinator will not perform Active Scan to locate available PAN ID. It will operate on ID (PAN ID).
	1 - Coordinator will perform Active Scan to determine an available ID (PAN ID). If a PAN ID conflict is found, the ID parameter will change.
1 - ReassignChannel	0 - Coordinator will not perform Energy Scan to determine free channel. It will operate on the channel determined by the CH parameter.
	1 - Coordinator will perform Energy Scan to find a free channel, then operate on that channel.
2 - AllowAssociate	0 - Coordinator will not allow any devices to associate to it.
	1 - Coordinator will allow devices to associate to it.
3 - 7	[reserved]

The binary equivalent of the default value (0x06) is 00000110. 'Bit 0' is the last digit of the sequence.

AC (Apply Changes) Command

<AT Command Mode Options> The AC command is used to explicitly apply changes to module parameter values. 'Applying changes' means that the module is re-initialized based on changes made to its parameter values. Once changes are applied, the module immediately operates according to the new parameter values.

This behavior is in contrast to issuing the WR (Write) command. The WR command saves parameter values to non-volatile memory, but the module still operates according to previously saved values until the module is re-booted or the CN (Exit AT Command Mode) command is issued.

AT Command: ATAC

Minimum Firmware Version Required: v1.xA0

Refer to the "AT Command – Queue Parameter Value" API type for more information.

AI (Association Indication) Command

<Networking {Association}> The AI command is used to indicate occurrences of errors during the last association request.

Use the table below to determine meaning of the returned values.

AT Command: ATAI

Parameter Range: 0 – 0x13 [read-only]

Related Commands: AS (Active Scan), ID (PAN ID), CH (Channel), ED (Energy Scan), A1 (End Device Association), A2 (Coordinator Association), CE (Coordinator Enable)

Minimum Firmware Version Required: v1.x80

Returned Value (Hex)	Association Indication
0x00	Successful Completion - Coordinator successfully started or End Device association complete
0x01	Active Scan Timeout
0x02	Active Scan found no PANs
0x03	Active Scan found PAN, but the Coordinator Allow Association bit is not set
0x04	Active Scan found PAN, but Coordinator and End Device are not configured to support beacons
0x05	Active Scan found PAN, but Coordinator ID (PAN ID) value does not match the ID of the End Device
0x06	Active Scan found PAN, but Coordinator CH (Channel) value does not match the CH of the End Device
0x07	Energy Scan Timeout
0x08	Coordinator start request failed
0x09	Coordinator could not start due to Invalid Parameter
0x0A	Coordinator Realignment is in progress
0x0B	Association Request not sent
0x0C	Association Request timed out - no reply was received
0x0D	Association Request had an Invalid Parameter
0x0E	Association Request Channel Access Failure - Request was not transmitted - CCA failure
0x0F	Remote Coordinator did not send an ACK after Association Request was sent
0x10	Remote Coordinator did not reply to the Association Request, but an ACK was received after sending the request
0x11	[reserved]
0x12	Sync-Loss - Lost synchronization with a Beaconsing Coordinator
0x13	Disassociated - No longer associated to Coordinator
0xFF	RF Module is attempting to associate

AP (API Enable) Command

<Serial Interfacing> The AP command is used to enable the RF module to operate using a frame-based API instead of using the default Transparent (UART) mode.

AT Command: ATAP

Parameter Range: 0 – 2

Parameter	Configuration
0	Disabled (Transparent operation)
1	API enabled
2	API enabled (with escaped characters)

Default Parameter Value: 0

Minimum Firmware Version Required: v1.x80

Refer to the API Operation section when API operation is enabled (AP = 1 or 2).

AS (Active Scan) Command

<Network {Association}> The AS command is used to send a Beacon Request to a Broadcast (0xFFFF) and Broadcast PAN (0xFFFF) on every channel. The parameter determines the amount of time the RF module will listen for Beacons on each channel. A 'PanDescriptor' is created and returned for every Beacon received from the scan. Each PanDescriptor contains the following information:

AT Command: ATAS

Parameter Range: 0 – 6

Related Command: SD (Scan Duration), DL (Destination Low Address), DH (Destination High Address), ID (PAN ID), CH (Channel)

Minimum Firmware Version Required: v1.x80

CoordAddress (SH + SL parameters) <CR> (NOTE: If MY on the coordinator is set less than 0xFFFF, the MY value is displayed)

CoordPanID (ID parameter) <CR>

CoordAddrMode <CR>

0x02 = 16-bit Short Address

0x03 = 64-bit Long Address

Channel (CH parameter) <CR>

SecurityUse <CR>

ACLEntry <CR>

SecurityFailure <CR>

SuperFrameSpec <CR> (2 bytes):

bit 15 - Association Permitted (MSB)

bit 14 - PAN Coordinator

bit 13 - Reserved

bit 12 - Battery Life Extension

bits 8-11 - Final CAP Slot

bits 4-7 - Superframe Order

bits 0-3 - Beacon Order

GtsPermit <CR>

RSSI <CR> (- RSSI is returned as -dBm)

TimeStamp <CR> (3 bytes)

<CR> (A carriage return <CR> is sent at the end of the AS command.

The Active Scan is capable of returning up to 5 PanDescriptors in a scan. The actual scan time on each channel is measured as $\text{Time} = [(2 \wedge (\text{SD Parameter})) * 15.36] \text{ ms}$. Total scan time is this time multiplied by the number of channels to be scanned (16 for the Xbee, 12 for the Xbee-PRO).

NOTE: Refer the scan table in the SD description to determine scan times. If using API Mode, no <CR>'s are returned in the response. Refer to the API Mode Operation section.

BD (Interface Data Rate) Command

<Serial Interfacing> The BD command is used to set and read the serial interface data rate used between the RF module and host. This parameter determines the rate at which serial data is sent to the module from the host. Modified interface data rates do not take effect until the CN (Exit AT Command Mode) command is issued and the system returns the 'OK' response.

When parameters 0-7 are sent to the module, the respective interface data rates are used (as shown in the table on the right).

The RF data rate is not affected by the BD parameter. If the interface data rate is set higher than the RF data rate, a flow control configuration may need to be implemented.

Non-standard Interface Data Rates:

Any value above 0x07 will be interpreted as an actual baud rate. When a value above 0x07 is sent, the closest interface data rate represented by the number is stored in the BD register. For example, a rate of 19200 bps can be set by sending the following command line "ATBD4B00". NOTE: When using Digi's X-CTU Software, non-standard interface data rates can only be set and read using the X-CTU 'Terminal' tab. Non-standard rates are not accessible through the 'Modem Configuration' tab.

When the BD command is sent with a non-standard interface data rate, the UART will adjust to accommodate the requested interface rate. In most cases, the clock resolution will cause the stored BD parameter to vary from the parameter that was sent (refer to the table below). Reading the BD command (send "ATBD" command without an associated parameter value) will return the value actually stored in the module's BD register.

Parameters Sent Versus Parameters Stored

BD Parameter Sent (HEX)	Interface Data Rate (bps)	BD Parameter Stored (HEX)
0	1200	0
4	19,200	4
7	115,200*	7
12C	300	12B
1C200	115,200	1B207

* The 115,200 baud rate setting is actually at 111,111 baud (-3.5% target UART speed).

AT Command: ATBD

Parameter Range: 0 – 7 (standard rates)
0x80–0x3D090 (non-standard rates up to 250 Kbps)

Parameter	Configuration (bps)
0	1200
1	2400
2	4800
3	9600
4	19200
5	38400
6	57600
7	115200

Default Parameter Value: 3

CA (CCA Threshold) Command

<RF Interfacing> CA command is used to set and read CCA (Clear Channel Assessment) thresholds.

Prior to transmitting a packet, a CCA is performed to detect energy on the transmit channel. If the detected energy is above the CCA Threshold, the RF module will not transmit the packet.

AT Command: ATCA

Parameter Range: 0 – 0x50 [–dBm]

Default Parameter Value: 0x2C
(–44 decimal dBm)

Minimum Firmware Version Required: v1.x80

CC (Command Sequence Character) Command

<AT Command Mode Options> The CC command is used to set and read the ASCII character used between guard times of the AT Command Mode Sequence (GT + CC + GT). This sequence enters the RF module into AT Command Mode so that data entering the module from the host is recognized as commands instead of payload.

The AT Command Sequence is explained further in the AT Command Mode section.

AT Command: ATCC

Parameter Range: 0 – 0xFF

Default Parameter Value: 0x2B (ASCII "+")

Related Command: GT (Guard Times)

CE (Coordinator Enable) Command

<Networking {Association}> The CE command is used to set and read the behavior (End Device vs. Coordinator) of the RF module.

AT Command: ATCE

Parameter Range: 0 – 1

Parameter	Configuration
0	End Device
1	Coordinator

Default Parameter Value: 0

Minimum Firmware Version Required: v1.x80

CH (Channel) Command

<Networking {Addressing}> The CH command is used to set/read the operating channel on which RF connections are made between RF modules. The channel is one of three addressing options available to the module. The other options are the PAN ID (ID command) and destination addresses (DL & DH commands).

In order for modules to communicate with each other, the modules must share the same channel number. Different channels can be used to prevent modules in one network from listening to transmissions of another. Adjacent channel rejection is 23 dB.

The module uses channel numbers of the 802.15.4 standard.

Center Frequency = $2.405 + (\text{CH} - 11d) * 5 \text{ MHz}$ (d = decimal)

AT Command: ATCH

Parameter Range: 0x0B – 0x1A (XBee)
0x0C – 0x17 (XBee-PRO)

Default Parameter Value: 0x0C (12 decimal)

Related Commands: ID (PAN ID), DL (Destination Address Low, DH (Destination Address High)

Refer to the XBee/XBee-PRO Addressing section for more information.

CN (Exit Command Mode) Command

<AT Command Mode Options> The CN command is used to explicitly exit the RF module from AT Command Mode.

AT Command: ATCN

CT (Command Mode Timeout) Command

<AT Command Mode Options> The CT command is used to set and read the amount of inactive time that elapses before the RF module automatically exits from AT Command Mode and returns to Idle Mode.

Use the CN (Exit Command Mode) command to exit AT Command Mode manually.

AT Command: ATCT

Parameter Range: 2 – 0xFFFF
[x 100 milliseconds]

Default Parameter Value: 0x64 (100 decimal (which equals 10 decimal seconds))

Number of bytes returned: 2

Related Command: CN (Exit Command Mode)

D0 - D4 (DIO Configuration) Commands

<I/O Settings> The D0, D1, D2, D3 and D4 commands are used to select/read the behavior of their respective AD/DIO lines (pins 20, 19, 18, 17 and 11 respectively).

Options include:

- Analog-to-digital converter
- Digital input
- Digital output

AT Commands:

ATD0, ATD1, ATD2, ATD3, ATD4

Parameter Range: 0 – 5

Parameter	Configuration
0	Disabled
1	n/a
2	ADC
3	DI
4	DO low
5	DO high

Default Parameter Value: 0

Minimum Firmware Version Required: 1.x.A0

D5 (DIO5 Configuration) Command

<I/O Settings> The D5 command is used to select/read the behavior of the DIO5 line (pin 15).

Options include:

- Associated Indicator (LED blinks when the module is associated)
- Analog-to-digital converter
- Digital input
- Digital output

AT Command: ATD5

Parameter Range: 0 – 5

Parameter	Configuration
0	Disabled
1	Associated Indicator
2	ADC
3	DI
4	DO low
5	DO high

Default Parameter Value: 1

Parameters 2–5 supported as of firmware version 1.x.A0

D6 (DIO6 Configuration) Command

<I/O Settings> The D6 command is used to select/read the behavior of the DIO6 line (pin 16).

Options include:

- RTS flow control
- Analog-to-digital converter
- Digital input
- Digital output

AT Command: ATD6

Parameter Range: 0 – 5

Parameter	Configuration
0	Disabled
1	RTS Flow Control
2	n/a
3	DI
4	DO low
5	DO high

Default Parameter Value: 0

Parameters 3–5 supported as of firmware version 1.x.A0

D7 (DIO7 Configuration) Command

<I/O Settings> The D7 command is used to select/read the behavior of the DIO7 line (pin 12). Options include:

- CTS flow control
- Analog-to-digital converter
- Digital input
- Digital output
- RS485 TX Enable (this output is 3V CMOS level, and is useful in a 3V CMOS to RS485 conversion circuit)

AT Command: ATD7

Parameter Range: 0 – 5

Parameter	Configuration
0	Disabled
1	CTS Flow Control
2	n/a
3	DI
4	DO low
5	DO high
6	RS485 TX Enable Low
7	RS485 TX Enable High

Default Parameter Value: 1

Parameters 3–7 supported as of firmware version 1.x.A0

D8 (DI8 Configuration) Command

<I/O Settings> The D8 command is used to select/read the behavior of the DI8 line (pin 9). This command enables configuring the pin to function as a digital input. This line is also used with Pin Sleep.

AT Command: ATD8

Parameter Range: 0 – 5

(1, 2, 4 & 5 n/a)

Parameter	Configuration
0	Disabled
3	DI

Default Parameter Value: 0

Minimum Firmware Version Required: 1.x.A0

DA (Force Disassociation) Command

<(Special)> The DA command is used to immediately disassociate an End Device from a Coordinator and reattempt to associate.

AT Command: ATDA

Minimum Firmware Version Required: v1.x.80

DB (Received Signal Strength) Command

<Diagnostics> DB parameter is used to read the received signal strength (in dBm) of the last RF packet received. Reported values are accurate between -40 dBm and the RF module's receiver sensitivity.

AT Command: ATDB

Parameter Range [read-only]:

0x17–0x5C (XBee), 0x24–0x64 (XBee-PRO)

Absolute values are reported. For example: 0x58 = -88 dBm (decimal). If no packets have been received (since last reset, power cycle or sleep event), "0" will be reported.

DH (Destination Address High) Command

<Networking {Addressing}> The DH command is used to set and read the upper 32 bits of the RF module's 64-bit destination address. When combined with the DL (Destination Address Low) parameter, it defines the destination address used for transmission.

An module will only communicate with other modules having the same channel (CH parameter), PAN ID (ID parameter) and destination address (DH + DL parameters).

AT Command: ATDH

Parameter Range: 0 – 0xFFFFFFFF

Default Parameter Value: 0

Related Commands: DL (Destination Address Low), CH (Channel), ID (PAN VID), MY (Source Address)

To transmit using a 16-bit address, set the DH parameter to zero and the DL parameter less than 0xFFFF. 0x000000000000FFFF (DL concatenated to DH) is the broadcast address for the PAN.

Refer to the XBee/XBee-PRO Addressing section for more information.

DL (Destination Address Low) Command

<Networking {Addressing}> The DL command is used to set and read the lower 32 bits of the RF module's 64-bit destination address. When combined with the DH (Destination Address High) parameter, it defines the destination address used for transmission.

A module will only communicate with other modules having the same channel (CH parameter), PAN ID (ID parameter) and destination address (DH + DL parameters).

To transmit using a 16-bit address, set the DH parameter to zero and the DL parameter less than 0xFFFF. 0x000000000000FFFF (DL concatenated to DH) is the broadcast address for the PAN.

Refer to the XBee/XBee-PRO Addressing section for more information.

AT Command: ATDL

Parameter Range: 0 - 0xFFFFFFFF

Default Parameter Value: 0

Related Commands: DH (Destination Address High), CH (Channel), ID (PAN VID), MY (Source Address)

DN (Destination Node) Command

<Networking {Identification}> The DN command is used to resolve a NI (Node Identifier) string to a physical address. The following events occur upon successful command execution:

1. DL and DH are set to the address of the module with the matching NI (Node Identifier).
2. 'OK' is returned.
3. RF module automatically exits AT Command Mode.

If there is no response from a modem within 200 msec or a parameter is not specified (left blank), the command is terminated and an 'ERROR' message is returned.

AT Command: ATDN

Parameter Range: 20-character ASCII String

Minimum Firmware Version Required: v1.x80

DP (Disassociation Cyclic Sleep Period) Command

<Sleep Mode (Low Power)>

NonBeacon Firmware

End Device - The DP command is used to set and read the time period of sleep for cyclic sleeping remotes that are configured for Association but are not associated to a Coordinator. (i.e. If a device is configured to associate, configured as a Cyclic Sleep remote, but does not find a Coordinator; it will sleep for DP time before reattempting association.) Maximum sleep period is 268 seconds (0x68B0). DP should be > 0 for NonBeacon systems.

AT Command: ATDP

Parameter Range: 1 - 0x68B0
[x 10 milliseconds]

Default Parameter Value: 0x3E8
(1000 decimal)

Related Commands: SM (Sleep Mode), SP (Cyclic Sleep Period), ST (Time before Sleep)

Minimum Firmware Version Required: v1.x80

EA (ACK Failures) Command

<Diagnostics> The EA command is used to reset and read the count of ACK (acknowledgement) failures. This parameter value increments when the module expires its transmission retries without receiving an ACK on a packet transmission. This count saturates at its maximum value.

Set the parameter to "0" to reset count.

AT Command: ATEA

Parameter Range: 0 - 0xFFFF

Minimum Firmware Version Required: v1.x80

EC (CCA Failures) Command

<Diagnostics> The EC command is used to read and reset the count of CCA (Clear Channel Assessment) failures. This parameter value increments when the RF module does not transmit a packet due to the detection of energy that is above the CCA threshold level (set with CA command). This count saturates at its maximum value.

Set the EC parameter to "0" to reset count.

AT Command: ATEC

Parameter Range: 0 – 0xFFFF

Related Command: CA (CCA Threshold)

Minimum Firmware Version Required: v1.x80

ED (Energy Scan) Command

<Networking {Association}> The ED command is used to send an "Energy Detect Scan". This parameter determines the length of scan on each channel. The maximal energy on each channel is returned and each value is followed by a carriage return. An additional carriage return is sent at the end of the command.

The values returned represent the detected energy level in units of -dBm. The actual scan time on each channel is measured as $\text{Time} = [(2 \wedge \text{ED PARAM}) * 15.36] \text{ ms}$.

AT Command: ATED

Parameter Range: 0 – 6

Related Command: SD (Scan Duration), SC (Scan Channel)

Minimum Firmware Version Required: v1.x80

Note: Total scan time is this time multiplied by the number of channels to be scanned. Also refer to the SD (Scan Duration) table. Use the SC (Scan Channel) command to choose which channels to scan.

EE (AES Encryption Enable) Command

<Networking {Security}> The EE command is used to set/read the parameter that disables/enables 128-bit AES encryption.

The XBee®/XBee-PRO® firmware uses the 802.15.4 Default Security protocol and uses AES encryption with a 128-bit key. AES encryption dictates that all modules in the network use the same key and the maximum RF packet size is 95 Bytes.

When encryption is enabled, the module will always use its 64-bit long address as the source address for RF packets. This does not affect how the MY (Source Address), DH (Destination Address High) and DL (Destination Address Low) parameters work

If MM (MAC Mode) > 0 and AP (API Enable) parameter > 0:

With encryption enabled and a 16-bit short address set, receiving modules will only be able to issue RX (Receive) 64-bit indicators. This is not an issue when MM = 0.

AT Command: ATEE

Parameter Range: 0 – 1

Parameter	Configuration
0	Disabled
1	Enabled

Default Parameter Value: 0

Related Commands: KY (Encryption Key), AP (API Enable), MM (MAC Mode)

Minimum Firmware Version Required: v1.xA0

If a module with a non-matching key detects RF data, but has an incorrect key: When encryption is enabled, non-encrypted RF packets received will be rejected and will not be sent out the UART.

Transparent Operation --> All RF packets are sent encrypted if the key is set.

API Operation --> Receive frames use an option bit to indicate that the packet was encrypted.

FP (Force Poll) Command

<Networking (Association)> The FP command is used to request indirect messages being held by a Coordinator.

AT Command: ATFP

Minimum Firmware Version Required: v1.x80

FR (Software Reset) Command

<Special> The FR command is used to force a software reset on the RF module. The reset simulates powering off and then on again the module.

AT Command: ATFR

Minimum Firmware Version Required: v1.x80

GT (Guard Times) Command

<AT Command Mode Options> GT Command is used to set the DI (data in from host) time-of-silence that surrounds the AT command sequence character (CC Command) of the AT Command Mode sequence (GT + CC + GT).

AT Command: ATGT

Parameter Range: 2 – 0x0CE4
[x 1 millisecond]

Default Parameter Value: 0x3E8
(1000 decimal)

The DI time-of-silence is used to prevent inadvertent entrance into AT Command Mode.

Related Command: CC (Command Sequence Character)

Refer to the Command Mode section for more information regarding the AT Command Mode Sequence.

HV (Hardware Version) Command

<Diagnostics> The HV command is used to read the hardware version of the RF module.

AT Command: ATHV

Parameter Range: 0 – 0xFFFF [Read-only]

Minimum Firmware Version Required: v1.x80

IA (I/O Input Address) Command

<I/O Settings {I/O Line Passing}> The IA command is used to bind a module output to a specific address. Outputs will only change if received from this address. The IA command can be used to set/read both 16 and 64-bit addresses.

AT Command: ATIA

Parameter Range: 0 – 0xFFFFFFFFFFFFFFFF

Default Parameter Value: 0xFFFFFFFFFFFFFFFF
(will not allow any received I/O packet to change outputs)

Setting all bytes to 0xFF will not allow the reception of any I/O packet to change outputs. Setting the IA address to 0xFFFF will cause the module to accept all I/O packets.

Minimum Firmware Version Required: v1.xA0

IC (DIO Change Detect) Command

<I/O Settings> Set/Read bitfield values for change detect monitoring. Each bit enables monitoring of DIO0 - DIO7 for changes.

AT Command: ATIC

Parameter Range: 0 – 0xFF [bitfield]

If detected, data is transmitted with DIO data only. Any samples queued waiting for transmission will be sent first.

Default Parameter Value: 0 (disabled)

Minimum Firmware Version Required: 1.xA0

Refer to the "ADC and Digital I/O Line Support" sections of the "RF Module Operations" chapter for more information.

ID (Pan ID) Command

<Networking {Addressing}> The ID command is used to set and read the PAN (Personal Area Network) ID of the RF module. Only modules with matching PAN IDs can communicate with each other. Unique PAN IDs enable control of which RF packets are received by a module.

AT Command: ATID

Parameter Range: 0 – 0xFFFF

Default Parameter Value: 0x3332
(13106 decimal)

Setting the ID parameter to 0xFFFF indicates a global transmission for all PANs. It does not indicate a global receive.

IO (Digital Output Level) Command

<I/O Settings> The IO command is used to set digital output levels. This allows DIO lines setup as outputs to be changed through Command Mode.

AT Command: ATIO

Parameter Range: 8-bit bitmap (where each bit represents the level of an I/O line that is setup as an output.)

Minimum Firmware Version Required: v1.xA0

IR (Sample Rate) Command

<I/O Settings> The IR command is used to set/read the sample rate. When set, the module will sample all enabled DIO/ADC lines at a specified interval. This command allows periodic reads of the ADC and DIO lines in a non-Sleep Mode setup. A sample rate which requires transmissions at a rate greater than once every 20ms is not recommended.

AT Command: ATIR

Parameter Range: 0 – 0xFFFF [x 1 msec] (cannot guarantee 1 ms timing when IT=1)

Default Parameter Value:0

Related Command: IT (Samples before TX)

Minimum Firmware Version Required: v1.xA0

Example: When IR = 0x14, the sample rate is 20 ms (or 50 Hz).

IS (Force Sample) Command

<I/O Settings> The IS command is used to force a read of all enabled DIO/ADC lines. The data is returned through the UART.

AT Command: ATIS

Parameter Range: 1 – 0xFF

Default Parameter Value:1

Minimum Firmware Version Required: v1.xA0

When operating in Transparent Mode (AP=0), the data is returned in the following format:

All bytes are converted to ASCII:
 number of samples<CR>
 channel mask<CR>
 DIO data<CR> (If DIO lines are enabled<CR>
 ADC channel Data<cr> <-This will repeat for every enabled ADC channel<CR>
 <CR> (end of data noted by extra <CR>)

When operating in API mode (AP > 0), the command will immediately return an 'OK' response. The data will follow in the normal API format for DIO data.

IT (Samples before TX) Command

<I/O Settings> The IT command is used to set/read the number of DIO and ADC samples to collect before transmitting data.

AT Command: ATIT

Parameter Range: 1 – 0xFF

Default Parameter Value:1

Minimum Firmware Version Required: v1.xA0

One ADC sample is considered complete when all enabled ADC channels have been read. The module can buffer up to 93 Bytes of sample data.

Since the module uses a 10-bit A/D converter, each sample uses two Bytes. This leads to a maximum buffer size of 46 samples or IT=0x2E.

When Sleep Modes are enabled and IR (Sample Rate) is set, the module will remain awake until IT samples have been collected.

IU (I/O Output Enable) Command

<I/O Settings> The IU command is used to disable/enable I/O UART output. When enabled (IU = 1), received I/O line data packets are sent out the UART. The data is sent using an API frame regardless of the current AP parameter value.

AT Command: ATIU

Parameter Range: 0 – 1

Parameter	Configuration
0	Disabled – Received I/O line data packets will be NOT sent out UART.
1	Enabled – Received I/O line data will be sent out UART

Default Parameter Value: 1

Minimum Firmware Version Required: 1.xA0

KY (AES Encryption Key) Command

<Networking {Security}> The KY command is used to set the 128-bit AES (Advanced Encryption Standard) key for encrypting/decrypting data. Once set, the key cannot be read out of the module by any means.

The entire payload of the packet is encrypted using the key and the CRC is computed across the ciphertext. When encryption is enabled, each packet carries an additional 16 Bytes to convey the random CBC Initialization Vector (IV) to the receiver(s). The KY value may be "0" or any 128-bit value. Any other value, including entering KY by itself with no parameters, is invalid. All ATKY entries (valid or not) are received with a returned 'OK'.

A module with the wrong key (or no key) will receive encrypted data, but the data driven out the serial port will be meaningless. A module with a key and encryption enabled will receive data sent from a module without a key and the correct unencrypted data output will be sent out the serial port. Because CBC mode is utilized, repetitive data appears differently in different transmissions due to the randomly-generated IV.

When queried, the system will return an 'OK' message and the value of the key will not be returned.

AT Command: ATKY

Parameter Range: 0 – (any 16-Byte value)

Default Parameter Value: 0

Related Command: EE (Encryption Enable)

Minimum Firmware Version Required: v1.xA0

M0 (PWM0 Output Level) Command

<I/O Settings> The M0 command is used to set/read the output level of the PWM0 line (pin 6).

Before setting the line as an output:

1. Enable PWM0 output (P0 = 2)
2. Apply settings (use CN or AC)

The PWM period is 64 µsec and there are 0x03FF (1023 decimal) steps within this period. When M0 = 0 (0% PWM), 0x01FF (50% PWM), 0x03FF (100% PWM), etc.

AT Command: ATM0

Parameter Range: 0 – 0x03FF [steps]

Default Parameter Value: 0

Related Commands: P0 (PWM0 Enable), AC (Apply Changes), CN (Exit Command Mode)

Minimum Firmware Version Required: v1.xA0

M1 (PWM1 Output Level) Command

<I/O Settings> The M1 command is used to set/read the output level of the PWM1 line (pin 7).

Before setting the line as an output:

1. Enable PWM1 output (P1 = 2)
2. Apply settings (use CN or AC)

AT Command: ATM1

Parameter Range: 0 – 0x03FF

Default Parameter Value: 0

Related Commands: P1 (PWM1 Enable), AC (Apply Changes), CN (Exit Command Mode)

Minimum Firmware Version Required: v1.xA0

MM (MAC Mode) Command

<Networking {Addressing}> The MM command is used to set and read the MAC Mode value. The MM command disables/enables the use of a Digi header contained in the 802.15.4 RF packet. By default (MM = 0), Digi Mode is enabled and the module adds an extra header to the data portion of the 802.15.4 packet. This enables the following features:

- ND and DN command support
- Duplicate packet detection when using ACKs
- "RR command
- "DIO/AIO sampling support

The MM command allows users to turn off the use of the extra header. Modes 1 and 2 are strict 802.15.4 modes. If the Digi header is disabled, ND and DN parameters are also disabled.

Note: When MM=0 or 3, application and CCA failure retries are not supported.

AT Command: ATMM

Parameter Range: 0 – 3

Parameter	Configuration
0	Digi Mode (802.15.4 + Digi header)
1	802.15.4 (no ACKs)
2	802.15.4 (with ACKs)
3	Digi Mode (no ACKs)

Default Parameter Value: 0

Related Commands: ND (Node Discover), DN (Destination Node)

Minimum Firmware Version Required: v1.x80

MY (16-bit Source Address) Command

<Networking {Addressing}> The MY command is used to set and read the 16-bit source address of the RF module.

By setting MY to 0xFFFF, the reception of RF packets having a 16-bit address is disabled. The 64-bit address is the module's serial number and is always enabled.

AT Command: ATMY

Parameter Range: 0 – 0xFFFF

Default Parameter Value: 0

Related Commands: DH (Destination Address High), DL (Destination Address Low), CH (Channel), ID (PAN ID)

NB (Parity) Command

<Serial Interfacing> The NB command is used to select/read the parity settings of the RF module for UART communications.

Note: the module does not actually calculate and check the parity; it only interfaces with devices at the configured parity and stop bit settings.

AT Command: ATNB

Parameter Range: 0 – 4

Parameter	Configuration
0	8-bit no parity
1	8-bit even
2	8-bit odd
3	8-bit mark
4	8-bit space

Default Parameter Value: 0

Number of bytes returned: 1

ND (Node Discover) Command

<Networking {Identification}> The ND command is used to discover and report all modules on its current operating channel (CH parameter) and PAN ID (ID parameter). ND also accepts an NI (Node Identifier) value as a parameter. In this case, only a module matching the supplied identifier will respond.

ND uses a 64-bit long address when sending and responding to an ND request. The ND command causes a module to transmit a globally addressed ND command packet. The amount of time allowed for responses is determined by the NT (Node Discover Time) parameter.

In AT Command mode, command completion is designated by a carriage return (0x0D). Since two carriage returns end a command response, the application will receive three carriage returns at the end of the command. If no responses are received, the application should only receive one carriage return. When in API mode, the application should receive a frame (with no data) and status (set to 'OK') at the end of the command. When the ND command packet is received, the remote sets up a random time delay (up to 2.2 sec) before replying as follows:

Node Discover Response (AT command mode format - Transparent operation):

MY (Source Address) value<CR>
 SH (Serial Number High) value<CR>
 SL (Serial Number Low) value<CR>
 DB (Received Signal Strength) value<CR>
 NI (Node Identifier) value<CR>
 <CR> (This is part of the response and not the end of command indicator.)

Node Discover Response (API format - data is binary (except for NI)):

2 bytes for MY (Source Address) value
 4 bytes for SH (Serial Number High) value
 4 bytes for SL (Serial Number Low) value
 1 byte for DB (Received Signal Strength) value
 NULL-terminated string for NI (Node Identifier) value (max 20 bytes w/out NULL terminator)

AT Command: ATND

Range: optional 20-character NI value

Related Commands: CH (Channel), ID (Pan ID), MY (Source Address), SH (Serial Number High), SL (Serial Number Low), NI (Node Identifier), NT (Node Discover Time)

Minimum Firmware Version Required: v1.x80

NI (Node Identifier) Command

<Networking {Identification}> The NI command is used to set and read a string for identifying a particular node.

Rules:

- Register only accepts printable ASCII data.
- A string can not start with a space.
- A carriage return ends command
- Command will automatically end when maximum bytes for the string have been entered.

This string is returned as part of the ND (Node Discover) command. This identifier is also used with the DN (Destination Node) command.

AT Command: ATNI

Parameter Range: 20-character ASCII string

Related Commands: ND (Node Discover), DN (Destination Node)

Minimum Firmware Version Required: v1.x80

NO (Node Discover Options) Command

<Networking {Identification}> The NO command is used to suppress/include a self-response to Node Discover commands. When NO=1 a module doing a Node Discover will include a response entry for itself.

AT Command: ATNO

Parameter Range: "0-1

Related Commands: ND (Node Discover), DN (Destination Node)

Minimum Firmware Version Required: v1.xC5

NT (Node Discover Time) Command

<Networking {Identification}> The NT command is used to set the amount of time a base node will wait for responses from other nodes when using the ND (Node Discover) command. The NT value is transmitted with the ND command.

Remote nodes will set up a random hold-off time based on this time. The remotes will adjust this time down by 250 ms to give each node the ability to respond before the base ends the command. Once the ND command has ended, any response received on the base will be discarded.

AT Command: ATNT

Parameter Range: 0x01 – 0xFC
[x 100 msec]

Default: 0x19 (2.5 decimal seconds)

Related Commands: ND (Node Discover)

Minimum Firmware Version Required: 1.xA0

P0 (PWM0 Configuration) Command

<I/O Setting {I/O Line Passing}> The P0 command is used to select/read the function for PWM0 (Pulse Width Modulation output 0). This command enables the option of translating incoming data to a PWM so that the output can be translated back into analog form.

With the IA (I/O Input Address) parameter correctly set, AD0 values can automatically be passed to PWM0.

AT Command: ATP0

The second character in the command is the number zero ("0"), not the letter "O".

Parameter Range: 0 – 2

Parameter	Configuration
0	Disabled
1	RSSI
2	PWM0 Output

Default Parameter Value: 1

P1 (PWM1 Configuration) Command

<I/O Setting {I/O Line Passing}> The P1 command is used to select/read the function for PWM1 (Pulse Width Modulation output 1). This command enables the option of translating incoming data to a PWM so that the output can be translated back into analog form.

With the IA (I/O Input Address) parameter correctly set, AD1 values can automatically be passed to PWM1.

AT Command: ATP1

Parameter Range: 0 – 2

Parameter	Configuration
0	Disabled
1	RSSI
2	PWM1 Output

Default Parameter Value: 0

Minimum Firmware Version Required: v1.xA0

PL (Power Level) Command

<RF Interfacing> The PL command is used to select and read the power level at which the RF module transmits conducted power.

When operating in Europe, XBee-PRO 802.15.4 modules must operate at or below a transmit power output level of 10dBm. Customers have 2 choices for transmitting at or below 10dBm:

- Order the standard XBee-PRO module and change the PL command to "0" (10dBm),
- Order the International variant of the XBee-PRO module, which has a maximum transmit output power of 10dBm.

AT Command: ATPL

Parameter Range: 0 – 4

Parameter	XBee	XBee-PRO	XBee-PRO International variant
0	-10 dBm	10 dBm	PL=4: 10 dBm
1	-6 dBm	12 dBm	PL=3: 8 dBm
2	-4 dBm	14 dBm	PL=2: 2 dBm
3	-2 dBm	16 dBm	PL=1: -3 dBm
4	0 dBm	18 dBm	PL=0: -3 dBm

Default Parameter Value: 4

PR (Pull-up Resistor) Command

<Serial Interfacing> The PR command is used to set and read the bit field that is used to configure internal the pull-up resistor status for I/O lines. "1" specifies the pull-up resistor is enabled. "0" specifies no pull up.

bit 0 - AD4/DIO4 (pin 11)
 bit 1 - AD3/DIO3 (pin 17)
 bit 2 - AD2/DIO2 (pin 18)
 bit 3 - AD1/DIO1 (pin 19)
 bit 4 - AD0/DIO0 (pin 20)
 bit 5 - AD6/DIO6 (pin 16)
 bit 6 - DI8 (pin 9)
 bit 7 - DIN/CONFIG (pin 3)

For example: Sending the command "ATPR 6F" will turn bits 0, 1, 2, 3, 5 and 6 ON; and bits 4 & 7 will be turned OFF. (The binary equivalent of "0x6F" is "01101111". Note that 'bit 0' is the last digit in the bitfield.

AT Command: ATPR

Parameter Range: 0 – 0xFF

Default Parameter Value: 0xFF
 (all pull-up resistors are enabled)

Minimum Firmware Version Required: v1.x80

PT (PWM Output Timeout) Command

<I/O Settings {I/O Line Passing}> The PT command is used to set/read the output timeout value for both PWM outputs.

When PWM is set to a non-zero value: Due to I/O line passing, a time is started which when expired will set the PWM output to zero. The timer is reset when a valid I/O packet is received.

AT Command: ATPT

Parameter Range: 0 – 0xFF [x 100 msec]

Default Parameter Value: 0xFF

Minimum Firmware Version Required: 1.xA0

RE (Restore Defaults) Command

<(Special)> The RE command is used to restore all configurable parameters to their factory default settings. The RE command does not write restored values to non-volatile (persistent) memory. Issue the WR (Write) command subsequent to issuing the RE command to save restored parameter values to non-volatile memory.

AT Command: ATRE

RN (Random Delay Slots) Command

<Networking & Security> The RN command is used to set and read the minimum value of the back-off exponent in the CSMA-CA algorithm. The CSMA-CA algorithm was engineered for collision avoidance (random delays are inserted to prevent data loss caused by data collisions).

If RN = 0, collision avoidance is disabled during the first iteration of the algorithm (802.15.4 - macMinBE).

CSMA-CA stands for "Carrier Sense Multiple Access - Collision Avoidance". Unlike CSMA-CD (reacts to network transmissions after collisions have been detected), CSMA-CA acts to prevent data collisions before they occur. As soon as a module receives a packet that is to be transmitted, it checks if the channel is clear (no other module is transmitting). If the channel is clear, the packet is sent over-the-air. If the channel is not clear, the module waits for a randomly selected period of time, then checks again to see if the channel is clear. After a time, the process ends and the data is lost.

AT Command: ATRN

Parameter Range: 0 – 3 [exponent]

Default Parameter Value: 0

RO (Packetization Timeout) Command

<Serial Interfacing> RO command is used to set and read the number of character times of inter-character delay required before transmission.

RF transmission commences when data is detected in the DI (data in from host) buffer and RO character times of silence are detected on the UART receive lines (after receiving at least 1 byte).

RF transmission will also commence after 100 Bytes (maximum packet size) are received in the DI buffer.

Set the RO parameter to '0' to transmit characters as they arrive instead of buffering them into one RF packet.

AT Command: ATRO

Parameter Range: 0 – 0xFF
[x character times]

Default Parameter Value: 3

RP (RSSI PWM Timer) Command

<I/O Settings {I/O Line Passing}> The RP command is used to enable PWM (Pulse Width Modulation) output on the RF module. The output is calibrated to show the level a received RF signal is above the sensitivity level of the module. The PWM pulses vary from 24 to 100%. Zero percent means PWM output is inactive. One to 24% percent means the received RF signal is at or below the published sensitivity level of the module. The following table shows levels above sensitivity and PWM values.

The total period of the PWM output is 64 μ s. Because there are 445 steps in the PWM output, the minimum step size is 144 ns.

PWM Percentages

dB above Sensitivity	PWM percentage (high period / total period)
10	41%
20	58%
30	75%

A non-zero value defines the time that the PWM output will be active with the RSSI value of the last received RF packet. After the set time when no RF packets are received, the PWM output will be set low (0 percent PWM) until another RF packet is received. The PWM output will also be set low at power-up until the first RF packet is received. A parameter value of 0xFF permanently enables the PWM output and it will always reflect the value of the last received RF packet.

AT Command: ATPR

Parameter Range: 0 – 0xFF
[x 100 msec]

Default Parameter Value: 0x28 (40 decimal)

RR (XBee Retries) Command

<Networking {Addressing}> The RR command is used set/read the maximum number of retries the module will execute in addition to the 3 retries provided by the 802.15.4 MAC. For each XBee retry, the 802.15.4 MAC can execute up to 3 retries.

This values does not need to be set on all modules for retries to work. If retries are enabled, the transmitting module will set a bit in the Digi RF Packet header which requests the receiving module to send an ACK (acknowledgement). If the transmitting module does not receive an ACK within 200 msec, it will re-send the packet within a random period up to 48 msec. Each XBee retry can potentially result in the MAC sending the packet 4 times (1 try plus 3 retries). Note that retries are not attempted for packets that are purged when transmitting with a Cyclic Sleep Coordinator.

AT Command: ATRR

Parameter Range: 0 – 6

Default: 0

Minimum Firmware Version Required: 1.xA0

SC (Scan Channels) Command

<Networking {Association}> The SC command is used to set and read the list of channels to scan for all Active and Energy Scans as a bit field.

This affects scans initiated in command mode [AS (Active Scan) and ED (Energy Scan) commands] and during End Device Association and Coordinator startup.

bit 0 - 0x0B	bit 4 - 0x0F	bit 8 - 0x13	bit 12 - 0x17
bit 1 - 0x0C	bit 5 - 0x10	bit 9 - 0x14	bit 13 - 0x18
bit 2 - 0x0D	bit 6 - 0x11	bit 10 - 0x15	bit 14 - 0x19
bit 3 - 0x0E	bit 7 - 0x12	bit 11 - 0x16	bit 15 - 0x1A

AT Command: ATSC

Parameter Range: 1-0xFFFF [Bitfield]
(bits 0, 14, 15 are not allowed when using the XBee-PRO)

Default Parameter Value: 0x1FFE (all XBee-PRO channels)

Related Commands: ED (Energy Scan), SD (Scan Duration)

Minimum Firmware Version Required: v1.x80

SD (Scan Duration) Command

<Networking {Association}> The SD command is used to set and read the exponent value that determines the duration (in time) of a scan.

End Device (Duration of Active Scan during Association) - In a Beacon system, set SD = BE of the Coordinator. SD must be set at least to the highest BE parameter of any Beaconsing Coordinator with which an End Device or Coordinator wish to discover.

Coordinator - If the 'ReassignPANID' option is set on the Coordinator [refer to A2 parameter], the SD parameter determines the length of time the Coordinator will scan channels to locate existing PANs. If the 'ReassignChannel' option is set, SD determines how long the Coordinator will perform an Energy Scan to determine which channel it will operate on.

Scan Time is measured as ((# of Channels to Scan) * (2 ^ SD) * 15.36ms). The number of channels to scan is set by the SC command. The XBee RF Module can scan up to 16 channels (SC = 0xFFFF). The XBee PRO RF Module can scan up to 12 channels (SC = 0x1FFE).

Examples: Values below show results for a 12-channel scan

If SD = 0, time = 0.18 sec	SD = 8, time = 47.19 sec
SD = 2, time = 0.74 sec	SD = 10, time = 3.15 min
SD = 4, time = 2.95 sec	SD = 12, time = 12.58 min
SD = 6, time = 11.80 sec	SD = 14, time = 50.33 min

AT Command: ATSD

Parameter Range: 0 - 0x0F

Default Parameter Value: 4

Related Commands: ED (Energy Scan), SC (Scan Channel)

Minimum Firmware Version Required: v1.x80

SH (Serial Number High) Command

<Diagnostics> The SH command is used to read the high 32 bits of the RF module's unique IEEE 64-bit address.

The module serial number is set at the factory and is read-only.

AT Command: ATSH

Parameter Range: 0 - 0xFFFFFFFF [read-only]

Related Commands: SL (Serial Number Low), MY (Source Address)

SL (Serial Number Low) Command

<Diagnostics> The SL command is used to read the low 32 bits of the RF module's unique IEEE 64-bit address.

The module serial number is set at the factory and is read-only.

AT Command: ATSL

Parameter Range: 0 - 0xFFFFFFFF [read-only]

Related Commands: SH (Serial Number High), MY (Source Address)

SM (Sleep Mode) Command

<Sleep Mode (Low Power)> The SM command is used to set and read Sleep Mode settings. By default, Sleep Modes are disabled (SM = 0) and the RF module remains in Idle/Receive Mode. When in this state, the module is constantly ready to respond to either serial or RF activity.

* The Sleep Coordinator option (SM=6) only exists for backwards compatibility with firmware version 1.x06 only. In all other cases, use the CE command to enable a Coordinator.

AT Command: ATSM

Parameter Range: 0 – 6

Parameter	Configuration
0	Disabled
1	Pin Hibernate
2	Pin Doze
3	(reserved)
4	Cyclic Sleep Remote
5	Cyclic Sleep Remote (with Pin Wake-up)
6	Sleep Coordinator*

Default Parameter Value: 0

SO (Sleep Mode Command)

Sleep (Low Power) Sleep Options Set/Read the sleep mode options.

Bit 0 - Poll wakeup disable

- 0 - Normal operations. A module configured for cyclic sleep will poll for data on waking.
- 1 - Disable wakeup poll. A module configured for cyclic sleep will not poll for data on waking.

Bit 1 - ADC/DIO wakeup sampling disable.

- 0 - Normal operations. A module configured in a sleep mode with ADC/DIO sampling enabled will automatically perform a sampling on wakeup.
- 1 - Suppress sample on wakeup. A module configured in a sleep mode with ADC/DIO sampling enabled will not automatically sample on wakeup.

AT Command: ATSO

Parameter Range: 0–4

Default Parameter Value:

Related Commands: SM (Sleep Mode), ST (Time before Sleep), DP (Disassociation Cyclic Sleep Period, BE (Beacon Order)

SP (Cyclic Sleep Period) Command

<Sleep Mode (Low Power)> The SP command is used to set and read the duration of time in which a remote RF module sleeps. After the cyclic sleep period is over, the module wakes and checks for data. If data is not present, the module goes back to sleep. The maximum sleep period is 268 seconds (SP = 0x68B0).

The SP parameter is only valid if the module is configured to operate in Cyclic Sleep (SM = 4-6). Coordinator and End Device SP values should always be equal.

To send Direct Messages, set SP = 0.

NonBeacon Firmware

End Device - SP determines the sleep period for cyclic sleeping remotes. Maximum sleep period is 268 seconds (0x68B0).

Coordinator - If non-zero, SP determines the time to hold an indirect message before discarding it. A Coordinator will discard indirect messages after a period of (2.5 * SP).

AT Command: ATSP

Parameter Range: NonBeacon Firmware:
0–0x68B0 [x 10 milliseconds]

Default Parameter Value:

Related Commands: SM (Sleep Mode), ST (Time before Sleep), DP (Disassociation Cyclic Sleep Period, BE (Beacon Order)

ST (Time before Sleep) Command

<Sleep Mode (Low Power)> The ST command is used to set and read the period of inactivity (no serial or RF data is sent or received) before activating Sleep Mode.

NonBeacon Firmware

Set/Read time period of inactivity (no serial or RF data is sent or received) before activating Sleep Mode. ST parameter is only valid with Cyclic Sleep settings (SM = 4 - 5).

Coordinator and End Device ST values must be equal.

AT Command: ATST

Parameter Range:	NonBeacon Firmware: 1 – 0xFFFF [x 1 millisecond]

Default Parameter Value:

Related Commands: SM (Sleep Mode), ST (Time before Sleep)



T0 - T7 ((D0-D7) Output Timeout) Command

<I/O Settings {I/O Line Passing}> The T0, T1, T2, T3, T4, T5, T6 and T7 commands are used to set/read output timeout values for the lines that correspond with the D0 - D7 parameters. When output is set (due to I/O line passing) to a non-default level, a timer is started which when expired, will set the output to its default level. The timer is reset when a valid I/O packet is received. The Tn parameter defines the permissible amount of time to stay in a non-default (active) state. If Tn = 0, Output Timeout is disabled (output levels are held indefinitely).

AT Commands: ATT0 – ATT7

Parameter Range: 0 – 0xFF [x 100 msec]

Default Parameter Value: 0xFF

Minimum Firmware Version Required: v1.xA0

VL (Firmware Version - Verbose)

<Diagnostics> The VL command is used to read detailed version information about the RF module. The information includes: application build date; MAC, PHY and bootloader versions; and build dates. This command was removed from firmware 1xC9 and later versions.

AT Command: ATVL

Parameter Range: 0 – 0xFF
[x 100 milliseconds]

Default Parameter Value: 0x28 (40 decimal)

Minimum Firmware Version Required: v1.x80 – v1.xC8

VR (Firmware Version) Command

<Diagnostics> The VR command is used to read which firmware version is stored in the module.

XBee version numbers will have four significant

digits. The reported number will show three or four numbers and is stated in hexadecimal notation. A version can be reported as "ABC" or "ABCD". Digits ABC are the main release number and D is the revision number from the main release. "D" is not required and if it is not present, a zero is assumed for D. "B" is a variant designator. The following variants exist:

- "0" = Non-Beacon Enabled 802.15.4 Code
- "1" = Beacon Enabled 802.15.4 Code

AT Command: ATVR

Parameter Range: 0 – 0xFFFF [read only]

WR (Write) Command

<(Special)> The WR command is used to write configurable parameters to the RF module's non-volatile memory. Parameter values remain in the module's memory until overwritten by subsequent use of the WR Command.

AT Command: ATWR

If changes are made without writing them to non-volatile memory, the module reverts back to previously saved parameters the next time the module is powered-on.

NOTE: Once the WR command is sent to the module, no additional characters should be sent until after the "OK/r" response is received.

API Operation

By default, XBee®/XBee-PRO® RF Modules act as a serial line replacement (Transparent Operation) - all UART data received through the DI pin is queued up for RF transmission. When the module receives an RF packet, the data is sent out the DO pin with no additional information.

Inherent to Transparent Operation are the following behaviors:

- If module parameter registers are to be set or queried, a special operation is required for transitioning the module into Command Mode.
- In point-to-multipoint systems, the application must send extra information so that the receiving module(s) can distinguish between data coming from different remotes.

As an alternative to the default Transparent Operation, API (Application Programming Interface) Operations are available. API operation requires that communication with the module be done through a structured interface (data is communicated in frames in a defined order). The API specifies how commands, command responses and module status messages are sent and received from the module using a UART Data Frame.

API Frame Specifications

Two API modes are supported and both can be enabled using the AP (API Enable) command. Use the following AP parameter values to configure the module to operate in a particular mode:

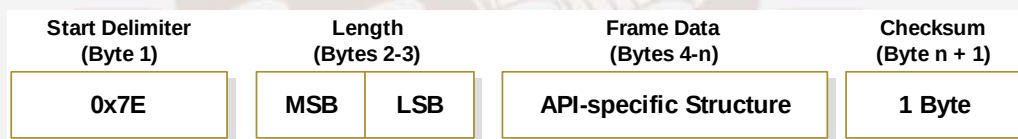
- AP = 0 (default): Transparent Operation (UART Serial line replacement)
API modes are disabled.
- AP = 1: API Operation
- AP = 2: API Operation (with escaped characters)

Any data received prior to the start delimiter is silently discarded. If the frame is not received correctly or if the checksum fails, the data is silently discarded.

API Operation (AP parameter = 1)

When this API mode is enabled (AP = 1), the UART data frame structure is defined as follows:

Figure 3-01. UART Data Frame Structure:

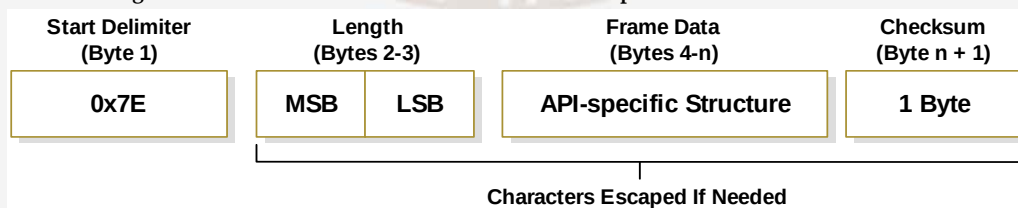


MSB = Most Significant Byte, LSB = Least Significant Byte

API Operation - with Escape Characters (AP parameter = 2)

When this API mode is enabled (AP = 2), the UART data frame structure is defined as follows:

Figure 3-02. UART Data Frame Structure - with escape control characters:



MSB = Most Significant Byte, LSB = Least Significant Byte

Escape characters. When sending or receiving a UART data frame, specific data values must be escaped (flagged) so they do not interfere with the UART or UART data frame operation. To escape an interfering data byte, insert 0x7D and follow it with the byte to be escaped XOR'd with 0x20.

Data bytes that need to be escaped:

- 0x7E – Frame Delimiter
- 0x7D – Escape
- 0x11 – XON
- 0x13 – XOFF

Example - Raw UART Data Frame (before escaping interfering bytes):

0x7E 0x00 0x02 0x23 0x11 0xCB

0x11 needs to be escaped which results in the following frame:

0x7E 0x00 0x02 0x23 0x7D 0x31 0xCB

Note: In the above example, the length of the raw data (excluding the checksum) is 0x0002 and the checksum of the non-escaped data (excluding frame delimiter and length) is calculated as:
 $0xFF - (0x23 + 0x11) = (0xFF - 0x34) = 0xCB$.

Checksum

To test data integrity, a checksum is calculated and verified on non-escaped data.

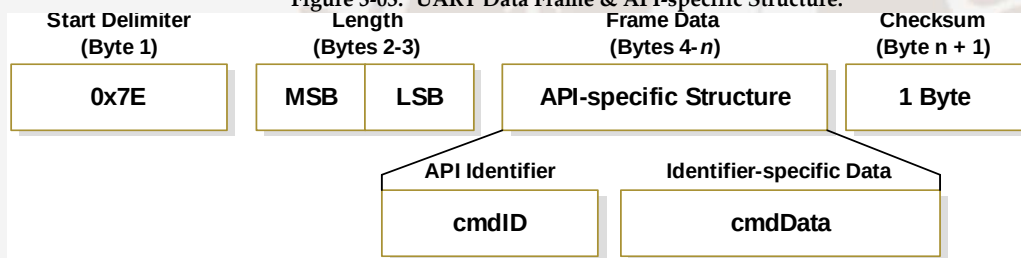
To calculate: Not including frame delimiters and length, add all bytes keeping only the lowest 8 bits of the result and subtract from 0xFF.

To verify: Add all bytes (include checksum, but not the delimiter and length). If the checksum is correct, the sum will equal 0xFF.

API Types

Frame data of the UART data frame forms an API-specific structure as follows:

Figure 3-03. UART Data Frame & API-specific Structure:



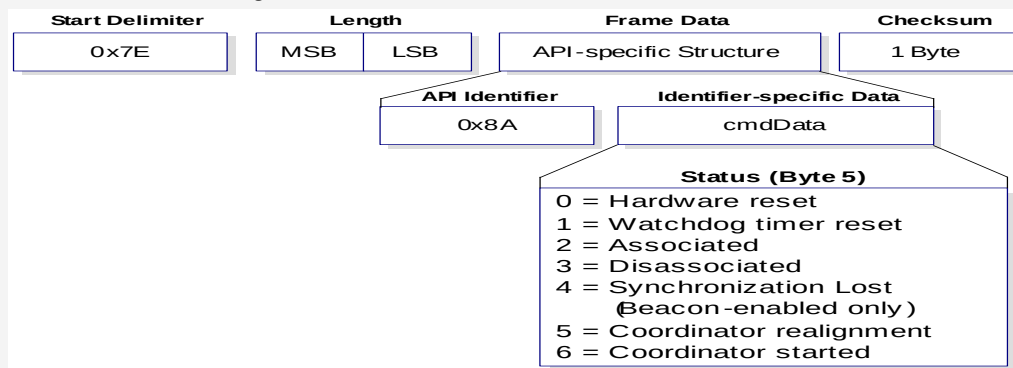
The cmdID frame (API-identifier) indicates which API messages will be contained in the cmdData frame (Identifier-specific data). Refer to the sections that follow for more information regarding the supported API types. Note that multi-byte values are sent big endian.

Modem Status

API Identifier: 0x8A

RF module status messages are sent from the module in response to specific conditions.

Figure 3-04. Modem Status Frames



AT Command

API Identifier Value: 0x08

The "AT Command" API type allows for module parameters to be queried or set. When using this command ID, new parameter values are applied immediately. This includes any register set with the "AT Command - Queue Parameter Value" (0x09) API type.

Figure 3-05. AT Command Frames

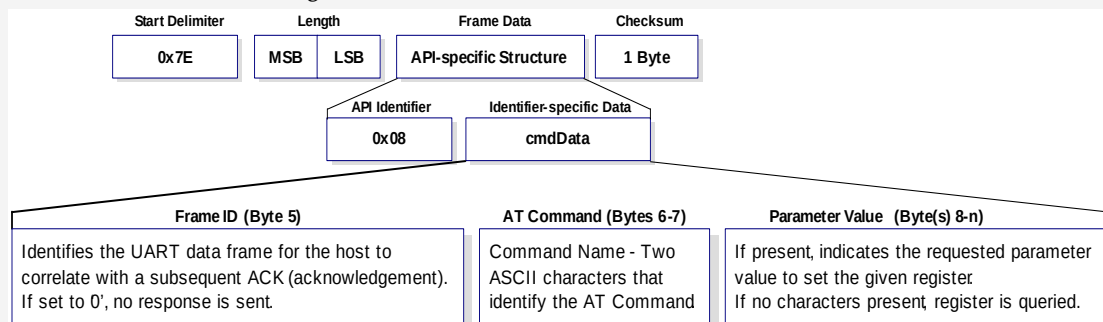


Figure 3-06. Example: API frames when reading the DL parameter value of the module.

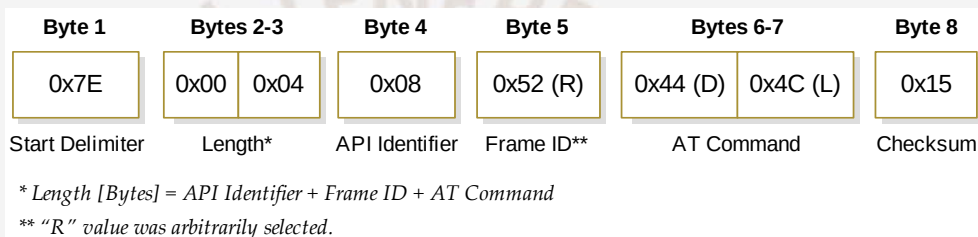
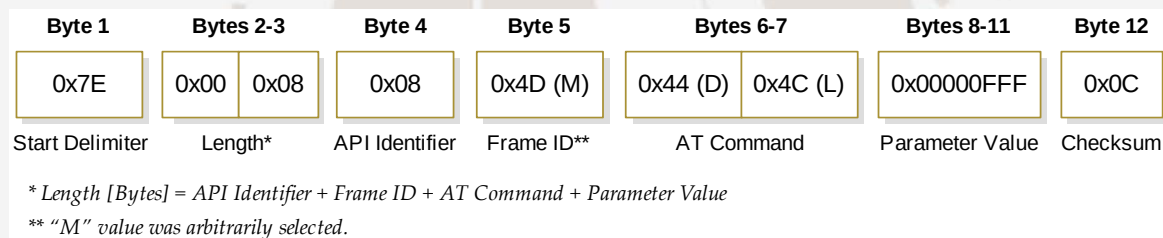


Figure 3-07. Example: API frames when modifying the DL parameter value of the module.



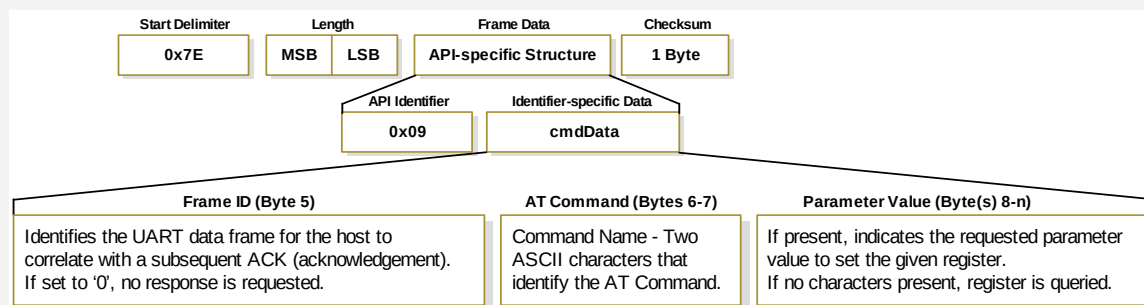
AT Command - Queue Parameter Value

API Identifier Value: 0x09

This API type allows module parameters to be queried or set. In contrast to the "AT Command" API type, new parameter values are queued and not applied until either the "AT Command" (0x08) API type or the AC (Apply Changes) command is issued. Register queries (reading parameter values) are returned immediately.

Figure 3-08. AT Command Frames

(Note that frames are identical to the "AT Command" API type except for the API identifier.)



AT Command Response

API Identifier Value: 0x88

Response to previous command.

In response to an AT Command message, the module will send an AT Command Response message. Some commands will send back multiple frames (for example, the ND (Node Discover) and AS (Active Scan) commands). These commands will end by sending a frame with a status of ATCMD_OK and no cmdData.

Figure 3-09. AT Command Response Frames.

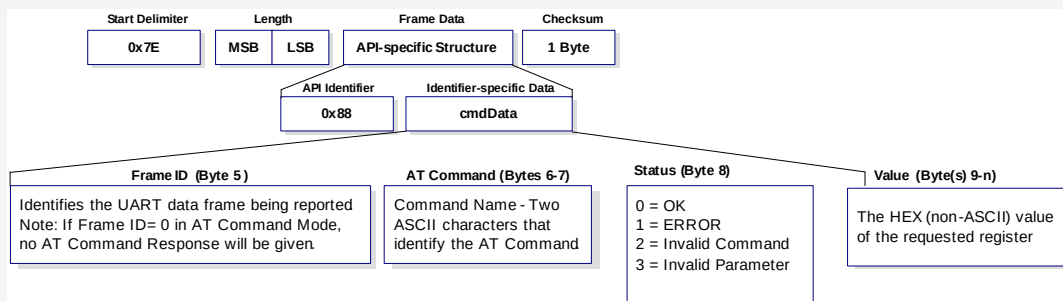
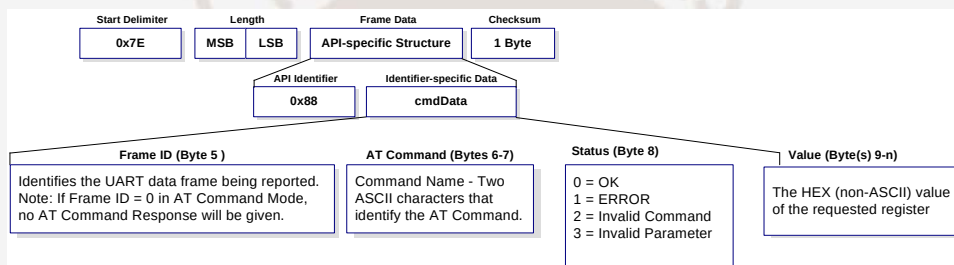


Figure 3-10. AT Command Response Frames.

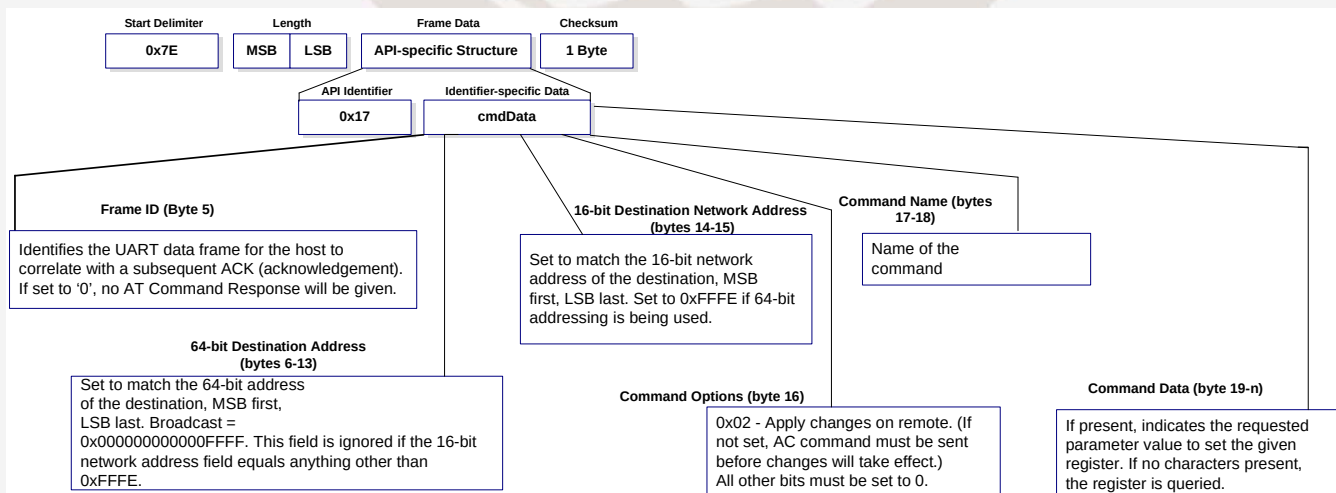


Remote AT Command Request

API Identifier Value: 0x17

Allows for module parameter registers on a remote device to be queried or set

Figure 3-11. Remote AT Command Request

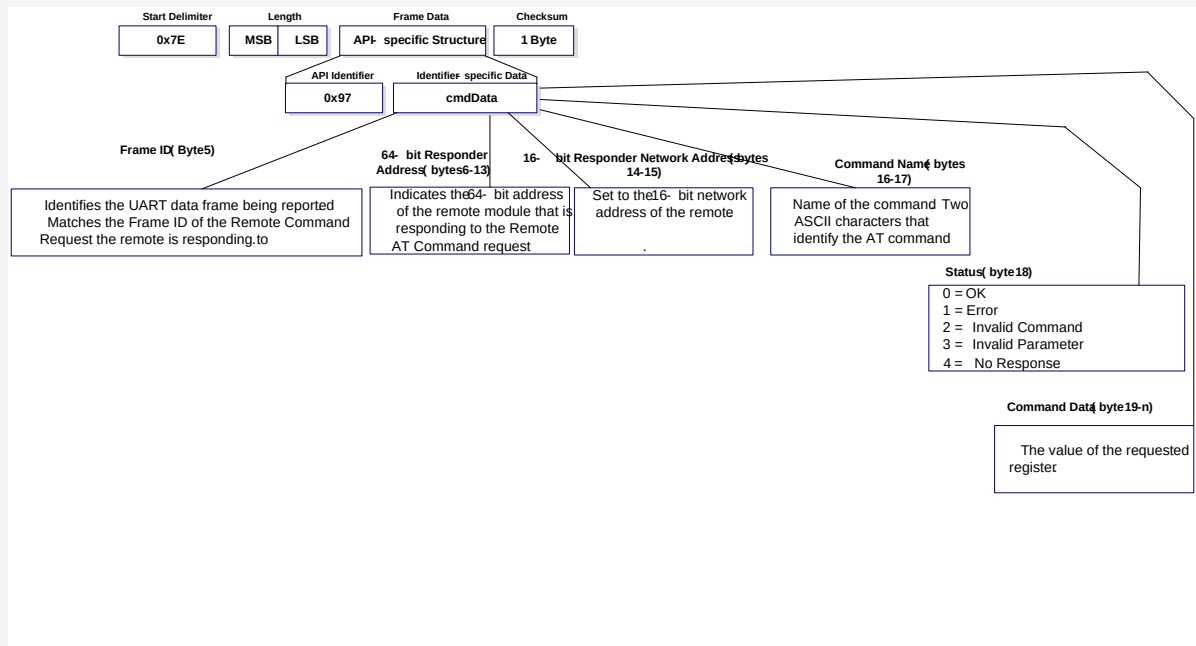


Remote Command Response

API Identifier Value: 0x97

If a module receives a remote command response RF data frame in response to a Remote AT Command Request, the module will send a Remote AT Command Response message out the UART. Some commands may send back multiple frames--for example, Node Discover (ND) command.

Figure 3-12. Remote AT Command Response.

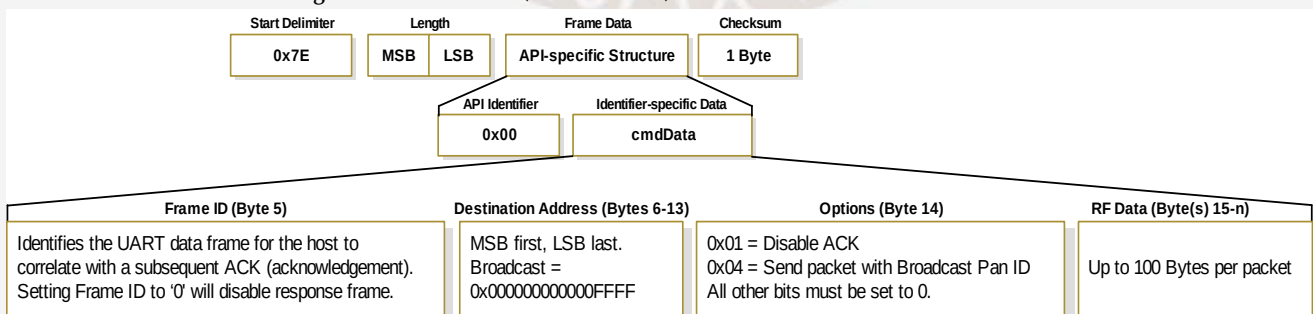


TX (Transmit) Request: 64-bit address

API Identifier Value: 0x00

A TX Request message will cause the module to send RF Data as an RF Packet.

Figure 3-13. TX Packet (64-bit address) Frames

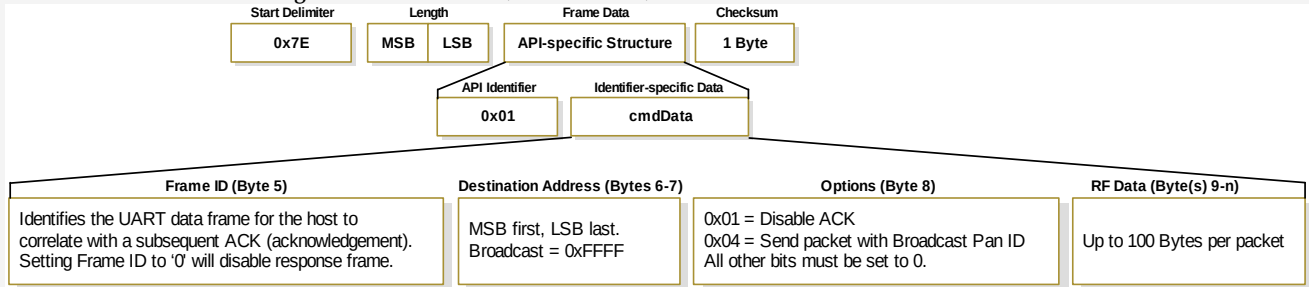


TX (Transmit) Request: 16-bit address

API Identifier Value: 0x01

A TX Request message will cause the module to send RF Data as an RF Packet.

Figure 3-14. TX Packet (16-bit address) Frames

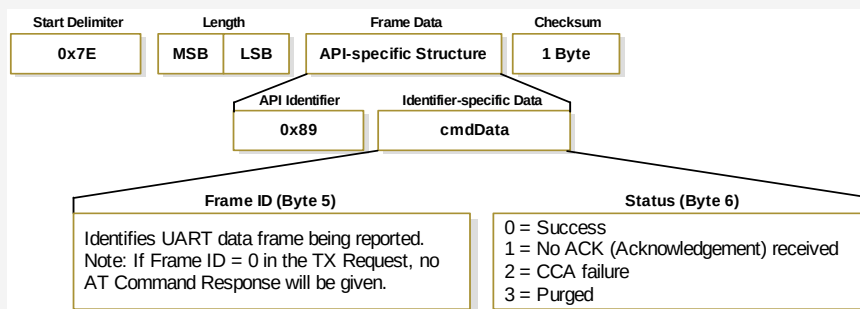


TX (Transmit) Status

API Identifier Value: 0x89

When a TX Request is completed, the module sends a TX Status message. This message will indicate if the packet was transmitted successfully or if there was a failure.

Figure 3-15. TX Status Frames



NOTES:

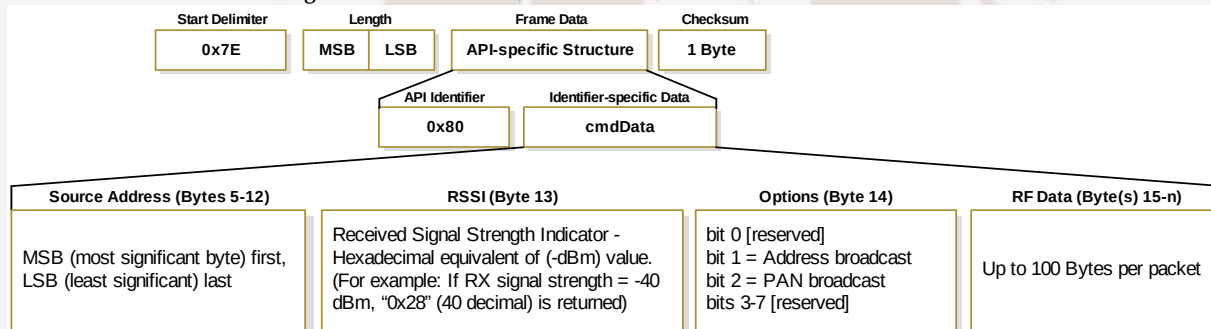
- "STATUS = 1" occurs when all retries are expired and no ACK is received.
- If transmitter broadcasts (destination address = 0x000000000000FFFF), only "STATUS = 0 or 2" will be returned.
- "STATUS = 3" occurs when Coordinator times out of an indirect transmission. Timeout is defined as (2.5 x SP (Cyclic Sleep Period) parameter value).

RX (Receive) Packet: 64-bit Address

API Identifier Value: 0x80

When the module receives an RF packet, it is sent out the UART using this message type.

Figure 3-16. RX Packet (64-bit address) Frames

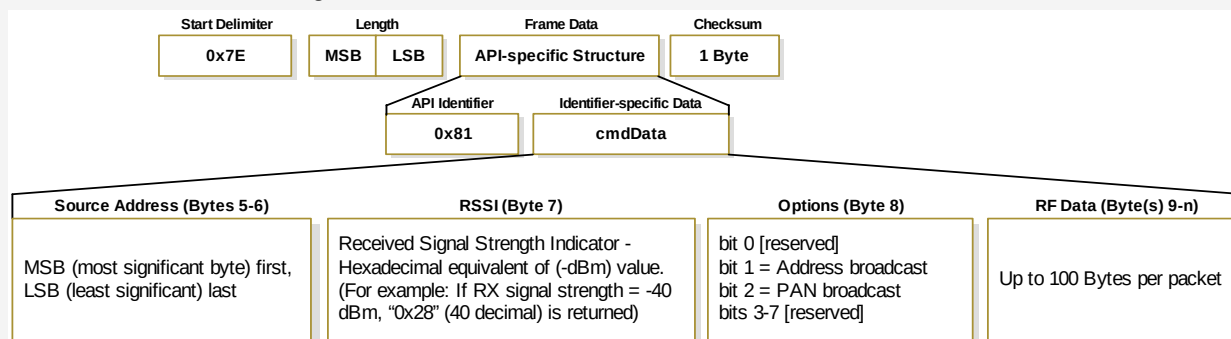


RX (Receive) Packet: 16-bit Address

API Identifier Value: 0x81

When the module receives an RF packet, it is sent out the UART using this message type.

Figure 3-17. RX Packet (16-bit address) Frames



Appendix A: Agency Certifications

United States (FCC)

XBee®/XBee-PRO® RF Modules comply with Part 15 of the FCC rules and regulations. Compliance with the labeling requirements, FCC notices and antenna usage guidelines is required.

To fulfill FCC Certification requirements, the OEM must comply with the following regulations:

1. The system integrator must ensure that the text on the external label provided with this device is placed on the outside of the final product [Figure A-01].
2. XBee®/XBee-PRO® RF Modules may only be used with antennas that have been tested and approved for use with this module [refer to the antenna tables in this section].

OEM Labeling Requirements



WARNING: The Original Equipment Manufacturer (OEM) must ensure that FCC labeling requirements are met. This includes a clearly visible label on the outside of the final product enclosure that displays the contents shown in the figure below.

Figure 4-01. Required FCC Label for OEM products containing the XBee®/XBee-PRO® RF Module

Contains FCC ID: OUR-XBEE/OUR-XBEEPRO**

The enclosed device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (i.) this device may not cause harmful interference and (ii.) this device must accept any interference received, including interference that may cause undesired operation.

* The FCC ID for the XBee is "OUR-XBEE". The FCC ID for the XBee-PRO is "OUR-XBEEPRO".

FCC Notices

IMPORTANT: The XBee®/XBee-PRO® RF Module has been certified by the FCC for use with other products without any further certification (as per FCC section 2.1091). Modifications not expressly approved by Digi could void the user's authority to operate the equipment.

IMPORTANT: OEMs must test final product to comply with unintentional radiators (FCC section 15.107 & 15.109) before declaring compliance of their final product to Part 15 of the FCC Rules.

IMPORTANT: The RF module has been certified for remote and base radio applications. If the module will be used for portable applications, the device must undergo SAR testing.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures: Re-orient or relocate the receiving antenna, Increase the separation between the equipment and receiver, Connect equipment and receiver to outlets on different circuits, or Consult the dealer or an experienced radio/TV technician for help.

FCC-Approved Antennas (2.4 GHz)

XBee/XBee-PRO RF Modules can be installed using antennas and cables constructed with standard connectors (Type-N, SMA, TNC, etc.) if the installation is performed professionally and according to FCC guidelines. For installations not performed by a professional, non-standard connectors (RPSMA, RPTNC, etc) must be used.

The modules are FCC-approved for fixed base station and mobile applications on channels 0x0B - 0x1A (XBee) and 0x0C - 0x17 (XBee-PRO). If the antenna is mounted at least 20cm (8 in.) from nearby persons, the application is considered a mobile application. Antennas not listed in the table must be tested to comply with FCC Section 15.203 (Unique Antenna Connectors) and Section 15.247 (Emissions).

XBee RF Modules (1 mW): XBee Modules have been tested and approved for use with all of the antennas listed in the tables below (Cable-loss IS NOT required).

XBee-PRO RF Modules (60 mW): XBee-PRO Modules have been tested and approved for use with the antennas listed in the tables below (Cable-loss IS required when using antennas listed in the second table).

The antennas in the tables below have been approved for use with this module. Digi does not carry all of these antenna variants. Contact Digi Sales for available antennas.

Antennas approved for use with the XBee®/XBee-PRO® RF Modules (Cable-loss is not required.)

Part Number	Type (Description)	Gain	Application*	Min. Separation
A24-HASM-450	Dipole (Half-wave articulated RPSMA - 4.5")	2.1 dBi	Fixed/Mobile	20 cm
A24-HABSM	Dipole (Articulated RPSMA)	2.1 dBi	Fixed	20 cm
A24-HABUF-P5I	Dipole (Half-wave articulated bulkhead mount U.F.L. w/ 5" pigtail)	2.1 dBi	Fixed	20 cm
A24-HASM-525	Dipole (Half-wave articulated RPSMA - 5.25")	2.1 dBi	Fixed/Mobile	20 cm
A24-QI	Monopole (Integrated whip)	1.5 dBi	Fixed	20 cm

Antennas approved for use with the XBee RF Modules (Cable-loss is required)

Part Number	Type (Description)	Gain	Application*	Min. Separation	Required Cable-loss
Omni-Directional Class Antennas					
A24-Y6NF	Yagi (6-element)	8.8 dBi	Fixed	2 m	1.7 dB
A24-Y7NF	Yagi (7-element)	9.0 dBi	Fixed	2 m	1.9 dB
A24-Y9NF	Yagi (9-element)	10.0 dBi	Fixed	2 m	2.9 dB
A24-Y10NF	Yagi (10-element)	11.0 dBi	Fixed	2 m	3.9 dB
A24-Y12NF	Yagi (12-element)	12.0 dBi	Fixed	2 m	4.9 dB
A24-Y13NF	Yagi (13-element)	12.0 dBi	Fixed	2 m	4.9 dB
A24-Y15NF	Yagi (15-element)	12.5 dBi	Fixed	2 m	5.4 dB
A24-Y16NF	Yagi (16-element)	13.5 dBi	Fixed	2 m	6.4 dB
A24-Y16RM	Yagi (16-element, RPSMA connector)	13.5 dBi	Fixed	2 m	6.4 dB
A24-Y18NF	Yagi (18-element)	15.0 dBi	Fixed	2 m	7.9 dB
Omni-Directional Class Antennas					
A24-C1	Surface Mount	-1.5 dBi	Fixed/Mobile	20 cm	-
A24-F2NF	Omni-directional (Fiberglass base station)	2.1 dBi	Fixed/Mobile	20 cm	
A24-F3NF	Omni-directional (Fiberglass base station)	3.0 dBi	Fixed/Mobile	20 cm	
A24-F5NF	Omni-directional (Fiberglass base station)	5.0 dBi	Fixed/Mobile	20 cm	
A24-F8NF	Omni-directional (Fiberglass base station)	8.0 dBi	Fixed	2 m	
A24-F9NF	Omni-directional (Fiberglass base station)	9.5 dBi	Fixed	2 m	0.2 dB
A24-F10NF	Omni-directional (Fiberglass base station)	10.0 dBi	Fixed	2 m	0.7 dB
A24-F12NF	Omni-directional (Fiberglass base station)	12.0 dBi	Fixed	2 m	2.7 dB
A24-F15NF	Omni-directional (Fiberglass base station)	15.0 dBi	Fixed	2 m	5.7 dB
A24-W7NF	Omni-directional (Base station)	7.2 dBi	Fixed	2 m	
A24-M7NF	Omni-directional (Mag-mount base station)	7.2 dBi	Fixed	2 m	
Panel Class Antennas					
A24-P8SF	Flat Panel	8.5 dBi	Fixed	2 m	1.5 dB
A24-P8NF	Flat Panel	8.5 dBi	Fixed	2 m	1.5 dB
A24-P13NF	Flat Panel	13.0 dBi	Fixed	2 m	6 dB
A24-P14NF	Flat Panel	14.0 dBi	Fixed	2 m	7 dB
A24-P15NF	Flat Panel	15.0 dBi	Fixed	2 m	8 dB
A24-P16NF	Flat Panel	16.0 dBi	Fixed	2 m	9 dB

Antennas approved for use with the XBee®/XBee-PRO® RF Modules (Cable-loss is required)

Part Number	Type (Description)	Gain	Application*	Min. Separation	Required Cable-loss
A24-C1	Surface Mount	-1.5 dBi	Fixed/Mobile	20 cm	-
A24-Y4NF	Yagi (4-element)	6.0 dBi	Fixed	2 m	8.1 dB
A24-Y6NF	Yagi (6-element)	8.8 dBi	Fixed	2 m	10.9 dB
A24-Y7NF	Yagi (7-element)	9.0 dBi	Fixed	2 m	11.1 dB
A24-Y9NF	Yagi (9-element)	10.0 dBi	Fixed	2 m	12.1 dB
A24-Y10NF	Yagi (10-element)	11.0 dBi	Fixed	2 m	13.1 dB
A24-Y12NF	Yagi (12-element)	12.0 dBi	Fixed	2 m	14.1 dB
A24-Y13NF	Yagi (13-element)	12.0 dBi	Fixed	2 m	14.1 dB
A24-Y15NF	Yagi (15-element)	12.5 dBi	Fixed	2 m	14.6 dB
A24-Y16NF	Yagi (16-element)	13.5 dBi	Fixed	2 m	15.6 dB
A24-Y16RM	Yagi (16-element, RPSMA connector)	13.5 dBi	Fixed	2 m	15.6 dB
A24-Y18NF	Yagi (18-element)	15.0 dBi	Fixed	2 m	17.1 dB
A24-F2NF	Omni-directional (Fiberglass base station)	2.1 dBi	Fixed/Mobile	20 cm	4.2 dB
A24-F3NF	Omni-directional (Fiberglass base station)	3.0 dBi	Fixed/Mobile	20 cm	5.1 dB
A24-F5NF	Omni-directional (Fiberglass base station)	5.0 dBi	Fixed/Mobile	20 cm	7.1 dB
A24-F8NF	Omni-directional (Fiberglass base station)	8.0 dBi	Fixed	2 m	10.1 dB
A24-F9NF	Omni-directional (Fiberglass base station)	9.5 dBi	Fixed	2 m	11.6 dB
A24-F10NF	Omni-directional (Fiberglass base station)	10.0 dBi	Fixed	2 m	12.1 dB
A24-F12NF	Omni-directional (Fiberglass base station)	12.0 dBi	Fixed	2 m	14.1 dB
A24-F15NF	Omni-directional (Fiberglass base station)	15.0 dBi	Fixed	2 m	17.1 dB
A24-W7NF	Omni-directional (Base station)	7.2 dBi	Fixed	2 m	9.3 dB
A24-M7NF	Omni-directional (Mag-mount base station)	7.2 dBi	Fixed	2 m	9.3 dB
A24-P8SF	Flat Panel	8.5 dBi	Fixed	2 m	8.6 dB
A24-P8NF	Flat Panel	8.5 dBi	Fixed	2 m	8.6 dB
A24-P13NF	Flat Panel	13.0 dBi	Fixed	2 m	13.1 dB
A24-P14NF	Flat Panel	14.0 dBi	Fixed	2 m	14.1 dB
A24-P15NF	Flat Panel	15.0 dBi	Fixed	2 m	15.1 dB
A24-P16NF	Flat Panel	16.0 dBi	Fixed	2 m	16.1 dB
A24-P19NF	Flat Panel	19.0 dBi	Fixed	2 m	19.1 dB

* **If using the RF module in a portable application** (For example - If the module is used in a handheld device and the antenna is less than 20cm from the human body when the device is operation): The integrator is responsible for passing additional SAR (Specific Absorption Rate) testing based on FCC rules 2.1091 and FCC Guidelines for Human Exposure to Radio Frequency Electromagnetic Fields, OET Bulletin and Supplement C. The testing results will be submitted to the FCC for approval prior to selling the integrated unit. The required SAR testing measures emissions from the module and how they affect the person.

RF Exposure

WARNING: To satisfy FCC RF exposure requirements for mobile transmitting devices, a separation distance of 20 cm or more should be maintained between the antenna of this device and persons during device operation. To ensure compliance, operations at closer than this distance is not recommended. The antenna used for this transmitter must not be co-located in conjunction with any other antenna or transmitter.

The preceding statement must be included as a CAUTION statement in OEM product manuals in order to alert users of FCC RF Exposure compliance.

Europe (ETSI)

The XBee RF Modules have been certified for use in several European countries. For a complete list, refer to www.digi.com

If the XBee RF Modules are incorporated into a product, the manufacturer must ensure compliance of the final product to the European harmonized EMC and low-voltage/safety standards. A Declaration of Conformity must be issued for each of these standards and kept on file as described in Annex II of the R&TTE Directive.

Furthermore, the manufacturer must maintain a copy of the XBee user manual documentation and ensure the final product does not exceed the specified power ratings, antenna specifications, and/or installation requirements as specified in the user manual. If any of these specifications are exceeded in the final product, a submission must be made to a notified body for compliance testing to all required standards.

OEM Labeling Requirements

The 'CE' marking must be affixed to a visible location on the OEM product.

CE Labeling Requirements

The CE mark shall consist of the initials "CE" taking the following form:

- If the CE marking is reduced or enlarged, the proportions given in the above graduated drawing must be respected.
- The CE marking must have a height of at least 5mm except where this is not possible on account of the nature of the apparatus.
- The CE marking must be affixed visibly, legibly, and indelibly.

Restrictions

Power Output: When operating in Europe, XBee-PRO 802.15.4 modules must operate at or below a transmit power output level of 10dBm. Customers have two choices for transmitting at or below 10dBm:

- a. Order the standard XBee-PRO module and change the PL command to 0 (10dBm)
- b. Order the International variant of the XBee-PRO module, which has a maximum transmit output power of 10dBm (@ PL=4).

Additionally, European regulations stipulate an EIRP power maximum of 12.86 dBm (19 mW) for the XBee-PRO and 12.11 dBm for the XBee when integrating antennas.

France: Outdoor use limited to 10 mW EIRP within the band 2454-2483.5 MHz.

Norway: Norway prohibits operation near Ny-Alesund in Svalbard. More information can be found at the Norway Posts and Telecommunications site (www.npt.no).

Declarations of Conformity

Digi has issued Declarations of Conformity for the XBee RF Modules concerning emissions, EMC and safety. Files can be obtained by contacting Digi Support.

Important Note:

Digi does not list the entire set of standards that must be met for each country. Digi customers assume full responsibility for learning and meeting the required guidelines for each country in their distribution market. For more information relating to European compliance of an OEM product incorporating the XBee RF Module, contact Digi, or refer to the following web sites:

CEPT ERC 70-03E - Technical Requirements, European restrictions and general requirements: Available at www.ero.dk/.

R&TTE Directive - Equipment requirements, placement on market: Available at www.ero.dk/.

Approved Antennas

When integrating high-gain antennas, European regulations stipulate EIRP power maximums. Use the following guidelines to determine which antennas to design into an application.

XBee-PRO RF Module

The following antenna types have been tested and approved for use with the XBee Module:

Antenna Type: Yagi

RF module was tested and approved with 15 dBi antenna gain with 1 dB cable-loss (EIRP Maximum of 14 dBm). Any Yagi type antenna with 14 dBi gain or less can be used with no cable-loss.

Antenna Type: Omni-directional

RF module was tested and approved with 15 dBi antenna gain with 1 dB cable-loss (EIRP Maxi-

mum of 14 dBm). Any Omni-directional type antenna with 14 dBi gain or less can be used with no cable-loss.

Antenna Type: Flat Panel

RF module was tested and approved with 19 dBi antenna gain with 4.8 dB cable-loss (EIRP Maximum of 14.2 dBm). Any Flat Panel type antenna with 14.2 dBi gain or less can be used with no cable-loss.

XBee-PRO RF Module (@ 10 dBm Transmit Power, PL parameter value must equal 0, or use International variant)

The following antennas have been tested and approved for use with the embedded XBee-PRO RF Module:

- Dipole (2.1 dBi, Omni-directional, Articulated RPSMA, Digi part number A24-HABSM)
- Chip Antenna (-1.5 dBi)
- Attached Monopole Whip (1.5 dBi)

The RF modem encasement was designed to accommodate the RPSMA antenna option.

Canada (IC)

Labeling Requirements

Labeling requirements for Industry Canada are similar to those of the FCC. A clearly visible label on the outside of the final product enclosure must display the following text:

Contains Model XBee Radio, IC: 4214A-XBEE

Contains Model XBee-PRO Radio, IC: 4214A-XBEEPRO

The integrator is responsible for its product to comply with IC ICES-003 & FCC Part 15, Sub. B - Unintentional Radiators. ICES-003 is the same as FCC Part 15 Sub. B and Industry Canada accepts FCC test report or CISPR 22 test report for compliance with ICES-003.

Japan

In order to gain approval for use in Japan, the XBee RF module or the International variant of the XBee-PRO RF module (which has 10 dBm transmit output power) must be used.

Labeling Requirements

A clearly visible label on the outside of the final product enclosure must display the following text:

ID: 005NYCA0378

Appendix B. Additional Information

1-Year Warranty

XBee®/XBee-PRO® RF Modules from Digi International, Inc. (the "Product") are warranted against defects in materials and workmanship under normal use, for a period of 1-year from the date of purchase. In the event of a product failure due to materials or workmanship, Digi will repair or replace the defective product. For warranty service, return the defective product to Digi, shipping prepaid, for prompt repair or replacement.

The foregoing sets forth the full extent of Digi's warranties regarding the Product. Repair or replacement at Digi's option is the exclusive remedy. THIS WARRANTY IS GIVEN IN LIEU OF ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, AND DIGI SPECIFICALLY DISCLAIMS ALL WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. IN NO EVENT SHALL DIGI, ITS SUPPLIERS OR LICENSORS BE LIABLE FOR DAMAGES IN EXCESS OF THE PURCHASE PRICE OF THE PRODUCT, FOR ANY LOSS OF USE, LOSS OF TIME, INCONVENIENCE, COMMERCIAL LOSS, LOST PROFITS OR SAVINGS, OR OTHER INCIDENTAL, SPECIAL OR CONSEQUENTIAL DAMAGES ARISING OUT OF THE USE OR INABILITY TO USE THE PRODUCT, TO THE FULL EXTENT SUCH MAY BE DISCLAIMED BY LAW. SOME STATES DO NOT ALLOW THE EXCLUSION OR LIMITATION OF INCIDENTAL OR CONSEQUENTIAL DAMAGES. THEREFORE, THE FOREGOING EXCLUSIONS MAY NOT APPLY IN ALL CASES. This warranty provides specific legal rights. Other rights which vary from state to state may also apply.

