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**PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERU**  
**Facultad de Ciencias e Ingeniería**



**DISEÑO E IMPLEMENTACIÓN DE UN SISTEMA DE  
CONTROL DIGITAL CON CONEXIÓN A REDES DE  
DATOS PARA MEDICIÓN DE PARÁMETROS  
ELÉCTRICOS**

*Tesis para optar el título de ingeniero electrónico*

**Presentado por:  
Gerardo Manuel Guerrero Quichiz**

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## RESUMEN

La introducción y continua mejora de elementos digitales en dispositivos, que antes se consideraban íntegramente analógicos, han causado toda una revolución en los diversos campos de los sistemas electrónicos. Dichos cambios han logrado integrar sistemas que, hasta hace unos años, no se consideraban dentro de una misma área temática. El presente proyecto de tesis busca ampliar la aplicación de la electrónica digital fusionando el área de Electricidad con la de Comunicaciones y desarrollando un Sistema de control digital basado en la tecnología del microcontrolador ATmega128 de la compañía ATMEL y del circuito integrado ADE7758 de Analog Devices, que además posea la lógica adecuada para la medición trifásica de parámetros eléctricos y permita la comunicación a redes de datos.

Con dicha aplicación será la etapa principal y básica de un sistema mayor, encargado de la medición digital de energía eléctrica trifásica en media y baja tensión, con un bajo porcentaje de error que permita comunicación remota en tiempo real de los parámetros eléctricos sensados (Voltaje RMS, Corriente RMS; Potencia Activa, Potencia Reactiva, Potencia Aparente, entre otros) hacia un computador de la red. La tesis comprenderá el desarrollo del sistema de control con la lógica adecuada para el procesamiento futuro de medición y de comunicación; contando con etapas de ingreso de datos, pre-procesamiento, control, visualización, comunicación y expansiones para mejoras futuras.

Respecto a la utilidad del proyecto, ésta se extiende al campo comercial puesto que la integración del proyecto de tesis como Sistema de control digital a un Sistema mayor de medición de energía eléctrica con comunicación en tiempo real dará versatilidad a los procesos industriales, convirtiéndose en un factor clave a nivel económico por el control eficiente del consumo eléctrico que posteriormente se verá reflejado en mejoras de los costos de producción.





¿A quién, sino a ti?

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## INTRODUCCIÓN

El desarrollo tecnológico, al igual que toda área de actividad humana, ha buscado satisfacer las necesidades, ya sean individuales o colectivas de los miembros de su comunidad. Particularmente la tecnología, en su finalidad de solución, ha dado cabida al desarrollo de nuevos sistemas, empleando para dicho fin los recursos de la sociedad en la que se halla inmersa. Debido a la pluralidad de los recursos existentes, las soluciones planteadas para afrontar una problemática específica son diversas e innovadoras entre ellas.

En la actualidad, a modo de preservar nuestro medio ambiente, nos enfrentamos al hecho de controlar eficientemente la energía eléctrica, así como su correcto control en el sector industrial que asegurará una mejor producción sin elevar costos. Ambos enfoques generan una necesidad: la medición eficiente del consumo de energía eléctrica.

Para dicho objetivo, desde hace algunos años se vienen realizando estudios, utilizando diferentes tecnologías para la determinación de los diversos parámetros que contempla la energía eléctrica. Los desarrollos han ido evolucionando a la par con los avances

científicos de la época, lográndose equipos versátiles y eficientes: desde los antiguos equipos medidores mecánicos, que sólo sensaban la potencia activa, hasta los equipos medidores digitales de hoy en día que sensan una variedad de parámetros eléctricos con una considerable exactitud, siendo estos últimos, los más costosos y eficientes.

Con el objetivo de mejorar el control de los sistemas de medición, nace una nueva tendencia que integra el área de electricidad con la de telecomunicaciones creando para ello un sistema de medición de parámetros eléctricos con la capacidad de comunicación en tiempo real.

Esta investigación e implementación constituye el primer paso para lograr este objetivo, puesto que la presente tesis desarrolla un Sistema de control digital para medición de parámetros eléctricos con conexión a redes de datos. El prototipo no realiza medición alguna pero posee la lógica adecuada para esta finalidad y para la comunicación mediante TCP/IP.

Para la evaluación del sistema, se ha acondicionado un software a fin de verificar la correcta interconexión entre el sistema de medición y la red de datos, además de dar lectura a registros internos del prototipo y de esta manera comprobar su correcto funcionamiento.

El presente documento se encuentra dividido en cuatro capítulos principales y las respectivas conclusiones: en el primer capítulo, se hace una revisión de la problemática actual de la energía eléctrica y se expone la necesidad de contar con un control eficiente de la energía eléctrica tanto a nivel ambiental, para la preservación del

ecosistema, como a nivel industrial, para reducir costos sin afectar la producción. Para realizar dicho control se requiere un sensor adecuado para efectos de medición, que es el Medidor de parámetros eléctricos. Siendo así, se presenta una breve reseña histórica de su evolución en el tiempo, pasando desde la primera patente dada en 1872 por Samuel Gardiner, hasta los últimos desarrollos en los llamados sistemas EEM que introducen conceptos de telemetría. En este mismo capítulo, luego del análisis de la problemática y las tecnologías de medidores que surgieron en el transcurso de los años, se establecen los objetivos que marcarán la investigación y desarrollo del prototipo digital.

La descripción más detallada de las diversas tecnologías de medición se presenta en el segundo capítulo, dividiéndolos en tres grupos: por mecanismos indicadores, por metodología y por aplicación; dando énfasis a los algoritmos digitales para los cálculos medición. Mas adelante, se presenta la tarjeta TEMPUS VI que por sus características se utiliza como módulo de control, y adicionalmente se exponen tecnologías de comunicación serial entre periféricos. Después de estudiar las diversas alternativas para resolver los objetivos planteados, se procede a hacer un análisis teórico a fin de elegir las técnicas y metodologías más adecuadas para este proyecto.

El tercer capítulo se concentra estrictamente en el diseño del sistema, se mencionan las diversas etapas que la conforman, para las cuales se hace un análisis de requerimientos, investigación y selección de componentes; tomando consideraciones técnicas para el diseño electrónico. Adicionalmente, se presenta el diseño industrial del chasis del prototipo, el cual se ha desarrollado conforme a los requerimientos comerciales futuros del equipo final.

En el cuarto capítulo se exponen los resultados obtenidos con el desarrollo del prototipo, los logros alcanzados y una descripción de las recomendaciones para su posterior desarrollo.

Finalmente, el último capítulo menciona las conclusiones obtenidas a partir del proceso de desarrollo del proyecto de tesis y de los objetivos inicialmente planteados.



## CAPÍTULO 1

### LA ENERGÍA EN EL SECTOR DE CONSUMO

#### 1.1 IMPORTANCIA DEL CONTROL DE LA ENERGÍA ELÉCTRICA

El control de la energía eléctrica es una pieza clave en como proyectamos nuestro futuro tanto a nivel ambiental como a nivel industrial, para resaltar su importancia se analizarán dos enfoques: el primero mostrará el inminente impacto al ecosistema ante la creciente población, mientras que en el segundo se analiza un hecho del ámbito industrial en donde reducir costos significa maximizar beneficios.

##### 1.1.1 EL CONTROL DE LA ENERGÍA ELÉCTRICA A NIVEL AMBIENTAL

Hoy en día muchas personas asumen que se hace un buen trabajo conservando la electricidad y en efecto, diversos artefactos utilizan mucho menos energía que en décadas anteriores. Pero a pesar de nuestros esfuerzos para conservar la energía, la cantidad de electricidad consumida, sólo en el Perú, ha ido en aumento con el pasar de los años (durante este tiempo la población también se ha incrementado). El Ministerio de energía y minas del Perú ha hecho unos interesantes estudios respecto a la relación Población – Producción de energía eléctrica:

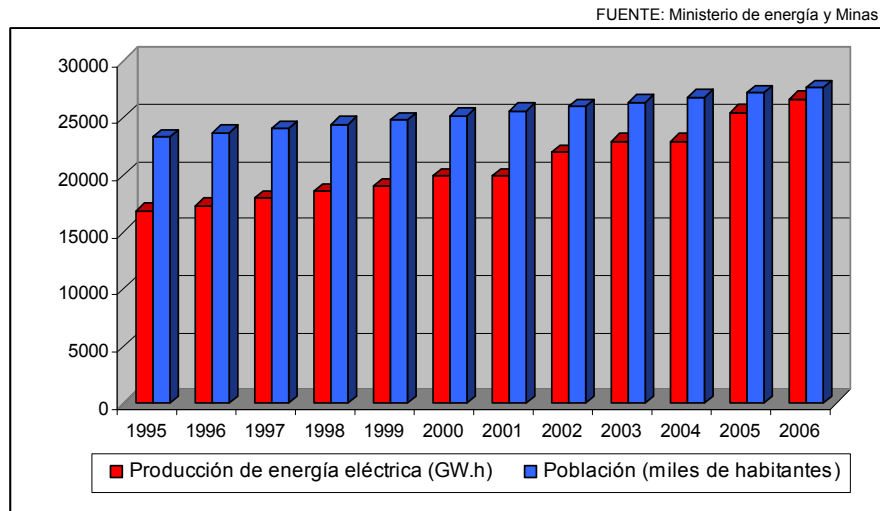


Figura 1.1 – Comparación de la producción de energía eléctrica y la población en el Perú

FUENTE: Ministerio de energía y Minas

INDICADORES	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006
NUMERO DE CLIENTES	2 492	2 776	2 964	3 057	3 217	3 352	3 463	3 614	3 727	3 861	3 977	4 065
PRODUCCIÓN DE ENERGÍA ELECTRICA (GW.h)	16 880	17 280	17 953	18 583	19 050	19 923	19 923	21 982	22 923	22 923	25 510	26 713
VENTAS DE ENERGIA ELECTRICA (GW.h)	9 849	10 331	12 451	14 009	14 592	15 546	16 629	17 605	18 375	19 641	20 701	21 753
COEFICIENTE DE ELECTRIFICACION NACIONAL (%)	64.9	66.1	67.65	69.5	72.2	73.5	74.94	75.3	76.0	76.3	78.1	80.0
<b>INDICADORES ENERGÉTICOS</b>												
Población (miles de habitantes)	23 345	23 707	24 073	24 446	24 824	25 208	25 598	25 994	26 396	26 805	27 219	27 640
Consumo de energía eléctrica per cápita (kW.h/hab.)	584	603	625	645	656	680	711	737	755	794	823	850
Producción de energía eléctrica per cápita (kW.h/hab.)	723	729	746	760	767	790	812	846	868	905	937	966

Tabla 1.1 – Evolución de indicadores del mercado eléctrico 1995 – 2006

Como se observa en la Figura 1.1, sólo en los últimos 5 años, la energía eléctrica producida (*República del Perú – Ministerio de energía y minas, Dirección general de electricidad/Dirección de promoción y estudios, 2006*) medida en billones de vatio por horas (GW.h) y la población (*INEI – X Censo Nacional de Población 2005 del Perú,*

año 2006) medida en miles de habitantes, muestran que la producción de electricidad durante los últimos 10 años ha aumentado en un 58.3% mientras que el número de habitantes sólo lo hizo en un 18.4%, entonces si dividimos la cantidad de energía eléctrica producida entre la población conseguimos la Figura 1.2 la cual muestra que nuestros esfuerzos de conservación no han sido del todo satisfactorios pues no han logrado reducir la cantidad de electricidad que consumimos por persona. Sólo en el periodo comprendido entre los años 1995 a 2006 ha ocurrido un aumento del 33.6% de la energía eléctrica consumida por hora por cada persona peruana promedio.

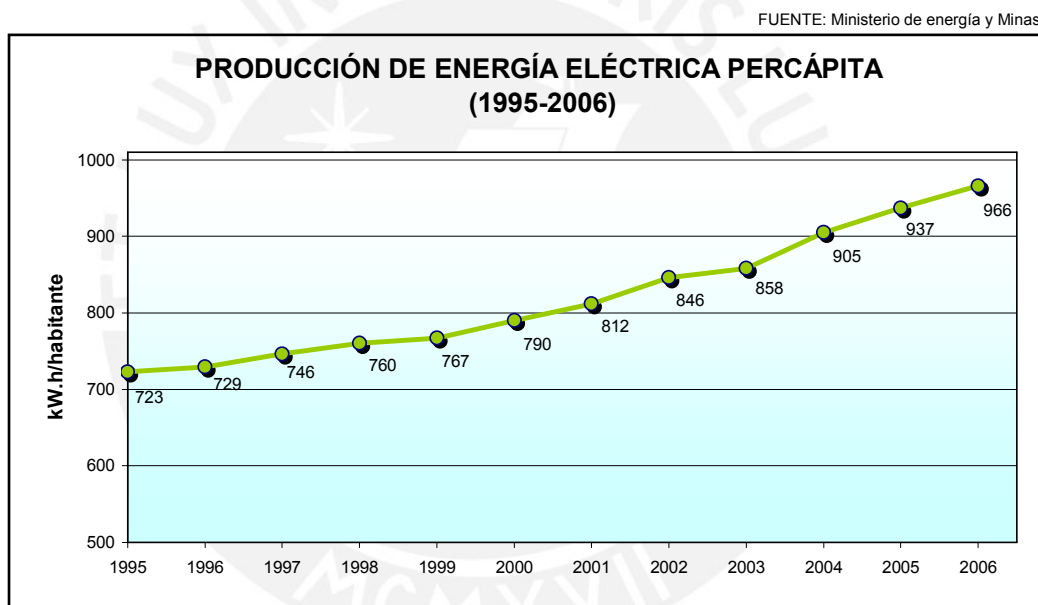


Figura 1.2 – Energía eléctrica producida por persona en el Perú

Este gran incremento en el consumo energético se puede comprender por dos factores básicos: Primero, los individuos consumen más electricidad cada año y, segundo, la población crece cada año. Según el INEI: Instituto Nacional de Estadística e Informática del Perú (2006), sólo considerando los datos de Lima metropolitana y el Callao, hay cuatro nacimientos cada 7 minutos y una muerte cada 8 minutos. Considerando las emigraciones e inmigraciones, tenemos un efecto neto que añadimos una persona a nuestra población total cada 2 minutos y medio.

En los siguientes 50 años, el Perú tendrá unos 10.5 millones de personas adicionales. Si tomamos los datos de consumo energético recopilados, y asumimos el mismo índice de crecimiento, tendríamos que considerar unos 1300 KWh de consumo de energía eléctrica para cada una de aquellas personas. Esto nos da un valor ascendente a 13.7 mil millones de KWh extras que se requerirían producir para satisfacer la demanda de energía eléctrica peruana en los próximos 50 años.

Una planta generadora mediana puede producir 1 000 KWs de poder (*Electric Power Monthly, Marzo 2002*). Si consideramos un funcionamiento al 85%, por todos los días y las noches durante un año, esta podrá producir 7.45 millones de KWh. Dividiendo los 13.7 mil millones de kWh que necesitaría la población adicional entre 7.45 millones de KWh que una central eléctrica puede producir, encontramos que se debería construir unas 20 centrales eléctricas medianas en los próximos cincuenta años para así abastecer a toda la población. Si usamos las mismas fuentes productoras de energía que alimentan a nuestras plantas generadoras actuales se producirá un daño irreversible al ecosistema, por el impacto directo sobre el ambiente, además de producir gases de invernadero y emisiones de azufre; si bien por un lado se busca reducir ambos, nuestra propia demanda energética los ocasionaría. Y según el The World Bank Group (*World Development Indicators database, Abril 2007*), otros países dentro de la región y Estados Unidos presentan consumos mayores al nuestro:

	Argentina	Brasil	Chile	Perú	Estados Unidos
CONSUMO ELÉCTRICO PER CÁPITA 2000 (KW.h)	1938	1811	2309	680	11994

Tabla 1.2 – Consumo eléctrico per cápita en los países de la región y Estados Unidos

Estos datos y resultados dan pie a examinar detalladamente los pasos de control que se realiza para maximizar la eficiencia del consumo de la energía eléctrica. Todo sistema de control consta de 3 etapas o partes básicas: El actuador, la planta y el sensor los cuales se comunican como se observa en la Figura 1.3.

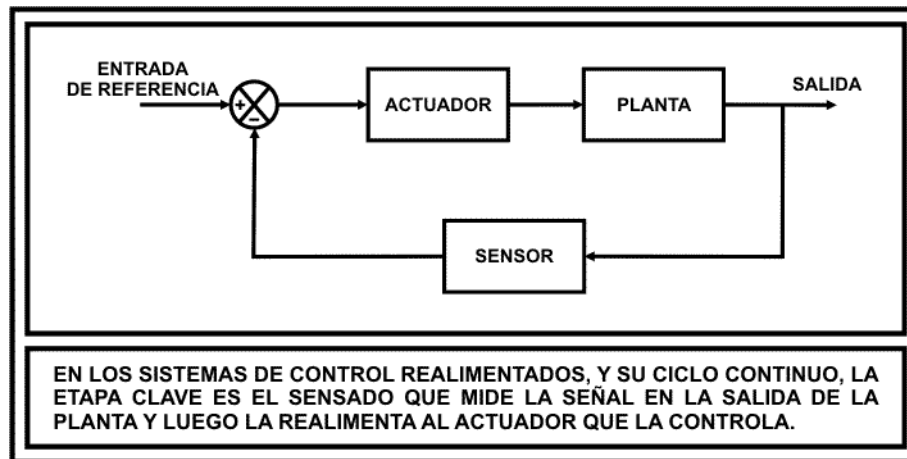


Figura 1.3 – Diagrama de bloques de un sistema de control básico

Un Actuador que será el encargado de contener la lógica de control para el manejo eficiente, la Planta que es la etapa a controlar y que a su vez será receptora de las acciones elegidas por el actuador y la última etapa, pero no menos importante, el Sensor cuyo objetivo será el de medir el desempeño de la Planta ante las acciones determinadas por el Actuador para luego realimentar al sistema y de ese modo el proceso de control continúe su normal desarrollo. En el caso que nos ocupa el Actuador será el contenedor de las decisiones y lógicas tomadas por los especialistas en el tema del control de la energía, la Planta serán nuestros sectores de consumo energético a nivel mundial y el Sensor serán los dispositivos tales que nos permitan cuantificar dicho consumo de energía eléctrica en todas sus variables, esto hace surgir la necesidad de contar con medidores eficientes para que el sistema también pueda ser eficiente, dichos medidores son los denominados medidores de energía.

### 1.1.2 EL CONTROL DE LA ENERGÍA ELÉCTRICA A NIVEL INDUSTRIAL

El uso de la energía eléctrica en el sector de consumo, se divide según el siguiente esquema:

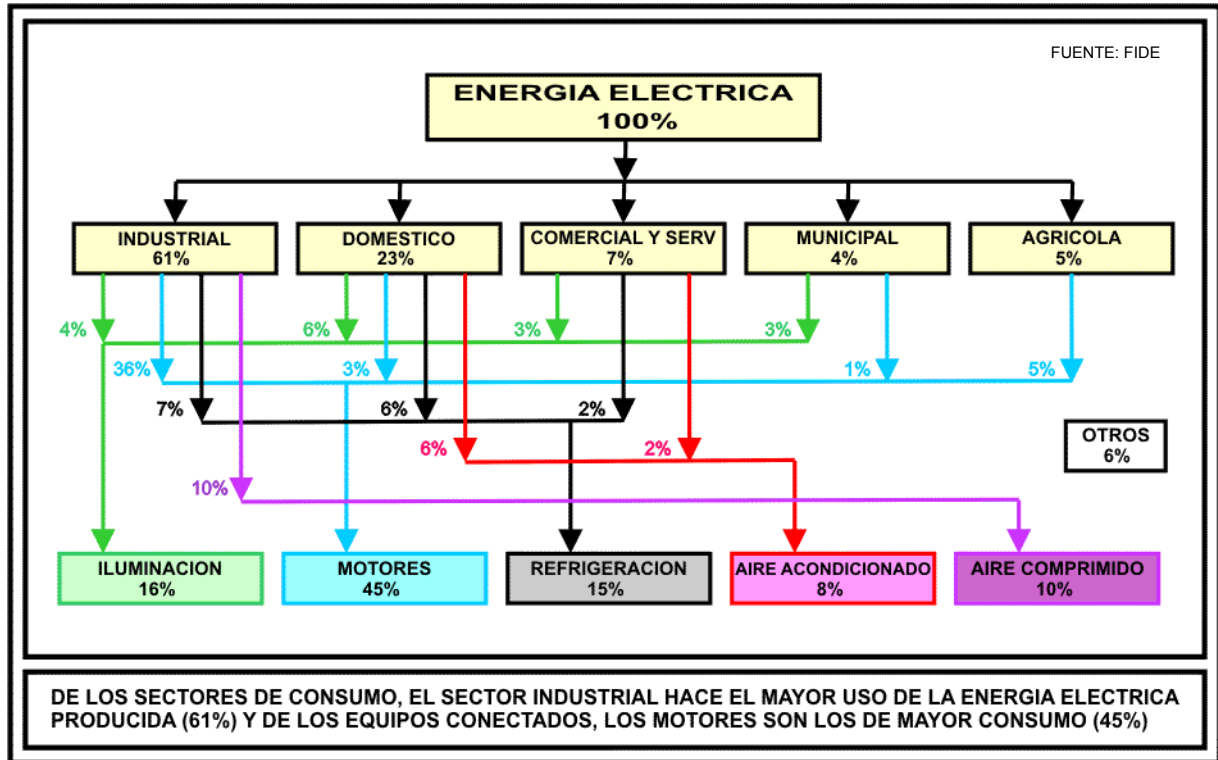


Figura 1.4 – Diagrama de distribución eléctrica en el sector de consumo

Se observa que el sector industrial es el que hace mayor uso de la energía eléctrica producida, este a su vez es uno de los sectores más competitivos y con alto grado tecnológico, entre los considerados. El hecho de competir a llevado a diversas compañías la mentalidad de dar mejores productos y/o servicios, tener mejores sistemas de producción, contar con personal idóneo para la labor, etc. pero todo ello a bajos costos de producción, tal y como lo define CEDSAL: “...las empresas han de buscar la manera de reducir los costos asociados con el uso de los recursos naturales y la energía, para lo que han de diseñar nuevos sistemas, procesos y productos que reduzcan el impacto ambiental y agreguen valor para los consumidores y la sociedad.

*Este proceso se fomenta mejor a través de una combinación de instrumentos económicos y autorregulación...*” (Empresa privada y sentido común, 1996). Esta definición muestra claramente que la realidad comercial no escapa al control eficiente de la energía eléctrica; la necesidad de cuantificar el consumo energético para facturar sus gastos en distintos periodos de producción muestra lo importante de contar con un medidor de energía. Hay que tener presente que para este sector de consumo, la versatilidad y exactitud de sus sistemas se vuelve básico para la maximización de beneficios, por ello buscarán contar con equipos que se encuentren diseñados acorde a sus necesidades y que puedan responder ante su cambiante mundo comercial.

Luego de haber presentado el análisis desde ambos enfoques, se llega a la conclusión que en cualquiera de las perspectivas, ya sea para el ecosistema a futuro como para el sector privado, surge la necesidad de contar con un equipo medidor de energía eléctrica. Ahondando un poco más, si bien el medidor de energía cumple la función de cuantificar la energía consumida se vuelve más útil un equipo que además de cuantificar dicho parámetro también pueda cubrir los otros parámetros de la electricidad como son voltajes, corrientes y los diversos tipos de potencias, con ello surge el denominado medidor de parámetros eléctricos.

## 1.2 MEDIDORES DE PARÁMETROS ELÉCTRICOS

El medidor de parámetros eléctricos, como su nombre lo indica, es un dispositivo encargado de la medición de parámetros eléctricos: Potencia activa, potencia reactiva, potencia aparente, voltaje, corriente, entre otros. Miden el consumo de dichos parámetros dentro de un circuito, servicio o sistema eléctrico al cual se hallen conectados. Según su construcción pueden ser mecánicos, electro-mecánicos o electrónicos, y según su modo de conexión a la red eléctrica, puede ser monofásicos o trifásicos.

Como toda tecnología, el desarrollo de medidores de parámetros eléctricos posee una línea evolutiva, desde sus inicios con medidores del tipo mecánicos hasta la actualidad con los medidores electrónicos o de estado sólido:

- Hacia el año 1870, la medición eléctrica se basaba en conocer el tiempo que fluyó la corriente sobre las lámparas de arco conectadas en serie. Dado que conocían previamente el voltaje requerido por lámpara y la corriente era constante.
- 1872: Samuel Gardiner saca la primera patente conocida sobre un medidor de electricidad. Este era medidor DC de horas-lámpara que tenía un electroimán que se encargaba de encender y apagar el mecanismo de un reloj.
- 1878: J.B. Fuller saca la patente de un medidor AC de horas-lámpara que tenía un reloj operado por una armadura metálica que vibraba entre dos resortes de espiral.

- 1882: Thomas Edison desarrolló un medidor químico de ampere-hora que consistía en una vasija contenedora de dos placas de zinc que se conectaban al circuito a medir. Cada mes los electrodos eran pesados y la facturación del cliente era determinada por la diferencia de peso.
- 1885: Galileo Ferrari de Turín, Italia hace el descubrimiento que dos campos de corriente alterna desfasados pueden hacer girar una armadura sólida. Este descubrimiento estimulará el desarrollo futuro de los medidores de inducción.
- 1886: El profesor Forbes de Londres, Inglaterra desarrolla el primer medidor para circuitos AC que utilizaba elementos calentadores unidos a un pequeño molino de viento conectado a un registro. Lamentablemente, este medidor era demasiado delicado para el uso comercial.
- 1889: Thomson introdujo el primer vatímetro tipo conmutador, el cual muchas empresas adoptaron como modelo "estándar". Aunque este medidor fuese diseñado en un inicio para medición AC, también dio buenos resultados con medición DC.
- 1892: Duncan desarrolla el primer vatímetro de inducción que usa un solo disco tanto para la conducción como para el elemento de frenado, este diseño nunca llegó a producirse.
- 1893: Nikola Tesla saca una patente que cubre el principio del motor de inducción propuesto por Ferrari y que más tarde sería comprada por Jorge Westinghouse.

- 1894: Shallenberger desarrolla un pequeño motor de inducción con el espiral de voltaje y corriente desfasados  $90^\circ$  el uno al otro. Este concepto fue refinado dando paso al primer vatímetro de inducción comercial, siendo este modelo uno de los más pesados (41 libras) y caros de su época.
- 1897: H. P. Davis y Frank Conrad rediseñan el medidor de Shallenberger, creando un pequeño, ligero (12 libras) y económico medidor conocido como "Tipo redondo", siendo tan popular como el vatímetro Thomson lo fuese años antes.
- 1897: General Electric introduce al mercado su primer medidor de inducción, el Thomson Induction Wattmeter. Este medidor utilizaba un rotor para el elemento conductor y un disco separado para el freno.
- 1899: GE introduce al mercado su primera tentativa de un medidor polifásico conocido como Thomson Polyphase Wattmeter. Al mismo tiempo Paul McGahan un ingeniero de Westinghouse diseña un medidor polifásico que integraba el uso de dos medidores monofásicos. Este último diseño fue adoptado por todos los fabricantes y construido en varias formas hasta 1969.
- 1899: GE crea un nuevo concepto, el medidor prepago con su nueva versión del vatímetro de Thomson.
- 1903: GE presenta el medidor Tipo I para AC, primer vatímetro producido en serie y que a su vez fue considerado como el primer medidor "moderno".

- 1904: Sangamo Electric Company, desarrolla una nueva línea basada en amperímetros con núcleo de mercurio, ampliamente desarrollados en Inglaterra en esos tiempos. No eran tan exactos como los de tipo de inducción, pero fácilmente podían ser usados en cualquier frecuencia comercial de 25Hz a 133 Hz.
- 1911: Las patentes de Tesla expiraron en diciembre de 1910, Sangamo introdujo un nuevo medidor de inducción con un disco que giraba en sentido anti-horario a diferencia de sus competidores que giraban en sentido horario.
- Finales de los años 1930: Los medidores polifásicos fueron diseñados para incorporar un disco laminado, que permitía a los estatores ser colocados juntos sin actuar recíprocamente el uno con el otro,
- Con los avances en la electrónica en los años 1970 los fabricantes comenzaron a introducir registros electrónicos y medidores automáticos de lectura.
- A mediados de los años 1980, los fabricantes ofrecían medidores híbridos con registros electrónicos montados sobre medidores de inducción.
- A principios de los años 1990, con los avances de la electrónica, los fabricantes comenzaron a producir medidores que eran totalmente electrónicos que ya no usaban ninguna etapa móvil (aparte de los interruptores solía tener acceso a varias funciones sobre los medidores).

- Hoy en día, con el auge de las telecomunicaciones la integración de los sistemas da nacimiento a una nueva tendencia en el manejo de energía en las empresas o Sistema EEM (Enterprise Energy Management, por sus siglas en inglés). El sistema EEM es una colección de software en red, medidores de parámetros eléctricos inteligentes y dispositivos de control. Un grupo de medidores son localizados en puntos clave dentro de las fuentes de energía para el consumidor tales como subestaciones, equipos, cargas, etc. (véase Figura 1.5). Su conexión es sobre toda una red de comunicaciones la cual puede incluir Internet, gíreles, teléfono, entre otros. Sobre esta red los medidores intercambian información en tiempo real, el software automáticamente se actualiza y con la información histórica de consumo la envía a una o más centrales para su proceso.

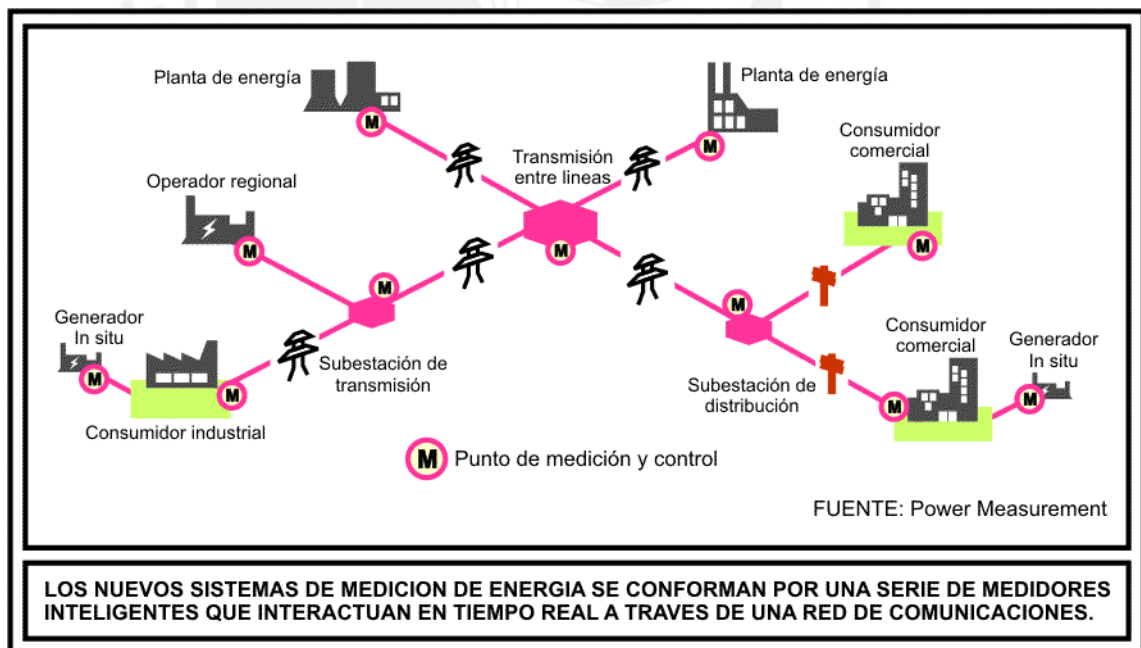


Figura 1.5 – Medidores en un sistema EEM

### 1.3 OBJETIVOS

#### 1.3.1 OBJETIVO GENERAL

Desarrollar un sistema de control digital que posea la lógica adecuada para la medición trifásica de parámetros eléctricos además de permitir la comunicación a redes de datos.

#### 1.3.2 OBJETIVOS ESPECÍFICOS

- Desarrollar la etapa básica de un equipo que contemple los principios de un sistema EEM, fusionando el área de potencia (medición de parámetros eléctricos) con el área de las comunicaciones (conexión a redes de datos).
- Estudiar las diversas tecnologías para medición de parámetros eléctricos, destacando el análisis lógico y numérico-matemático que pueda ser implementado en sistemas electrónicos digitales.
- Elaborar un equipo con capacidad de comunicación que le permita conexión a una red local por medio del protocolo TCP/IP.
- Al ser un sistema que conformará la etapa principal y básica de un sistema mayor, se le diseñará para adaptarse y expandirse respecto a necesidades futuras, previo análisis e investigación de las posibles aplicaciones.

- Desarrollar un equipo con características comerciales, por lo cual se tomarán consideraciones:

Para el chasis:

- ✓ Dimensiones: Deben ser adecuadas para que se acondicione a los equipos o soportes ya existentes (rack, paneles, tableros eléctricos, etc.)
- ✓ Material: Al trabajarse con energía eléctrica, el material de construcción del chasis debe considerar precauciones para evitar daños al equipo y/o usuarios.
- ✓ Color: Con finalidad comercial, el color debe guardar relación a otros equipos.

Para las tarjetas de componentes:

- ✓ Dimensiones: Basado en la distribución de componentes y conectores respetando las consideraciones de diseño.
- ✓ Material: Al ser la base para los componentes electrónicos, su material de construcción debe soportar corrientes de trabajo, exposición al ambiente, etc.
- ✓ Diseño electrónico: Se deben respetar conceptos teóricos de conexión para el ruteo de las pistas, máscara de componentes, además de consideraciones para evitar ruido electrónico, corrientes parásitas, efectos capacitivos, etc.
- ✓ Elección de componentes: Esta elección estará sujeta a la disponibilidad comercial de los componentes, la facilidad de conseguirse dentro del país o de importarse, además de tomar consideraciones de precios.

## CAPÍTULO 2

### TECNOLOGÍAS APLICABLES PARA LA MEDICIÓN DE LOS PARÁMETROS

#### ELÉCTRICOS Y TRANSMISIÓN DE DATOS

La investigación de las tecnologías aplicables para el desarrollo del proyecto de tesis se ha dividido en tres grupos, los cuales son consecuentes uno del otro: Primero se expondrán las tecnologías concernientes a la medición de parámetros eléctricos. Luego se presentará la tecnología del módulo de control digital, para analizar si es el adecuado a las presentadas para medición, cabe resaltar que el módulo posee integrada la etapa de comunicación a redes de datos con lo cual se cubre una de las características del proyecto. Finalmente, para la comunicación entre los módulos del equipo, se expondrán las tecnologías de interconexión entre periféricos.

#### 2.1 TECNOLOGÍAS PARA LA MEDICIÓN DE PARÁMETROS ELÉCTRICOS

La medición de parámetros eléctricos se efectúa mediante medidores o contadores, dicha medición resulta de interés para calcular la cantidad de energía facturable a los consumidores y también para conocer la cantidad de energía a través de las redes de distribución que no son traducidas precisamente en trabajo útil por falta de

compensación de cargas reactivas. Años atrás, la comercialización de la energía eléctrica se efectuaba de manera muy simple porque se facturaba en función de la unidad de energía vigente, sin embargo con el permanente desarrollo industrial, y la consecuente búsqueda del abaratamiento de la producción por parte de las fábricas, se hizo necesaria la aplicación de tarifas más complejas. La complejidad de las tarifaciones, ha logrado consecuentemente que los equipos medidores también sean más complejos. La tecnología de los medidores expondrá y dividirá: por mecanismos indicadores, por metodologías de medición y por aplicación.

### 2.1.1 MECANISMOS INDICADORES

- Instrumentos de magneto permanente y bobina móvil

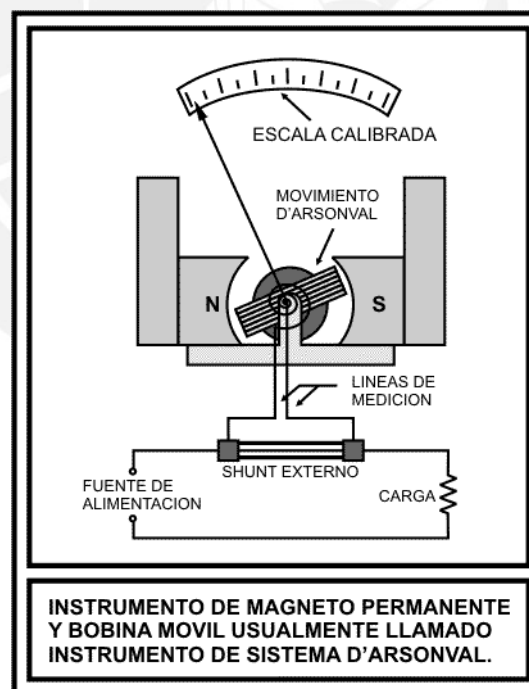


Figura 2.1 – Mecanismo básico de un medidor con magneto permanente y bobina móvil

La Figura 2.1 puede apreciarse un sistema móvil de este tipo, usualmente llamado Instrumento d'Arsonval. Utiliza una bobina que termina en un par de resortes

antagónicos en espiral, a través de los cuales circula la corriente a medir. La bobina está dentro del campo magnético casi homogéneo que produce un imán permanente y se desplaza con un movimiento giratorio. El ángulo de rotación es proporcional a la corriente que circula por la bobina. Una aguja, indica la posición de éste sobre una escala calibrada en términos de corriente o voltaje. Este mecanismo indicador sólo responde a la corriente continua y presenta una calibración casi lineal. El "shunt" magnético, que altera la intensidad del campo, se emplea para la calibración.

- **Instrumentos electrodinamométricos**

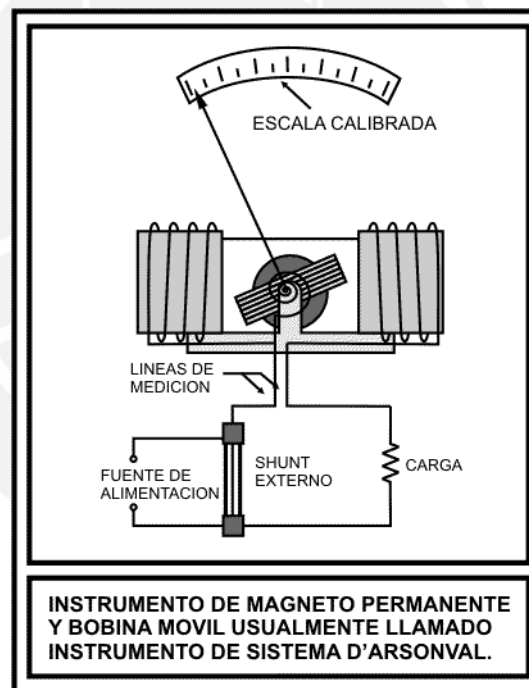


Figura 2.2 – Mecanismo básico de un instrumento dinamométrico

Un instrumento dinamométrico es muy similar al sistema D'Arsonval pero en lugar de utilizar un imán permanente posee una bobina móvil que gira en el campo establecido por la corriente de una bobina de campo que la rodea, tal y como se observa en la Figura 2.2. La escala de estos dispositivos tiene una relación cuadrática: el momento

de torsión es proporcional al producto de los amperes vuelta de la bobina móvil y los amperes vuelta de la bobina de campo. La conexión de las bobinas de campo y de la bobina móvil en serie brinda la respuesta en términos del cuadrado de la corriente, haciendo del dinamómetro un instrumento de lectura RMS para corriente o voltaje.

- **Instrumentos de hierro móvil**

Este tipo de instrumentos se emplean ampliamente a frecuencias de la red. Operan por medio de la corriente en la bobina que rodea dos aletas magnéticas, una fija y una que puede rotar de modo que aumente el espaciamiento entre ellas. La corriente en la bobina ocasiona que las aletas se magneticen de manera similar y que de esa forma se repelan entre sí. El momento de torsión producido por la aleta móvil es proporcional al cuadrado de la corriente y es independiente de su polaridad. Esto brinda las bases para la operación de CA y para la indicación RMS mediante una escala adecuada

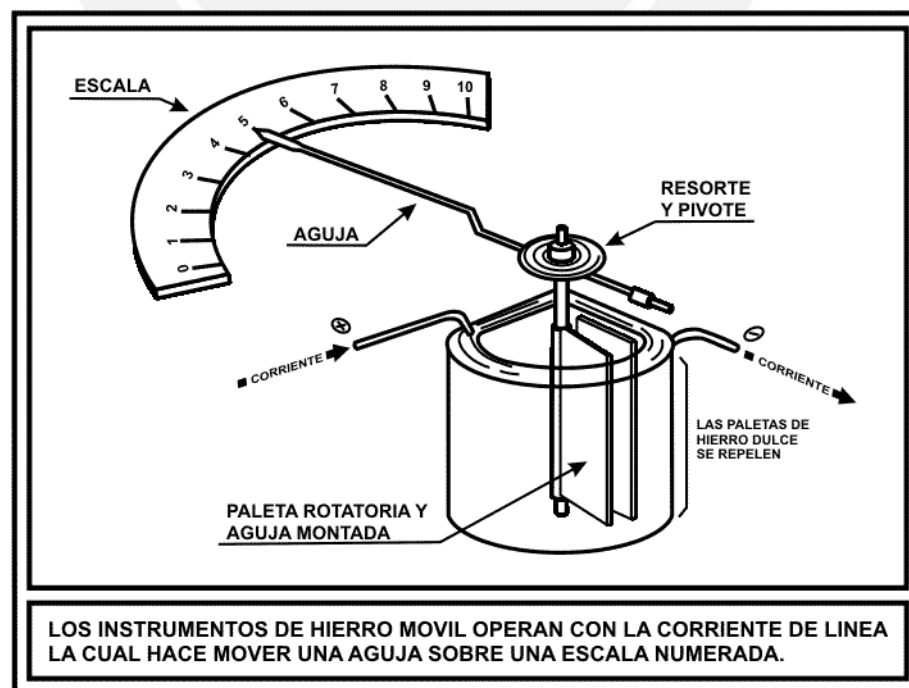


Figura 2.3 – Mecanismo básico de un medidor de hierro móvil

- **Instrumentos digitales multifuncionales**

Un instrumento digital multifuncional es un dispositivo electrónico que puede hacer mediciones de voltaje, corriente y/o resistencia; esto lo consigue al convertir la señal de entrada analógica en una representación digital, la cual puede ser muestreada como una lectura digital por el instrumento.

Los avances en la tecnología han hecho que los instrumentos digitales puedan ser capaces de obtener una gran precisión en la medición de voltajes, corrientes y resistencias alrededor de su rango de trabajo.

En cuanto a su modo de funcionamiento, las señales de entradas analógicas AC son convertidas a señales equivalentes digitales mediante unos transductores de entrada llamados Conversores Analógicos Digitales (ADC); luego, dichos valores digitales ingresan a un módulo de control dentro del equipo de medición el cual se encarga de procesar los datos ingresados y dar como resultado un valor que será equivalente al voltaje, corriente o potencia, según sea el algoritmo de control del dispositivo de medición.

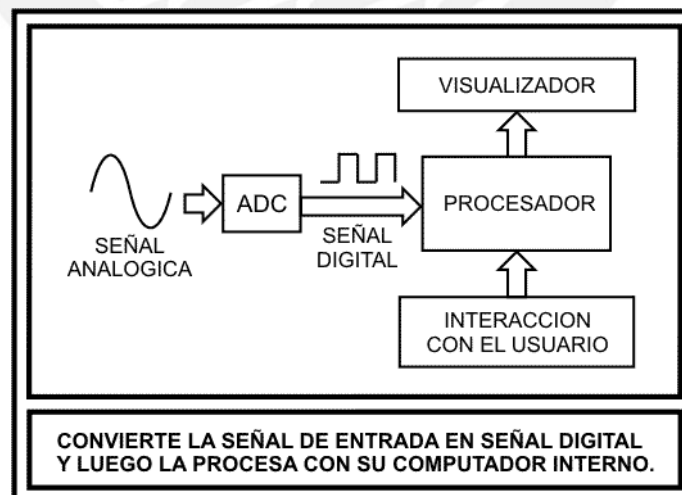


Figura 2.4 – Diagrama básico de un medidor digital

## 2.1.2 INSTRUMENTOS DE MEDICIÓN POR METODOLOGÍA

- **Medidores de voltaje y corriente rms analógica**

Para medir los valores RMS tanto de voltaje como de corriente de manera analógica, los instrumentos de medición son esencialmente electromecánicos. Aprovechan el par útil generado por la interacción entre la corriente que circula por un bobinado interno del instrumento y el campo magnético existente en el ambiente donde se encuentra dicho bobinado. Este movimiento producido por el torque generado, movimiento de D'arsonval, es usado para producir la deflexión de la aguja del instrumento.

- **Medidores de voltaje y corriente rms digital**

La metodología para calcular el voltaje o la corriente RMS de forma digital sigue la misma lógica de funcionamiento, sólo diferenciadas por el tipo de señal de entrada.

Para calcular el valor RMS, los instrumentos digitales utilizan dos métodos que se pueden definir como el método teórico y el método del filtro pasa-bajos:

### Método teórico

Consiste en aplicar el conocimiento teórico de la definición RMS, de ese modo el cálculo de una señal variable en el tiempo será:

$$F_{RMS} = \sqrt{\frac{1}{T_2 - T_1} \int_{T_1}^{T_2} f^2(t) dt} \quad \text{Ecuación 1.1}$$

Si la señal ha sido muestreada previamente, es decir se han tomado pequeños valores en ciertos periodos de tiempo, los cuales poseen una frecuencia de muestreo mucho mayor que la frecuencia de la señal variable en el tiempo, la definición vendría a ser:

$$F_{RMS} = \sqrt{\frac{1}{N} \sum_{n=1}^N f^2[n]} \quad \text{Ecuación 1.2}$$

### Método del filtro pasa-bajos

Es un método práctico para el cálculo del valor RMS y consiste que a partir de una señal muestreada como la presentada en la Ecuación 1.3:

$$f(t) = f_{\max} \cdot \text{sen}(wt) \quad \text{Ecuación 1.3}$$

sea :

$$f(t) = \sqrt{2} \cdot F_{RMS} \cdot \text{sen}(wt)$$

donde :

$$F_{RMS} = \frac{f_{\max}}{\sqrt{2}}$$

→ Elevando al cuadrado la señal muestreada

$$f^2(t) = 2 \cdot F_{RMS}^2 \cdot \text{sen}^2(2wt)$$

Considerando la razón trigonométrica :

$$2 \cdot \text{sen}^2\left(\frac{\alpha}{2}\right) = 1 - \cos \alpha$$

$$f^2(t) = F_{RMS}^2 - F_{RMS}^2 \cdot \cos(2wt) \quad \text{Ecuación 1.4}$$

→ La Ecuación 1.4 posee dos partes: una constante en el tiempo con el valor cuadrático del RMS (DC) que es nuestro valor deseado y la otra parte variable en el tiempo (AC) que contiene una señal cosenoidal no deseada. Para eliminar el valor no deseado, se aplica un Filtro Pasa Bajos (FPB) con una frecuencia de corte menor a la frecuencia de la señal AC.

Luego del filtro pasabajos :

$$f^2(t) = F_{RMS}^2$$

→ Finalmente se saca la raíz cuadrada al resultado y de ese modo se obtiene el valor RMS de la señal.

$$f(t) = F_{RMS} \quad \text{Ecuación 1.5}$$

- **Medidores de potencia activa analógica**

Este tipo de medidores se basan en rotores de discos, los cuales operan bajo el principio del electromagnetismo.

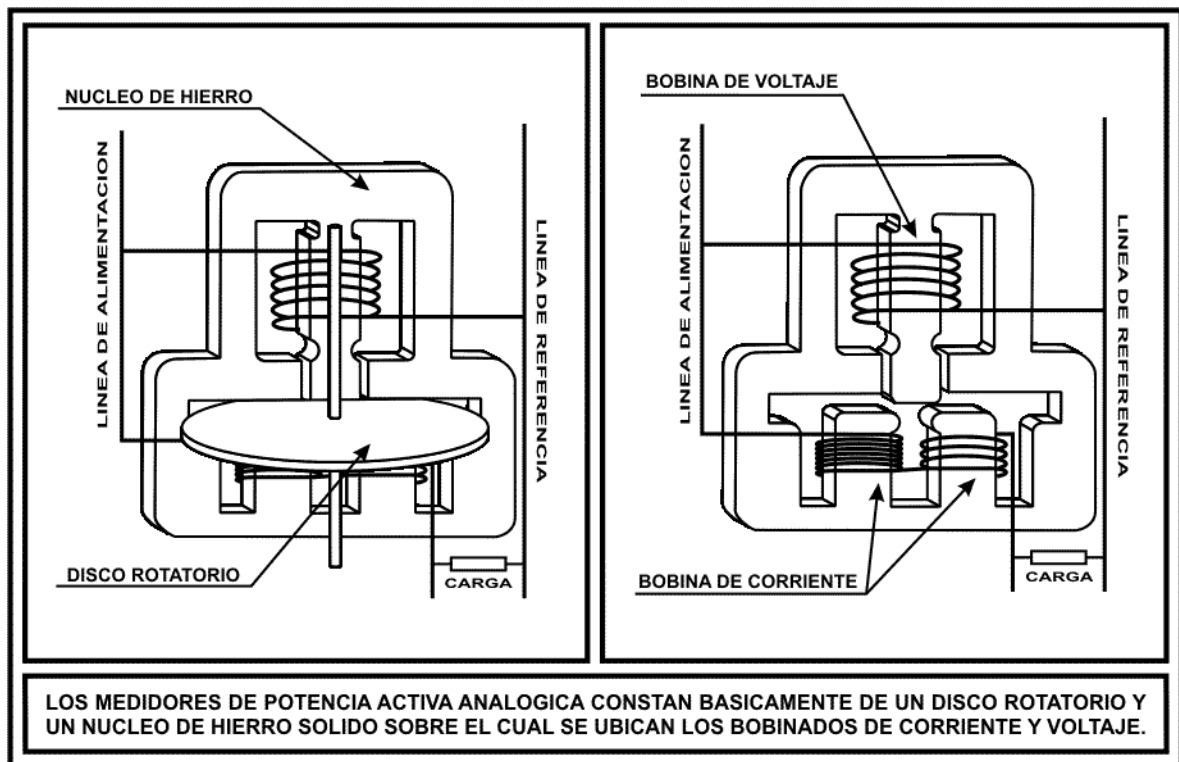


Figura 2.5 – Medidor de potencia activa analógica

Las características esenciales se muestran en la Figura 2.5, el medidor posee una bobina de voltaje conectada en paralelo con las cargas, un par de bobinas de corriente conectadas en serie y un disco de aluminio gira libremente entre los polos. El devanado de la bobina de voltaje tiene muchas vueltas y es altamente inductivo, de modo que el flujo del voltaje aplicado está retrasado en casi  $90^\circ$ , mientras que los flujos en los polos de corriente, están en fase con la corriente.

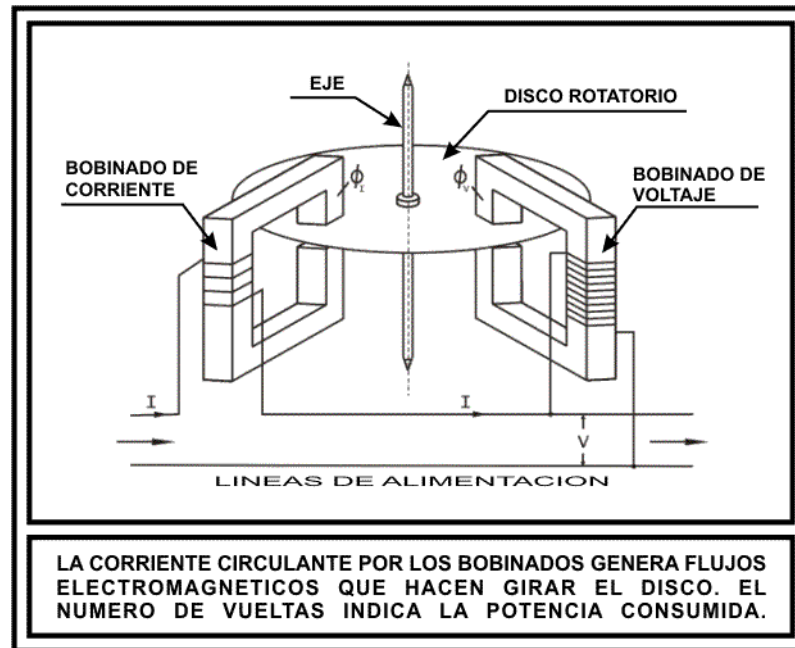


Figura 2.6 – Diagrama equivalente del medidor de potencia activa

Según la intensidad de corriente que circule por el bobinado de corriente y según el voltaje que exista entre los bornes del bobinado de voltaje, se generarán dos flujos en el núcleo, quienes a su vez inducirán corrientes de Foucault en el disco, las cuales conjuntamente con los dos flujos y gobernados por la Ley de Lenz, producirán un momento de torsión (torque) que finalmente ocasionará que el disco-rotor de aluminio gire en una dirección, la cantidad de vueltas que dé el disco será la cantidad de Potencia Activa consumida.

- **Medidores de potencia activa digital**

Para el cálculo digital, se debe considerar un paso previo para muestrear y convertir a datos binarios los valores de las señales analógicas de voltaje y corriente. Y al igual que la lógica del cálculo RMS digital, los instrumentos usan dos métodos: el método teórico y el método del filtro pasa-bajos.

Método teórico

La definición para el cálculo de la potencia activa se expresa de la siguiente manera:

$$P_{activa} = \frac{1}{nT} \int_0^{nT} p(t) = VRMS \times IRMS = V_{RMS} \times I_{RMS} - V_{RMS} \times I_{RMS} \times \cos(2\omega t)$$

Teóricamente, la potencia activa será la parte de la ecuación que no contiene componentes en frecuencia, es decir la parte DC del producto entre corriente y voltaje.

Método del filtro pasa-bajos

Este resulta el método más práctico. Para su demostración:

$$v(t) = \sqrt{2} \cdot V_{RMS} \cdot \text{sen}(\omega t) \quad \text{Ecuación 2.1}$$

$$i(t) = \sqrt{2} \cdot I_{RMS} \cdot \text{sen}(\omega t) \quad \text{Ecuación 2.2}$$

→ Por definición teórica se multiplican ambas ecuaciones (2.1 y 2.2)

$$p(t) = v(t) \cdot i(t)$$

$$p(t) = V_{RMS} \cdot I_{RMS} - V_{RMS} \cdot I_{RMS} \cdot \cos(2\omega t) \quad \text{Ecuación 2.3}$$

→ Graficando la ecuación 2.3 en función del tiempo:

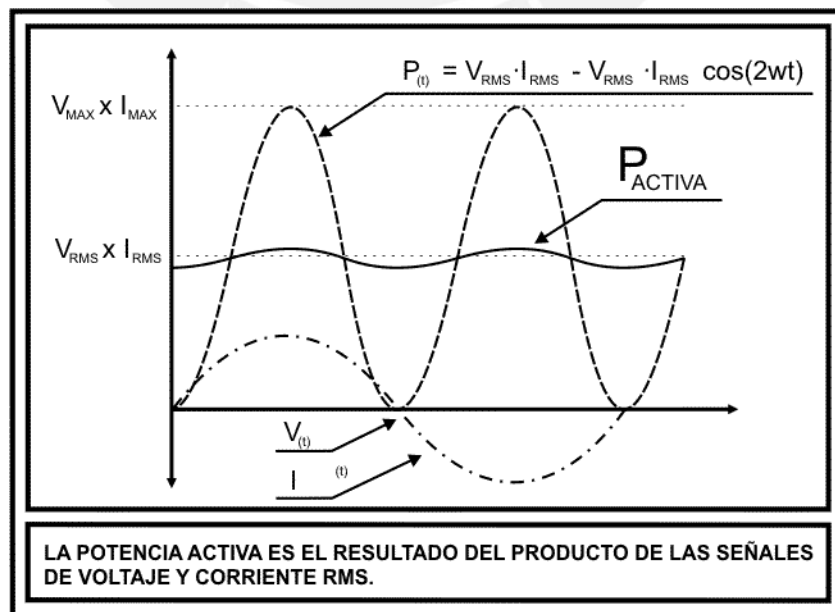


Figura 2.7 – Gráfica de señales de la potencia activa

→ La Potencia activa será la componente DC de la señal  $p(t)$  de la ecuación 2.3. Para eliminar la componente en AC de la ecuación, y por ende hallar el valor de la potencia activa, de manera práctica se aplica un Filtro Pasa Bajos (FPB) con frecuencia de corte menor a la frecuencia de la componente en AC.

$$p(t) = V_{RMS} \cdot I_{RMS}$$

Ecuación 2.4

- **Medidores de potencia reactiva analógica**

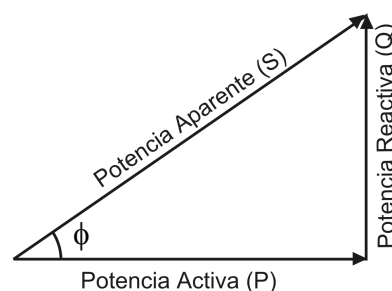
Por lo general son medidores de potencia activa ordinarios en los que la bobina de corriente se inserta en serie con la carga de la manera usual, en tanto que la bobina de voltaje se arregla para recibir un voltaje en cuadratura con el voltaje de la carga.

- **Medidores de potencia reactiva digital**

La implementación digital de la potencia reactiva se torna compleja en un sistema electrónico y más aún a un costo razonable, pues requiere un dedicado procesamiento digital de señales (DSP, por sus siglas en inglés) para el desarrollo de la transformada de Hilbert con el objetivo de hallar la constante de la condición de  $90^\circ$  por cada frecuencia. Ante esta dificultad, se han desarrollado diversas soluciones:

#### Método del triángulo de potencia

Este método está basado en el uso de las tres energías: aparente, activa y reactiva



Para hallar el valor de la potencia reactiva se puede aplicar la relación pitagórica:

$$P_{\text{reactiva}} = \sqrt{P_{\text{aparente}}^2 - P_{\text{activa}}^2}$$

**Ecuación 3.1**

Este método otorga excelentes resultados con formas de onda puramente sinusoidales (ideales), pero notables errores aparecen ante la presencia de armónicos, lo cual lo vuelve ineficiente ante señales reales, además se requeriría conocer previamente los valores de Potencia Activa y Reactiva.

### Método del retardo de tiempo con filtro pasa bajos

Un retardo de tiempo es introducido para mover una de las formas de onda en 90° de la frecuencia fundamental y finalmente multiplicar las dos formas de onda.

$$\text{Energía Reactiva} = \frac{1}{T} \int_0^T v(t) \cdot i\left(t + \frac{T}{4}\right) dt$$

**Ecuación 3.2**

Donde T es el periodo de la frecuencia fundamental. Este método puede ser implementado por el retraso de muestreo de una de las entradas en un número de ciclos igual a un cuarto de ciclo de la frecuencia fundamental. Pero se mediante el uso de un filtro pasa bajos, de manera similar se consigue un desfase de 90°.

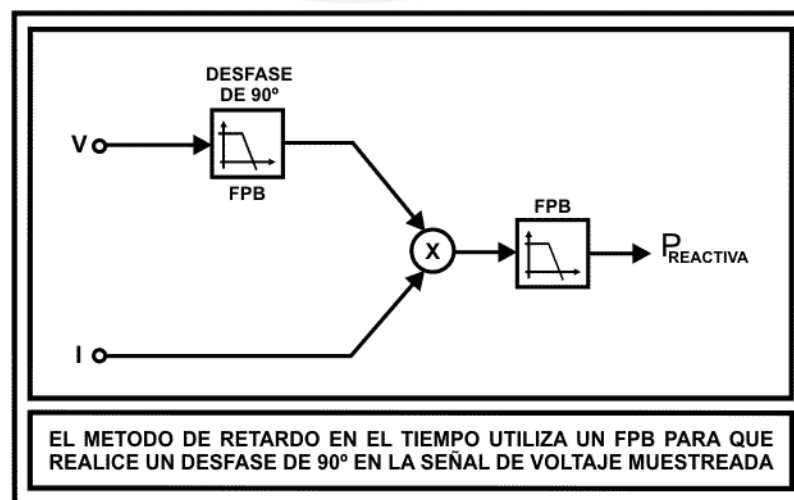


Figura 2.8 – Diagrama equivalente del método del retardo de tiempo

Si la frecuencia de corte del filtro pasa bajos es mucho menor que la frecuencia fundamental, esta solución realiza un movimiento de fase de  $90^\circ$  en toda frecuencia mayor a la frecuencia fundamental. Y al hacer esto realiza una atenuación de esta frecuencia en 20dB/década. Esta solución es susceptible a la variación de la frecuencia de línea, pero con una compensación de la atenuación de la ganancia con la frecuencia de línea puede reducir el efecto desfavorable en el cálculo.

En la Figura 2.8 el segundo FPB se encuentra para eliminar cualquier inserción de ruido en la medición.

- **Medidores de potencia aparente analógica**

Es posible calcular la energía aparente si el factor de potencia es constante (fdp) a partir de los valores de Watts-hora (P) y Var-hora (Q):

$$\text{var hora} = \sqrt{P^2 + Q^2}$$

**Ecuación 4.1**

Sin embargo, si el fdp no es constante, este método puede producir errores.

Se han propuesto diversos dispositivos para la medición directa de la energía aparente. En una clase están aquellos en los que el fdp del medidor se hace más o menos igual al fdp de línea, esto se logra insertando un miembro móvil en la estructura del polo de la bobina de voltaje, que desplaza el flujo resultante cuando cambia el fdp de línea. En otra, se emplea autotransformadores con los elementos de voltaje para obtener un fdp en el medidor, cercano al fdp de línea, se logra una exactitud de casi 1% con fdp que varían de la unidad hasta el 40%. Otra clase surge de la suma vectorial de las energías activa y reactiva se efectúa ya sea por medios electromagnéticos o electromecánicos, muchos de ellos muy ingeniosos.

- **Medidores de potencia aparente digital**

Para el cálculo de la potencia aparente se utiliza el concepto que enuncia:

$$S = V_{RMS} \cdot I_{RMS}$$

**Ecuación 5.1**

Para ello se hace referencia al método que nos permitió obtener el valor RMS en la Ecuación 1.5. Esto es, hallar el valor RMS tanto para la señal de voltaje como de la corriente y finalmente se saca el producto de ambos valores RMS, como lo expresa la Ecuación 5.1.

### 2.1.3 INSTRUMENTOS DE MEDICIÓN POR APLICACIÓN

- **Medidores monofásicos**

Hace referencia a los medidores que son diseñados para calcular el consumo de parámetros eléctricos en un sistema de distribución monofásico de 2 hilos (1 Fase y un Neutro)

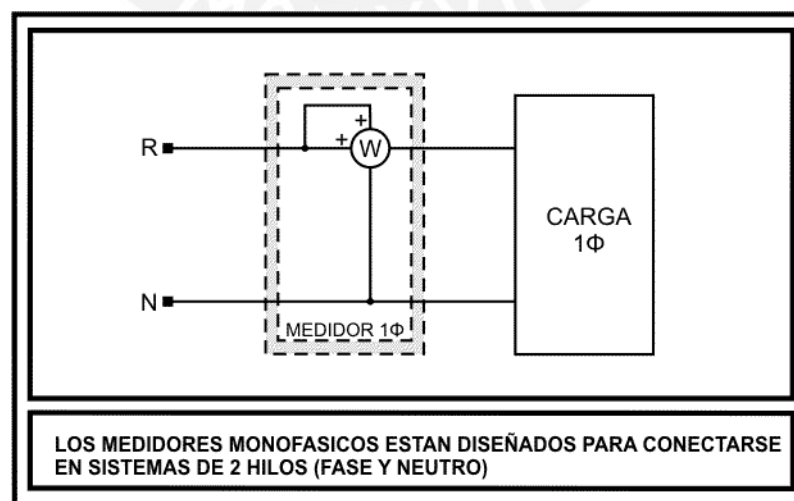


Figura 2.9 – Conexión de un medidor del tipo monofásico (1 fase – 1 neutro)

- **Medidores trifásicos**

Hace referencia a los medidores que son diseñados para calcular el consumo de parámetros eléctricos en un sistema de distribución trifásico de 3 hilos (2 Fases y un Neutro) y de 4 hilos (3 Fases y un Neutro).

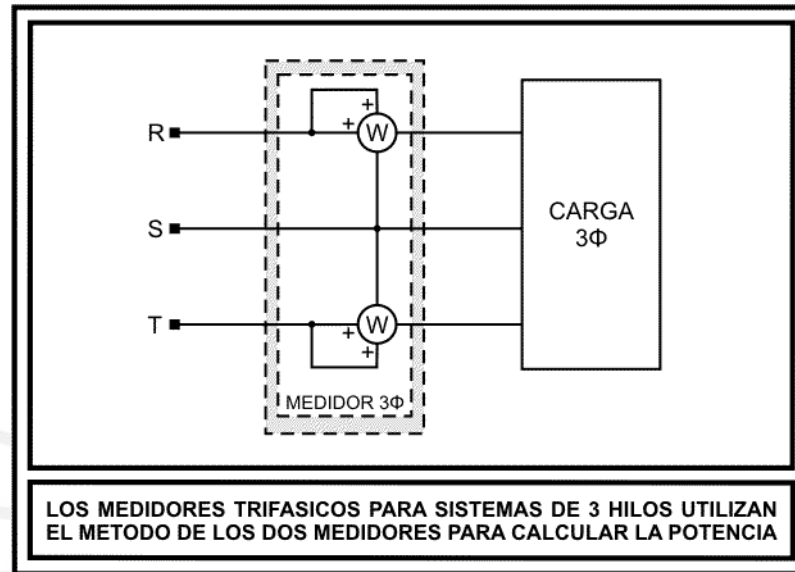


Figura 2.10 – Conexión de un medidor del tipo trifásico (3 fases)

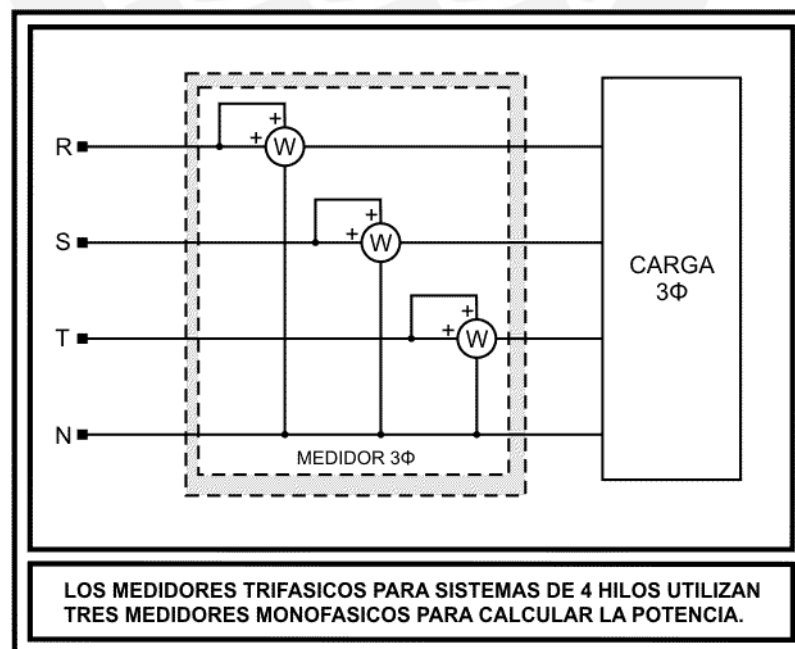


Figura 2.11 – Conexión de un medidor del tipo trifásico (3 fases – 1 neutro)

## 2.2 EL MÓDULO DE CONTROL: TARJETA TEMPUS VI

El proyecto de tesis contará con una etapa de control digital que estará cargo del módulo de procesamiento de datos y comunicaciones TEMPUS VI, desarrollada en el país por una empresa privada. Actualmente, este módulo viene siendo aplicado en dispositivos de marcación de personal y control de acceso, sin embargo por la versatilidad de su microcontrolador interno (ATmega128) y por su capacidad de comunicación TCP/IP se prevé la capacidad de ser utilizada para múltiples finalidades no contempladas en su actual funcionamiento.



Figura 2.12 – Aplicación actual de la tarjeta TEMPUS VI

En el Capítulo 3 (Sección “*Etapa de control y comunicación*”, Pág. 55), se describe detalladamente la tecnología que contiene el módulo, además se presenta el estudio que se realizó para acondicionarlo al proyecto de tesis, el cual innova su aplicación convirtiéndolo en un sistema de control digital para medición de energía.

## 2.3 TECNOLOGÍAS PARA LA INTERCONEXIÓN ENTRE PERIFÉRICOS

La comunicación entre periféricos electrónicos es el transporte información, enviadas mediante señales analógicas o digitales, por un medio físico. El tipo de comunicación es diversa y en distintos niveles; para el objeto que nos ocupa el proyecto se encargará de comunicar circuitos integrados dentro de una misma tarjeta o módulos. Para este fin, quedaría analizar las diversas soluciones aplicables: Por un lado tenemos a los circuitos integrados con lógicas de comunicación cuya aplicación genera mayores costos por el uso de hardware adicional, sin embargo cuenta con gran flexibilidad en el transporte de datos; y por otro lado tenemos las lógicas de buses seriales que no requieren hardware adicional, por ende más económicas, pero con cierta complejidad en programación. Por la comodidad y economía, se optará por la comunicación por bus serial la cual puede ser: Estándares RS, SPI, I<sup>2</sup>C, 1-Wire.

### 2.3.1 RECOMMENDED STANDARD 232-C (RS-232)

Inicialmente denominado EIA232C y renombrando como RS-232-C a inicios de 1990. Es la norma de comunicación serie asíncrona más popular y aceptada por la industria. Su conexión de transmisión es punto a punto, es decir un emisor y un receptor, utiliza la referencia a tierra para poder distinguir los valores de voltaje entre su comunicación.

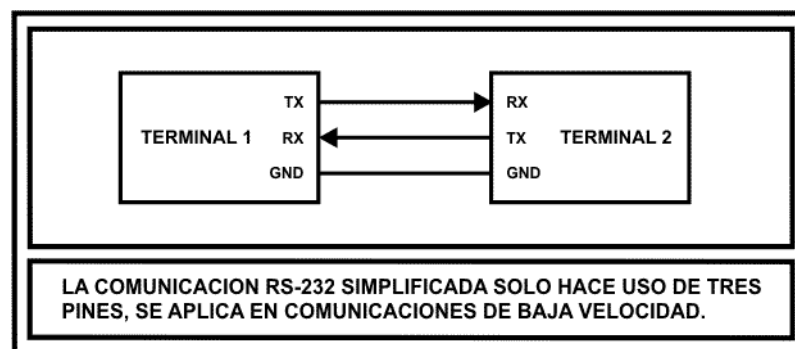


Figura 2.13 – Comunicación RS-232 de 3 hilos

### 2.3.2 SPI (SERIAL PERIPHERAL INTERFACE BUS)

El bus SPI (algunas veces llamado “spy”) es un estándar de comunicación de datos serial síncrono diseñado por Motorola que opera en modo full duplex. Los dispositivos conectados se comunican en modo Maestro/Esclavo, siendo el dispositivo Maestro aquel que mantiene la sincronización. Es una comunicación multipunto, es decir, puede existir un Maestro y múltiples Esclavos, elegidos por medio de un selector (SS).

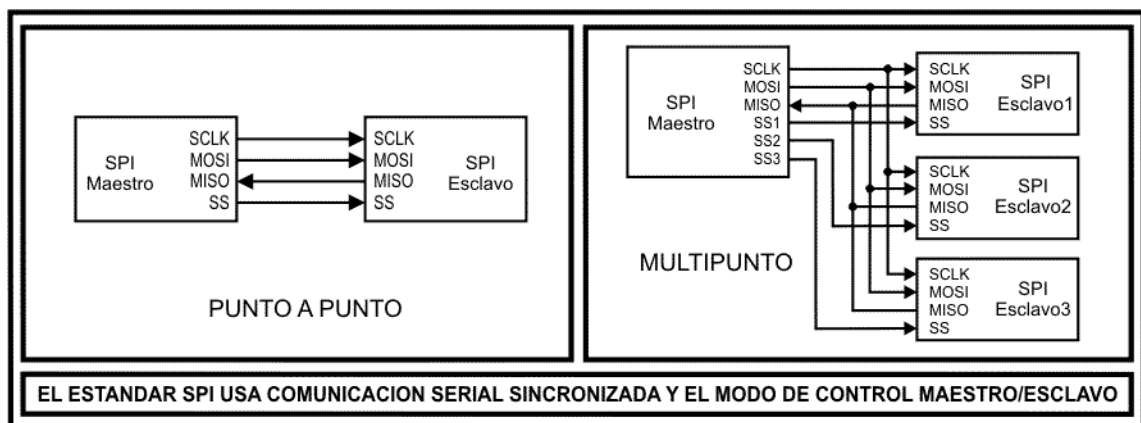


Figura 2.14 – Protocolo SPI

### 2.3.3 I<sup>2</sup>C

La comunicación de Circuitos Inter-Integrados (I<sup>2</sup>C, por sus siglas en inglés) fue desarrollada y patentada por Philips. El I<sup>2</sup>C sólo usa dos hilos para transmitir la información: uno para los datos y otro para la señal de sincronización. También es necesaria una tercera línea, la referencia. Se les denomina multimaestros, pues no necesariamente el maestro debe ser el mismo dispositivo.

### 2.3.4 1-WIRE

Protocolo diseñado por Dallas Semiconductor, provee datos a baja velocidad, señales y alimentación sobre una única línea (una línea de tierra también es necesaria). Su concepto es similar al del I<sup>2</sup>C, pero con menores velocidades de comunicación y a un costo más bajo. Pero complejo de implementar.

## 2.4 CONCEPTUALIZACIONES GENERALES

- **TCP/IP**

Es un protocolo DARPA, siglas en inglés de la Agencia de Investigación de Defensa de Proyectos Avanzados, que proporciona transmisión fiable de paquetes de datos sobre redes, recibe el nombre por la unión de dos definiciones: Protocolo de Transmisión y Control; y Protocolo de Internet, o TCP e IP, por sus siglas en inglés respectivamente. Su aplicación es la de enlazar computadoras que utilizan diferentes sistemas operativos, incluyendo PC, minicomputadoras y computadoras centrales sobre redes de área local y área extensa.

- **Transformada de Hilbert**

Definición utilizada en matemáticas y en procesamiento de señales, la transformada de Hilbert ( $\mathcal{H}$ ), es una herramienta útil para describir la envolvente compleja de una señal modulada por una portadora real. Su definición es:

$$\hat{s}(t) = H\{s\}(t) = (h \times s)(t) = \frac{1}{\pi} \int_{-\infty}^{+\infty} \frac{s(\tau)}{t - \tau} d\tau$$

Donde:

$$h(t) = \frac{1}{\pi t}$$

La transformada de Hilbert produce el efecto de desplazar la componente de frecuencias negativas de  $s(t)$  en  $+90^\circ$  y las parte de frecuencias positivas en  $-90^\circ$ . Es el concepto teórico base para el cálculo de potencia reactiva.

- **Firmware**

El Firmware es un bloque de instrucciones de programa, usualmente grabado en un microcontrolador, cuya función es establecer la lógica de más bajo nivel que controla los circuitos electrónicos de un dispositivo de cualquier tipo. Al estar integrado en la electrónica del dispositivo es en parte hardware, pero también es software, ya que proporciona lógica y se dispone en algún tipo de lenguaje de programación. Funcionalmente, el firmware es el intermediario (interfaz) entre las órdenes externas que recibe el dispositivo y su electrónica, ya que es el encargado de controlar a ésta última para ejecutar correctamente dichas órdenes externas.

- **Driver**

Un controlador de dispositivos, o driver en el inglés, es un programa informático que permite al sistema operativo interactuar con un periférico, haciendo una abstracción del hardware y proporcionando una interfaz para usarlo. Se puede esquematizar como un manual de instrucciones que le indica cómo debe controlar y comunicarse con un dispositivo en particular. Por tanto, es una pieza esencial, sin la cual no se podría usar el hardware.

La diferencia con el firmware es que el driver se ejecuta sobre un sistema operativo y no directamente sobre la electrónica del dispositivo, es decir, el driver se encarga de indicar las respectivas instrucciones que utilizará el sistema operativo para controlar algún dispositivo específico; en tanto el firmware indica, ejecuta y controla los dispositivos a los que se halla conectada la electrónica.

- **Electricidad: Voltajes y frecuencias**

El sistema de generación y distribución de corriente alterna trifásico fue inventado por Nikola Tesla en el s. XIX. Él consideró a 60Hz la mejor frecuencia para la distribución de corriente alterna (CA) y 240V el mejor voltaje para circuitos de larga distribución. Muchas diferentes frecuencias se usaron en el s. XIX, y tempranamente en el s. XX la mayoría de la potencia se producía a 60Hz (Norteamérica) o 50Hz (Europa, mayoría de Asia). En el Reino Unido, diferentes frecuencias (incluyendo 25Hz, 40Hz, y CC) proliferaban, y el estándar 50Hz fue establecido luego de la segunda Guerra Mundial.

Toda Europa, gran parte de África y Asia usan 230V ( $\pm 10\%$ ), mientras Japón, Norteamérica, algunas partes de Sudamérica usan de 100 a 127V.

- **Ruido eléctrico**

Se denomina ruido eléctrico a todas aquellas señales, de origen eléctrico, no deseadas y que están unidas a la señal principal o útil de manera que la pueden alterar produciendo efectos que pueden ser más o menos perjudiciales.

La principal fuente de ruido es la red que suministra la energía eléctrica, y lo es porque alrededor de los conductores se produce un campo magnético a la frecuencia de 50 ó 60Hz. Además por estos conductores se propagan los parásitos o el ruido producido por otros dispositivos eléctricos o electrónicos.

## 2.5 MODELO TEÓRICO

Luego de analizar las respectivas tecnologías para medición de parámetros eléctricos presentadas, la alternativa adecuada a los requerimientos del sistema de control resulta ser la tecnología digital que permite la mejor adaptación entre módulos y la capacidad necesaria para realizar el procesamiento matemático.

Además, es importante señalar que el Equipo de medición trifásica de parámetros eléctricos comprende dos partes básicas: El Acondicionamiento de datos y el **Sistema de control digital**, siendo esta última la más importante por ser el núcleo del equipo. Como se observa en la Figura 2.15, la unión del Equipo de medición trifásica con la Interfaz remota da origen a un Sistema mayor de medición trifásica de parámetros eléctricos, conformando de esta manera un Punto de Medición y control que tiene todo Sistema EEM, véase Capítulo 1 (Sección “Medidores de parámetros eléctricos” Pág.12)

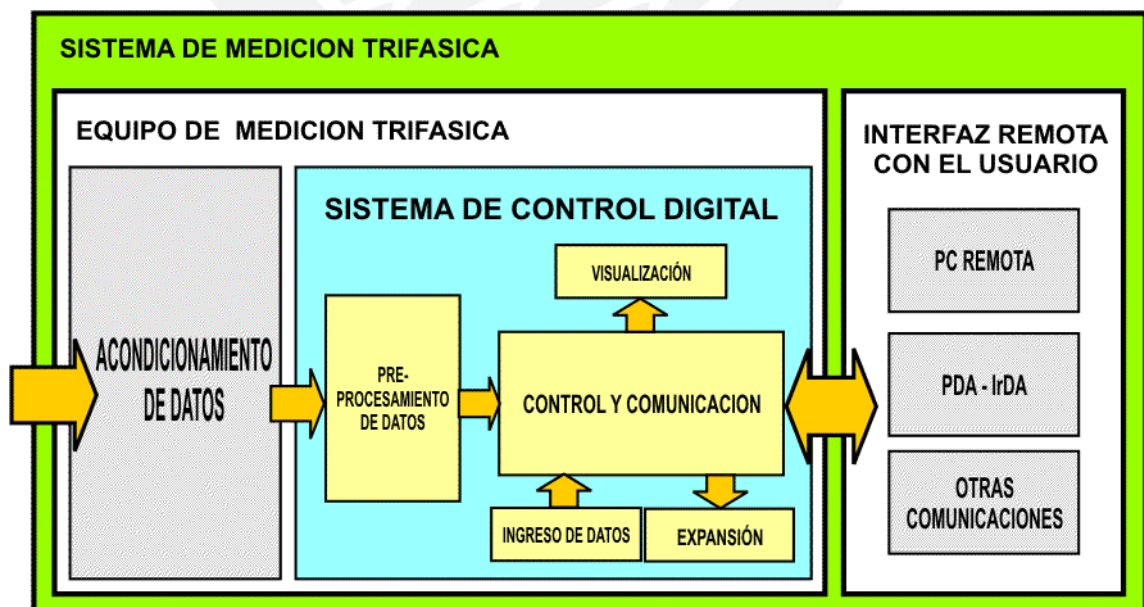


Figura 2.15 – Diagrama del sistema de medición trifásica

Este proyecto de tesis busca desarrollar la parte más importante del Equipo de medición trifásica: el **Sistema de control digital**, el mismo que contendrá toda la lógica de control para realizar el procesamiento digital y la comunicación entre dispositivos. Este equipo recibirá la señal eléctrica externa ya digitalizada, la procesará con la lógica numérico-matemática de medición adecuada y podrá interactuar con el usuario mediante visualizadores; luego podrá enviarla mediante TCP/IP hacia alguna interfaz remota. El prototipo no llegará a realizar medición alguna, pero contendrá el sistema de control digital para la medición, siendo esta etapa la más compleja e innovadora del desarrollo.

En la Figura 2.15, se presentan las etapas denominadas como **Acondicionamiento de datos** e **Interfaz remota con el usuario** la cuales se encargan de convertir la señal eléctrica de 220VAC, 380VAC, 440VAC a valores adecuados para el procesamiento y la comunicación con el usuario final, respectivamente; cabe precisar que dichas etapas no serán consideradas en el desarrollo del proyecto de tesis, la primera por ser íntegramente eléctrica y la segunda por ser exclusivamente de programación. Sin embargo, se ha investigado al respecto y se presentan algunos alcances para su desarrollo en el Anexo B: Comunicación IrDA (*Sección “Comunicación IrDA”, Pág. 3*) y en el Anexo C: Tecnologías para medición de corriente (*Sección “Tecnologías para medición de corriente”, Pág. 9*).

### CAPÍTULO 3

#### DISEÑO E IMPLEMENTACIÓN DE LA INTERFAZ DIGITAL

El sistema de control digital para medición consta básicamente de 5 etapas: Pre-procesamiento de datos, visualización, ingreso de datos, expansión, control y comunicación. La distribución de las mencionadas etapas es la siguiente:

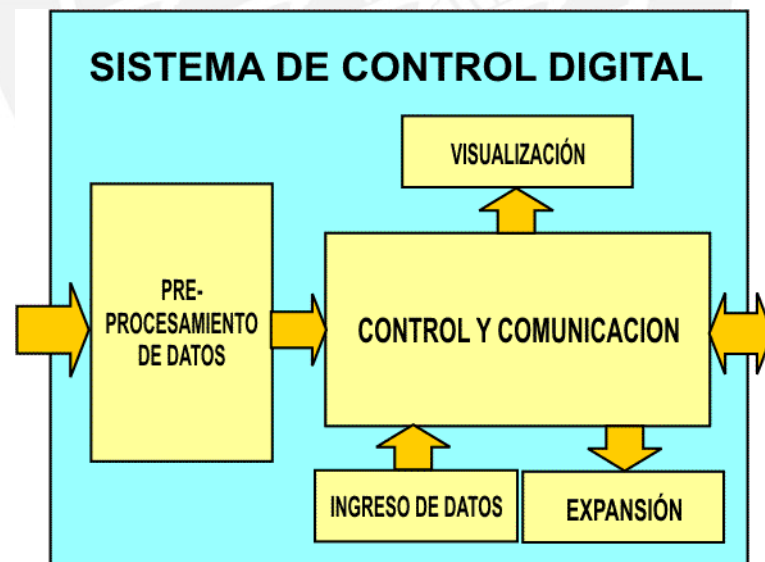


Figura 3.1 – Diagramas de bloques de la interfaz digital

Para el diseño de cada etapa se realizó una investigación respecto de componentes y consideraciones de diseño acordes con la tecnología a aplicar.

### 3.1 ETAPA DE PRE-PROCESAMIENTO DE DATOS

#### A) PRE-PROCESADOR DE PARAMETROS ELÉCTRICOS

##### Descripción

El pre-procesador de parámetros eléctricos se encarga de recibir la señal analógica acondicionada de la red, digitalizarla, evaluarla y procesarla para convertirla en un dato que pueda ser entendido por un microcontrolador. El tipo de pre-procesador dependerá en gran parte de las características de la red eléctrica a la cual se requiera conectar el dispositivo, para ello el pre-procesador podrá ser del tipo monofásico o trifásico.

##### Criterios de selección

Para el proyecto se seleccionará un pre-procesador de parámetros eléctricos que pueda cubrir los requerimientos físicos y eléctricos del sistema a desarrollar.

Como nuestro tipo de red eléctrica será trifásica, será necesario el uso de un dispositivo que pueda sensor valores trifásicos en sus diversas configuraciones: delta ( $\Delta$ ) y estrella (Y). El equipo llegará a ser más óptimo en cuanto permita sensor la mayor cantidad de parámetros eléctricos de la red, entre los cuales, los que ocupan nuestro campo de interés serán: Medición de energías (Potencia activa, reactiva y aparente), medición RMS de voltajes y corrientes. Se espera que el mismo pueda ser reconfigurado y recalibrado, para efectos de pruebas y/o experimentaciones.

Considerando que este elemento pre-procesador será un dispositivo que actuará como Esclavo (Slave, por su nombre en inglés) de un controlador principal, será muy útil que cuente con una interfaz de programación e intercambio de datos cómoda y fiable, esto con el objetivo de reducción de pines en el Maestro (Master, por su nombre en inglés).

Según los modos de comunicación estudiados en el Capítulo 2 (Sección “Tecnologías para la interconexión entre periféricos”, Pág. 31), se elegirán dispositivos que cuenten con el protocolo de comunicación síncrona SPI.

### Componente seleccionado

De las compañías fabricantes de estos dispositivos de medición, se ha elegido un integrado de la familia ADE de *Analog Devices*, cuyo código es ADE7758 que cumple con los criterios de selección requeridos, además de poseer características adicionales como la de muestrear la señal sensada, es decir, muestrear los valores de voltaje, corriente, potencia activa, reactiva y aparente para que puedan ser graficados en función del tiempo; medición de la frecuencia de la señal de la red; detector de sobretensiones de la red; indicador de desbalance de voltaje; sensor de la temperatura del dispositivo; así también, cumple con estándares internacionales de la Comisión Electrotécnica Internacional, IEC por sus siglas en inglés, que son: IEC 60687, IEC 61036, IEC 61268, IEC 62053-21, IEC 62053-22 y IEC 62053-23. Véase Anexo F: Hojas técnicas (Hoja técnica del ADE7758. Rev. C - Sección “Features”, Pág. 1).

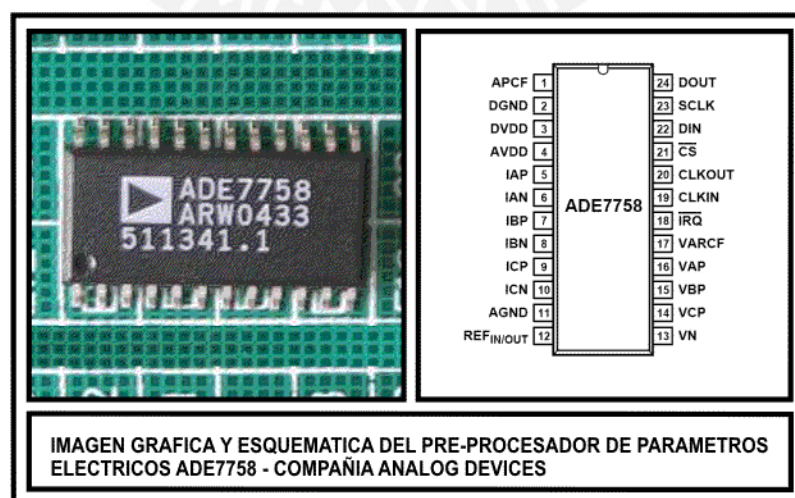


Figura 3.2 – Pre-procesador ADE7758

Como dispositivo el ADE7758 posee interfaz serial de cuatro hilos compatible con SPI, que permite la comunicación entre microcontroladores. Sensor de temperatura incorporado. Disponibilidad de 18 registros de datos (6 de solo lectura y 12 de lectura y escritura), accesible a través de la interfaz serial desde un registro maestro de comunicaciones. Ancho de banda nominal de 14kHz. Variación típica en la frecuencia de salida del orden de 0,2%. Entradas analógicas de alta impedancia (390K $\Omega$  mínima), capaces de aceptar señales hasta de  $\pm 1V$ . Opera con frecuencias de reloj desde 1MHz hasta 10MHz. Entradas y salidas lógicas compatibles con TTL y CMOS. Alimentación a partir de una fuente sencilla de +5VDC regulada. Bajo consumo de potencia (15mW, típico). Rango de temperaturas de desde  $-40^{\circ}C$  hasta  $+85^{\circ}C$ .

En el Capítulo 2 (Sección “Instrumentos de medición por metodología”: Ecuación 1.5, Pág.21; Ecuación 2.4, Pág.25; Ecuación 3.2, Pág.26; Ecuación 5.1, Pág.28) se expusieron las teorías y fórmulas de medición digital, tecnología que usa el ADE7758 para sus cálculos, por ello no se ahondará nuevamente en explicaciones al respecto y se mostrarán los diagramas de bloques para el pre-procesamiento de datos.

- **Medición RMS**

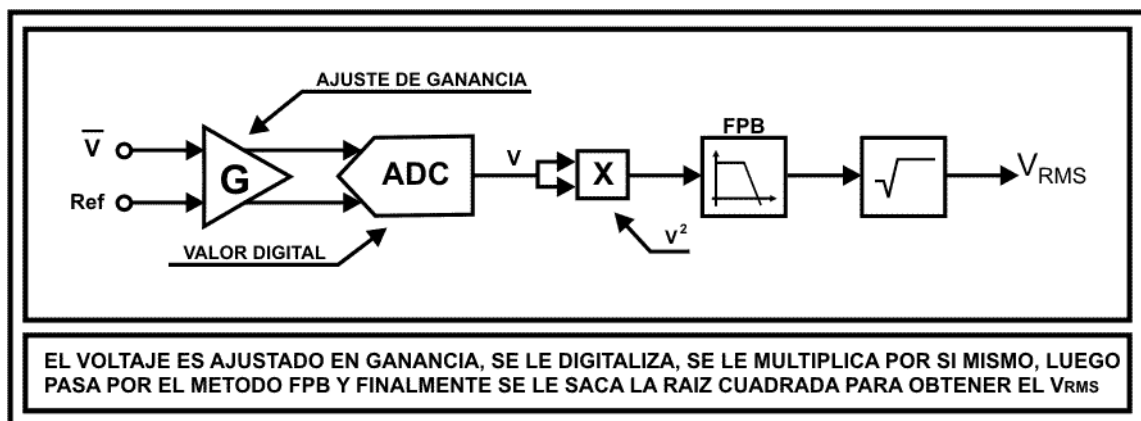


Figura 3.3 – Diagramas de bloques de la medición de voltaje RMS

- Medición de potencia activa

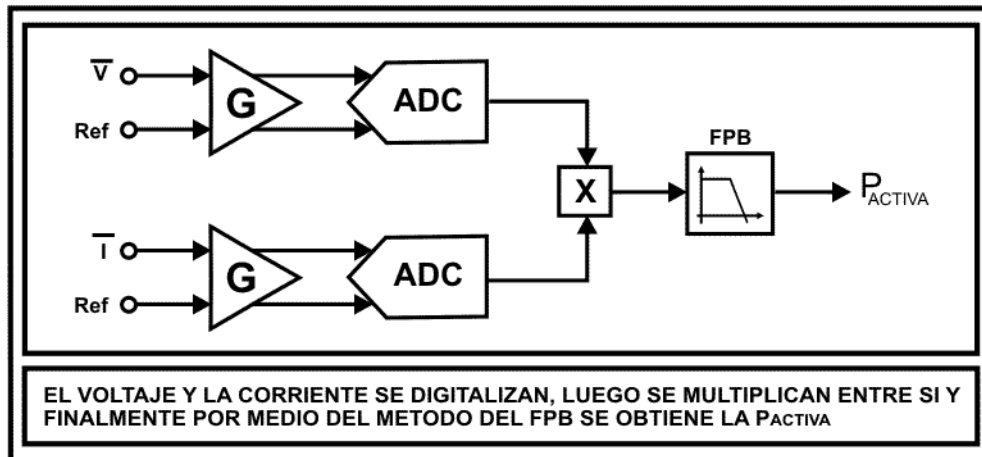


Figura 3.4 – Diagramas de bloques de la medición de potencia activa

- Medición de potencia reactiva

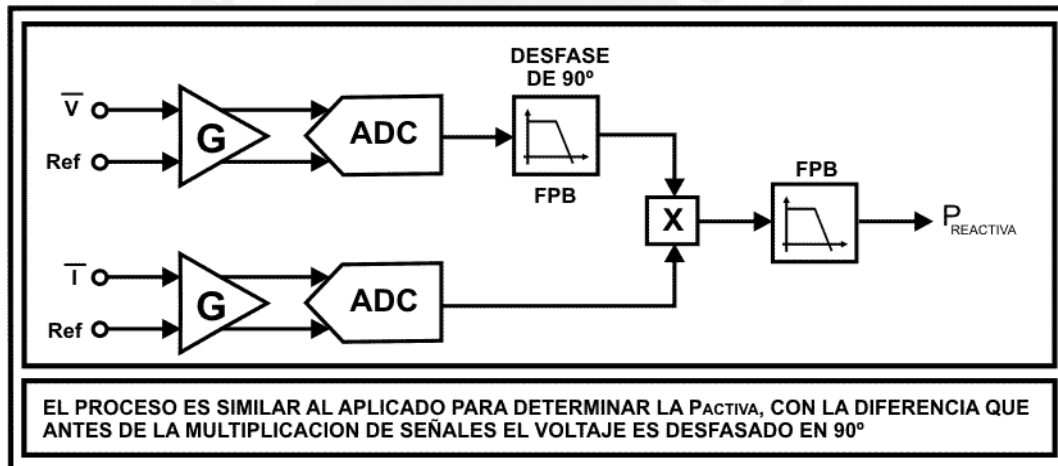


Figura 3.5 – Diagramas de bloques de la medición de potencia reactiva

- Medición de potencia aparente

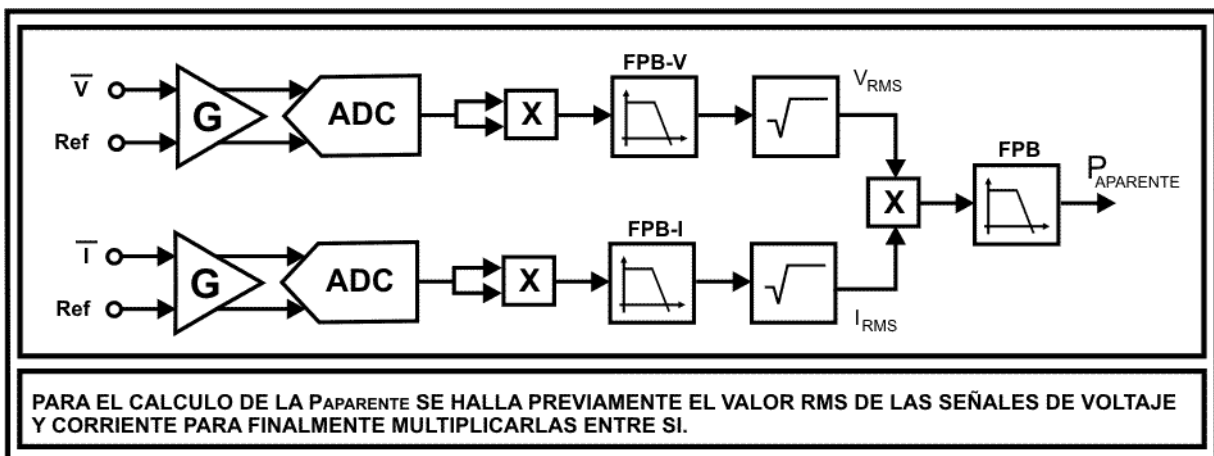


Figura 3.6 – Diagramas de bloques de la medición de potencia aparente

En cuanto a su funcionamiento, el ADE7758 realiza el cálculo de potencia mediante lógicas numérico-matemáticas digitales, en la Figura 3.7 se puede observar los pasos para el cálculo de la potencia activa.

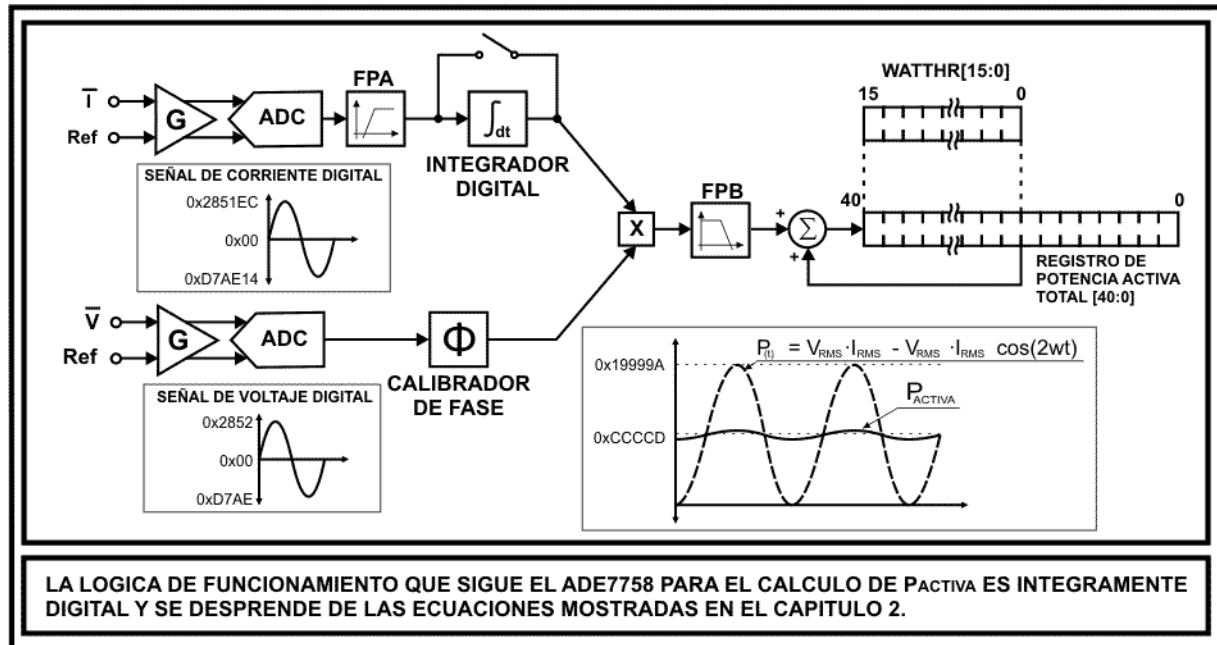


Figura 3.7 – Lógica de funcionamiento del ADE7758 para el cálculo de potencia

La señal de corriente analógica ingresa y es ajustada por una Ganancia (G) programable, luego se le digitaliza siendo sus valores digitales a máxima escala  $\pm 2642412$ , o con signo y complemento a 2: 0x2851EC y 0xD7AE14 para el máximo y mínimo respectivamente, después pasa por un filtro pasa-altos (FPA) para remover algún posible desplazamiento en DC (offset DC, en inglés), luego se puede optar por la señal acondicionada o pasarlo previamente por un integrador digital, esta última opción se aplica cuando la entrada de corriente pasa por una bobina de Rogowski, esto se detalla en el Anexo C: Tecnologías para medición de corriente (Sección “Bobina Rogowski”, Pág. 11) y Anexo F: Hojas técnicas (Hoja técnica del ADE7758. Rev. C.- Sección “di/dt current sensor and digital integrator”, Pág. 20). Por otro lado, la señal de

voltaje analógica sigue el mismo proceso de ajuste de ganancia y digitalización, siendo sus valores digitales a máxima escala  $\pm 10322$ , o con signo y complemento a 2: 0x2852 y 0xD7AE para el máximo y mínimo respectivamente, que luego llega a una etapa en donde se puede hacer un ajuste de fase ante cualquier posible error inducido por los sistemas de baja potencia. El FPA no está implementado en el canal de voltaje porque el FPA de la corriente es suficiente para eliminar el desplazamiento en DC. Después las señales de corriente y voltaje se multiplican entre si para finalmente aplicar el método del filtro pasa-bajos explicado el Capítulo 2 (Sección “Medidores de potencia activa digital”, Pág. 24). La acumulación del valor de la potencia activa total se almacena en un registro de 40 bits, el cual es constantemente actualizado según frecuencia del reloj del sistema, sin embargo el valor entregado es el registro denominado WATTHR que contiene los 16 MSB del mencionado registro acumulador, esta denominación la entrega el fabricante en su hoja de datos, Anexo F: Hojas técnicas (Hoja técnica del ADE7758. Rev. C.- Sección “Register”, Pág. 60).

Supóngase que se desea conocer cuál es el valor de energía consumida en Watt-hora cada vez que se llena el registro interno. Para esto se necesita conocer con que valores de tensión y corriente funcionará el dispositivo; utilizando valores estándar de medición: tensión nominal de 220V, corriente nominal de 10A y corriente máxima de 50A. Entonces calculando con señal máxima se obtiene:  $P = 220V \times 50A = 11000W$ . Con señal sinusoidal máxima en las entradas analógicas, el valor digital promedio de la potencia activa es 0xCCCCD (ver Figura 3.7). El máximo valor que puede almacenarse en el registro antes que sobresature es  $2^{40} - 1$  ó 0xFF FFFF FFFF, el tiempo de integración calculado en estas condiciones cumplirá la Ecuación 6.1.

$$E = \frac{0xFF FFFF FFFF}{0XCCCCD} \times \frac{4}{\text{freq. de clock}}$$

Ecuación 6.1

Considerando que en nuestro caso se utilizó un oscilador de 10MHz, se tiene:

$$E = 11000W \times \frac{4}{10Mhz} \times \frac{1h}{3600s} = 1.60Wh$$

Por lo tanto cada vez que se llene el registro interno se habrá consumido una cantidad de energía igual a 1.6Watt-hora.

## B) FILTROS PASIVOS DE SEÑAL

### Descripción

Encargados de separar la señal eléctrica de los efectos del ruido de la red.

### Criterios de selección

Se sabe por cuestiones teóricas que los valores entre los cuales oscila la energía eléctrica, según la zona, están entre 50 y 60Hz, mientras que el ruido eléctrico se encuentra a frecuencias superiores, entonces los filtros a utilizar serán del tipo Pasa-bajos, que dejarán pasar la señal eléctrica e impedirán el paso del ruido no deseado. Según el fabricante en el Anexo F: Hojas técnicas (*AN-559: Application note. Rev. A.- Sección "Antialias filter", Pág. 4*). Para digitalizar las señales de voltaje y corriente, el ADE7758 usa ADCs de alta velocidad de muestreo, alrededor de los 900kHz, y por lo tanto posee una banda de interés entre 0 y 2 kHz que se desea proteger del ruido eléctrico pues la señal de 900kHz se refleja en frecuencia a los 450kHz. Adicionalmente, el fabricante asegura que no se opte por un filtro de gran precisión, recomendando el filtro RC.

### Componentes seleccionados

Los valores de diseño recomendados por Analog Devices para el Filtro RC son:  $R = 1k\Omega$ ,  $C = 33\text{ nF}$ , cuya respuesta en magnitud y fase se presenta en la Figura 3.8. Se puede ver que la atenuación a los 900kHz para este simple FPB es mayor a los 40dB, lo cual representa la suficiente atenuación para asegurar que no se presentarán efectos de ruido.

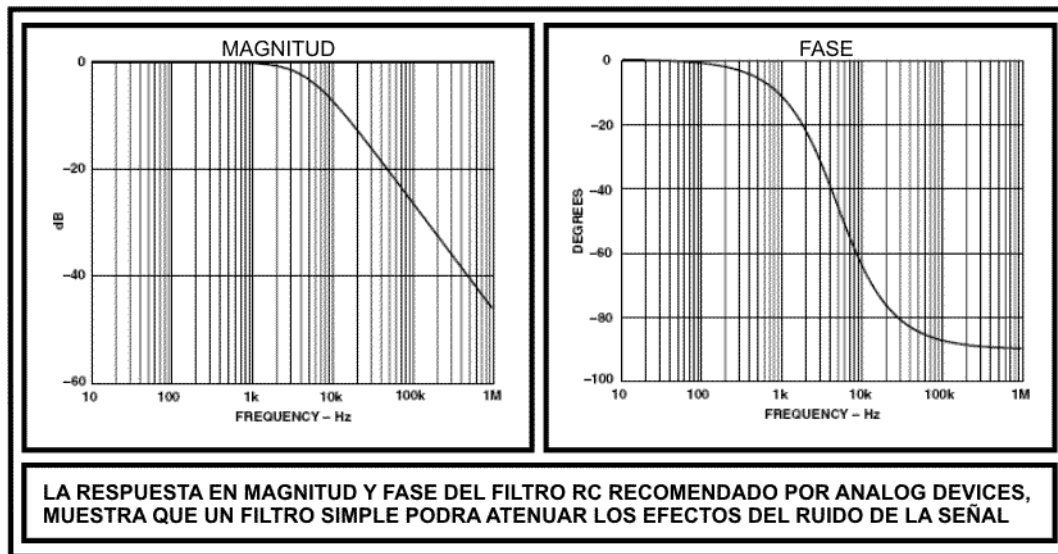


Figura 3.8 – Respuesta en frecuencia del filtro RC ( $R = 1\text{ k}\Omega$ ,  $C = 33\text{ nF}$ )

Adicionalmente, por la ecuación del filtro RC:  $F_c = \frac{1}{2\pi \times RC}$  y con los valores de diseño

$R = 1K\Omega$  y  $C = 33\text{ nF}$ . Se tiene una frecuencia de corte de de y diseño:

$$F_c = \frac{1}{2\pi \times (1000)(33 \times 10^{-9})}$$

$$F_c = 4822.877063\text{ Hz}$$

$$\Rightarrow F_c \approx 5\text{ KHz}$$

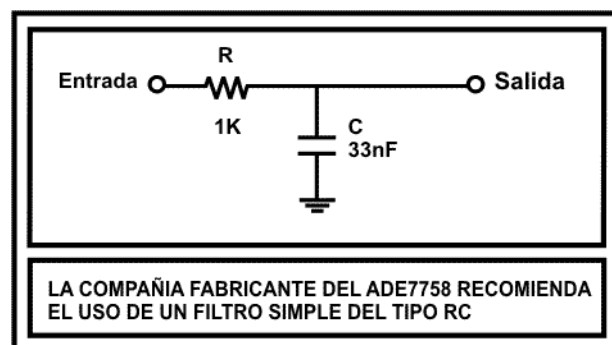


Figura 3.9 – Filtro RC Pasa-bajos

## C) DISEÑO DE LA ETAPA

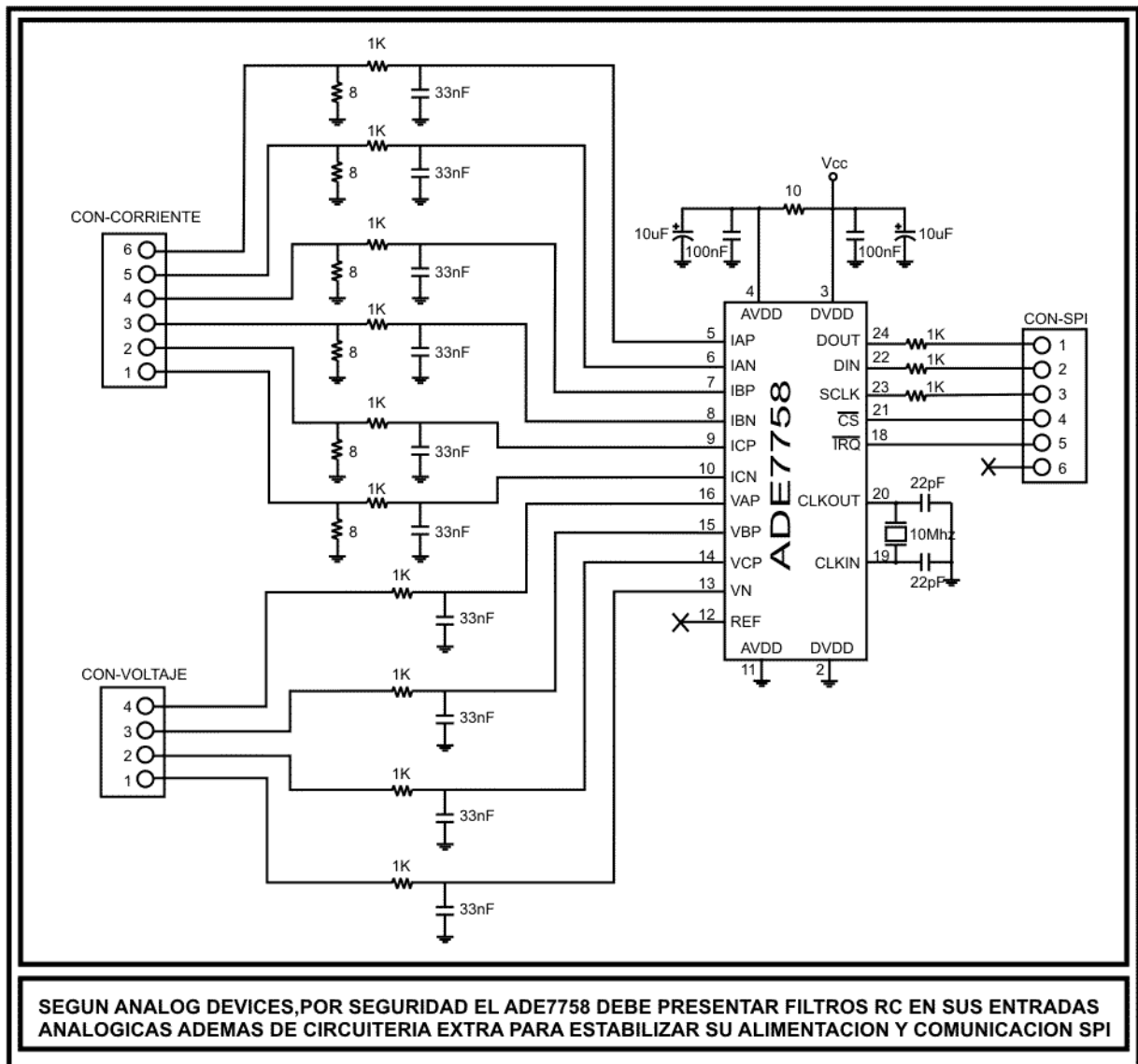


Figura 3.10 – Esquema circuital de la etapa de pre-procesamiento de datos

El elemento básico de ésta etapa es el transductor de parámetros eléctricos, el ADE7758. Para el diseño se investigó acerca de conexiones y topologías de conexión recomendadas por el fabricante en el Anexo F: Hojas técnicas (*AN-559: Application note. Rev. A.- Sección “Design goals”, Pág.2*).

Posee tres entradas de corriente separadas en grupos de a dos: un pin para la entrada positiva y un pin para la salida negativa de la corriente (IAP, IAN, IBP, IBN, ICP, ICN). Para la medición de los voltajes trifásicos el ADE7758 cuenta con tres pines destinados para ello (VAP, VBP, VCP) cuya referencia a negativo es el pin denominado como VN. Además utiliza sus pines DOUT, DIN, SCLK, CS e IRQ para comunicación SPI en modo Esclavo: recepción y envío de datos.

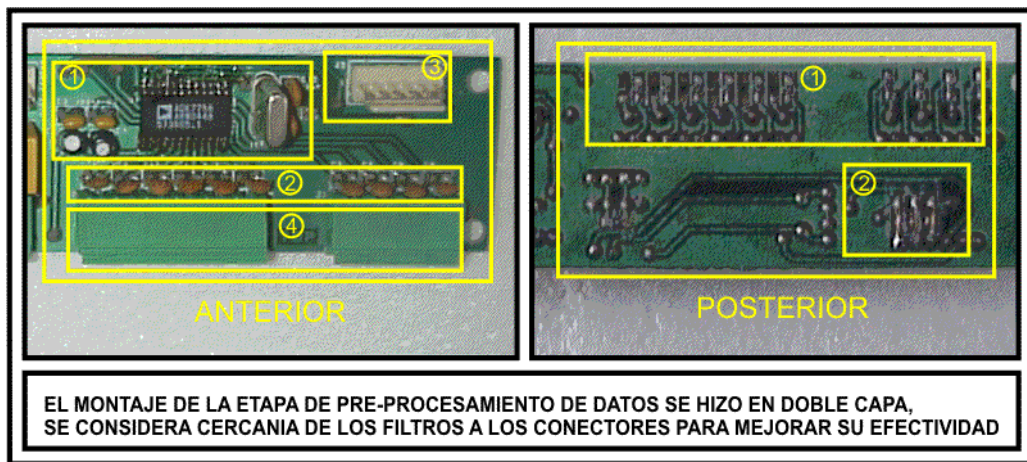


Figura 3.11 – Vista anterior y posterior de la etapa de pre-procesamiento

VISTA ANTERIOR		VISTA POSTERIOR	
①	Pre-procesador	①	Filtro
②	Filtro	②	Conector SPI
③	Conector SPI		
④	Conectores de pre-procesamiento		

### Consideraciones de diseño

La descripción de cada uno de los pines del ADE7758 se encuentra detallada en el Anexo F: Hojas técnicas (*Hoja técnica del ADE7758. Rev. C.- Sección “Pin Configuration and Function Description”, Pág. 9*). Sin embargo, se tomaron en cuenta ciertos aspectos al desarrollar el módulo de procesamiento de datos, los cuales no son descritos en la hoja de datos.

- Los pines 1 (APCF) y 17 (VARCF) son salidas usadas para la calibración de potencia activa y reactiva respectivamente. Para el proyecto se prefiere la calibración mediante registros del software, por lo que se procedió a su deshabilitación.
- Los pines 2 y 11 pertenecen a la misma señal a tierra (GND). No se requiere de un GND independiente para alguna de ellas pues el desacoplo de señales se realiza por los transformadores de voltaje y corriente que acondicionarán la señal de entrada.
- Los pines 3 y 4 se encuentran alimentados bajo la misma señal DC a los cuales se les ha agregado unos filtros para minimizar el ruido de la fuente.
- Todos los pines de alimentación deben tener un condensador de 100nF y 10uF con referencia a tierra que actúen como filtros. El condensador se debe colocar lo más cerca posible a estos dos pines del integrado (alimentación y tierra) para evitar introducir ruido de fuente, motivo por el cual, en la Figura 3.2, el ADE7758 posee los pines de alimentación (DVDD) y tierra digital (DGND) seguidos uno de otro.
- El pin 12 ( $REF_{IN/OUT}$ ) que hace referencia a la señal para conversión ADC, es inhabilitado pues se utilizan las señales de referencia interna de 2.42V. Anexo F: Hojas técnicas (*Hoja técnica del ADE7758. Rev. C.- Sección "Reference circuit", Pág. 27*).
- Los pines de corriente (IAP, IAN, IBP, IBN, ICP, ICN) y voltaje (VAP, VBP, VCP, VN) se dirigen hacia su respectivo conector mediante el filtro RC diseñado.

- Un detalle importante es que para la comunicación SPI los pines DOUT, DIN y SCLK (pines 24, 22 y 23 respectivamente) deben contar con un resistor de  $1K\Omega$  para evitar conflictos con la programación del microcontrolador quien usa los mismos pines SPI para programarse, Anexo F: Hojas técnicas (Hoja técnica del ATmega128. Rev. C. - Sección “Serial Peripheral Interface”, Pág. 162 y Sección “Serial downloading”, Pág. 303).
- Se colocaron dos conectores para voltaje y corriente, que dan ingreso a las señales acondicionadas para el pre-procesamiento, los cuales se conectarán posteriormente en la etapa de acondicionamiento de datos (véase Figura 2.15). Se proyecta que en esta última etapa se diseñará un sistema con desacoplo magnético de tierras y debido a que se trabajará con señales eléctricas que pueden ser perjudiciales al usuario, esta precaución minimizará el riesgo de descargas eléctricas; además asegura la estabilidad del equipo ante fluctuaciones de la red eléctrica.

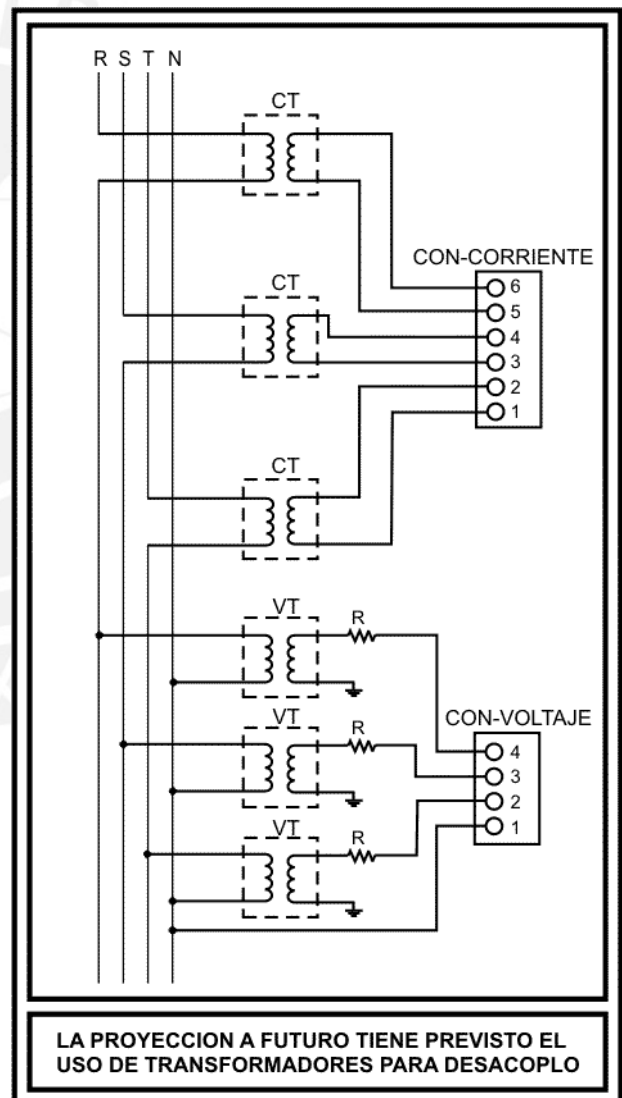


Figura 3.12 – Desacoplo magnético con transformadores

- Para el diseño del software se tomará en consideración los modos de escritura y lectura de registros del pre-procesador, mediante lógica SPI

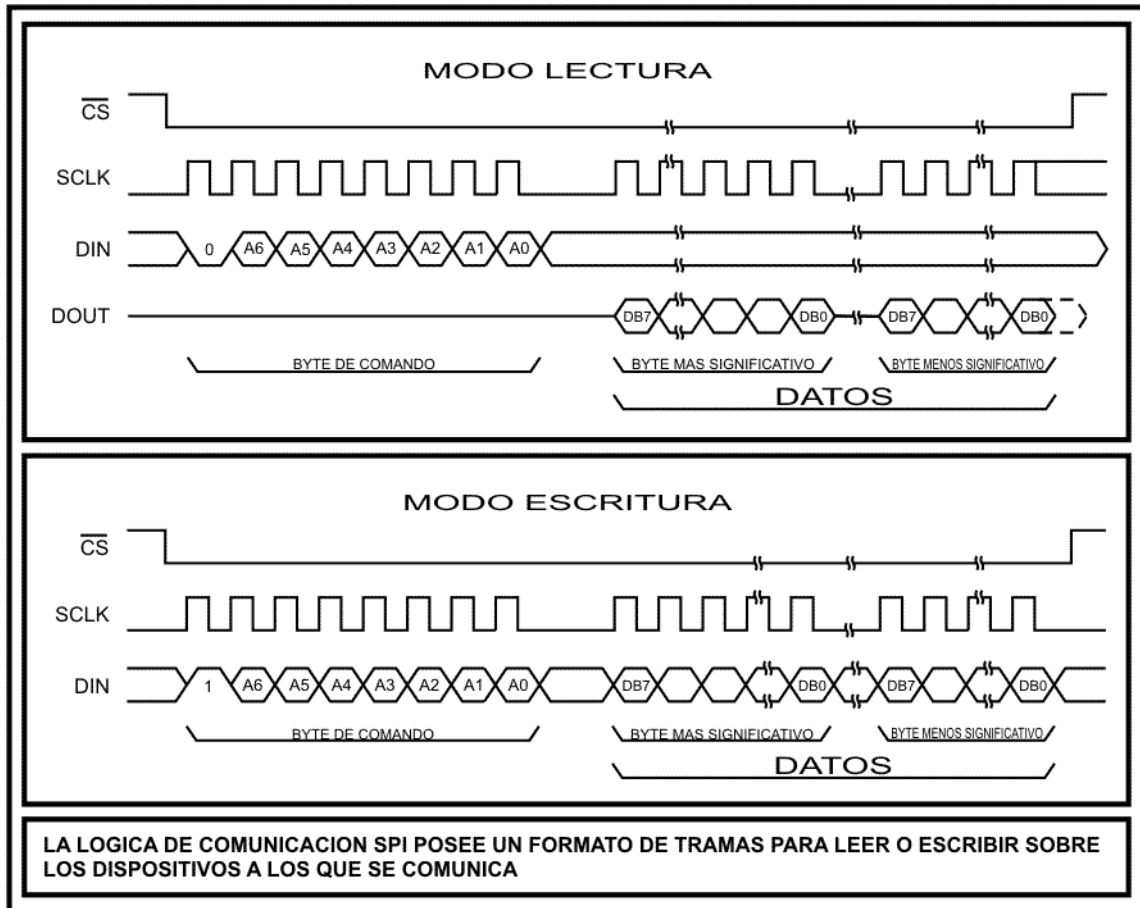


Figura 3.13 – Modo Lectura y Escritura desde el ADE7758 al microcontrolador

En donde, el byte de comando se define como:

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W/R	A6	A5	A4	A3	A2	A1	A0

El valor de DB7 será 1 para escritura (W) y será 0 para lectura (R).

Los valores de A0..6 indican un valor de registro interno del chip de medición. Esto se detalla en el Anexo F: Hojas técnicas (*Hoja técnica del ADE7758. Rev. C.- Sección “Communications register”, Pág. 60*).

### 3.2 ETAPA DE VISUALIZACION DE DATOS

#### A) VISUALIZADOR

##### **Descripción**

Dispositivo que se encarga de mostrar gráficamente los datos enviados por el microcontrolador. El visualizador específico que se utilizará para este desarrollo es del tipo LCD (Pantalla de Cristal Liquido, por sus siglas en inglés “Liquid Cristal Display”).

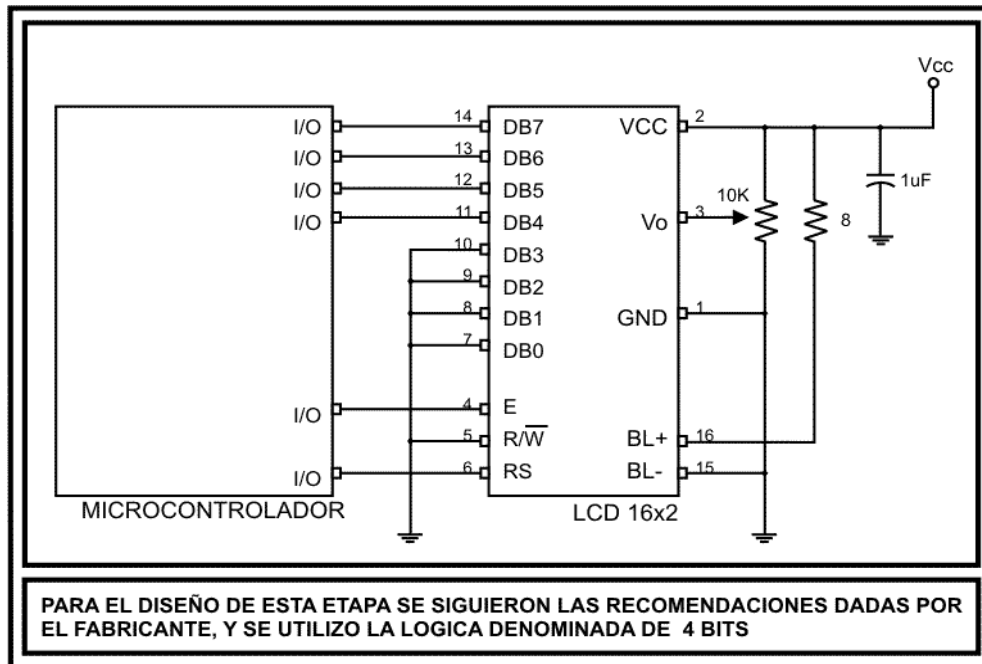
##### **Criterios de selección**

En el proyecto, se requiere visualizar los datos de la señal muestreada en valores discretos. Por ello se plantea el criterio de elegir una pantalla LCD que cumpla con la característica de mostrar valores alpha-numéricos, con capacidad de dígitos no mayor a 20 por línea y con un máximo de 2 líneas para visualización. Su voltaje de operación deberá ser cercano a los 5VDC y de bajo consumo de potencia.

##### **Componente seleccionado**

Se ha elegido una pantalla LCD estándar de 16 caracteres por 2 líneas (LCD 16x2), que posee la característica de programación en paralelo mediante pines del bus de datos, además posee un pin analógico a fin de acondicionar el contraste de la pantalla. Al ser un display de configuración estándar puede ser direccionable por sólo 4 pines de su bus de datos, normalmente se hace con 8 de ellos, esto con el objeto de reducir pines de control para el controlador principal del sistema.

**B) DISEÑO DE LA ETAPA**



**Figura 3.14 – Esquema circuital de la etapa de visualización de datos**

Esta etapa gobernada por el visualizador LCD de 16x2 se maneja con la lógica denominada de 4-bits. Es por ello que el microcontrolador está conectado únicamente a los Bits Más Significativos (MSB) del bus de datos del display (DB7, DB6, DB5 y DB4) y los Bits Menos Significativos (LSB) están conectados a tierra (GND).



**Figura 3.15 – Visualizador LCD de 16x2**

### Consideraciones de diseño

La configuración de los pines del LCD 16x2 es estándar para los fabricantes y se encuentra detallada en su hoja de datos.

- Los pines 4 (E) y 6 (RS) van conectados al microcontrolador, con el primero se habilita el uso del visualizador y con el segundo se indica el modo de acceso a sus registros internos. Estas funciones se dan acorde a la lógica del microcontrolador.
- El pin 5 (R/W) va conectado a tierra para encontrarse siempre en modo ESCRITURA pues no se requerirá leer los registros internos del LCD.
- El pin 3 (Vo) es una entrada analógica que maneja el contraste del LCD, se le conecta a un potenciómetro de 10K el cual podrá hacerlo variar desde 0 a 5V en una escala adecuada.
- Los pines 15 (BL-) y 16 (BL+) son opcionales de los LCDs de 16x2 que controlan iluminación (backlight), han sido considerados en el diseño pero no son limitantes para el correcto funcionamiento del equipo.

### 3.3 ETAPA DE CONTROL Y COMUNICACIÓN

#### A) MÓDULO DE CONTROL Y COMUNICACIÓN

##### Descripción

Un módulo de control, como su nombre lo indica, es un dispositivo encargado del control y manejo de otros dispositivos dentro del sistema. Actúa como un cerebro, debido a que contiene toda la lógica necesaria para el funcionamiento adecuado de las otras partes del sistema. Incluye en su interior las tres funcionalidades de un computador: Microprocesador, memoria y unidades de Entrada/Salida.

La característica básica de estos sistemas es su capacidad de re-configuración, pues sin alterar de modo alguno su entorno electrónico, sólo mediante programación, puede realizar funciones muy diferentes a las iniciales.

##### Tarjeta TEMPUS VI

Como se definió en el Capítulo 2, para el desarrollo del proyecto de tesis se hace uso de la tarjeta de control TEMPUS VI. Cuyos datos técnicos:

- Nombre: TEMPUS VI – Rev. 2.1 (P/N: 030006)
- Microcontrolador ATmega128 – empaquetado TQFP
- Voltaje de alimentación
  - 12 ~ 20 VDC regulado
  - Conector RJ11 para alimentación externa

- Capacidad de programación in-situ - ISP
  - Conector IDC de 3x2 para programación
  - En la hoja de datos del microcontrolador ATmega128, ATMEL provee información del software y hardware necesario para programación.  
(Sección “Serial downloading”, Pág. 303).
  
- Interfaz de comunicación
  - 2 conectores molex con comunicación RS-232C
  - 1 conector RJ-45 con comunicación TCP/IP
  - 1 conector con comunicación SPI
  
- Recursos de la tarjeta
  - Buzzer
  - Pila de Litio
  - Reloj en tiempo real (RTC: Real Time Clock)
  - Memoria flash externa de 1MB
  
- Conector IDC de 2x20 para:
  - LCD de 16x2
  - Teclado matricial de 4x4
  - 4 LEDs de control
  
- Reloj del sistema: Cristal de 16Mhz
  
- Consumo máximo de corriente : 100 mA
  
- Temperatura de trabajo: -5 ~ 70 °C

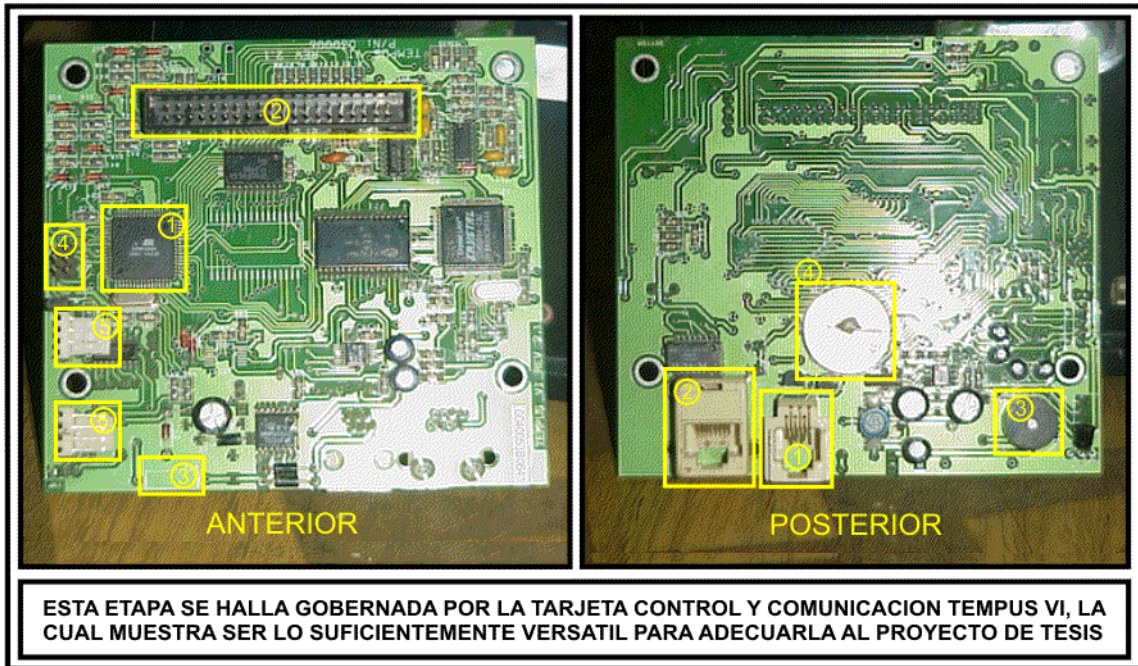


Figura 3.16 – Vista anterior y posterior del módulo de control

VISTA ANTERIOR		VISTA POSTERIOR	
①	Microcontrolador ATmega128 (TQFP)	①	Conector de alimentación
②	Conector IDC 2x20	②	Conector TCP/IP
③	Conector SPI	③	Buzzer
④	Conector SPI	④	Pila de litio
⑤	Conector Serial 1		
⑥	Conector Serial 2		

El TEMPUS VI posee como corazón un microcontrolador de la familia AVR de ATMEL, el ATmega128 en empaquetado TQFP:

- Frecuencia : 1~16 MHz
- Pines I/O máximo : 53 pines
- Canales PWM : 1~8 canales
- Canales ADC : 8 canales de 10 bits
- Temporizadores : 2 temporizadores de 16-bits

- Memoria Flash : 128 Kbytes
- Memoria SRAM : 4 096 bytes
- Memoria EEPROM : 4 Kbytes

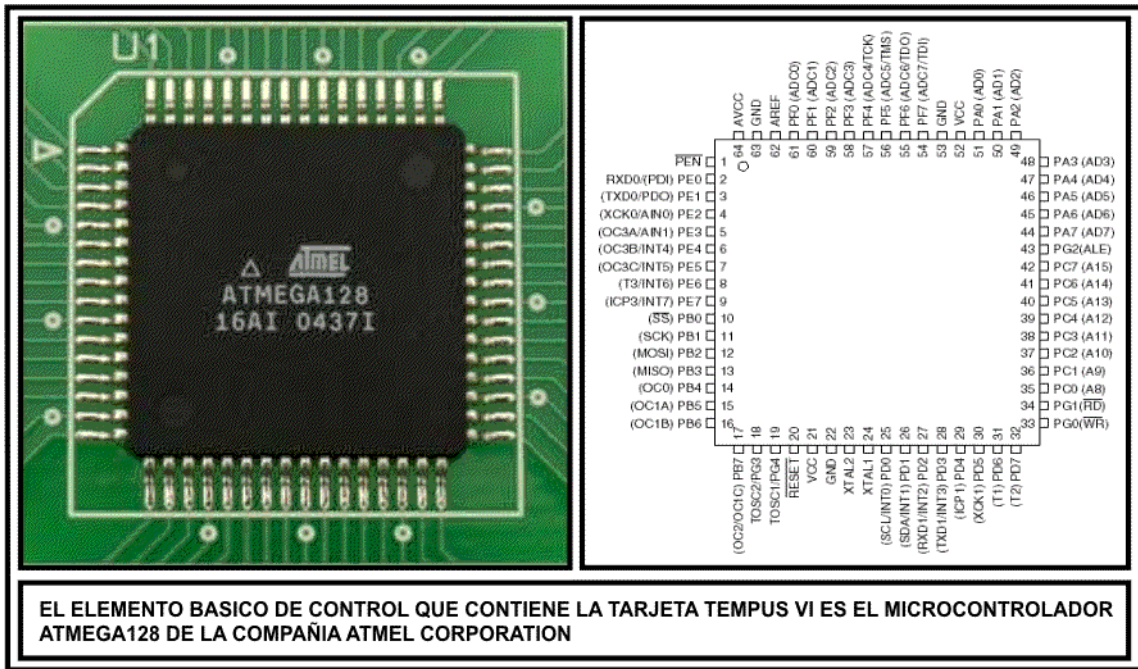


Figura 3.17 – Microcontrolador ATmega128 - Empaquetado TQFP64

Dentro de sus consideraciones de software, la tarjeta TEMPUS VI cuenta con:

- Lógica de control del hardware para TCP/IP y formación de datagramas en la comunicación a red.
- Lógica de manejo de pines digitales de Entrada/Salida, conversores análogos-digitales (ADC), temporizadores internos, UARTs, buses de comunicación, Reloj en Tiempo Real (TRC) y específicamente control de la lógica SPI para comunicación con el pre-procesador, pantalla LCD para visualización, Teclado matricial de 4x4 para ingreso de datos, actuadores, comunicación serial por bus.

- Opciones de control para el usuario, configuraciones a nivel programador, uso de niveles de seguridad, textos a visualizar en el LCD, control para los actuadores, entre otras funcionalidades.

Respecto al diseño, los pines que serán necesarios del microcontrolador:

- Teclado 4x4 (ingreso de datos) : 8 E/S
- LCD (Visualizador) : 6 E/S
- Indicadores luminosos : 4 E/S (con temporizador opcional)
- Comunicación SPI : 4 (MISO, MOSI, SCK, SS)
- Interrupción : 1 Interrupción externa (IRQ)
- Comunicación serial (RS-485) : 3 (TX, RX y E/S)
- Manejo de actuadores : 2 Open Collector (Relé 1 y 2)
- Comunicación TCP/IP : Conector RJ-45 (8 pines)

## B) LÓGICA DE CONTROL

### Descripción

En el proyecto de tesis se ha considerado la programación, por ser un punto importante para el desarrollo del mismo, esta lógica control se basa en un lenguaje de programación de bajo nivel, también denominado código assembler. Por características del software programador y por su dominio, se trabajó con el programa que provee el fabricante del microcontrolador: AVRstudio.

### Consideraciones de diseño

- Como la tarjeta TEMPUS VI ya posee un firmware incorporado, para agregar la nueva lógica de control se tuvo un periodo de estudio para conocer sus funciones y a partir de ello acondicionar el firmware diseñado.
- La lógica de control diseñada incorpora las funcionalidades de lectura por SPI del ADE7758 y el uso de datagramas TCP/IP para la comunicación a red. Además de hacer uso de las opciones de configuración para datagramas, reloj en tiempo real, manejo de teclado y LCD, entre otras funciones ya provistas por el TEMPUS VI.
- El firmware se desarrolló en código assembler con el programa AVRstudio 4 provisto por la compañía ATMEL. El AVRstudio es de descarga y licencia libre, utilizado para el diseño y programación de los microcontroladores AVR.

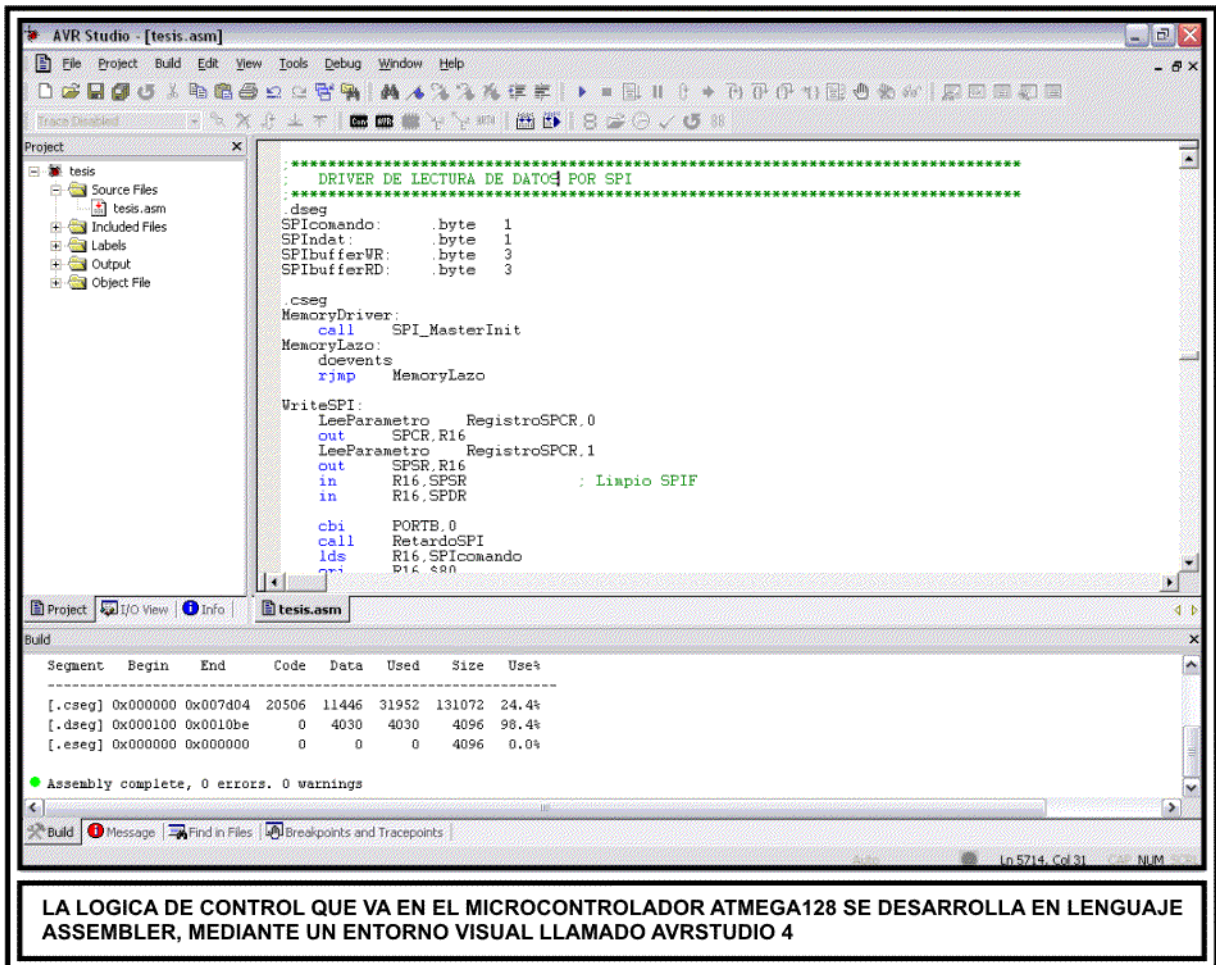


Figura 3.18 – Desarrolló del software en la plataforma AVRstudio

- El diagrama de flujo de la Figura 3.19 es referencial, pues el módulo de control Tempos VI trabaja bajo un sistema denominado multitarea, lo cual asegura que no correrá en una sola función durante en un bucle infinito y secuencial, sino que ejecutará diversas funciones de modo simultáneo.

Diseño del software

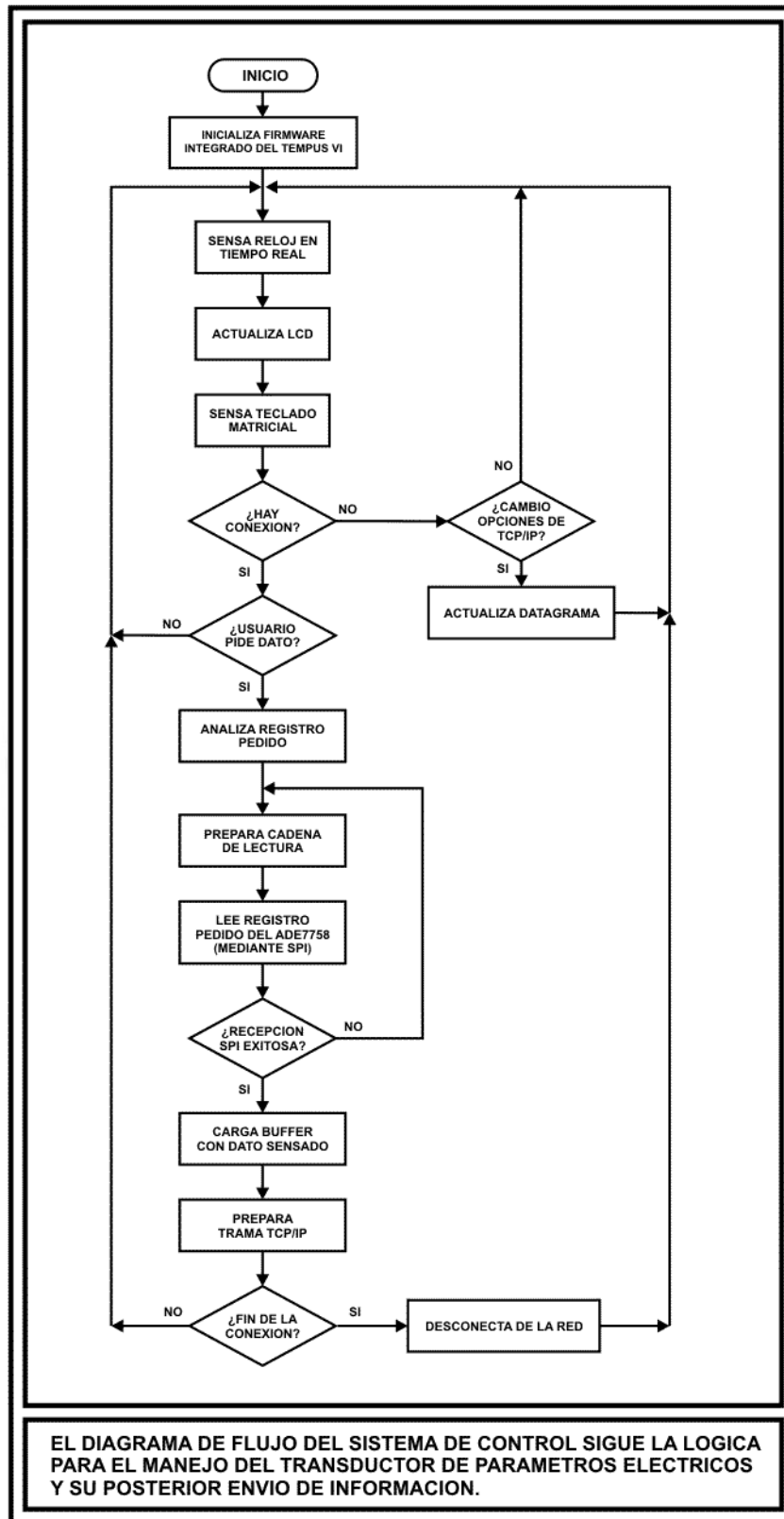


Figura 3.19 – Diagrama de flujo del software

### 3.4 ETAPA DE INGRESO DE DATOS

Esta etapa consta básicamente de un teclado matricial de 4x4, el cual será el encargado de recibir las acciones del usuario y enviarlas al microcontrolador para su procesamiento.

#### A) DISEÑO DE LA ETAPA

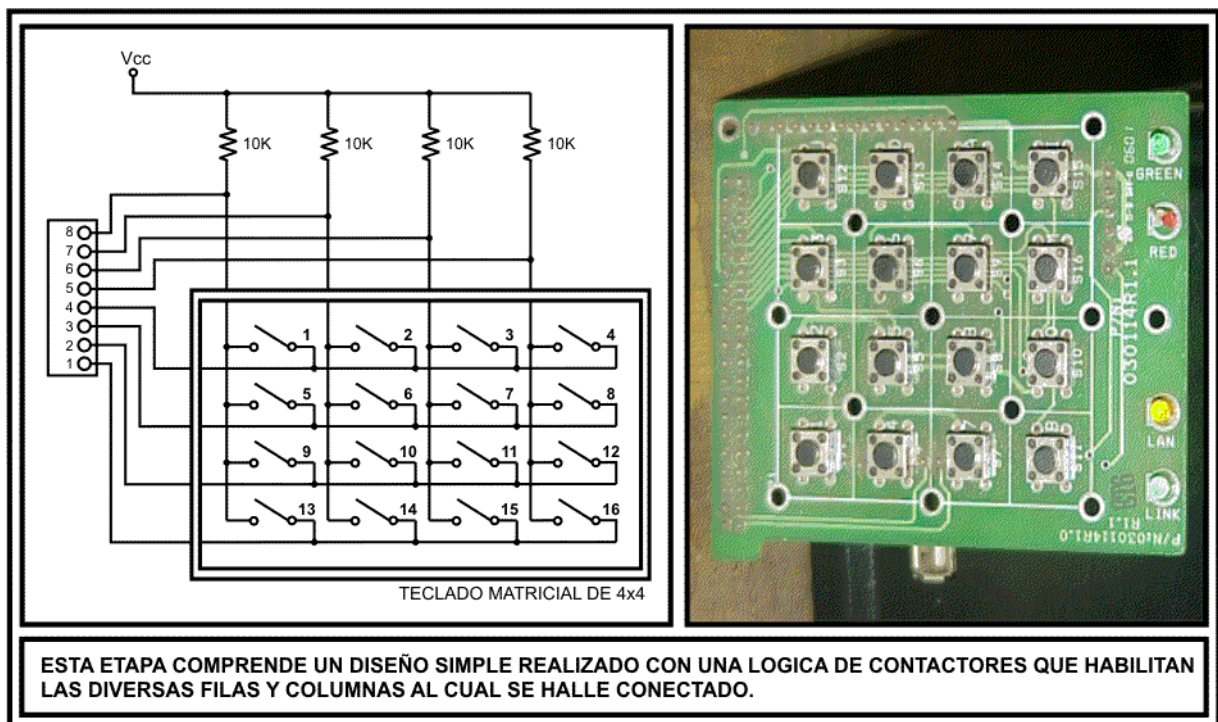


Figura 3.20 – Esquema circuital de la etapa de ingreso de datos

Para esta parte no se requiere una gran descripción, como se puede observar en la Figura 3.20 se ha hecho uso de una etapa de ingreso de datos la cual está básicamente conformada por un teclado de 4x4 que dará al usuario las teclas necesarias para la configuración del sistema.

### **3.5 ETAPA DE EXPANSIÓN**

A nivel de ingeniería los cambios se presentan de manera constante e inesperada, por ello los proyectos deben de estar en capacidad de adaptarse rápidamente y sin inconvenientes, la etapa de expansión de este proyecto de tesis tiene como objeto permitir que el prototipo pueda ser adaptado a otros dispositivos o sistemas mayores.

Se ha implementado la lógica de comunicación por bus diferencial denominado RS-485, esta lógica permitirá comunicar otros dispositivos que se ubiquen a grandes distancias. Adicionalmente se ha desarrollado una etapa de actuadores externos, de este modo busca aplicar la característica de manejo de actuadores externos, o control de acceso, que presenta el módulo TEMPUS VI.

#### **A) COMUNICACIÓN SERIAL RS-485**

##### **Descripción**

Frecuentemente los microcontroladores cuentan con buses y puertos de comunicación serial, los cuales son usados por los módulos como puertos de comunicación con protocolo estándar.

##### **Criterios de selección**

En el caso de este proyecto, se plantea hacer uso de un protocolo de comunicación por bus serial que permita transmitir datos a grandes distancias, superiores a los 15m, y que sea, en lo posible, insensible ante el ruido de campos electromagnéticos externos generados por algún equipo, como un transformador o generador, en donde se halle cercano el sistema.

Además, el dispositivo deberá contar con la capacidad de modelar los voltajes diferenciales adecuados, para la comunicación exitosa, a partir de valores digitales entregados por los pines de comunicación serial del microcontrolador principal.

### Componente seleccionado

El dispositivo seleccionado fue el Bus Diferencial de Transmisión SN75176 de la compañía Texas Instruments, el cual contiene la lógica de comunicación RS-485 de transmisión serial diferencial, la cual permite comunicación a distancias de hasta 1000m, además de ser inmunes al ruido electromagnético externo. La elección en cuanto a costos se dio porque éste dispositivo es uno de los más económico en el mercado, y en cuanto a funcionalidades electrónicas resaltan sus características de convertir datos digitales del UART en valores para RS-485 y viceversa.

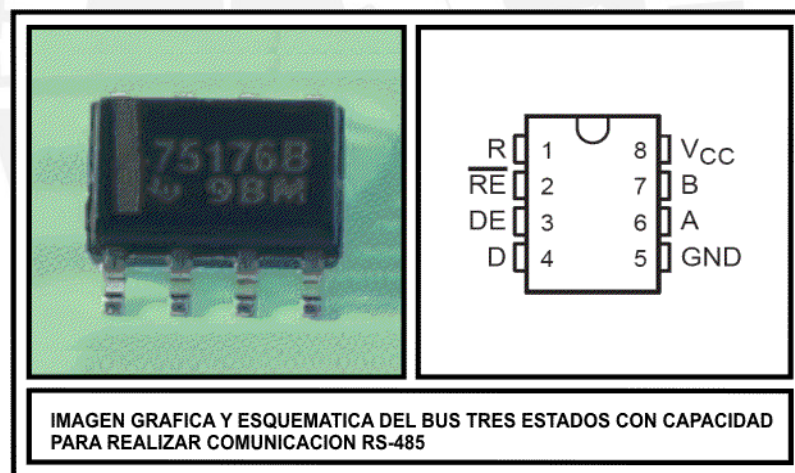


Figura 3.21 – Bus diferencial de datos SN75176

Las características del dispositivo son:

Transmisión bidireccional, Driver tres estados de recepción, capacidad de salida por bus de datos de  $\pm 60$  mA Máx., protección termal ante aparición de sobrevoltaje cumple con requerimientos del estándar ANSI EIA/TIA-422 y las recomendaciones V.11 de la ITU. Anexo F: Hojas técnicas (*Hoja técnica del SN75176, Sección "Description". Pág. 1*).

- Impedancia de entrada del receptor : 12KΩ min.
- Sensitividad de entrada del receptor : ±200 mV
- Histéresis de entrada del receptor : 50 mV Typ
- Voltaje de operación : 5VDC ± 10%
- Bajos requerimientos de potencia

Para la lógica de comunicación para envío y recepción de datos el SN75176 sigue:

EMISOR				RECEPTOR		
ENTRADA (D)	HABILITADOR (DE)	SALIDAS		ENTRADAS DIFERENCIALES A-B	HABILITADOR (RE)	SALIDA (R)
		A	B			
H	H	H	L	$V_{ID} \geq 0.2 V$	L	H
L	H	L	H	$-0.2 V < V_{ID} < 0.2 V$	L	?
X	L	Z	Z	$V_{ID} \leq -0.2 V$	L	L
				X	H	Z
				Abierto	L	?

Donde:  
 H = Nivel Alto  
 L = Nivel Bajo  
 ? = Indeterminado  
 X = Irrelevante  
 Z = Alta impedancia

Tabla 3.1 – Lógica de funcionamiento del SN75176

### Diseño electrónico

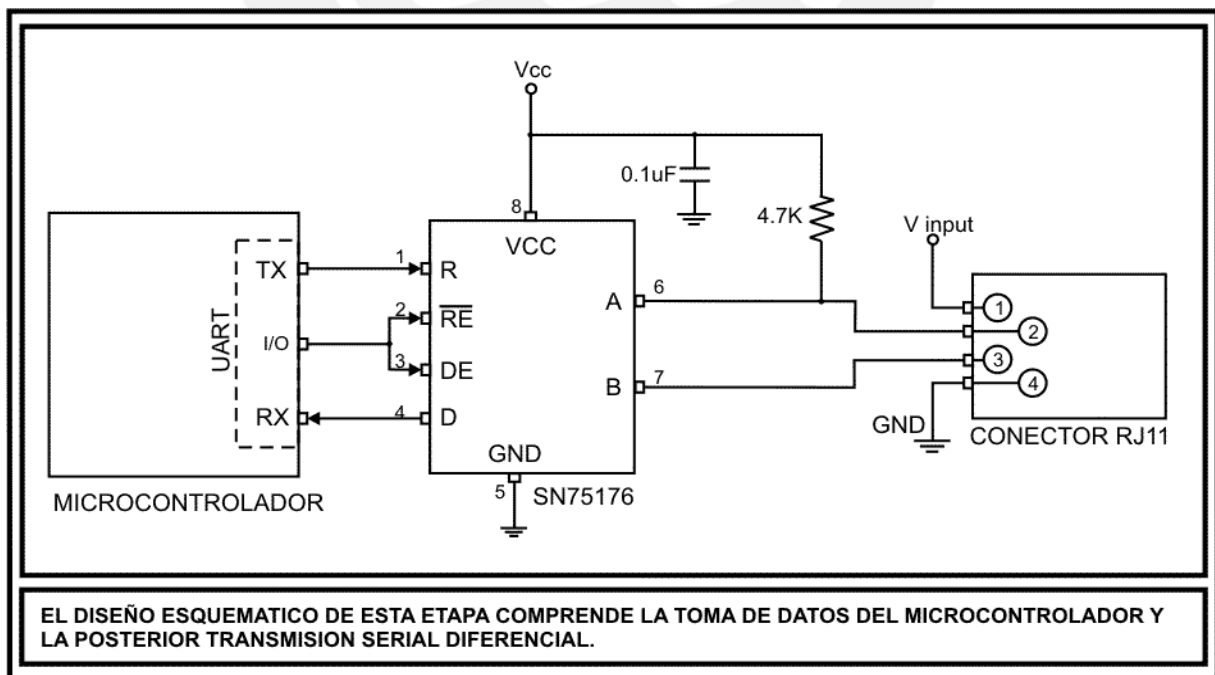


Figura 3.22 – Esquema circuital de la comunicación RS-485 (etapa de expansión)

Esta comunicación se encuentra básicamente realizada por el bus diferencial SN75176, el cual está gobernado por el microcontrolador que envía la data mediante sus pines de comunicación (TX y RX) del puerto UART y que a la vez maneja un pin I/O para diferenciar entre el envío y recepción de datos, según especificación de las tablas presentadas para la lógica de comunicación.

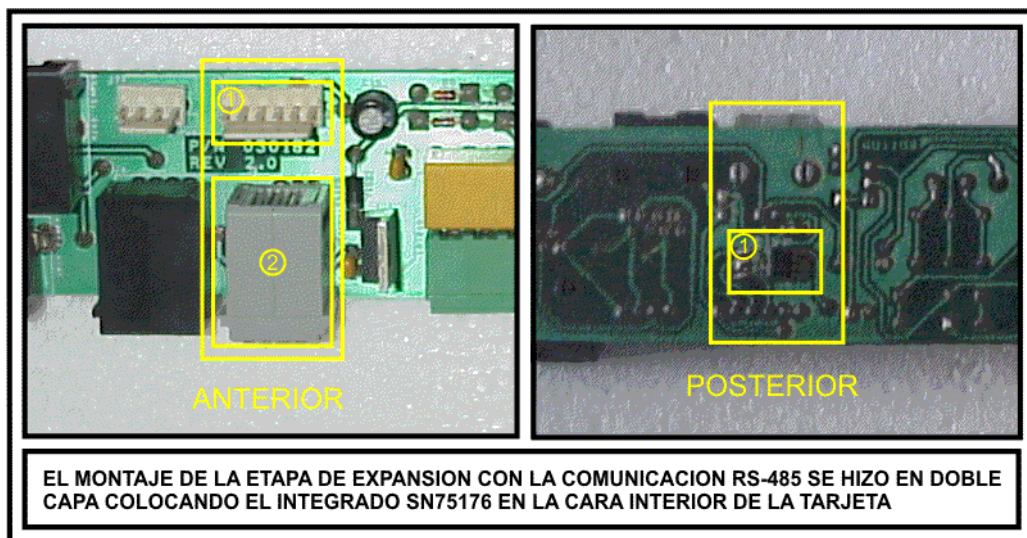


Figura 3.23 – Vista anterior y posterior de la comunicación RS-485

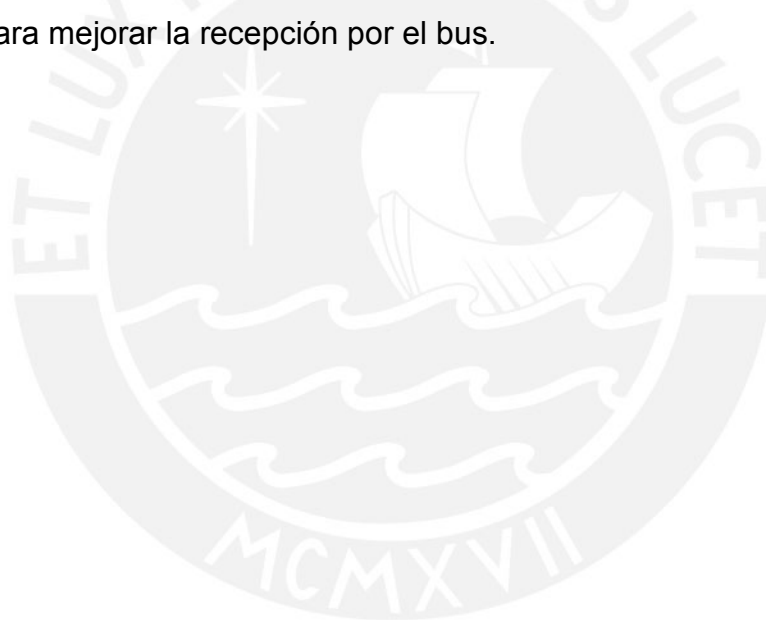
VISTA ANTERIOR		VISTA POSTERIOR	
①	Conector serial (UART)	①	Bus diferencial de datos - SN75176
②	Conector de comunicación RS-485		

### Consideraciones de diseño

- Los pines 2 (RE) y 3 (DE) están cortocircuitados pues su funcionamiento es contrario el uno con el otro, por la negación del pin 2. Cuando el microcontrolador envía un 1-lógico por su pin I/O, el SN75176 se encuentra en modo emisor transfiriendo toda data que le llega por el pin 1 (R) hacia sus pines

diferenciales (A y B); y cuando el microcontrolador envía un 0-lógico por el I/O, el SN75176 se encuentra en modo recepción transfiriendo toda la información que llega a sus pines diferenciales hacia el pin 4 (D). Véase las tablas lógicas presentadas del bus diferencial.

- Al estar diseñado físicamente para la conversión UART – 485 el SN75176 se puede conectar directamente a los pines de comunicación digital con el microcontrolador y a la salida del bus diferencial sin necesidad de contar con elementos resistivos o filtros de acoplo. A excepción del pin 6 (A) que posee un filtro para mejorar la recepción por el bus.



## B) ACTUADORES

### Descripción

Los actuadores serán elementos o conjuntos de elementos cuya función será realizar una función específica a partir de un comando recibido, esto puede ser: abrir o cerrar puertas, activar o desactivar alarmas, encender o apagar luminarias, entre otros.

### Criterios de selección

Al diseñarse un módulo que recibe voltajes DC que pueden ser 5 o 12 voltios, se hace lógico el uso de un componente que pueda trabajar con dichos voltajes de trabajo. Con el fin del control de acceso, el componente deberá manejar dos estados (encendido/apagado), soportar el paso de voltajes AC sobre sus pines de contacto y niveles de amperaje máximos de 1A.

### Componente seleccionado

De los criterios de selección, el tipo de componente adecuado para el proyecto es el actuador de contacto, también conocido como Relé. Este es un dispositivo electromecánico, que funciona como un interruptor controlado por un circuito eléctrico el que, por medio de un electroimán, acciona uno o varios contactos que permiten abrir o cerrar otros circuitos eléctricos independientes.

Luego de hacer un análisis en el mercado peruano, revisando precios y disponibilidad, el componente seleccionado fue el relé HK19F de la compañía HUI KE, que cumple con lo requerido pues trabaja con valores de 5VDC y consume aproximadamente 200mA de corriente, además maneja dos estados:

- Normalmente Abiertos (NO, por sus siglas en inglés),
- Normalmente Cerrados (NC)

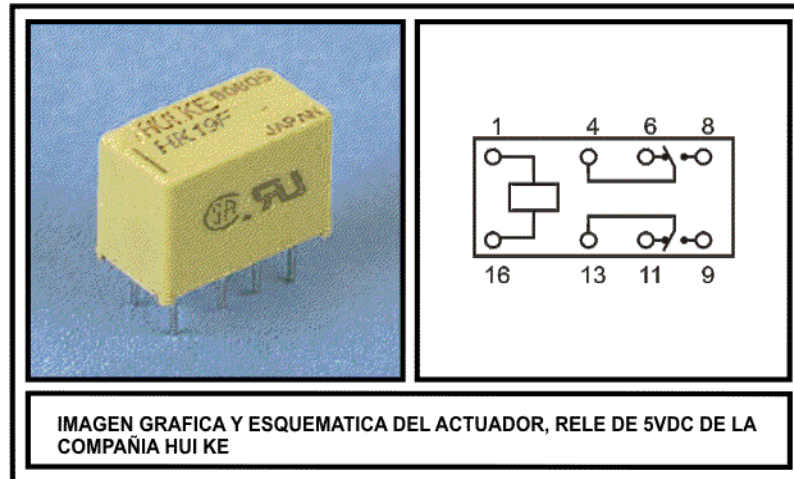


Figura 3.24 – Relé HK19F de 5VDC

Las características de este relé de baja potencia son:

- Tensión de bobina : 5VDC regulado
- Corriente de conmutación : 1A max (120VAC / 30VDC)
- Consumo promedio de corriente : 200mA
- Dimensiones : L 20.2 x A 10 x H12.5 mm

### Diseño electrónico

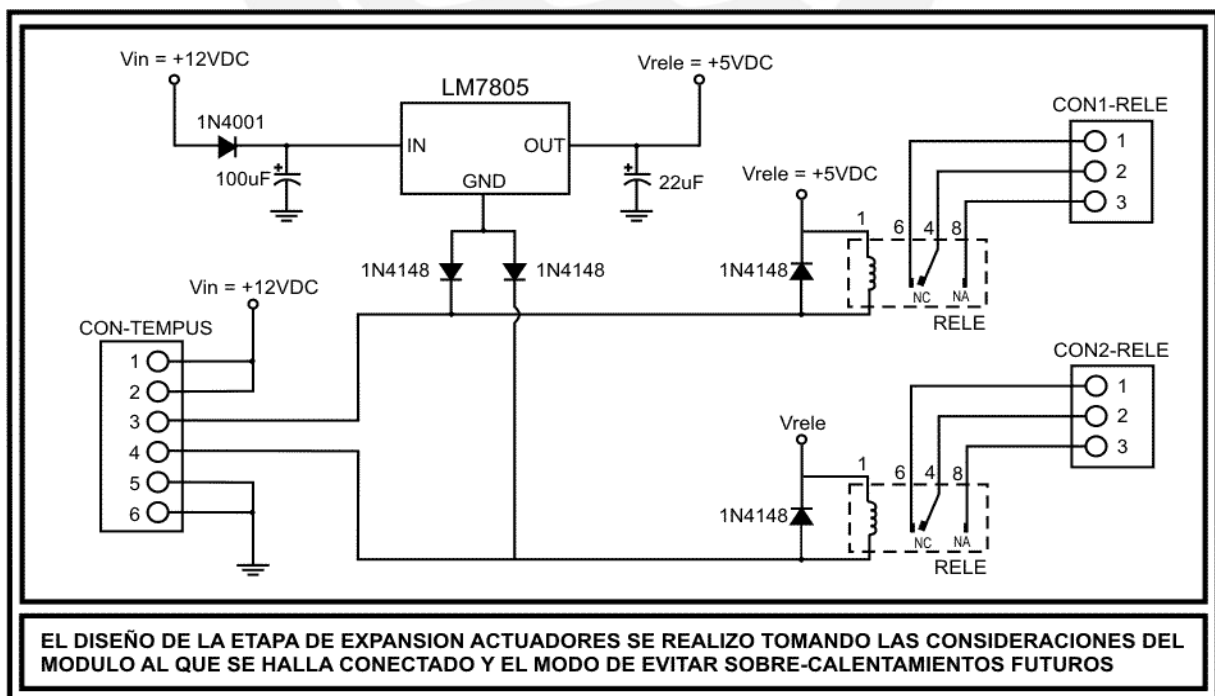


Figura 3.25 – Esquema circuital de los actuadores (Etapa de expansión)

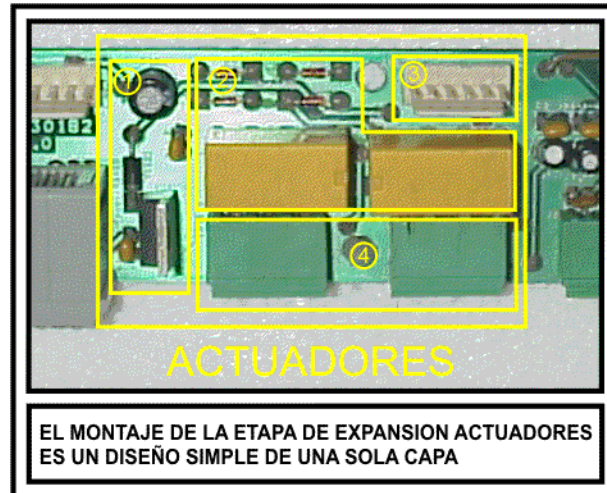


Figura 3.26 – Actuadores en la tarjeta de componentes

ACTUADORES	
① Regulador LM7805	③ Conector del TEMPUSVI
② Relés 5VDC	④ Conector de actuadores

### Consideraciones de diseño

- Esta etapa de expansión presentó un primer inconveniente de diseño pues el relé al ser un dispositivo que consume mucha corriente en un largo periodo, tanto como dure su funcionamiento, no se podía alimentar directamente con la fuente de los módulos digitales pues se corría el riesgo que la fuente se dañe por sobre exigencia. Entonces se diseñó una fuente de alimentación basada en el LM7805 con una consideración adicional, la cual responde a la mejora del tiempo de vida del regulador y los componentes cercanos que pueden ser afectados por sobrecalentamiento. Teóricamente un relé consume corriente sólo en uno de sus estados, sin embargo en la práctica el relé llega a consumir corriente en cualquiera de sus dos estados, siendo siempre un estado de mayor

consumo que el otro. Para limitar el funcionamiento y posterior calentamiento del regulador LM7805 se colocó un juego de diodos que conectan a tierra con la señal del microcontrolador y que lo deja trabajar sólo en el momento que el microcontrolador necesite que los relés cambien a estado activo.

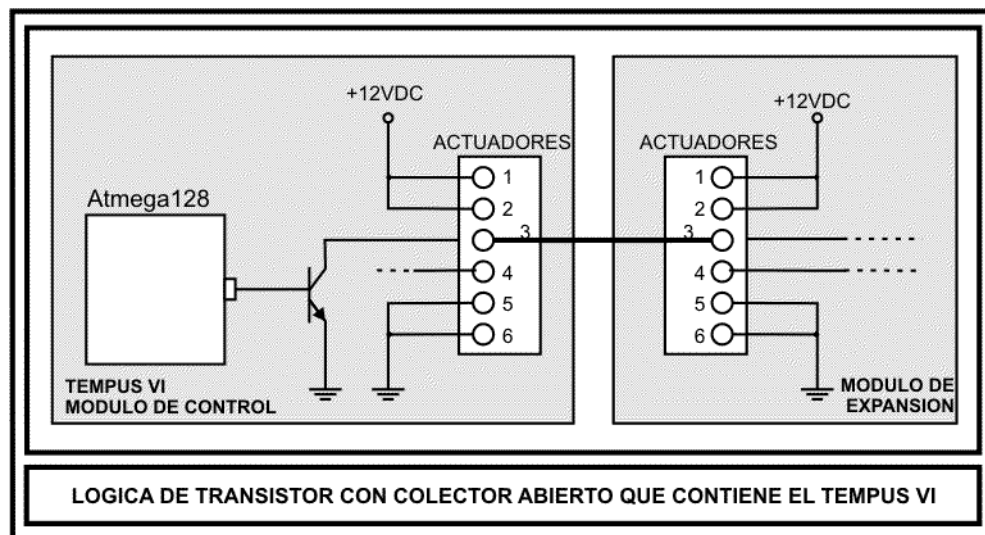


Figura 3.27 – Transistor en modo Colector abierto

- Como se observa en la Figura 3.27, los pines que envían la señal desde el microcontrolador, en el módulo TEMPUS VI, constan de un transistor en modo Colector Abierto el cual se satura cuando recibe un 1 lógico del microcontrolador y llega al corte cuando recibe un 0 lógico, dando de ese modo el paso de la energía que se necesita para activar al relé al que se halle conectado.
- En el relé, los pines 1-16, 4-13, 6-11 y 8-9 fueron cortocircuitados pues si bien se conoce que cada relé de los elegidos posee 2 contactores, se prefirió utilizarlos como uno solo pues se busca la mejor precisión de contacto a través de un largo periodo de funcionamiento del equipo. Véase Anexo E: Diseño del sistema (Sección "Diseño del sistema". Pág. 16).

### 3.6 CONECTORES

Esta sección contiene una breve descripción de los conectores elegidos para el desarrollo del proyecto, que si bien no cumplen un rol determinante dentro del funcionamiento del equipo su elección es importante porque brinda funcionalidad al diseño. Los conectores que se presentan en el Anexo A: Conectores (*Sección “Conectores”. Pág. 1*) se eligieron siguiendo los requerimientos de voltaje y corriente a los que será sometido el equipo, su disponibilidad en el mercado peruano, comodidad de uso para el usuario, además de brindar orden al diseño.

#### Aplicación

Para la implementación de conectores, se dividió la tarjeta de componentes en dos caras: Conectores externos, como se observa en la Figura 3.28 tiene los conectores que brindan comunicación con el usuario; Conectores internos, como se observa en la Figura 3.29 que tiene comunicación con los otros módulos del sistema.

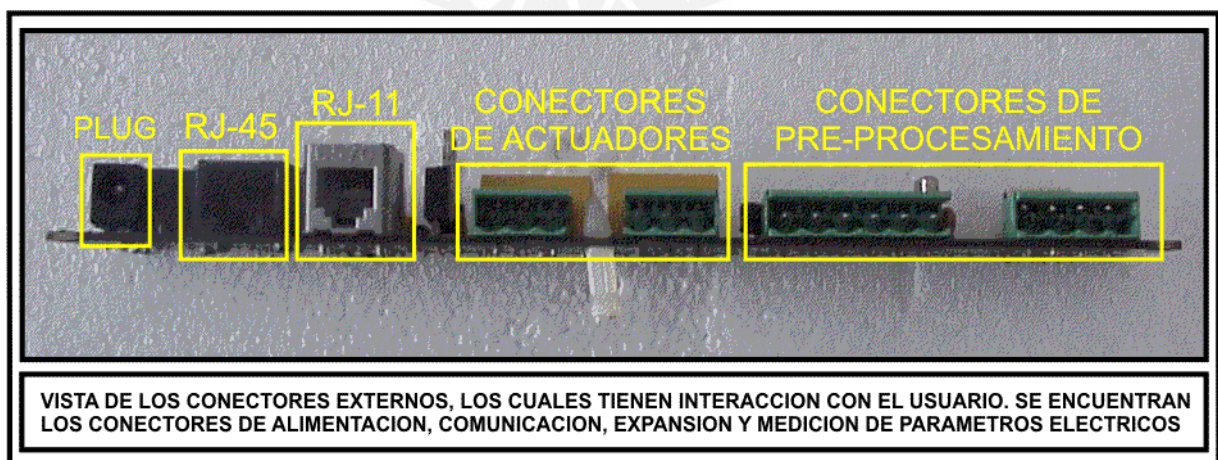


Figura 3.28 – Vista y descripción de los conectores externos

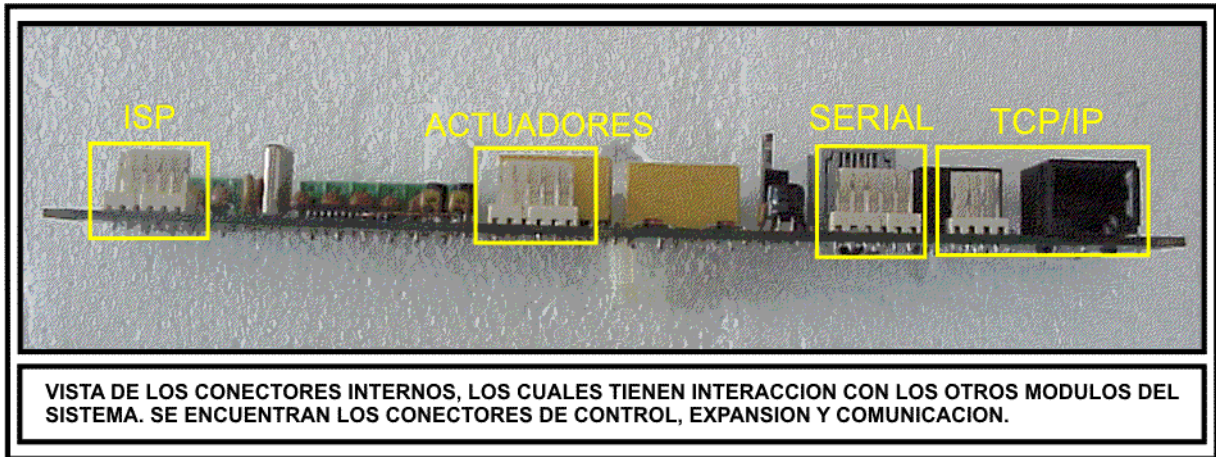


Figura 3.29 – Vista y descripción de los conectores internos

### Consideraciones de diseño para los conectores externos

- El plug de alimentación fue elegido por ser el más adecuado para recibir una señal de 12VDC regulados y por considerársele un estándar dentro de la industria comercial.
- El conector RJ-45 se utilizó por ser el conector estándar para la comunicación TCP/IP. Además de cumplir con las configuraciones recomendadas por la norma del protocolo.

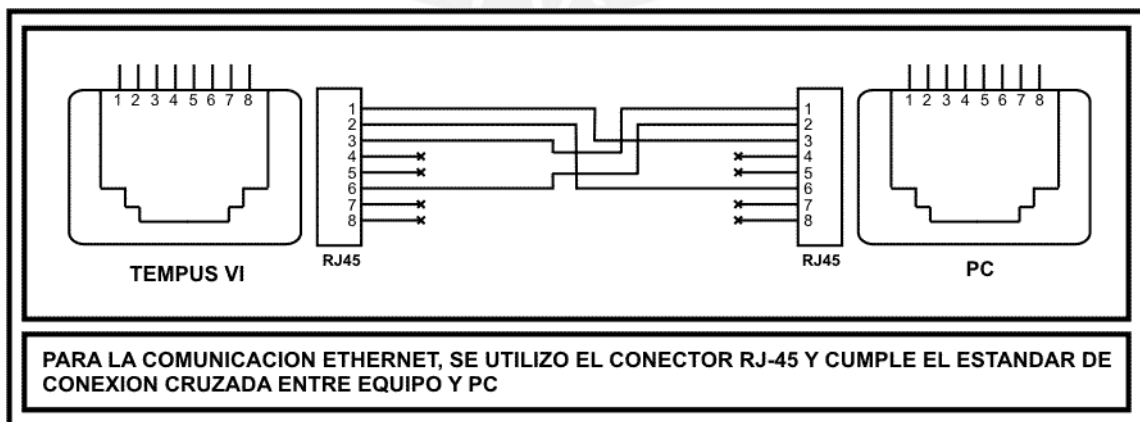


Figura 3.30 – Conexión a red: EQUIPO – PC



Figura 3.31 – Conexión a red: EQUIPO – HUB

- Como se mencionó en la Sección “Etapa de expansión”. Pág. 64), el sistema alimentará un equipo esclavo y se comunicará protocolo RS-485. Para cumplir con dichos requisitos se eligió el conector RJ-11 por su cómodo manejo y facilidad de ensamblaje del conector aéreo.

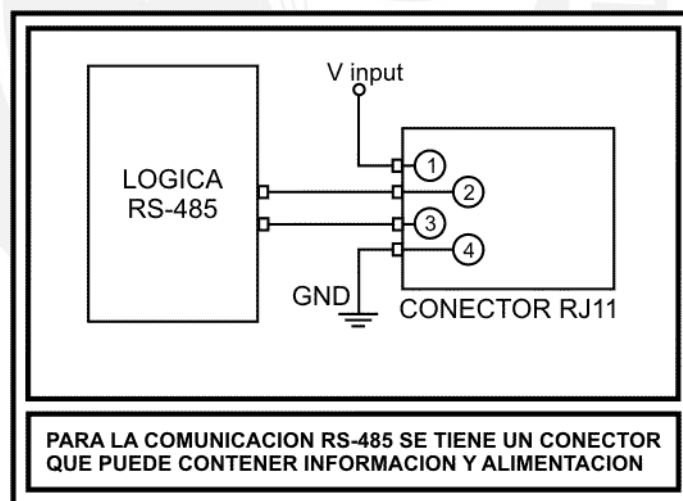


Figura 3.32 – Conector RJ-11 externo

Se observa que el conector RJ-11 posee los pines de comunicación serial diferencial RS-485 además de un par de pines de denominados  $V_{input}$  y GND que serán la alimentación para el equipo a expandir.

- Se eligieron los Bloques terminales para los conectores de pre-procesamiento y de actuadores pues constan de dos partes acoplables entre si (una para la base de la tarjeta de componentes y una aérea) esto otorga comodidad para la interconexión de las etapas además de cumplir con requerimientos eléctricos del sistema.

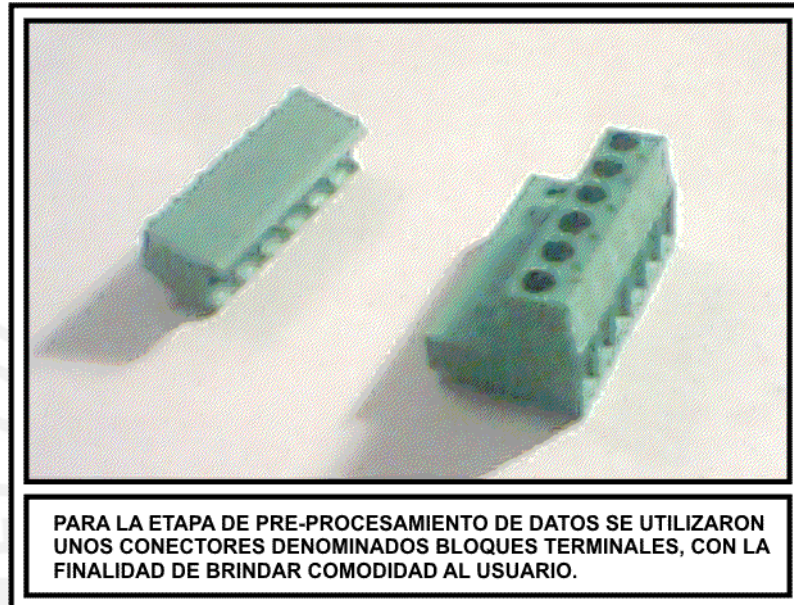


Figura 3.33 – Bloque Terminal aéreo y base

### Consideraciones de diseño para los conectores internos

Los conectores internos del módulo del sistema permiten comunicar las etapas de pre-procesamiento de datos, expansión y conectores externos con el módulo de control. En la Figura 3.34 se puede observar los conectores de los módulo de control y del sistema que se interconectan entre si.

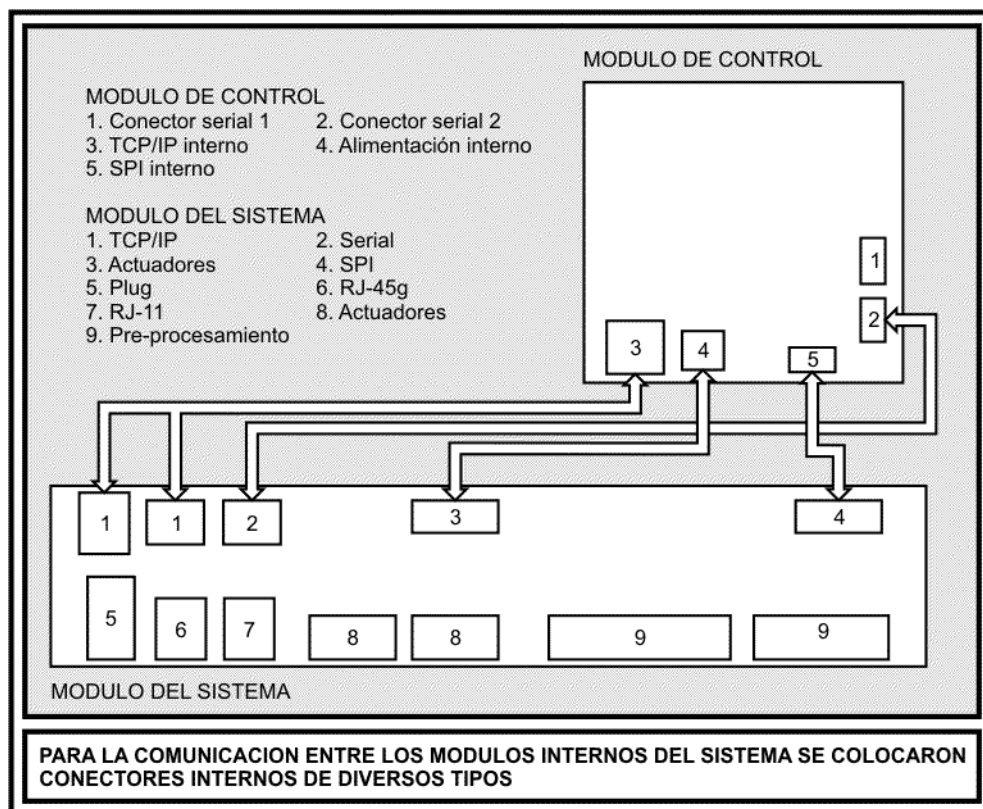


Figura 3.34 – Distribución de los conectores internos

- El conector SPI es un molex de 6 pines que se encarga de recibir la señal SPI desde la tarjeta TEMPUS VI para distribuirla hacia el pre-procesador ADE7758. Nótese que de los 6 pines sólo se da uso a 5 de ellos, no se eligió usar un molex de 5 pines por su escasa disponibilidad en el mercado peruano y como se necesitaban características comerciales, un molex de 6 pines resultó más viable que uno de 5 pines.

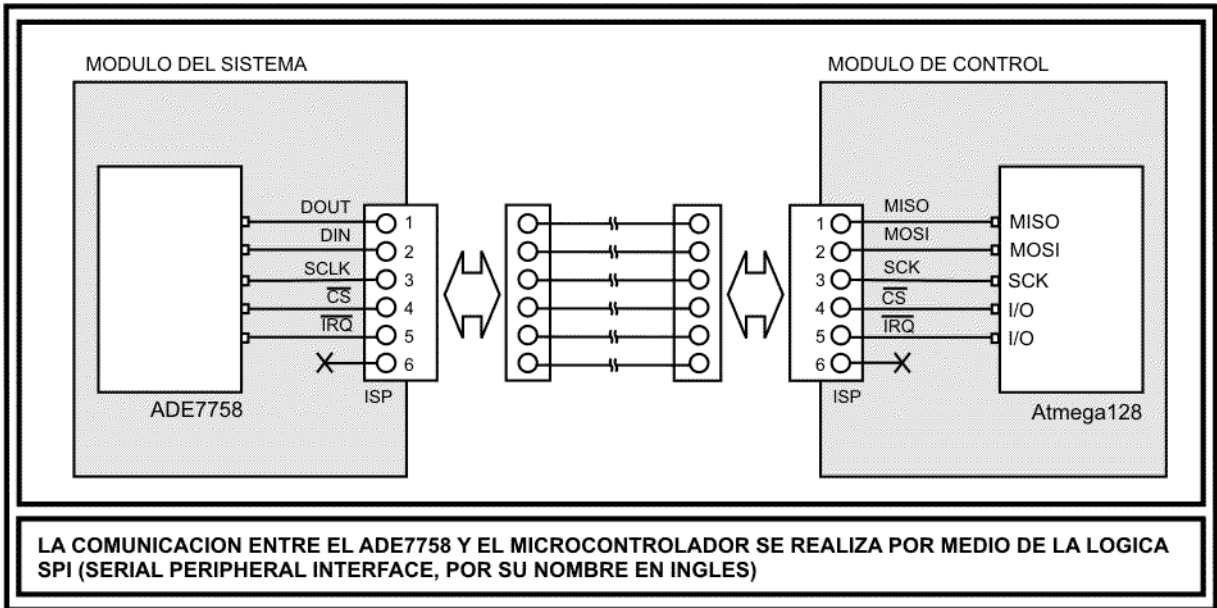


Figura 3.35 – Conector SPI interno

- El conector denominado ACTUADORES es un molex que cumple con la extensión del conector original para alimentación del módulo de control, el cual usa 4 pines: 2 de ellos como alimentación (VCC y GND) y los otros 2 con el manejo de los actuadores para la etapa de expansión.

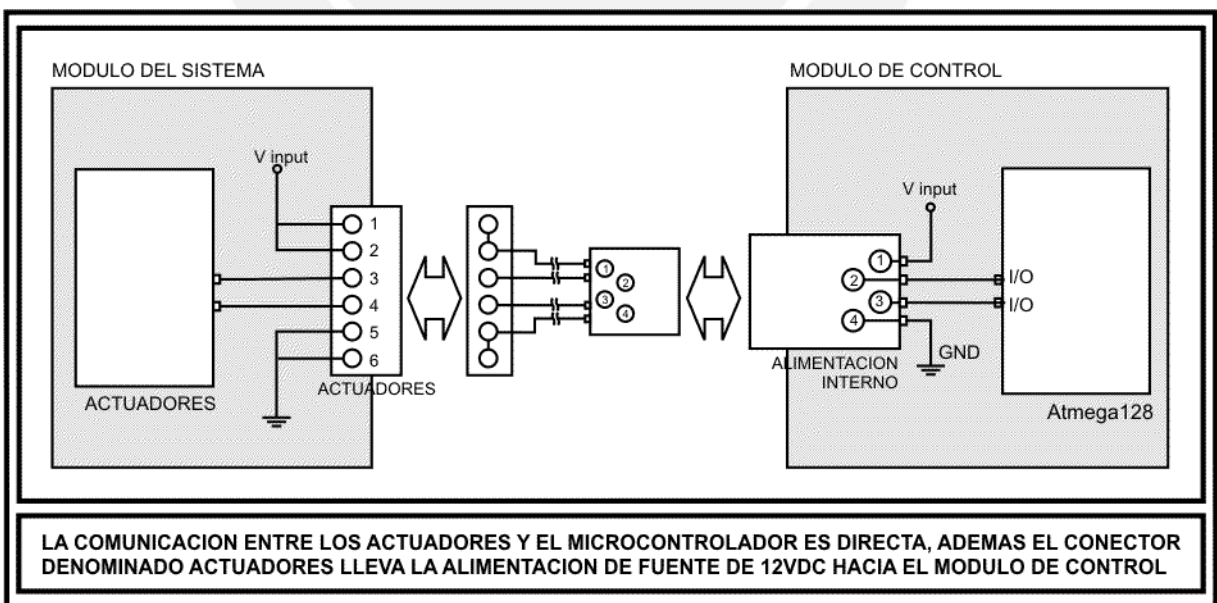


Figura 3.36 – Conector ACTUADORES interno

- El conector SERIAL se encarga de traer los 5VDC regulados en el Módulo de control hasta la tarjeta de componentes desarrollada, además de los pines de control desde el microcontrolador para la lógica RS-485.

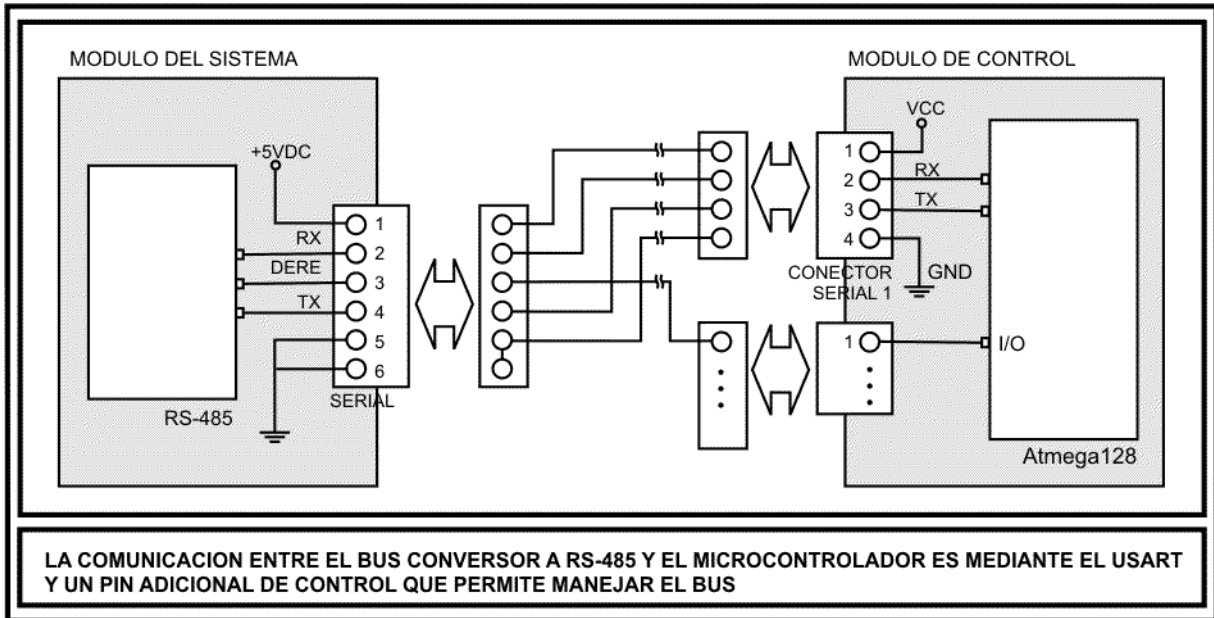


Figura 3.37 – Conector SERIAL interno

- EL conector TCP/IP solo es una extensión del RJ-45 que sale del módulo de control. La tarjeta de componentes desarrollada posee dos diferentes conectores para comodidad en las pruebas del prototipo.

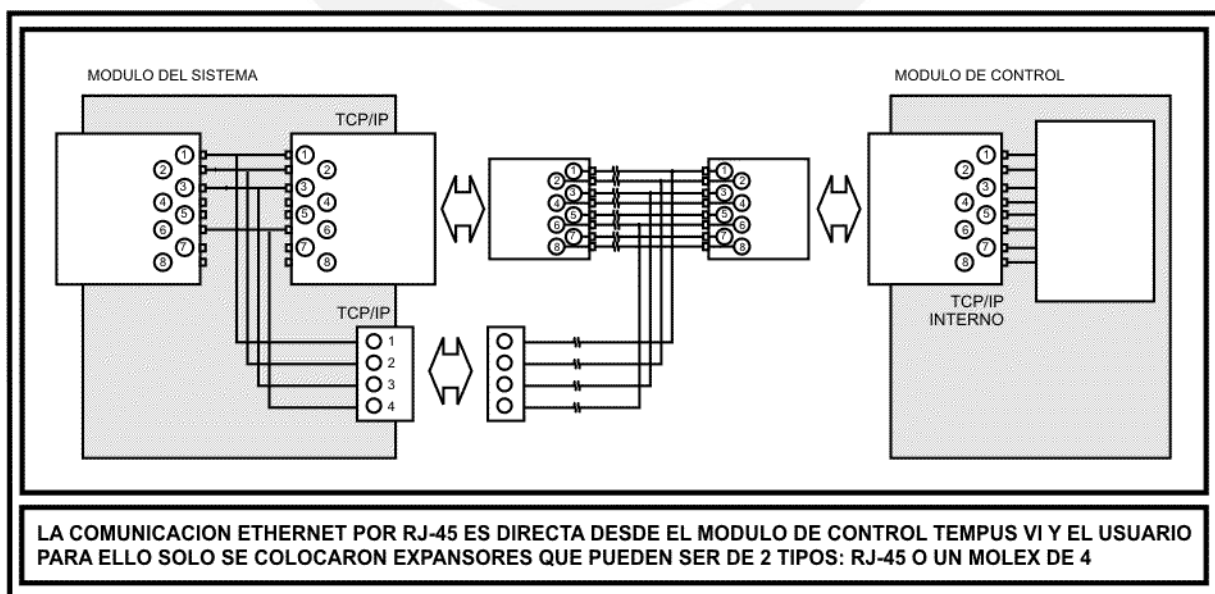


Figura 3.38 – Conector TCP/IP interno

### 3.7 DISEÑO MECANICO DEL CHASIS

La última etapa, y no menos importante, del proyecto fue el diseño del chasis cuya función será de contener, proteger y aislar las tarjetas de componentes del sistema con el exterior, además de brindar comodidad para el manejo del sistema.

El material con el que se trabajó fue Hierro (Fe) de calidad 10/10 de grosor 1/20 pulgadas, conocido como lata de aleación. Se eligió dicho material por sus capacidades magnéticas y conductivas lo cual asegura un buen aislamiento a campos magnéticos externos para la parte interna de la caja del chasis, conformando de ese modo la denominada Jaula de Faraday. La protección Farádica evitará que el ruido eléctrico afecte en gran medida las señales analógicas sensadas por el sistema.

Las características físicas se determinaron respetando dimensiones de un rack estándar con una altura de 2U (465mm x 625mm x 90mm aprox.) y se realizó con un diseño simple, como se observa en la Figura 3.39.

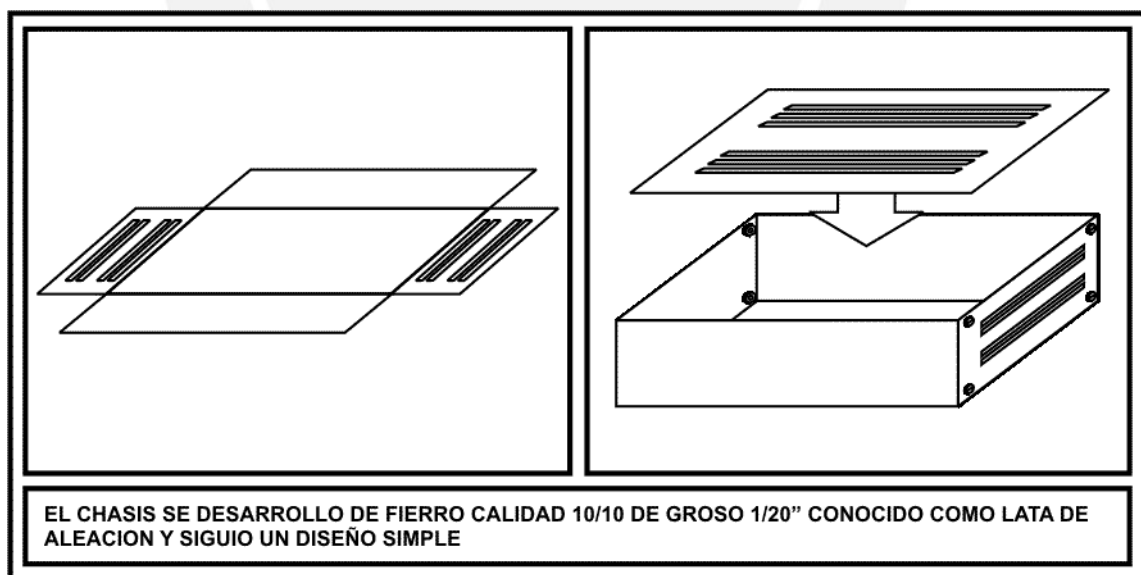


Figura 3.39 – Diseño del chasis del equipo

Para que los conectores de la tarjeta del sistema puedan comunicarse con el exterior se hicieron agujeros a medida en la parte Posterior del chasis; del mismo modo, en la parte Frontal se hicieron agujeros para la salida del teclado y del visualizador.

Además posee agujeros para sujeción interna de las tarjetas, encontrando una buena disposición entre espacio y cableado.

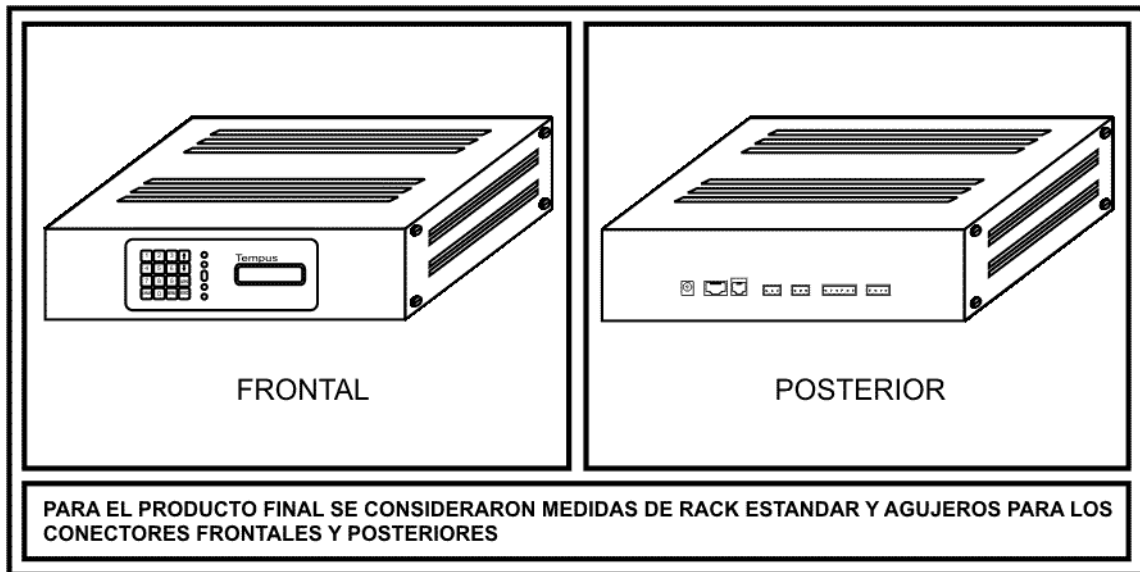


Figura 3.40 – Vista frontal y posterior en diseño

El color final es negro, para hacer referencia a la tonalidad estándar de los productos comerciales.



Figura 3.41 – Vista superior, frontal y posterior del chasis

### 3.8 DISTRIBUCIÓN DE MÓDULOS

La distribución de las tarjetas en el chasis y sus componentes es la siguiente:

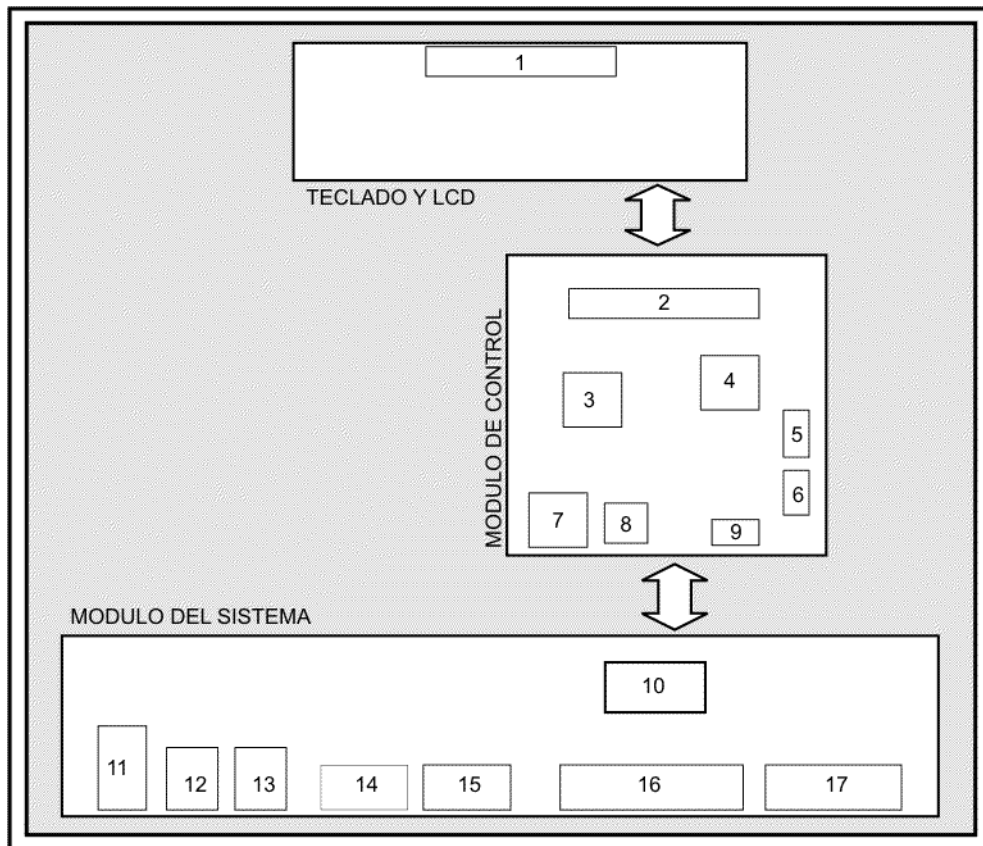


Figura 3.42 – Diagrama de bloques de las tarjetas del sistema

<b>MÓDULO DE TECLADO Y LCD</b>	9 Conector de comunicación SPI
1 Teclado y Display LCD	<b>MÓDULO DEL SISTEMA</b>
<b>MÓDULO DE CONTROL</b>	10 ADE7758
2 Conector hacia el teclado y LCD	11 Conector de alimentación externo
3 Microcontrolador ATmega128	12 Conector de TCP/IP externo
4 Integrado de comunicación a red	13 Conector de expansión y RS-485
5 Puerto de comunicación serial 1	14 Actuador 1 (relé)
6 Puerto de comunicación serial 2	15 Actuador 2 (relé)
7 Conector de TCP/IP interno	16 Conector para medición de corriente
8 Conector de alimentación interno	17 Conector para medición de voltaje

Físicamente, la ubicación de los módulos del sistema:

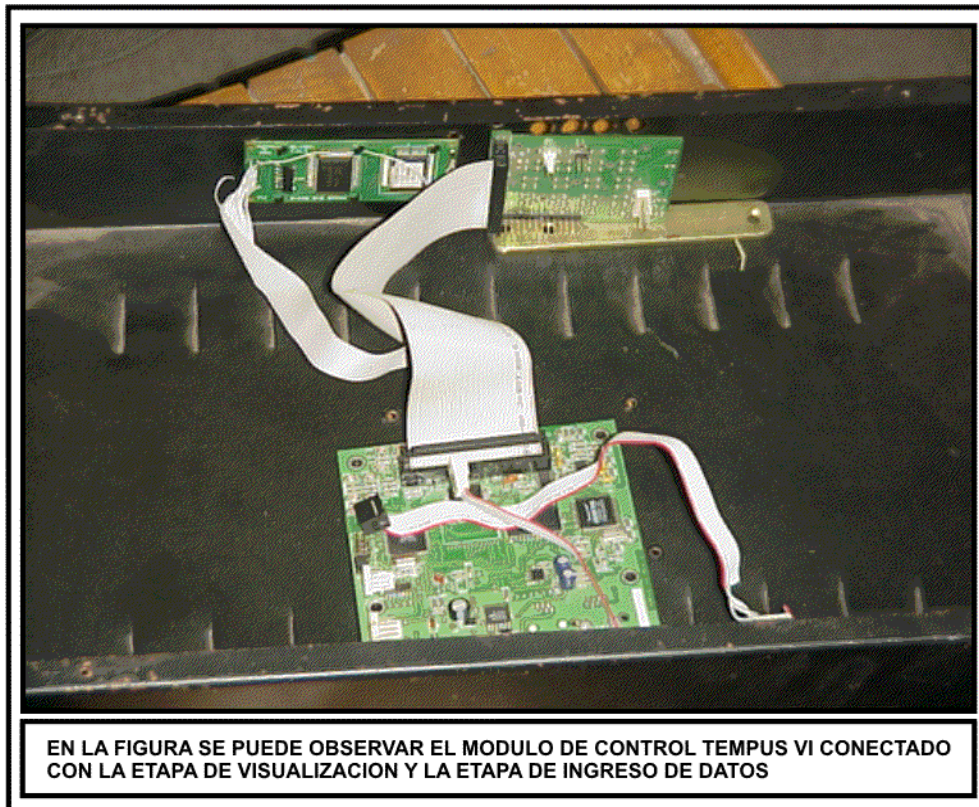


Figura 3.43 – Implementación física del proyecto de tesis



Figura 3.44 –Implementación física del proyecto de tesis

## CAPÍTULO 4

### EVALUACIÓN DE RESULTADOS

#### 4.1 DESARROLLO DEL PROTOTIPO

De los módulos considerados en el sistema de control digital para medición:

- Módulo del sistema: Investigado, diseñado e implementado como proyecto de tesis (contiene la lógica para medición, expansión y alimentación).

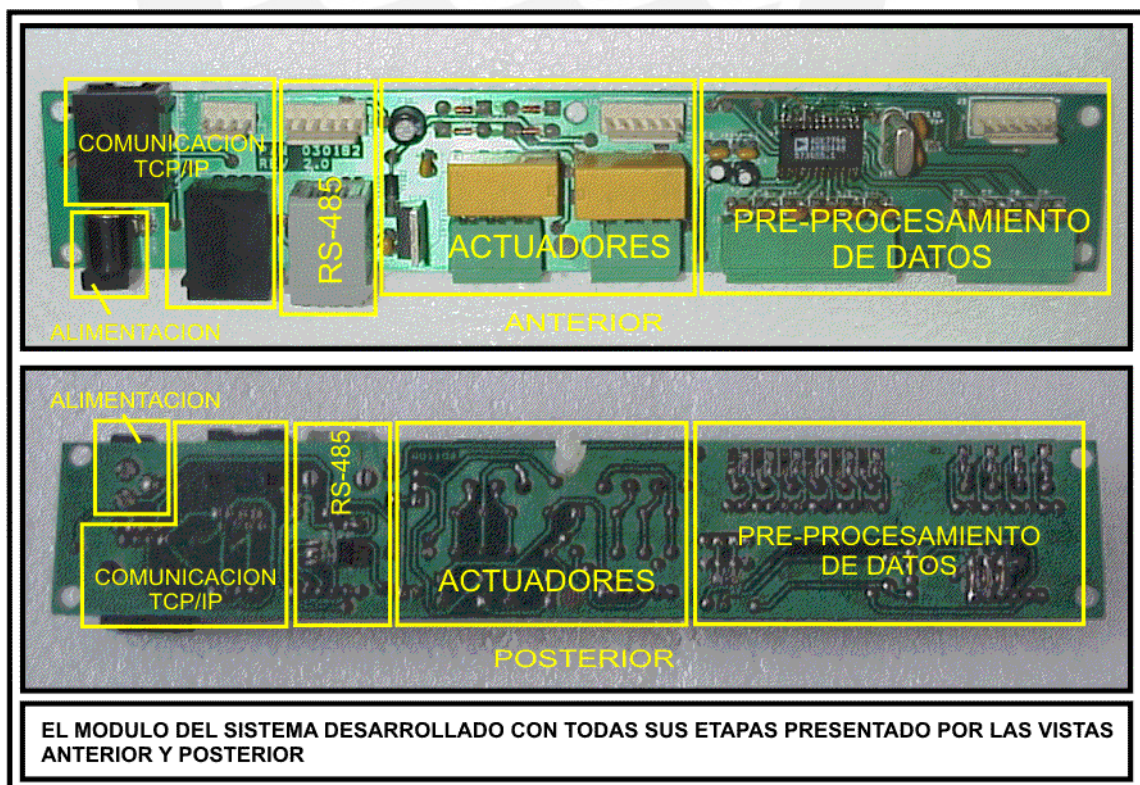


Figura 4.1 – Módulo del sistema

- Teclado y LCD: Implementación a partir de su diseño simple de conexión.
- Módulo de control: Facilitado por la empresa Sistemas Inteligentes S.A.C.

Todos los módulos y etapas del sistema se encuentran funcionales.

De las etapas de programación en los diversos lenguajes:

- Módulo de medición: Lógica realizada en código assembler utilizando para ello el software de programación y motor de compilación AVR Studio 4. Se desarrolló una nueva rutina secuencial basada en la lógica multitareas del firmware original del TEMPUS VI: lógica de interacción con el ADE7758, manejo de teclado, LCD y comunicación a red.

Cabe destacar que el desarrollo del nuevo sistema requirió de un periodo íntegramente destinado al estudio de la tarjeta TEMPUS VI, para manejar sus funciones y luego poder aplicarla como uno de los módulos del proyecto de tesis. Por políticas de confidencialidad de los productos de la empresa desarrolladora no tengo la autorización de publicar los esquemáticos y/o firmwares completos del equipo actual que ellos comercializan.

## 4.2 EVALUACIÓN DE RESULTADOS

Para reconocer el establecimiento de conexión se acondicionó un software de comunicación PC – TEMPUS VI, llamado Winsock:

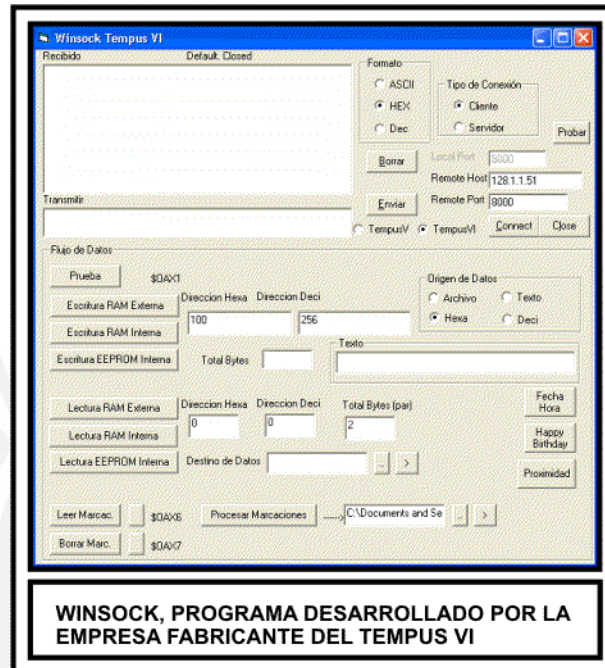


Figura 4.2 – Winsock: Programa para comunicación con el TEMPUS VI

La modificación del programa se puede observar en la Figura 4.3, esta modificación logra leer con un PC los registros internos del ADE7758 en el prototipo mediante la comunicación TCP/IP

El programa modificado contiene una sección denominada Medidor de energía, en la cual figuran todos los registros que maneja el ADE7758, estos registros están acondicionados como lectura y/o escritura según se indica en el Anexo F: Hojas técnicas (*Hoja técnica del ADE7758. Rev. C - Sección “Registers”, Pág. 60*).

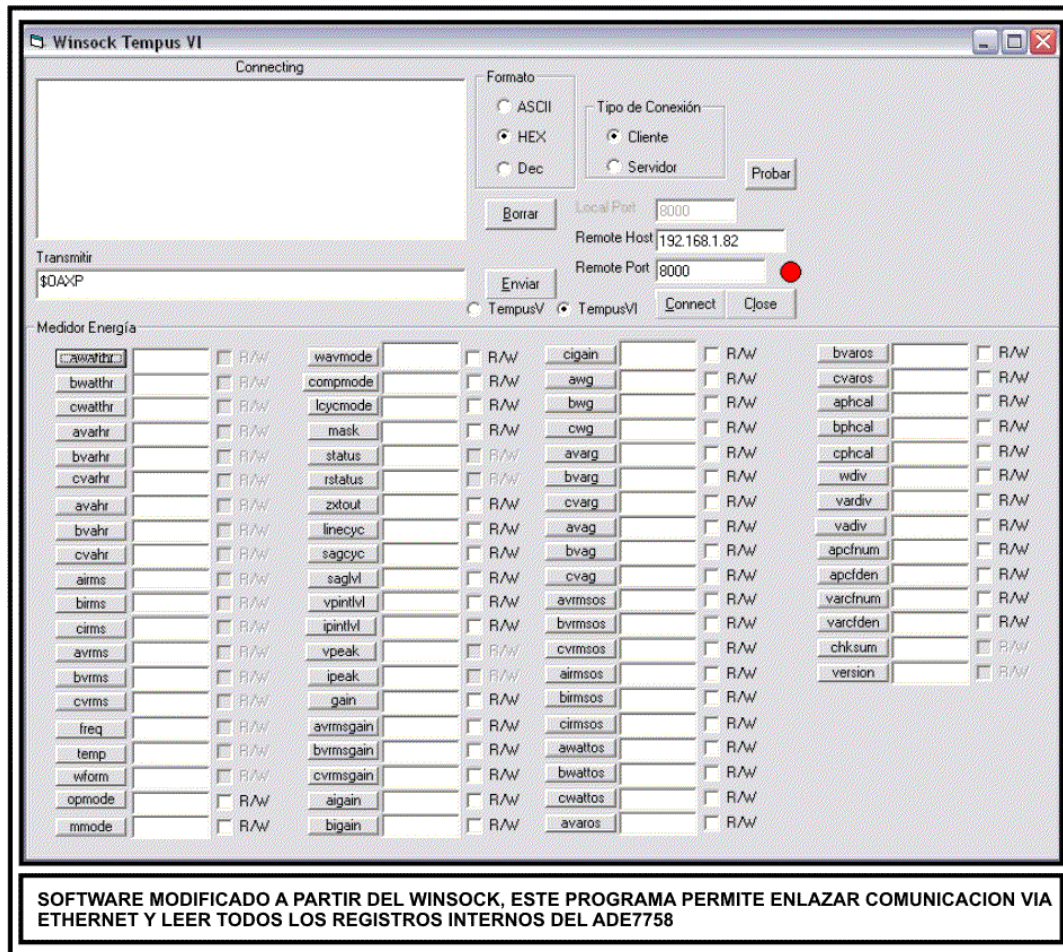


Figura 4.3 – Winsock modificado para lectura de registros del ADE7758

- Las pruebas del software realizadas con el hardware de medición, en lectura y escritura mediante SPI fueron satisfactorias. Estableciéndose conexión correctamente y obteniendo de los registros internos valores idénticos a los especificados en la hoja de datos del ADE7758.
- Las pruebas de comunicación ADE7758 – ATmega128 no presentó errores, salvo por fallas iniciales de sincronización SPI.
- Se realizaron pruebas de las etapas de expansión en conjunto con la lectura/escritura de los registros internos del ADE7758 y los resultados fueron exitosos no encontrándose retardos o fallas debidas al ruido.

### 4.3 ANÁLISIS DE COSTOS

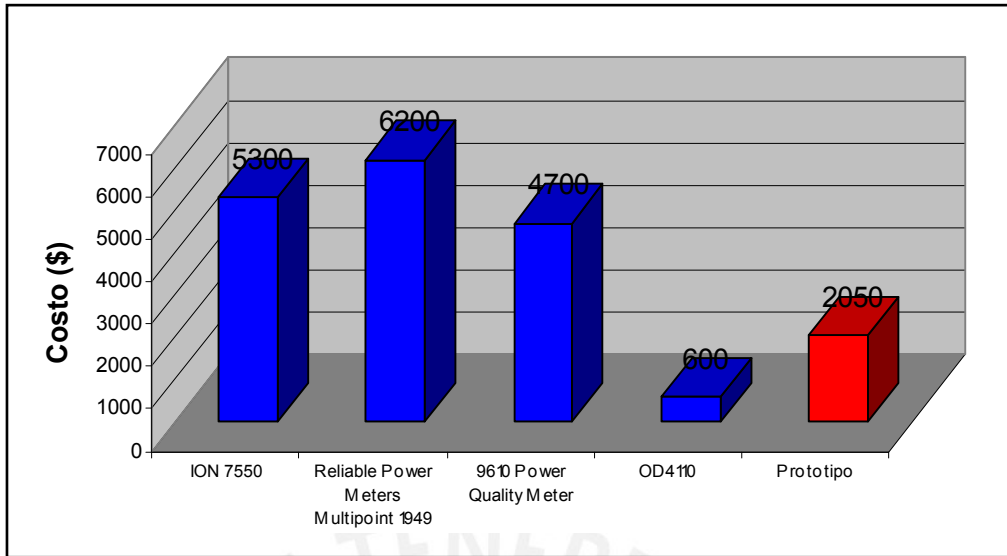
Se hizo un análisis de costos en base al prototipo desarrollado y se le comparó con algunos equipos comerciales. A pesar que el prototipo no es un producto final, y la comparación con los otros equipos no fue directa, en base a los resultados obtenidos de diversos estudios se pudo constatar por que el prototipo posee buenos resultados ante productos comerciales y su desarrollo no va a conllevar a utilizar materiales costosos.

Entonces, es requerido el uso de un sistema del tipo EEM que permita la medición de diversos parámetros eléctricos además de brindar comunicación Ethernet. Existen ciertos requerimientos técnicos para la elaboración del prototipo, los cuales se deben implementar para un desarrollo óptimo,

Cabe resaltar que los equipos aquí expuestos son actualmente comerciales y los datos son en general aproximados pero muy cercanos a la realidad.

	ION 7550	Reliable Power Meters Multipoint 1949	9610 Power Quality Meter	OD4110	Prototipo
<b>FABRICANTE</b>	Schneider Electric	Fluke	Siemens	ABB	
<b>TIPO DE SEÑAL</b>	Trifásico	Monofásico-Trifásico	Trifásico	Trifásico	Trifásico
<b>MEDICIÓN DE VOLTAJE</b>	Si	Si	Si	Si	Si
<b>MEDICIÓN DE CORRIENTE</b>	Si	Si	Si	Si	Si
<b>CALCULO DE POTENCIAS</b>	Activa Reactiva Aparente	Activa Reactiva Aparente	Activa	Activa	Activa Reactiva Aparente
<b>ANALIZADOR DE ENERGÍA</b>	Sobre-voltajes Sobre-corrientes	Armónicos	Armónicos Desfase de red	No	Sobre-voltajes Sobre-corrientes Desfase de red
<b>TIPO DE COMUNICACIÓN</b>	Ethernet	Ethernet RS-485	Ethernet RS-485	No	Ethernet RS-485
<b>COSTO (\$)</b>	5300.00	6200.00	4700.00	600.00	2050.00

**Tabla 4.1 – Comparación de equipos medidores de parámetros eléctricos**



**Figura 4.4 – Comparación en los costos de los equipos**

Como se puede observar en la Figura 4.4 el precio del prototipo es inferior al resto de equipos comerciales con similares características, considerando que el proyecto de tesis es parte de un sistema mayor y que aún se encuentra en desarrollo, en la Tabla 4.1 se ha asumido un costo igual al doble de lo invertido en el desarrollo actual.

A continuación se muestra una tabla con los precios aproximados, de las diversas partes del prototipo realizado (Tabla 4.2).

Sistema de control digital de parámetros eléctricos	Costo (\$)
Módulo TEMPUS VI	100.00
Etapa de Pre-procesamiento de datos	20.00
Etapa de Visualización de datos	20.00
Etapa de control y comunicación	15.00
Etapa de expansión	50.00
Chasis	20.00
Diseño e implementación (8 meses)	800.00
<b>TOTAL</b>	<b>1025.00</b>

**Tabla 4.2 – Costo del Sistema de Presión Negativa**

4.4 PRUEBAS DEL PROTOTIPO



Figura 4.5 – Pruebas del prototipo



Figura 4.6 –Pruebas del prototipo



Figura 4.7 – Pruebas del prototipo

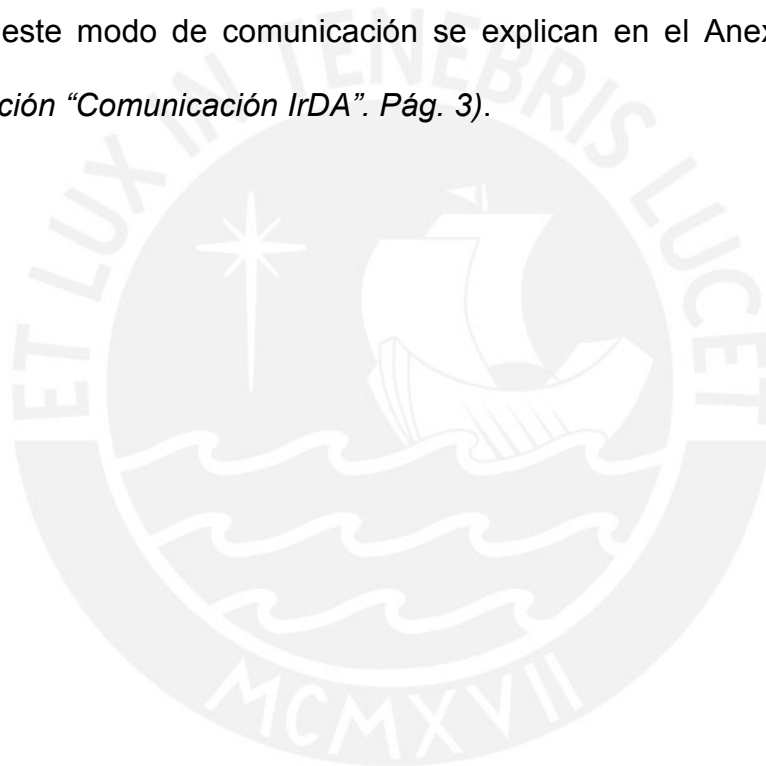
#### 4.5 RECOMENDACIONES

Finalizado el proyecto de tesis, luego de meses de intenso trabajo, se procede a plantear las siguientes recomendaciones pues, como se mencionó, el equipo desarrollado es parte de un sistema mayor de medición de parámetros eléctricos. Las recomendaciones tienen por objetivo plantear las tareas a resolver para futuras investigaciones en este tema:

- Ahondar en el estudio de corrientes y voltajes de las fuentes directas de alimentación industrial (220VAC, 380VAC, 440VAC, etc.) para así desarrollar el ACONDICIONAMIENTO DE DATOS y se pueda hacer experimentaciones con señales eléctricas reales.
- Desarrollar un software sencillo para PC de interacción con el usuario, que en lo posible sea de manejo intuitivo y no presente datos a nivel programador.
- El ADE7758 presenta entre sus diversas configuraciones el modo de integrador para la corriente de entrada. Una solución de mejorar y disminuir costos es utilizando la denominada bobina de Rogowski para la etapa de sensado corriente como se explica en el Anexo C: Tecnologías para medición de corriente (*Sección “Bobina Rogowski”. Pág. 11*).
- De los parámetros eléctricos registrados por el ADE7758, se puede encontrar aplicaciones futuras mejorando la lógica de control para que se encargue de

procesar mayores datos eléctricos, por ejemplo el cálculo de armónicos de la red y adicionalmente el efecto del ruido Flicker.

- Con el objetivo de comunicación con otros dispositivos, se investigó un modo de intercambio de datos infrarrojos denominado IrDA, que actualmente se utiliza en PDAs y celulares. La recomendación se enfoca en implementar el protocolo IrDA para utilizar las PALM a modo de control remoto especializado para el equipo. Los datos de este modo de comunicación se explican en el Anexo B: Comunicación IrDA (*Sección “Comunicación IrDA”. Pág. 3*).



## CONCLUSIONES

De la presente investigación se desprenden una serie de conclusiones relevantes no tan sólo enfocadas en temas de medición de parámetros eléctricos y comunicaciones, sino que permiten reflexionar sobre situaciones, planteamientos, que en un principio no eran trascendentales, y que finalmente afectaron la forma de ejecutar el trabajo, mostrando así una forma de afrontar proyectos futuros como Ingeniero Electrónico:

- Se ha logrado desarrollar un sistema de control digital que, a pesar de ser la etapa inicial, posee características avanzadas tal cual las presentan equipos comerciales. Además de lograr la base para un sistema EEM, el prototipo posee un bajo costo, y puede ser íntegramente desarrollado en el país.
- Como elemento clave del sistema, se destaca el dispositivo ADE7758 que aunque presentó dificultades para la manipulación, representa una herramienta muy poderosa y económica, para la medición de parámetros de calidad de energía. Contemplando las múltiples alternativas y opciones de medición que ofrece el dispositivo, se considera que puede ser la base para desarrollar equipos de gestión

de parámetros de energía a nivel domiciliario, por lo que recomiendo promover su profundización para desarrollo de futuros trabajos de grado.

- A pesar de haber sido desarrollada para otro fin, la tarjeta TEMPUS VI ha mostrado ser lo suficientemente versátil para cumplir con la función de control y cálculo de parámetros eléctricos.
- Se considera significativo resaltar la importancia del montaje físico para todo proyecto y lo atractivo de una interfaz gráfica en el desarrollo de software. Desde el punto de vista comercial es fundamental tener en cuenta cada detalle en lo referente al montaje y condiciones específicas del cliente.
- Otro aspecto el cual no debe pasar por alto es la importancia del análisis de costos, ya que el éxito en el desarrollo de proyectos incluye una adecuada planificación de todas las variables externas, imprevistos, disponibilidad de elementos y todos los incrementos que esto puede traer a un proyecto real, pudiendo convertirlo en un fracaso o éxito rotundo. Lo anterior se resalta teniendo en cuenta que en el desarrollo del presente proyecto se presentaron situaciones que no fueron planificadas ni proyectadas a nivel de costos y que aumentaron el valor final del producto desarrollado; pero precisamente ayuda a reflexionar sobre la importancia de la planificación y el análisis previo de manera global.
- Finalmente, por las diversas características integradas en el sistema de control para medición, se concluye que se ha desarrollado un prototipo muy competitivo que cubre con todos los objetivos planteados.

## FUENTES

- [1] MINISTERIO DE ENERGÍA Y MINAS – PERU  
2005 – Compendio de normas del sub-sector electricidad  
<http://www.minem.gob.pe/electricidad/index.asp>
- [2] The ABB Group  
2001 October – ODIN Meter An electricity energy meter from ABB: Technical documentation  
[http://www.abb.nl/GLOBAL/NLABB/NLABB032.NSF/viewunid/7209F451A8659515C1256B82004C3D80/\\$file/Odin+meter+\(E\).pdf](http://www.abb.nl/GLOBAL/NLABB/NLABB032.NSF/viewunid/7209F451A8659515C1256B82004C3D80/$file/Odin+meter+(E).pdf)  
[Consultado: 25/Oct/2005]
- [3] KARCZ, ANDRES M.  
1977 – Fundamentos de metrología electrónica – Tomo III: Potencia y energía  
Ediciones Técnicas Marcombo S.A., Boixareu editores. Barcelona – España.
- [4] KINNARD, ISAAC F.  
1958 – Medidas eléctricas y sus aplicaciones  
Ediciones Técnicas Marcombo S.A. – Barcelona, España
- [5] KARSA, BÉLA E.  
1967 – Electrical measuring instruments and measurements  
Ed. Akadémiai Kiadó & Villamos mérőműszerek és mérések. Budapest - Hungary

- [6] Instituto Nacional de Defensa de la Competencia y de la Protección de la Propiedad Intelectual – INDECOPI  
2005 – Servicio Nacional de Metrología – Metrología y calibración  
<http://www.indecopi.gob.pe/nuestrosservicios/metrologiaycalibracion>  
[Consultado: 27/Oct/2005]
- [7] EL PERUANO (diario oficial)  
2001 – Ministerio de energía y minas. Dirección general de Electricidad.  
Código nacional de electricidad suministro 2001.  
Resolución Ministerial N° 366-2001-EM/VME  
[http://www.editoraperu.com.pe/normas/Pdfs/cod\\_nc\\_Elec.pdf](http://www.editoraperu.com.pe/normas/Pdfs/cod_nc_Elec.pdf)  
[Consultado: 27/Oct/2005]
- [8] Gobierno del Perú  
Ley N° 23560 - Sistema Legal de Unidades de Medida del Perú (SLUMP)  
Promulgado: 31-Dic-1982. Según Decreto Supremo N° 026-93-ITINCI  
[Vigente hasta el presente: 27/Oct/2005]
- [9] METERING INTERNATIONAL  
2002 – Magazine archive. Issue 1. Measuring reactive power in energy meters  
[http://www.metering.com/archive/021/52\\_1.htm](http://www.metering.com/archive/021/52_1.htm)  
[Consultado: 28/Oct/2005]
- [10] METERING INTERNATIONAL  
2003 – Magazine archive. Energy measurement ICs.  
[http://www.metering.com/archive/031/42\\_1.htm](http://www.metering.com/archive/031/42_1.htm)  
[Consultado: 28/Oct/2005]
- [11] GERENCIA ADJUNTA DE REGULACIÓN TARIFARIA (GART) – COMISIÓN DE TARIFAS ELÉCTRICAS  
1997 – Resolución de la comisión de tarifas eléctricas No. 024-97 P/CTE  
<http://www.cte.org.pe/resoluciones/pdf/RE024-1997.pdf>  
[Consultado: 04/Nov/2005]
- [12] Gobierno del Perú  
Decreto Supremo N° 016-2000-EM – Fijan horas de regulación y probabilidad de excedencia mensual de centrales hidráulicas, horas punta del sistema eléctrico y margen de reserva a que se refiere el Reglamento de la Ley de Concesiones Eléctricas. Incluye modificaciones según Decreto Supremo N° 032-2001-EM; Decreto Supremo N° 034-2001-EM y D.S. N° 055-2002-EM  
Artículo 2°  
Promulgado: 13-Sep-2000

- [13] Gobierno del Perú  
Decreto Supremo N° 027-2003-EM.- Fijan horas de punta del Sistema Eléctrico Interconectado  
Artículo 1°  
Promulgado: 06-Ago-2003
- [14] JUAN LUIS HERNÁNDEZ  
2004 – Factor de Potencia (FDP)  
<http://endrino.cnice.mecd.es/~jhem0027/fdp/fdp.htm>  
[Consultado: 28/Oct/2005]
- [15] CRISTOPHER E. STRANGIO  
2005 – The RS-232 standard  
CAMI Research Inc., Lexington, Massachusett. – USA.  
[http://www.camiresearch.com/Data\\_Com\\_Basics/RS232\\_standard.html](http://www.camiresearch.com/Data_Com_Basics/RS232_standard.html)
- [16] THE MATHWORKS – ACCELERATING THE PACE OF ENGINEERING AND SCIENCE  
2005 – Serial Port Interface Standard  
The MathWorks Inc. – USA.  
<http://www.mathworks.com/access/helpdesk/help/toolbox/instrument>  
[Consultado: 28/Oct/2005]
- [17] CISCO SYSTEMS INC.  
2005 - Ethernet Technologies documentation  
[http://www.cisco.com/univercd/cc/td/doc/cisintwk/ito\\_doc/ethernet.htm](http://www.cisco.com/univercd/cc/td/doc/cisintwk/ito_doc/ethernet.htm)  
[Consultado: 28/Oct/2005]
- [18] PROCOBRE  
Confiabilidad de Sistemas Eléctricos  
[http://www.procobreperu.org/c\\_confiabelec.pdf](http://www.procobreperu.org/c_confiabelec.pdf)  
[Consultado: 30/Oct/2005]
- [19] VIERA DE CARVALHO, ARNALDO; POVEDA, MANUEL; ZAK, JUAN  
1996 - OLADE : Diseño de Programas de Eficiencia energética.  
Revista Energética N°3, Septiembre-Diciembre 1996. Pag. 6 y 7
- [20] HANDHELD BASIC ++  
HB++, The best development enviroment for Palm Powered handhelds  
<http://www.handheld-basic.com/>  
[Consultado: 06/Jul/2006]

- [21] PALM ONE  
Welcome to palm  
<http://www.palm.com/>  
[Consultado: 06/Jul/2006]
- [22] TEMPUS  
Tempus  
<http://www.tempus.com.pe/>  
[Consultado: 06/Jul/2006]
- [23] INFARED DATA ASSOCIATION - IRDA  
International organization that creates and promotes interoperable, low cost  
infrared data interconnection  
[www.irda.org/](http://www.irda.org/)  
[Consultado: 06/Jul/2006]
- [24] LUIS ERNESTO BORGES  
Sistemas de lectura remota del consumo  
<http://neutron.ing.ucv.ve/>  
[Consultado: 13/Nov/2006]
- [25] ENERGY COMMISSION  
Energy Commission History  
<http://www.a2gov.org/PublicServices/SystemsPlanning/Energy/EnergyCommissionHistory.html>  
[Consultado: 16/Oct/2006]
- [26] THE WORLD BANK  
[www.worldbank.org](http://www.worldbank.org)  
Peru Data Profile  
<http://devdata.worldbank.org/external/CPProfile.asp?SelectedCountry=PER&CODE=PER&CNAME=Peru&PTYPE=CP>  
[Consultado: 12/Ene/2007]

**PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERU**  
**Facultad de Ciencias e Ingeniería**



**DISEÑO E IMPLEMENTACIÓN DE UN SISTEMA DE  
CONTROL DIGITAL CON CONEXIÓN A REDES DE  
DATOS PARA MEDICIÓN DE PARÁMETROS  
ELÉCTRICOS**

**ANEXOS**

**Presentado por:**  
**Gerardo Manuel Guerrero Quichiz**

**Lima – Perú**  
**2007**

## RESUMEN

La introducción y continua mejora de elementos digitales en dispositivos, que antes se consideraban íntegramente analógicos, han causado toda una revolución en los diversos campos de los sistemas electrónicos. Dichos cambios han logrado integrar sistemas que, hasta hace unos años, no se consideraban dentro de una misma área temática. El presente proyecto de tesis busca ampliar la aplicación de la electrónica digital fusionando el área de Electricidad con la de Comunicaciones y desarrollando un Sistema de control digital basado en la tecnología del microcontrolador ATmega128 de la compañía ATMEL y del circuito integrado ADE7758 de Analog Devices, que además posea la lógica adecuada para la medición trifásica de parámetros eléctricos y permita la comunicación a redes de datos.

Con dicha aplicación será la etapa principal y básica de un sistema mayor, encargado de la medición digital de energía eléctrica trifásica en media y baja tensión, con un bajo porcentaje de error que permita comunicación remota en tiempo real de los parámetros eléctricos sensados (Voltaje RMS, Corriente RMS; Potencia Activa, Potencia Reactiva, Potencia Aparente, entre otros) hacia un computador de la red. La tesis comprenderá el desarrollo del sistema de control con la lógica adecuada para el procesamiento futuro de medición y de comunicación; contando con etapas de ingreso de datos, pre-procesamiento, control, visualización, comunicación y expansiones para mejoras futuras.

Respecto a la utilidad del proyecto, ésta se extiende al campo comercial puesto que la integración del proyecto de tesis como Sistema de control digital a un Sistema mayor de medición de energía eléctrica con comunicación en tiempo real dará versatilidad a los procesos industriales, convirtiéndose en un factor clave a nivel económico por el control eficiente del consumo eléctrico que posteriormente se verá reflejado en mejoras de los costos de producción.



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## ANEXO A

### CONECTORES

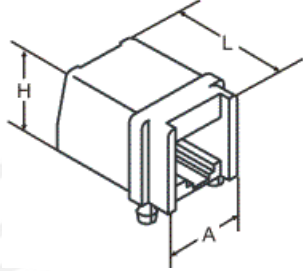
MOLEX BASE Y AEREO DE 6 PINES		
	DIMENSIONES (LxAxH)	9.40 x 23.70 x 8.50 mm (izq) 13.30 x 23.70 x 10.50 mm (der)
	MATERIAL	Bronce, lata plateada Nylon 66
	TENSION NOMINAL	250V AC/DC
	CORRIENTE NOMINAL	10A AC/DC
	CABLE PERMITIDO	22 ~ 16 AWG
	COLOR	Blanco
	TEMPERATURA	-25°C ~ 85°C

MOLEX CONECTOR AEREO		
12.60 mm	DIMENSIONES (L)	
Lata plateada	MATERIAL	
Depende del cable conductor	TENSION NOMINAL	
Depende del cable conductor	CORRIENTE NOMINAL	
30 ~ 12 AWG	CABLE PERMITIDO	
Metálico plateado/dorado	COLOR	
-25°C ~ 85°C	TEMPERATURA	

BLOQUE TERMINAL AEREO DE 6 PINES		
	DIMENSIONES (LxAxH)	17.30 x 23.65 x 15.00 mm
	MATERIAL	6.6 polymide (Nylon)
	TENSION NOMINAL	300V AC/DC
	CORRIENTE NOMINAL	15A AC/DC
	CABLE PERMITIDO	22 ~ 12 AWG
	COLOR	Verde
	TEMPERATURA	-30°C ~ 105°C

BLOQUE TERMINAL BASE DE 6 PINES		
12.00 x 30.48 x 8.30 mm	DIMENSIONES (LxAxH)	
6.6 polymide (Nylon)	MATERIAL	
300V AC/DC	TENSION NOMINAL	
15A AC/DC	CORRIENTE NOMINAL	
No se aplica	CABLE PERMITIDO	
Verde	COLOR	
-30°C ~ 105°C	TEMPERATURA	

RECEPTACULO RJ-45		
	DIMENSIONES (LxAxH)	20.57 x 15.88 x 13.60 mm
	MATERIAL	Black plastic PBT / Nylon Bronce
	NIVELES DE TENSION	120VAC max.
	NIVELES DE CORRIENTE	1.5A max.
	CABLE PERMITIDO	No se aplica
	COLOR	Negro
	TEMPERATURA	-40°C ~ 80°C

RECEPTACULO RJ-11		
20.80 x 29.80 x 12.50 mm	DIMENSIONES (LxAxH)	
Grey plastic / Nylon Bronce	MATERIAL	
120V AC/DC	NIVELES DE TENSION	
1.2A AC/DC	NIVELES DE CORRIENTE	
No se aplica	CABLE PERMITIDO	
Gris	COLOR	
-25°C ~ 95°C	TEMPERATURA	

PLUG DE ALIMENTACION		
	DIMENSIONES (LxAxH)	14.40 x 9.00 x 11.00 mm
	MATERIAL	6.6 polyimide (Nylon) Bronce
	TENSION NOMINAL	24 VDC
	CORRIENTE NOMINAL	5A
	CABLE PERMITIDO	No se aplica
	COLOR	Negro
	TEMPERATURA	-30°C ~ 120°C

## ANEXO B

### COMUNICACIÓN IrDA

#### **A) TRANSDUCTOR IrDA**

##### **Descripción**

Un transductor IrDA permite realizar conversión de datos de una UART (Universal asynchronous receiver transmitter o Receptor Transmisor Asíncrono Universal) a la codificación IrDA, que es el formato que utilizan las PDAs para realizar transmisión por su puerto infrarrojo.

##### **Criterios de selección**

Por efecto de ahorro de presupuesto se buscará un componente que permita la conexión más sencilla para los datos del UART del microcontrolador con una salida de datos infrarrojos en protocolo IrDA, además de su disponibilidad en el mercado.

##### **Componente seleccionado**

El componente seleccionado fue el MCP2120, Codificador/Decodificador de infrarrojo de la compañía Microchip. Los datos de una UART estándar se ingresan a este integrado, el cual procesa los datos recibidos y los convierte en pulsos para enviar a un emisor de infrarrojos; adicionalmente para la salida de datos se hace uso de un emisor/receptor infrarrojo, también llamado transceptor óptico, para el cual se ha seleccionado el IrDA transceiver de Sharp, GP2W0110YPS. Los datos recibidos por un receptor de infrarrojos como el elegido se ingresan al MCP2120 y son convertidos a datos para una UART estándar.

La velocidad de transferencia (en baudios o bits por segundo) se define con unas entradas del integrado, que permiten seleccionar entre un amplio rango de velocidades (dependiendo también de la frecuencia de reloj que se aplica al circuito).

### B) DISEÑO DE LA ETAPA

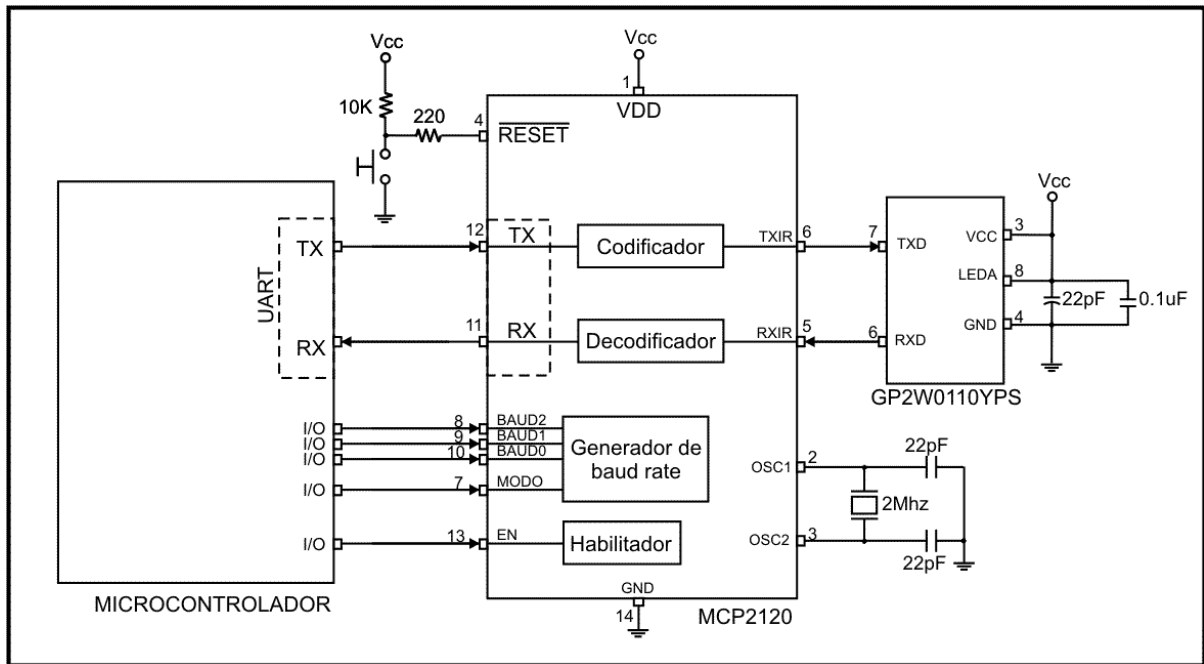


Figura: Esquema del transductor IrDA

La lógica de funcionamiento del MCP2120 es la siguiente:

Para codificación de UART a IrDA

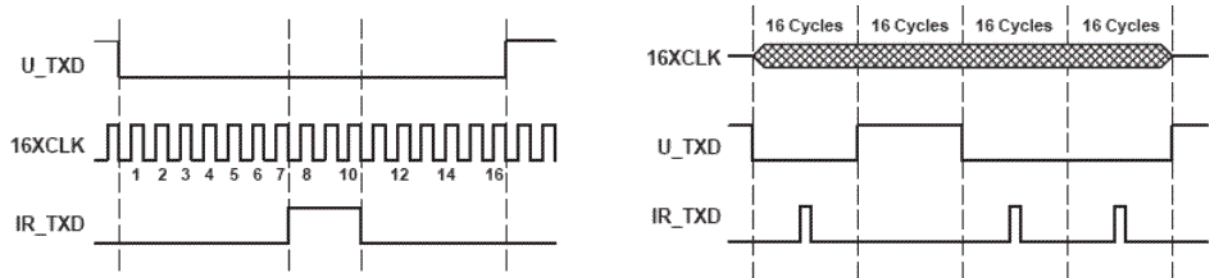


Figura: Diagrama de tiempos de la conversión USART- IrDA

El clock ingresado en los pines de BAUD, se divide en 16 clocks, de los cuales, por cada bit 0 del UART el codificador cuenta 7 ciclos de este 16clock, luego pone en alta la salida durante 3 ciclos de 16clock y finalmente lo envía nuevamente a cero hasta terminar los 16 clocks; por cada bit en 1, mantiene su salida en un valor bajo.

Para decodificación de IrDA a UART

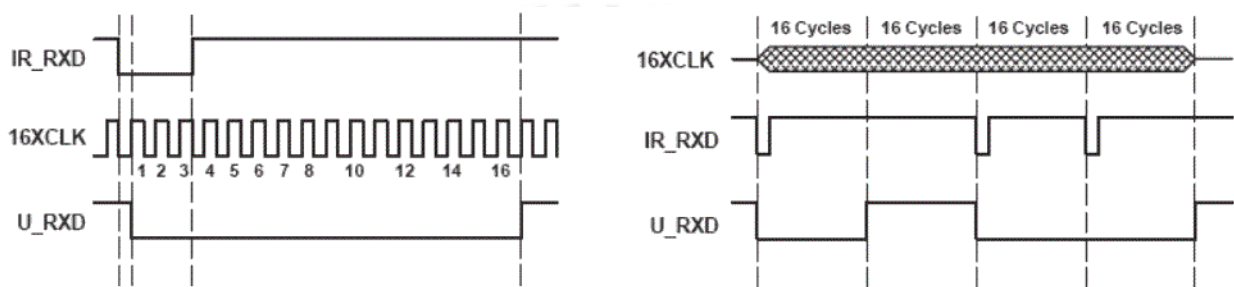


Figura: Diagrama de tiempos de la conversión IrDA- USART

El clock ingresado en los pines de BAUD, se divide en 16 clocks, de los cuales, por cada bit 1 recibido por el puerto infrarrojo envía la salida del UART a cero (con un pequeño de aproximadamente medio ciclo de 16clock); por cada bit 0 recibido envía que la salida del UART sea uno.

### C) PROGRAMACION PARA PDAs

Entre las diversas PDAs existentes en el mercado, he elegido trabajar con los dispositivos móviles de la compañía PALM ONE por su disponibilidad en el mercado peruano actual. En la investigación de lenguajes y entornos de programación para PALMs he tratado de cubrir la mayoría de Sistemas Operativos (SO) que posee esta firma.

## Descripción

Un entorno de programación para PALMs es un programa que se ubica en una PC, denominada como PC de programación, en la cual se desarrollará un código específico basado en un lenguaje de medio o alto nivel. Los entornos de programación luego que han recibido el código en un lenguaje de programación determinado se encargan de procesar los datos ingresados y los convierten en códigos de lenguaje máquina, los cuales pueden a su vez generar ejecutables o instaladores.

## Criterios de selección

Para la selección del entorno de programación adecuado, primero se realizó un análisis de las limitaciones que poseo como programador, pues la programación en lenguajes de alto nivel no es un área que nos llegue a competir a los estudiantes de electrónica, entonces la primera característica que debía poseer el entorno de programación es que sea de cómodo entendimiento, ni que demande grandes y complejos conocimientos en el tema. Adicionalmente, el entorno de programación debía soportar como mínimo compiladores para equipos de la compañía PALM y que puedan generar instaladores para las diversas versiones de SO que provee dicha empresa.

## Componente seleccionado

Entre los entornos de programación investigados se hallaban:

- SUPERWABA: Entorno de programación basado en tecnología Java, con manejo de objetos. No genera código nativos de PALM sino que requiere la instalación una maquina virtual de Waba para la correcta ejecución de sus instaladores. Para iniciar el modo de programación se requiere de otros

entornos en JAVA (ECLIPSE, NETBEAMS, ente otros) y su configuración inicial no es apta para principiantes en el tema de programación. Es gratis y de descarga libre a sola suscripción.

- CODEWARRIOR: Entorno de programación basado en lenguaje C, C+, C++, es un código que lo provee la misma empresa PALM ONE para el desarrollo de programas para sus equipos. Al no ser un código abierto y de libre descarga se hace difícil probarlo en todas sus funciones.
- HANDHELD BASIC++ (HB++): El HandHeld Basic al igual que el CodeWarrior no es un entorno de programación de libre acceso y libre de descarga. Sin embargo los límites de la versión libre a comparación de la versión profesional, sólo radican en un mensaje de alerta que indica que el software es libre, sin limitación de funciones o librerías para funciones complejas. Es un entorno que ha sido desarrollado basándose en Visual Basic y Visual C++, convirtiéndose en un lenguaje muy gráfico.

Finalmente se seleccionó el entorno del HB++, por la comodidad de su código y por su entorno tan visual, que no difiere de las versiones de VISUAL BASIC, además posee diversos ejemplos de programas en donde se pueden apreciar los códigos de programación que realizó la propia empresa HB++.

Otra de las ventajas de este entorno de programación para PDAs es que permite crear instaladores en código nativo para PALMs y en casi todas las versiones existentes de SO que tiene PALM en el mercado.

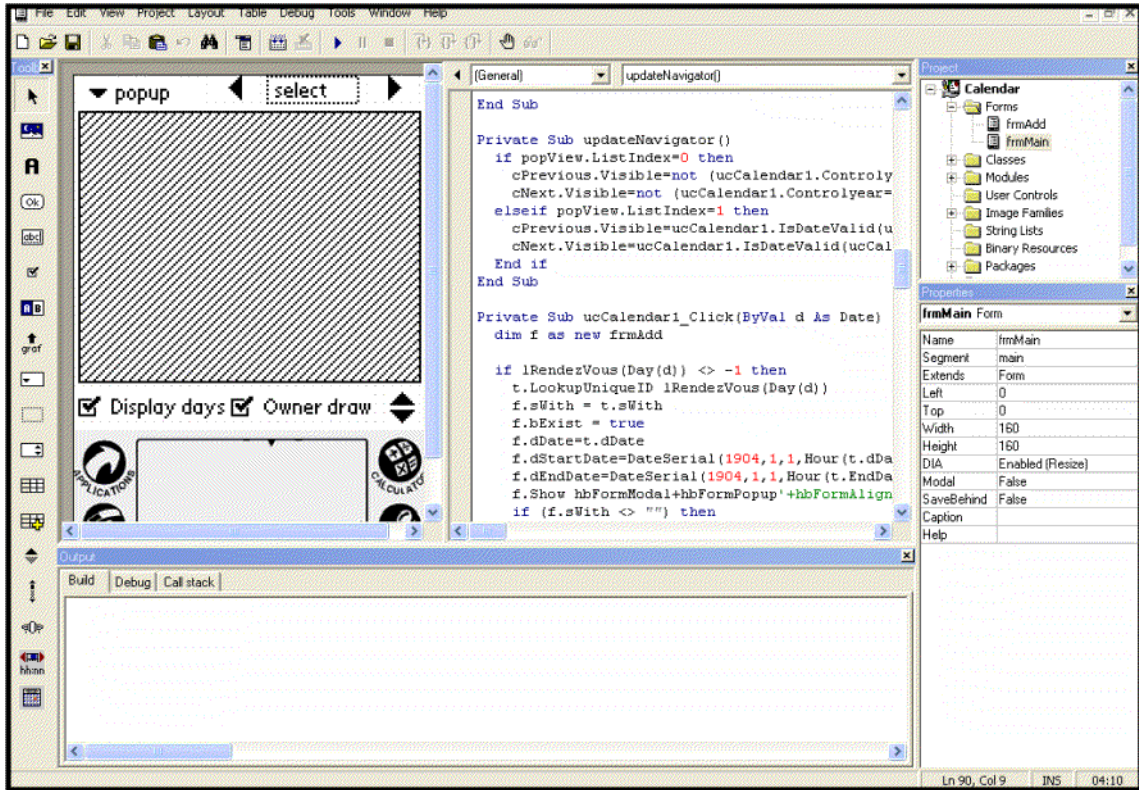


Figura: Ventana de programación del entorno HB++

Además, para hacer las respectivas pruebas y compilaciones en tiempo real, hace uso del emulador para PALM que provee como libre descarga la compañía PALM ONE.

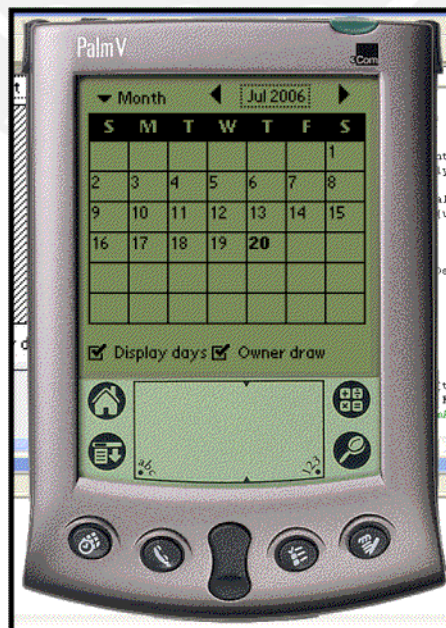


Figura: Emulador provisto por PALM ONE

## ANEXO C

### TECNOLOGÍAS PARA MEDICIÓN DE CORRIENTE

Los modernos medidores de energía de estado sólido contienen elementos sensores tanto de voltaje como de corriente. La lectura del voltaje se consigue típicamente al dividir el voltaje de la línea por medio de un divisor con resistencias o un transformador de potencial, cuando se necesita aislamiento de la línea. Sin embargo, la lectura de la corriente es un problema bastante más complejo de resolver. No solamente el sensor de corriente exige un rango de medición mucho mayor, sino que éste también necesita manipular un rango de frecuencias mucho más amplio dado el rico contenido de armónicas en la onda de corriente.

#### **A) SHUNT DE CORRIENTE DE BAJA RESISTENCIA**

El modelo de ésta tecnología es el de una resistencia, es la solución de más bajo costo actualmente disponible y ofrece una lectura sencilla con excelente precisión. Cuando se estén practicando mediciones de corriente de alta precisión, se debe tener en cuenta la inductancia parásita del Shunt y aunque ésta afecta la magnitud de la impedancia a frecuencias relativamente altas, su efecto sobre la fase a las frecuencias de la línea es suficiente para causar un error notable a bajo factor de potencia. Un desfase de  $0.1^\circ$  llevará a un error de 0.3% aprox. a un factor de potencia de 0.5.

El bajo costo y la alta confiabilidad hacen del Shunt de corriente de baja resistencia una solución popular para la medición de corriente. Sin embargo, dado que el Shunt es fundamentalmente un elemento resistivo, la pérdida de potencia es proporcional al cuadrado de la corriente que pasa por la resistencia y consecuentemente es inusual entre los medidores de energía de alta corriente.

## B) TRANSFORMADOR DE CORRIENTE

El transformador de corriente (TC) usa el principio de un transformador para convertir la alta corriente primaria a una corriente secundaria más pequeña. El TC es común entre los medidores de energía de estado sólido de alta corriente. Es un aparato pasivo que no necesita circuitos adicionales de control. Adicionalmente, el TC puede medir corrientes muy altas y consumir poca potencia.

El inconveniente con los TC se debe a su material ferrítico usado en el núcleo, que se puede saturar cuando la corriente primaria es muy alta o cuando hay un componente importante de DC en la corriente. Una vez magnetizado, el núcleo contendrá histéresis y su precisión se degradará a menos que éste se desmagnetice de nuevo.

## C) SENSOR DE EFECTO HALL

Existen dos tipos principales de sensores de Efecto Hall: anillo abierto (open-loop) y anillo cerrado (closed-loop); el segundo ofrece mejor precisión y rangos dinámicos más amplios pero a un costo mayor. La mayoría de los sensores de Efecto Hall que se encuentran en medidores de energía usan el diseño anillo abierto para lograr costos más bajos.

El sensor de Efecto Hall tiene una excelente respuesta a la frecuencia y está capacitado para medir corrientes muy altas. Sin embargo, las desventajas incluyen un resultado con alta deriva por temperatura y la necesidad de circuitos externos de control. Estos, adicionados al relativo alto costo, hacen de los sensores de Efecto Hall algo raros comparados con los TC.

## D) BOBINA ROGOWSKI

Un modelo sencillo de la bobina Rogowski es un inductor con inductancia mutua con la corriente primaria.

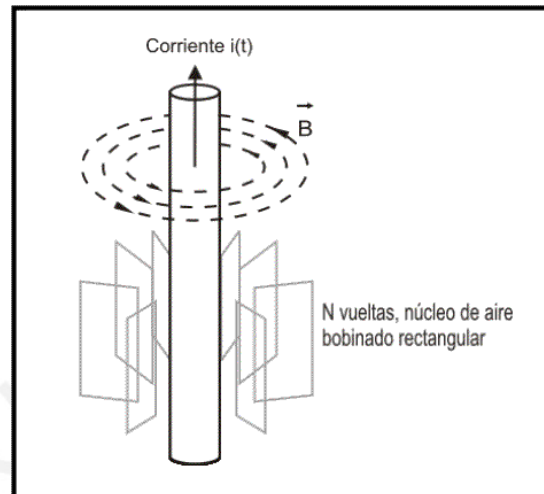


Figura: Modelo básico de conducción

Si una corriente  $i(t)$  pasa a través de un largo conductor en el eje  $z$ , el campo magnético en un punto aleatorio "p" que tiene las coordenadas  $(r, \phi, z)$  en coordenadas cilíndricas es:

$$\vec{B} = \frac{\mu}{2\pi} \times \frac{i(t)}{\rho} \vec{\Phi}$$

La fuerza electromotriz (EMF) generada por el campo magnético en cualquier área en el espacio puede ser calculada usando la ecuación de Maxwell:

$$\text{Electromotive Force (EMF)} = \frac{\partial \vec{B}}{\partial t} \cdot d\vec{S}$$

Asumiendo que hay  $N$  vueltas en la bobina rectangular con núcleo de aire dispuestas en sentido perpendicular al campo magnético, la EMF de la bobina en esta disposición:

$$EMF = \frac{\mu_{air} N L}{2\pi} \ln\left(\frac{c}{b}\right) \frac{di}{dt} = M \frac{di}{dt}$$

El término constante  $M$  se llama la inductancia mutua de la bobina Rogowski, y tiene una unidad Henry (H). Esta indica el nivel de señal de la salida de la bobina por unidad  $di/dt$ . La salida de voltaje de la bobina depende solamente de los cambios en la corriente primaria. Cuando se conecta a un circuito integrado con integrador digital incluido en el chip, hacer un medidor con una bobina Rogowski es tan sencillo como usar sensores de corriente como el TC o el Shunt. La bobina con núcleo de aire no tiene histéresis, saturación, o problemas de no linealidad. Además, tiene una capacidad extraordinaria para manejar altas corrientes donde el límite superior teórico de la bobina es el voltaje de ruptura (breakdown) del mismo aire.

Dado que la salida de la bobina Rogowski es proporcional a la derivada del tiempo de la corriente, es necesario usar un integrador para convertirlo al formato  $i(t)$ . En el dominio de frecuencia, esto es equivalente a una atenuación de  $-20$  dB/dec y un cambio constante de fase de  $-90^\circ$ . Las figuras muestran las respuestas de frecuencia y de fase del integrador digital implementado para medición de energía en el circuito integrado ADE7758 de Analog Devices.

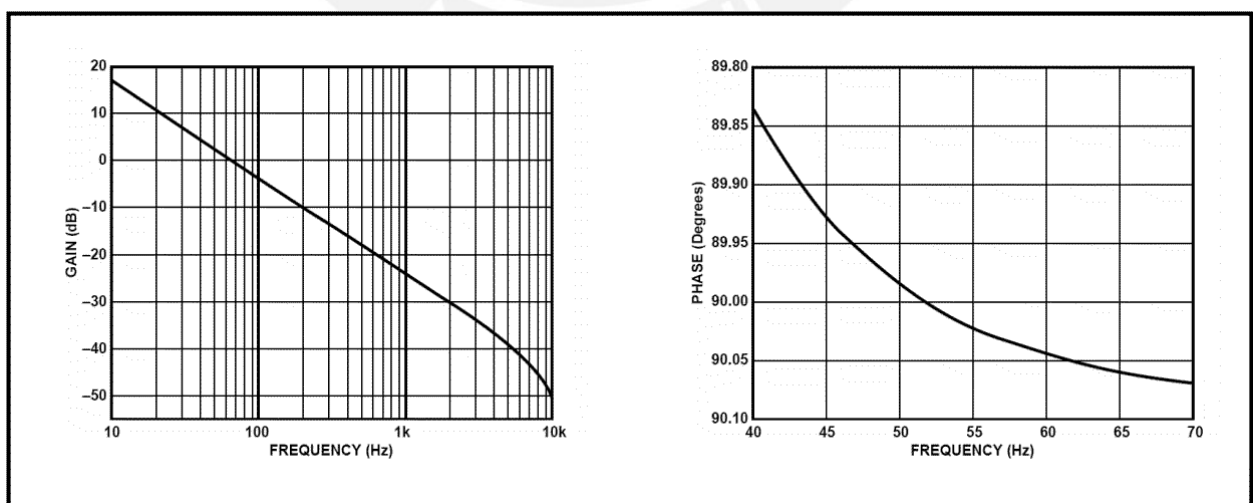


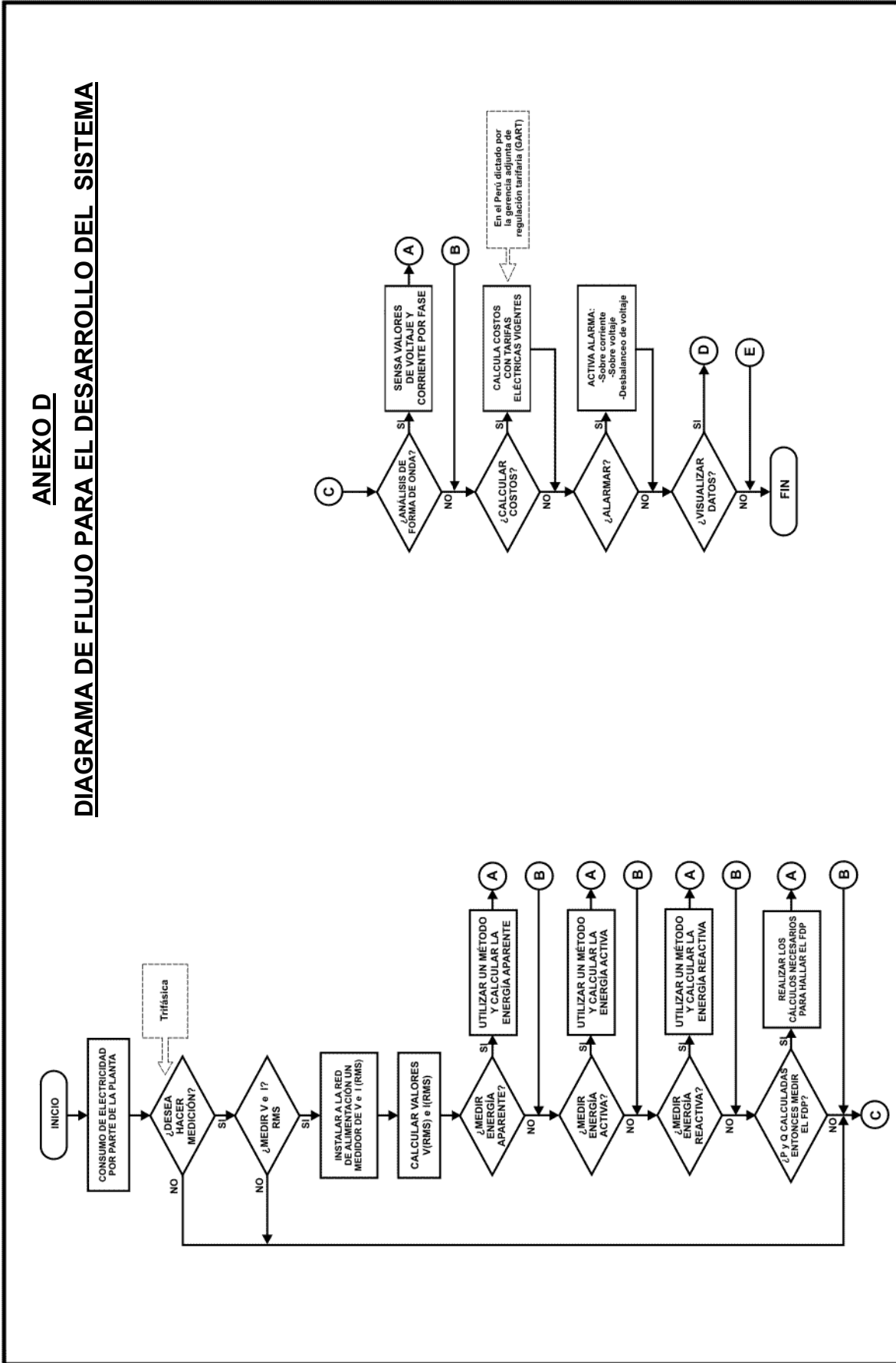
Figura: Respuesta de frecuencia y fase del integrador digital del ADE7758

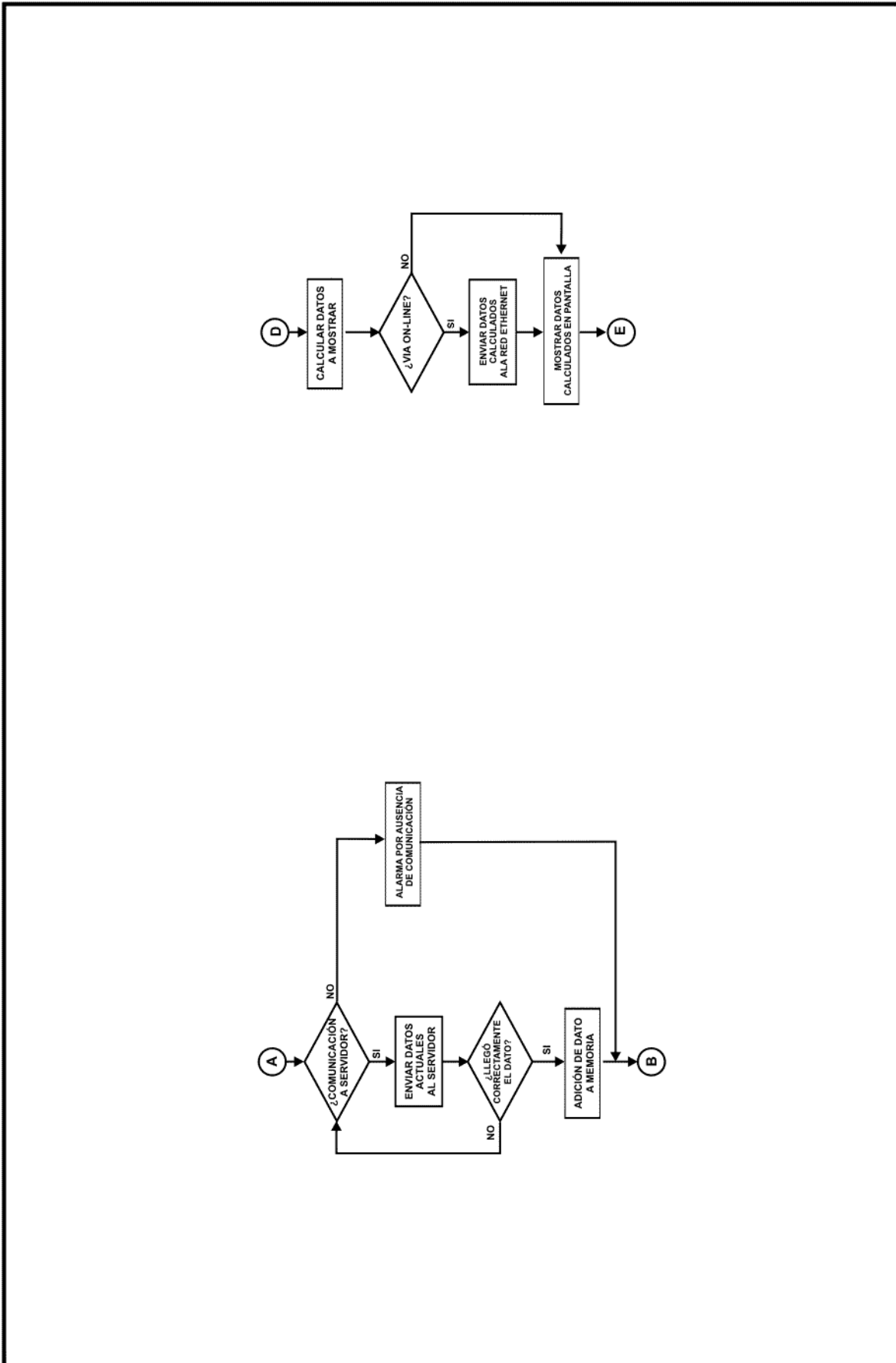
Como se puede ver, las respuestas de fase y magnitud del integrador digital son muy cercanas a lo ideal. El beneficio adicional de la implementación digital es la mayor estabilidad durante los cambios en el tiempo y fenómenos ambientales. Esto es muy importante en las aplicaciones de medición de energía dadas las condiciones de operación hostiles durante la larga vida operacional del medidor.

Haciendo un análisis de las tecnologías para la medición de corriente, se presenta el siguiente cuadro comparativo:

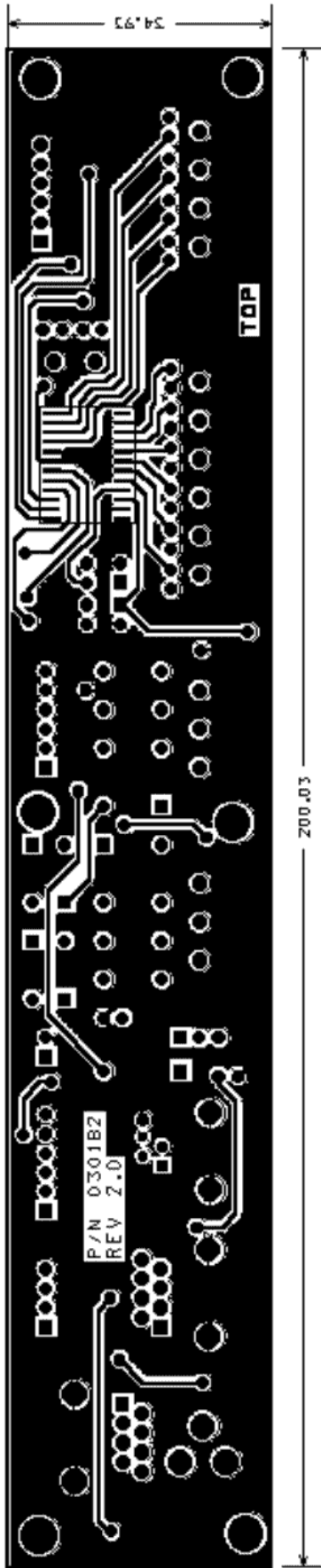
TECNOLOGIA DEL SENSOR	SHUNT DE CORRIENTE	TRANSFORMADOR DE CORRIENTE	SENSOR DE EFECTO HALL	BOBINA DE ROGOWSKI
Costo	Muy Bajo	Medio	Alto	Bajo
Linealidad en el rango de la medición	Muy Buena	Buena	Pobre	Muy Buena
Capacidad de medición de alta corriente	Muy Pobre	Buena	Buena	Muy Buena
Consumo de Potencia	Alto	Bajo	Medio	Bajo
Problema de Saturación de Corriente DC	No	Si	Si	No
Variación de la Salida con respecto a la Temperatura	Medio	Bajo	Alto	Muy Bajo
Problema Offset de DC	Si	No	Si	No
Problema de saturación e histéresis	No	Si	Si	No

**ANEXO D**  
**DIAGRAMA DE FLUJO PARA EL DESARROLLO DEL SISTEMA**

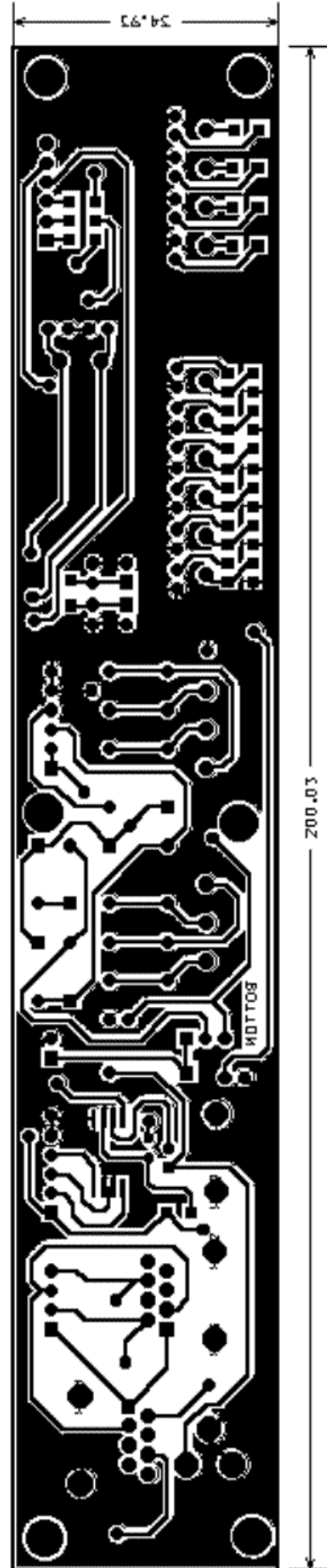




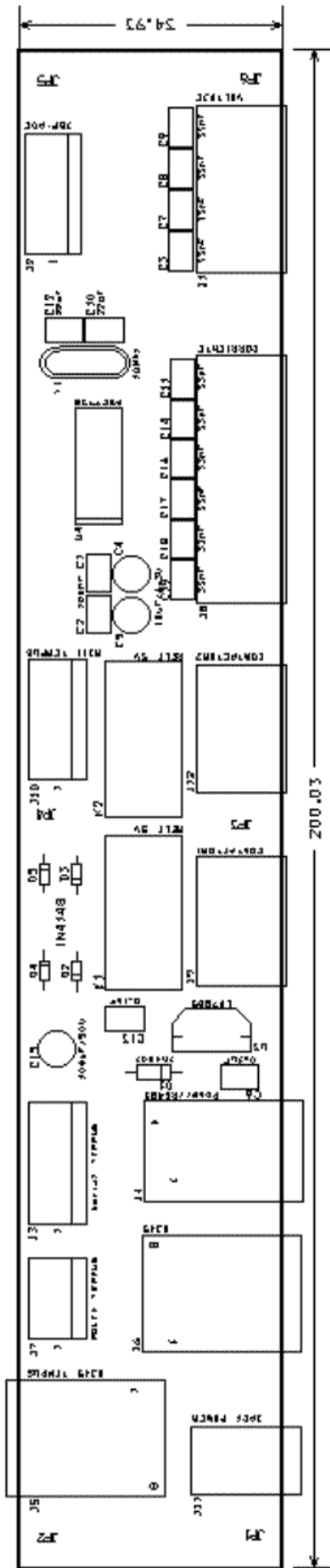




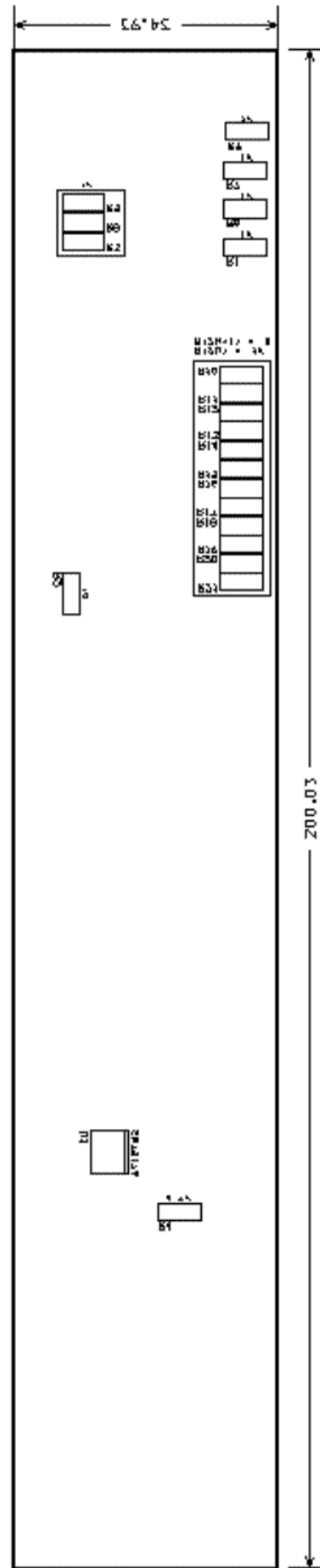
ROUTEADO DEL MÓDULO DEL SISTEMA – VISTA DE PISTAS EN TOP  
(DESARROLLADO EN ORCAD RELEASE 9.1 – LAYOUT)



ROUTEADO DEL MÓDULO DEL SISTEMA – VISTA DE PISTAS EN BOTTOM  
(DESARROLLADO EN ORCAD RELEASE 9.1 – LAYOUT)



ROUTEADO DEL MÓDULO DEL SISTEMA – VISTA DE COMPONENTES EN TOP  
(DESARROLLADO EN ORCAD RELEASE 9.1 – LAYOUT)



ROUTEADO DEL MÓDULO DEL SISTEMA – VISTA DE COMPONENTES EN BOTTOM  
(DESARROLLADO EN ORCAD RELEASE 9.1 – LAYOUT)

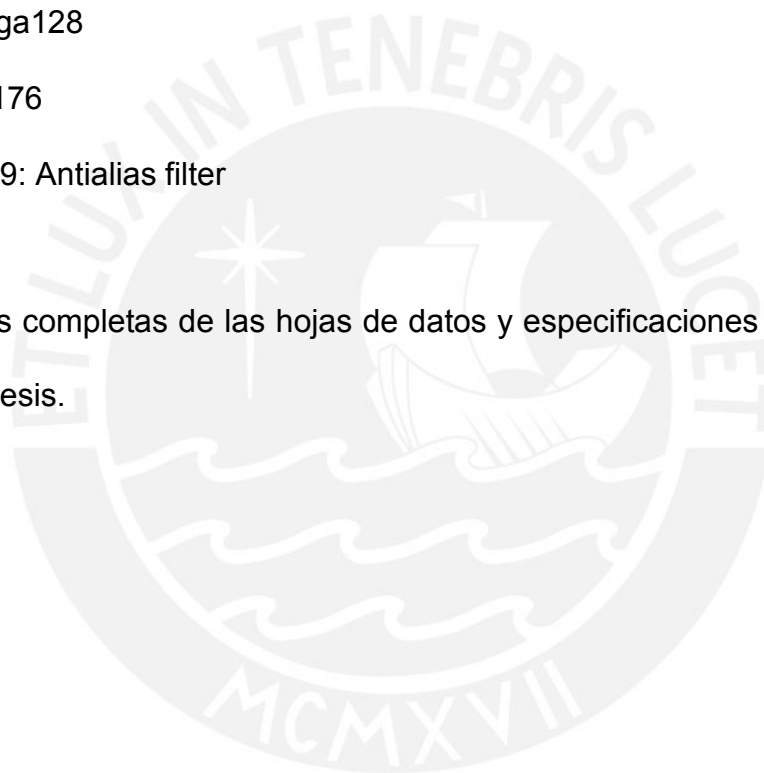
## ANEXO F

### HOJAS TÉCNICAS

En esta sección se presentan los resúmenes y páginas más importantes de las hojas técnicas de los siguientes dispositivos y documentos:

- ADE7758
- ATmega128
- SN75176
- AN-559: Antialias filter

Las versiones completas de las hojas de datos y especificaciones se encuentran en el CD de tesis.



## FUENTES

- [1] MINISTERIO DE ENERGÍA Y MINAS – PERU  
2005 – Compendio de normas del sub-sector electricidad  
<http://www.minem.gob.pe/electricidad/index.asp>
- [2] The ABB Group  
2001 October – ODIN Meter An electricity energy meter from ABB: Technical documentation  
[http://www.abb.nl/GLOBAL/NLABB/NLABB032.NSF/viewunid/7209F451A8659515C1256B82004C3D80/\\$file/Odin+meter+\(E\).pdf](http://www.abb.nl/GLOBAL/NLABB/NLABB032.NSF/viewunid/7209F451A8659515C1256B82004C3D80/$file/Odin+meter+(E).pdf)  
[Consultado: 25/Oct/2005]
- [3] KARCZ, ANDRES M.  
1977 – Fundamentos de metrología electrónica – Tomo III: Potencia y energía  
Ediciones Técnicas Marcombo S.A., Boixareu editores. Barcelona – España.
- [4] KINNARD, ISAAC F.  
1958 – Medidas eléctricas y sus aplicaciones  
Ediciones Técnicas Marcombo S.A. – Barcelona, España
- [5] KARSA, BÉLA E.  
1967 – Electrical measuring instruments and measurements  
Ed. Akadémiai Kiadó & Villamos mérőműszerek és mérések. Budapest - Hungary

- [6] Instituto Nacional de Defensa de la Competencia y de la Protección de la Propiedad Intelectual – INDECOPI  
2005 – Servicio Nacional de Metrología – Metrología y calibración  
<http://www.indecopi.gob.pe/nuestrosservicios/metrologiaycalibracion>  
[Consultado: 27/Oct/2005]
- [7] EL PERUANO (diario oficial)  
2001 – Ministerio de energía y minas. Dirección general de Electricidad.  
Código nacional de electricidad suministro 2001.  
Resolución Ministerial N° 366-2001-EM/VME  
[http://www.editoraperu.com.pe/normas/Pdfs/cod\\_nc\\_Elec.pdf](http://www.editoraperu.com.pe/normas/Pdfs/cod_nc_Elec.pdf)  
[Consultado: 27/Oct/2005]
- [8] Gobierno del Perú  
Ley N° 23560 - Sistema Legal de Unidades de Medida del Perú (SLUMP)  
Promulgado: 31-Dic-1982. Según Decreto Supremo N° 026-93-ITINCI  
[Vigente hasta el presente: 27/Oct/2005]
- [9] METERING INTERNATIONAL  
2002 – Magazine archive. Issue 1. Measuring reactive power in energy meters  
[http://www.metering.com/archive/021/52\\_1.htm](http://www.metering.com/archive/021/52_1.htm)  
[Consultado: 28/Oct/2005]
- [10] METERING INTERNATIONAL  
2003 – Magazine archive. Energy measurement ICs.  
[http://www.metering.com/archive/031/42\\_1.htm](http://www.metering.com/archive/031/42_1.htm)  
[Consultado: 28/Oct/2005]
- [11] GERENCIA ADJUNTA DE REGULACIÓN TARIFARIA (GART) – COMISIÓN DE TARIFAS ELÉCTRICAS  
1997 – Resolución de la comisión de tarifas eléctricas No. 024-97 P/CTE  
<http://www.cte.org.pe/resoluciones/pdf/RE024-1997.pdf>  
[Consultado: 04/Nov/2005]
- [12] Gobierno del Perú  
Decreto Supremo N° 016-2000-EM – Fijan horas de regulación y probabilidad de excedencia mensual de centrales hidráulicas, horas punta del sistema eléctrico y margen de reserva a que se refiere el Reglamento de la Ley de Concesiones Eléctricas. Incluye modificaciones según Decreto Supremo N° 032-2001-EM; Decreto Supremo N° 034-2001-EM y D.S. N° 055-2002-EM  
Artículo 2°  
Promulgado: 13-Sep-2000

- [13] Gobierno del Perú  
Decreto Supremo N° 027-2003-EM.- Fijan horas de punta del Sistema Eléctrico Interconectado  
Artículo 1°  
Promulgado: 06-Ago-2003
- [14] JUAN LUIS HERNÁNDEZ  
2004 – Factor de Potencia (FDP)  
<http://endrino.cnice.mecd.es/~jhem0027/fdp/fdp.htm>  
[Consultado: 28/Oct/2005]
- [15] CRISTOPHER E. STRANGIO  
2005 – The RS-232 standard  
CAMI Research Inc., Lexington, Massachusett. – USA.  
[http://www.camiresearch.com/Data\\_Com\\_Basics/RS232\\_standard.html](http://www.camiresearch.com/Data_Com_Basics/RS232_standard.html)
- [16] THE MATHWORKS – ACCELERATING THE PACE OF ENGINEERING AND SCIENCE  
2005 – Serial Port Interface Standard  
The MathWorks Inc. – USA.  
<http://www.mathworks.com/access/helpdesk/help/toolbox/instrument>  
[Consultado: 28/Oct/2005]
- [17] CISCO SYSTEMS INC.  
2005 - Ethernet Technologies documentation  
[http://www.cisco.com/univercd/cc/td/doc/cisintwk/ito\\_doc/ethernet.htm](http://www.cisco.com/univercd/cc/td/doc/cisintwk/ito_doc/ethernet.htm)  
[Consultado: 28/Oct/2005]
- [18] PROCOBRE  
Confiabilidad de Sistemas Eléctricos  
[http://www.procobreperu.org/c\\_confiabelec.pdf](http://www.procobreperu.org/c_confiabelec.pdf)  
[Consultado: 30/Oct/2005]
- [19] VIERA DE CARVALHO, ARNALDO; POVEDA, MANUEL; ZAK, JUAN  
1996 - OLADE : Diseño de Programas de Eficiencia energética.  
Revista Energética N°3, Septiembre-Diciembre 1996. Pag. 6 y 7
- [20] HANDHELD BASIC ++  
HB++, The best development enviroment for Palm Powered handhelds  
<http://www.handheld-basic.com/>  
[Consultado: 06/Jul/2006]

- [21] PALM ONE  
Welcome to palm  
<http://www.palm.com/>  
[Consultado: 06/Jul/2006]
- [22] TEMPUS  
Tempus  
<http://www.tempus.com.pe/>  
[Consultado: 06/Jul/2006]
- [23] INFARED DATA ASSOCIATION - IRDA  
International organization that creates and promotes interoperable, low cost  
infrared data interconnection  
[www.irda.org/](http://www.irda.org/)  
[Consultado: 06/Jul/2006]
- [24] LUIS ERNESTO BORGES  
Sistemas de lectura remota del consumo  
<http://neutron.ing.ucv.ve/>  
[Consultado: 13/Nov/2006]
- [25] ENERGY COMMISSION  
Energy Commission History  
<http://www.a2gov.org/PublicServices/SystemsPlanning/Energy/EnergyCommissionHistory.html>  
[Consultado: 16/Oct/2006]
- [26] THE WORLD BANK  
[www.worldbank.org](http://www.worldbank.org)  
Peru Data Profile  
<http://devdata.worldbank.org/external/CPProfile.asp?SelectedCountry=PER&CODE=PER&CNAME=Peru&PTYPE=CP>  
[Consultado: 12/Ene/2007]



### FEATURES

- Highly accurate; supports IEC 60687, IEC 61036, IEC 61268, IEC 62053-21, IEC 62053-22, and IEC 62053-23
- Compatible with 3-phase/3-wire, 3-phase/4-wire, and other 3-phase services
- Less than 0.1% active energy error over a dynamic range of 1000 to 1 at 25°C
- Supplies active/reactive/apparent energy, voltage rms, current rms, and sampled waveform data
- Two pulse outputs, one for active power and the other selectable between reactive and apparent power with programmable frequency
- Digital power, phase, and rms offset calibration
- On-chip, user-programmable thresholds for line voltage SAG and overvoltage detections
- An on-chip, digital integrator enables direct interface-to-current sensors with di/dt output
- A PGA in the current channel allows direct interface to shunts and current transformers
- An SPI<sup>®</sup>-compatible serial interface with  $\overline{IRQ}$
- Proprietary ADCs and DSP provide high accuracy over large variations in environmental conditions and time
- Reference 2.4 V (drift 30 ppm/°C typical) with external overdrive capability
- Single 5 V supply, low power (70 mW typical)

### GENERAL DESCRIPTION

The ADE7758<sup>1</sup> is a high accuracy, 3-phase electrical energy measurement IC with a serial interface and two pulse outputs. The ADE7758 incorporates second-order  $\Sigma$ - $\Delta$  ADCs, a digital integrator, reference circuitry, a temperature sensor, and all the signal processing required to perform active, reactive, and apparent energy measurement and rms calculations.

The ADE7758 is suitable to measure active, reactive, and apparent energy in various 3-phase configurations, such as WYE or DELTA services, with both three and four wires. The ADE7758 provides system calibration features for each phase, that is, rms offset correction, phase calibration, and power calibration. The APCF logic output gives active power information, and the VARCF logic output provides instantaneous reactive or apparent power information (*continued on Page 4*).

<sup>1</sup> U.S. patents pending.

### FUNCTIONAL BLOCK DIAGRAM

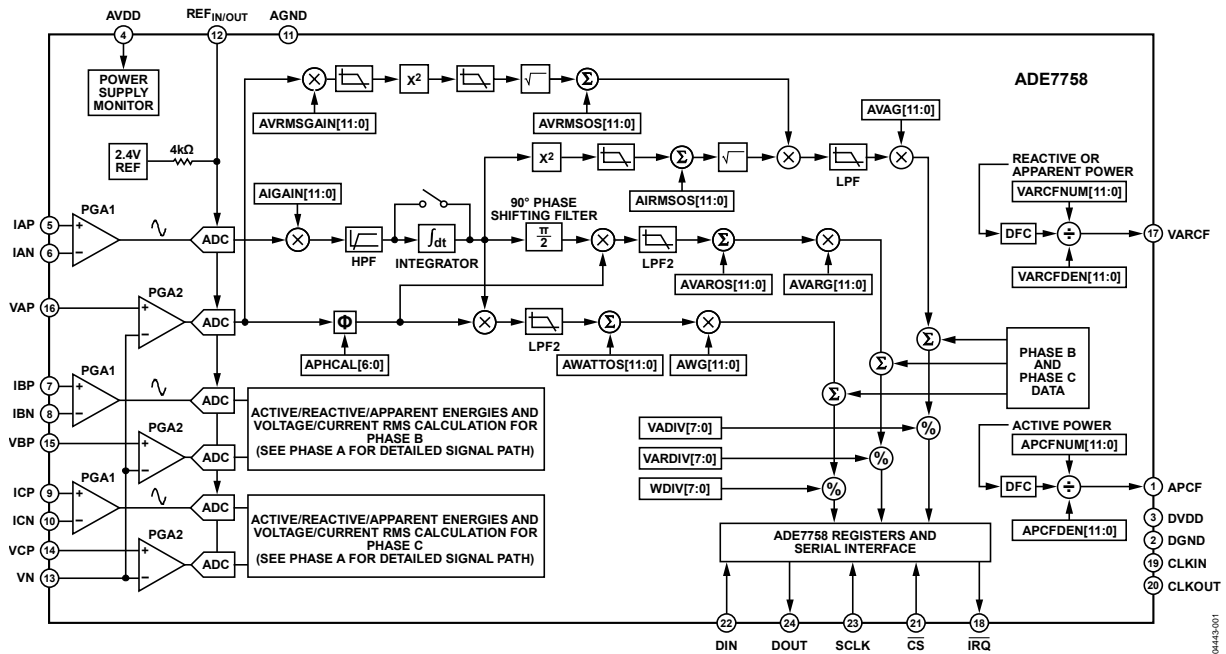


Figure 1.

### Rev. C

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**1/04—Revision 0: Initial Version**

## GENERAL DESCRIPTION

*(continued from Page 1)* The ADE7758 has a waveform sample register that allows access to the ADC outputs. The part also incorporates a detection circuit for short duration low or high voltage variations. The voltage threshold levels and the duration (number of half-line cycles) of the variation are user programmable. A zero-crossing detection is synchronized with the zero-crossing point of the line voltage of any of the three phases. This information can be used to measure the period of any one of the three voltage inputs. The zero-crossing detection is used inside the chip for the line cycle energy accumulation mode. This mode permits faster and more accurate calibration by synchronizing the energy accumulation with an integer number of line cycles.

Data is read from the ADE7758 via the SPI serial interface. The interrupt request output ( $\overline{\text{IRQ}}$ ) is an open-drain, active low logic output. The  $\overline{\text{IRQ}}$  output goes active low when one or more interrupt events have occurred in the ADE7758. A status register indicates the nature of the interrupt. The ADE7758 is available in a 24-lead SOIC package.

## SPECIFICATIONS

AVDD = DVDD = 5 V  $\pm$  5%, AGND = DGND = 0 V, on-chip reference, CLKIN = 10 MHz XTAL, T<sub>MIN</sub> to T<sub>MAX</sub> = -40°C to +85°C.

Table 1.

Parameter <sup>1,2</sup>	Specification	Unit	Test Conditions/Comments
<b>ACCURACY</b>			
Active Energy Measurement Error (per Phase)	0.1	% typ	Over a dynamic range of 1000 to 1
Phase Error Between Channels			Line frequency = 45 Hz to 65 Hz, HPF on
PF = 0.8 Capacitive	$\pm 0.05$	°max	Phase lead 37°
PF = 0.5 Inductive	$\pm 0.05$	°max	Phase lag 60°
AC Power Supply Rejection			AVDD = DVDD = 5 V + 175 mV rms/120 Hz
Output Frequency Variation	0.01	% typ	V1P = V2P = V3P = 100 mV rms
DC Power Supply Rejection			AVDD = DVDD = 5 V $\pm$ 250 mV dc
Output Frequency Variation	0.01	% typ	V1P = V2P = V3P = 100 mV rms
Active Energy Measurement Bandwidth	14	kHz	
IRMS Measurement Error	0.5	% typ	Over a dynamic range of 500:1
IRMS Measurement Bandwidth	14	kHz	
VRMS Measurement Error	0.5	% typ	Over a dynamic range of 20:1
VRMS Measurement Bandwidth	260	Hz	
<b>ANALOG INPUTS</b>			
Maximum Signal Levels	$\pm 500$	mV max	See the Analog Inputs section
Input Impedance (DC)	380	k $\Omega$ min	Differential input
ADC Offset Error <sup>3</sup>	$\pm 30$	mV max	Uncalibrated error, see the Terminology section
Gain Error <sup>3</sup>	$\pm 6$	% typ	External 2.5 V reference
<b>WAVEFORM SAMPLING</b>			
Current Channels			Sampling CLKIN/128, 10 MHz/128 = 78.1 kSPS
Signal-to-Noise Plus Distortion	62	dB typ	See the Current Channel ADC section
Bandwidth (-3 dB)	14	kHz	
Voltage Channels			See the Voltage Channel ADC section
Signal-to-Noise Plus Distortion	62	dB typ	
Bandwidth (-3 dB)	260	Hz	
<b>REFERENCE INPUT</b>			
REF <sub>IN/OUT</sub> Input Voltage Range	2.6	V max	2.4 V + 8%
	2.2	V min	2.4 V - 8%
Input Capacitance	10	pF max	
<b>ON-CHIP REFERENCE</b>			
Reference Error	$\pm 200$	mV max	Nominal 2.4 V at REF <sub>IN/OUT</sub> pin
Current Source	6	$\mu$ A max	
Output Impedance	4	k $\Omega$ min	
Temperature Coefficient	30	ppm/°C typ	
<b>CLKIN</b>			
Input Clock Frequency	15	MHz max	All specifications CLKIN of 10 MHz
	5	MHz min	
<b>LOGIC INPUTS</b>			
DIN, SCLK, CLKIN, and $\overline{CS}$			
Input High Voltage, V <sub>INH</sub>	2.4	V min	DVDD = 5 V $\pm$ 5%
Input Low Voltage, V <sub>INL</sub>	0.8	V max	DVDD = 5 V $\pm$ 5%
Input Current, I <sub>IN</sub>	$\pm 3$	$\mu$ A max	Typical 10 nA, V <sub>IN</sub> = 0 V to DVDD
Input Capacitance, C <sub>IN</sub>	10	pF max	

# ADE7758

Parameter <sup>1,2</sup>	Specification	Unit	Test Conditions/Comments
<b>LOGIC OUTPUTS</b>			
$\overline{\text{IRQ}}$ , DOUT, and CLKOUT			DVDD = 5 V ± 5% $\overline{\text{IRQ}}$ is open-drain, 10 kΩ pull-up resistor
Output High Voltage, V <sub>OH</sub>	4	V min	I <sub>SOURCE</sub> = 5 mA
Output Low Voltage, V <sub>OL</sub>	0.4	V max	I <sub>SINK</sub> = 1 mA
<b>APCF and VARCF</b>			
Output High Voltage, V <sub>OH</sub>	4	V min	I <sub>SOURCE</sub> = 8 mA
Output Low Voltage, V <sub>OL</sub>	1	V max	I <sub>SINK</sub> = 5 mA
<b>POWER SUPPLY</b>			
AVDD	4.75	V min	For specified performance 5 V – 5%
	5.25	V max	5 V + 5%
DVDD	4.75	V min	5 V – 5%
	5.25	V max	5 V + 5%
A <sub>IDD</sub>	8	mA max	Typically 5 mA
D <sub>IDD</sub>	13	mA max	Typically 9 mA

<sup>1</sup> See the Typical Performance Characteristics.

<sup>2</sup> See the Terminology section for a definition of the parameters.

<sup>3</sup> See the Analog Inputs section.

## TIMING CHARACTERISTICS

AVDD = DVDD = 5 V ± 5%, AGND = DGND = 0 V, on-chip reference, CLKIN = 10 MHz XTAL, T<sub>MIN</sub> to T<sub>MAX</sub> = –40°C to +85°C.

Table 2.

Parameter <sup>1,2</sup>	Specification	Unit	Test Conditions/Comments
<b>WRITE TIMING</b>			
t <sub>1</sub>	50	ns (min)	$\overline{\text{CS}}$ falling edge to first SCLK falling edge
t <sub>2</sub>	50	ns (min)	SCLK logic high pulse width
t <sub>3</sub>	50	ns (min)	SCLK logic low pulse width
t <sub>4</sub>	10	ns (min)	Valid data setup time before falling edge of SCLK
t <sub>5</sub>	5	ns (min)	Data hold time after SCLK falling edge
t <sub>6</sub>	900	ns (min)	Minimum time between the end of data byte transfers
t <sub>7</sub>	50	ns (min)	Minimum time between byte transfers during a serial write
t <sub>8</sub>	100	ns (min)	$\overline{\text{CS}}$ hold time after SCLK falling edge
<b>READ TIMING</b>			
t <sub>9</sub> <sup>3</sup>	4	μs (min)	Minimum time between read command (that is, a write to communication register) and data read
t <sub>10</sub>	50	ns (min)	Minimum time between data byte transfers during a multibyte read
t <sub>11</sub> <sup>4</sup>	30	ns (min)	Data access time after SCLK rising edge following a write to the communications register
t <sub>12</sub> <sup>5</sup>	100	ns (max)	Bus relinquish time after falling edge of SCLK
	10	ns (min)	
t <sub>13</sub> <sup>5</sup>	100	ns (max)	Bus relinquish time after rising edge of $\overline{\text{CS}}$
	10	ns (min)	

<sup>1</sup> Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are specified with tr = tf = 5 ns (10% to 90%) and timed from a voltage level of 1.6 V.

<sup>2</sup> See the timing diagrams in Figure 3 and Figure 4 and the Serial Interface section.

<sup>3</sup> Minimum time between read command and data read for all registers except waveform register, which is t<sub>9</sub> = 500 ns min.

<sup>4</sup> Measured with the load circuit in Figure 2 and defined as the time required for the output to cross 0.8 V or 2.4 V.

<sup>5</sup> Derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time quoted here is the true bus relinquish time of the part and is independent of the bus loading.

# TIMING DIAGRAMS

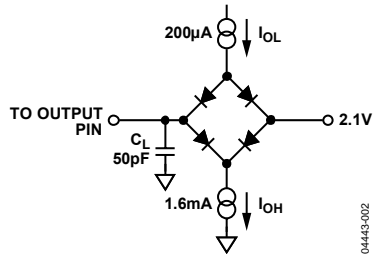


Figure 2. Load Circuit for Timing Specifications

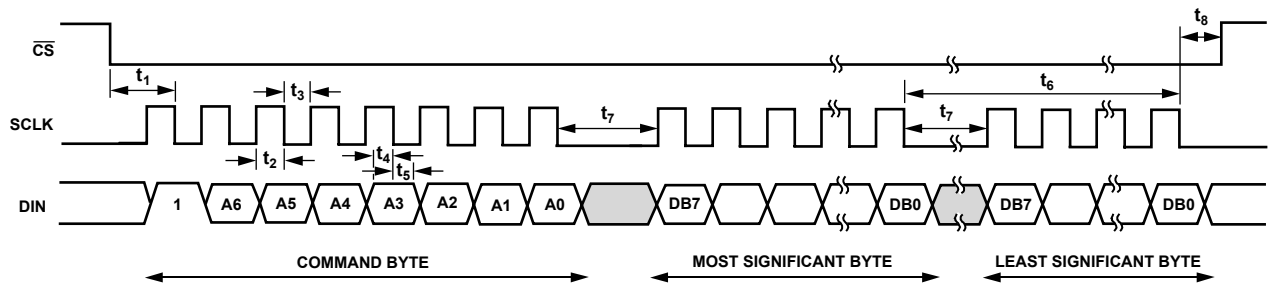


Figure 3. Serial Write Timing

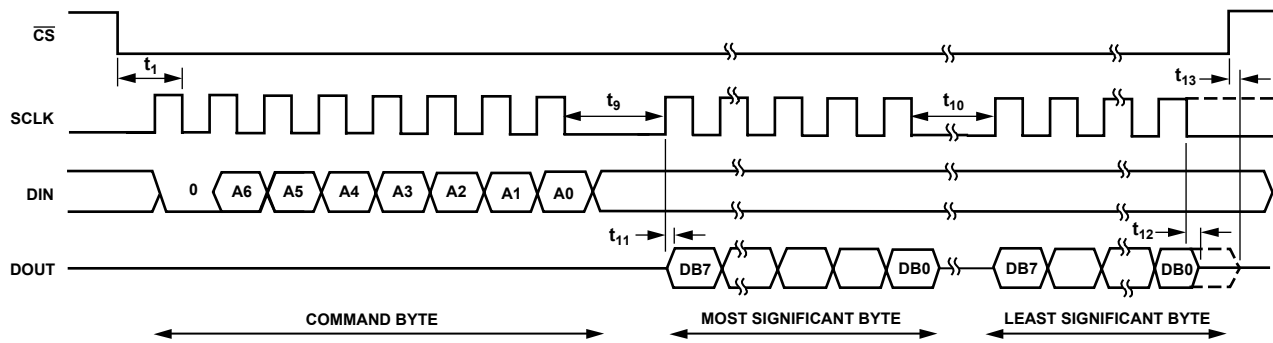


Figure 4. Serial Read Timing

## ABSOLUTE MAXIMUM RATINGS

T<sub>A</sub> = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AVDD to AGND	-0.3 V to +7 V
DVDD to DGND	-0.3 V to +7 V
DVDD to AVDD	-0.3 V to +0.3 V
Analog Input Voltage to AGND, IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, VCP, VN	-6 V to +6 V
Reference Input Voltage to AGND	-0.3 V to AVDD + 0.3 V
Digital Input Voltage to DGND	-0.3 V to DVDD + 0.3 V
Digital Output Voltage to DGND	-0.3 V to DVDD + 0.3 V
Operating Temperature	
Industrial Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
24-Lead SOIC, Power Dissipation	88 mW
$\theta_{JA}$ Thermal Impedance	53°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

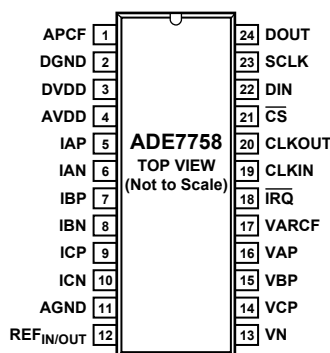


Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	APCF	Active Power Calibration Frequency (APCF) Logic Output. It provides active power information. This output is used for operational and calibration purposes. The full-scale output frequency can be scaled by writing to the APCFNUM and APCFDEN registers (see the Active Power Frequency Output section).
2	DGND	This provides the ground reference for the digital circuitry in the ADE7758, that is, the multiplier, filters, and digital-to-frequency converter. Because the digital return currents in the ADE7758 are small, it is acceptable to connect this pin to the analog ground plane of the whole system. However, high bus capacitance on the DOUT pin can result in noisy digital current that could affect performance.
3	DVDD	Digital Power Supply. This pin provides the supply voltage for the digital circuitry in the ADE7758. The supply voltage should be maintained at $5\text{ V} \pm 5\%$ for specified operation. This pin should be decoupled to DGND with a $10\ \mu\text{F}$ capacitor in parallel with a ceramic $100\ \text{nF}$ capacitor.
4	AVDD	Analog Power Supply. This pin provides the supply voltage for the analog circuitry in the ADE7758. The supply should be maintained at $5\text{ V} \pm 5\%$ for specified operation. Every effort should be made to minimize power supply ripple and noise at this pin by the use of proper decoupling. The Typical Performance Characteristics show the power supply rejection performance. This pin should be decoupled to AGND with a $10\ \mu\text{F}$ capacitor in parallel with a ceramic $100\ \text{nF}$ capacitor.
5, 6, 7, 8, 9, 10	IAP, IAN, IBP, IBN, ICP, ICN	Analog Inputs for Current Channel. This channel is used with the current transducer and is referenced in this document as the current channel. These inputs are fully differential voltage inputs with maximum differential input signal levels of $\pm 0.5\text{ V}$ , $\pm 0.25\text{ V}$ , and $\pm 0.125\text{ V}$ , depending on the gain selections of the internal PGA (see the Analog Inputs section). All inputs have internal ESD protection circuitry. In addition, an overvoltage of $\pm 6\text{ V}$ can be sustained on these inputs without risk of permanent damage.
11	AGND	This pin provides the ground reference for the analog circuitry in the ADE7758, that is, ADCs, temperature sensor, and reference. This pin should be tied to the analog ground plane or the quietest ground reference in the system. This quiet ground reference should be used for all analog circuitry, for example, antialiasing filters, current, and voltage transducers. To keep ground noise around the ADE7758 to a minimum, the quiet ground plane should be connected to the digital ground plane at only one point. It is acceptable to place the entire device on the analog ground plane.
12	REF <sub>IN/OUT</sub>	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of $2.4\text{ V} \pm 8\%$ and a typical temperature coefficient of $30\ \text{ppm}/^\circ\text{C}$ . An external reference source can also be connected at this pin. In either case, this pin should be decoupled to AGND with a $1\ \mu\text{F}$ ceramic capacitor.
13, 14, 15, 16	VN, VCP, VBP, VAP	Analog Inputs for the Voltage Channel. This channel is used with the voltage transducer and is referenced as the voltage channels in this document. These inputs are single-ended voltage inputs with the maximum signal level of $\pm 0.5\text{ V}$ with respect to VN for specified operation. These inputs are voltage inputs with maximum input signal levels of $\pm 0.5\text{ V}$ , $\pm 0.25\text{ V}$ , and $\pm 0.125\text{ V}$ , depending on the gain selections of the internal PGA (see the Analog Inputs section). All inputs have internal ESD protection circuitry, and in addition, an overvoltage of $\pm 6\text{ V}$ can be sustained on these inputs without risk of permanent damage.

# ADE7758

Pin No.	Mnemonic	Description
17	VARCF	Reactive Power Calibration Frequency Logic Output. It gives reactive power or apparent power information depending on the setting of the VACF bit of the WAVMODE register. This output is used for operational and calibration purposes. The full-scale output frequency can be scaled by writing to the VARCFNUM and VARCFDEN registers (see the Reactive Power Frequency Output section).
18	$\overline{\text{IRQ}}$	Interrupt Request Output. This is an active low open-drain logic output. Maskable interrupts include: an active energy register at half level, an apparent energy register at half level, and waveform sampling up to 26 kSPS (see the Interrupts section).
19	CLKIN	Master Clock for ADCs and Digital Signal Processing. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7758. The clock frequency for specified operation is 10 MHz. Ceramic load capacitors of a few tens of picofarad should be used with the gate oscillator circuit. Refer to the crystal manufacturer's data sheet for the load capacitance requirements
20	CLKOUT	A crystal can be connected across this pin and CLKIN as previously described to provide a clock source for the ADE7758. The CLKOUT pin can drive one CMOS load when either an external clock is supplied at CLKIN or a crystal is being used.
21	$\overline{\text{CS}}$	Chip Select. Part of the 4-wire serial interface. This active low logic input allows the ADE7758 to share the serial bus with several other devices (see the Serial Interface section).
22	DIN	Data Input for the Serial Interface. Data is shifted in at this pin on the falling edge of SCLK (see the Serial Interface section).
23	SCLK	Serial Clock Input for the Synchronous Serial Interface. All serial data transfers are synchronized to this clock (see the Serial Interface section). The SCLK has a Schmidt-trigger input for use with a clock source that has a slow edge transition time, for example, opto-isolator outputs.
24	DOUT	Data Output for the Serial Interface. Data is shifted out at this pin on the rising edge of SCLK. This logic output is normally in a high impedance state, unless it is driving data onto the serial data bus (see the Serial Interface section).

## TERMINOLOGY

### Measurement Error

The error associated with the energy measurement made by the ADE7758 is defined by

$$\text{Measurement Error} = \frac{\text{Energy Registered by ADE7758} - \text{True Energy}}{\text{True Energy}} \times 100\% \quad (1)$$

### Phase Error Between Channels

The high-pass filter (HPF) and digital integrator introduce a slight phase mismatch between the current and the voltage channel. The all-digital design ensures that the phase matching between the current channels and voltage channels in all three phases is within  $\pm 0.1^\circ$  over a range of 45 Hz to 65 Hz and  $\pm 0.2^\circ$  over a range of 40 Hz to 1 kHz. This internal phase mismatch can be combined with the external phase error (from current sensor or component tolerance) and calibrated with the phase calibration registers.

### Power Supply Rejection (PSR)

This quantifies the ADE7758 measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (5 V) is taken. A second reading is obtained with the same input signal levels when an ac signal (175 mV rms/100 Hz) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading—see the Measurement Error definition.

For the dc PSR measurement, a reading at nominal supplies (5 V) is taken. A second reading is obtained with the same input signal levels when the power supplies are varied  $\pm 5\%$ . Any error introduced is again expressed as a percentage of the reading.

### ADC Offset Error

This refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND that the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection (see the Typical Performance Characteristics section). However, when HPFs are switched on, the offset is removed from the current channels and the power calculation is not affected by this offset.

### Gain Error

The gain error in the ADCs of the ADE7758 is defined as the difference between the measured ADC output code (minus the offset) and the ideal output code (see the Current Channel ADC section and the Voltage Channel ADC section). The difference is expressed as a percentage of the ideal code.

### Gain Error Match

The gain error match is defined as the gain error (minus the offset) obtained when switching between a gain of 1, 2, or 4. It is expressed as a percentage of the output ADC code obtained under a gain of 1.

TYPICAL PERFORMANCE CHARACTERISTICS

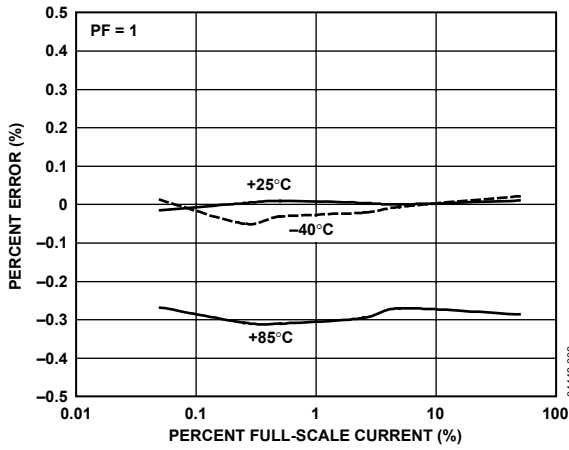


Figure 6. Active Energy Error as a Percentage of Reading (Gain = +1) over Temperature with Internal Reference and Integrator Off

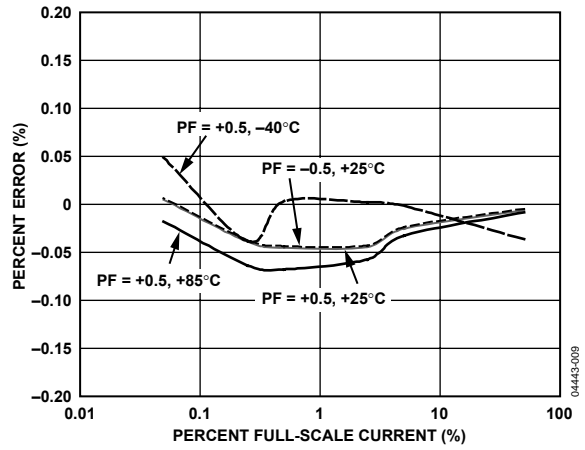


Figure 9. Active Energy Error as a Percentage of Reading (Gain = +1) over Temperature with External Reference and Integrator Off

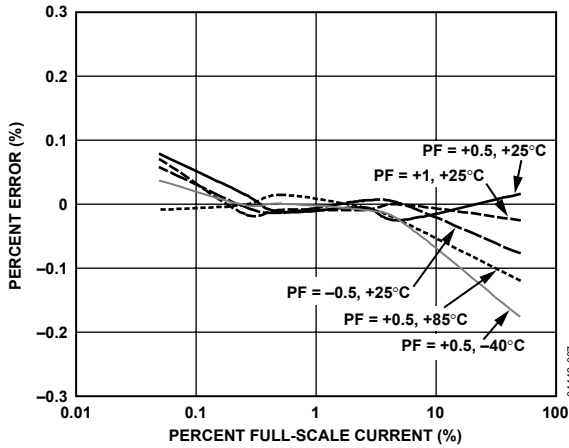


Figure 7. Active Energy Error as a Percentage of Reading (Gain = +1) over Power Factor with Internal Reference and Integrator Off

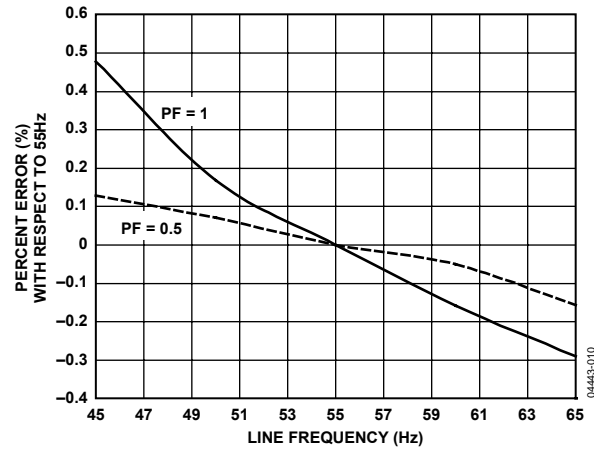


Figure 10. Active Energy Error as a Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off

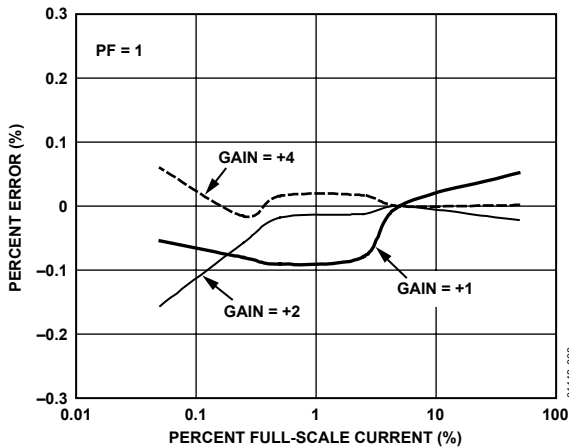


Figure 8. Active Energy Error as a Percentage of Reading over Gain with Internal Reference and Integrator Off

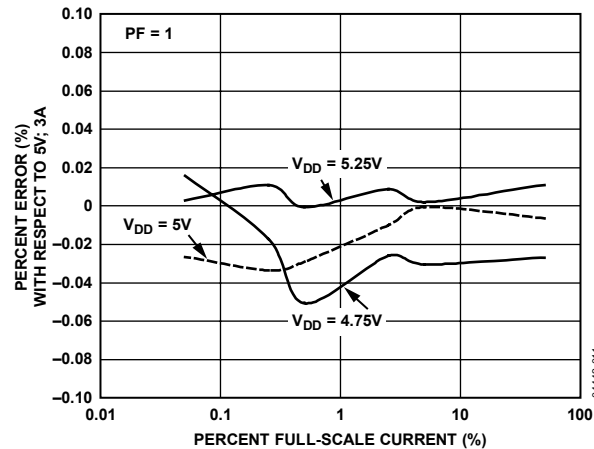


Figure 11. Active Energy Error as a Percentage of Reading (Gain = +1) over Power Supply with Internal Reference and Integrator Off

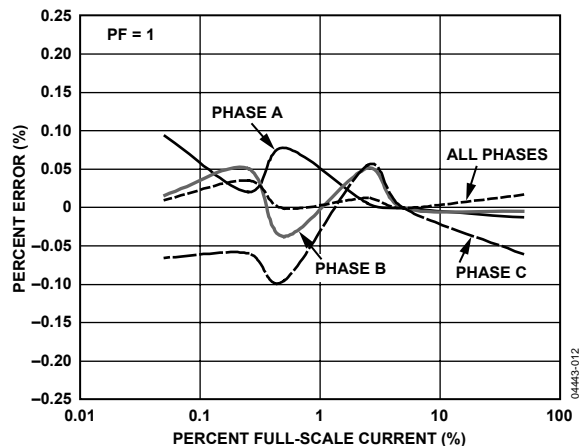


Figure 12. ACF Error as a Percentage of Reading (Gain = +1) with Internal Reference and Integrator Off

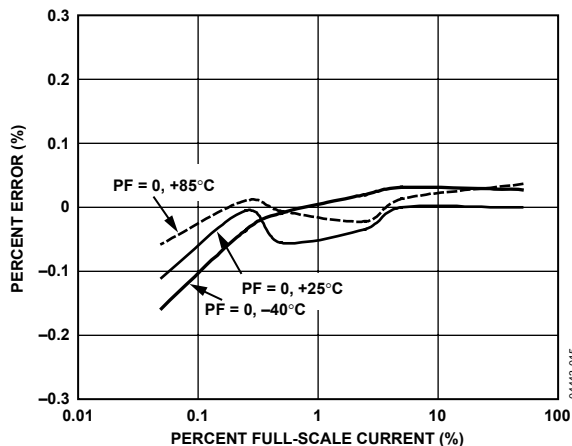


Figure 15. Reactive Energy Error as a Percentage of Reading (Gain = +1) over Temperature with External Reference and Integrator Off

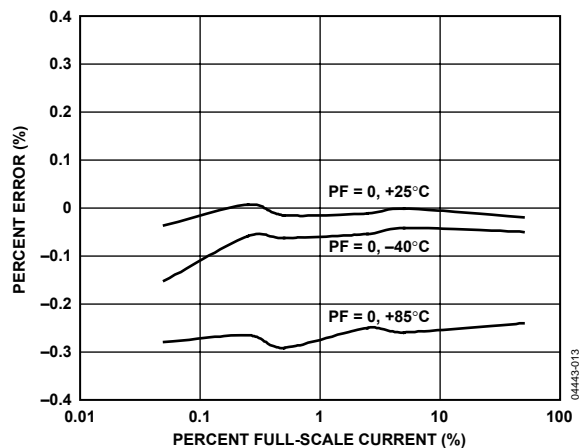


Figure 13. Reactive Energy Error as a Percentage of Reading (Gain = +1) over Temperature with Internal Reference and Integrator Off

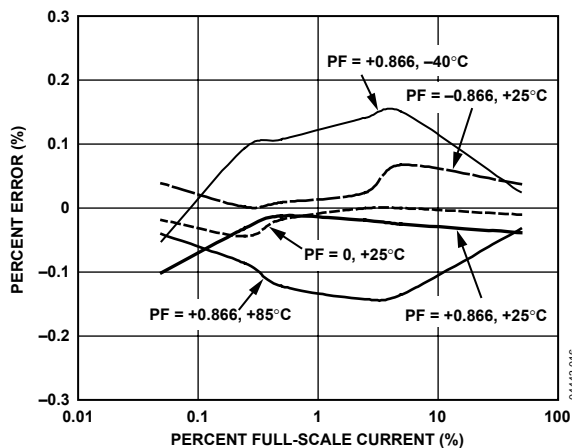


Figure 16. Reactive Energy Error as a Percentage of Reading (Gain = +1) over Power Factor with External Reference and Integrator Off

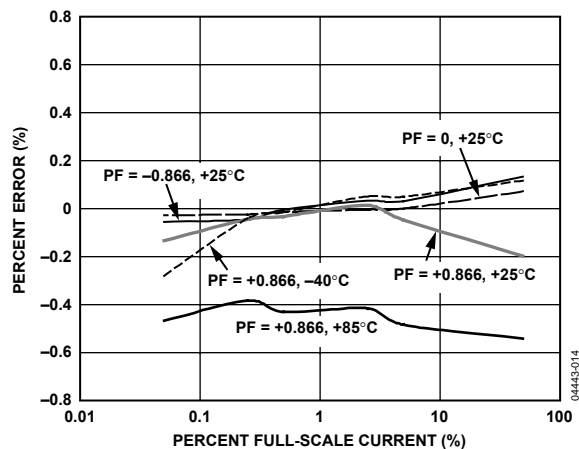


Figure 14. Reactive Energy Error as a Percentage of Reading (Gain = +1) over Power Factor with Internal Reference and Integrator Off

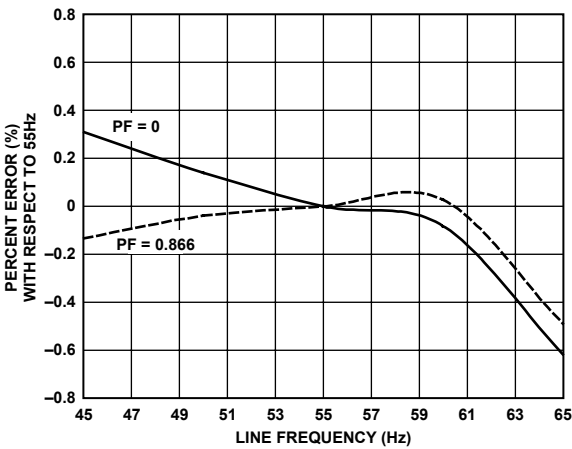


Figure 17. Reactive Energy Error as a Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off

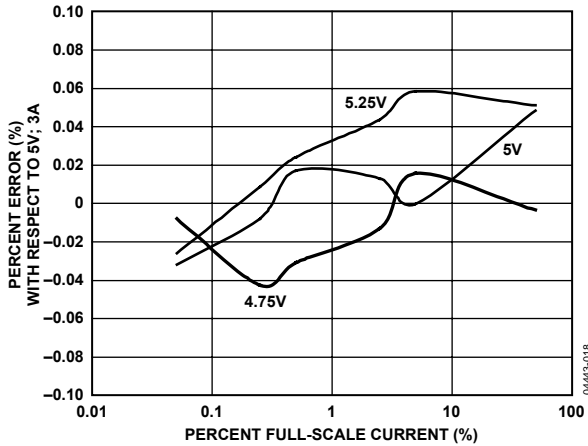


Figure 18. Reactive Energy Error as a Percentage of Reading (Gain = +1) over Supply with Internal Reference and Integrator Off

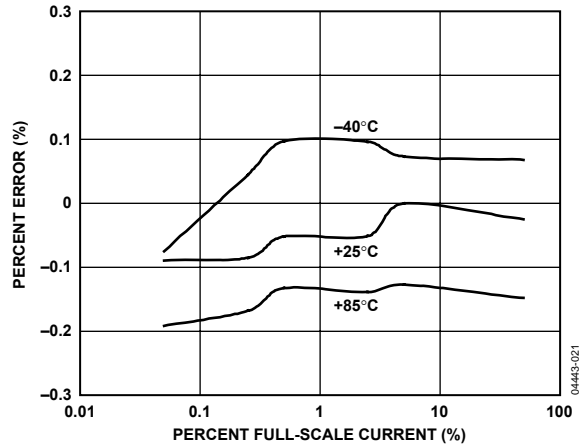


Figure 21. Active Energy Error as a Percentage of Reading (Gain = +4) over Temperature with Internal Reference and Integrator On

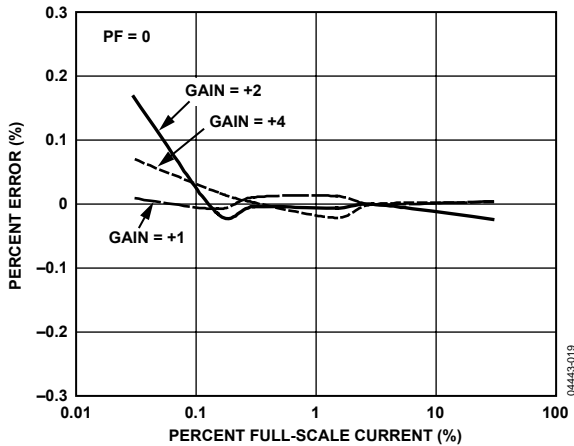


Figure 19. Reactive Energy Error as a Percentage of Reading over Gain with Internal Reference and Integrator Off

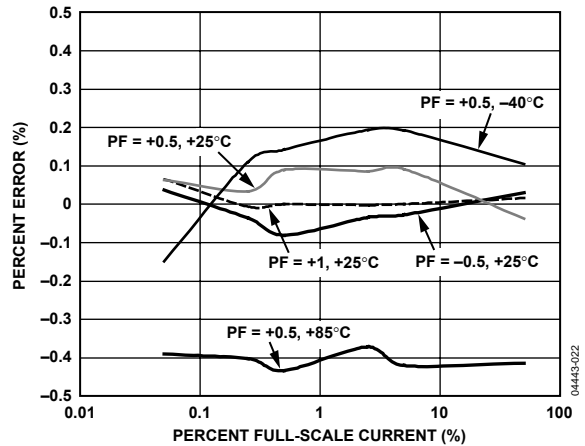


Figure 22. Active Energy Error as a Percentage of Reading (Gain = +4) over Power Factor with Internal Reference and Integrator On

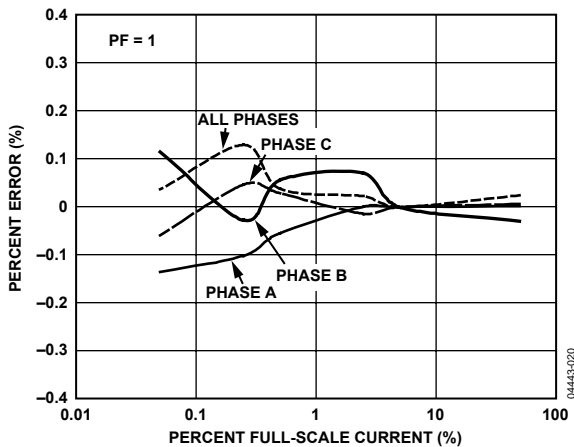


Figure 20. VARCF Error as a Percentage of Reading (Gain = +1) with Internal Reference and Integrator Off

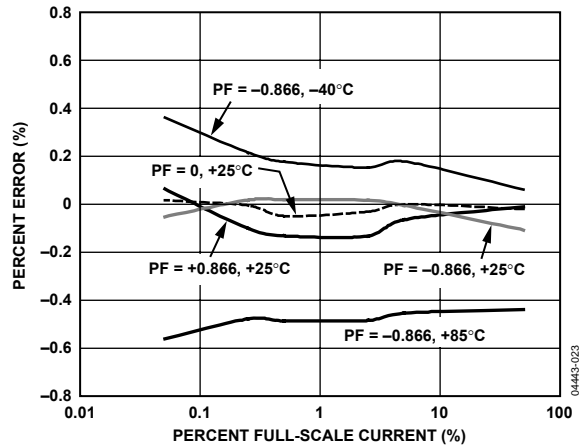


Figure 23. Reactive Energy Error as a Percentage of Reading (Gain = +4) over Power Factor with Internal Reference and Integrator On

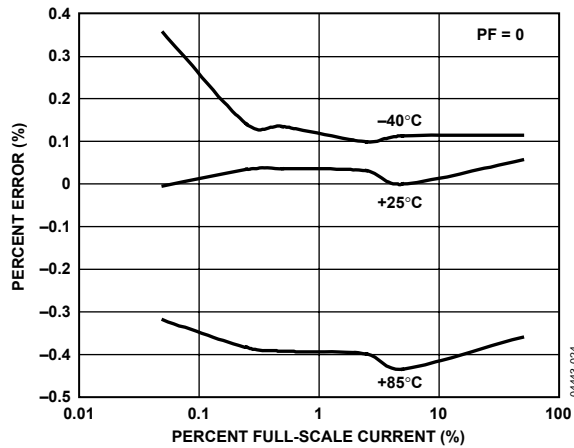


Figure 24. Reactive Energy Error as a Percentage of Reading (Gain = +4) over Temperature with Internal Reference and Integrator On

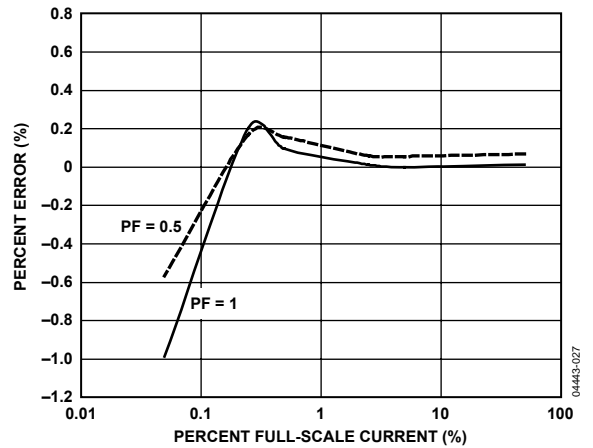


Figure 27. IRMS Error as a Percentage of Reading (Gain = +1) with Internal Reference and Integrator Off

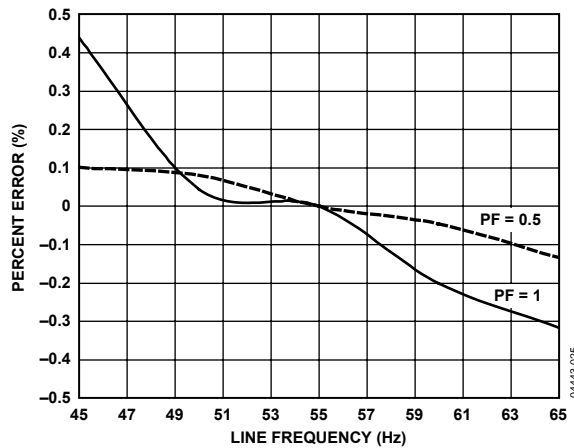


Figure 25. Active Energy Error as a Percentage of Reading (Gain = +4) over Frequency with Internal Reference and Integrator On

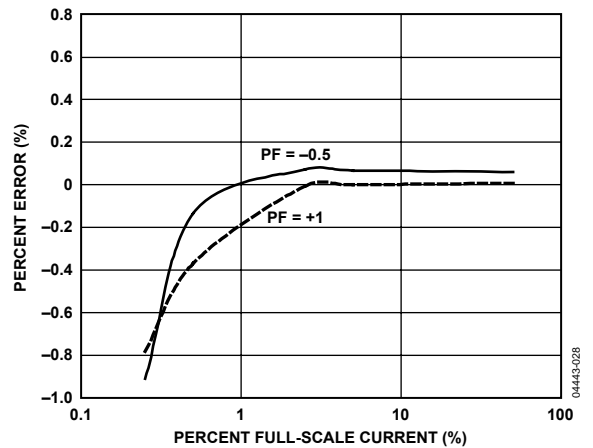


Figure 28. IRMS Error as a Percentage of Reading (Gain = +4) with Internal Reference and Integrator On

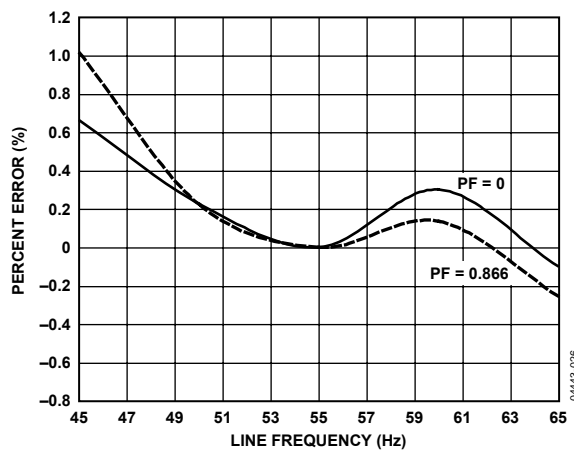


Figure 26. Reactive Energy Error as a Percentage of Reading (Gain = +4) over Frequency with Internal Reference and Integrator On

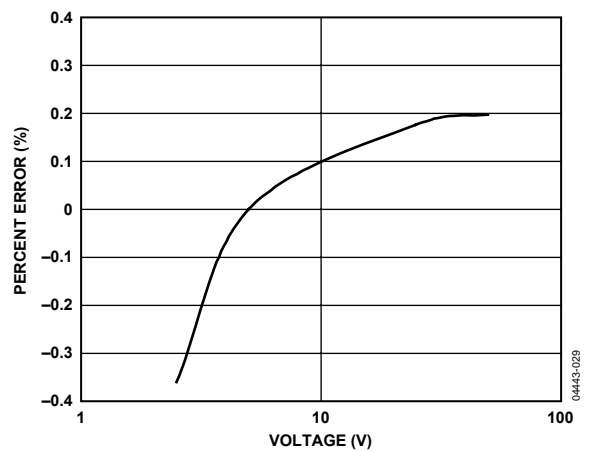


Figure 29. VRMS Error as a Percentage of Reading (Gain = +1) with Internal Reference

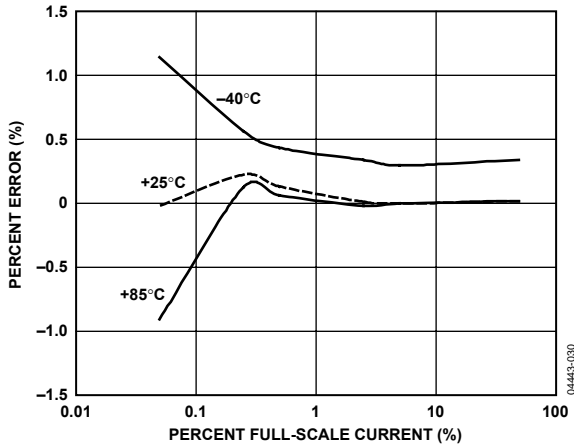


Figure 30. Apparent Energy Error as a Percentage of Reading (Gain = +1) over Temperature with Internal Reference and Integrator Off

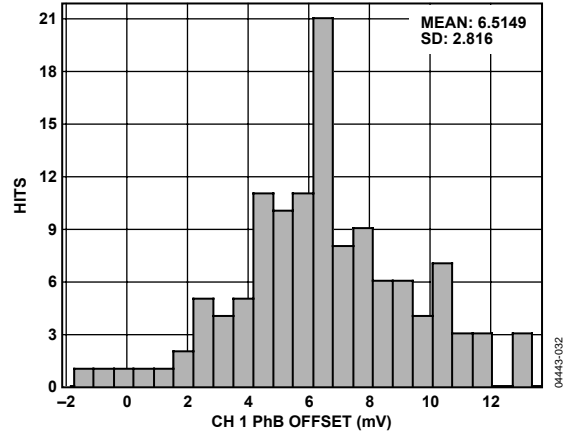


Figure 32. Phase B Channel 1 Offset Distribution

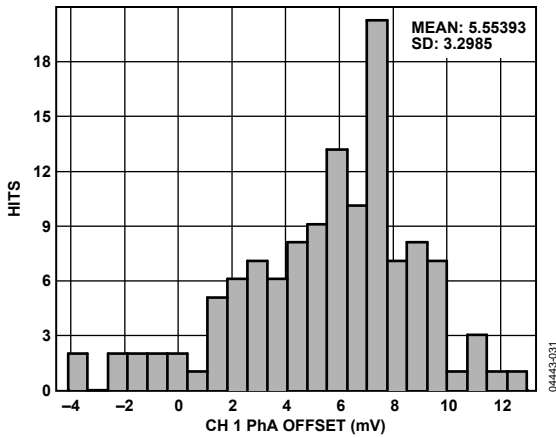


Figure 31. Phase A Channel 1 Offset Distribution

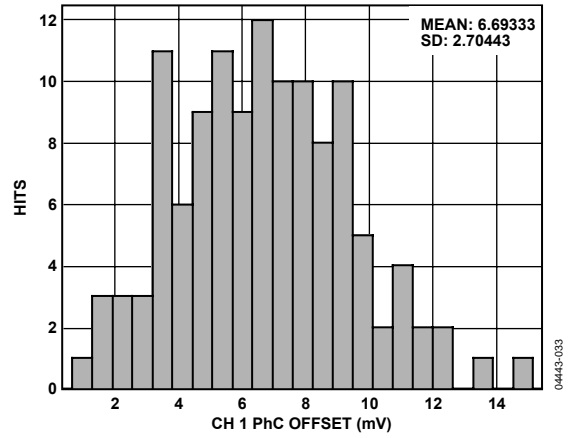


Figure 33. Phase C Channel 1 Offset Distribution

TEST CIRCUITS

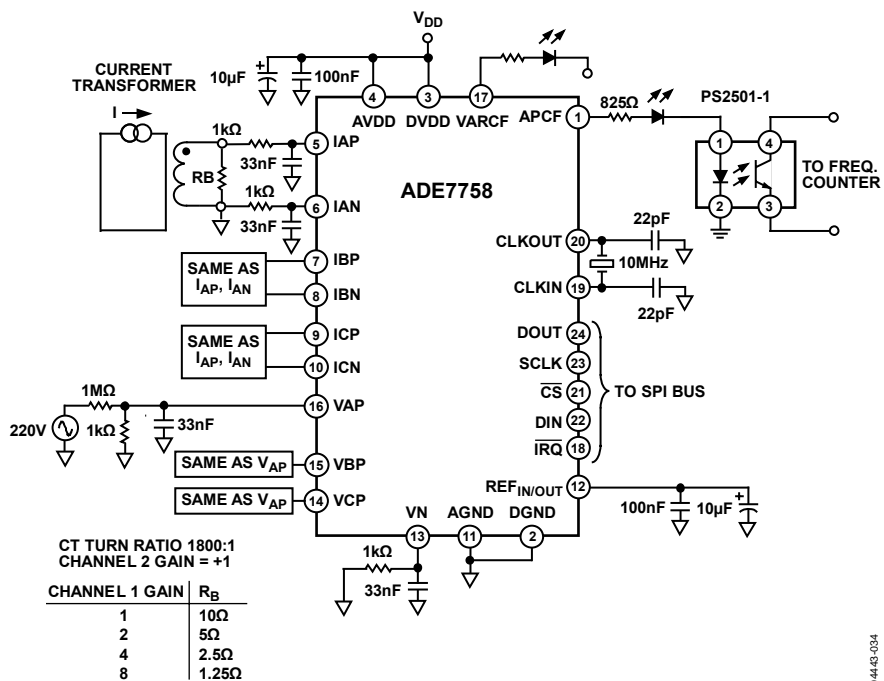


Figure 34. Test Circuit for Integrator Off

0445-034

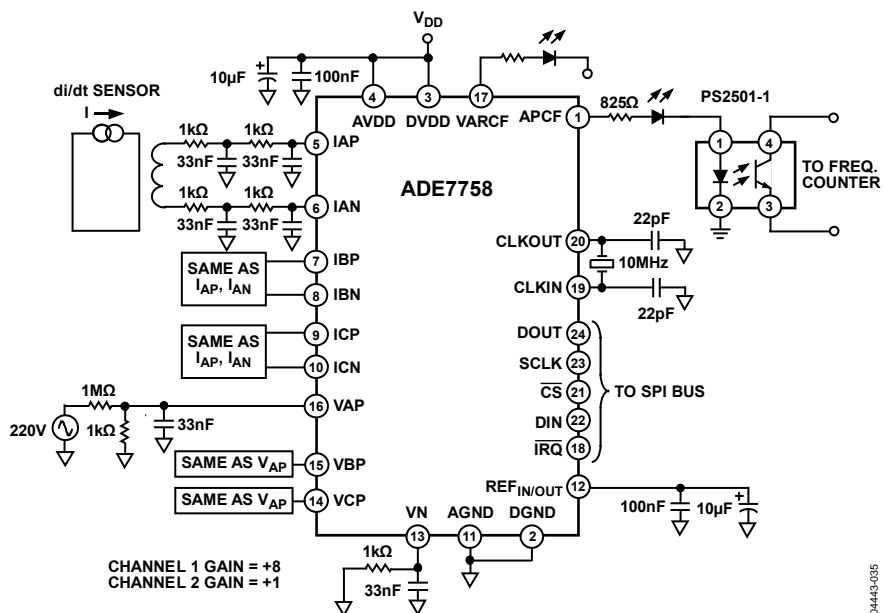


Figure 35. Test Circuit for Integrator On

0445-035

## THEORY OF OPERATION

### ANTI\_ALIASING FILTER

This filter prevents aliasing, which is an artifact of all sampled systems. Input signals with frequency components higher than half the ADC sampling rate distort the sampled signal at a frequency below half the sampling rate. This happens with all ADCs, regardless of the architecture. The combination of the high sampling rate  $\Sigma$ - $\Delta$  ADC used in the ADE7758 with the relatively low bandwidth of the energy meter allows a very simple low-pass filter (LPF) to be used as an antialiasing filter. A simple RC filter (single pole) with a corner frequency of 10 kHz produces an attenuation of approximately 40 dB at 833 kHz. This is usually sufficient to eliminate the effects of aliasing.

### ANALOG INPUTS

The ADE7758 has six analog inputs divided into two channels: current and voltage. The current channel consists of three pairs of fully differential voltage inputs: IAP and IAN, IBP and IBN, and ICP and ICN. These fully differential voltage input pairs have a maximum differential signal of  $\pm 0.5$  V. The current channel has a programmable gain amplifier (PGA) with possible gain selection of 1, 2, or 4. In addition to the PGA, the current channels also have a full-scale input range selection for the ADC. The ADC analog input range selection is also made using the gain register (see Figure 38). As mentioned previously, the maximum differential input voltage is  $\pm 0.5$  V. However, by using Bit 3 and Bit 4 in the gain register, the maximum ADC input voltage can be set to  $\pm 0.5$  V,  $\pm 0.25$  V, or  $\pm 0.125$  V on the current channels. This is achieved by adjusting the ADC reference (see the Reference Circuit section).

Figure 36 shows the maximum signal levels on the current channel inputs. The maximum common-mode signal is  $\pm 25$  mV, as shown in Figure 37.

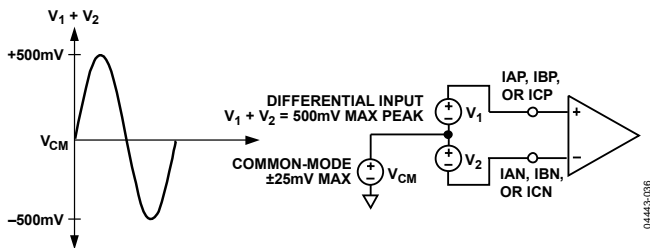


Figure 36. Maximum Signal Levels, Current Channels, Gain = 1

The voltage channel has three single-ended voltage inputs: VAP, VBP, and VCP. These single-ended voltage inputs have a maximum input voltage of  $\pm 0.5$  V with respect to VN. Both the current and voltage channel have a PGA with possible gain selections of 1, 2, or 4. The same gain is applied to all the inputs of each channel.

Figure 37 shows the maximum signal levels on the voltage channel inputs. The maximum common-mode signal is  $\pm 25$  mV, as shown in Figure 36.

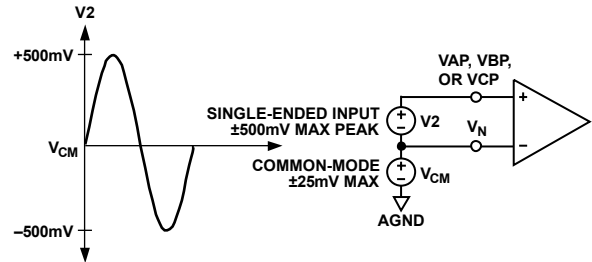


Figure 37. Maximum Signal Levels, Voltage Channels, Gain = 1

The gain selections are made by writing to the gain register. Bit 0 to Bit 1 select the gain for the PGA in the fully differential current channel. The gain selection for the PGA in the single-ended voltage channel is made via Bit 5 to Bit 6. Figure 38 shows how a gain selection for the current channel is made using the gain register.

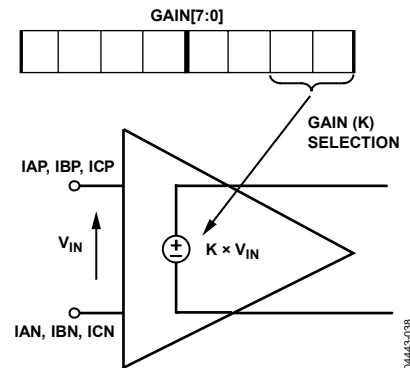
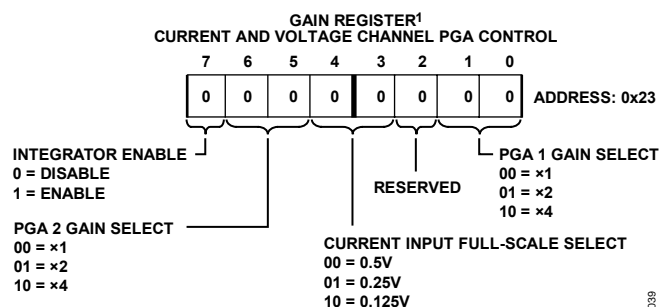


Figure 38. PGA in Current Channel

Figure 39 shows how the gain settings in PGA 1 (current channel) and PGA 2 (voltage channel) are selected by various bits in the gain register.



<sup>1</sup>REGISTER CONTENTS SHOW POWER-ON DEFAULTS

Figure 39. Analog Gain Register

Bit 7 of the gain register is used to enable the digital integrator in the current signal path. Setting this bit activates the digital integrator (see the DI/DT Current Sensor and Digital Integrator section).

### CURRENT CHANNEL ADC

Figure 41 shows the ADC and signal processing path for the input IA of the current channels (same for IB and IC). In waveform sampling mode, the ADC outputs are signed two's complement 24-bit data-words at a maximum of 26.0 kSPS (thousand samples per second). With the specified full-scale analog input signal of ±0.5 V, the ADC produces its maximum output code value (see Figure 41). This diagram shows a full-scale voltage signal being applied to the differential inputs IAP and IAN. The ADC output swings between 0xD7AE14 (−2,642,412) and 0x2851EC (+2,642,412).

### Current Waveform Gain Registers

There is a multiplier in the signal path in the current channel for each phase. The current waveform can be changed by ±50% by writing a two's complement number to the 12-bit signed current waveform gain registers (AIGAIN[11:0], BIGAIN[11:0], and CIGAIN[11:0]). For example, if 0x7FF is written to those registers, the ADC output is scaled up by +50%. To scale the input by −50%, write 0x800 to the registers. Equation 2 describes mathematically the function of the current waveform gain registers.

$$\text{Current Waveform} = \text{ADC Output} \times \left( 1 + \frac{\text{Content of Current Gain Register}}{2^{12}} \right) \quad (2)$$

Changing the content of AIGAIN[11:0], BIGAIN[11:0], or CIGAIN[11:0] affects all calculations based on its current; that is, it affects the phase's active/reactive/apparent energy as well as

its current rms calculation. In addition, waveform samples are also scaled accordingly. IGAIN should not be used when using Mode 0 of CONSEL, COMPMODE[1:0].

### Current Channel Sampling

The waveform samples of the current channel can be routed to the WFORM register at fixed sampling rates by setting the WAVSEL[2:0] bit in the WAVMODE register to 000 (binary) (see Table 20). The phase in which the samples are routed is set by setting the PHSEL[1:0] bits in the WAVMODE register. Energy calculation remains uninterrupted during waveform sampling.

When in waveform sample mode, one of four output sample rates can be chosen by using Bit 5 and Bit 6 of the WAVMODE register (DTRT[1:0]). The output sample rate can be 26.04 kSPS, 13.02 kSPS, 6.51 kSPS, or 3.25 kSPS. By setting the WFSM bit in the interrupt mask register to Logic 1, the interrupt request output  $\overline{\text{IRQ}}$  goes active low when a sample is available. The timing is shown in Figure 40. The 24-bit waveform samples are transferred from the ADE7758 one byte (8-bits) at a time, with the most significant byte shifted out first.

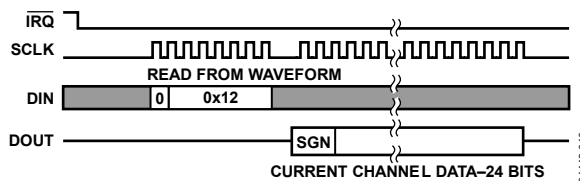


Figure 40. Current Channel Waveform Sampling

The interrupt request output  $\overline{\text{IRQ}}$  stays low until the interrupt routine reads the reset status register (see the Interrupts section).

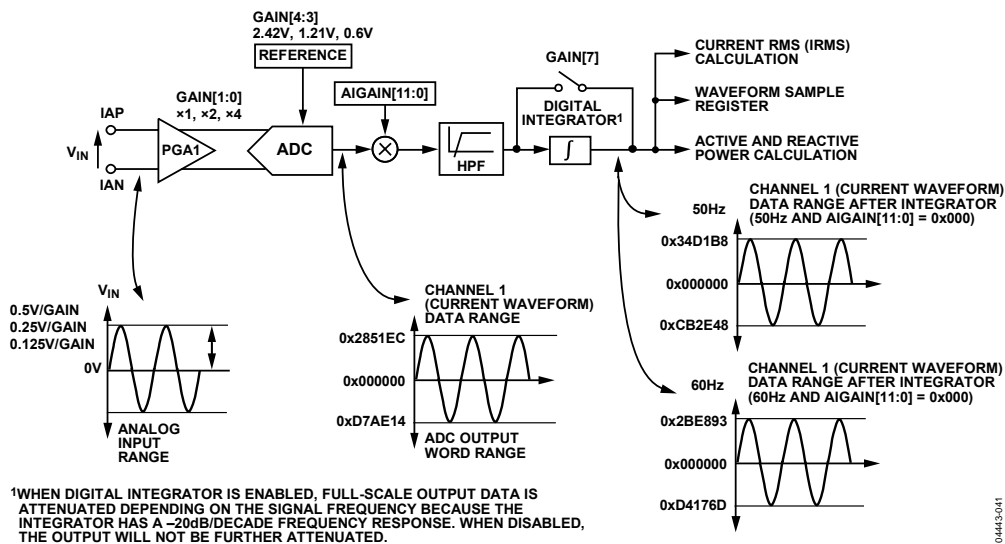


Figure 41. Current Channel Signal Path

## di/dt CURRENT SENSOR AND DIGITAL INTEGRATOR

The di/dt sensor detects changes in the magnetic field caused by the ac current. Figure 42 shows the principle of a di/dt current sensor.

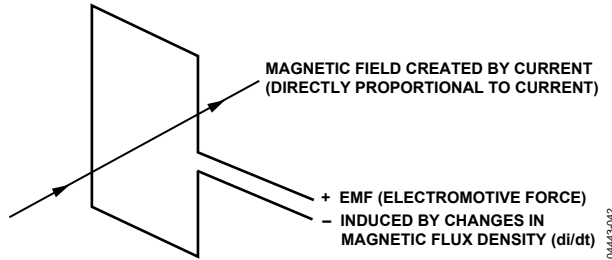


Figure 42. Principle of a di/dt Current Sensor

The flux density of a magnetic field induced by a current is directly proportional to the magnitude of the current. The changes in the magnetic flux density passing through a conductor loop generate an electromotive force (EMF) between the two ends of the loop. The EMF is a voltage signal that is proportional to the di/dt of the current. The voltage output from the di/dt current sensor is determined by the mutual inductance between the current carrying conductor and the di/dt sensor.

The current signal needs to be recovered from the di/dt signal before it can be used. An integrator is therefore necessary to restore the signal to its original form. The ADE7758 has a built-in digital integrator to recover the current signal from the di/dt sensor. The digital integrator on Channel 1 is disabled by default when the ADE7758 is powered up. Setting the MSB of the GAIN[7:0] register turns on the integrator. Figure 43 to Figure 46 show the magnitude and phase response of the digital integrator.

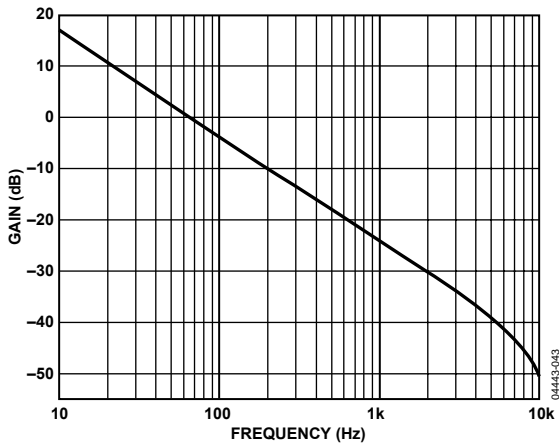


Figure 43. Combined Gain Response of the Digital Integrator and Phase Compensator

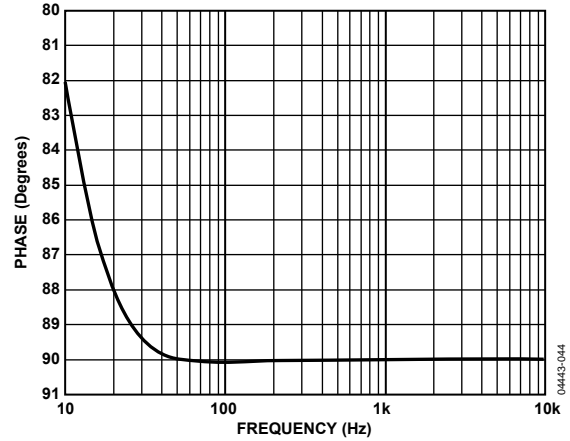


Figure 44. Combined Phase Response of the Digital Integrator and Phase Compensator

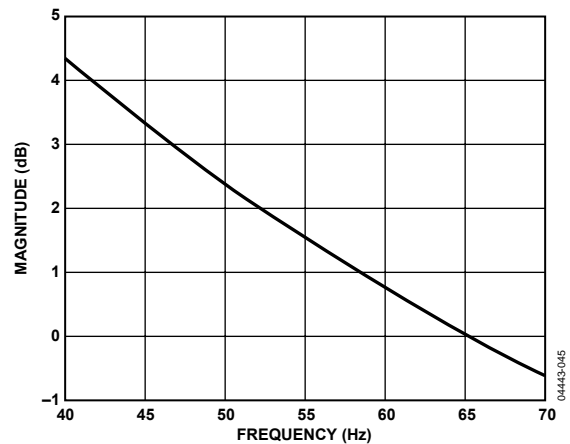


Figure 45. Combined Gain Response of the Digital Integrator and Phase Compensator (40 Hz to 70 Hz)

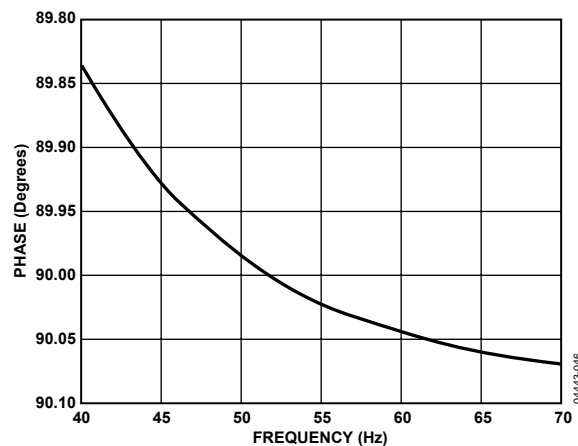


Figure 46. Combined Phase Response of the Digital Integrator and Phase Compensator (40 Hz to 70 Hz)

Note that the integrator has a  $-20$  dB/dec attenuation and approximately  $-90^\circ$  phase shift. When combined with a di/dt sensor, the resulting magnitude and phase response should be a flat gain over the frequency band of interest. However, the di/dt sensor has a 20 dB/dec gain associated with it and generates significant high frequency noise. A more effective antialiasing filter is needed to avoid noise due to aliasing (see the Theory of Operation section).

When the digital integrator is switched off, the ADE7758 can be used directly with a conventional current sensor, such as a current transformer (CT) or a low resistance current shunt.

### PEAK CURRENT DETECTION

The ADE7758 can be programmed to record the peak of the current waveform and produce an interrupt if the current exceeds a preset limit.

#### Peak Current Detection Using the PEAK Register

The peak absolute value of the current waveform within a fixed number of half-line cycles is stored in the IPEAK register. Figure 47 illustrates the timing behavior of the peak current detection.

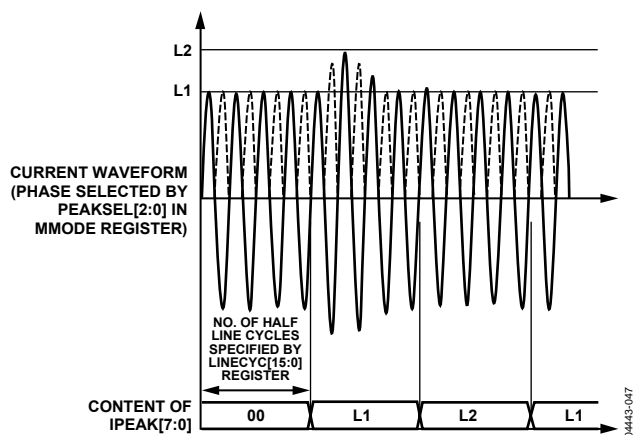


Figure 47. Peak Current Detection Using the IPEAK Register

Note that the content of the IPEAK register is equivalent to Bit 14 to Bit 21 of the current waveform sample. At full-scale analog input, the current waveform sample is 0x2851EC. The IPEAK at full-scale input is therefore expected to be 0xA1.

In addition, multiple phases can be activated for the peak detection simultaneously by setting more than one of the PEAKSEL[2:4] bits in the MMODE register to logic high. These bits select the phase for both voltage and current peak measurements. Note that if more than one bit is set, the VPEAK and IPEAK registers can hold values from two different phases, that is, the voltage and current peak are independently processed (see the Peak Current Detection section).

Note that the number of half-line cycles is based on counting the zero crossing of the voltage channel. The ZXSEL[2:0] bits in the LCYCMODE register determine which voltage channels are used for the zero-crossing detection. The same signal is also used for line cycle energy accumulation mode if activated (see the Line Cycle Accumulation Mode Register (0x17) section).

### OVERCURRENT DETECTION INTERRUPT

Figure 48 illustrates the behavior of the overcurrent detection.

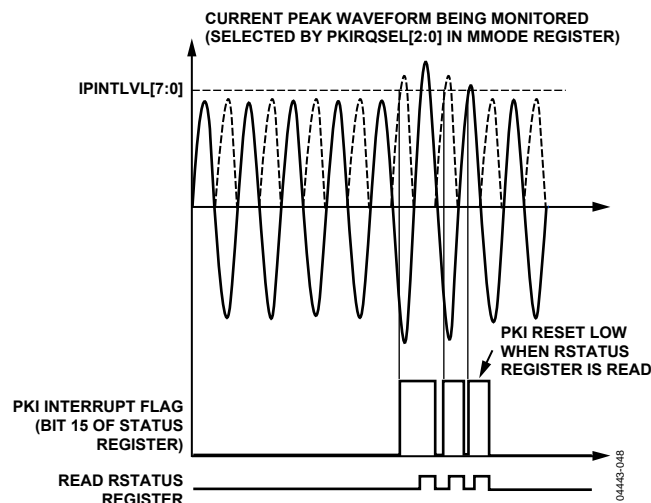


Figure 48. ADE7758 Overcurrent Detection

Note that the content of the IPINTLVL[7:0] register is equivalent to Bit 14 to Bit 21 of the current waveform sample. Therefore, setting this register to 0xA1 represents putting peak detection at full-scale analog input. Figure 48 shows a current exceeding a threshold. The overcurrent event is recorded by setting the PKI flag (Bit 15) in the interrupt status register. If the PKI enable bit is set to Logic 1 in the interrupt mask register, the  $\overline{IRQ}$  logic output goes active low (see the Interrupts section).

Similar to peak level detection, multiple phases can be activated for peak detection. If any of the active phases produce waveform samples above the threshold, the PKI flag in the interrupt status register is set. The phase of which overcurrent is monitored is set by the PKIRQSEL[2:0] bits in the MMODE register (see Table 19).

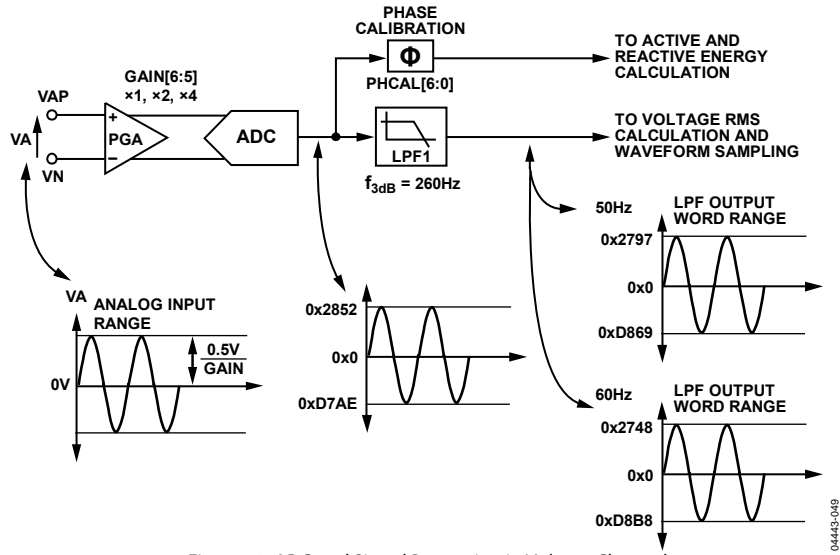


Figure 49. ADC and Signal Processing in Voltage Channel

## VOLTAGE CHANNEL ADC

Figure 49 shows the ADC and signal processing chain for the input VA in the voltage channel. The VB and VC channels have similar processing chains.

For active and reactive energy measurements, the output of the ADC passes to the multipliers directly and is not filtered. This solution avoids the much larger multibit multiplier and does not affect the accuracy of the measurement. An HPF is not implemented on the voltage channel to remove the dc offset because the HPF on the current channel alone should be sufficient to eliminate error due to ADC offsets in the power calculation. However, ADC offset in the voltage channels produces large errors in the voltage rms calculation and affects the accuracy of the apparent energy calculation.

## Voltage Channel Sampling

The waveform samples on the voltage channels can also be routed to the WFORM register. However, before passing to the WFORM register, the ADC outputs pass through a single-pole, low-pass filter (LPF1) with a cutoff frequency at 260 Hz. Figure 50 shows the magnitude and phase response of LPF1. This filter attenuates the signal slightly. For example, if the line frequency is 60 Hz, the signal at the output of LPF1 is attenuated by 3.575%. The waveform samples are 16-bit, twos complement data ranging between 0x2748 (+10,056d) and 0xD8B8 (-10,056d). The data is sign extended to 24-bit in the WFORM register.

$$H(f) = \frac{1}{\sqrt{1 + \left(\frac{60 \text{ Hz}}{260 \text{ Hz}}\right)^2}} = 0.974 = -0.225 \text{ dB} \quad (3)$$

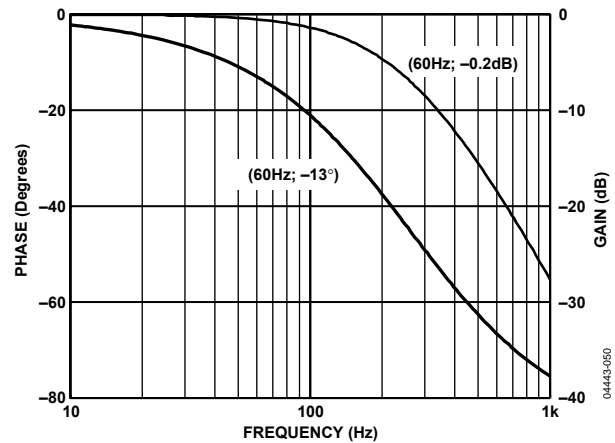


Figure 50. Magnitude and Phase Response of LPF1

Note that LPF1 does not affect the active and reactive energy calculation because it is only used in the waveform sampling signal path. However, waveform samples are used for the voltage rms calculation and the subsequent apparent energy accumulation.

The WAVSEL[2:0] bits in the WAVMODE register should be set to 001 (binary) to start the voltage waveform sampling. The PHSEL[1:0] bits control the phase from which the samples are routed. In waveform sampling mode, one of four output sample rates can be chosen by changing Bit 5 and Bit 6 of the WAVMODE register (see Table 20). The available output sample rates are 26.0 kSPS, 13.5 kSPS, 6.5 kSPS, or 3.3 kSPS. By setting the WFSM bit in the interrupt mask register to Logic 1, the interrupt request output IRQ goes active low when a sample is available. The 24-bit waveform samples are transferred from the ADE7758 one byte (8 bits) at a time, with the most significant byte shifted out first.

The sign of the register is extended in the upper 8 bits. The timing is the same as for the current channels, as seen in Figure 40.

### ZERO-CROSSING DETECTION

The ADE7758 has zero-crossing detection circuits for each of the voltage channels (VAN, VBN, and VCN). Figure 51 shows how the zero-cross signal is generated from the output of the ADC of the voltage channel.

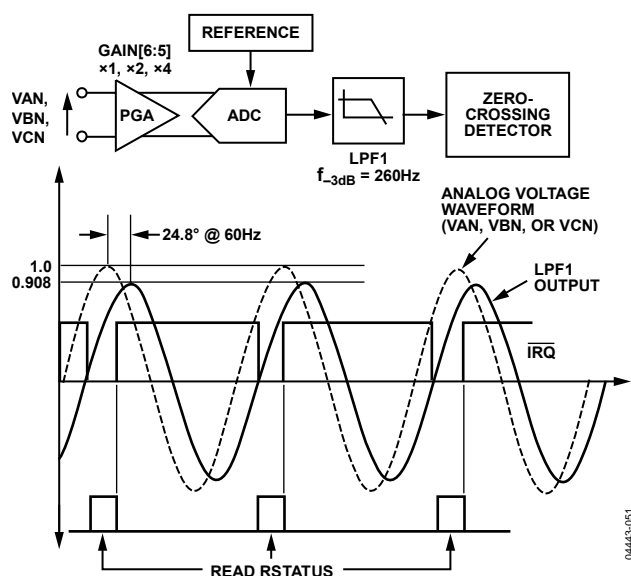


Figure 51. Zero-Crossing Detection on Voltage Channels

The zero-crossing interrupt is generated from the output of LPF1. LPF1 has a single pole at 260 Hz (CLKIN = 10 MHz). As a result, there is a phase lag between the analog input signal of the voltage channel and the output of LPF1. The phase response of this filter is shown in the Voltage Channel Sampling section. The phase lag response of LPF1 results in a time delay of approximately 1.1 ms (at 60 Hz) between the zero crossing on the voltage inputs and the resulting zero-crossing signal. Note that the zero-crossing signal is used for the line cycle accumulation mode, zero-crossing interrupt, and line period/frequency measurement.

When one phase crosses from negative to positive, the corresponding flag in the interrupt status register (Bit 9 to Bit 11) is set to Logic 1. An active low in the IRQ output also appears if the corresponding ZX bit in the interrupt mask register is set to Logic 1. Note that only zero crossing from negative to positive generates an interrupt.

The flag in the interrupt status register is reset to 0 when the interrupt status register with reset (RSTATUS) is read. Each phase has its own interrupt flag and mask bit in the interrupt register.

### Zero-Crossing Timeout

Each zero-crossing detection has an associated internal timeout register (not accessible to the user). This unsigned, 16-bit register is decreased by 1 every 384/CLKIN seconds. The registers are reset to a common user-programmed value, that is, the zero-crossing timeout register (ZXTOUT[15:0], Address 0x1B), every time a zero crossing is detected on its associated input. The default value of ZXTOUT is 0xFFFF. If the internal register decrements to 0 before a zero crossing at the corresponding input is detected, it indicates an absence of a zero crossing in the time determined by the ZXTOUT[15:0]. The ZXTOx detection bit of the corresponding phase in the interrupt status register is then switched on (Bit 6 to Bit 8). An active low on the IRQ output also appears if the ZXTOx mask bit for the corresponding phase in the interrupt mask register is set to Logic 1. Figure 52 shows the mechanism of the zero-crossing timeout detection when the Line Voltage A stays at a fixed dc level for more than 384/CLKIN × ZXTOUT[15:0] seconds.

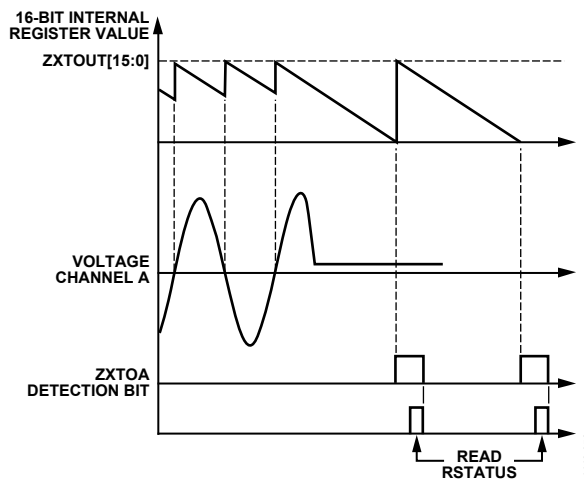


Figure 52. Zero-Crossing Timeout Detection

### PHASE COMPENSATION

When the HPF in the current channel is disabled, the phase error between the current channel (IA, IB, or IC) and the corresponding voltage channel (VA, VB, or VC) is negligible. When the HPF is enabled, the current channels have phase response (see Figure 53 through Figure 55). The phase response is almost 0 from 45 Hz to 1 kHz. The frequency band is sufficient for the requirements of typical energy measurement applications.

However, despite being internally phase compensated, the ADE7758 must work with transducers that may have inherent phase errors. For example, a current transformer (CT) with a phase error of 0.1° to 0.3° is not uncommon. These phase errors can vary from part to part, and they must be corrected to perform accurate power calculations.

# ADE7758

The errors associated with phase mismatch are particularly noticeable at low power factors. The ADE7758 provides a means of digitally calibrating these small phase errors. The ADE7758 allows a small time delay or time advance to be introduced into the signal processing chain to compensate for the small phase errors.

The phase calibration registers (APHCAL, BPHCAL, and CPHCAL) are two's complement, 7-bit sign-extended registers that can vary the time advance in the voltage channel signal path from +153.6  $\mu\text{s}$  to -75.6  $\mu\text{s}$  (CLKIN = 10 MHz), respectively. Negative values written to the PHCAL registers represent a time advance, and positive values represent a time delay. One LSB is equivalent to 1.2  $\mu\text{s}$  of time delay or 2.4  $\mu\text{s}$  of time advance with a CLKIN of 10 MHz. With a line frequency of 60 Hz, this gives a phase resolution of  $0.026^\circ$  ( $360^\circ \times 1.2 \mu\text{s} \times 60 \text{ Hz}$ ) at the fundamental in the positive direction (delay) and  $0.052^\circ$  in the negative direction (advance). This corresponds to a total correction range of  $-3.32^\circ$  to  $+1.63^\circ$  at 60 Hz.

Figure 56 illustrates how the phase compensation is used to remove a  $0.1^\circ$  phase lead in IA of the current channel from the external current transducer. To cancel the lead ( $0.1^\circ$ ) in the current channel of Phase A, a phase lead must be introduced into the corresponding voltage channel. The resolution of the phase adjustment allows the introduction of a phase lead of  $0.104^\circ$ . The phase lead is achieved by introducing a time advance into VA. A time advance of 4.8  $\mu\text{s}$  is made by writing -2 (0x7E) to the time delay block (APHCAL[6:0]), thus reducing the amount of time delay by 4.8  $\mu\text{s}$  or equivalently,  $360^\circ \times 4.8 \mu\text{s} \times 60 \text{ Hz} = 0.104^\circ$  at 60 Hz.

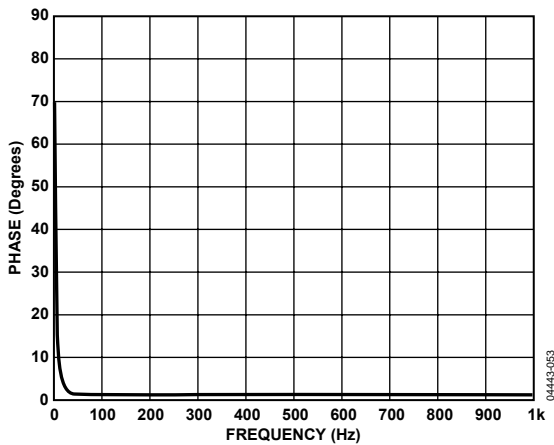


Figure 53. Phase Response of the HPF and Phase Compensation (10 Hz to 1 kHz)

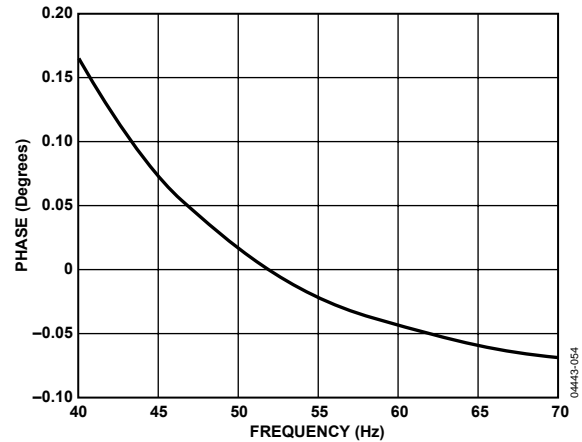


Figure 54. Phase Response of the HPF and Phase Compensation (40 Hz to 70 Hz)

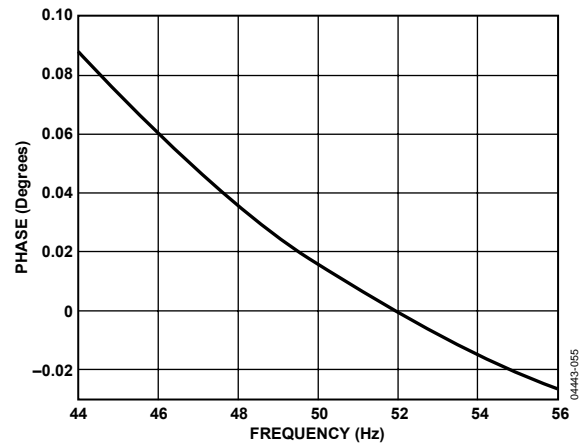


Figure 55. Phase Response of HPF and Phase Compensation (44 Hz to 56 Hz)

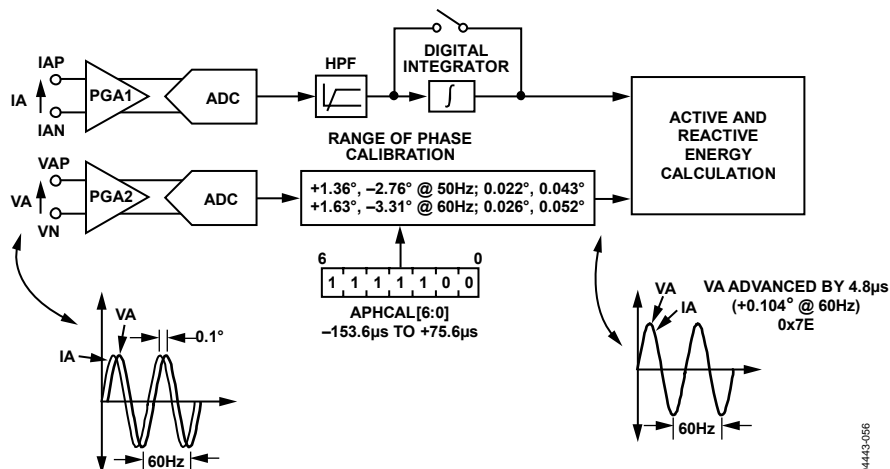


Figure 56. Phase Calibration on Voltage Channels

**PERIOD MEASUREMENT**

The ADE7758 provides the period or frequency measurement of the line voltage. The period is measured on the phase specified by Bit 0 to Bit 1 of the MMODE register. The period register is an unsigned 12-bit FREQ register and is updated every four periods of the selected phase.

Bit 7 of the LCYCMODE selects whether the period register displays the frequency or the period. Setting this bit causes the register to display the period. The default setting is logic low, which causes the register to display the frequency.

When set to measure the period, the resolution of this register is 96/CLKIN per LSB (9.6 µs/LSB when CLKIN is 10 MHz), which represents 0.06% when the line frequency is 60 Hz. At 60 Hz, the value of the period register is 1737d. At 50 Hz, the value of the period register is 2084d. When set to measure frequency, the value of the period register is approximately 960d at 60 Hz and 800d at 50 Hz. This is equivalent to 0.0625 Hz/LSB.

**LINE VOLTAGE SAG DETECTION**

The ADE7758 can be programmed to detect when the absolute value of the line voltage of any phase drops below a certain peak value for a number of half cycles. Each phase of the voltage channel is controlled simultaneously. This condition is illustrated in Figure 57.

Figure 57 shows a line voltage fall below a threshold, which is set in the SAG level register (SAGLVL[7:0]), for nine half cycles. Because the SAG cycle register indicates a six half-cycle threshold (SAGCYC[7:0] = 0x06), the SAG event is recorded at the end of the sixth half cycle by setting the SAG flag of the corresponding phase in the interrupt status register (Bit 1 to Bit 3 in the interrupt status register).

If the SAG enable bit is set to Logic 1 for this phase (Bit 1 to Bit 3 in the interrupt mask register), the  $\overline{\text{IRQ}}$  logic output goes active low (see the Interrupts section). The phases are compared to the same parameters defined in the SAGLVL and SAGCYC registers.

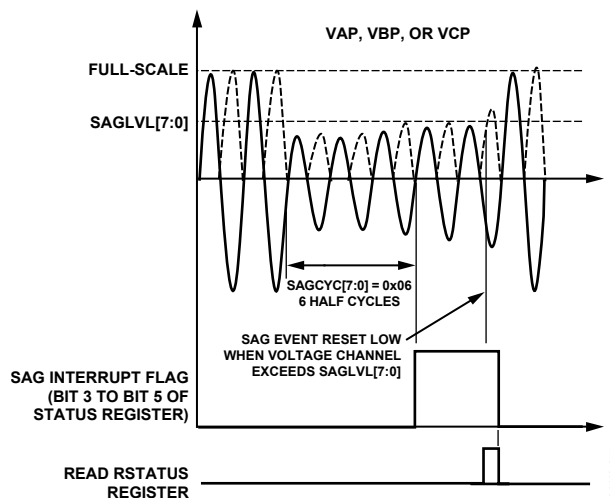


Figure 57. ADE7758 SAG Detection

Figure 57 shows a line voltage fall below a threshold, which is set in the SAG level register (SAGLVL[7:0]), for nine half cycles. Because the SAG cycle register indicates a six half-cycle threshold (SAGCYC[7:0] = 0x06), the SAG event is recorded at the end of the sixth half cycle by setting the SAG flag of the corresponding phase in the interrupt status register (Bit 1 to Bit 3 in the interrupt status register). If the SAG enable bit is set to Logic 1 for this phase (Bit 1 to Bit 3 in the interrupt mask register), the  $\overline{\text{IRQ}}$  logic output goes active low (see the Interrupts section). The phases are compared to the same parameters defined in the SAGLVL and SAGCYC registers.

## SAG LEVEL SET

The contents of the single-byte SAG level register, SAGLVL[0:7], are compared to the absolute value of Bit 6 to Bit 13 from the voltage waveform samples. For example, the nominal maximum code of the voltage channel waveform samples with a full-scale signal input at 60 Hz is 0x2748 (see the Voltage Channel Sampling section). Bit 13 to Bit 6 are 0x9D. Therefore, writing 0x9D to the SAG level register puts the SAG detection level at full scale and sets the SAG detection to its most sensitive value.

The detection is made when the content of the SAGLVL[7:0] register is greater than the incoming sample. Writing 0x00 puts the SAG detection level at 0. The detection of a decrease of an input voltage is disabled in this case.

## PEAK VOLTAGE DETECTION

The ADE7758 can record the peak of the voltage waveform and produce an interrupt if the current exceeds a preset limit.

### Peak Voltage Detection Using the VPEAK Register

The peak absolute value of the voltage waveform within a fixed number of half-line cycles is stored in the VPEAK register. Figure 58 illustrates the timing behavior of the peak voltage detection.

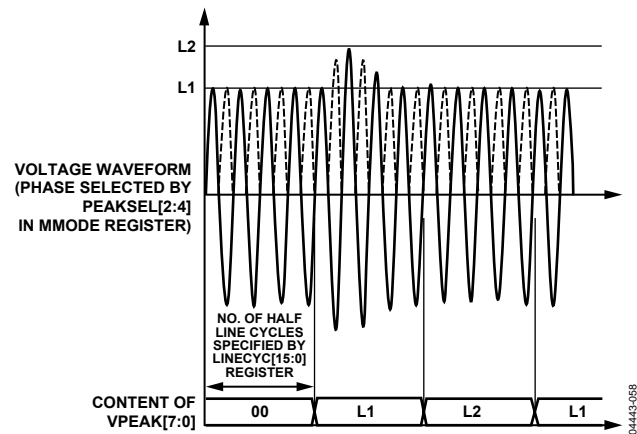


Figure 58. Peak Voltage Detection Using the VPEAK Register

Note that the content of the VPEAK register is equivalent to Bit 6 to Bit 13 of the 16-bit voltage waveform sample. At full-scale analog input, the voltage waveform sample at 60 Hz is 0x2748. The VPEAK at full-scale input is therefore expected to be 0x9D.

In addition, multiple phases can be activated for the peak detection simultaneously by setting multiple bits among the PEAKSEL[2:4] bits in the MMODE register. These bits select the phase for both voltage and current peak measurements.

Note that if more than one bit is set, the VPEAK and IPEAK registers can hold values from two different phases, that is, the voltage and current peak are independently processed (see the Peak Current Detection section).

Note that the number of half-line cycles is based on counting the zero crossing of the voltage channel. The ZXSEL[2:0] bits in the LCYCMODE register determine which voltage channels are used for the zero-crossing detection (see Table 22). The same signal is also used for line cycle energy accumulation mode if activated.

## Overvoltage Detection Interrupt

Figure 59 illustrates the behavior of the overvoltage detection.

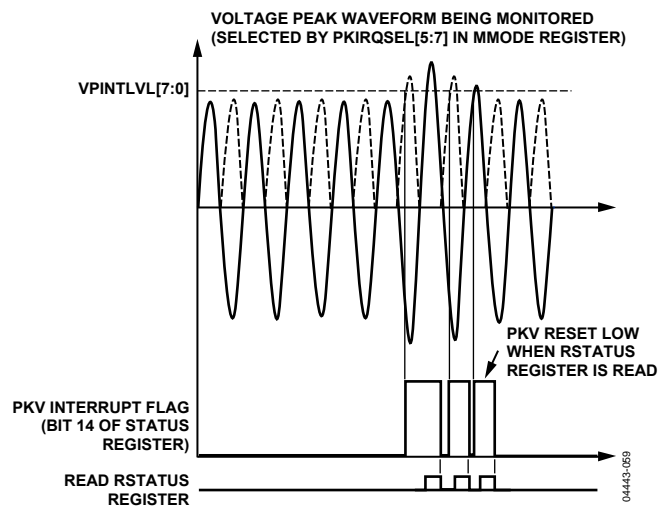


Figure 59. ADE7758 Overvoltage Detection

Note that the content of the VPINTLVL[7:0] register is equivalent to Bit 6 to Bit 13 of the 16-bit voltage waveform samples; therefore, setting this register to 0x9D represents putting the peak detection at full-scale analog input. Figure 59 shows a voltage exceeding a threshold. By setting the PKV flag (Bit 14) in the interrupt status register, the overvoltage event is recorded. If the PKV enable bit is set to Logic 1 in the interrupt mask register, the  $\overline{\text{IRQ}}$  logic output goes active low (see the Interrupts section).

Multiple phases can be activated for peak detection. If any of the active phase produces waveform samples above the threshold, the PKV flag in the interrupt status register is set. The phase in which overvoltage is monitored is set by the PKIRQSEL[5:7] bits in the MMODE register (see Table 19).

### PHASE SEQUENCE DETECTION

The ADE7758 has an on-chip phase sequence error detection interrupt. If the zero crossing of Phase A is not followed by Phase C but by Phase B, the SEQERR bit (Bit 19) in the STATUS register is set. If SEQERR is set in the mask register, the  $\overline{\text{IRQ}}$  logic output goes active low (see the Interrupts section). Figure 60 depicts how the interrupt is issued in two different configurations.

Note that if it is desired to have the interrupt occur when Phase A is followed by Phase B and not Phase C, then the analog inputs for Phase B and Phase C should be swapped. In this case, the Phase B voltage input should be wired to the VCP pin and the Phase C voltage input should be wired to the VBP pin.

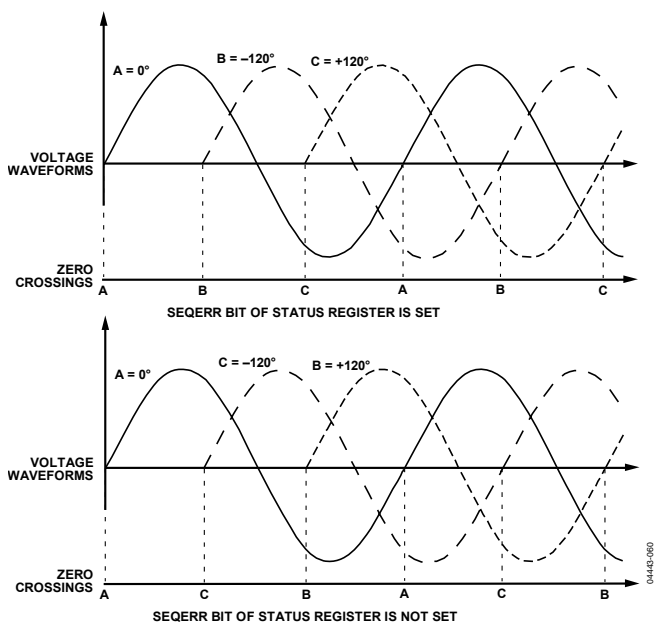


Figure 60. Phase Sequence Detection

### POWER-SUPPLY MONITOR

The ADE7758 also contains an on-chip power-supply monitor. The analog supply (AVDD) is monitored continuously by the ADE7758. If the supply is less than  $4\text{ V} \pm 5\%$ , the ADE7758 goes into an inactive state, that is, no energy is accumulated when the supply voltage is below 4 V. This is useful to ensure correct device operation at power-up and during power-down. The power-supply monitor has built-in hysteresis and filtering. This gives a high degree of immunity to false triggering due to noisy supplies. Figure 61 shows the behavior of the ADE7758 when the voltage of AVDD falls below the power-supply monitor threshold. The power supply and decoupling for the part should be designed such that the ripple at AVDD does not exceed  $5\text{ V} \pm 5\%$  as specified for normal operation.

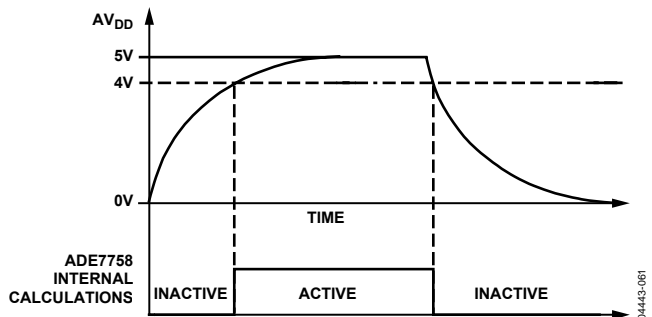


Figure 61. On-Chip, Power-Supply Monitoring

### REFERENCE CIRCUIT

The nominal reference voltage at the REF<sub>IN/OUT</sub> pin is 2.42 V. This is the reference voltage used for the ADCs in the ADE7758. However, the current channels have three input range selections (full scale is selectable among 0.5 V, 0.25 V, and 0.125 V). This is achieved by dividing the reference internally by 1, 1/2, and 1/4. The reference value is used for the ADC in the current channels. Note that the full-scale selection is only available for the current inputs.

The REF<sub>IN/OUT</sub> pin can be overdriven by an external source, for example, an external 2.5 V reference. Note that the nominal reference value supplied to the ADC is now 2.5 V and not 2.42 V. This has the effect of increasing the nominal analog input signal range by  $2.5/2.42 \times 100\% = 3\%$  or from 0.5 V to 0.5165 V.

The voltage of the ADE7758 reference drifts slightly with temperature; see the Specifications section for the temperature coefficient specification (in ppm/°C). The value of the temperature drift varies from part to part. Because the reference is used for all ADCs, any x% drift in the reference results in a 2x% deviation of the meter accuracy. The reference drift resulting from temperature changes is usually very small and typically much smaller than the drift of other components on a meter. Alternatively, the meter can be calibrated at multiple temperatures.

## TEMPERATURE MEASUREMENT

The ADE7758 also includes an on-chip temperature sensor. A temperature measurement is made every 4/CLKIN seconds. The output from the temperature sensing circuit is connected to an ADC for digitizing. The resultant code is processed and placed in the temperature register (TEMP[7:0]). This register can be read by the user and has an address of 0x11 (see the Serial Interface section). The contents of the temperature register are signed (twos complement) with a resolution of 3°C/LSB. The offset of this register may vary significantly from part to part. To calibrate this register, the nominal value should be measured, and the equation should be adjusted accordingly.

$$Temp (^{\circ}C) = [(TEMP[7:0] - Offset) \times 3^{\circ}C/LSB] + Ambient(^{\circ}C) \quad (4)$$

For example, if the temperature register produces a code of 0x46 at ambient temperature (25°C), and the temperature register currently reads 0x50, then the temperature is 55°C :

$$Temp (^{\circ}C) = [(0x50 - 0x46) \times 3^{\circ}C/LSB] + 25^{\circ}C = 55^{\circ}C$$

Depending on the nominal value of the register, some finite temperature can cause the register to roll over. This should be compensated for in the system master (MCU).

The ADE7758 temperature register varies with power supply. It is recommended to use the temperature register only in applications with a fixed, stable power supply. Typical error with respect to power supply variation is show in Table 5.

**Table 5. Temperature Register Error with Power Supply Variation**

	4.5 V	4.75 V	5 V	5.25 V	5.5 V
<b>Register Value</b>	219	216	214	211	208
<b>% Error</b>	+2.34	+0.93	0	-1.40	-2.80

## ROOT MEAN SQUARE MEASUREMENT

Root mean square (rms) is a fundamental measurement of the magnitude of an ac signal. Its definition can be both practical and mathematical. Defined practically, the rms value assigned to an ac signal is the amount of dc required to produce an equivalent amount of power in the load. Mathematically, the rms value of a continuous signal  $f(t)$  is defined as

$$FRMS = \sqrt{\frac{1}{T} \int_0^T f^2(t) dt} \quad (5)$$

For time sampling signals, rms calculation involves squaring the signal, taking the average, and obtaining the square root.

$$FRMS = \sqrt{\frac{1}{N} \sum_{n=1}^N f^2[n]} \quad (6)$$

The method used to calculate the rms value in the ADE7758 is to low-pass filter the square of the input signal (LPF3) and take the square root of the result (see Figure 62).

$$i(t) = \sqrt{2} \times IRMS \times \sin(\omega t) \quad (7)$$

then

$$i^2(t) = IRMS^2 - IRMS^2 \times \cos(\omega t) \quad (8)$$

The rms calculation is simultaneously processed on the six analog input channels. Each result is available in separate registers.

While the ADE7758 measures nonsinusoidal signals, it should be noted that the voltage rms measurement, and therefore the apparent energy, are bandlimited to 260 Hz. The current rms as well as the active power have a bandwidth of 14 kHz.

### Current RMS Calculation

Figure 62 shows the detail of the signal processing chain for the rms calculation on one of the phases of the current channel. The current channel rms value is processed from the samples used in the current channel waveform sampling mode. The current rms values are stored in unsigned 24-bit registers (AIRMS, BIRMS, and CIRMS). One LSB of the current rms register is equivalent to one LSB of the current waveform sample. The update rate of the current rms measurement is CLKIN/12.

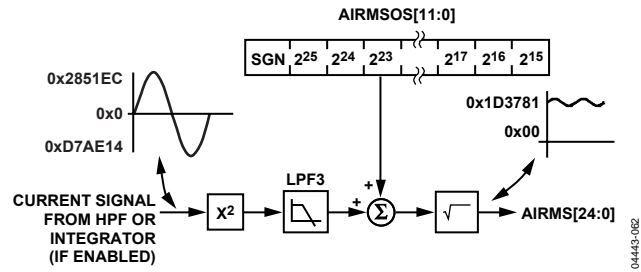


Figure 62. Current RMS Signal Processing

With the specified full-scale analog input signal of 0.5 V, the ADC produces an output code that is approximately  $\pm 2,642,412d$  (see the Current Channel ADC section). The equivalent rms value of a full-scale sinusoidal signal at 60 Hz is 1,914,753 (0x1D3781).

The accuracy of the current rms is typically 0.5% error from the full-scale input down to 1/500 of the full-scale input. Additionally, this measurement has a bandwidth of 14 kHz. It is recommended to read the rms registers synchronous to the voltage zero crossings to ensure stability. The IRQ can be used to indicate when a zero crossing has occurred (see the Interrupts section).

Table 6 shows the settling time for the IRMS measurement, which is the time it takes for the rms register to reflect the value at the input to the current channel.

**Table 6. Settling Time for IRMS Measurement**

	63%	100%
<b>Integrator Off</b>	80 ms	960 ms
<b>Integrator On</b>	40 ms	1.68 sec

### Current RMS Offset Compensation

The ADE7758 incorporates a current rms offset compensation register for each phase (AIRMSOS, BIRMSOS, and CIRMSOS). These are 12-bit signed registers that can be used to remove offsets in the current rms calculations. An offset can exist in the rms calculation due to input noises that are integrated in the dc component of  $I^2(t)$ . Assuming that the maximum value from the current rms calculation is 1,914,753d with full-scale ac inputs (60 Hz), one LSB of the current rms offset represents 0.94% of the measurement error at 60 dB down from full scale. The IRMS measurement is undefined at zero input. Calibration of the offset should be done at low current and values at zero input should be ignored. For details on how to calibrate the current rms measurement, see the Calibration section.

$$IRMS = \sqrt{IRMS_0^2 + 16384 \times IRMSOS} \tag{9}$$

where  $IRMS_0$  is the rms measurement without offset correction.

**Table 7. Approximate IRMS Register Values**

Frequency (Hz)	Integrator Off (d)	Integrator On (d)
50	1,921,472	2,489,581
60	1,914,752	2,067,210

### Voltage Channel RMS Calculation

Figure 63 shows the details of the signal path for the rms calculation on Phase A of the voltage channel. The voltage channel rms value is processed from the waveform samples after the low-pass filter LPF1. The output of the voltage channel ADC can be scaled by  $\pm 50\%$  by changing VRMSGAIN[11:0] registers to perform an overall rms voltage calibration. The VRMSGAIN registers scale the rms calculations as well as the apparent energy calculation because apparent power is the product of the voltage and current rms values. The voltage rms values are stored in unsigned 24-bit registers (AVRMS, BVRMS, and CVRMS). One LSB of a voltage waveform sample is approximately equivalent to 256 LSBs of the voltage rms register. The update rate of the voltage rms measurement is  $CLKIN/12$ .

With the specified full-scale ac analog input signal of 0.5 V, the LPF1 produces an output code that is approximately 63% of its full-scale value, that is,  $\pm 9,372d$ , at 60 Hz (see the Voltage Channel ADC section). The equivalent rms value of a full-scale ac signal is approximately 1,639,101 (0x1902BD) in the VRMS register.

The accuracy of the VRMS measurement is typically 0.5% error from the full-scale input down to 1/20 of the full-scale input. Additionally, this measurement has a bandwidth of 260 Hz. It is recommended to read the rms registers synchronous to the voltage zero crossings to ensure stability. The IRQ can be used to indicate when a zero crossing has occurred (see the Interrupts section).

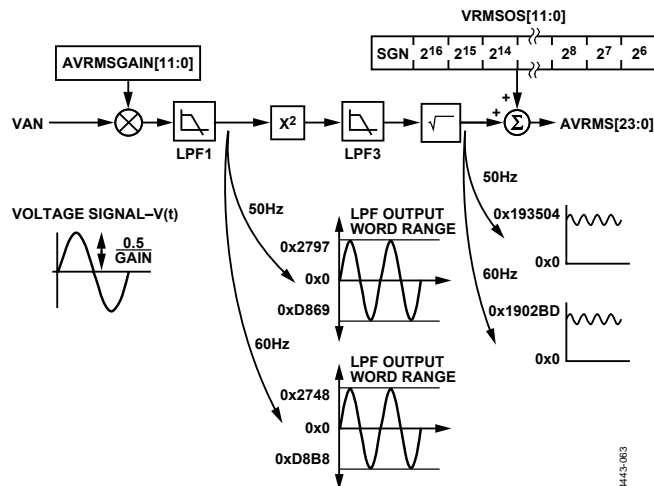


Figure 63. Voltage RMS Signal Processing

Table 8 shows the settling time for the VRMS measurement, which is the time it takes for the rms register to reflect the value at the input to the voltage channel.

**Table 8. Settling Time for VRMS Measurement**

63%	100%
100 ms	960 ms

### Voltage RMS Offset Compensation

The ADE7758 incorporates a voltage rms offset compensation for each phase (AVRMSOS, BVRMSOS, and CVRMSOS). These are 12-bit signed registers that can be used to remove offsets in the voltage rms calculations. An offset can exist in the rms calculation due to input noises and offsets in the input samples. It should be noted that the offset calibration does not allow the contents of the VRMS registers to be maintained at 0 when no voltage is applied. This is caused by noise in the voltage rms calculation, which limits the usable range between full scale and 1/50th of full scale. One LSB of the voltage rms offset is equivalent to 64 LSBs of the voltage rms register.

Assuming that the maximum value from the voltage rms calculation is 1,639,101d with full-scale ac inputs, then 1 LSB of the voltage rms offset represents 0.042% of the measurement error at 1/10 of full scale.

$$VRMS = VRMS_0 + VRMSOS \times 64 \tag{10}$$

where  $VRMS_0$  is the rms measurement without the offset correction.

**Table 9. Approximate VRMS Register Values**

Frequency (Hz)	Value (d)
50	1,678,210
60	1,665,118

## Voltage RMS Gain Adjust

The ADC gain in each phase of the voltage channel can be adjusted for the rms calculation by using the voltage rms gain registers (AVRMSGAIN, BVRMSGAIN, and CVRMSGAIN). The gain of the voltage waveforms before LPF1 is adjusted by writing twos complement, 12-bit words to the voltage rms gain registers. Equation 11 shows how the gain adjustment is related to the contents of the voltage gain register.

Content of VRMS Register =

$$\text{Nominal RMS Values Without Gain} \times \left(1 + \frac{\text{VRMSGAIN}}{2^{12}}\right) \quad (11)$$

For example, when 0x7FF is written to the voltage gain register, the RMS value is scaled up by 50%.

$$\begin{aligned} 0x7FF &= 2047d \\ 2047/2^{12} &= 0.5 \end{aligned}$$

Similarly, when 0x800, which equals -2047d (signed twos complement), is written the ADC output is scaled by -50%.

## ACTIVE POWER CALCULATION

Electrical power is defined as the rate of energy flow from source to load. It is given by the product of the voltage and current waveforms. The resulting waveform is called the instantaneous power signal and it is equal to the rate of energy flow at every instant of time. The unit of power is the watt or joules/sec. Equation 14 gives an expression for the instantaneous power signal in an ac system.

$$v(t) = \sqrt{2} \times VRMS \times \sin(\omega t) \quad (12)$$

$$i(t) = \sqrt{2} \times IRMS \times \sin(\omega t) \quad (13)$$

where  $VRMS$  = rms voltage and  $IRMS$  = rms current.

$$p(t) = v(t) \times i(t)$$

$$p(t) = IRMS \times VRMS - IRMS \times VRMS \times \cos(2\omega t) \quad (14)$$

The average power over an integral number of line cycles ( $n$ ) is given by the expression in Equation 15.

$$p = \frac{1}{nT} \int_0^{nT} p(t) dt = VRMS \times IRMS \quad (15)$$

where:

$t$  is the line cycle period.

$P$  is referred to as the active or real power. Note that the active power is equal to the dc component of the instantaneous power signal  $p(t)$  in Equation 14, that is,  $VRMS \times IRMS$ . This is the relationship used to calculate the active power in the ADE7758 for each phase.

The instantaneous power signal  $p(t)$  is generated by multiplying the current and voltage signals in each phase. The dc component of the instantaneous power signal in each phase (A, B, and C) is then extracted by LPF2 (the low-pass filter) to obtain the average active power information on each phase. Figure 64 shows this process. The active power of each phase accumulates in the corresponding 16-bit watt-hour register (AWATTHR, BWATTHR, or CWATTHR). The input to each active energy register can be changed depending on the accumulation mode setting (see Table 22).

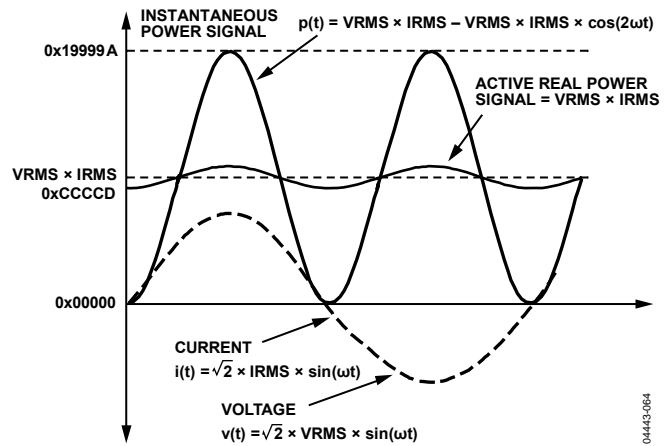


Figure 64. Active Power Calculation

Because LPF2 does not have an ideal brick wall frequency response (see Figure 65), the active power signal has some ripple due to the instantaneous power signal. This ripple is sinusoidal and has a frequency equal to twice the line frequency. Because the ripple is sinusoidal in nature, it is removed when the active power signal is integrated over time to calculate the energy.

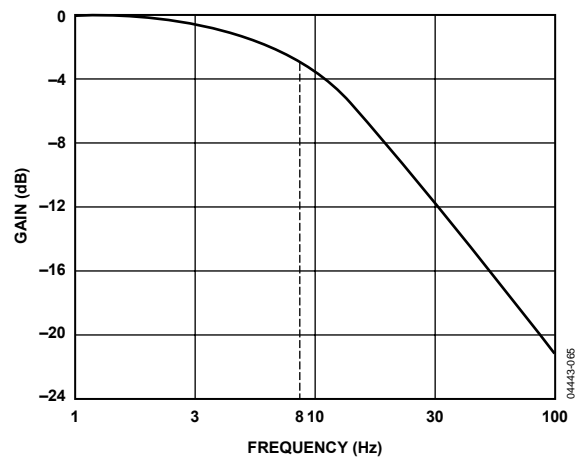


Figure 65. Frequency Response of the LPF Used to Filter Instantaneous Power in Each Phase

**Active Power Gain Calibration**

Note that the average active power result from the LPF output in each phase can be scaled by ±50% by writing to the phase's watt gain register (AWG, BWG, or CWG). The watt gain registers are twos complement, signed registers and have a resolution of 0.024%/LSB. Equation 16 describes mathematically the function of the watt gain registers.

$$\text{Average Power Data} = \text{LPF2 Output} \times \left( 1 + \frac{\text{Watt Gain Register}}{2^{12}} \right) \quad (16)$$

The output is scaled by –50% by writing 0x800 to the watt gain registers and increased by +50% by writing 0x7FF to them. These registers can be used to calibrate the active power (or energy) calculation in the ADE7758 for each phase.

**Active Power Offset Calibration**

The ADE7758 also incorporates a watt offset register on each phase (AWATTOS, BWATTOS, and CWATTOS). These are signed twos complement, 12-bit registers that are used to remove offsets in the active power calculations. An offset can exist in the power calculation due to crosstalk between channels on the PCB or in the chip itself. The offset calibration allows the contents of the active power register to be maintained at 0 when no power is being consumed. One LSB in the active power offset register is equivalent to 1/16 LSB in the active power multiplier output. At full-scale input, if the output from the multiplier is 0xCCCCD (838,861d), then 1 LSB in the LPF2 output is equivalent to 0.0075% of measurement error at 60 dB down from full scale on the current channel. At –60 dB down on full scale (the input signal level is 1/1000 of full-scale signal inputs), the average word value from LPF2 is 838.861 (838,861/1000). One LSB is equivalent to 1/838.861/16 × 100% = 0.0075% of the measured value. The active power offset register has a correction resolution equal to 0.0075% at –60 dB.

**Sign of Active Power Calculation**

Note that the average active power is a signed calculation. If the phase difference between the current and voltage waveform is more than 90°, the average power becomes negative. Negative power indicates that energy is being placed back on the grid. The ADE7758 has a sign detection circuitry for active power calculation.

The REVPAP bit (Bit 17) in the interrupt status register is set if the average power from any one of the phases changes sign. The phases monitored are selected by TERMSEL bits in the COMPMODE register (see Table 21). The TERMSEL bits are also used to select which phases are included in the APCF and VARCF pulse outputs. If the REVPAP bit is set in the mask register, the  $\overline{\text{IRQ}}$  logic output goes active low (see the Interrupts section). Note that this bit is set whenever there are sign changes, that is, the REVPAP bit is set for both a positive-to-negative change or a negative-to-positive change of the sign bit. The response time of this bit is approximately 176 ms for a full-scale signal, which has an average value of 0xCCCCD at the low pass filter output. For smaller inputs, the time is longer.

$$\text{Response Time} \cong 160 \text{ ms} + \left[ \frac{2^{25}}{\text{Average Value}} \right] \times \frac{4}{\text{CLKIN}} \quad (17)$$

The APCFNUM [15:13] indicate reverse power on each of the individual phases. Bit 15 is set if the sign of the power on Phase A is negative, Bit 14 for Phase B, and Bit 13 for Phase C.

**No-Load Threshold**

The ADE7758 has an internal no-load threshold on each phase. The no-load threshold can be activated by setting the NOLOAD bit (Bit 7) of the COMPMODE register. If the active power falls below 0.005% of full-scale input, the energy is not accumulated in that phase. As stated, the average multiplier output with full-scale input is 0xCCCCD. Therefore, if the average multiplier output falls below 0x2A, the power is not accumulated to avoid creep in the meter. The no-load threshold is implemented only on the active energy accumulation. The reactive and apparent energies do not have the no-load threshold option.

**Active Energy Calculation**

As previously stated, power is defined as the rate of energy flow. This relationship can be expressed mathematically as

$$\text{Power} = \frac{d\text{Energy}}{dt} \quad (18)$$

Conversely, Energy is given as the integral of power.

$$\text{Energy} = \int p(t)dt \quad (19)$$

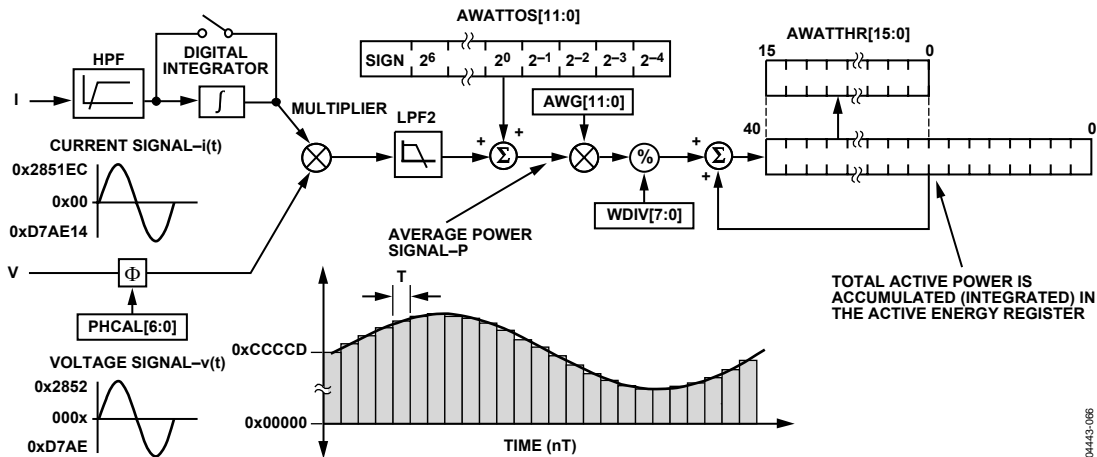


Figure 66. ADE7758 Active Energy Accumulation

The ADE7758 achieves the integration of the active power signal by continuously accumulating the active power signal in the internal 41-bit energy registers. The watt-hr registers (AWATTHR, BWATTHR, and CWATTHR) represent the upper 16 bits of these internal registers. This discrete time accumulation or summation is equivalent to integration in continuous time. Equation 20 expresses the relationship.

$$Energy = \int p(t)dt = \lim_{T \rightarrow 0} \left\{ \sum_{n=0}^{\infty} p(nT) \times T \right\} \quad (20)$$

where:

$n$  is the discrete time sample number.

$T$  is the sample period.

Figure 66 shows a signal path of this energy accumulation. The average active power signal is continuously added to the internal active energy register. This addition is a signed operation. Negative energy is subtracted from the active energy register. Note the values shown in Figure 66 are the nominal full-scale values, that is, the voltage and current inputs at the corresponding phase are at their full-scale input level. The average active power is divided by the content of the watt divider register before it is added to the corresponding watt-hr accumulation registers. When the value in the WDIV[7:0] register is 0 or 1, active power is accumulated without division. WDIV is an 8-bit unsigned register that is useful to lengthen the time it takes before the watt-hr accumulation registers overflow.

Figure 67 shows the energy accumulation for full-scale signals (sinusoidal) on the analog inputs. The three displayed curves show the minimum time it takes for the watt-hr accumulation register to overflow when the watt gain register of the corresponding phase equals to 0x7FF, 0x000, and 0x800. The watt gain registers are used to carry out a power calibration in the ADE7758. As shown, the fastest integration time occurs when the watt gain registers are set to maximum full scale, that is, 0x7FF.

This is the time it takes before overflow can be scaled by writing to the WDIV register and therefore can be increased by a maximum factor of 255.

Note that the active energy register content can roll over to full-scale negative (0x8000) and continue increasing in value when the active power is positive (see Figure 66). Conversely, if the active power is negative, the energy register would under flow to full-scale positive (0x7FFF) and continue decreasing in value.

By setting the AEHF bit (Bit 0) of the interrupt mask register, the ADE7758 can be configured to issue an interrupt (IRQ) when Bit 14 of any one of the three watt-hr accumulation registers has changed, indicating that the accumulation register is half full (positive or negative).

Setting the RSTREAD bit (Bit 6) of the LCYMODE register enables a read-with-reset for the watt-hr accumulation registers, that is, the registers are reset to 0 after a read operation.

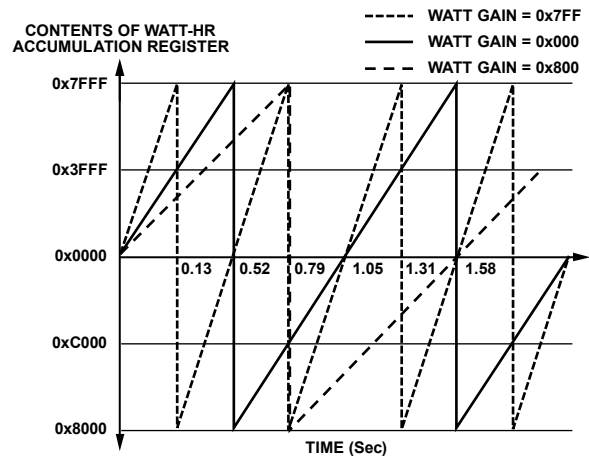


Figure 67. Energy Register Roll-Over Time for Full-Scale Power (Minimum and Maximum Power Gain)

**Integration Time Under Steady Load**

The discrete time sample period (T) for the accumulation register is 0.4 μs (4/CLKIN). With full-scale sinusoidal signals on the analog inputs and the watt gain registers set to 0x000, the average word value from each LPF2 is 0xCCCCD (see Figure 64 and Figure 66). The maximum value that can be stored in the watt-hr accumulation register before it overflows is 2<sup>15</sup> – 1 or 0x7FFF. Because the average word value is added to the internal register, which can store 2<sup>40</sup> – 1 or 0xFF, FFFF, FFFF before it overflows, the integration time under these conditions with WDIV = 0 is calculated as

$$Time = \frac{0xFF, FFFF, FFFF}{0xCCCCD} \times 0.4 \mu s = 0.524 \text{ sec} \quad (21)$$

When WDIV is set to a value different from 0, the time before overflow is scaled accordingly as shown in Equation 22.

$$Time = Time (WDIV = 0) \times WDIV[7:0] \quad (22)$$

**Energy Accumulation Mode**

The active power accumulated in each watt-hr accumulation register (AWATTHR, BWATTHR, or CWATTHR) depends on the configuration of the CONSEL bits in the COMPMODE register (Bit 0 and Bit 1). The different configurations are described in Table 10.

**Table 10. Inputs to Watt-Hr Accumulation Registers**

CONSEL[1, 0]	AWATTHR	BWATTHR	CWATTHR
00	VA × IA	VB × IB	VC × IC
01	VA × (IA – IB)	0	VC × (IC – IB)
10	VA × (IA – IB)	0	VC × IC
11	Reserved	Reserved	Reserved

The contents of the watt-hr accumulation registers are affected by both the current gain register (IGAIN) and the watt gain register of the corresponding phase. IGAIN should not be used when using Mode 0 of CONSEL, COMPMODE[1:0].

Depending on the poly phase meter service, the appropriate formula should be chosen to calculate the active energy. The American ANSI C12.10 Standard defines the different configurations of the meter.

Table 11 describes which mode should be chosen in these different configurations.

**Table 11. Meter Form Configuration**

ANSI Meter Form		CONSEL (d)	TERMSEL (d)
5S/13S	3-Wire Delta	0	3, 5, or 6
6S/14S	4-Wire Wye	1	7
8S/15S	4-Wire Delta	2	7
9S/16S	4-Wire Wye	0	7

Different gain calibration parameters are offered in the ADE7758 to cover the calibration of the meter in different configurations. It should be noted that in CONSEL Mode 0d, the IGAIN and WGAIN registers have the same effect on the end result. However, changing IGAIN also changes all other calculations that use the current waveform. In other words, changing IGAIN changes the active, reactive, and apparent energy, as well as the rms current calculation results. IGAIN should not be used when using Mode 0 of CONSEL COMPMODE[1:0].

**Active Power Frequency Output**

Pin 1 (APCF) of the ADE7758 provides frequency output for the total active power. After initial calibration during manufacturing, the manufacturer or end customer often verifies the energy meter calibration. One convenient way to verify the meter calibration is for the manufacturer to provide an output frequency that is proportional to the energy or active power under steady load conditions. This output frequency can provide a simple, single-wire, optically isolated interface to external calibration equipment. Figure 68 illustrates the energy-to-frequency conversion in the ADE7758.

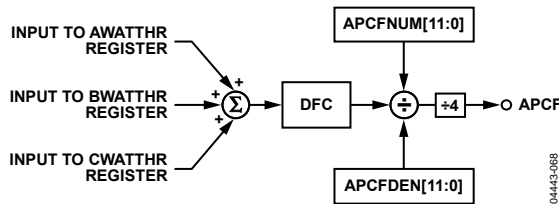


Figure 68. Active Power Frequency Output

A digital-to-frequency converter (DFC) is used to generate the APCF pulse output from the total active power. The TERMSEL bits (Bit 2 to Bit 4) of the COMPMODE register can be used to select which phases to include in the total power calculation. Setting Bit 2, Bit 3, and Bit 4 includes the input to the AWATTHR, BWATTHR, and CWATTHR registers in the total active power calculation. The total active power is signed addition. However, setting the ABS bit (Bit 5) in the COMPMODE register enables the absolute-only mode; that is, only the absolute value of the active power is considered.

The output from the DFC is divided down by a pair of frequency division registers before being sent to the APCF pulse output. Namely, APCFDEN/APCFNUM pulses are needed at the DFC output before the APCF pin outputs a pulse. Under steady load conditions, the output frequency is directly proportional to the total active power. The pulse width of APCF is 64/CLKIN if APCFNUM and APCFDEN are both equal. If APCFDEN is greater than APCFNUM, the pulse width depends on APCFDEN. The pulse width in this case is  $T \times (APCFDEN/2)$ , where T is the period of the APCF pulse and APCFDEN/2 is rounded to the nearest whole number. An exception to this is when the period is greater than 180 ms. In this case, the pulse width is fixed at 90 ms.

# ADE7758

The maximum output frequency (APCFNUM = 0x00 and APCFDEN = 0x00) with full-scale ac signals on one phase is approximately 16 kHz.

The ADE7758 incorporates two registers to set the frequency of APCF (APCFNUM[11:0] and APCFDEN[11:0]). These are unsigned 12-bit registers that can be used to adjust the frequency of APCF by  $1/2^{12}$  to 1 with a step of  $1/2^{12}$ . For example, if the output frequency is 1.562 kHz while the contents of APCFDEN are 0 (0x000), then the output frequency can be set to 6.103 Hz by writing 0xFF to the APCFDEN register.

If 0 were written to any of the frequency division registers, the divider would use 1 in the frequency division. In addition, the ratio APCFNUM/APCFDEN should be set not greater than 1 to ensure proper operation. In other words, the APCF output frequency cannot be higher than the frequency on the DFC output.

The output frequency has a slight ripple at a frequency equal to  $2 \times$  the line frequency. This is due to imperfect filtering of the instantaneous power signal to generate the active power signal (see the Active Power Calculation section). Equation 14 gives an expression for the instantaneous power signal. This is filtered by LPF2, which has a magnitude response given by Equation 23.

$$H(f) = \frac{1}{\sqrt{1 + \frac{f^2}{8^2}}} \quad (23)$$

The active power signal (output of the LPF2) can be rewritten as

$$p(t) = VRMS \times IRMS - \left[ \frac{VRMS \times IRMS}{\sqrt{1 + \frac{(2f_1)^2}{8^2}}} \right] \times \cos(4\pi f_1 t) \quad (24)$$

where  $f_1$  is the line frequency, for example, 60 Hz.

From Equation 24,  $E(t)$  equals

$$VRMS \times IRMS \times t - \left[ \frac{VRMS \times IRMS}{4\pi f_1 t \sqrt{1 + \frac{(2f_1)^2}{8^2}}} \right] \times \cos(4\pi f_1 t) \quad (25)$$

From Equation 25, it can be seen that there is a small ripple in the energy calculation due to the  $\sin(2\omega t)$  component (see Figure 69). The ripple gets larger with larger loads. Choosing a lower output frequency for APCF during calibration by using a large APCFDEN value and keeping APCFNUM relatively small can significantly reduce the ripple. Averaging the output frequency over a longer period achieves the same results.

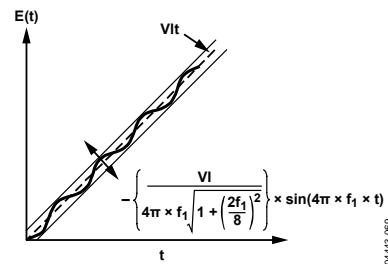
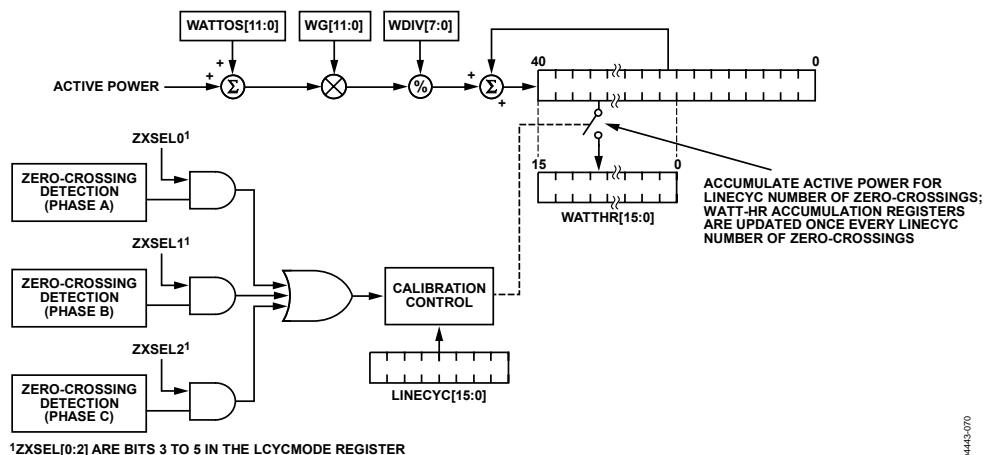


Figure 69. Output Frequency Ripple

## Line Cycle Active Energy Accumulation Mode

The ADE7758 is designed with a special energy accumulation mode that simplifies the calibration process. By using the on-chip, zero-crossing detection, the ADE7758 updates the watt-hr accumulation registers after an integer number of zero crossings (see Figure 70). The line-active energy accumulation mode for watt-hr accumulation is activated by setting the LWATT bit (Bit 0) of the LCYCMODE register. The total energy accumulated over an integer number of half-line cycles is written to the watt-hr accumulation registers after the LINECYC number of zero crossings is detected. When using the line cycle accumulation mode, the RSTREAD bit (Bit 6) of the LCYCMODE register should be set to Logic 0.



<sup>1</sup>ZXSEL[0:2] ARE BITS 3 TO 5 IN THE LCYCMODE REGISTER

Figure 70. ADE7758 Line Cycle Active Energy Accumulation Mode

Phase A, Phase B, and Phase C zero crossings are, respectively, included when counting the number of half-line cycles by setting ZXSEL[0:2] bits (Bit 3 to Bit 5) in the LCYCMODE register. Any combination of the zero crossings from all three phases can be used for counting the zero crossing. Only one phase should be selected at a time for inclusion in the zero crossings count during calibration (see the Calibration section).

The number of zero crossings is specified by the LINECYC register. LINECYC is an unsigned 16-bit register. The ADE7758 can accumulate active power for up to 65535 combined zero crossings. Note that the internal zero-crossing counter is always active. By setting the LWATT bit, the first energy accumulation result is, therefore, incorrect. Writing to the LINECYC register when the LWATT bit is set resets the zero-crossing counter, thus ensuring that the first energy accumulation result is accurate.

At the end of an energy calibration cycle, the LENERGY bit (Bit 12) in the STATUS register is set. If the corresponding mask bit in the interrupt mask register is enabled, the  $\overline{\text{IRQ}}$  output also goes active low; thus, the  $\overline{\text{IRQ}}$  can also be used to signal the end of a calibration.

Because active power is integrated on an integer number of half-line cycles in this mode, the sinusoidal component is reduced to 0, eliminating any ripple in the energy calculation. Therefore, total energy accumulated using the line-cycle accumulation mode is

$$E(t) = VRMS \times IRMS \times t \quad (26)$$

where  $t$  is the accumulation time.

Note that line cycle active energy accumulation uses the same signal path as the active energy accumulation. The LSB size of these two methods is equivalent. Using the line cycle accumulation to calculate the kWh/LSB constant results in a value that can be applied to the WATTHR registers when the line accumulation mode is not selected (see the Calibration section).

### REACTIVE POWER CALCULATION

A load that contains a reactive element (inductor or capacitor) produces a phase difference between the applied ac voltage and the resulting current. The power associated with reactive elements is called reactive power, and its unit is VAR. Reactive power is defined as the product of the voltage and current waveforms when one of these signals is phase shifted by 90°.

Equation 30 gives an expression for the instantaneous reactive power signal in an ac system when the phase of the current channel is shifted by +90°.

$$v(t) = \sqrt{2} V \sin(\omega t - \theta) \quad (27)$$

$$i(t) = \sqrt{2} I \sin(\omega t) \quad (28)$$

$$i'(t) = \sqrt{2} I \sin\left(\omega t + \frac{\pi}{2}\right)$$

where:

$v$  = rms voltage.

$i$  = rms current.

$\theta$  = total phase shift caused by the reactive elements in the load.

Then the instantaneous reactive power  $q(t)$  can be expressed as

$$q(t) = v(t) \times i'(t) \quad (29)$$

$$q(t) = VI \cos\left(-\theta - \frac{\pi}{2}\right) - VI \cos\left(2\omega t - \theta - \frac{\pi}{2}\right)$$

where  $i'(t)$  is the current waveform phase shifted by 90°.

Note that  $q(t)$  can be rewritten as

$$q(t) = VI \sin(\theta) + VI \sin(2\omega t - \theta) \quad (30)$$

The average reactive power over an integral number of line cycles ( $n$ ) is given by the expression in Equation 31.

$$Q = \frac{1}{nT} \int_0^{nT} q(t) dt = V \times I \times \sin(\theta) \quad (31)$$

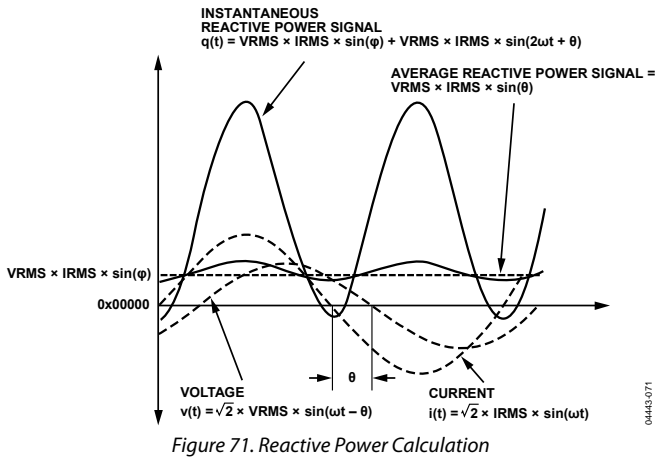
where:

$T$  is the period of the line cycle.

$Q$  is referred to as the average reactive power. The instantaneous reactive power signal  $q(t)$  is generated by multiplying the voltage signals and the 90° phase-shifted current in each phase.

The dc component of the instantaneous reactive power signal in each phase (A, B, and C) is then extracted by a low-pass filter to obtain the average reactive power information on each phase. This process is illustrated in Figure 71. The reactive power of each phase is accumulated in the corresponding 16-bit VAR-hour register (AVARHR, BVARHR, or CVARHR). The input to each reactive energy register can be changed depending on the accumulation mode setting (see Table 21).

The frequency response of the LPF in the reactive power signal path is identical to that of the LPF2 used in the average active power calculation (see Figure 65).



The low-pass filter is nonideal, so the reactive power signal has some ripple. This ripple is sinusoidal and has a frequency equal to  $2 \times$  the line frequency. Because the ripple is sinusoidal in nature, it is removed when the reactive power signal is integrated over time to calculate the reactive energy.

The phase-shift filter has  $-90^\circ$  phase shift when the integrator is enabled and  $+90^\circ$  phase shift when the integrator is disabled. In addition, the filter has a nonunity magnitude response. Because the phase-shift filter has a large attenuation at high frequency, the reactive power is primarily for the calculation at line frequency. The effect of harmonics is largely ignored in the reactive power calculation. Note that because of the magnitude characteristic of the phase shifting filter, the LSB weight of the reactive power calculation is slightly different from that of the active power calculation (see the Energy Registers Scaling section). The ADE7758 uses the line frequency of the phase selected in the `FREQSEL[1:0]` bits of the `MMODE[1:0]` to compensate for attenuation of the reactive energy phase shift filter over frequency (see the Period Measurement section).

### Reactive Power Gain Calibration

The average reactive power from the LPF output in each phase can be scaled by  $\pm 50\%$  by writing to the phase's VAR gain register (AVARG, BVAR, or CVARG). The VAR gain registers are two complement, signed registers and have a resolution of  $0.024\%/LSB$ . The function of the VAR gain registers is expressed by

$$\text{Average Reactive Power} = \text{LPF2 Output} \times \left( 1 + \frac{\text{VAR Gain Register}}{2^{12}} \right) \quad (32)$$

The output is scaled by  $-50\%$  by writing `0x800` to the VAR gain registers and increased by  $+50\%$  by writing `0x7FF` to them. These registers can be used to calibrate the reactive power (or energy) calculation in the ADE7758 for each phase.

### Reactive Power Offset Calibration

The ADE7758 incorporates a VAR offset register on each phase (AVAROS, BVAROS, and CVAROS). These are signed two's complement, 12-bit registers that are used to remove offsets in the reactive power calculations. An offset can exist in the power calculation due to crosstalk between channels on the PCB or in the chip itself. The offset calibration allows the contents of the reactive power register to be maintained at 0 when no reactive power is being consumed. The offset registers' resolution is the same as the active power offset registers (see the Apparent Power Offset Calibration section).

### Sign of Reactive Power Calculation

Note that the average reactive power is a signed calculation. As stated previously, the phase shift filter has  $-90^\circ$  phase shift when the integrator is enabled and  $+90^\circ$  phase shift when the integrator is disabled.

Table 12 summarizes the relationship between the phase difference between the voltage and the current and the sign of the resulting VAR calculation.

The ADE7758 has a sign detection circuit for the reactive power calculation. The `REVPRP` bit (Bit 18) in the interrupt status register is set if the average reactive power from any one of the phases changes. The phases monitored are selected by `TERMSEL` bits in the `COMPmode` register (see Table 21). If the `REVPRP` bit is set in the mask register, the `IRQ` logic output goes active low (see the Interrupts section). Note that this bit is set whenever there is a sign change; that is, the bit is set for either a positive-to-negative change or a negative-to-positive change of the sign bit. The response time of this bit is approximately 176 ms for a full-scale signal, which has an average value of `0xCCCCD` at the low-pass filter output. For smaller inputs, the time is longer.

$$\text{Response Time} \cong 160 \text{ ms} + \left[ \frac{2^{25}}{\text{Average Value}} \right] \times \frac{4}{\text{CLKIN}} \quad (33)$$

**Table 12. Sign of Reactive Power Calculation**

$\Phi^1$	Integrator	Sign of Reactive Power
Between 0 to $+90$	Off	Positive
Between $-90$ to 0	Off	Negative
Between 0 to $+90$	On	Positive
Between $-90$ to 0	On	Negative

<sup>1</sup>  $\Phi$  is defined as the phase angle of the voltage signal minus the current signal; that is,  $\Phi$  is positive if the load is inductive and negative if the load is capacitive.

**Reactive Energy Calculation**

Reactive energy is defined as the integral of reactive power.

$$Reactive\ Energy = \int q(t) dt \tag{34}$$

Similar to active power, the ADE7758 achieves the integration of the reactive power signal by continuously accumulating the reactive power signal in the internal 41-bit accumulation registers. The VAR-hr registers (AVARHR, BVARHR, and CVARHR) represent the upper 16 bits of these internal registers. This discrete time accumulation or summation is equivalent to integration in continuous time. Equation 35 expresses the relationship

$$Reactive\ Energy = \int q(t) dt = \lim_{T \rightarrow 0} \left\{ \sum_{n=0}^{\infty} q(nT) \times T \right\} \tag{35}$$

where:

*n* is the discrete time sample number.

*T* is the sample period.

Figure 72 shows the signal path of the reactive energy accumulation. The average reactive power signal is continuously added to the internal reactive energy register. This addition is a signed operation. Negative energy is subtracted from the reactive energy register. The average reactive power is divided by the content of the VAR divider register before it is added to the corresponding VAR-hr accumulation registers. When the value in the VARDIV[7:0] register is 0 or 1, the reactive power is accumulated without any division.

VARDIV is an 8-bit unsigned register that is useful to lengthen the time it takes before the VAR-hr accumulation registers overflow.

Similar to reactive power, the fastest integration time occurs when the VAR gain registers are set to maximum full scale, that is, 0x7FF. The time it takes before overflow can be scaled by writing to the VARDIV register; and, therefore, it can be increased by a maximum factor of 255.

When overflow occurs, the VAR-hr accumulation registers content can rollover to full-scale negative (0x8000) and continue increasing in value when the reactive power is positive. Conversely, if the reactive power is negative, the VAR-hr accumulation registers content can roll over to full-scale positive (0x7FFF) and continue decreasing in value.

By setting the REHF bit (Bit 1) of the interrupt mask register, the ADE7758 can be configured to issue an interrupt (IRQ) when Bit 14 of any one of the three VAR-hr accumulation registers has changed, indicating that the accumulation register is half full (positive or negative).

Setting the RSTREAD bit (Bit 6) of the LCYMODE register enables a read-with-reset for the VAR-hr accumulation registers; that is, the registers are reset to 0 after a read operation.

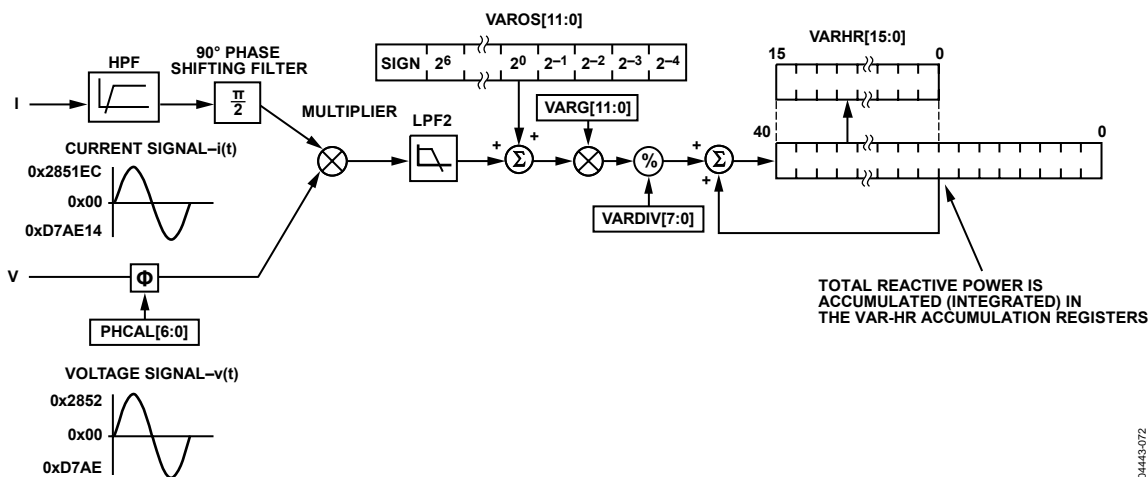


Figure 72. ADE7758 Reactive Energy Accumulation

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## Integration Time Under Steady Load

The discrete time sample period (T) for the accumulation register is 0.4 μs (4/CLKIN). With full-scale sinusoidal signals on the analog inputs, a 90° phase difference between the voltage and the current signal (the largest possible reactive power), and the VAR gain registers set to 0x000, the average word value from each LPF2 is 0xCCCCD.

The maximum value that can be stored in the reactive energy register before it overflows is 2<sup>15</sup> – 1 or 0x7FFF. Because the average word value is added to the internal register, which can store 2<sup>40</sup> – 1 or 0xFF, FFFF, FFFF before it overflows, the integration time under these conditions with VARDIV = 0 is calculated as

$$Time = \frac{0xFF, FFFF, FFFF}{0xCCCCD} \times 0.4 \mu s = 0.5243 \text{ sec} \quad (36)$$

When VARDIV is set to a value different from 0, the time before overflow are scaled accordingly as shown in Equation 37.

$$Time = Time(VARDIV = 0) \times VARDIV \quad (37)$$

## Energy Accumulation Mode

The reactive power accumulated in each VAR-hr accumulation register (AVARHR, BVARHR, or CVARHR) depends on the configuration of the CONSEL bits in the COMPMODE register (Bit 0 and Bit 1). The different configurations are described in Table 13. Note that IA'/IB'/IC' are the current phase-shifted current waveform.

**Table 13. Inputs to VAR-Hr Accumulation Registers**

CONSEL[1, 0]	AVARHR	BVARHR	CVARHR
00	VA × IA'	VB × IB	VC × IC'
01	VA (IA' – IB')	0	VC (IC' – IB')
10	VA (IA' – IB')	0	VC × IC'
11	Reserved	Reserved	Reserved

The contents of the VAR-hr accumulation registers are affected by both the current gain register (IGAIN) and the VAR gain register of the corresponding phase. IGAIN should not be used when using Mode 0 of CONSEL COMPMODE[1:0].

## Reactive Power Frequency Output

Pin 17 (VARCF) of the ADE7758 provides frequency output for the total reactive power. Similar to APCF, this pin provides an output frequency that is directly proportional to the total reactive power. The pulse width of VARPCF is 64/CLKIN if VARCFNUM and VARCFDEN are both equal. If VARCFDEN is greater than VARCFNUM, the pulse width depends on VARCFDEN. The pulse width in this case is  $T \times (VARCFDEN/2)$ , where T is the period of the VARCF pulse and VARCFDEN/2 is rounded to the nearest whole number. An exception to this is when the period is greater than 180 ms. In this case, the pulse width is fixed at 90 ms.

A digital-to-frequency converter (DFC) is used to generate the VARCF pulse output from the total reactive power. The TERMSEL bits (Bit 2 to Bit 4) of the COMPMODE register can be used to select which phases to include in the total reactive power calculation. Setting Bit 2, Bit 3, and Bit 4 includes the input to the AVARHR, BVARHR, and CVARHR registers in the total reactive power calculation. The total reactive power is signed addition. However, setting the SAVAR bit (Bit 6) in the COMPMODE register enables absolute value calculation. If the active power of that phase is positive, no change is made to the sign of the reactive power. However, if the sign of the active power is negative in that phase, the sign of its reactive power is inverted before summing and creating VARCF pulses. This mode should be used in conjunction with the absolute value mode for active power (Bit 5 in the COMPMODE register) for APCF pulses.

The effects of setting the ABS and SAVAR bits of the COMPMODE register are as follows when ABS = 1 and SAVAR = 1:

If watt > 0, APCF = Watts, VARCF = +VAR.

If watt < 0, APCF = |Watts|, VARCF = –VAR.

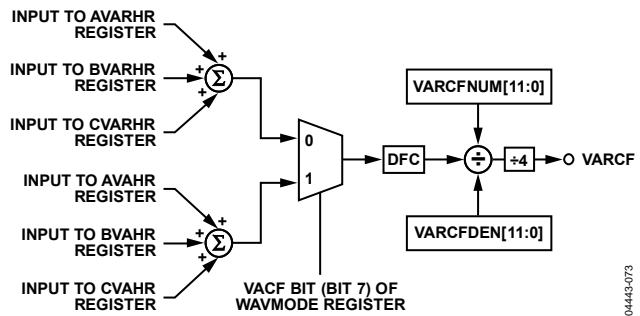


Figure 73. Reactive Power Frequency Output

The output from the DFC is divided down by a pair of frequency division registers before sending to the VARCF pulse output. Namely, VARCFDEN/VARCFNUM pulses are needed at the DFC output before the VARCF pin outputs a pulse. Under steady load conditions, the output frequency is directly proportional to the total reactive power.

Figure 73 illustrates the energy-to-frequency conversion in the ADE7758. Note that the input to the DFC can be selected between the total reactive power and total apparent power. Therefore, the VARCF pin can output frequency that is proportional to the total reactive power or total apparent power. The selection is made by setting the VACF bit (Bit 7) in the WAVMODE register. Setting this bit switches the input to the total apparent power. The default value of this bit is logic low. Therefore, the default output from the VARCF pin is the total reactive power.

All other operations of this frequency output are similar to that of the active power frequency output (see the Active Power Frequency Output section).

**Line Cycle Reactive Energy Accumulation Mode**

The line cycle reactive energy accumulation mode is activated by setting the LVAR bit (Bit 1) in the LCYCMODE register. The total reactive energy accumulated over an integer number of zero crossings is written to the VAR-hr accumulation registers after the LINECYC number of zero crossings is detected. The operation of this mode is similar to watt-hr accumulation (see the Line Cycle Active Energy Accumulation Mode section). When using the line cycle accumulation mode, the RSTREAD bit (Bit 6) of the LCYCMODE register should be set to Logic 0.

**APPARENT POWER CALCULATION**

Apparent power is defined as the amplitude of the vector sum of the active and reactive powers. Figure 74 shows what is typically referred to as the power triangle.

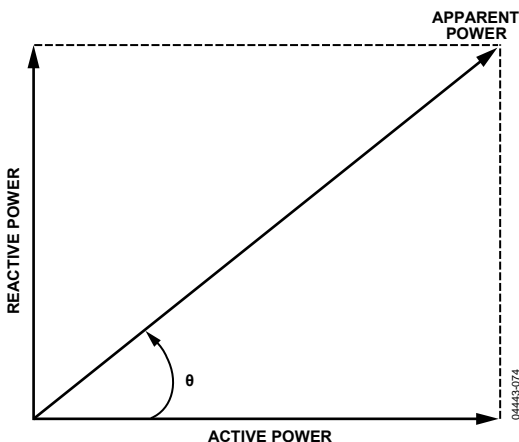


Figure 74. Power Triangle

There are two ways to calculate apparent power: the arithmetical approach or the vectorial method. The arithmetical approach uses the product of the voltage rms value and current rms value to calculate apparent power. Equation 38 describes the arithmetical approach mathematically.

$$S = VRMS \times IRMS \tag{38}$$

where S is the apparent power, and VRMS and IRMS are the rms voltage and current, respectively.

The vectorial method uses the square root of the sum of the active and reactive power, after the two are individually squared. Equation 39 shows the calculation used in the vectorial approach.

$$S = \sqrt{P^2 + Q^2} \tag{39}$$

where:

- S is the apparent power.
- P is the active power.
- Q is the reactive power.

For a pure sinusoidal system, the two approaches should yield the same result. The apparent energy calculation in the ADE7758 uses the arithmetical approach. However, the line cycle energy accumulation mode in the ADE7758 enables energy accumulation between active and reactive energies over a synchronous period, thus the vectorial method can be easily implemented in the external MCU (see the Line Cycle Active Energy Accumulation Mode section).

Note that apparent power is always positive regardless of the direction of the active or reactive energy flows. The rms value of the current and voltage in each phase is multiplied to produce the apparent power of the corresponding phase.

The output from the multiplier is then low-pass filtered to obtain the average apparent power. The frequency response of the LPF in the apparent power signal path is identical to that of the LPF2 used in the average active power calculation (see Figure 65).

**Apparent Power Gain Calibration**

Note that the average active power result from the LPF output in each phase can be scaled by  $\pm 50\%$  by writing to the phase's VAGAIN register (AVAG, BVAG, or CVAG). The VAGAIN registers are two's complement, signed registers and have a resolution of 0.024%/LSB. The function of the VAGAIN registers is expressed mathematically as

$$\begin{aligned} \text{Average Apparent Power} = \\ \text{LPF2 Output} \times \left( 1 + \frac{\text{VAGAIN Register}}{2^{12}} \right) \end{aligned} \tag{40}$$

The output is scaled by  $-50\%$  by writing 0x800 to the VAR gain registers and increased by  $+50\%$  by writing 0x7FF to them. These registers can be used to calibrate the apparent power (or energy) calculation in the ADE7758 for each phase.

**Apparent Power Offset Calibration**

Each rms measurement includes an offset compensation register to calibrate and eliminate the dc component in the rms value (see the Current RMS Calculation section and the Voltage Channel RMS Calculation section). The voltage and current rms values are then multiplied together in the apparent power signal processing. As no additional offsets are created in the multiplication of the rms values, there is no specific offset compensation in the apparent power signal processing. The offset compensation of the apparent power measurement in each phase should be done by calibrating each individual rms measurement (see the Calibration section).

## Apparent Energy Calculation

Apparent energy is defined as the integral of apparent power.

$$\text{Apparent Energy} = \int S(t)dt \quad (41)$$

Similar to active and reactive energy, the ADE7758 achieves the integration of the apparent power signal by continuously accumulating the apparent power signal in the internal 41-bit, unsigned accumulation registers. The VA-hr registers (AVAHR, BVAHR, and CVAHR) represent the upper 16 bits of these internal registers. This discrete time accumulation or summation is equivalent to integration in continuous time. Equation 42 expresses the relationship

$$\text{Apparent Energy} = \int S(t) dt = \lim_{T \rightarrow 0} \left\{ \sum_{n=0}^{\infty} S(nT) \times T \right\} \quad (42)$$

where:

$n$  is the discrete time sample number.

$T$  is the sample period.

Figure 75 shows the signal path of the apparent energy accumulation. The apparent power signal is continuously added to the internal apparent energy register. The average apparent power is divided by the content of the VA divider register before it is added to the corresponding VA-hr accumulation register. When the value in the VADIV[7:0] register is 0 or 1, apparent power is accumulated without any division. VADIV is an 8-bit unsigned register that is useful to lengthen the time it takes before the VA-hr accumulation registers overflow.

Similar to active or reactive power accumulation, the fastest integration time occurs when the VAGAIN registers are set to maximum full scale, that is, 0x7FF. When overflow occurs, the content of the VA-hr accumulation registers can roll over to 0 and continue increasing in value.

By setting the VAEHF bit (Bit 2) of the mask register, the ADE7758 can be configured to issue an interrupt ( $\overline{\text{IRQ}}$ ) when the MSB of any one of the three VA-hr accumulation register has changed, indicating that the accumulation register is half full.

Setting the RSTREAD bit (Bit 6) of the LCYMODE register enables a read-with-reset for the VA-hr accumulation registers; that is, the registers are reset to 0 after a read operation.

## Integration Time Under Steady Load

The discrete time sample period ( $T$ ) for the accumulation register is  $0.4 \mu\text{s}$  ( $4/\text{CLKIN}$ ). With full-scale, 60 Hz sinusoidal signals on the analog inputs and the VAGAIN registers set to 0x000, the average word value from each LPF2 is 0xB9954. The maximum value that can be stored in the apparent energy register before it overflows is  $2^{16} - 1$  or 0xFFFF. As the average word value is first added to the internal register, which can store  $2^{41} - 1$  or 0x1FF, FFFF, FFFF before it overflows, the integration time under these conditions with VADIV = 0 is calculated as

$$\text{Time} = \frac{0x1FF, FFFF, FFFF}{0xB9954} \times 0.4 \mu\text{s} = 1.157 \text{ sec} \quad (43)$$

When VADIV is set to a value different from 0, the time before overflow is scaled accordingly, as shown in Equation 44.

$$\text{Time} = \text{Time}(VADIV = 0) \times VADIV \quad (44)$$

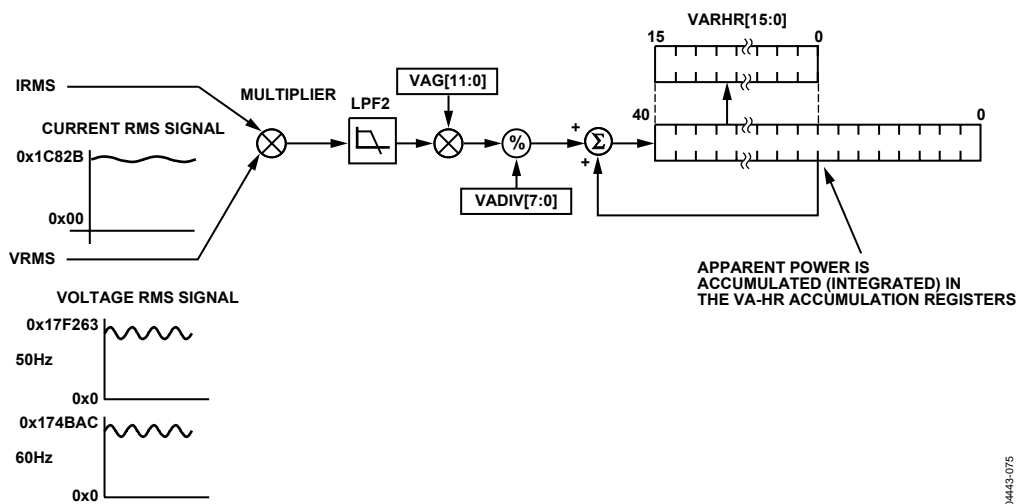


Figure 75. ADE7758 Apparent Energy Accumulation

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**Table 14. Inputs to VA-Hr Accumulation Registers**

CONSEL[1, 0]	AVAHR <sup>1</sup>	BVAHR	CVAHR
00	AVRMS × AIRMS	BVRMS × BIRMS	CVRMS × CIRMS
01	AVRMS × AIRMS	AVRMS + CVRMS/2 × BIRMS	CVRMS × CIRMS
10	AVRMS × AIRMS	BVRMS × BIRMS	CVRMS × CIRMS
11	Reserved	Reserved	Reserved

<sup>1</sup> AVRMS/BVRMS/CVRMS are the rms voltage waveform, and AIRMS/BIRMS/CIRMS are the rms values of the current waveform.

**Energy Accumulation Mode**

The apparent power accumulated in each VA-hr accumulation register (AVAHR, BVAHR, or CVAHR) depends on the configuration of the CONSEL bits in the COMPMODE register (Bit 0 and Bit 1). The different configurations are described in Table 14.

The contents of the VA-hr accumulation registers are affected by both the registers for the current gain (IGAIN) and rms voltage gain (VRMSGAIN), as well as the VAGAIN register of the corresponding phase. IGAIN should not be used when using CONSEL Mode 0, COMPMODE[1:0].

**Apparent Power Frequency Output**

Pin 17 (VARCF) of the ADE7758 provides frequency output for the total apparent power. By setting the VACF bit (Bit 7) of the WAVMODE register, this pin provides an output frequency that is directly proportional to the total apparent power.

A digital-to-frequency converter (DFC) is used to generate the pulse output from the total apparent power. The TERMSEL bits (Bit 2 to Bit 4) of the COMPMODE register can be used to select which phases to include in the total power calculation. Setting Bit 2, Bit 3, and Bit 4 includes the input to the AVAHR, BVAHR, and CVAHR registers in the total apparent power calculation. A pair of frequency divider registers, namely VARCFDEN and VARCFNUM, can be used to scale the output frequency of this pin. Note that either VAR or apparent power can be selected at one time for this frequency output (see the Reactive Power Frequency Output section).

**Line Cycle Apparent Energy Accumulation Mode**

The line cycle apparent energy accumulation mode is activated by setting the LVA bit (Bit 2) in the LCYCMODE register. The total apparent energy accumulated over an integer number of zero crossings is written to the VA-hr accumulation registers after the LINECYC number of zero crossings is detected. The operation of this mode is similar to watt-hr accumulation (see the Line Cycle Active Energy Accumulation Mode section). When using the line cycle accumulation mode, the RSTREAD bit (Bit 6) of the LCYCMODE register should be set to Logic 0.

Note that this mode is especially useful when the user chooses to perform the apparent energy calculation using the vectorial method.

By setting LWATT and LVAR bits (Bit 0 and Bit 1) of the LCYCMODE register, the active and reactive energies are accumulated over the same period. Therefore, the MCU can perform the squaring of the two terms and then take the square root of their sum to determine the apparent energy over the same period.

**ENERGY REGISTERS SCALING**

The ADE7758 provides measurements of active, reactive, and apparent energies that use separate signal paths and filtering for calculation. The differences in the datapaths can result in small differences in LSB weight between the active, reactive, and apparent energy registers. These measurements are internally compensated so that the scaling is nearly one to one. The relationship between the registers is shown in Table 15.

**Table 15. Energy Registers Scaling**

	Frequency	
	60 Hz	50 Hz
<b>Integrator Off</b>		
VAR	1.004 × WATT	1.0054 × WATT
VA	1.00058 × WATT	1.0085 × WATT
<b>Integrator On</b>		
VAR	1.0059 × WATT	1.0064 × WATT
VA	1.00058 × WATT	1.00845 × WATT

**WAVEFORM SAMPLING MODE**

The waveform samples of the current and voltage waveform, as well as the active, reactive, and apparent power multiplier outputs, can all be routed to the WAVEFORM register by setting the WAVSEL[2:0] bits (Bit 2 to Bit 4) in the WAVMODE register. The phase in which the samples are routed is set by setting the PHSEL[1:0] bits (Bit 0 and Bit 1) in the WAVMODE register. All energy calculation remains uninterrupted during waveform sampling. Four output sample rates can be chosen by using Bit 5 and Bit 6 of the WAVMODE register (DTRT[1:0]). The output sample rate can be 26.04 kSPS, 13.02 kSPS, 6.51 kSPS, or 3.25 kSPS (see Table 20).

By setting the WFSM bit in the interrupt mask register to Logic 1, the interrupt request output  $\overline{\text{IRQ}}$  goes active low when a sample is available. The 24-bit waveform samples are transferred from the ADE7758 one byte (8 bits) at a time, with the most significant byte shifted out first.

# ADE7758

The interrupt request output  $\overline{\text{IRQ}}$  stays low until the interrupt routine reads the reset status register (see the Interrupts section).

## CALIBRATION

A reference meter or an accurate source is required to calibrate the ADE7758 energy meter. When using a reference meter, the ADE7758 calibration output frequencies APCF and VARCF are adjusted to match the frequency output of the reference meter under the same load conditions. Each phase must be calibrated separately in this case. When using an accurate source for calibration, one can take advantage of the line cycle accumulation mode and calibrate the three phases simultaneously.

There are two objectives in calibrating the meter: to establish the correct impulses/kW-hr constant on the pulse output and to obtain a constant that relates the LSBs in the energy and rms registers to Watt/VA/VAR hours, amps, or volts. Additionally, calibration compensates for part-to-part variation in the meter design as well as phase shifts and offsets due to the current sensor and/or input networks.

## Calibration Using Pulse Output

The ADE7758 provides a pulsed output proportional to the active power accumulated by all three phases, called APCF. Additionally, the VARCF output is proportional to either the reactive energy or apparent energy accumulated by all three phases. The following section describes how to calibrate the gain, offset, and phase angle using the pulsed output information. The equations are based on the pulse output from the ADE7758 (APCF or VARCF) and the pulse output of the reference meter or  $CF_{\text{EXPECTED}}$ .

Figure 76 shows a flowchart of how to calibrate the ADE7758 using the pulse output. Because the pulse outputs are proportional to the total energy in all three phases, each phase must be calibrated individually. Writing to the registers is fast to reconfigure the part for calibrating a different phase; therefore, Figure 76 shows a method that calibrates all phases at a given test condition before changing the test condition.

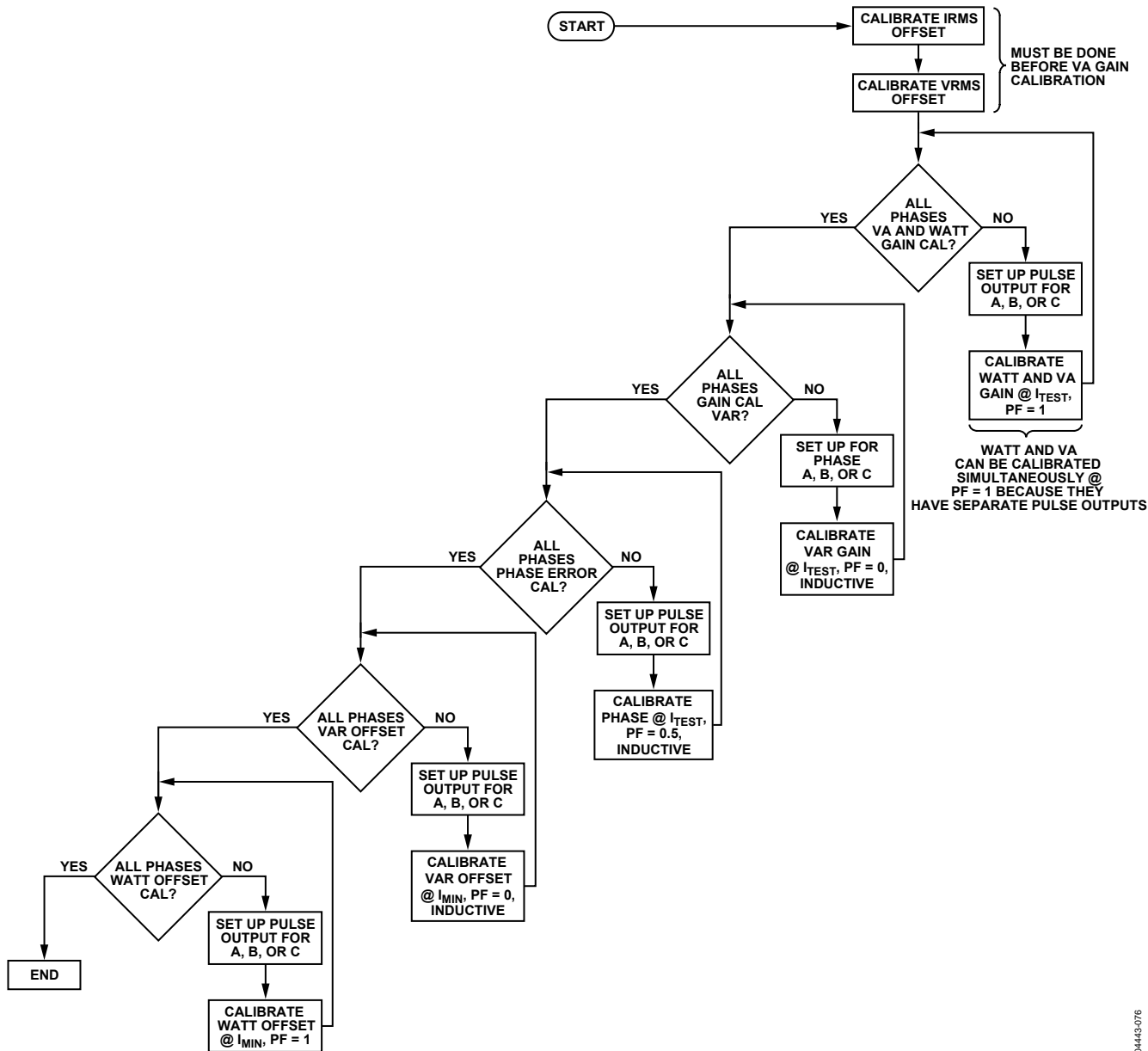


Figure 76. Calibration Using Pulse Output

**Gain Calibration Using Pulse Output**

Gain calibration is used for meter-to-meter gain adjustment, APCF or VARCF output rate calibration, and determining the Wh/LSB, VARh/LSB, and VAh/LSB constant. The registers used for watt gain calibration are APCFNUM (0x45), APCFDEN (0x46), and xWG (0x2A to 0x2C). Equation 50 through Equation 52 show how these registers affect the Wh/LSB constant and the APCF pulses.

For calibrating VAR gain, the registers in Equation 50 through Equation 52 should be replaced by VARCFNUM (0x47), VARCFDEN (0x48), and xVARG (0x2D to 0x2F). For VAGAIN, they should be replaced by VARCFNUM (0x47), VARCFDEN (0x48), and xVAG (0x30 to 0x32).

Figure 77 shows the steps for gain calibration of watts, VA, or VAR using the pulse outputs.

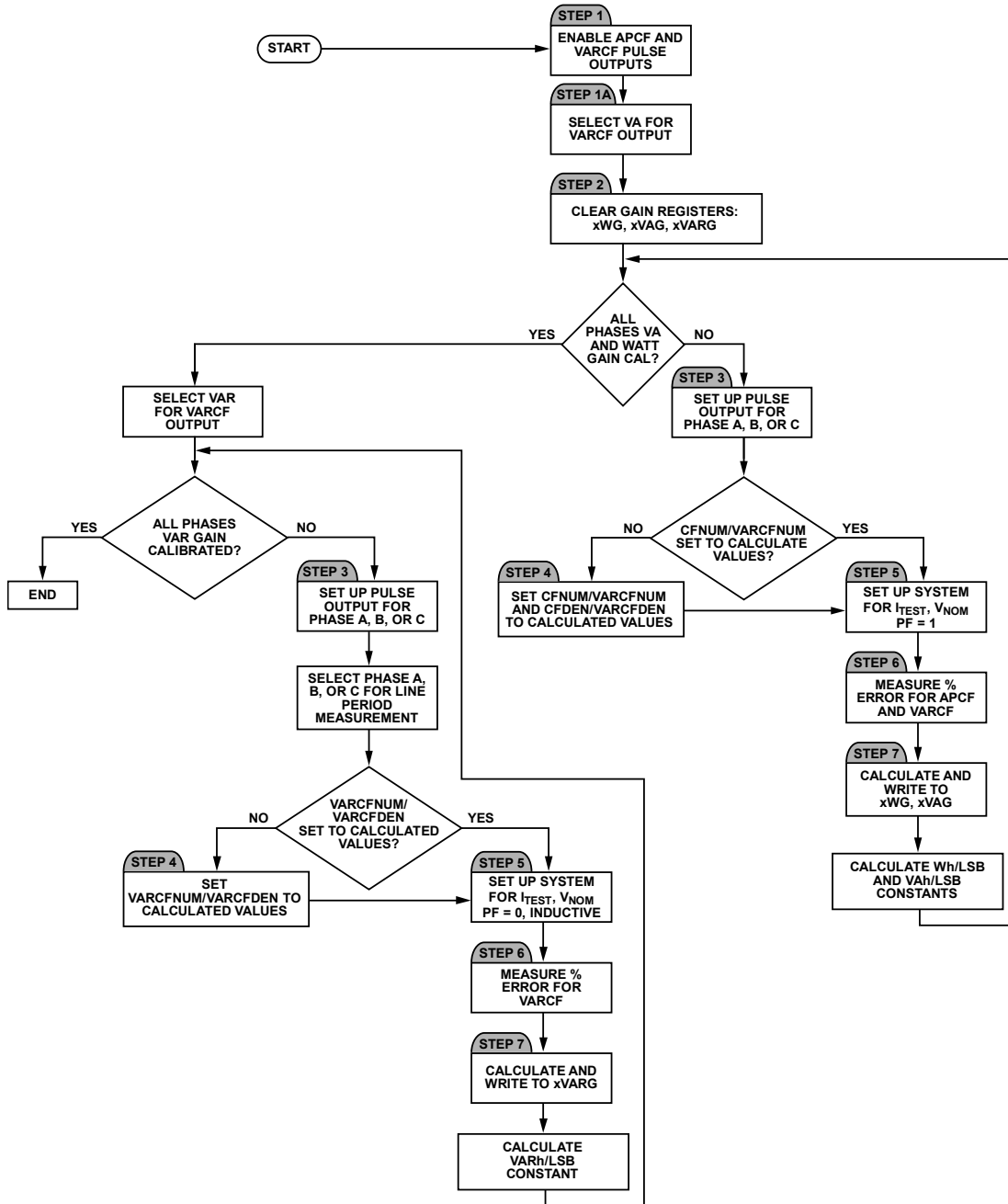


Figure 77. Gain Calibration Using Pulse Output

Step 1: Enable the pulse output by setting Bit 2 of the OPMODE register (0x13) to Logic 0. This bit enables both the APCF and VARCF pulses.

Step 1a: VAR and VA share the VARCF pulse output. WAVMODE[7], Address (0x15), should be set to choose between VAR or VA pulses on the output. Setting the bit to Logic 1 selects VA. The default is Logic 0 or VARCF pulse output.

Step 2: Ensure the xWG/xVARG/xVAG are zero.

Step 3: Disable the Phase B and Phase C contribution to the APCF and VARCF pulses. This is done by the TERMSSEL[2:4] bits of the COMPMODE register (0x16). Setting Bit 2 to Logic 1 and Bit 3 and Bit 4 to Logic 0 allows only Phase A to be included in the pulse outputs. Select Phase A, Phase B, or Phase C for a line period measurement with the FREQSEL[1:0] bits in the MMODE register (0x14). For example, clearing Bit 1 and Bit 0 selects Phase A for line period measurement.

Step 4: Set APCFNUM (0x45) and APCFDEN (0x46) to the calculated value to perform a coarse adjustment on the imp/kWh ratio. For VAR/VA calibration, set VARCFNUM (0x47) and VARCFDEN (0x48) to the calculated value.

The pulse output frequency with one phase at full-scale inputs is approximately 16 kHz. A sample set of meters could be tested to find a more exact value of the pulse output at full scale in the user application.

To calculate the values for APCFNUM/APCFDEN and VARCFNUM/VARCFDEN, use the following formulas:

$$APCF_{NOMINAL} = 16 \text{ kHz} \times \frac{V_{NOM}}{V_{FULLSCALE}} \times \frac{I_{TEST}}{I_{FULLSCALE}} \quad (45)$$

$$APCF_{EXPECTED} = \frac{MC \times I_{TEST} \times V_{NOM}}{1000 \times 3600} \times \cos(\theta) \quad (46)$$

$$APCFDEN = INT\left(\frac{APCF_{NOMINAL}}{APCF_{EXPECTED}}\right) \quad (47)$$

where:

$MC$  is the meter constant.

$I_{TEST}$  is the test current.

$V_{NOM}$  is the nominal voltage at which the meter is tested.

$V_{FULLSCALE}$  and  $I_{FULLSCALE}$  are the values of current and voltage, which correspond to the full-scale ADC inputs of the ADE7758.

$\theta$  is the angle between the current and the voltage channel.

$APCF_{EXPECTED}$  is equivalent to the reference meter output under the test conditions.

$APCFNUM$  is written to 0 or 1.

The equations for calculating the VARCFNUM and VARCFDEN during VAR calibration are similar:

$$VARCF_{EXPECTED} = \frac{MC \times I_{TEST} \times V_{NOM}}{1000 \times 3600} \times \sin(\theta) \quad (48)$$

Because the APCFDEN and VARCFDEN values can be calculated from the meter design, these values can be written to the part automatically during production calibration.

Step 5: Set the test system for  $I_{TEST}$ ,  $V_{NOM}$ , and the unity power factor. For VAR calibration, the power factor should be set to 0 inductive in this step. For watt and VA, the unity power factor should be used. VAGAIN can be calibrated at the same time as WGAIN because VAGAIN can be calibrated at the unity power factor, and both pulse outputs can be measured simultaneously. However, when calibrating VAGAIN at the same time as WGAIN, the rms offsets should be calibrated first (see the Calibration of IRMS and VRMS Offset section).

Step 6: Measure the percent error in the pulse output, APCF and/or VARCF, from the reference meter:

$$\%Error = \frac{APCF - CF_{REF}}{CF_{REF}} \times 100\% \quad (49)$$

where  $CF_{REF} = APCF_{EXPECTED}$  = the pulse output of the reference meter.

Step 7: Calculate xWG adjustment. One LSB change in xWG (12 bits) changes the WATTHR register by 0.0244% and therefore APCF by 0.0244%. The same relationship holds true for VARCF.

$$APCF_{EXPECTED} = APCF_{NOMINAL} \times \frac{APCFNUM[11:0]}{APCFDEN[11:0]} \times \left(1 + \frac{xWG[11:0]}{2^{12}}\right) \quad (50)$$

$$xWG = -\frac{\%Error}{0.0244\%} \quad (51)$$

When APCF is calibrated, the xWATTHR registers have the same Wh/LSB from meter to meter if the meter constant and the APCFNUM/APCFDEN ratio remain the same. The Wh/LSB constant is

$$\frac{Wh}{LSB} = \frac{1}{4 \times \frac{MC}{1000} \times \frac{APCFDEN}{APCFNUM} \times \frac{1}{WDIV}} \quad (52)$$

Return to Step 2 to calibrate Phase B and Phase C gain.

### Example: Watt Gain Calibration of Phase A Using Pulse Output

For this example,  $I_{TEST} = 10 \text{ A}$ ,  $V_{NOM} = 220 \text{ V}$ ,  $V_{FULLSCALE} = 500 \text{ V}$ ,  $I_{FULLSCALE} = 130 \text{ A}$ ,  $MC = 3200 \text{ impulses/kWh}$ , Power Factor = 1, and Frequency = 50 Hz.

Clear APCFNUM (0x45) and write the calculated value to APCFDEN (0x46) to perform a coarse adjustment on the imp/kWh ratio, using Equation 45 through Equation 47.

$$APCF_{NOMINAL} = 16 \text{ kHz} \times \frac{220}{500} \times \frac{10}{130} = 0.542 \text{ kHz}$$

$$APCF_{EXPECTED} = \frac{3200 \times 10 \times 220}{1000 \times 3600} \times \cos(0) = 1.9556 \text{ Hz}$$

$$APCFDEN = INT\left(\frac{542 \text{ Hz}}{1.9556 \text{ Hz}}\right) = 277$$

With Phase A contributing to CF, at  $I_{TEST}$ ,  $V_{NOM}$ , and the unity power factor, the example ADE7758 meter shows 2.058 Hz on the pulse output. This is equivalent to a 5.26% error from the reference meter value using Equation 49.

$$\%Error = \frac{2.058 \text{ Hz} - 1.9556 \text{ Hz}}{1.9556 \text{ Hz}} \times 100\% = 5.26\%$$

The AWG value is calculated to be -216 d using Equation 51, which means the value 0xF28 should be written to AWG.

$$AWG = -\frac{5.26\%}{0.0244\%} = -215.5 = -216 = 0xF28$$

## Phase Calibration Using Pulse Output

The ADE7758 includes a phase calibration register on each phase to compensate for small phase errors. Large phase errors should be compensated by adjusting the antialiasing filters. The ADE7758's phase calibration is a time delay with different weights in the positive and negative direction (see the Phase Compensation section). Because a current transformer is a source of phase error, a fixed nominal value can be decided on to load into the xPHCAL registers at power-up. During calibration, this value can be adjusted for CT-to-CT error. Figure 78 shows the steps involved in calibrating the phase using the pulse output.

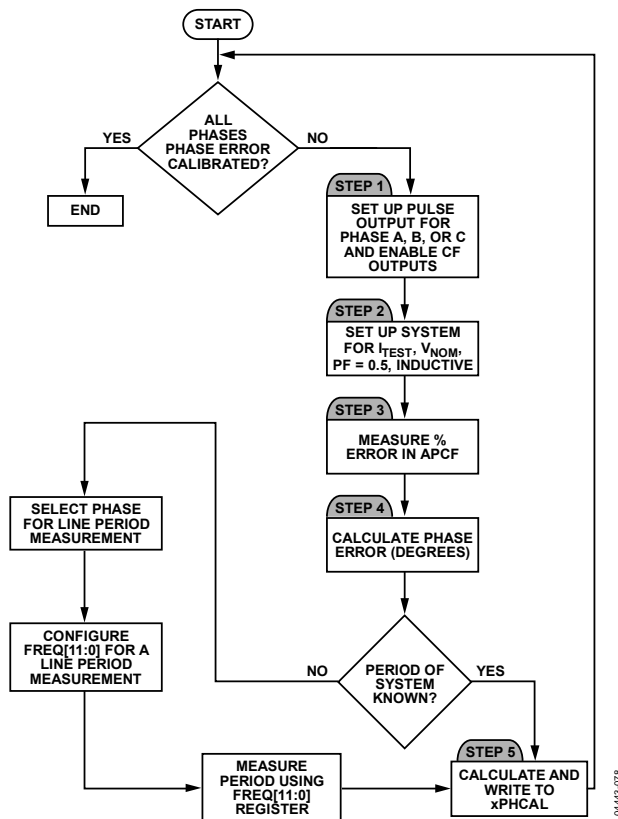


Figure 78. Phase Calibration Using Pulse Output

Step 1: Step 1 and Step 3 from the gain calibration should be repeated to configure the ADE7758 pulse output. Ensure the xPHCAL registers are zero.

Step 2: Set the test system for  $I_{TEST}$ ,  $V_{NOM}$ , and 0.5 power factor inductive.

Step 3: Measure the percent error in the pulse output, APCF, from the reference meter using Equation 49.

Step 4: Calculate the Phase Error in degrees by

$$Phase\ Error(^{\circ}) = -\text{Arcsin}\left(\frac{\%Error}{100\% \times \sqrt{3}}\right) \quad (53)$$

Step 5: Calculate xPHCAL.

$$xPHCAL =$$

$$Phase\ Error \times \frac{1}{PHCAL\_LSB\_Weight} \times \frac{1}{Line\ Period(s)} \times \frac{1}{360^{\circ}} \quad (54)$$

where  $PHCAL\_LSB\_Weight$  is 1.2  $\mu\text{s}$  if the %Error is negative or 2.4  $\mu\text{s}$  if the %Error is positive (see the Phase Compensation section).

If it is not known, the line period is available in the ADE7758's frequency register,  $FREQ$  (0x10). To configure line period measurement, select the phase for period measurement in the  $MMODE[1:0]$  and set  $LCYCMODE[7]$ . Equation 55 shows how to determine the value that needs to be written to xPHCAL using the period register measurement.

$$xPHCAL =$$

$$Phase\ Error \times \frac{9.6\ \mu\text{s}}{PHCAL\_LSB\_Weight} \times \frac{FREQ[11:0]}{360^{\circ}} \quad (55)$$

## Example: Phase Calibration of Phase A Using Pulse Output

For this example,  $I_{TEST} = 10\text{ A}$ ,  $V_{NOM} = 220\text{ V}$ ,  $V_{FULLSCALE} = 500\text{ V}$ ,  $I_{FULLSCALE} = 130\text{ A}$ ,  $MC = 3200\text{ impulses/kWh}$ , Power Factor = 0.5 inductive, and Frequency = 50 Hz.

With Phase A contributing to CF, at  $I_{TEST}$ ,  $V_{NOM}$ , and 0.5 inductive power factor, the example ADE7758 meter shows 0.9668 Hz on the pulse output. This is equivalent to  $-1.122\%$  error from the reference meter value using Equation 49.

The  $Phase\ Error$  in degrees using Equation 53 is  $0.3713^{\circ}$ .

$$Phase\ Error(^{\circ}) = -\text{Arcsin}\left(\frac{-1.122\%}{100\% \times \sqrt{3}}\right) = 0.3713^{\circ}$$

If at 50 Hz the  $FREQ$  register = 2083d, the value that should be written to  $APHCAL$  is 17d, or 0x11 using Equation 55. Note that a  $PHCAL\_LSB\_Weight$  of 1.2  $\mu\text{s}$  is used because the %Error is negative.

$$APHCAL = 0.3713^{\circ} \times \frac{9.6\ \mu\text{s}}{1.2\ \mu\text{s}} \times \frac{2083}{360^{\circ}} = 17.19 = 17 = 0x11$$

## Power Offset Calibration Using Pulse Output

Power offset calibration should be used for outstanding performance over a wide dynamic range (1000:1). Calibration of the power offset is done at or close to the minimum current where the desired accuracy is required.

The ADE7758 has power offset registers for watts and VAR ( $xWATTOS$  and  $xVAROS$ ). Offsets in the VA measurement are compensated by adjusting the rms offset registers (see the Calibration of IRMS and VRMS Offset section). Figure 79 shows the steps to calibrate the power offsets using the pulse outputs.

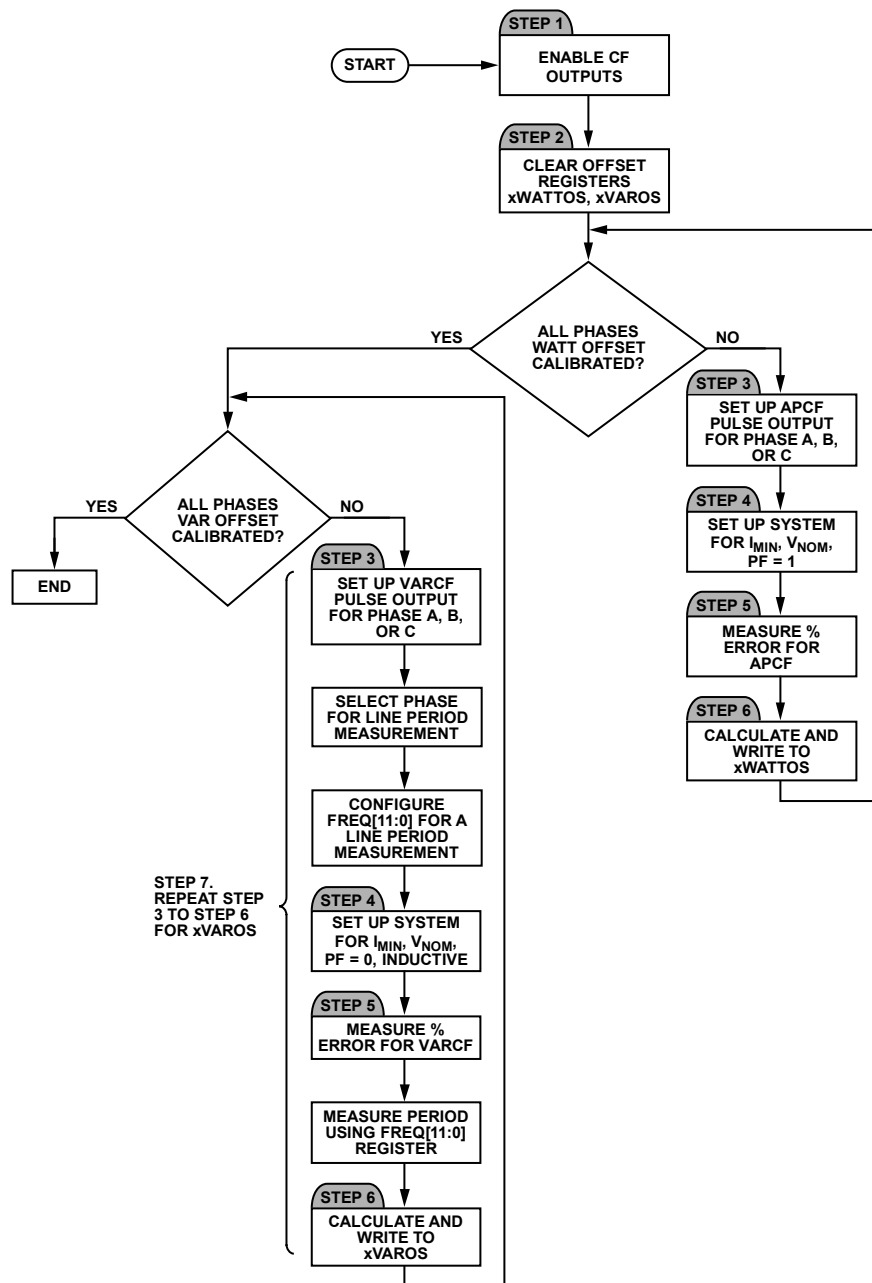


Figure 79. Offset Calibration Using Pulse Output

Step 1: Repeat Step 1 and Step 3 from the gain calibration to configure the ADE7758 pulse output.

Step 2: Clear the xWATTOS and xVAROS registers.

Step 3: Disable the Phase B and Phase C contribution to the APCF and VARCF pulses. This is done by the TERMSSEL[2:4] bits of the COMPMODE register (0x16). Setting Bit 2 to Logic 1 and Bit 3 and Bit 4 to Logic 0 allows only Phase A to be included in the pulse outputs. Select Phase A, Phase B, or Phase C for a line period measurement with the FREQSEL[1:0] bits in the MMODE register (0x14). For example, clearing Bit 1 and Bit 0 selects Phase A for line period measurement.

Step 4: Set the test system for  $I_{MIN}$ ,  $V_{NOM}$ , and unity power factor. For Step 6, set the test system for  $I_{MIN}$ ,  $V_{NOM}$ , and zero-power factor inductive.

Step 5: Measure the percent error in the pulse output, APCF or VARCF, from the reference meter using Equation 49.

Step 6: Calculate xWATTOS using Equation 56 (for xVAROS use Equation 57).

$$xWATTOS = -\left(\frac{\%APCF_{ERROR}}{100\%} \times APCF_{EXPECTED}\right) \times \frac{2^4}{Q} \times \frac{APCFDEN}{APCFNUM} \quad (56)$$

$$xVAROS = \frac{-\left(\frac{\%VARCF_{ERROR}}{100\%} \times VARCF_{EXPECTED}\right) \times \frac{2^4}{Q} \times \frac{VARCFDEN}{VARCFNUM}}{(57)}$$

where Q is defined in Equation 58 and Equation 59.

For xWATTOS,

$$Q = \frac{CLKIN}{4} \times \frac{1}{2^{25}} \times \frac{1}{4} \quad (58)$$

For xVAROS,

$$Q = \frac{CLKIN}{4} \times \frac{1}{2^{24}} \times \frac{202}{\left(\frac{FREQ[11:0]}{4}\right)} \times \frac{1}{4} \quad (59)$$

where the FREQ (0x10) register is configured for line period measurements.

Step 7: Repeat Step 3 to Step 6 for xVAROS calibration.

### Example: Offset Calibration of Phase A Using Pulse Output

For this example,  $I_{MIN} = 50$  mA,  $V_{NOM} = 220$  V,  $V_{FULLSCALE} = 500$  V,  $I_{FULLSCALE} = 130$  A,  $MC = 3200$  impulses/kWh, Power Factor = 1, Frequency = 50 Hz, and  $CLKIN = 10$  MHz.

With  $I_{MIN}$ ,  $V_{NOM}$ , and unity power factor, the example ADE7758 meter shows 0.009789 Hz on the APCF pulse output. When the power factor is changed to 0.5 inductive, the VARCF output is 0.009769 Hz.

This is equivalent to 0.1198% for the watt measurement and -0.0860% for the VAR measurement. Using Equation 56 through Equation 59, the values 0xFFD and 0x3 should be written to AWATTOS (0x39) and AVAROS (0x3C), respectively.

$$AWATTOS = -\left(\frac{0.1198\%}{100\%} \times 0.009778\right) \times \frac{2^4}{0.01863} \times \frac{277}{1} = -2.8 = -3 = 0xFFD$$

$$AVAROS = -\left(\frac{-0.0860\%}{100\%} \times 0.009778\right) \times \frac{2^4}{0.01444} \times \frac{277}{1} = 2.6 = 3$$

For AWATTOS,

$$Q = \frac{10E6}{4} \times \frac{1}{2^{25}} \times \frac{1}{4} = 0.01863$$

For AVAROS,

$$Q = \frac{10E6}{4} \times \frac{1}{2^{24}} \times \frac{202}{\frac{2083}{4}} \times \frac{1}{4} = 0.01444$$

### Calibration Using Line Accumulation

Line cycle accumulation mode configures the nine energy registers such that the amount of energy accumulated over an integer number of half line cycles appears in the registers after the LENERGY interrupt. The benefit of using this mode is that the sinusoidal component of the active energy is eliminated.

Figure 80 shows a flowchart of how to calibrate the ADE7758 using the line accumulation mode. Calibration of all phases and energies can be done simultaneously using this mode to save time during calibration.

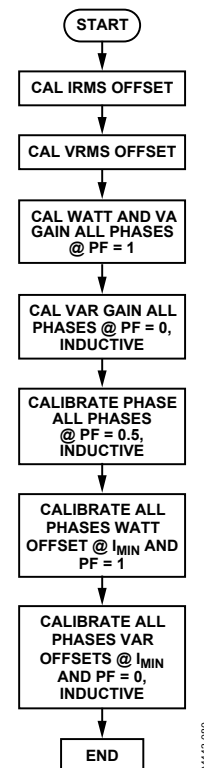


Figure 80. Calibration Using Line Accumulation

**Gain Calibration Using Line Accumulation**

Gain calibration is used for meter-to-meter gain adjustment, APCF or VARCF output rate calibration, and determining the Wh/LSB, VARh/LSB, and VAh/LSB constant.

Step 0: Before performing the gain calibration, the APCFNUM/APCFDEN (0x45/0x46) and VARCFNUM/ VARCFDEN (0x47/0x48) values can be set to achieve the correct impulses/kWh, impulses/kVAh, or impulses/kVARh using the same method outlined in Step 4 in the Gain Calibration Using Pulse Output section. The calibration of xWG/xVARG/xVAG (0x2A through 0x32) is done with the line accumulation mode. Figure 81 shows the steps involved in calibrating the gain registers using the line accumulation mode.

Step 1: Clear xWG, xVARG, and xVAG.

Step 2: Select Phase A, Phase B, or Phase C for a line period measurement with the FREQSEL[1:0] bits in the MMODE register (0x14). For example, clearing Bit 1 and Bit 0 selects Phase A for line period measurement.

Step 3: Set up ADE7758 for line accumulation by writing 0xBF to LCYCMODE. This enables the line accumulation mode on the xWATTHR, xVARHR, and xVAHR (0x01 to 0x09) registers by setting the LWATT, LVAR, and LVA bits, LCYCMODE[0:2] (0x17), to Logic 1. It also sets the ZXSEL bits, LCYCMODE[3:5], to Logic 1 to enable the zero-crossing detection on all phases for line accumulation. Additionally, the FREQSEL bit, LCYCMODE[7], is set so that FREQ (0x10) stores the line period. When using the line accumulation mode, the RSTREAD bit of LCYCMODE should be set to 0 to disable the read with reset mode. Select the phase for line period measurement in MMODE[1:0].

Step 4: Set the number of half-line cycles for line accumulation by writing to LINECYC (0x1C).

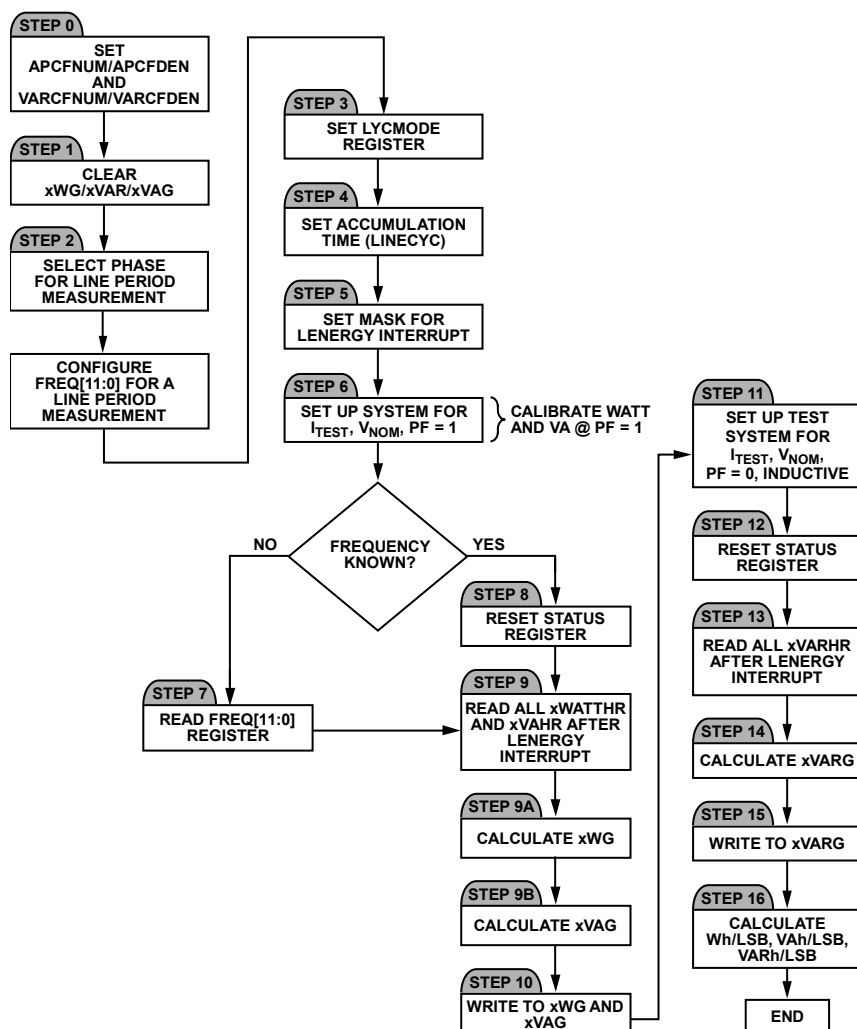


Figure 81. Gain Calibration Using Line Accumulation

Step 5: Set the LENERGY bit, MASK[12] (0x18), to Logic 1 to enable the interrupt signaling the end of the line cycle accumulation.

Step 6: Set the test system for  $I_{TEST}$ ,  $V_{NOM}$ , and unity power factor (calibrate watt and VA simultaneously and first).

Step 7: Read the FREQ (0x10) register if the line frequency is unknown.

Step 8: Reset the interrupt status register by reading RSTATUS (0x1A).

Step 9: Read all six xWATTHR (0x01 to 0x03) and xVAHR (0x07 to 0x09) energy registers after the LENERGY interrupt and store the values.

Step 9a: Calculate the values to be written to xWG registers according to the following equations:

$$WATTHR_{EXPECTED} = \frac{4 \times MC \times I_{TEST} \times V_{NOM} \times \cos(\theta) \times AccumTime}{1000 \times 3600} \times \frac{APCFDEN}{APCFNUM} \times \frac{1}{WDIV} \quad (60)$$

where *AccumTime* is

$$\frac{LINECYC[15:0]}{2 \times Line\ Frequency \times No.\ of\ Phases\ Selected} \quad (61)$$

where:

*MC* is the meter constant.

$\theta$  is the angle between the current and voltage.

*Line Frequency* is known or calculated from the FREQ[11:0] register. With the FREQ[11:0] register configured for line period measurements, the line frequency is calculated with Equation 62.

$$Line\ Frequency = \frac{1}{FREQ[11:0] \times 9.6 \times 10^{-6}} \quad (62)$$

*No. of Phases Selected* is the number of ZXSEL bits set to Logic 1 in LCYCMODE (0x17).

Then, *xWG* is calculated as

$$xWG = \left( \frac{WATTHR_{EXPECTED}}{WATTHR_{MEASURED}} - 1 \right) \times 2^{12} \quad (63)$$

Step 9b: Calculate the values to be written to the xVAG registers according to the following equation:

$$VAHR_{EXPECTED} = \frac{4 \times MC \times I_{TEST} \times V_{NOM} \times AccumTime}{1000 \times 3600} \times \frac{VARCFDEN}{VARCFNUM} \times \frac{1}{VADIV} \quad (64)$$

$$xVAG = \left( \frac{VAHR_{EXPECTED}}{VAHR_{MEASURED}} - 1 \right) \times 2^{12}$$

Step 10: Write to xWG and xVAG.

Step 11: Set the test system for  $I_{TEST}$ ,  $V_{NOM}$ , and zero power factor inductive to calibrate VAR gain.

Step 12: Repeat Step 7.

Step 13: Read the xVARHR (0x04 to 0x06) after the LENERGY interrupt and store the values.

Step 14: Calculate the values to be written to the xVARG registers (to adjust VARCF to the expected value).

$$VARHR_{EXPECTED} = \frac{4 \times MC \times I_{TEST} \times V_{NOM} \times \sin(\theta) \times AccumTime}{1000 \times 3600} \times \frac{VARCFDEN}{VARCFNUM} \times \frac{1}{VARDIV} \quad (65)$$

$$xVARG = \left( \frac{VARHR_{EXPECTED}}{VARHR_{MEASURED}} - 1 \right) \times 2^{12}$$

Step 15: Write to xVARG.

Step 16: Calculate the Wh/LSB, VARh/LSB, and VAh/LSB constants.

$$\frac{Wh}{LSB} = \frac{I_{TEST} \times V_{NOM} \times \cos(\theta) \times AccumTime}{3600 \times xWATTHR} \quad (66)$$

$$\frac{VAh}{LSB} = \frac{I_{TEST} \times V_{NOM} \times AccumTime}{3600 \times xVAHR} \quad (67)$$

$$\frac{VARh}{LSB} = \frac{I_{TEST} \times V_{NOM} \times \sin(\theta) \times AccumTime}{3600 \times xVARHR} \quad (68)$$

### Example: Watt Gain Calibration Using Line Accumulation

This example shows only Phase A watt calibration. The steps outlined in the Gain Calibration Using Line Accumulation section show how to calibrate watt, VA, and VAR. All three phases can be calibrated simultaneously because there are nine energy registers.

For this example,  $I_{TEST} = 10$  A,  $V_{NOM} = 220$  V, Power Factor = 1, Frequency = 50 Hz, LINECYC (0x1C) is set to 0x800, and MC = 3200 imp/kWhr.

To set APCFNUM (0x45) and APCFDEN (0x46) to the calculated value to perform a coarse adjustment on the imp/kW-hr ratio, use Equation 45 to Equation 47.

$$APCF_{NOMINAL} = 16 \text{ kHz} \times \frac{220}{500} \times \frac{10}{130} = 0.5415 \text{ kHz}$$

$$APCF_{EXPECTED} = \frac{3200 \times 10 \times 220}{1000 \times 3600} \times \cos(\theta) = 1.956 \text{ Hz}$$

$$APCFDEN = \text{INT}\left(\frac{541.5 \text{ Hz}}{1.956 \text{ Hz}}\right) = 277$$

Under the test conditions above, the AWATTHR register value is 15559d after the LENERGY interrupt. Using Equation 60 and Equation 61, the value to be written to AWG is -199d, 0xF39.

$$AccumTime = \frac{LINECYC[15:0]}{2 \times \frac{1}{FREQ[11:0] \times 9.6 \times 10^{-6}} \times \text{No. of Phases Selected}}$$

$$AccumTime = \frac{0x800}{2 \times \frac{1}{2085 \times 9.6 \times 10^{-6}} \times 3} = 6.832128s$$

$$WATTHR_{EXPECTED} = \frac{4 \times 3200 \times 10 \times 220 \times 1 \times 6.832}{1000 \times 3600} \times \frac{277}{1} \times 1 = 14804$$

$$xWG = \left(\frac{14804}{15559} - 1\right) \times 2^{12} = -198.87640 = -199 = 0xF39$$

Using Equation 66, the Wh/LSB constant is

$$\frac{Wh}{LSB} = \frac{10 \times 220 \times 6.832}{3600 \times 14804} = 0.0002820$$

### Phase Calibration Using Line Accumulation

The ADE7758 includes a phase calibration register on each phase to compensate for small phase errors. Large phase errors should be compensated by adjusting the antialiasing filters. The ADE7758's phase calibration is a time delay with different weights in the positive and negative direction (see the Phase Compensation section). Because a current transformer is a source of phase error, a fixed nominal value can be decided on to load into the xPHCAL (0x3F to 0x41) registers at power-up. During calibration, this value can be adjusted for CT-to-CT error. Figure 82 shows the steps involved in calibrating the phase using the line accumulation mode.

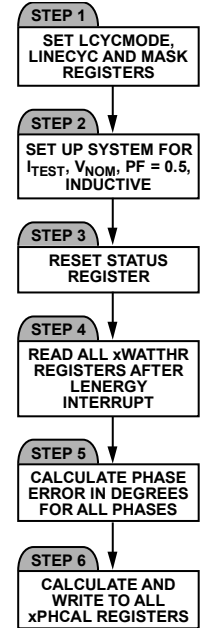


Figure 82. Phase Calibration Using Line Accumulation

Step 1: If the values were changed after gain calibration, Step 1, Step 3, and Step 4 from the gain calibration should be repeated to configure the LCYCMODE and LINECYC registers.

Step 2: Set the test system for  $I_{TEST}$ ,  $V_{NOM}$ , and 0.5 power factor inductive.

Step 3: Reset the interrupt status register by reading RSTATUS (0x1A).

Step 4: The xWATTHR registers should be read after the LENERGY interrupt. Measure the percent error in the energy register readings (AWATTHR, BWATTHR, and CWATTHR) compared to the energy register readings at unity power factor (after gain calibration) using Equation 69. The readings at unity power factor should have been repeated after the gain calibration and stored for use in the phase calibration routine.

$$Error = \frac{xWATTHR_{PF=5} - \frac{xWATTHR_{PF=1}}{2}}{\frac{xWATTHR_{PF=1}}{2}} \quad (69)$$

Step 5: Calculate the *Phase Error* in degrees using the equation

$$Phase\ Error(^{\circ}) = -\text{Arcsin}\left(\frac{Error}{\sqrt{3}}\right) \quad (70)$$

Step 6: Calculate xPHCAL and write to the xPHCAL registers (0x3F to 0x41).

$$xPHCAL = Phase\ Error \times \frac{1}{PHCAL\_LSB\_Weight} \times \frac{1}{Line\ Period(s)} \times \frac{1}{360^{\circ}} \quad (71)$$

# ADE7758

where PHCAL\_LSB\_Weight is 1.2 μs if the %Error is negative or 2.4 μs if the %Error is positive (see the Phase Compensation section).

If it is not known, the line period is available in the ADE7758's frequency register, FREQ (0x10). To configure line period measurement, select the phase for period measurement in the MMODE[1:0] and set LCYCMODE[7]. Equation 72 shows how to determine the value that needs to be written to xPHCAL using the period register measurement.

$$xPHCAL = \text{Phase Error} \times \frac{9.6 \mu\text{s}}{\text{PHCAL\_LSB\_Weight}} \times \frac{\text{FREQ}[11:0]}{360^\circ} \quad (72)$$

### Example: Phase Calibration Using Line Accumulation

This example shows only Phase A phase calibration. All three PHCAL registers can be calibrated simultaneously using the same method.

For this example, I<sub>TEST</sub> = 10 A, V<sub>NOM</sub> = 220 V, Power Factor = 0.5 inductive, and Frequency = 50 Hz. Also, LINECYC = 0x800.

With I<sub>TEST</sub>, V<sub>NOM</sub>, and 0.5 inductive power factor, the example ADE7758 meter shows 7318d in the AWATTHR (0x01) register. For unity power factor (after gain calibration), the meter shows 14804d in the AWATTHR register. This is equivalent to -1.132% error.

$$\text{Error} = \frac{7318 - \frac{14804}{2}}{\frac{14804}{2}} = -0.01132 = -1.132\%$$

The Phase Error in degrees using Equation 66 is 0.374°.

$$\text{Phase Error}(\text{°}) = -\text{Arcsin}\left(\frac{-0.01132}{\sqrt{3}}\right) = 0.374^\circ$$

Using Equation 72, the value written to APHCAL (0x3F), if at 50 Hz, the FREQ (0x10) register = 2085d, is 17d. Note that a PHCAL\_LSB\_Weight of 1.2 μs is used because the %Error is negative.

$$\text{APHCAL} = 0.374^\circ \times \frac{9.6}{1.2} \times \frac{2085}{360} = 17 = 0x11$$

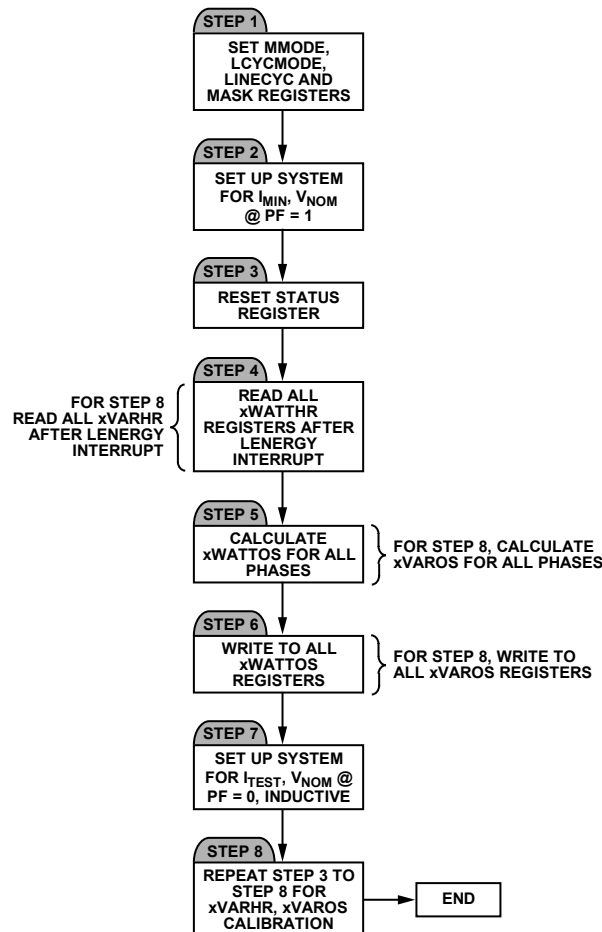


Figure 83. Power Offset Calibration Using Line Accumulation

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**Power Offset Calibration Using Line Accumulation**

Power offset calibration should be used for outstanding performance over a wide dynamic range (1000:1). Calibration of the power offset is done at or close to the minimum current. The ADE7758 has power offset registers for watts and VAR, xWATTOS (0x39 to 0x3B) and xVAROS (0x3C to 0x3E). Offsets in the VA measurement are compensated by adjusting the rms offset registers (see the Calibration of IRMS and VRMS Offset section).

More line cycles could be required at the minimum current to minimize the effect of quantization error on the offset calibration. For example, if a current of 40 mA results in an active energy accumulation of 113 after 2000 half line cycles, one LSB variation in this reading represents an 0.8% error. This measurement does not provide enough resolution to calibrate out a <1% offset error. However, if the active energy is accumulated over 37,500 half line cycles, one LSB variation results in 0.05% error, reducing the quantization error.

Figure 83 shows the steps to calibrate the power offsets using the line accumulation mode.

Step 1: If the values change after gain calibration, Step 1, Step 3, and Step 4 from the gain calibration should be repeated to configure the LCYCMODE, LINECYC, and MASK registers. Select Phase A, Phase B, or Phase C for a line period measurement with the FREQSEL[1:0] bits in the MMODE register (0x14). For example, clearing Bit 1 and Bit 0 selects Phase A for line period measurement.

Step 2: Set the test system for I<sub>MIN</sub>, V<sub>NOM</sub>, and unity power factor.

Step 3: Reset the interrupt status register by reading RSTATUS (0x1A).

Step 4: Read all xWATTHR energy registers (0x01 to 0x03) after the LENERGY interrupt and store the values.

Step 4a: If it is not known, the line period is available in the ADE7758's frequency register, FREQ (0x10). To configure line period measurement, select the phase for period measurement in the MMODE[1:0] and set LCYCMODE[7].

Step 5: Calculate the value to be written to the xWATTOS registers according to the following equations:

$$Offset = \frac{xWATTHR_{I_{MIN}} \times I_{TEST} - \left( xWATTHR_{I_{TEST}} \times \frac{LINECYC_{IMIN}}{LINECYC_{ITEST}} \right) \times I_{MIN}}{I_{MIN} - I_{TEST}} \quad (73)$$

$$xWATTOS[11:0] = \frac{Offset \times 4}{AccumTime \times CLKIN} \times 2^{29} \quad (74)$$

where:

AccumTime is defined in Equation 58.

xWATTHR<sub>I<sub>TEST</sub></sub> is the value in the energy register at I<sub>TEST</sub>.

xWATTHR<sub>I<sub>MIN</sub></sub> is the value in the energy register at I<sub>MIN</sub>.

LINECYC<sub>IMIN</sub> is the number of line cycles accumulated at I<sub>MIN</sub>.

LINECYC<sub>IMAX</sub> is the number of line cycles accumulated at I<sub>MAX</sub>.

Step 6: Write to all xWATTOS registers (0x39 to 0x3B).

Step 7: Set the test system for I<sub>MIN</sub>, V<sub>NOM</sub>, and zero power factor inductive to calibrate VAR gain.

Step 8: Repeat Steps 3, 4, and 5.

Step 9: Calculate the value written to the xVAROS registers according to the following equations:

$$Offset = \frac{xVARHR_{I_{MIN}} \times I_{TEST} - \left( xVARHR_{I_{TEST}} \times \frac{LINECYC_{IMIN}}{LINECYC_{ITEST}} \right) \times I_{MIN}}{I_{MIN} - I_{TEST}} \quad (75)$$

$$xVAROS[11:0] = \frac{Offset \times 4}{AccumTime \times CLKIN} \times \frac{FREQ[11:0]}{202} \times 2^{26} \quad (76)$$

where the FREQ[11:0] register is configured for line period readings.

**Example: Power Offset Calibration Using Line Accumulation**

This example only shows Phase A of the phase active power offset calibration. Both active and reactive power offset for all phases can be calibrated simultaneously using the method explained in the Power Offset Calibration Using Line Accumulation section.

For this example, I<sub>MIN</sub> = 50 mA, I<sub>TEST</sub> = 10 A, V<sub>NOM</sub> = 220 V, V<sub>FULLSCALE</sub> = 500 V, I<sub>FULLSCALE</sub> = 130 A, MC = 3200 impulses/kWh, Power Factor = 1, Frequency = 50 Hz, and CLKIN = 10 MHz. Also, LINECYC<sub>ITEST</sub> = 0x800 and LINECYC<sub>IMIN</sub> = 0x4000.

After accumulating over 0x800 line cycles for gain calibration at I<sub>TEST</sub>, the example ADE7758 meter shows 14804d in the AWATTHR (0x01) register. At I<sub>MIN</sub>, the meter shows 592d in the AWATTHR register. By using Equation 73, this is equivalent to 0.161 LSBs of offset; therefore, using Equation 61 and Equation 74, the value written to AWATTOS is 0d.

$$Offset = \frac{592 \times 10 - \left( 14804 \times \frac{0x4000}{0x800} \right) \times 0.05}{0.05 - 10} = 0.16$$

$$AccumTime = \frac{0 \times 4000}{2 \times \frac{1}{2085 \times 9.6 \times 10^{-6}} \times 3} = 54.64s$$

$$AWATTOS = \frac{0.161 \times 4}{54.64 \times 10 \text{ MHz}} \times 2^{29} = -0.088 = 0$$

## Calibration of IRMS and VRMS Offset

IRMSOS and VRMSOS are used to cancel noise and offset contributions from the inputs. The calibration method is the same whether calibrating using the pulse outputs or line accumulation. Reading the registers is required for this calibration because there is no rms pulse output. The rms offset calibration should be performed before VAGAIN calibration. The rms offset calibration also removes offset from the VA calculation. For this reason, no VA offset register exists in the ADE7758.

The low-pass filter used to obtain the rms measurements is not ideal; therefore, it is recommended to synchronize the readings with the zero crossings of the voltage waveform and to average a few measurements when reading the rms registers.

The ADE7758 IRMS measurement is linear over a 500:1 range, and the VRMS measurement is linear over a 20:1 range. To measure the voltage VRMS offset (xVRMSOS), measure rms values at two different nonzero current levels, for example,  $V_{NOM}$  and  $V_{FULLSCALE}/20$ .

To measure the current rms offset (IRMSOS), measure rms values at two different nonzero current levels, for example,  $I_{TEST}$  and  $I_{FULLSCALE}/500$ . This translates to two test conditions:  $I_{TEST}$  and  $V_{NOM}$ , and  $I_{FULLSCALE}/500$  and  $V_{FULLSCALE}/20$ . Figure 84 shows a flowchart for calibrating the rms measurements.

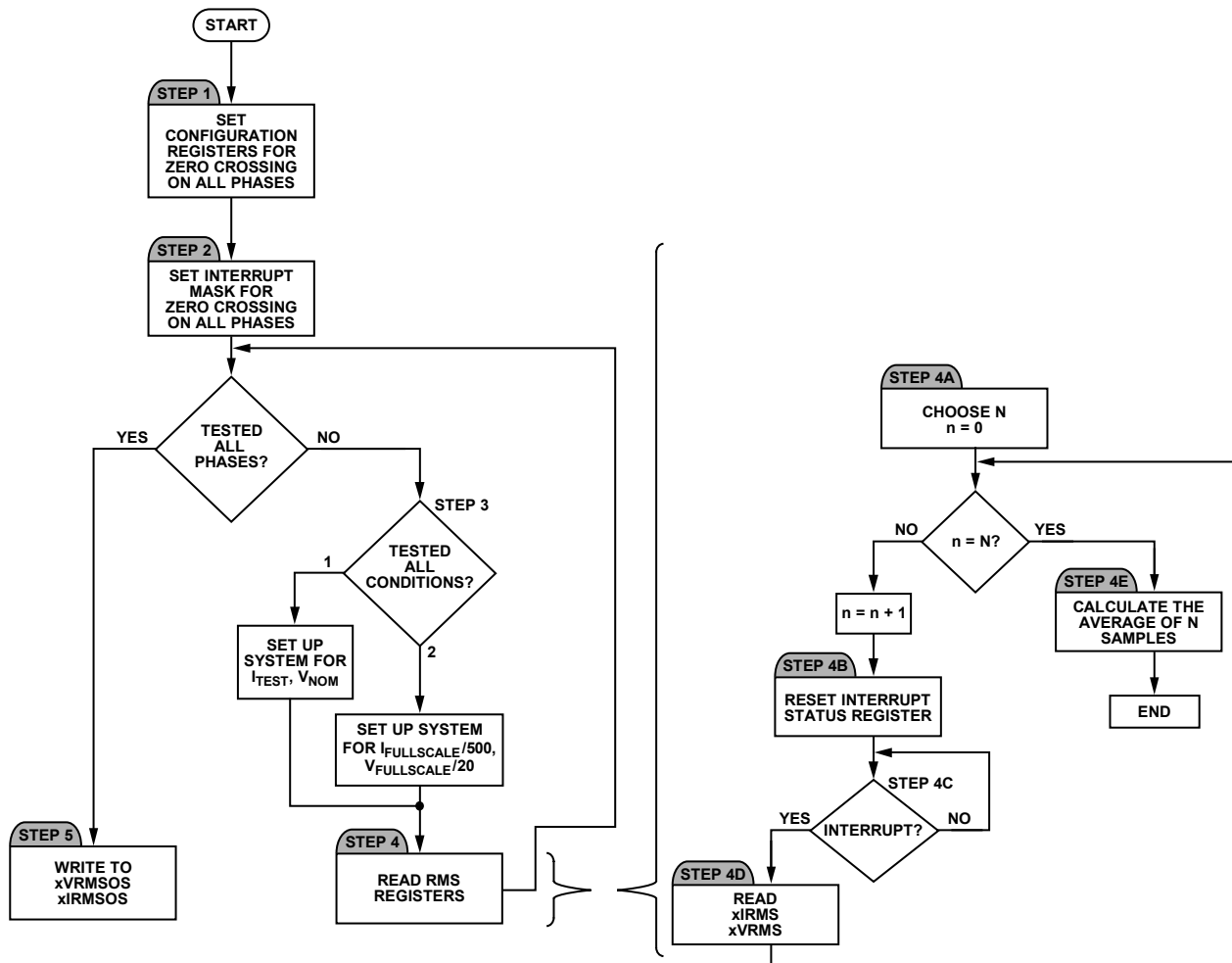


Figure 84. RMS Calibration Routine

Step 1: Set configuration registers for zero crossings on all phases by writing the value 0x38 to the LCYCMODE register (0x17). This sets all of the ZXSEL bits to Logic 1.

Step 2: Set the interrupt mask register for zero-crossing detection on all phases by writing 0xE00 to the MASK[0:24] register (0x18). This sets all of the ZX bits to Logic 1.

Step 3: Set up the calibration system for one of the two test conditions:  $I_{TEST}$  and  $V_{NOM}$ , and  $I_{FULLSCALE}/500$  and  $V_{FULLSCALE}/20$ .

Step 4: Read the rms registers after the zero-crossing interrupt and take an average of N samples. This is recommended to get the most stable rms readings. This procedure is detailed in Figure 84: Steps 4a through 4e.

Step 4a. Choose the number of samples, N, to be averaged.

Step 4b. Reset the interrupt status register by reading RSTATUS (0x1A).

Step 4c. Wait for the zero-crossing interrupt. When the zero-crossing interrupt occurs, move to Step 4d.

Step 4d. Read the xIRMS and xVRMS registers. These values will be averaged in Step 4e.

Step 4e: Average the N samples of xIRMS and xVRMS. The averaged values will be used in Step 5.

Step 5: Write to the xVRMSOS (0x33 to 0x35) and xIRMSOS (0x36 to 0x38) registers according to the following equations:

$$xIRMSOS = \frac{1}{16384} \times \frac{(I_{TEST}^2 \times IRMS_{IMIN}^2) - (I_{MIN}^2 \times IRMS_{ITEST}^2)}{I_{MIN}^2 - I_{TEST}^2} \quad (77)$$

where:

$I_{MIN}$  is the full scale current/500.

$I_{TEST}$  is the test current.

$IRMS_{IMIN}$  and  $IRMS_{ITEST}$  are the current rms register values without offset correction for the inputs  $I_{MIN}$  and  $I_{TEST}$ , respectively.

$$xVRMSOS = \frac{1}{64} \times \frac{V_{NOM} \times VRMS_{VMIN} - V_{MIN} \times VRMS_{VNOM}}{V_{MIN} - V_{NOM}} \quad (78)$$

where:

$V_{MIN}$  is the full scale voltage/20

$V_{NOM}$  is the nominal line voltage.

$VRMS_{VMIN}$  and  $VRMS_{VNOM}$  are the voltage rms register values without offset correction for the input  $V_{MIN}$  and  $V_{NOM}$ , respectively.

### Example: Calibration of RMS Offsets

For this example,  $I_{TEST} = 10$  A,  $I_{MAX} = 100$  A,  $V_{NOM} = 220$  V,  $V_{FULLSCALE} = 500$  V, Power Factor = 1, and Frequency = 50 Hz.

Twenty readings are taken synchronous to the zero crossings of all three phases at each current and voltage to determine the average xIRMS and xVRMS readings. At  $I_{TEST}$  and  $V_{NOM}$ , the example ADE7758 meter gets an average AIRMS (0x0A) reading of 148242.2 and 744570.8 in the AVRMS (0x0D) register. Then the current is set to  $I_{MIN} = I_{FULLSCALE}/500$  or 260 mA. At  $I_{MIN}$ , the average AIRMS reading is 3885.68. At  $V_{MIN} = V_{FULLSCALE}/20$  or 25 V, the example meter gets an average AVRMS of 86362.36. Using this data, -15d is written to AIRMSOS (0x36) and -31d is written to AVRMSOS (0x33) registers according to the Equation 77 and Equation 78.

$$AIRMSOS = \frac{1}{16384} \times \frac{(10^2 \times 3885.68^2) - (0.260^2 \times 148242.2^2)}{(0.260 - 10^2)} = -14.8 = -15 = 0xFF2$$

$$AVRMSOS = \frac{1}{64} \times \frac{(220 \times 86362.36) - (25 \times 744570.8)}{(25 - 220)} = -30.9 = -31 = 0xFE1$$

This example shows the calculations and measurements for Phase A only. However, all three xIRMS and xVRMS registers can be read simultaneously to compute the values for each xIRMSOS and xVRMSOS register.

### CHECKSUM REGISTER

The ADE7758 has a checksum register CHKSUM[7:0] (0x7E) to ensure the data bits received in the last serial read operation are not corrupted. The 8-bit checksum register is reset before the first bit (MSB of the register to be read) is put on the DOUT pin. During a serial read operation, when each data bit becomes available on the rising edge of SCLK, the bit is added to the checksum register. In the end of the serial read operation, the contents of the checksum register are equal to the sum of all the 1s in the register previously read. Using the checksum register, the user can determine if an error has occurred during the last read operation. Note that a read to the checksum register also generates a checksum of the checksum register itself.

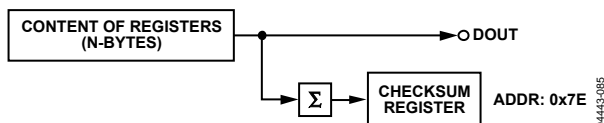


Figure 85. Checksum Register for Serial Interface Read

## INTERRUPTS

The ADE7758 interrupts are managed through the interrupt status register (STATUS[23:0], Address 0x19) and the interrupt mask register (MASK[23:0], Address 0x18). When an interrupt event occurs in the ADE7758, the corresponding flag in the interrupt status register is set to a Logic 1 (see Table 24). If the mask bit for this interrupt in the interrupt mask register is Logic 1, then the  $\overline{\text{IRQ}}$  logic output goes active low. The flag bits in the interrupt status register are set irrespective of the state of the mask bits. To determine the source of the interrupt, the MCU should perform a read from the reset interrupt status register with reset. This is achieved by carrying out a read from RSTATUS, Address 0x1A. The  $\overline{\text{IRQ}}$  output goes logic high on completion of the interrupt status register read command (see the Interrupt Timing section). When carrying out a read with reset, the ADE7758 is designed to ensure that no interrupt events are missed. If an interrupt event occurs just as the interrupt status register is being read, the event is not lost, and the  $\overline{\text{IRQ}}$  logic output is guaranteed to go logic high for the duration of the interrupt status register data transfer before going logic low again to indicate the pending interrupt. Note that the reset interrupt bit in the status register is high for only one clock cycle, and it then goes back to 0.

## USING THE INTERRUPTS WITH AN MCU

Figure 86 shows a timing diagram that illustrates a suggested implementation of ADE7758 interrupt management using an MCU. At time  $t_1$ , the  $\overline{\text{IRQ}}$  line goes active low indicating that one or more interrupt events have occurred in the ADE7758. The  $\overline{\text{IRQ}}$  logic output should be tied to a negative-edge-triggered external interrupt on the MCU. On detection of the negative edge, the MCU should be configured to start executing its interrupt service routine (ISR). On entering the ISR, all interrupts should be disabled using the global interrupt mask bit. At this point, the MCU external interrupt flag can be cleared to capture interrupt events that occur during the current ISR. When the MCU interrupt flag is cleared, a read from the reset interrupt status register with reset is carried out. (This causes the  $\overline{\text{IRQ}}$  line to be reset logic high ( $t_2$ ); see the Interrupt Timing section.) The reset interrupt status register contents are used to determine the source of the interrupt(s) and hence the appropriate action to be taken. If a subsequent interrupt event occurs during the ISR ( $t_3$ ) that event is recorded by the MCU external interrupt flag being set again.

On returning from the ISR, the global interrupt mask bit is cleared (same instruction cycle) and the external interrupt flag uses the MCU to jump to its ISR once again. This ensures that the MCU does not miss any external interrupts. The reset bit in the status register is an exception to this and is only high for one clock cycle after a reset event.

## INTERRUPT TIMING

The Serial Interface section should be reviewed before reviewing this section. As previously described, when the  $\overline{\text{IRQ}}$  output goes low, the MCU ISR must read the interrupt status register to determine the source of the interrupt. When reading the interrupt status register contents, the  $\overline{\text{IRQ}}$  output is set high on the last falling edge of SCLK of the first byte transfer (read interrupt status register command). The  $\overline{\text{IRQ}}$  output is held high until the last bit of the next 8-bit transfer is shifted out (interrupt status register contents), as shown in Figure 87. If an interrupt is pending at this time, the  $\overline{\text{IRQ}}$  output goes low again. If no interrupt is pending, the  $\overline{\text{IRQ}}$  output remains high.

## SERIAL INTERFACE

The ADE7758 has a built-in SPI interface. The serial interface of the ADE7758 is made of four signals: SCLK, DIN, DOUT, and  $\overline{\text{CS}}$ . The serial clock for a data transfer is applied at the SCLK logic input. This logic input has a Schmitt trigger input structure that allows slow rising (and falling) clock edges to be used. All data transfer operations are synchronized to the serial clock. Data is shifted into the ADE7758 at the DIN logic input on the falling edge of SCLK. Data is shifted out of the ADE7758 at the DOUT logic output on a rising edge of SCLK.

The  $\overline{\text{CS}}$  logic input is the chip select input. This input is used when multiple devices share the serial bus. A falling edge on  $\overline{\text{CS}}$  also resets the serial interface and places the ADE7758 in communications mode.

The  $\overline{\text{CS}}$  input should be driven low for the entire data transfer operation. Bringing  $\overline{\text{CS}}$  high during a data transfer operation aborts the transfer and places the serial bus in a high impedance state. The  $\overline{\text{CS}}$  logic input can be tied low if the ADE7758 is the only device on the serial bus.

However, with  $\overline{\text{CS}}$  tied low, all initiated data transfer operations must be fully completed. The LSB of each register must be transferred because there is no other way of bringing the ADE7758 back into communications mode without resetting the entire device, that is, performing a software reset using Bit 6 of the OPMODE[7:0] register, Address 0x13.

The functionality of the ADE7758 is accessible via several on-chip registers (see Figure 88). The contents of these registers can be updated or read using the on-chip serial interface. After a falling edge on  $\overline{\text{CS}}$ , the ADE7758 is placed in communications mode. In communications mode, the ADE7758 expects the first communication to be a write to the internal communications register. The data written to the communications register contains the address and specifies the next data transfer to be a read or a write command. Therefore, all data transfer operations with the ADE7758, whether a read or a write, must begin with a write to the communications register.

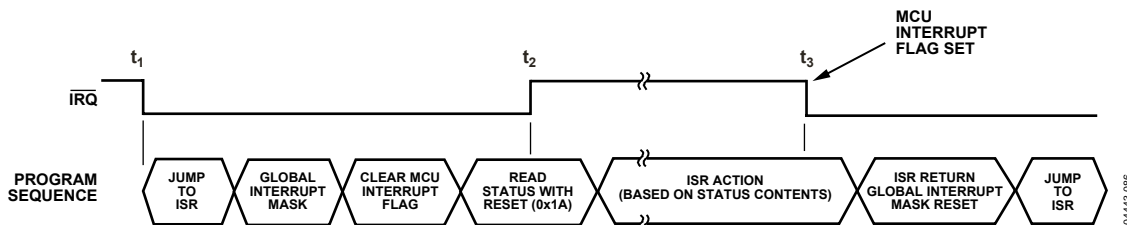


Figure 86. ADE7758 Interrupt Management

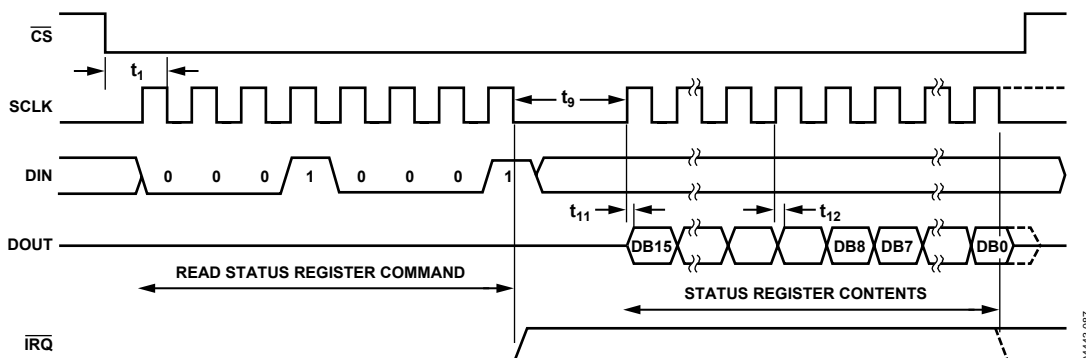


Figure 87. ADE7758 Interrupt Timing

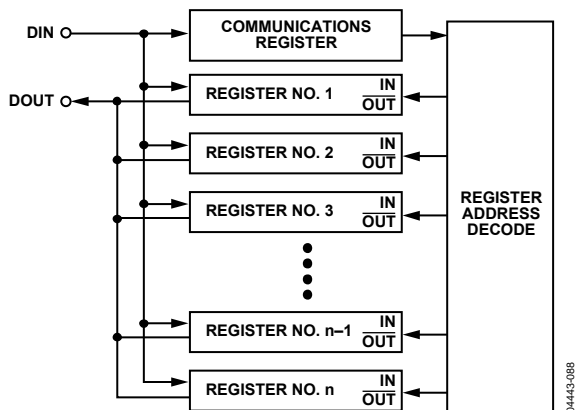


Figure 88. Addressing ADE7758 Registers via the Communications Register

The communications register is an 8-bit, write-only register. The MSB determines whether the next data transfer operation is a read or a write. The seven LSBs contain the address of the register to be accessed (see Table 16).

Figure 89 and Figure 90 show the data transfer sequences for a read and write operation, respectively.

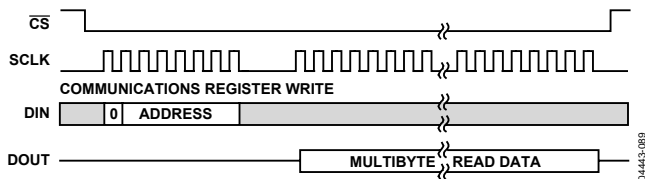


Figure 89. Reading Data from the ADE7758 via the Serial Interface

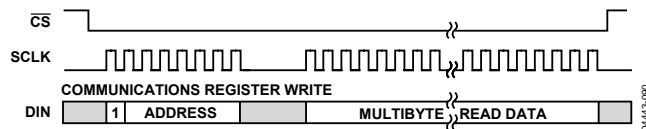


Figure 90. Writing Data to the ADE7758 via the Serial Interface

On completion of a data transfer (read or write), the ADE7758 once again enters into communications mode, that is, the next instruction followed must be a write to the communications register.

A data transfer is completed when the LSB of the ADE7758 register being addressed (for a write or a read) is transferred to or from the ADE7758.

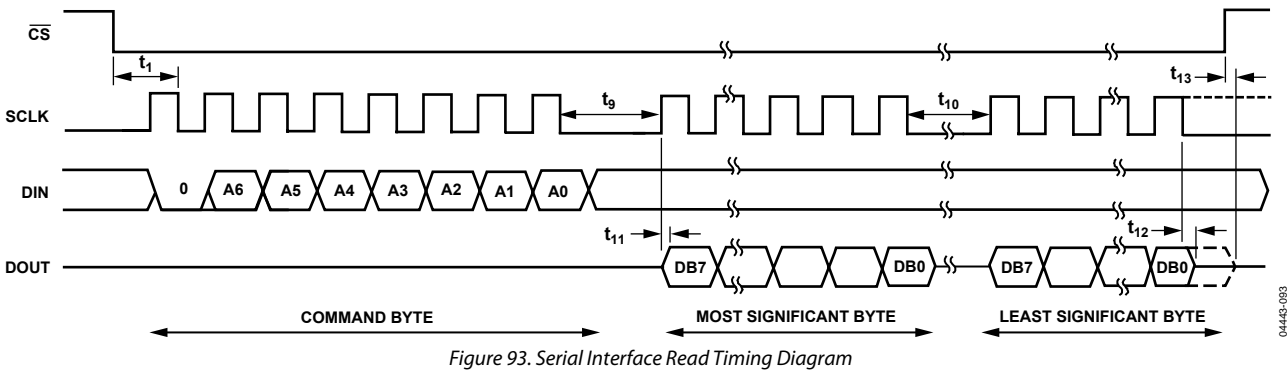
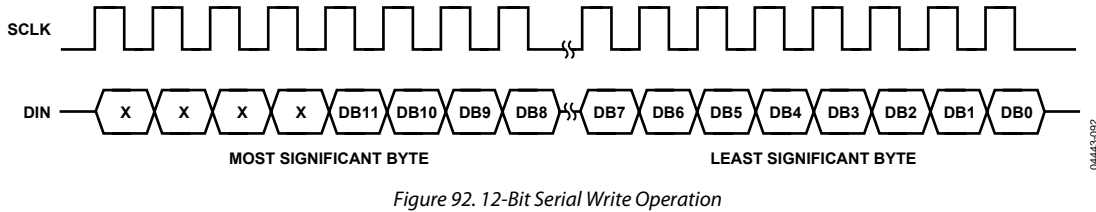
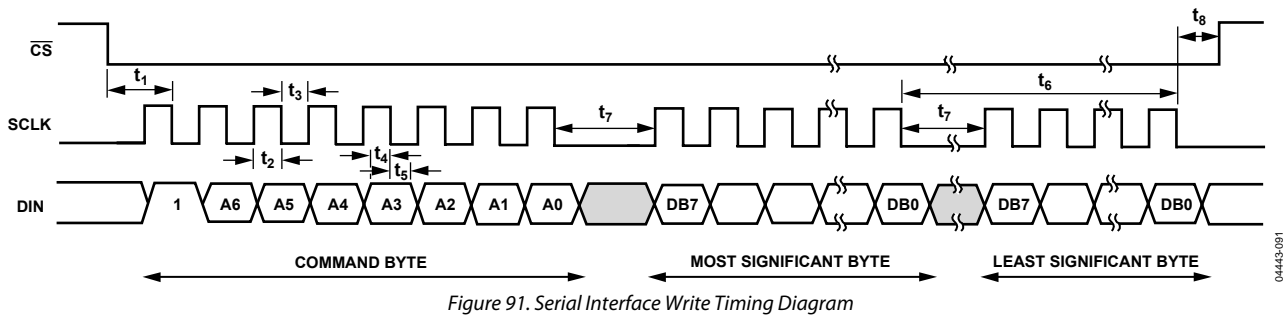
### SERIAL WRITE OPERATION

The serial write sequence takes place as follows. With the ADE7758 in communications mode and the CS input logic low, a write to the communications register takes place first. The MSB of this byte transfer must be set to 1, indicating that the next data transfer operation is a write to the register. The seven LSBs of this byte contain the address of the register to be written to. The ADE7758 starts shifting in the register data on the next falling edge of SCLK. All remaining bits of register data are shifted in on the falling edge of the subsequent SCLK pulses (see Figure 91).

# ADE7758

As explained earlier, the data write is initiated by a write to the communications register followed by the data. During a data write operation to the ADE7758, data is transferred to all on-chip registers one byte at a time. After a byte is transferred into the serial port, there is a finite time duration before the content in the serial port buffer is transferred to one of the ADE7758 on-chip registers. Although another byte transfer to the serial port can start while the previous byte is being transferred to the destination register, this second-byte transfer should not finish until at least 900 ns after the end of the previous byte transfer. This functionality is expressed in the timing specification  $t_6$  (see Figure 91). If a write operation is aborted during a byte transfer ( $\overline{CS}$  brought high), then that byte is not written to the destination register.

Destination registers can be up to 3 bytes wide (see the Accessing the On-Chip Registers section). Therefore, the first byte shifted into the serial port at DIN is transferred to the most significant byte (MSB) of the destination register. If the destination register is 12 bits wide, for example, a two-byte data transfer must take place. The data is always assumed to be right justified; therefore, in this case, the four MSBs of the first byte would be ignored, and the four LSBs of the first byte written to the ADE7758 would be the four MSBs of the 12-bit word. Figure 92 illustrates this example.



## SERIAL READ OPERATION

During a data read operation from the ADE7758, data is shifted out at the DOUT logic output on the rising edge of SCLK. As was the case with the data write operation, a data read must be preceded with a write to the communications register.

With the ADE7758 in communications mode and  $\overline{\text{CS}}$  logic low, an 8-bit write to the communications register takes place first. The MSB of this byte transfer must be a 0, indicating that the next data transfer operation is a read. The seven LSBs of this byte contain the address of the register that is to be read. The ADE7758 starts shifting out of the register data on the next rising edge of SCLK (see Figure 93). At this point, the DOUT logic output switches from a high impedance state and starts driving the data bus. All remaining bits of register data are shifted out on subsequent SCLK rising edges. The serial interface enters communications mode again as soon as the read is completed. The DOUT logic output enters a high impedance state on the falling edge of the last SCLK pulse.

The read operation can be aborted by bringing the  $\overline{\text{CS}}$  logic input high before the data transfer is completed. The DOUT output enters a high impedance state on the rising edge of  $\overline{\text{CS}}$ .

When an ADE7758 register is addressed for a read operation, the entire contents of that register are transferred to the serial port. This allows the ADE7758 to modify its on-chip registers without the risk of corrupting data during a multibyte transfer.

Note that when a read operation follows a write operation, the read command (that is, write to communications register) should not happen for at least 1.1  $\mu\text{s}$  after the end of the write operation. If the read command is sent within 1.1  $\mu\text{s}$  of the write operation, the last byte of the write operation can be lost.

## ACCESSING THE ON-CHIP REGISTERS

All ADE7758 functionality is accessed via the on-chip registers. Each register is accessed by first writing to the communications register and then transferring the register data. For a full description of the serial interface protocol, see the Serial Interface section.

# ADE7758

## REGISTERS

### COMMUNICATIONS REGISTER

The communications register is an 8-bit, write-only register that controls the serial data transfer between the ADE7758 and the host processor. All data transfer operations must begin with a write to the communications register.

The data written to the communications register determines whether the next operation is a read or a write and which register is being accessed.

Table 16 outlines the bit designations for the communications register.

**Table 16. Communications Register**

Bit Location	Bit Mnemonic	Description
0 to 6	A0 to A6	The seven LSBs of the communications register specify the register for the data transfer operation. Table 17 lists the address of each ADE7758 on-chip register.
7	$W/\bar{R}$	When this bit is a Logic 1, the data transfer operation immediately following the write to the communications register is interpreted as a write to the ADE7758. When this bit is a Logic 0, the data transfer operation immediately following the write to the communications register is interpreted as a read operation.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W/R	A6	A5	A4	A3	A2	A1	A0

**Table 17. ADE7758 Register List**

Address [A6:A0]	Name	R/W <sup>1</sup>	Length	Type <sup>2</sup>	Default Value	Description
0x00	Reserved	–				Reserved.
0x01	AWATTHR	R	16	S	0	Watt-Hour Accumulation Register for Phase A. Active power is accumulated over time in this read-only register. The AWATTHR register can hold a maximum of 0.52 seconds of active energy information with full-scale analog inputs before it overflows (see the Active Energy Calculation section). Bit 0 and Bit 1 of the COMPMODE register determine how the active energy is processed from the six analog inputs.
0x02	BWATTHR	R	16	S	0	Watt-Hour Accumulation Register for Phase B.
0x03	CWATTHR	R	16	S	0	Watt-Hour Accumulation Register for Phase C.
0x04	AVARHR	R	16	S	0	VAR-Hour Accumulation Register for Phase A. Reactive power is accumulated over time in this read-only register. The AVARHR register can hold a maximum of 0.52 seconds of reactive energy information with full-scale analog inputs before it overflows (see the Reactive Energy Calculation section). Bit 0 and Bit 1 of the COMPMODE register determine how the reactive energy is processed from the six analog inputs.
0x05	BVARHR	R	16	S	0	VAR-Hour Accumulation Register for Phase B.
0x06	CVARHR	R	16	S	0	VAR-Hour Accumulation Register for Phase C.
0x07	AVAHR	R	16	U	0	VA-Hour Accumulation Register for Phase A. Apparent power is accumulated over time in this read-only register. The AVAHR register can hold a maximum of 1.15 seconds of apparent energy information with full-scale analog inputs before it overflows (see the Apparent Energy Calculation section). Bit 0 and Bit 1 of the COMPMODE register determine how the apparent energy is processed from the six analog inputs.
0x08	BVAHR	R	16	U	0	VA-Hour Accumulation Register for Phase B.
0x09	CVAHR	R	16	U	0	VA-Hour Accumulation Register for Phase C.
0x0A	AIRMS	R	24	U	0	Phase A Current Channel RMS Register. The register contains the rms component of the Phase A input of the current channel. The source is selected by data bits in the mode register.
0x0B	BIRMS	R	24	U	0	Phase B Current Channel RMS Register.
0x0C	CIRMS	R	24	U	0	Phase C Current Channel RMS Register.
0x0D	AVRMS	R	24	U	0	Phase A Voltage Channel RMS Register.

Address [A6:A0]	Name	R/W <sup>1</sup>	Length	Type <sup>2</sup>	Default Value	Description
0x0E	BVRMS	R	24	U	0	Phase B Voltage Channel RMS Register.
0x0F	CVRMS	R	24	U	0	Phase C Voltage Channel RMS Register.
0x10	FREQ	R	12	U	0	Frequency of the Line Input Estimated by the Zero-Crossing Processing. It can also display the period of the line input. Bit 7 of the LCYCMODE register determines if the reading is frequency or period. Default is frequency. Data Bit 0 and Bit 1 of the MMODE register determine the voltage channel used for the frequency or period calculation.
0x11	TEMP	R	8	S	0	Temperature Register. This register contains the result of the latest temperature conversion. Refer to the Temperature Measurement section for details on how to interpret the content of this register.
0x12	WFORM	R	24	U	0	Waveform Register. This register contains the digitized waveform of one of the six analog inputs or the digitized power waveform. The source is selected by Data Bit 0 to Bit 4 in the WAVMODE register.
0x13	OPMODE	R/W	8	U	4	Operational Mode Register. This register defines the general configuration of the ADE7758 (see Table 18).
0x14	MMODE	R/W	8	U	0xFC	Measurement Mode Register. This register defines the channel used for period and peak detection measurements (see Table 19).
0x15	WAVMODE	R/W	8	U	0	Waveform Mode Register. This register defines the channel and sampling frequency used in the waveform sampling mode (see Table 20).
0x16	COMPmode	R/W	8	U	0x1C	Computation Mode Register. This register configures the formula applied for the energy and line active energy measurements (see Table 22).
0x17	LCYCMODE	R/W	8	U	0x78	Line Cycle Mode Register. This register configures the line cycle accumulation mode for WATT-HR, VAR-HR, and VA-Hr (see Table 23).
0x18	MASK	R/W	24	U	0	IRQ Mask Register. It determines if an interrupt event generates an active-low output at the IRQ pin (see the Interrupts section).
0x19	STATUS	R	24	U	0	IRQ Status Register. This register contains information regarding the source of the ADE7758 interrupts (see the Interrupts section).
0x1A	RSTATUS	R	24	U	0	IRQ Reset Status Register. Same as the STATUS register, except that its contents are reset to 0 (all flags cleared) after a read operation.
0x1B	ZXTOUT	R/W	16	U	0xFFFF	Zero-Cross Timeout Register. If no zero crossing is detected within the time period specified by this register, the interrupt request line (IRQ) goes active low for the corresponding line voltage. The maximum timeout period is 2.3 seconds (see the Zero-Crossing Detection section).
0x1C	LINECYC	R/W	16	U	0xFFFF	Line Cycle Register. The content of this register sets the number of half-line cycles that the active, reactive, and apparent energies are accumulated for in the line accumulation mode.
0x1D	SAGCYC	R/W	8	U	0xFF	SAG Line Cycle Register. This register specifies the number of consecutive half-line cycles where voltage channel input may fall below a threshold level. This register is common to the three line voltage SAG detection. The detection threshold is specified by the SAGLVL register (see the Line Voltage SAG Detection section).
0x1E	SAGLVL	R/W	8	U	0	SAG Voltage Level. This register specifies the detection threshold for the SAG event. This register is common to all three phases' line voltage SAG detections. See the description of the SAGCYC register for details.
0x1F	VPINTLVL	R/W	8	U	0xFF	Voltage Peak Level Interrupt Threshold Register. This register sets the level of the voltage peak detection. Bit 5 to Bit 7 of the MMODE register determine which phases are to be monitored. If the selected voltage phase exceeds this level, the PKV flag in the IRQ status register is set.
0x20	IPINTLVL	R/W	8	U	0xFF	Current Peak Level Interrupt Threshold Register. This register sets the level of the current peak detection. Bit 5 to Bit 7 of the MMODE register determine which phases are to be monitored. If the selected current phase exceeds this level, the PKI flag in the IRQ status register is set.
0x21	VPEAK	R	8	U	0	Voltage Peak Register. This register contains the value of the peak voltage waveform that has occurred within a fixed number of half-line cycles. The number of half-line cycles is set by the LINECYC register.

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Address [A6:A0]	Name	R/W <sup>1</sup>	Length	Type <sup>2</sup>	Default Value	Description
0x22	IPEAK	R	8	U	0	Current Peak Register. This register holds the value of the peak current waveform that has occurred within a fixed number of half-line cycles. The number of half-line cycles is set by the LINECYC register.
0x23	GAIN	R/W	8	U	0	PGA Gain Register. This register is used to adjust the gain selection for the PGA in the current and voltage channels (see the Analog Inputs section).
0x24	AVRMSGAIN	R/W	12	S	0	Phase A VRMS Gain Register. The range of the voltage rms calculation can be adjusted by writing to this register. It has an adjustment range of $\pm 50\%$ with a resolution of 0.0244%/LSB.
0x25	BVRMSGAIN	R/W	12	S	0	Phase B VRMS Gain Register.
0x26	CVRMSGAIN	R/W	12	S	0	Phase C VRMS Gain Register.
0x27	AIGAIN	R/W	12	S	0	Phase A Current Gain Register. The range of the current rms calculation can be adjusted by writing to this register. It has an adjustment range of $\pm 50\%$ with a resolution of 0.0244%/LSB. Adjusting this register also scales the watt and VAR calculation. Not for use with Mode 0 of CONSEL, COMPMODE[1:0].
0x28	BIGAIN	R/W	12	S	0	Phase B Current Gain Register. Not for use with Mode 0 of CONSEL COMPMODE[1:0].
0x29	CIGAIN	R/W	12	S	0	Phase C Current Gain Register. Not for use with Mode 0 of CONSEL COMPMODE[1:0].
0x2A	AWG	R/W	12	S	0	Phase A Watt Gain Register. The range of the watt calculation can be adjusted by writing to this register. It has an adjustment range of $\pm 50\%$ with a resolution of 0.0244%/LSB.
0x2B	BWG	R/W	12	S	0	Phase B Watt Gain Register.
0x2C	CWG	R/W	12	S	0	Phase C Watt Gain Register.
0x2D	AVARG	R/W	12	S	0	Phase A VAR Gain Register. The range of the VAR calculation can be adjusted by writing to this register. It has an adjustment range of $\pm 50\%$ with a resolution of 0.0244%/LSB.
0x2E	BVARG	R/W	12	S	0	Phase B VAR Gain Register.
0x2F	CVARG	R/W	12	S	0	Phase C VAR Gain Register.
0x30	AVAG	R/W	12	S	0	Phase A VA Gain Register. The range of the VA calculation can be adjusted by writing to this register. It has an adjustment range of $\pm 50\%$ with a resolution of 0.0244%/LSB.
0x31	BVAG	R/W	12	S	0	Phase B VA Gain Register.
0x32	CVAG	R/W	12	S	0	Phase C VA Gain Register.
0x33	AVRMSOS	R/W	12	S	0	Phase A Voltage RMS Offset Correction Register.
0x34	BVRMSOS	R/W	12	S	0	Phase B Voltage RMS Offset Correction Register.
0x35	CVRMSOS	R/W	12	S	0	Phase C Voltage RMS Offset Correction Register.
0x36	AIRMSOS	R/W	12	S	0	Phase A Current RMS Offset Correction Register.
0x37	BIRMSOS	R/W	12	S	0	Phase B Current RMS Offset Correction Register.
0x38	CIRMSOS	R/W	12	S	0	Phase C Current RMS Offset Correction Register.
0x39	AWATTOS	R/W	12	S	0	Phase A Watt Offset Calibration Register.
0x3A	BWATTOS	R/W	12	S	0	Phase B Watt Offset Calibration Register.
0x3B	CWATTOS	R/W	12	S	0	Phase C Watt Offset Calibration Register.
0x3C	AVAROS	R/W	12	S	0	Phase A VAR Offset Calibration Register.
0x3D	BVAROS	R/W	12	S	0	Phase B VAR Offset Calibration Register.
0x3E	CVAROS	R/W	12	S	0	Phase C VAR Offset Calibration Register.
0x3F	APHCAL	R/W	7	S	0	Phase A Phase Calibration Register. The phase relationship between the current and voltage channel can be adjusted by writing to this signed 7-bit register (see the Phase Compensation section).
0x40	BPHCAL	R/W	7	S	0	Phase B Phase Calibration Register.
0x41	CPHCAL	R/W	7	S	0	Phase C Phase Calibration Register.
0x42	WDIV	R/W	8	U	0	Active Energy Register Divider.
0x43	VARDIV	R/W	8	U	0	Reactive Energy Register Divider.
0x44	VADIV	R/W	8	U	0	Apparent Energy Register Divider.

Address [A6:A0]	Name	R/W <sup>1</sup>	Length	Type <sup>2</sup>	Default Value	Description
0x45	APCFNUM	R/W	16	U	0	Active Power CF Scaling Numerator Register. The content of this register is used in the numerator of the APCF output scaling calculation. Bits [15:13] indicate reverse polarity active power measurement for Phase A, Phase B, and Phase C in order; that is, Bit 15 is Phase A, Bit 14 is Phase B, and so on.
0x46	APCFDEN	R/W	12	U	0x3F	Active Power CF Scaling Denominator Register. The content of this register is used in the denominator of the APCF output scaling.
0x47	VARCFNUM	R/W	16	U	0	Reactive Power CF Scaling Numerator Register. The content of this register is used in the numerator of the VARCF output scaling. Bits [15:13] indicate reverse polarity reactive power measurement for Phase A, Phase B, and Phase C in order; that is, Bit 15 is Phase A, Bit 14 is Phase B, and so on.
0x48	VARCFDEN	R/W	12	U	0x3F	Reactive Power CF Scaling Denominator Register. The content of this register is used in the denominator of the VARCF output scaling.
0x49 to 0x7D	RESERVED	–	–	–	–	Reserved.
0x7E	CHKSUM	R	8	U	–	Checksum Register. The content of this register represents the sum of all the ones in the last register read from the SPI port.
0x7F	VERSION	R	8	U	–	Version of the Die.

<sup>1</sup> This column specifies the read/write capability of the register. R = Read only register. R/W = Register that can be both read and written.

<sup>2</sup> Type decoder: U = unsigned; S = signed.



**WAVEFORM MODE REGISTER (0x15)**

The waveform sampling mode of the ADE7758 is defined by writing to the WAVMODE register. Table 20 summarizes the functionality of each bit in the WAVMODE register.

**Table 20. WAVMODE Register**

Bit Location	Bit Mnemonic	Default Value	Description																												
0 to 1	PHSEL	0	<p>These bits are used to select the phase of the waveform sample.</p> <table border="0"> <tr> <td colspan="2"><b>PHSEL[1:0]</b></td> <td><b>Source</b></td> </tr> <tr> <td>0</td> <td>0</td> <td>Phase A</td> </tr> <tr> <td>0</td> <td>1</td> <td>Phase B</td> </tr> <tr> <td>1</td> <td>0</td> <td>Phase C</td> </tr> <tr> <td>1</td> <td>1</td> <td>Reserved</td> </tr> </table>	<b>PHSEL[1:0]</b>		<b>Source</b>	0	0	Phase A	0	1	Phase B	1	0	Phase C	1	1	Reserved													
<b>PHSEL[1:0]</b>		<b>Source</b>																													
0	0	Phase A																													
0	1	Phase B																													
1	0	Phase C																													
1	1	Reserved																													
2 to 4	WAVSEL	0	<p>These bits are used to select the type of waveform.</p> <table border="0"> <tr> <td colspan="3"><b>WAVSEL[2:0]</b></td> <td><b>Source</b></td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Current</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Voltage</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Active Power Multiplier Output</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Reactive Power Multiplier Output</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>VA Multiplier Output</td> </tr> <tr> <td colspan="3">-Others-</td> <td>Reserved</td> </tr> </table>	<b>WAVSEL[2:0]</b>			<b>Source</b>	0	0	0	Current	0	0	1	Voltage	0	1	0	Active Power Multiplier Output	0	1	1	Reactive Power Multiplier Output	1	0	0	VA Multiplier Output	-Others-			Reserved
<b>WAVSEL[2:0]</b>			<b>Source</b>																												
0	0	0	Current																												
0	0	1	Voltage																												
0	1	0	Active Power Multiplier Output																												
0	1	1	Reactive Power Multiplier Output																												
1	0	0	VA Multiplier Output																												
-Others-			Reserved																												
5 to 6	DTRT	0	<p>These bits are used to select the data rate.</p> <table border="0"> <tr> <td colspan="2"><b>DTRT[1:0]</b></td> <td><b>Update Rate</b></td> </tr> <tr> <td>0</td> <td>0</td> <td>26.04 kSPS (CLKIN/3/128)</td> </tr> <tr> <td>0</td> <td>1</td> <td>13.02 kSPS (CLKIN/3/256)</td> </tr> <tr> <td>1</td> <td>0</td> <td>6.51 kSPS (CLKIN/3/512)</td> </tr> <tr> <td>1</td> <td>1</td> <td>3.25 kSPS (CLKIN/3/1024)</td> </tr> </table>	<b>DTRT[1:0]</b>		<b>Update Rate</b>	0	0	26.04 kSPS (CLKIN/3/128)	0	1	13.02 kSPS (CLKIN/3/256)	1	0	6.51 kSPS (CLKIN/3/512)	1	1	3.25 kSPS (CLKIN/3/1024)													
<b>DTRT[1:0]</b>		<b>Update Rate</b>																													
0	0	26.04 kSPS (CLKIN/3/128)																													
0	1	13.02 kSPS (CLKIN/3/256)																													
1	0	6.51 kSPS (CLKIN/3/512)																													
1	1	3.25 kSPS (CLKIN/3/1024)																													
7	VACF	0	<p>Setting this bit to Logic 1 switches the VARCF output pin to an output frequency that is proportional to the total apparent power (VA). In the default state, Logic 0, the VARCF pin outputs a frequency proportional to the total reactive power (VAR).</p>																												

## COMPUTATIONAL MODE REGISTER (0x16)

The computational method of the ADE7758 is defined by writing to the COMPMODE register. Table 21 summarizes the functionality of each bit in the COMPMODE register.

**Table 21. COMPMODE Register**

Bit Location	Bit Mnemonic	Default Value	Description																																								
0 to 1	CONSEL	0	<p>These bits are used to select the input to the energy accumulation registers. CONSEL[1:0] = 11 is reserved. <math>\overline{IA}</math>, <math>\overline{IB}</math>, and <math>\overline{IC}</math> are IA, IB, and IC phase shifted by <math>-90^\circ</math>, respectively.</p> <table border="1"> <thead> <tr> <th>Registers</th> <th>CONSEL[1, 0] = 00</th> <th>CONSEL[1, 0] = 01</th> <th>CONSEL[1, 0] = 10</th> </tr> </thead> <tbody> <tr> <td>AWATTHR</td> <td><math>VA \times IA</math></td> <td><math>VA \times (IA - IB)</math></td> <td><math>VA \times (IA - IB)</math></td> </tr> <tr> <td>BWATTHR</td> <td><math>VB \times IB</math></td> <td>0</td> <td>0</td> </tr> <tr> <td>CWATTHR</td> <td><math>VC \times IC</math></td> <td><math>VC \times (IC - IB)</math></td> <td><math>VC \times IC</math></td> </tr> <tr> <td>AVARHR</td> <td><math>VA \times \overline{IA}</math></td> <td><math>VA \times (\overline{IA} - \overline{IB})</math></td> <td><math>VA \times (IA - IB)</math></td> </tr> <tr> <td>BVARHR</td> <td><math>VB \times \overline{IB}</math></td> <td>0</td> <td>0</td> </tr> <tr> <td>CVARHR</td> <td><math>VC \times \overline{IC}</math></td> <td><math>VC \times (\overline{IC} - \overline{IB})</math></td> <td><math>VC \times IC</math></td> </tr> <tr> <td>AVAHR</td> <td><math>V_{RMS} \times I_{RMS}</math></td> <td><math>V_{RMS} \times I_{RMS}</math></td> <td><math>V_{RMS} \times A_{RMS}</math></td> </tr> <tr> <td>BVAHR</td> <td><math>V_{RMS} \times I_{RMS}</math></td> <td><math>(V_{RMS} + V_{C_{RMS}})/2 \times I_{RMS}</math></td> <td><math>V_{RMS} \times I_{RMS}</math></td> </tr> <tr> <td>CVAHR</td> <td><math>V_{RMS} \times I_{RMS}</math></td> <td><math>V_{RMS} \times I_{RMS}</math></td> <td><math>V_{RMS} \times I_{C_{RMS}}</math></td> </tr> </tbody> </table>	Registers	CONSEL[1, 0] = 00	CONSEL[1, 0] = 01	CONSEL[1, 0] = 10	AWATTHR	$VA \times IA$	$VA \times (IA - IB)$	$VA \times (IA - IB)$	BWATTHR	$VB \times IB$	0	0	CWATTHR	$VC \times IC$	$VC \times (IC - IB)$	$VC \times IC$	AVARHR	$VA \times \overline{IA}$	$VA \times (\overline{IA} - \overline{IB})$	$VA \times (IA - IB)$	BVARHR	$VB \times \overline{IB}$	0	0	CVARHR	$VC \times \overline{IC}$	$VC \times (\overline{IC} - \overline{IB})$	$VC \times IC$	AVAHR	$V_{RMS} \times I_{RMS}$	$V_{RMS} \times I_{RMS}$	$V_{RMS} \times A_{RMS}$	BVAHR	$V_{RMS} \times I_{RMS}$	$(V_{RMS} + V_{C_{RMS}})/2 \times I_{RMS}$	$V_{RMS} \times I_{RMS}$	CVAHR	$V_{RMS} \times I_{RMS}$	$V_{RMS} \times I_{RMS}$	$V_{RMS} \times I_{C_{RMS}}$
Registers	CONSEL[1, 0] = 00	CONSEL[1, 0] = 01	CONSEL[1, 0] = 10																																								
AWATTHR	$VA \times IA$	$VA \times (IA - IB)$	$VA \times (IA - IB)$																																								
BWATTHR	$VB \times IB$	0	0																																								
CWATTHR	$VC \times IC$	$VC \times (IC - IB)$	$VC \times IC$																																								
AVARHR	$VA \times \overline{IA}$	$VA \times (\overline{IA} - \overline{IB})$	$VA \times (IA - IB)$																																								
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CVARHR	$VC \times \overline{IC}$	$VC \times (\overline{IC} - \overline{IB})$	$VC \times IC$																																								
AVAHR	$V_{RMS} \times I_{RMS}$	$V_{RMS} \times I_{RMS}$	$V_{RMS} \times A_{RMS}$																																								
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CVAHR	$V_{RMS} \times I_{RMS}$	$V_{RMS} \times I_{RMS}$	$V_{RMS} \times I_{C_{RMS}}$																																								
2 to 4	TERMSEL	7	<p>These bits are used to select the phases to be included in the APCF and VARCF pulse outputs. Setting Bit 2 selects Phase A (the inputs to AWATTHR and AVARHR registers) to be included. Bit 3 and Bit 4 are for Phase B and Phase C, respectively. Setting all three bits enables the sum of all three phases to be included in the frequency outputs (see the Active Power Frequency Output and the Reactive Power Frequency Output sections).</p>																																								
5	ABS	0	<p>Setting this bit places the APCF output pin in absolute only mode. Namely, the APCF output frequency is proportional to the sum of the absolute values of the watt-hour accumulation registers (AWATTHR, BWATTHR, and CWATTHR). Note that this bit only affects the APCF pin and has no effect on the content of the corresponding registers.</p>																																								
6	SAVAR	0	<p>Setting this bit places the VARCF output pin in the signed adjusted mode. Namely, the VARCF output frequency is proportional to the sign-adjusted sum of the VAR-hour accumulation registers (AVARHR, BVARHR, and CVARHR). The sign of the VAR is determined from the sign of the watt calculation from the corresponding phase, that is, the sign of the VAR is flipped if the sign of the watt is negative, and if the watt is positive, there is no change to the sign of the VAR. Note that this bit only affects the VARCF pin and has no effect on the content of the corresponding registers.</p>																																								
7	NOLOAD	0	<p>Setting this bit activates the no-load threshold in the ADE7758.</p>																																								

**LINE CYCLE ACCUMULATION MODE REGISTER (0x17)**

The functionalities involved the line-cycle accumulation mode in the ADE7758 are defined by writing to the LCYCMODE register. Table 22 summarizes the functionality of each bit in the LCYCMODE register.

**Table 22. LCYCMODE Register**

Bit Location	Bit Mnemonic	Default Value	Description
0	LWATT	0	Setting this bit places the watt-hour accumulation registers (AWATTHR, BWATTHR, and CWATTHR registers) into line-cycle accumulation mode.
1	LVAR	0	Setting this bit places the VAR-hour accumulation registers (AVARHR, BVARHR, and CVARHR registers) into line-cycle accumulation mode.
2	LVA	0	Setting this bit places the VA-hour accumulation registers (AVAHR, BVAHR, and CVAHR registers) into line-cycle accumulation mode.
3 to 5	ZXSEL	7	These bits select the phases used for counting the number of zero crossings in the line-cycle accumulation mode. Bit 3, Bit 4, and Bit 5 select Phase A, Phase B, and Phase C, respectively. More than one phase can be selected for the zero-crossing detection, and the accumulation time is shortened accordingly.
6	RSTREAD	1	Setting this bit enables the read-with-reset for all the WATTHR, VARHR, and VAHR registers for all three phases, that is, a read to those registers resets the registers to 0 after the content of the registers have been read. This bit should be set to Logic 0 when the LWATT, LVAR, or LVA bits are set to Logic 1.
7	FREQSEL	0	Setting this bit causes the FREQ (0x10) register to display the period, instead of the frequency of the line input.

# ADE7758

## INTERRUPT MASK REGISTER (0x18)

When an interrupt event occurs in the ADE7758, the  $\overline{\text{IRQ}}$  logic output goes active low if the mask bit for this event is Logic 1 in the MASK register. The  $\overline{\text{IRQ}}$  logic output is reset to its default collector open state when the RSTATUS register is read. Table 23 describes the function of each bit in the interrupt mask register.

**Table 23. Function of Each Bit in the Interrupt Mask Register**

Bit Location	Interrupt Flag	Default Value	Description
0	AEHF	0	Enables an interrupt when there is a change in Bit 14 of any one of the three WATTHR registers, that is, the WATTHR register is half full.
1	REHF	0	Enables an interrupt when there is a change in Bit 14 of any one of the three VARHR registers, that is, the VARHR register is half full.
2	VAEHF	0	Enables an interrupt when there is a 0 to 1 transition in the MSB of any one of the three VAHR registers, that is, the VAHR register is half full.
3	SAGA	0	Enables an interrupt when there is a SAG on the line voltage of the Phase A.
4	SAGB	0	Enables an interrupt when there is a SAG on the line voltage of the Phase B.
5	SAGC	0	Enables an interrupt when there is a SAG on the line voltage of the Phase C.
6	ZXTOA	0	Enables an interrupt when there is a zero-crossing timeout detection on Phase A.
7	ZXTOB	0	Enables an interrupt when there is a zero-crossing timeout detection on Phase B.
8	ZXTOC	0	Enables an interrupt when there is a zero-crossing timeout detection on Phase C.
9	ZXA	0	Enables an interrupt when there is a zero crossing in the voltage channel of Phase A (see the Zero-Crossing Detection section).
10	ZXB	0	Enables an interrupt when there is a zero crossing in the voltage channel of Phase B (see the Zero-Crossing Detection section).
11	ZXC	0	Enables an interrupt when there is a zero crossing in the voltage channel of Phase C (see the Zero-Crossing Detection section).
12	LENERGY	0	Enables an interrupt when the energy accumulations over LINECYC are finished.
13	RESERVED	0	Reserved.
14	PKV	0	Enables an interrupt when the voltage input selected in the MMODE register is above the value in the VPINTLVL register.
15	PKI	0	Enables an interrupt when the current input selected in the MMODE register is above the value in the IPINTLVL register.
16	WFSM	0	Enables an interrupt when data is present in the WAVEMODE register.
17	REVPAP	0	Enables an interrupt when there is a sign change in the watt calculation among any one of the phases specified by the TERMSEL bits in the COMPMODE register.
18	REVPRP	0	Enables an interrupt when there is a sign change in the VAR calculation among any one of the phases specified by the TERMSEL bits in the COMPMODE register.
19	SEQERR	0	Enables an interrupt when the zero crossing from Phase A is followed not by the zero crossing of Phase C but with that of Phase B.

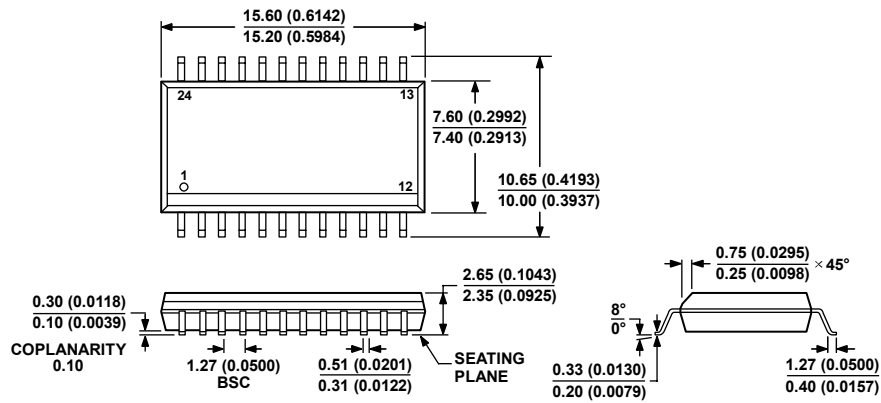
**INTERRUPT STATUS REGISTER (0x19)/RESET INTERRUPT STATUS REGISTER (0x1A)**

The interrupt status register is used to determine the source of an interrupt event. When an interrupt event occurs in the ADE7758, the corresponding flag in the interrupt status register is set. The  $\overline{\text{IRQ}}$  pin goes active low if the corresponding bit in the interrupt mask register is set. When the MCU services the interrupt, it must first carry out a read from the interrupt status register to determine the source of the interrupt. All the interrupts in the interrupt status register stay at their logic high state after an event occurs. The state of the interrupt bit in the interrupt status register is reset to its default value once the reset interrupt status register is read.

**Table 24. Interrupt Status Register**

Bit Location	Interrupt Flag	Default Value	Event Description
0	AEHF	0	Indicates that an interrupt was caused by a change in Bit 14 among any one of the three WATTHR registers, that is, the WATTHR register is half full.
1	REHF	0	Indicates that an interrupt was caused by a change in Bit 14 among any one of the three VARHR registers, that is, the VARHR register is half full.
2	VAEHF	0	Indicates that an interrupt was caused by a 0 to 1 transition in Bit 15 among any one of the three VAHR registers, that is, the VAHR register is half full.
3	SAGA	0	Indicates that an interrupt was caused by a SAG on the line voltage of the Phase A.
4	SAGB	0	Indicates that an interrupt was caused by a SAG on the line voltage of the Phase B.
5	SAGC	0	Indicates that an interrupt was caused by a SAG on the line voltage of the Phase C.
6	ZXTOA	0	Indicates that an interrupt was caused by a missing zero crossing on the line voltage of the Phase A.
7	ZXTOB	0	Indicates that an interrupt was caused by a missing zero crossing on the line voltage of the Phase B.
8	ZXTOC	0	Indicates that an interrupt was caused by a missing zero crossing on the line voltage of the Phase C.
9	ZXA	0	Indicates a detection of a rising edge zero crossing in the voltage channel of Phase A.
10	ZXB	0	Indicates a detection of a rising edge zero crossing in the voltage channel of Phase B.
11	ZXC	0	Indicates a detection of a rising edge zero crossing in the voltage channel of Phase C.
12	LENERGY	0	In line energy accumulation, indicates the end of an integration over an integer number of half-line cycles (LINECYC). See the Calibration section.
13	RESET	1	Indicates that the 5 V power supply is below 4 V. Enables a software reset of the ADE7758 and sets the registers back to their default values. This bit in the STATUS or RSTATUS register is logic high for only one clock cycle after a reset event.
14	PKV	0	Indicates that an interrupt was caused when the selected voltage input is above the value in the VPINTLVL register.
15	PKI	0	Indicates that an interrupt was caused when the selected current input is above the value in the IPINTLVL register.
16	WFSM	0	Indicates that new data is present in the waveform register.
17	REVPAP	0	Indicates that an interrupt was caused by a sign change in the watt calculation among any one of the phases specified by the TERMSEL bits in the COMPMODE register.
18	REVPRP	0	Indicates that an interrupt was caused by a sign change in the VAR calculation among any one of the phases specified by the TERMSEL bits in the COMPMODE register.
19	SEQERR	0	Indicates that an interrupt was caused by a zero crossing from Phase A followed not by the zero crossing of Phase C but by that of Phase B.

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AD  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 94. 24-Lead Standard Small Outline Package [SOIC\_W]  
 Wide Body (RW-24)  
 Dimensions shown in millimeters and (inches)

060706-A

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADE7758ARW	-40°C to +85°C	24-Lead Wide Body SOIC_W	RW-24
ADE7758ARWRL	-40°C to +85°C	24-Lead Wide Body SOIC_W	RW-24
ADE7758ARWZ <sup>1</sup>	-40°C to +85°C	24-Lead Wide Body SOIC_W	RW-24
ADE7758ARWZRL <sup>1</sup>	-40°C to +85°C	24-Lead Wide Body SOIC_W	RW-24
EVAL-ADE7758EB		Evaluation Board	

<sup>1</sup> Z = Pb-free part.

**NOTES**

**ADE7758**

**NOTES**

## A Low Cost Watt-Hour Energy Meter Based on the AD7755

By Anthony Collins

### INTRODUCTION

This application note describes a low-cost, high-accuracy watt-hour meter based on the AD7755. The meter described is intended for use in single phase, two-wire distribution systems. However the design can easily be adapted to suit specific regional requirements, e.g., in the United States power is usually distributed to residential customers as single-phase, three-wire.

The AD7755 is a low-cost, single-chip solution for electrical energy measurement. The AD7755 is comprised of two ADCs, reference circuit, and all the signal processing necessary for the calculation of real (active) power. The AD7755 also includes direct drive capability for electromechanical counters (i.e., the energy register), and has a high-frequency pulse output for calibration and communications purposes.

This application note should be used in conjunction with the AD7755 data sheet. The data sheet provides detailed information on the functionality of the AD7755 and will be referenced several times in this application note.

### DESIGN GOALS

The international Standard IEC1036 (1996-09) – *Alternating Current Watt-Hour Meters for Active Energy (Classes 1 and 2)*, was used as the primary specification for this design. For readers more familiar with the ANSI C12.16 specification, see the section at the end of this application note, which compares the IEC1036 and ANSI C12.16 standards. This section explains the key IEC1036 specifications in terms of their ANSI equivalents.

The design greatly exceeds this basic specification for many of the accuracy requirements, e.g., accuracy at unity-power factor and at low (PF = ±0.5) power factor. In addition, the dynamic range performance of the meter has been extended to 500. The IEC1036 standard specifies accuracy over a range of 5% Ib to I<sub>MAX</sub>—see Table I. Typical values for I<sub>MAX</sub> are 400% to 600% of Ib. Table I outlines the accuracy requirements for a static watt-hour meter. The current range (dynamic range) for accuracy is specified in terms of Ib (basic current).

Table I. Accuracy Requirements

Current Value <sup>1</sup>	PF <sup>2</sup>	Percentage Error Limits <sup>3</sup>	
		Class 1	Class 2
0.05 Ib ≤ I < 0.1 Ib	1	±1.5%	±2.5%
0.1 Ib ≤ I ≤ I <sub>MAX</sub>	1	±1.0%	±2.0%
0.1 Ib ≤ I ≤ 0.2 Ib	0.5 Lag	±1.5%	±2.5%
	0.8 Lead	±1.5%	
0.2 Ib ≤ I ≤ I <sub>MAX</sub>	0.5 Lag	±1.0%	±2.0%
	0.8 Lead	±1.0%	

#### NOTES

<sup>1</sup>The current ranges for specified accuracy shown in Table I are expressed in terms of the basic current (Ib). The basic current is defined in IEC1036 (1996-09) section 3.5.1.1 as the value of current in accordance with which the relevant performance of a direct connection meter is fixed. I<sub>MAX</sub> is the maximum current at which accuracy is maintained.

<sup>2</sup>Power Factor (PF) in Table I relates the phase relationship between the fundamental (45 Hz to 65 Hz) voltage and current waveforms. PF in this case can be simply defined as PF = cos(φ), where φ is the phase angle between pure sinusoidal current and voltage.

<sup>3</sup>Class index is defined in IEC1036 (1996-09) section 3.5.5 as the limits of the permissible percentage error. The percentage error is defined as:

$$\text{Percentage Error} = \frac{\text{Energy Registered by Meter} - \text{True Energy}}{\text{True Energy}} \times 100\%$$

The schematic in Figure 1 shows the implementation of a simple, low-cost watt-hour meter using the AD7755. A shunt is used to provide the current-to-voltage conversion needed by the AD7755 and a simple divider network attenuates the line voltage. The energy register (kWh) is a simple electromechanical counter that uses a two-phase stepper motor. The AD7755 provides direct drive capability for this type of counter. The AD7755 also provides a high-frequency output at the CF pin for the meter constant (3200 imp/kWh). Thus a high-frequency output is available at the LED and opto-isolator output. This high-frequency output is used to speed up the calibration process and provides a means of quickly verifying meter functionality and accuracy in a production environment. The meter is calibrated by varying the line voltage attenuation using the resistor network R5 to R14.

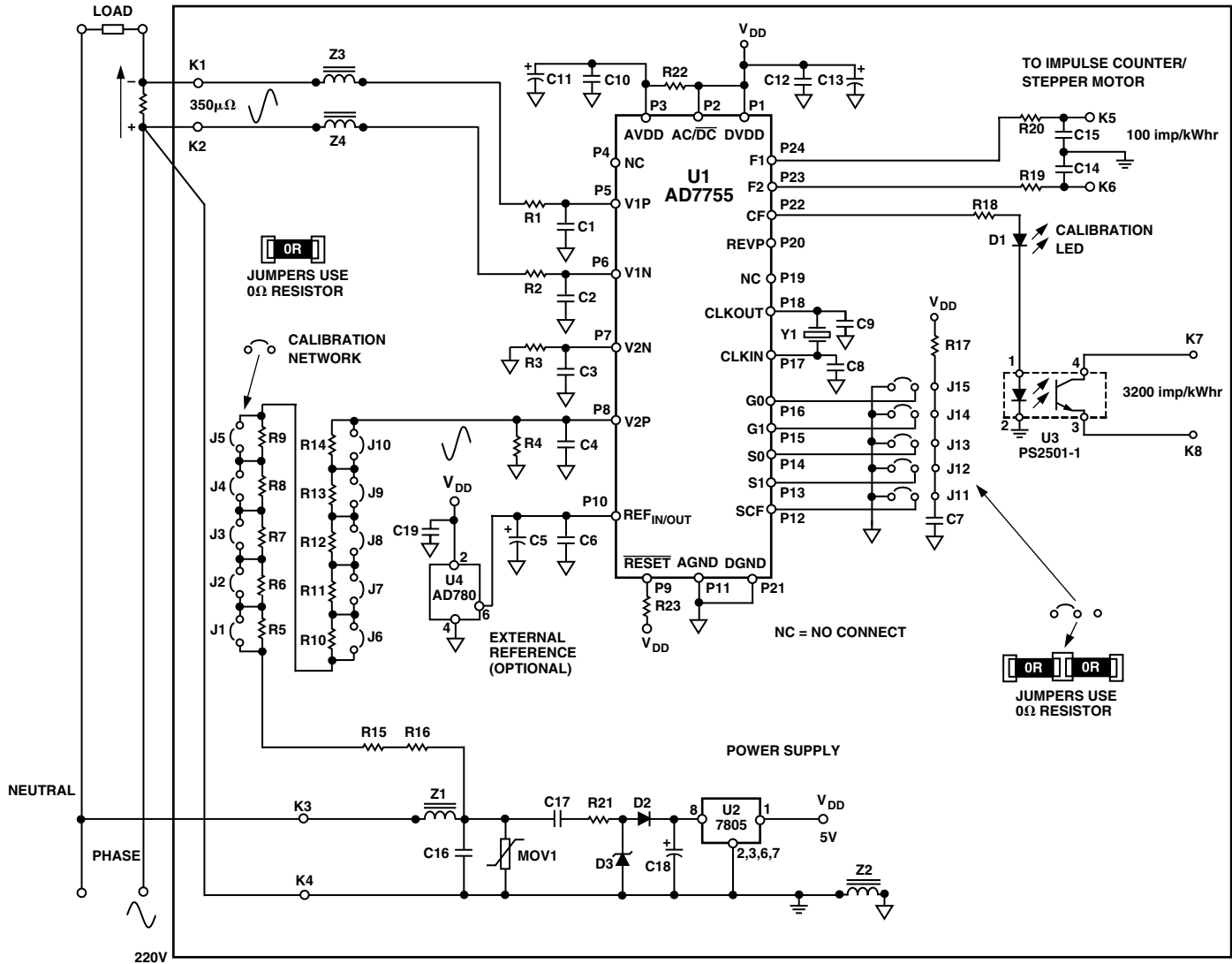


Figure 1. Simple Single-Phase Watt-Hour Meter Based on the AD7755

**DESIGN EQUATIONS**

The AD7755 produces an output frequency that is proportional to the time average value of the product of two voltage signals. The input voltage signals are applied at V1 and V2. The detailed functionality of the AD7755 is explained in the AD7755 data sheet, Theory Of Operation section. The AD7755 data sheet also provides an equation that relates the output frequency on F1 and F2 (counter drive) to the product of the rms signal levels at V1 and V2. This equation is shown here again for convenience and will be used to determine the correct signal scaling at V2 in order to calibrate the meter to a fixed constant.

$$Frequency = \frac{8.06 \times V1 \times V2 \times Gain \times F_{1-4}}{V_{REF}^2} \quad (1)$$

The meter shown in Figure 1 is designed to operate at a line voltage of 220 V and a maximum current ( $I_{MAX}$ ) of

40 A. However, by correctly scaling the signals on Channel 1 and Channel 2, a meter operating of any line voltage and maximum current could be designed.

The four frequency options available on the AD7755 will allow similar meters (i.e., direct counter drive) with an  $I_{MAX}$  of up to 120 A to be designed. The basic current ( $I_b$ ) for this meter is selected as 5 A and the current range for accuracy will be 2%  $I_b$  to  $I_{MAX}$ , or a dynamic range of 400 (100 mA to 40 A). The electromechanical register (kWh) will have a constant of 100 imp/kWh, i.e., 100 impulses from the AD7755 will be required in order to register 1 kWh. IEC1036 section 4.2.11 specifies that electromagnetic registers have their lowest values numbered in ten division, each division being subdivided into ten parts. Hence a display with a five plus one digits is used, i.e., 10,000s, 1,000s, 100s, 10s, 1s, 1/10s. The meter constant (for calibration and test) is selected as 3200 imp/kWh.

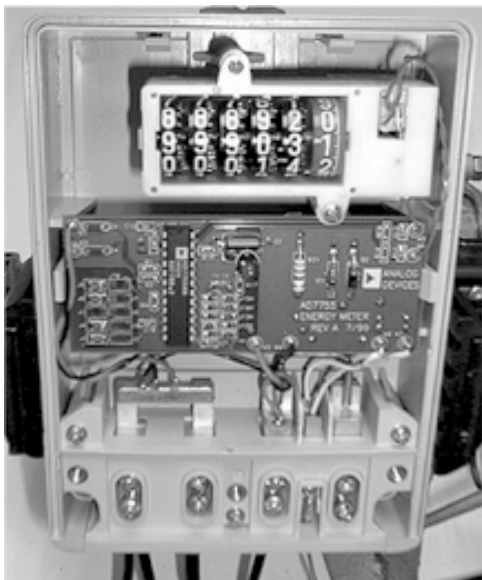


Figure 2. Final Implementation of the AD7755 Meter

#### AD7755 Reference

The schematic in Figure 1 also shows an optional reference circuit. The on-chip reference circuit of the AD7755 has a temperature coefficient of typically 30 ppm/°C. However, on A Grade parts this specification is not guaranteed and may be as high as 80 ppm/°C. At 80 ppm/°C the AD7755 error at -20°C/+60°C could be as high as 0.65%, assuming a calibration at 25°C.

#### Shunt Selection

The shunt size (350  $\mu\Omega$ ) is selected to maximize the use of the dynamic range on Channel V1 (current channel). However there are some important considerations when selecting a shunt for an energy metering application. First, minimize the power dissipation in the shunt. The maximum rated current for this design is 40 A, therefore, the maximum power dissipated in the shunt is  $(40 \text{ A})^2 \times 350 \mu\Omega = 560 \text{ mW}$ . IEC1036 calls for a maximum power dissipation of 2 W (including power supply). Secondly, the higher power dissipation may make it difficult to manage the thermal issues. Although the shunt is manufactured from Manganin material, which is an alloy with a low temperature coefficient of resistance, high temperatures may cause significant error at heavy loads. A third consideration is the ability of the meter to resist attempts to tamper by shorting the phase circuit. With a very low value of shunt resistance the effects of externally shorting the shunt are very much minimized. Therefore, the shunt should always be made as small as possible, but this must be offset against the signal range on V1 (0 mV–20 mV rms with a gain of 16). If the shunt is made too small it will not be possible to meet the IEC1036 accuracy requirements at light loads. A shunt value of 350  $\mu\Omega$  was considered a good compromise for this design.

#### Design Calculations

Design parameters:

Line voltage = 220 V (nominal)

$I_{\text{MAX}} = 40 \text{ A}$  ( $I_b = 5 \text{ A}$ )

Counter = 100 imp/kWh

Meter constant = 3200 imp/kWh

Shunt size = 350  $\mu\Omega$

100 imp/hour = 100/3600 sec = 0.027777 Hz

Meter will be calibrated at  $I_b$  (5A)

Power dissipation at  $I_b = 220 \text{ V} \times 5 \text{ A} = 1.1 \text{ kW}$

Frequency on F1 (and F2) at  $I_b = 1.1 \times 0.027777 \text{ Hz}$   
= 0.0305555 Hz

Voltage across shunt (V1) at  $I_b = 5 \text{ A} \times 350 \mu\Omega = 1.75 \text{ mV}$ .

To select the  $F_{1-4}$  frequency for Equation 1 see the AD7755 data sheet, Selecting a Frequency for an Energy Meter Application section. From Tables V and VI in the AD7755 data sheet it can be seen that the best choice of frequency for a meter with  $I_{\text{MAX}} = 40 \text{ A}$  is 3.4 Hz ( $F_2$ ). This frequency selection is made by the logic inputs S0 and S1—see Table II in the AD7755 data sheet. The CF frequency selection (meter constant) is selected by using the logic input SCF. The two available options are  $64 \times F_1$  (6400 imp/kWh) or  $32 \times F_1$  (3200 imp/kWh). For this design, 3200 imp/kWh is selected by setting SCF logic low. With a meter constant of 3200 imp/kWh and a maximum current of 40 A, the maximum frequency from CF is 7.82 Hz. Many calibration benches used to verify meter accuracy still use optical techniques. This limits the maximum frequency that can be reliably read to about 10 Hz. The only remaining unknown from equation 1 is V2 or the signal level on Channel 2 (the voltage channel).

From Equation 1 on the previous page:

$$0.030555 \text{ Hz} = \frac{8.06 \times 1.75 \text{ mV} \times V2 \times 16 \times 3.4 \text{ Hz}}{2.5^2}$$

$$V2 = 248.9 \text{ mV rms}$$

Therefore, in order to calibrate the meter the line voltage needs to be attenuated down to 248.9 mV.

#### CALIBRATING THE METER

From the previous section it can be seen that the meter is simply calibrated by attenuating the line voltage down to 248.9 mV. The line voltage attenuation is carried out by a simple resistor divider as shown in Figure 3. The attenuation network should allow a calibration range of at least  $\pm 30\%$  to allow for shunt tolerances and the on-chip reference tolerance of  $\pm 8\%$ —see AD7755 data sheet. In addition, the topology of the network is such that the phase-matching between Channel 1 and Channel 2 is preserved, even when the attenuation is being adjusted (see Correct Phase Matching Between Channels section).

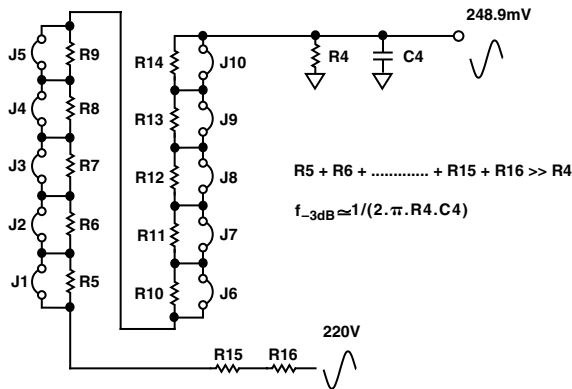


Figure 3. Attenuation Network

As can be seen from Figure 3, the -3 dB frequency of this network is determined by R4 and C4. Even with all the jumpers closed, the resistance of R15 (330 kΩ) and R16 (330 kΩ) is still much greater than R4 (1 kΩ). Hence varying the resistance of the resistor chain R5 to R14 will have little effect on the -3 dB frequency of the network. The network shown in Figure 3 allows the line voltage to be attenuated and adjusted in the range 175 mV to 333 mV with a resolution of 10 bits or 154 μV. This is achieved by using the binary weighted resistor chain R5 to R14. This will allow the meter to be accurately calibrated using a successive approximation technique. Starting with J1, each jumper is closed in order of ascendance, e.g., J1, J2, J3, etc. If the calibration frequency on CF, i.e., 32 × 100 imp/hr (0.9777 Hz), is exceeded when any jumper is closed, it should be opened again. All jumpers are tested, J10 being the last jumper. Note jumper connections are made with 0 Ω fixed resistors which are soldered into place. This approach is preferred over the use of trim pots, as the stability of the latter over time and environmental conditions is questionable.

Since the AD7755 transfer function is extremely linear a one-point calibration (1b) at unity power factor, is all that is needed to calibrate the meter. If the correct precautions have been taken at the design stage, no calibration will be necessary at low-power factor (PF = 0.5). The next section discusses phase matching for correct calculation of energy at low-power factor.

**CORRECT PHASE MATCHING BETWEEN CHANNELS**

The AD7755 is internally phase-matched over the frequency range 40 Hz to 1 kHz. Correct phase matching is important in an energy metering application because any phase mismatch between channels will translate into significant measurement error at low-power factor. This is easily illustrated with the following example. Figure 4 shows the voltage and current waveforms for an inductive load. In the example shown, the current lags the voltage by 60° (PF = -0.5). Assuming pure sinusoidal conditions, the power is easily calculated as  $V_{rms} \times I_{rms} \times \cos(60^\circ)$ .

If, however, a phase error ( $\phi_e$ ) is introduced externally to the AD7755, e.g., in the antialias filters, the error is calculated as:

$$[\cos(\delta^\circ) - \cos(\delta^\circ + \phi_e)] / \cos(\delta^\circ) \times 100\% \tag{2}$$

See Note 3 on Table I. Where  $\delta$  is the phase angle between voltage and current and  $\phi_e$  is the external phase error. With a phase error of 0.2°, for example, the error at PF = 0.5 (60°) is calculated as 0.6%. As this example demonstrates, even a very small phase error will produce a large measurement error at low power factor.

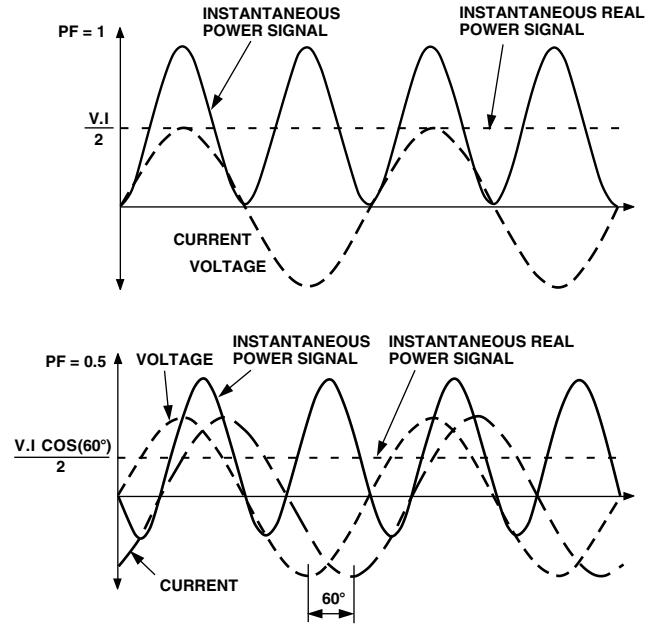


Figure 4. Voltage and Current (Inductive Load)

**ANTI\_ALIAS FILTERS**

As mentioned in the previous section, one possible source of external phase errors are the antialias filters on Channel 1 and Channel 2. The antialias filters are low-pass filters that are placed before the analog inputs of any ADC. They are required to prevent a possible distortion due to sampling called aliasing. Figure 5 illustrates the effects of aliasing.

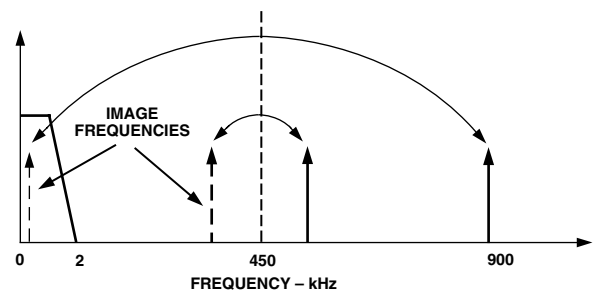


Figure 5. Aliasing Effects

Figure 5 shows how aliasing effects could introduce inaccuracies in an AD7755-based meter design. The AD7755 uses two  $\Sigma$ - $\Delta$  ADCs to digitize the voltage and current signals. These ADCs have a very high sampling rate, i.e., 900 kHz. Figure 5 shows how frequency components (arrows shown in black) above half the sampling frequency (also known as the Nyquist frequency), i.e., 450 kHz is imaged or folded back down below 450 kHz (arrows shown dashed). This will happen with all ADCs no matter what the architecture. In the example shown it can be seen that only frequencies near the sampling frequency, i.e., 900 kHz, will move into the band of interest for metering, i.e., 0 kHz–2 kHz. This fact will allow us to use a very simple LPF (Low-Pass Filter) to attenuate these high frequencies (near 900 kHz) and so prevent distortion in the band of interest.

The simplest form of LPF is the simple RC filter. This is a single-pole filter with a roll-off or attenuation of  $-20$  dB/dec.

#### Choosing the Filter $-3$ dB Frequency

As well as having a magnitude response, all filters also have a phase response. The magnitude and phase response of a simple RC filter ( $R = 1$  k $\Omega$ ,  $C = 33$  nF) are shown in Figures 6 and 7. From Figure 6 it is seen that the attenuation at 900 kHz for this simple LPF is greater than 40 dBs. This is enough attenuation to ensure no ill effects due to aliasing.

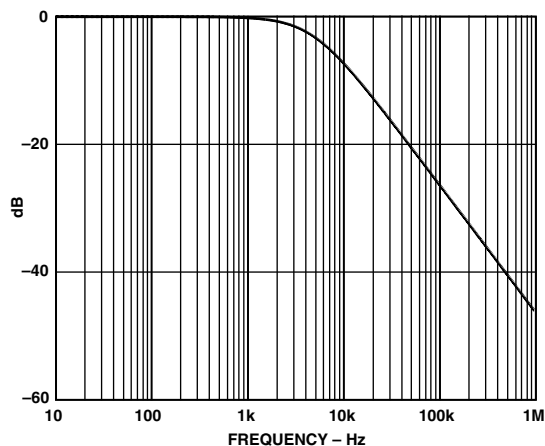


Figure 6. RC Filter Magnitude Response

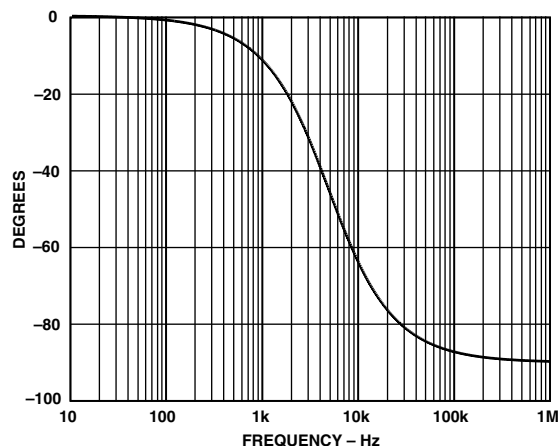


Figure 7. RC Filter Phase Response

As explained in the last section, the phase response can introduce significant errors if the phase response of the LPFs on both Channel 1 and Channel 2 are not matched. Phase mismatch can easily occur due to poor component tolerances in the LPF. The lower the  $-3$  dB frequency in the LPF (antialias filter) the more pronounced these errors will be at the fundamental frequency component or the line frequency. Even with the corner frequency set at 4.8 kHz ( $R = 1$  k $\Omega$ ,  $C = 33$  nF) the phase errors due to poor component tolerances can be significant. Figure 8 illustrates the point. In Figure 8, the phase response for the simple LPF is shown at 50 Hz for  $R = 1$  k $\Omega \pm 10\%$ ,  $C = 33$  nF  $\pm 10\%$ . Remember a phase shift of  $0.2^\circ$  can cause measurement errors of 0.6% at low-power factor. This design uses resistors of 1% tolerance and capacitors of 10% tolerance for the antialias filters to reduce the possible problems due to phase mismatch. Alternatively the corner frequency of the antialias filter could be pushed out to 10 kHz–15 Hz. However, the corner frequency should not be made too high, as this could allow enough high-frequency components to be aliased and so cause accuracy problems in a noisy environment.

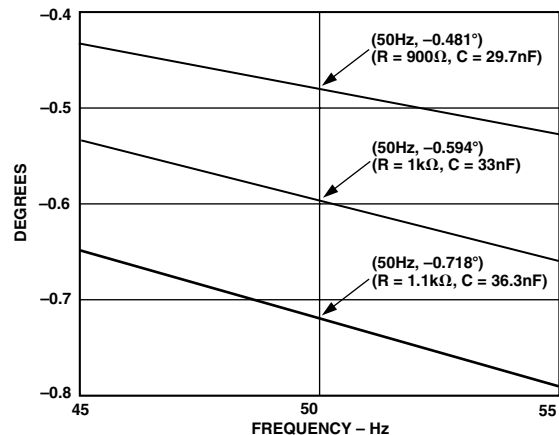


Figure 8. Phase Shift at 50 Hz Due to Component Tolerances

Note that this is also why precautions were taken with the design of the calibration network on Channel 2 (voltage channel). Calibrating the meter by varying the resistance of the attenuation network will not vary the  $-3$  dB frequency and hence the phase response of the network on Channel 2—see Calibrating the Meter section. Shown in Figure 9 is a plot of phase lag at 50 Hz when the resistance of the calibration network is varied from 660 k $\Omega$  (J1–J10 closed) to 1.26 M $\Omega$  (J1–J10 open).

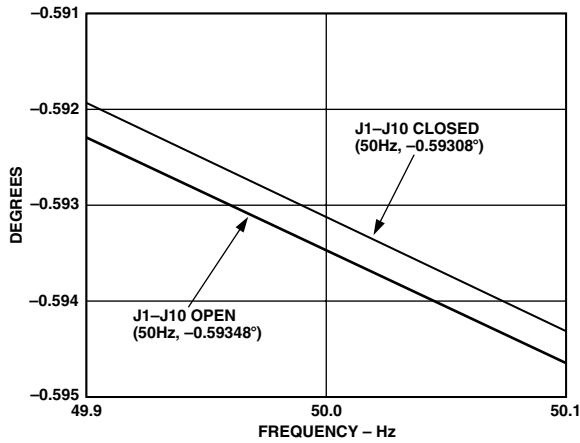


Figure 9. Phase Shift Due to Calibration

## COMPENSATING FOR PARASITIC SHUNT INDUCTANCE

When used at low frequencies a shunt can be considered a purely resistive element with no significant reactive elements. However, under certain situations even a small amount of stray inductance can cause undesirable effects when a shunt is used in a practical data acquisition system. The problem is very noticeable when the resistance of the shunt is very low, in the order of 200  $\mu\Omega$ . Shown below is an equivalent circuit for the shunt used in the AD7755 reference design. There are three connections to the shunt. One pair of connections provides the current sense inputs (V1P and V1N) and the third connection is the ground reference for the system.

The shunt resistance is shown as  $R_{SH1}$  (350  $\mu\Omega$ ).  $R_{SH2}$  is the resistance between the V1N input terminal and the system ground reference point. The main parasitic elements (inductance) are shown as  $L_{SH1}$  and  $L_{SH2}$ . Figure 10 also shows how the shunt is connected to the AD7755 inputs (V1P and V1N) through the antialias filters. The function of the antialias filters is explained in the previous section and their ideal magnitude and phase responses are shown in Figures 6 and 7.

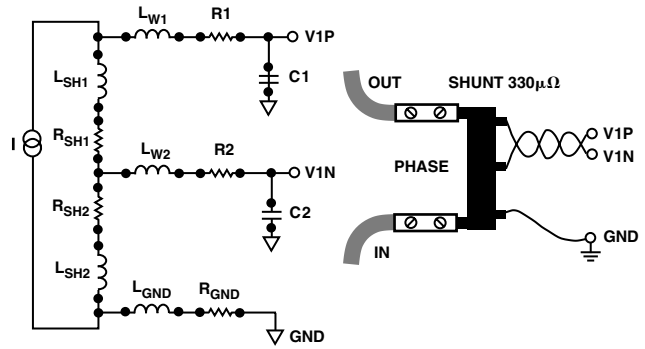


Figure 10. Equivalent Circuit for the Shunt

## Canceling the Effects of the Parasitic Shunt Inductance

The effect of the parasitic shunt inductance is shown in Figure 11. The plot shows the phase and magnitude response of the antialias filter network with and without (dashed) a parasitic inductance of 2 nH. As can be seen from the plot, both the gain and phase response of the network are affected. The attenuation at 1 MHz is now only about  $-15$  dB, which could cause some repeatability and accuracy problems in a noisy environment. More importantly, a phase mismatch may now exist between the current and voltage channels. Assuming the network on Channel 2 has been designed to match the ideal phase response of Channel 1, there now exists a phase mismatch of  $0.1^\circ$  at 50 Hz. Note that  $0.1^\circ$  will cause a 0.3% measurement error at  $PF = \pm 0.5$ . See Equation 2 (Correct Phase Matching Between Channels).

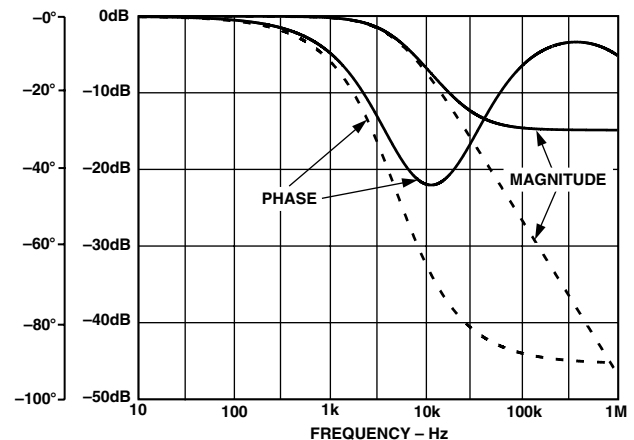


Figure 11. Effect of Parasitic Shunt Inductance on the Antialias Network

The problem is caused by the addition of a zero into the antialias network. Using the simple model for the shunt shown in Figure 10, the location of the zero is given as  $R_{SH1}/L_{SH1}$  radians.

One way to cancel the effects of this additional zero in the network is to add an additional pole at (or close to) the same location. The addition of an extra RC on each analog input of Channel 1 will achieve the additional

pole required. The new antialias network for Channel 1 is shown in Figure 12. To simplify the calculation and demonstrate the principle, the Rs and Cs of the network are assumed to have the same value.

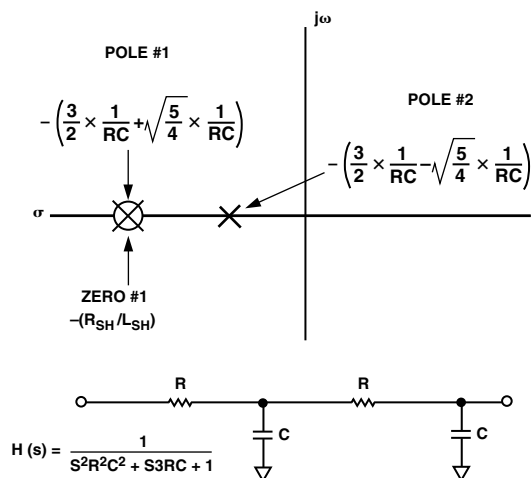


Figure 12. Shunt Inductance Compensation Network

Figure 12 also gives an expression for the location of the poles of this compensation network. The purpose of Pole #1 is to cancel the effects of the zero due to the shunt inductance. Pole #2 will perform the function of the antialias filters as described in the Antialias Filters section. The following illustrates a sample calculation for a shunt of 330 μΩ with a parasitic inductance of 2 nH.

The location of the pole #1 is given as:

$$-\left(\frac{3}{2} \times \frac{1}{RC} + \sqrt{\frac{5}{4}} \times \frac{1}{RC}\right) = \frac{R_{SH1}}{L_{SH1}}$$

For  $R_{SH1} = 330 \mu\Omega$ ,  $L_{SH1} = 2 \text{ nH}$ ,  $C = 33 \text{ nF}$

$R$  is calculated as approximately 480 Ω (use 470 Ω).

The location of Pole #1 is 165,000 rads or 26.26 kHz.

This places the location of Pole # 2 at:

$$-\left(\frac{3}{2} \times \frac{1}{RC} + \sqrt{\frac{5}{4}} \times \frac{1}{RC}\right) = 3.838 \text{ kHz}$$

To ensure phase-matching between Channel 1 and Channel 2, the pole at Channel 2 must also be positioned at this location. With  $C = 33 \text{ nF}$ , the new value of resistance for the antialias filters on Channel 2 is approximately 1.23 kΩ (use 1.2 kΩ).

Figure 13 shows the effect of the compensation network on the phase and magnitude response of the antialias network in Channel 1. The dashed line shows the response of Channel 2 using practical values for the

newly calculated component values, i.e., 1.2 kΩ and 33 nF. The solid line shows the response of Channel 1 with the parasitic shunt inductance included. Notice phase and magnitude responses match very closely with the ideal response—shown as a dashed line. This is the objective of the compensation network.

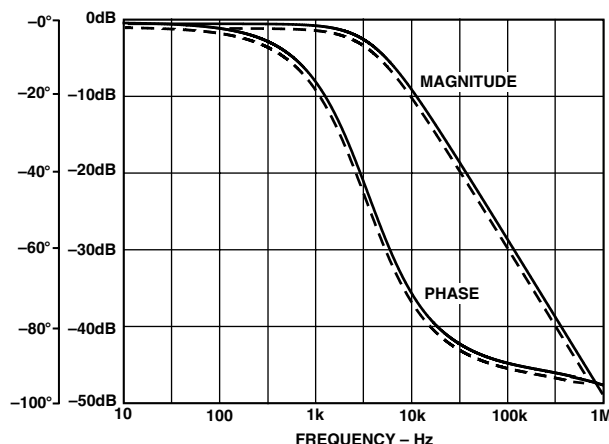


Figure 13. Antialias Network Phase and Magnitude Response after Compensation

The method of compensation works well when the pole due to shunt inductance is less than 25 kHz or so. If zero is at a much higher frequency its effects may simply be eliminated by placing an extra RC on Channel 1 with a pole that is a decade greater than that of the antialias filter, e.g., 100 Ω and 33 nF.

Care should be taken when selecting a shunt to ensure its parasitic inductance is small. This is especially true of shunts with small values of resistance, e.g., <200 μΩ. Note that the smaller the shunt resistance, the lower the zero frequency for a given parasitic inductance (Zero =  $R_{SH1}/L_{SH1}$ ).

**POWER SUPPLY DESIGN**

This design uses a simple low-cost power supply based on a capacitor divider network, i.e., C17 and C18. Most of the line voltage is dropped across C17, a 470 nF 250 V metalized polyester film capacitor. The impedance of C17 dictates the effective VA rating of the supply. However the size of C17 is constrained by the power consumption specification in IEC1036. The total power consumption in the voltage circuit, including power supply, is specified in section 4.4.1.1 of IEC1036 (1996-9). The total power consumption in each phase is 2 W and 10 VA under nominal conditions. The nominal VA rating of the supply in this design is 7 VA. The total power dissipation is approximately 0.5 W. Together with the power dissipated in the shunt at 40 A load, the total power consumption of the meter is 1.06 W. Figure 14 shows the basic power supply design.

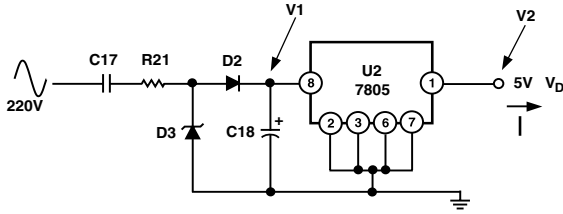


Figure 14. Power Supply

The plots shown in Figures 15, 16, 17, and 18 show the PSU performance under heavy load (50 A) with the line voltage varied from 180 V to 250 V. By far the biggest load on the power supply is the current required to drive the stepper motor which has a coil impedance of about 400 Ω. This is clearly seen by looking at V1 (voltage on C18) in the plots below. Figure 16 shows the current drawn from the supply. Refer to Figure 14 when reviewing the simulation plots below.

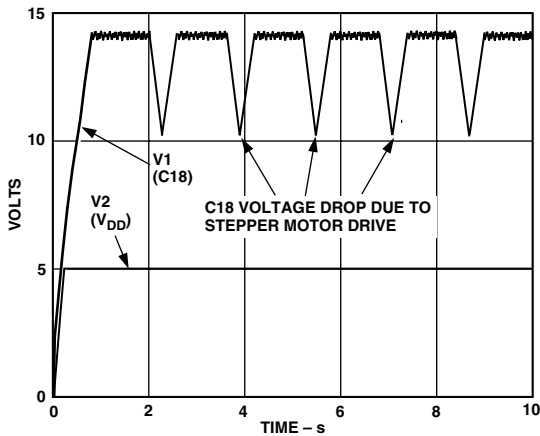


Figure 15. Power Supply Voltage Output at 220 V and 50 A Load

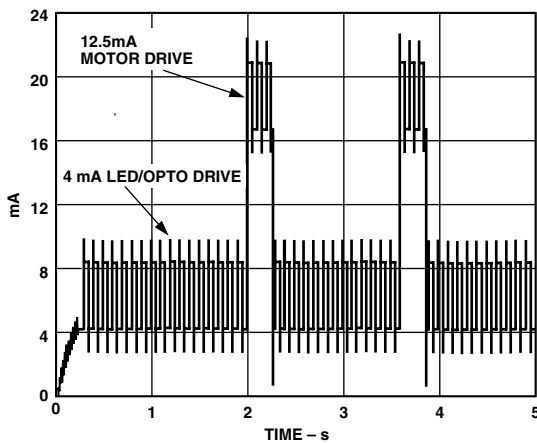


Figure 16. Power Supply Current Output at 220 V and 50 A Load

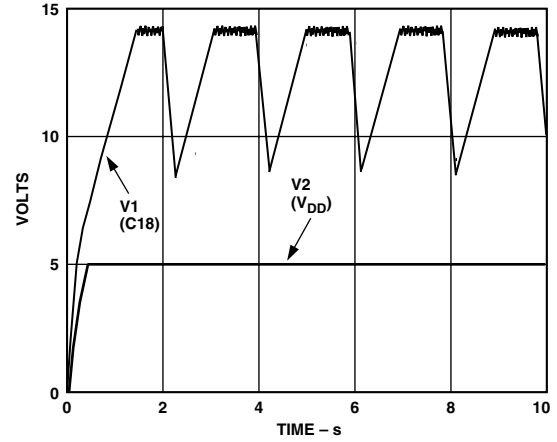


Figure 17. Power Supply Voltage Output at 180 V and 50 A Load

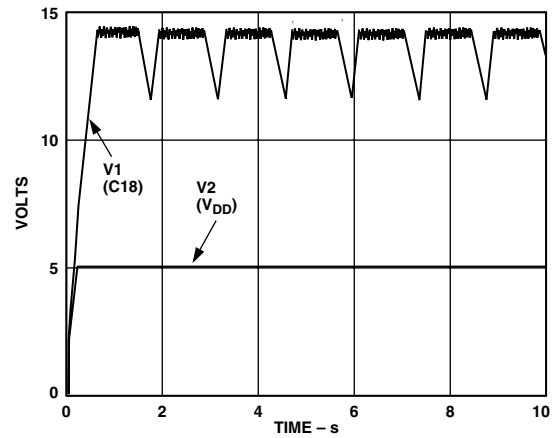


Figure 18. Power Supply Voltage Output at 250 V and 50 A Load

**DESIGN FOR IMMUNITY TO ELECTROMAGNETIC DISTURBANCE**

In Section 4.5 of IEC1036 it is stated that “the meter shall be designed in such a way that conducted or radiated electromagnetic disturbances as well as electrostatic discharge do not damage nor substantially influence the meter.” The considered disturbances are:

1. Electrostatic Discharge
2. Electromagnetic HF Fields
3. Fast Transience Burst

All of the precautions and design techniques (e.g., ferrite beads, capacitor line filters, physically large SMD resistors, PCB layout including grounding) contribute to a certain extent in protecting the meter electronics from each form of electromagnetic disturbance. Some precautions (e.g., ferrite beads), however, play a more important role in the presence of certain kinds of disturbances (e.g., RF and fast transience burst). The following discusses each of the disturbances listed above and details what protection has been put in place.

## ELECTROSTATIC DISCHARGE (ESD)

Although many sensitive electronic components contain a certain amount of ESD protection on-chip, it is not possible to protect against the kind of severe discharge described below. Another problem is that the effect of an ESD discharge is cumulative, i.e., a device may survive an ESD discharge, but it is no guarantee that it will survive multiple discharges at some stage in the future. The best approach is to eliminate or attenuate the effects of the ESD event before it comes in contact with sensitive electronic devices. This holds true for all conducted electromagnetic disturbances. This test is carried out according to IEC1000-4-2, under the following conditions:

- Contact Discharge;
- Test Severity Level 4;
- Test Voltage 8 kV;
- 10 Discharges.

Very often no additional components are necessary to protect devices. With a little care those components already required in the circuit can perform a dual role. For example, the meter must be protected from ESD events at those points where it comes in contact with the “outside world,” e.g., the connection to the shunt. Here the AD7755 is connected to the shunt via two LPFs (antialias filters) which are required by the ADC—see Antialias Filters section. This RC filter can also be enough to protect against ESD damage to CMOS devices. However, some care must be taken with the type of components used. For example, the resistors should not be wire-wound as the discharge will simply travel across them. The resistors should also be physically large to stop the discharge arcing across the resistor. In this design 1/8W SMD 1206 resistors were used in the antialias filters. Two ferrite beads are also placed in series with the connection to the shunt. A ferrite choke is particularly effective at slowing the fast rise time of an ESD current pulse. The high-frequency transient energy is absorbed in the ferrite material rather than being diverted or reflected to another part of the system. (*The properties of ferrite are discussed later.*) The PSU circuit is also directly connected to the terminals of the meter. Here the discharge will be dissipated by the ferrite, the line filter capacitor (C16), and the rectification diodes D2 and D3. The analog input V2P is protected by the large impedance of the attenuation network used for calibration.

Another very common low-cost technique employed to arrest ESD events is to use a spark gap on the component side of the PCB—see Figure 19. However, since the meter will likely operate in an open air environment and be subject to many discharges, this is not recommended at sensitive nodes like the shunt connection. Multiple

discharges could cause carbon buildup across the spark gap which could cause a short or introduce an impedance that will in time affect accuracy. A spark gap was introduced in the PSU after the MOV to take care of any very high amplitude/fast rise time discharges.

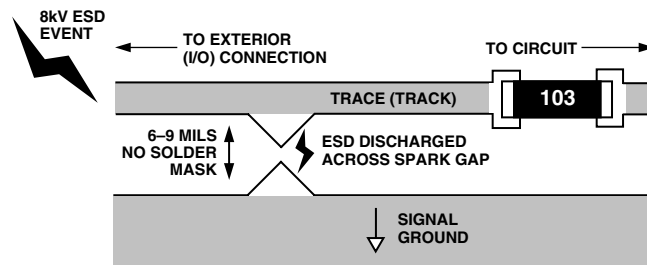


Figure 19. Spark Gap to Arrest ESD Events

## ELECTROMAGNETIC HF FIELDS

Testing is carried out according to IEC100-4-3. Susceptibility of integrated circuits to RF tends to be more pronounced in the 20 MHz–200 MHz region. Frequencies higher than this tend to be shunted away from sensitive devices by parasitic capacitances. In general, at the IC level, the effects of RF in the region 20 MHz–200 MHz will tend to be broadband in nature, i.e., no individual frequency is more troublesome than another. However, there may be higher sensitivity to certain frequencies due to resonances on the PCB. These resonances could cause insertion gain at certain frequencies which, in turn, could cause problems for sensitive devices. By far the greatest RF signal levels are those coupled into the system via cabling. These connection points should be protected. Some techniques for protecting the system are:

1. Minimize Circuit Bandwidth
2. Isolate Sensitive Parts of the System

### Minimize Bandwidth

In this application the required analog bandwidth is only 2 kHz. This is a significant advantage when trying to reduce the effects of RF. The cable entry points can be low-pass filtered to reduce the amount of RF radiation entering the system. The shunt output is already filtered before being connected to the AD7755. This is to prevent aliasing effects that were described earlier. By choosing the correct components and adding some additional components (e.g., ferrite beads) these antialias filters can double as very effective RF filters. Figure 7 shows a somewhat idealized frequency response for the antialias filters on the analog inputs. When considering higher frequencies (e.g., > 1 MHz), the parasitic reactive elements of each lumped component must be considered. Figure 20 shows the antialias filters with the parasitic elements included. These small values of parasitic capacitance and inductance become significant at higher frequencies and therefore must be considered.

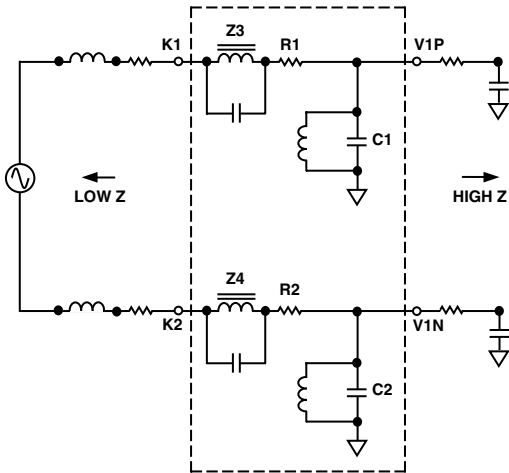


Figure 20. Antialias Filters Showing Parasitics

Parasitics can be kept at a minimum by using physically small components with short lead lengths (i.e., surface mount). Because the exact source impedance conditions are not known (this will depend on the source impedance of the electricity supply), some general precautions should be taken to minimize the effects of potential resonances. Resonances that result from the interaction of the source impedance and filter networks could cause insertion gain effects and so increase the exposure of the system to RF radiation at certain (resonant) frequencies. Lossy (i.e., having large resistive elements) components like capacitors with lossy dielectric (e.g., Type X7R) and ferrite are ideal components for reducing the “Q” of the input network. The RF radiation is dissipated as heat, rather than being reflected or diverted to another part of the system. The ferrite beads Z3 and Z4 perform very well in this respect. Figure 21 shows how the impedance of the ferrite beads varies with frequency.

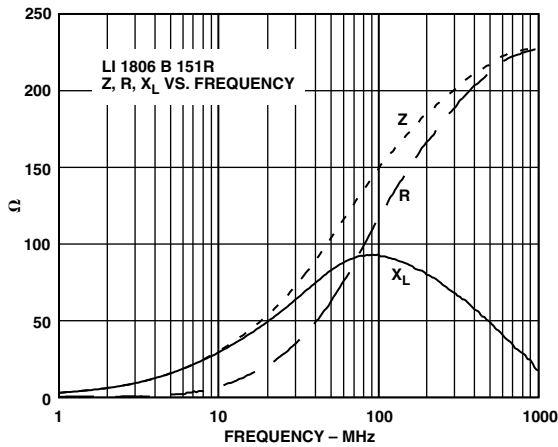


Figure 21. Frequency Response of the Ferrite Chips (Z3 and Z4) in the Antialias Filter

From Figure 21 it can be seen that the ferrite material becomes predominately resistive at high frequencies. Note also that the impedance of the ferrite material

increases with frequency, causing only high (RF) frequencies to be attenuated.

**Isolation**

The shunt connection is the only location where the AD7755 is connected directly (via antialias filters) to the “outside world.” The system is also connected to the phase and neutral lines for the purpose of generating a power supply and voltage channel signal (V2). The ferrite bead (Z1) and line filter capacitor (C16) should significantly reduce any RF radiation on the power supply.

Another possible path for RF is the signal ground for the system. A moating technique has been used to help isolate the signal ground surrounding the AD7755 from the external ground reference point (K4). Figure 22 illustrates the principle of this technique called partitioning or “moating.”

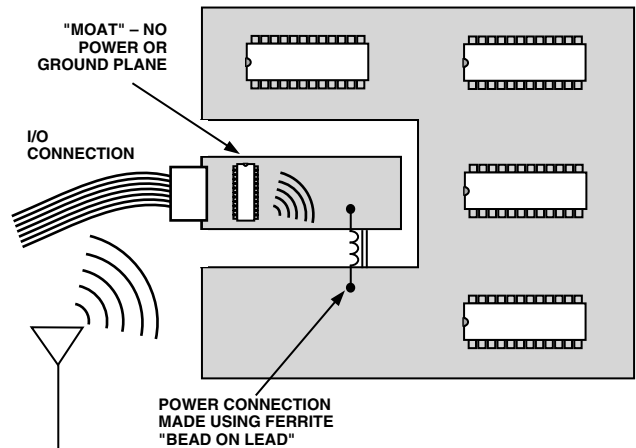


Figure 22. High-Frequency Isolation of I/O Connections Using a Moat

Sensitive regions of the system are protected from RF radiation entering the system at the I/O connection. An area surrounding the I/O connection does not have any ground or power planes. This limits the conduction paths for RF radiation and is called a “moat.” Obviously power, ground, and signal connections must cross this moat and Figure 22 shows how this can be safely achieved by using a ferrite bead. Remember that ferrite offers a large impedance to high frequencies (see Figure 21).

**ELECTRICAL FAST TRANSIENCE (EFT) BURST TESTING**

This testing determines the immunity of a system to conducted transients. Testing is carried out in accordance with IEC1000-4-4 under well-defined conditions. The EFT pulse can be particularly difficult to guard against because the disturbance is conducted into the system via external connections, e.g., power lines. Figure 23 shows the physical properties of the EFT pulse used in IEC1000-4-4. Perhaps the most debilitating attribute of the pulse is not its amplitude (which can be as high as 4 kV), but

the high-frequency content due to the fast rise times involved. Fast rise times mean high-frequency content which allows the pulse to couple to other parts of the system through stray capacitance, etc. Large differential signals can be generated by the inductance of PCB traces and signal ground. These large differential signals could interrupt the operation of sensitive electronic components. Digital systems are generally most at risk because of data corruption. Analog electronic systems tend only to be affected for the duration of the disturbance.

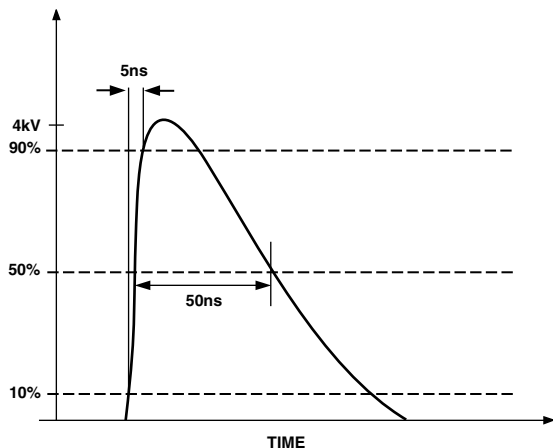


Figure 23. Single EFT Pulse Characteristics

Another possible issue with conducted EFT is that the effects of the radiation will, like ESD, generally be cumulative for electronic components. The energy in an EFT pulse can be as high as 4 mJ and deliver 40 A into a 50  $\Omega$  load (see Figure 26). Therefore continued exposure to EFT due to inductive load switching etc., may have implications for the long-term reliability of components. The best approach is to protect those parts of the system that could be sensitive to EFT.

The protection techniques described in the last section (Electromagnetic HF Fields) also apply equally well in the case of EFT. The electronics should be isolated as much as possible from the source of the disturbance through PCB layout (i.e., moating) and filtering signal and power connections. In addition, a 10 nF capacitor (C16) placed across the mains provides a low impedance shunt for differential EFT pulses. Stray inductance due to leads and PCB traces will mean that the MOV will not be very effective in attenuating the differential EFT pulse. The MOV is very effective in attenuating high energy, relatively long duration disturbances, e.g., due to lightning strikes, etc. The MOV is discussed in the next section.

#### MOV Type S20K275

The MOV used in this design was of type S20K275 from Siemens. An MOV is basically a voltage-dependant resistor whose resistance decreases with increasing voltage. They are typically connected in parallel with the

device or circuit being protected. During an overvoltage event they form a low-resistance shunt and thus prevent any further rise in the voltage across the circuit being protected. The overvoltage is essentially dropped across the source impedance of the overvoltage source, e.g., the mains network source impedance. Figure 24 illustrates the principle of operation.

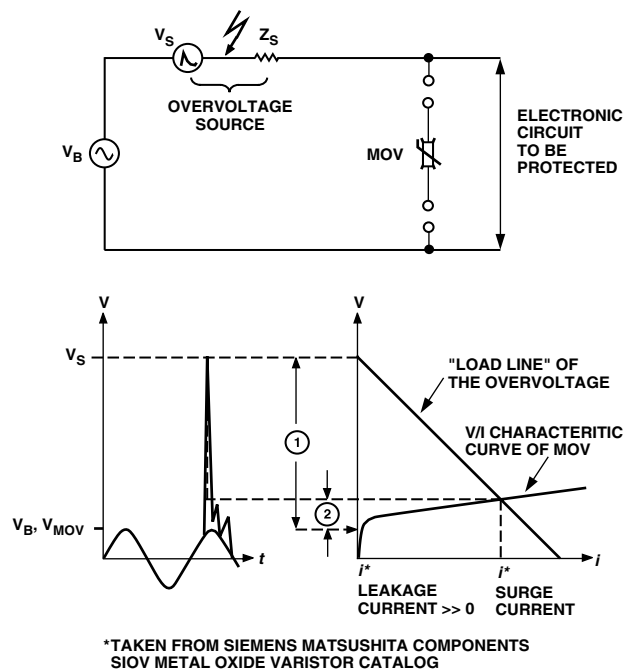


Figure 24. Principle of MOV Overvoltage Protection

The plot in Figure 24 shows how the MOV voltage and current can be estimated for a given overvoltage and source impedance. A load line (open-circuit voltage, short-circuit current) is plotted on the same graph as the MOV characteristic curve. Where the curves intersect, the MOV clamping voltage and current can be read. Note that care must be taken when determining the short-circuit current. The frequency content of the overvoltage must be taken into account as the source impedance (e.g., mains) may vary considerably with frequency. A typical impedance of 50  $\Omega$  is used for mains source impedance during fast transience (high-frequency) pulse testing. The next section discusses IEC1000-4-4 and IEC1000-4-5, which are transience and overvoltage EMC compliance tests.

#### IEC1000-4-4 and the S20K275

While the graphical technique just described is useful, an even better approach is to use simulation to obtain a better understanding of MOV operation. EPCOS Components provides SPICE models for all their MOVs and these are very useful in determining device operation under the various IEC EMC compliance tests. For more information on EPCOS SPICE models and their applications see:

<http://www.epcos.de/inf/70/e0000000.htm>

The purpose of IEC1000-4-4 is to determine the effect of repetitive, low energy, high-voltage, fast rise time pulses on an electronic system. This test is intended to simulate transient disturbances such as those originating from switching transience (e.g., interruption of inductive loads, relay contact bounce, etc.).

Figure 25 shows an equivalent circuit intended to replicate the EFT test pulse as specified in IEC1000-4-4. The generator circuit is based on Figure 1 IEC1000-4-4 (1995-01). The characteristics of operation are:

- Maximum energy of 4 mJ/pulse at 2 kV into 50 Ω
- Source impedance of 50 Ω ± 20%
- DC blocking capacitor of 10 nF
- Pulse rise time of 5 ns ± 30%
- Pulse duration (50% value) of 50 ns ± 30%
- Pulse shape as shown in Figure 23.

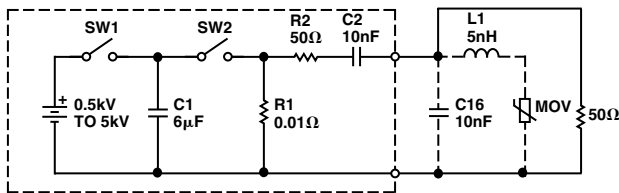


Figure 25. EFT Generator

The simulated output of this generator delivered to a purely resistive 50 Ω load is shown in Figure 26. The open-circuit output pulse amplitude from the generator is 4 kV. Therefore, the source impedance of the generator is 50 Ω as specified by the IEC1000-4-4, i.e., ratio of peak pulse output unloaded and loaded (50 Ω) is 2:1.

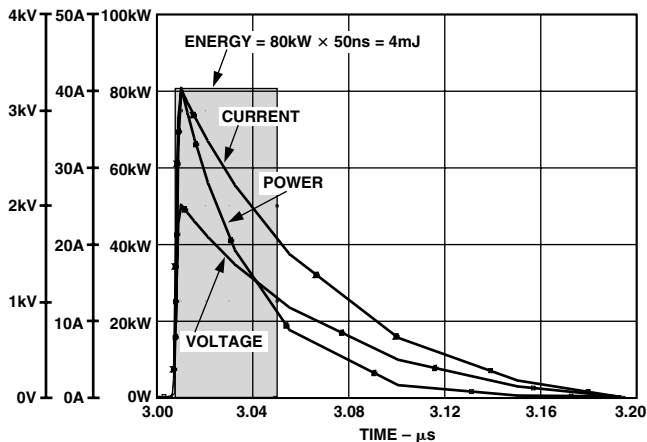


Figure 26. EFT Generator Output into 50 Ω (No Protection)

The plot in Figure 26 also shows the current and instantaneous power ( $V \times I$ ) delivered to the load. The total energy is the integral of the power and can be approximated by the rectangle method as shown. It is approximately 4 mJ at 2 kV as per specification.

Figure 27 shows the generator output into 50 Ω load with the MOV and some inductance (5 nH). This is included to take into account stray inductance due to PCB traces and leads. Although the simulation result shows that the EFT pulse has been attenuated (600 V) and most of the energy being absorbed by the MOV (only 0.8 mJ is delivered to the 50 Ω load) it should be noted that stray inductance and capacitance could render the MOV useless. For example Figure 28 shows the same simulation with the stay inductance increased to 1 µH, which could easily happen if proper care is not taken with the layout. The pulse amplitude reaches 2 kV once again.

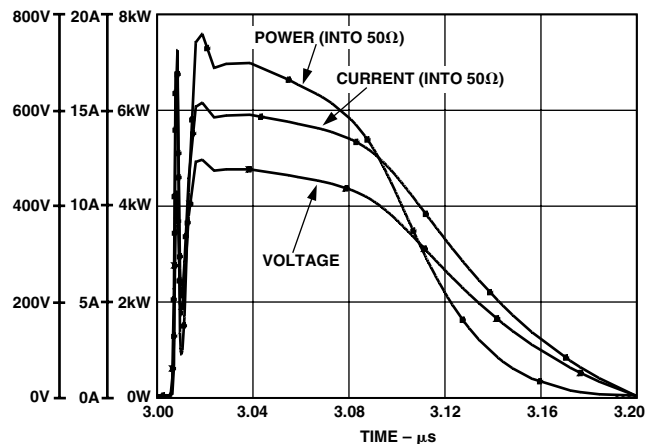


Figure 27. EFT Generator Output into 50 Ω with MOV in Place

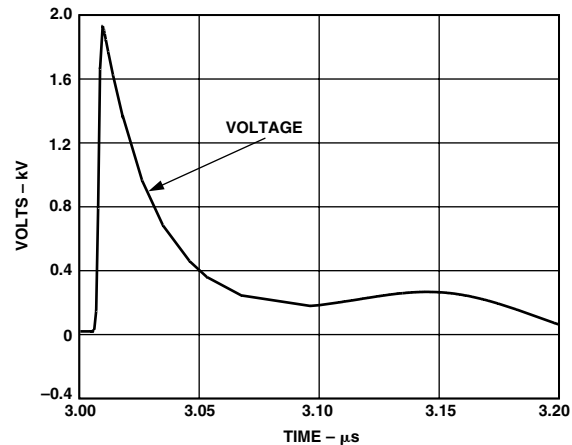


Figure 28. EFT Generator Output into 50 Ω with MOV in Place and Stray Inductance of 1 µH

When the 10 nF Capacitor (C16) is connected, a low impedance path is provided for differential EFT pulses. Figure 29 shows the effect of connecting C16. Here the stray inductance (L1) is left at 1 µH and the MOV is in place. The plot shows the current through C16 and the voltage across the 50 Ω load. The capacitor C16 provides a low impedance path for the EFT pulse. Note the peak current through C16 of 80 A. The result is that the amplitude of the EFT pulse is greatly attenuated.

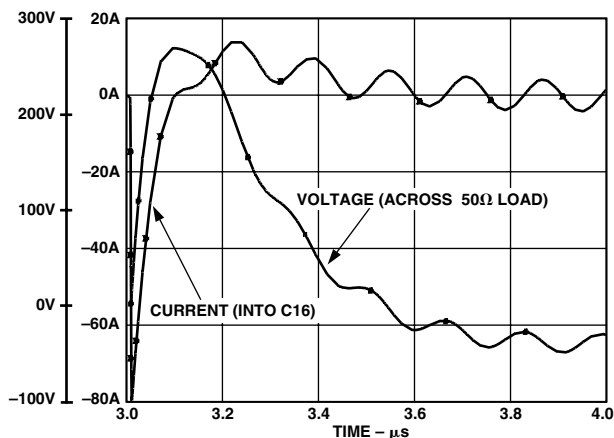


Figure 29. EFT Generator Output into 50 Ω with MOV in Place, Stray Inductance of 1 μH and C16 (10 nF) in Place

**IEC1000-4-5**

The purpose of IEC1000-4-5 is to establish a common reference for evaluating the performance of equipment when subjected to high-energy disturbances on the power and interconnect lines. Figure 30 shows a circuit that was used to generate the combinational wave (hybrid) pulse described in IEC1000-4-5. It is based on the circuit shown in Figure 1 of IEC1000-4-5 (1995-02). Such a generator produces a 1.2 μs/50 μs open-circuit voltage waveform and an 8 μs/20 μs short circuit current waveform, which is why it is referred to as a hybrid generator. The surge generator has an effective output impedance of 2 Ω. This is defined as the ratio of peak open-circuit voltage to peak short-circuit current.

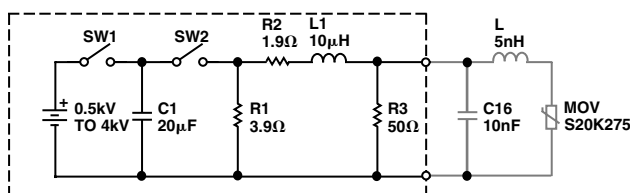


Figure 30. Surge Generator (IEC1000-4-5)

Figure 31 shows the generator voltage and current output waveforms. The characteristics of the combination wave generator are:

Open Circuit Voltage:

- 0.5 kV to at least 4.0 kV
- Waveform as shown in Figure 31
- Tolerance on open-circuit voltage is ±10%.

Short-Circuit Current:

- 0.25 kA to 2.0 kA
- Waveform as shown in Figure 31
- Tolerance on short-circuit current is ±10%.

Repetition rate of a least 60 seconds.

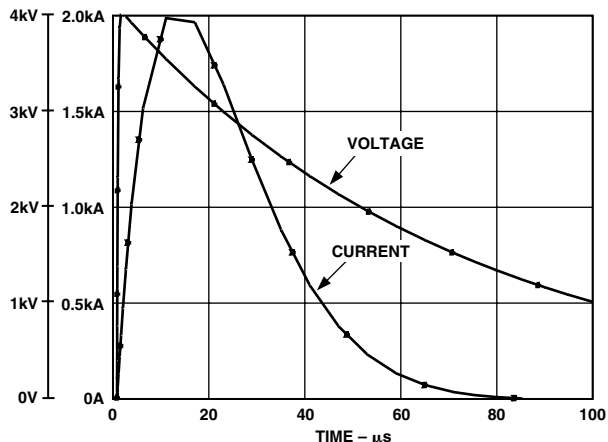


Figure 31. Open-Circuit Voltage/Short-Circuit Current

The MOV is very effective in suppressing these kinds of high energy/long duration surges. Figure 32 shows the voltage across the MOV when it is connected to the generator as shown in Figure 30. Also shown are the current and instantaneous power waveform. The energy absorbed by the MOV is readily estimated using the rectangle method as shown.

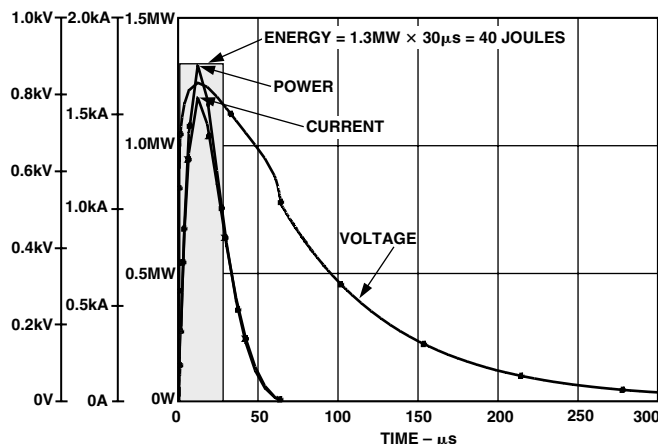


Figure 32. Energy Absorbed by MOV During 4 kV Surge

**Derating the MOV Surge Current**

The maximum surge current (and, therefore, energy absorbed) that an MOV can handle is dependant on the number of times the MOV will be exposed to surges over its lifetime. The life of an MOV is shortened every time it is exposed to a surge event. The data sheet for an MOV device will list the maximum nonrepetitive surge current for an 8 μs/20 μs current pulse. If the current pulse is of longer duration, and if it occurs more than once during the life of the device, this maximum current must be derated. Figure 33 shows the derating curve for the S20K275. Assuming exposures of 30 μs duration, and a peak current as shown in Figure 32, the maximum number of surges the MOV can handle before it goes out of specification is about 10. After repeated loading (10 times in the case just described) the MOV voltage will change. After initially increasing, it will rapidly decay.

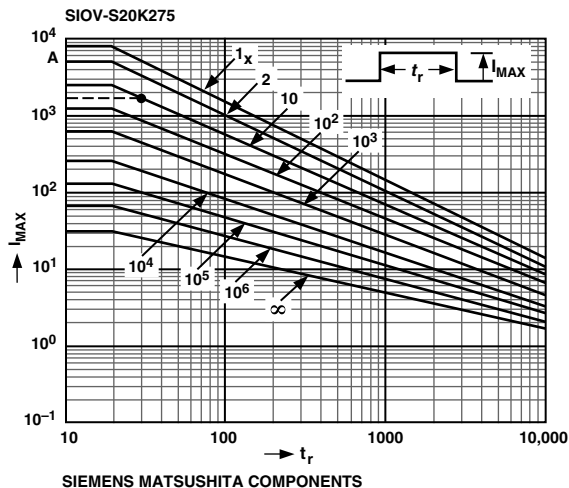


Figure 33. Derating Curve for S20K275

### EMC Test Results

The reference design has been fully tested for EMC at an independent test house. Testing was carried out by Integrity Design & Test Services Inc., Littleton, MA 01460, USA. The reference design was also evaluated for Emissions (EN 55022 Class B) pursuant to IEC 1036:1996 requirements. A copy of the test report can be obtained from the Analog Devices website at:

[http://www.analog.com/techsupt/application\\_notes/ad7755/64567\\_e1.pdf](http://www.analog.com/techsupt/application_notes/ad7755/64567_e1.pdf)

The design was also evaluated for susceptibility to electrostatic discharge (ESD), radio frequency interference (RFI), keyed radio frequency interference, and electrical fast transients (EFT), pursuant to IEC 1036:1996 requirements. The test report is available at:

[http://www.analog.com/techsupt/application\\_notes/ad7755/64567\\_c1.pdf](http://www.analog.com/techsupt/application_notes/ad7755/64567_c1.pdf)

A copy of the certification issued for the design is shown in the test results section of this application note.

### PCB DESIGN

Both susceptibility to conducted or radiated electromagnetic disturbances and analog performance were considered at the PCB design stage. Fortunately, many of the design techniques used to enhance analog and mixed-signal performance also lend themselves well to improving the EMI robustness of the design. The key idea is to isolate that part of the circuit that is sensitive to noise and electromagnetic disturbances. Since the AD7755 carries out all the data conversion and signal processing, the robustness of the meter will be determined to a large extent by how protected the AD7755 is.

In order to ensure accuracy over a wide dynamic range, the data acquisition portion of the PCB should be kept as quiet as possible, i.e., minimal electrical noise. Noise

will cause inaccuracies in the analog-to-digital conversion process that takes place in the AD7755. One common source of noise in any mixed-signal system is the ground return for the power supply. Here high-frequency noise (from fast edge rise times) can be coupled into the analog portion of the PCB by the common impedance of the ground return path. Figure 34 illustrates the mechanism.

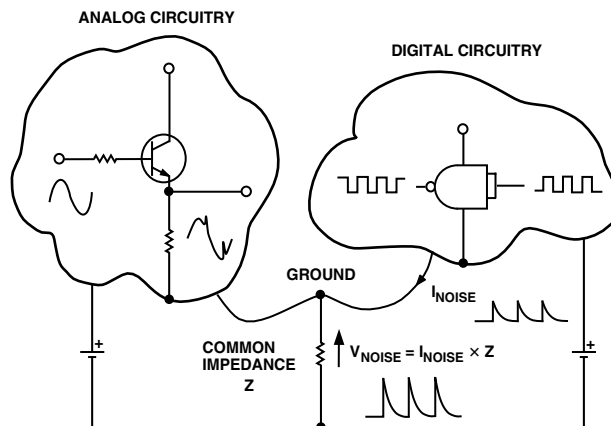


Figure 34. Noise Coupling via Ground Return Impedance

One common technique to overcome these kinds of problems is to use separate analog and digital return paths for the supply. Also, every effort should be made to keep the impedance of these return paths as low as possible. In the PCB design for the AD7755, separate ground planes were used to isolate the noisy ground returns. The use of ground plane also ensures the impedance of the ground return path is kept as very low.

The AD7755 and sensitive signal paths are located in a “quiet” part of the board that is isolated from the noisy elements of the design like the power supply, flashing LED, etc. Since the PSU is capacitor-based, a substantial current (approximately 32 mA at 220 V) will flow in the ground return back to the phase wire (system ground). This is shown in Figure 35. By locating the PSU in the digital portion of the PCB, this return current is kept away from the AD7755 and analog input signals. This current is at the same frequency as the signals being measured and could cause accuracy issues (e.g., crosstalk between the PSU as analog inputs) if care is not taken with the routing of the return current. Also, part of the attenuation network for the Channel 2 (voltage channel) is in the digital portion of the PCB. This helps to eliminate possible crosstalk to Channel 1 by ensuring analog signal amplitudes are kept as low as possible in the analog (“quiet”) portion of the PCB. Remember that with a shunt size of 350  $\mu\Omega$ , the voltage signal range on Channel 1 is 35  $\mu\text{V}$  to 14 mV (2%  $I_b$  to 800%  $I_b$ ). Figure 35 shows the PCB floor plan which was eventually adopted for the watt-hour meter.

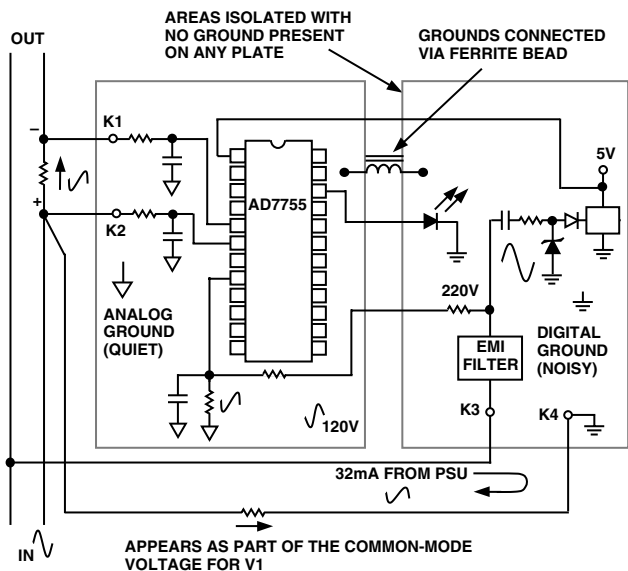


Figure 35. AD7755 Watt-Hour Meter PCB Design

The partitioning of the power planes in the PCB design as shown in Figure 35 also allows us to implement the idea of a “moat” for the purposes of immunity to electromagnetic disturbances. The digital portion of the PCB is the only place where both phase and neutral wires are connected. This portion of the PCB contains the transience suppression circuitry (MOV, ferrite, etc.) and power supply circuitry. The ground planes are connected via a ferrite bead that helps to isolate the analog ground from high-frequency disturbances (see Design For Immunity to Electromagnetic Disturbances section).

**METER ACCURACY/TEST RESULTS**

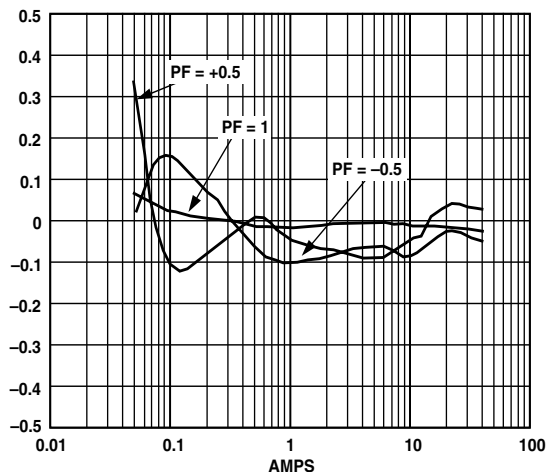


Figure 36. Measurement Error (% Reading) @ 25°C, 220 V, PF = +0.5/-0.5, Frequency = 50 Hz

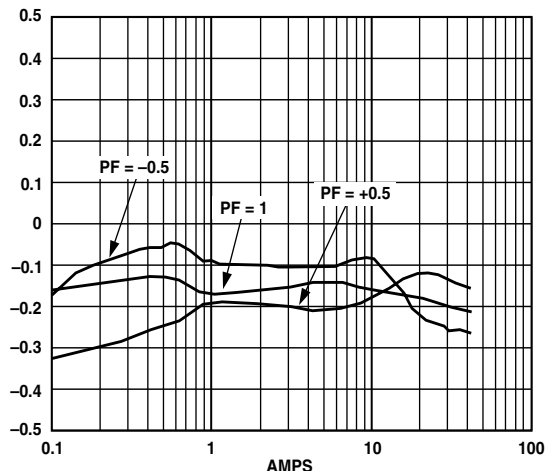


Figure 37. Measurement Error (% Reading) @ 70°C, 220 V, PF = +0.5/-0.5, Frequency = 50 Hz

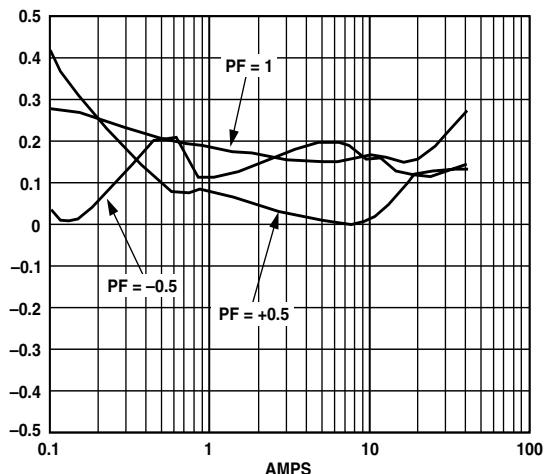


Figure 38. Measurement Error (% Reading) @ -25°C, 220 V, PF = +0.5/-0.5, Frequency = 50 Hz

**EMISSIONS TESTING (EMC) N55022:1994**

At end of data sheet.

**SUSCEPTIBILITY TESTING (EMC) EN 61000-4-2, EN 61000-4-3, EN 61000-4-4, ENV 50204**

At end of data sheet.

**ANSI C12.16 AND IEC1039**

The ANSI standard governing Solid-State Electricity Meters is ANSI C12.16-1991. Since this application note refers to the IEC 1036 specifications when explaining the design, this section will explain some of those key IEC1036 specifications in terms of their ANSI equivalents. This should help eliminate any confusion caused by the different application of some terminology contained in both standards.

## **Class—IEC1036**

The class designation of an electricity meter under IEC1036 refers to its accuracy. For example a Class 1 meter will have a deviation from reference performance of no more than 1%. A Class 0.5 meter will have a maximum deviation of 0.5% and so on. Under ANSI C12.16 Class refers to the maximum current the meter can handle for rated accuracy. The given classes are: 10, 20, 100, 200 and 320. These correspond to a maximum meter current of 10 A, 20 A, 100 A, 200 A and 320 A respectively.

## **I<sub>basic</sub> (I<sub>b</sub>)—IEC1036**

The basic current (I<sub>b</sub>) is a value of current with which the operating range of the meter is defined. IEC1036 defines the accuracy class of a meter over a specific dynamic range, e.g.,  $0.05 I_b \leq I \leq I_{MAX}$ . It is also used as the test load when specifying the maximum permissible effect of influencing factors, e.g., voltage variation and frequency variation. The closest equivalent in ANSI C12.16 is the Test Current. The Test Current for each meter class (maximum current) is given below:

Class 10 : 2.5 A  
Class 20 : 2.5 A  
Class 100 : 15 A  
Class 200 : 30 A  
Class 320 : 50 A

## **I<sub>MAX</sub>—IEC1036**

I<sub>MAX</sub> is the maximum current for which the meter meets rated accuracy. This would correspond to the meter class under ANSI C12.16. For example a meter with an I<sub>MAX</sub> of 20 A under IEC 1026 would be designated Class 20 under ANSI C12.16.

## **NO LOAD THRESHOLD**

The AD7755 has on-chip anticreep functionality. The AD7755 will not produce a pulse on CF, F1, or F2 if the output frequency falls below a certain level. This feature ensures that the energy meter will not register energy when no load is connected. IEC 1036 (1996-09) section 4.6.4 specifies the start-up current as being not more than 0.4% I<sub>b</sub> at PF = 1. For this design the start current is calculated at 7.8 mA or 0.16% I<sub>b</sub>—see No Load Threshold section in the AD7755 data sheet.

## Bill of Materials

Part(s)	Details	Comments
R1, R2, R3, R4	1 k $\Omega$ , 1%, 1/8 W	SMD 1206 Resistor Surface Mount, Panasonic ERJ-8ENF1001 Digi-Key No. P 1K FCT-ND
R5	300 k $\Omega$ , 5%, 1/2 W, 200 V	SMD 2010 Resistor Surface Mount, Panasonic, ERJ-12ZY304 Digi-Key No. P 300K WCT-ND
R6	150 k $\Omega$ , 5%, 1/2 W, 200 V	SMD 1210 Resistor Surface Mount, Panasonic, ERJ-14YJ154 Digi-Key No. P 150K VCT-ND
R7	75 k $\Omega$ , 5%, 1/8 W, 200 V	SMD 1206 Resistor Surface Mount, Panasonic, ERJ-8GEYJ753 Digi-Key No. P 75K ECT-ND
R8	39 k $\Omega$ , 5%, 1/16 W, 50 V	SMD 0402 Resistor Surface Mount, Panasonic, ERJ-2GEJ393 Digi-Key No. P 39K JCT-ND
R9	18 k $\Omega$ , 5%, 1/16 W, 50 V	SMD 0402 Resistor Surface Mount, Panasonic, ERJ-2GEJ183 Digi-Key No. P 18K JCT-N
R10	9.1 k $\Omega$ , 5%, 1/16 W, 50 V	SMD 0402 Resistor Surface Mount, Panasonic, ERJ-2GEJ912 Digi-Key No. P 9.1K JCT-ND
R11	5.1 k $\Omega$ , 5%, 1/16 W, 50 V	SMD 0402 Resistor Surface Mount, Panasonic, ERJ-2GEJ512 Digi-Key No. P 5.1K JCT-ND
R12	2.2 k $\Omega$ , 5%, 1/16 W, 50 V	SMD 0402 Resistor Surface Mount, Panasonic, ERJ-2GEJ222 Digi-Key No. P 2.2K JCT-ND
R13	1.2 k $\Omega$ , 5%, 1/16 W, 50 V	SMD 0402 Resistor Surface Mount, Panasonic, ERJ-2GEJ122 Digi-Key No. P 1.2K JCT-ND
R14	560 $\Omega$ , 5%, 1/16 W, 50 V	SMD 0402 Resistor Surface Mount, Panasonic, ERJ-2GEJ561 Digi-Key No. P 560 JCT-ND
R15, R16	330 k $\Omega$ , 5%, 1/2 W, 200 V	SMD 2010 Resistor Surface Mount, Panasonic, ERJ-12ZY334 Digi-Key No. P 330K WCT-ND
R17, R23	1 k $\Omega$ , 5%, 1/8 W, 200 V	SMD 1206 Resistor Surface Mount, Panasonic, ERJ-8GEYJ102 Digi-Key No. P 1K ECT-ND
R18	820 $\Omega$ , 5%, 1/8 W, 200 V	SMD 1206 Resistor Surface Mount, Panasonic, ERJ-8GEYJ821 Digi-Key No. P 820 ECT-ND
R19, R20	20 $\Omega$ , 5%, 1/8 W, 200 V	Resistor Surface Mount, Panasonic, ERJ-8GEYJ200 Digi-Key No. P 20 ECT-ND
R21	470 $\Omega$ , 5%, 1 W	Through-hole, Panasonic, Digi-Key No. P470W-1BK-ND
R22	10 $\Omega$ , 5%, 1/8 W, 200 V	SMD 1206 Resistor Surface Mount, Panasonic, ERJ-8GEYJ100 Digi-Key No. P 10 ECT-ND
C1, C2, C3, C4	33 nF, Multilayer Ceramic, 10% 50 V, X7R	SMD 0805 Capacitor Surface Mount, Panasonic, ECJ-2VB1H333K Digi-Key No. PCC 1834 CT-ND
C5, C13	10 $\mu$ F, 6.3 V	EIA size A Capacitor Surface Chip-Cap, Panasonic, ECS-TOJY106R Digi-Key No. PCS 1106CT-ND – 3.2 mm $\times$ 1.6 mm

# AN-559

Part(s)	Details	Comments
C6, C7, C10, C12, C14, C15, C19	100 nF, Multilayer Ceramic, 10%, 16 V, X7R	SMD 0805 Capacitor Surface Mount, Panasonic, ECJ-2VB1E104K Digi-Key No. PCC 1812 CT-ND
C8, C9	22 pF, Multilayer Ceramic, 5%, 50 V, NPO	SMD 0402 Capacitor Surface Mount, Panasonic, ECU-E1H220JCQ Digi-Key No. PCC 220CQCT-ND
C11	6.3 V, 220 μF, Electrolytic	Through-hole Panasonic, ECA-OJFQ221 Digi-Key P5604 – ND D = 6.3 mm, H = 11.2 mm, Pitch = 2.5 mm, Dia. = 0.5 mm
C16	10 nF, 250 V, Class X2	Metallized Polyester Film Through-Hole Panasonic, ECQ-U2A103MN Digi-Key No. P4601-ND
C17	470 nF, 250 V AC	Metallized Polyester Film Through-Hole Panasonic, ECQ-E6474KF Digi-Key No. EF6474-NP
C18	35 V, 470 μF, Electrolytic	Through-Hole Panasonic, ECA-1VHG471 Digi-Key P5554 – ND
U1	AD7755AN	Supplied by ADI – 24 Pin DIP, Use Pin Receptacles (P1–P24)
U2	LM78L05	National Semiconductor, LM78L05ACM, S0-8 Digi-Key LM78L05ACM-ND
U3	PS2501-1	Opto, NEC, Digi-key No PS2501-1NEC-ND
U4	AD780BRS	Supplied by ADI – 8 Pin SOIC
D1	Low Current LED	HP HLMP-D150 Newark 06F6429 (Farnell 323-123)
D2	Rectifying Diode	1 W, 400 V, DO-41, 1N4004, Digi-Key 1N4004DICT-ND
D3	Zener Diode	15 V, 1 W, DO-41, 1N4744A Digi-Key 1N4744ADICT-ND
Z1, Z2	Ferrite Bead Cores	Axial-Leaded (15 mm × 3.8 mm ) 0.6 mm Lead Diameter Panasonic, EXCELSA391, Digi-Key P9818BK-ND
Z3, Z4	Ferrite SMD Bead	SMD 1806 Steward, LI 1806 E 151 R Digi-Key 240-1030-1-ND
Y1	3.579545 MHz XTAL	Quartz Crystal, HC-49(US), ECS No. ECS-35-17-4 Digi-Key No. X079-ND
MOV1	Metal Oxide Varistors	AC 275 V, 140 Joules FARNELL No. 580-284, Siemens, S20K275
J1–J10	0.1 Ω, 5%, 1/4 W, 200 V	SMD 1210 Resistor Surface Mount, Panasonic ERJ-14RSJ0R1, Digi-Key No. P0.1SCT-ND
J11–J15	0 Ω, 5%, 1/8 W, 200 V	SMD 1206 Resistor Surface Mount, Panasonic, ERJ-8GEYJ000 Digi-Key No. P0.0ECT-ND
P1–P24	Single Low Profile	Sockets for U1 0.022" to 0.025" Pin Diameter ADI Stock 12-18-33. ADVANCE KSS100-85TG
K1–K8	Pin Receptacles	0.037" to 0.043" Pin Diameter, Hex Press Fit Mil-Max no. 0328-0-15-XX-34-XX-10-0 Digi-Key ED5017-ND
Counter	2 Phase Stepper, 100 imp	China National Electronics Import & Export Shaanxi Co. No.11 A, Jinhua northern Road, Xi'an China. Email: chenyf@public.xa.sn.cn Tel: 86-29 3218247,3221399 Fax: 86-29 3217977, 3215870

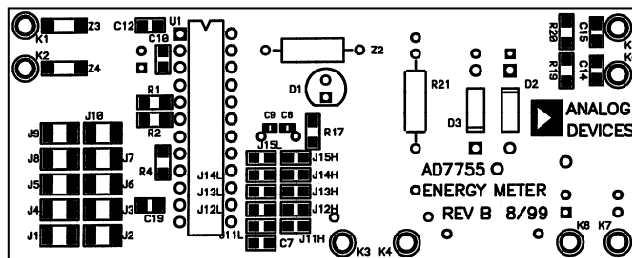


Figure 39. PCB Assembly (Top Layer)

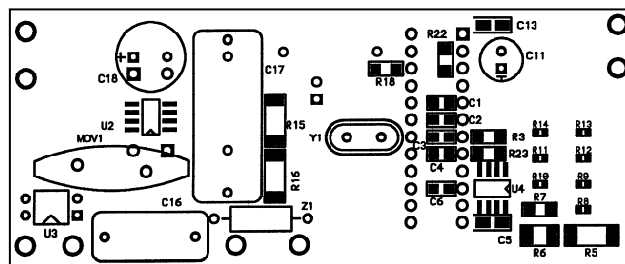


Figure 40. PCB Assembly (Bottom Layer)

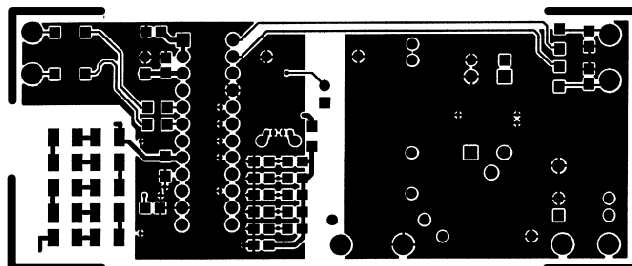


Figure 41. PCB (Top Layer)

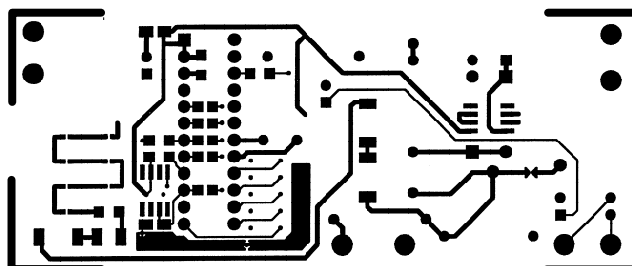


Figure 42. PCB (Bottom Layer)

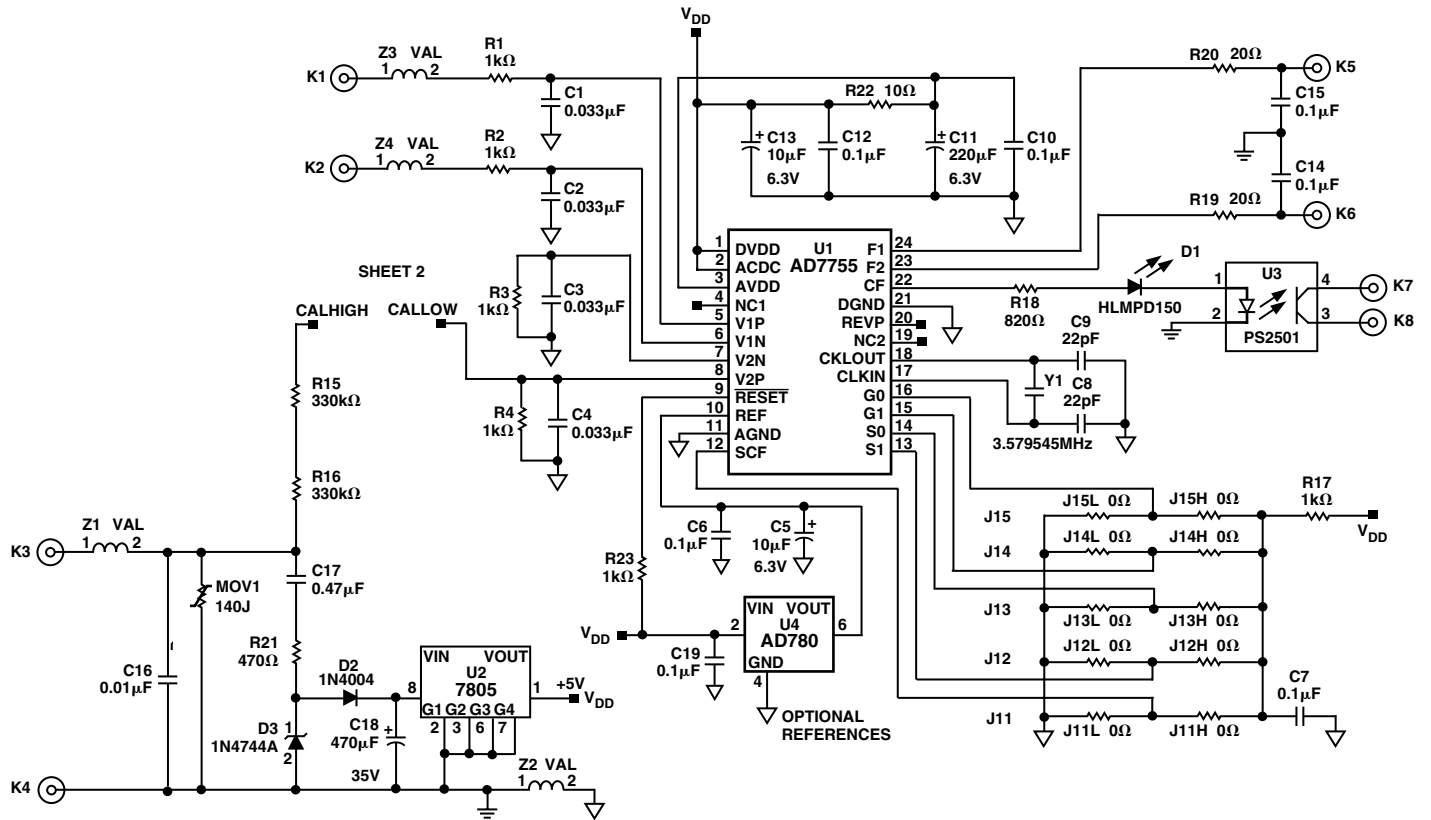


Figure 43. Schematic 1

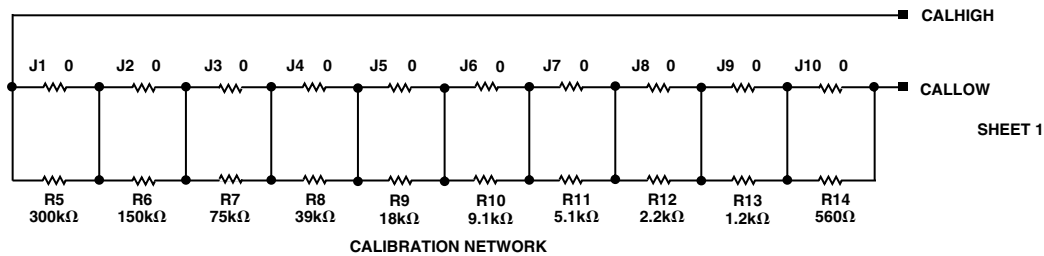


Figure 44. Schematic 2

					
<h2 style="margin: 0;">Certificate of Compliance</h2>					
<p>The following product was found to comply with the requirement stated below when tested in accordance with the test procedures described in the accompanying test/measurement report. Reference report number 64567.e1</p>					
Manufacturer:	Analog Devices, Inc. 804 Woburn Street Wilmington, MA 01887				
Model:	Energy Meter (AD7755)				
Requirement:	EN55022:1994 + A1:1995 + A2:1997, Class B				
Applicable Directive:	89/336/EEC				
Approved By:					
<table border="1" style="width: 100%;"> <tr> <td style="padding: 5px;">Robert D. Goyette NVLAP Signatory</td> <td style="text-align: center; vertical-align: middle;">  </td> </tr> <tr> <td style="text-align: center; padding: 5px;">Date</td> <td style="text-align: center; vertical-align: middle;"> <p>9/13/99</p> </td> </tr> </table>	Robert D. Goyette NVLAP Signatory		Date	<p>9/13/99</p>	
Robert D. Goyette NVLAP Signatory					
Date	<p>9/13/99</p>				
Remarks:	<p><i>Testing is performed using calibrated equipment traceable to the National Institute of Standards and Technology (NIST).</i></p> <p><i>This certificate is valid for products tested as described in the accompanying test report. Specific modifications necessary to meet the above requirement, recommended by Integrity Design &amp; Test Services, Inc. are described therein.</i></p> <p style="text-align: center;"><i>Integrity Design &amp; Test Services, Inc. is accredited by the National Voluntary Laboratory Accreditation Program (NVLAP) for Electromagnetic Emissions Testing</i></p>				

Figure 45. Certificate 1, Emissions Testing



**Integrity**  
 Design & Test  
 Services, Inc.

**Certificate of Compliance**

The following product was found to comply with the requirement stated below when tested in accordance with the test procedures described in the accompanying test/measurement report. Reference report number 64567.c1

Manufacturer: Analog Devices, Inc.  
 804 Woburn Street  
 Wilmington, MA 01887

Model Number: Solid State Energy Meter

Requirement: EN 61000-4-2:1996, EN 61000-4-3:1996,  
 ENV 50204:1993 and EN 61000-4-4:1995  
 (pursuant to IEC 1036:1996)

Applicable Directive: 89/336/EEC

Approved By:

Christopher P. Burch Immunity Section Manager	<i>Christopher P. Burch</i>
Date	9-13-99

Remarks: *Testing is performed using calibrated equipment traceable to the National Institute of Standards and Technology (NIST).*

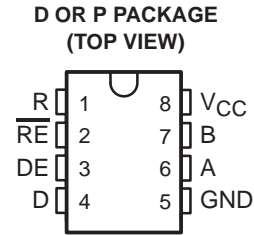
*This certificate is valid for products tested as described in the accompanying test report. Specific modifications necessary to meet the above requirement, recommended by Integrity Design & Test Services, Inc. are described therein.*

Figure 46. Certificate 2, Susceptibility

# SN75176A DIFFERENTIAL BUS TRANSCEIVER

SLLS100A – JUNE 1984 – REVISED MAY 1995

- Bidirectional Transceiver
- Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and ITU Recommendation V.11
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability . . .  $\pm 60$  mA Max
- Thermal-Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Impedance . . . 12 k $\Omega$  Min
- Receiver Input Sensitivity . . .  $\pm 200$  mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates From Single 5-V Supply
- Low Power Requirements



## description

The SN75176A differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus-transmission lines. It is designed for balanced transmission lines and meets ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11.

The SN75176A combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or  $V_{CC} = 0$ . These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 k $\Omega$ , an input sensitivity of  $\pm 200$  mV, and a typical input hysteresis of 50 mV.

The SN75176A can be used in transmission-line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

The SN75176A is characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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# SN75176A DIFFERENTIAL BUS TRANSCEIVER

SLLS100A – JUNE 1984 – REVISED MAY 1995

## Function Tables

### DRIVER

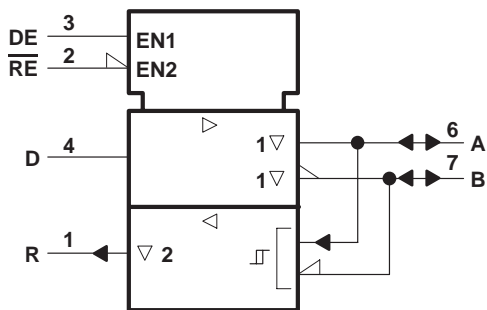
INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

### RECEIVER

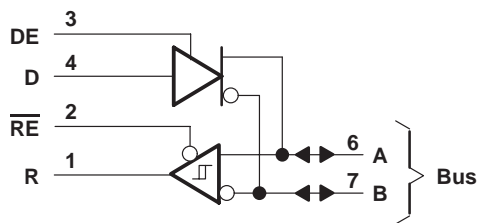
DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2 V$	L	H
$-0.2 V < V_{ID} < 0.2 V$	L	?
$V_{ID} \leq -0.2 V$	L	L
X	H	Z
Open	L	?

H = high level, L = low level, ? = indeterminate,  
X = irrelevant, Z = high impedance (off)

### logic symbol†

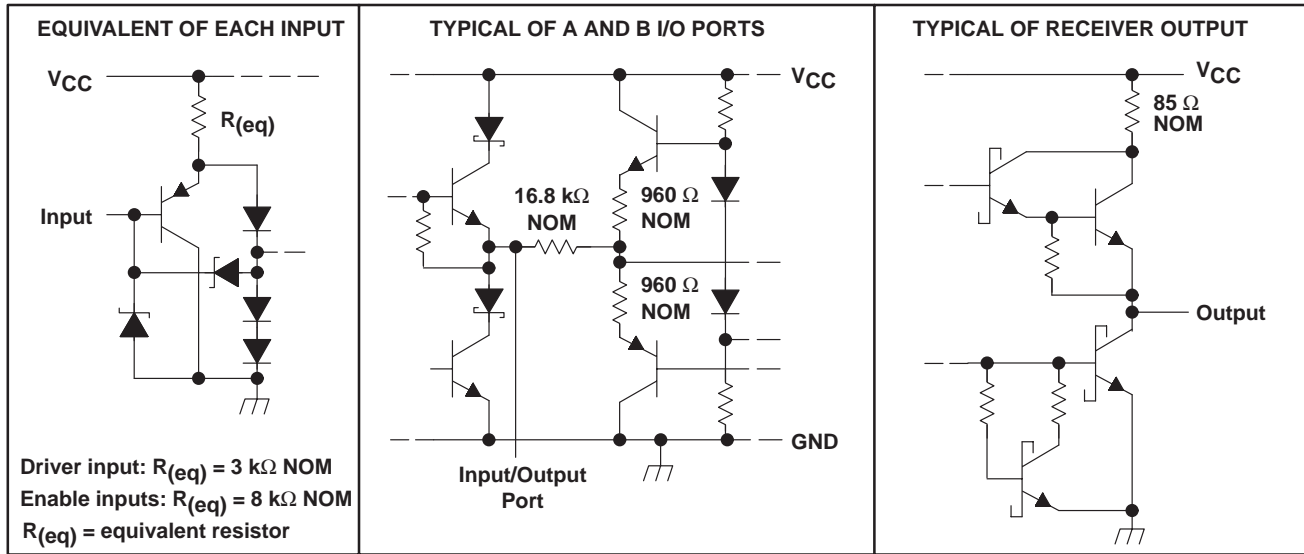


### logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**schematics of inputs and outputs**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Voltage range at any bus terminal	-10 V to 15 V
Enable input voltage, $V_I$	5.5 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 105^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW
P	1100 mW	8.8 mW/°C	704 mW	396 mW

# SN75176A

## DIFFERENTIAL BUS TRANSCEIVER

SLLS100A – JUNE 1984 – REVISED MAY 1995

### recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), $V_I$ or $V_{IC}$		-7		12	V
High-level input voltage, $V_{IH}$	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, $V_{IL}$	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, $V_{ID}$ (see Note 2)				$\pm 12$	V
High-level output current, $I_{OH}$	Driver			-60	mA
	Receiver			-400	$\mu A$
Low-level output current, $I_{OL}$	Driver			60	mA
	Receiver			8	
Operating free-air temperature, $T_A$		0		70	$^{\circ}C$

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.



### DRIVER SECTION

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	Input clamp voltage	$I_I = -18 \text{ mA}$				-1.5	V
$V_{OH}$	High-level output voltage	$V_{IH} = 2 \text{ V}$ , $I_{OH} = -33 \text{ mA}$	$V_{IL} = 0.8 \text{ V}$ ,		3.7		V
$V_{OL}$	Low-level output voltage	$V_{IH} = 2 \text{ V}$ , $I_{OH} = 33 \text{ mA}$	$V_{IL} = 0.8 \text{ V}$ ,		1.1		V
$ V_{OD1} $	Differential output voltage	$I_O = 0$				$2V_{OD2}$	V
$ V_{OD2} $	Differential output voltage	$R_L = 100 \Omega$ ,	See Figure 1	2	2.7		V
		$R_L = 54 \Omega$ ,	See Figure 1	1.5	2.4		
$\Delta V_{OD} $	Change in magnitude of differential output voltage ‡					$\pm 0.2$	V
$V_{OC}$	Common-mode output voltage§	$R_L = 54 \Omega$ or $100 \Omega$ , See Figure 1				3	V
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage ‡					$\pm 0.2$	V
$I_O$	Output current	Output disabled, See Note 3	$V_O = 12 \text{ V}$			1	mA
			$V_O = -7 \text{ V}$			-0.8	
$I_{IH}$	High-level input current	$V_I = 2.4 \text{ V}$				20	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_I = 0.4 \text{ V}$				-400	$\mu\text{A}$
$I_{OS}$	Short-circuit output current	$V_O = -7 \text{ V}$				-250	mA
		$V_O = V_{CC}$				250	
		$V_O = 12 \text{ V}$				500	
$I_{CC}$	Supply current (total package)	No load	Outputs enabled		35	50	mA
			Outputs disabled		26	40	

† All typical values are at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

‡  $\Delta|V_{OD}|$  and  $\Delta|V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$  respectively, that occur when the input is changed from a high level to a low level.

§ In ANSI Standard EIA/TIA-422-B,  $V_{OC}$ , which is the average of the two output voltages with respect to GND, is called output offset voltage,  $V_{OS}$ .

NOTE 3: This applies for both power on and off; refer to ANSI Standard EIA/TIA-422-B for exact conditions.

### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	$R_L = 60 \Omega$ ,	See Figure 3		40	60	ns
$t_{t(OD)}$	Differential-output transition time				65	95	
$t_{PZH}$	Output enable time to high level	$R_L = 110 \Omega$ ,	See Figure 4		55	90	ns
$t_{PZL}$	Output enable time to low level	$R_L = 110 \Omega$ ,	See Figure 5		30	50	ns
$t_{PHZ}$	Output disable time from high level	$R_L = 110 \Omega$ ,	See Figure 4		85	130	ns
$t_{PLZ}$	Output disable time from low level	$R_L = 110 \Omega$ ,	See Figure 5		20	40	ns

# SN75176A

## DIFFERENTIAL BUS TRANSCEIVER

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### RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>O</sub> = 2.7 V,	I <sub>O</sub> = -0.4 mA			0.2	V	
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>O</sub> = 0.5 V,	I <sub>O</sub> = 8 mA	-0.2‡			V	
V <sub>hys</sub>	Input hysteresis voltage (V <sub>IT+</sub> - V <sub>IT-</sub> )				50		mV	
V <sub>IK</sub>	Enable clamp voltage	I <sub>I</sub> = -18 mA				-1.5	V	
V <sub>OH</sub>	High-level output voltage	V <sub>ID</sub> = 200 mV, See Figure 2	I <sub>OH</sub> = -400 μA,		2.7		V	
V <sub>OL</sub>	Low-level output voltage	V <sub>ID</sub> = -200 mV, See Figure 2	I <sub>OL</sub> = 8 mA,			0.45	V	
I <sub>OZ</sub>	High-impedance-state output current	V <sub>O</sub> = 0.4 V to 2.4 V				±20	μA	
I <sub>I</sub>	Line input current	Other input = 0 V, See Note 3	V <sub>I</sub> = 12 V			1	mA	
			V <sub>I</sub> = -7 V			-0.8		
I <sub>IH</sub>	High-level enable input current	V <sub>IH</sub> = 2.7 V				20	μA	
I <sub>IL</sub>	Low-level enable input current	V <sub>IL</sub> = 0.4 V				-100	μA	
r <sub>i</sub>	Input resistance				12		kΩ	
I <sub>OS</sub>	Short-circuit output current					-15	-85	mA
I <sub>CC</sub>	Supply current (total package)	No load	Outputs enabled			35	50	mA
			Outputs disabled			26	40	

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 3: This applies for both power on and power off. Refer to ANSI Standard EIA/TIA-422-B for exact conditions.

### switching characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 15 pF, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output	V <sub>ID</sub> = -1.5 V to 1.5 V,	See Figure 6		21	35	ns
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output				23	35	ns
t <sub>PZH</sub>	Output enable time to high level	See Figure 7			10	30	ns
t <sub>PZL</sub>	Output enable time to low level				12	30	ns
t <sub>PHZ</sub>	Output disable time from high level	See Figure 7			20	35	ns
t <sub>PLZ</sub>	Output disable time from low level				17	25	ns



PARAMETER MEASUREMENT INFORMATION

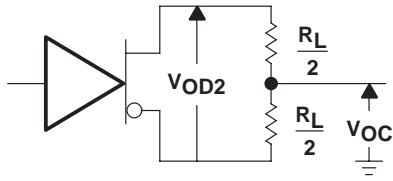


Figure 1. Driver  $V_{OD}$  and  $V_{OC}$

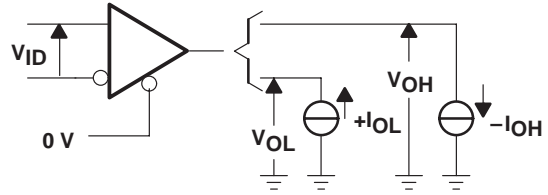
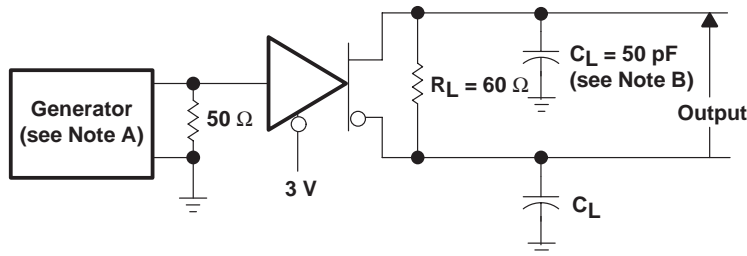
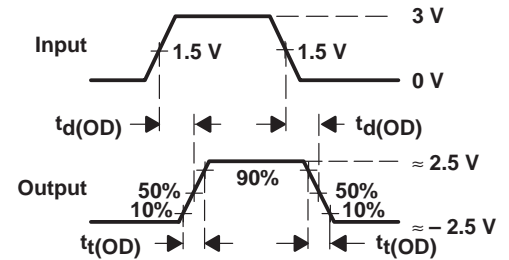


Figure 2. Receiver  $V_{OH}$  and  $V_{OL}$



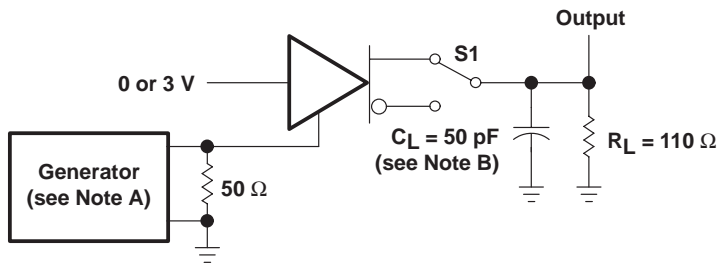
TEST CIRCUIT



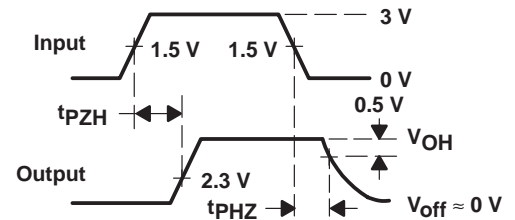
VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT



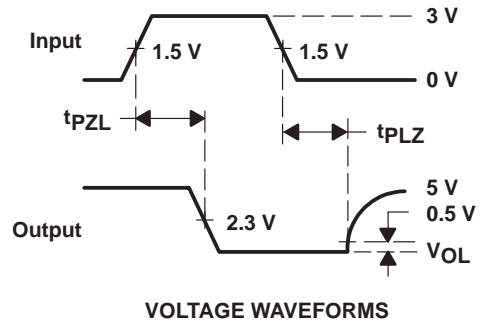
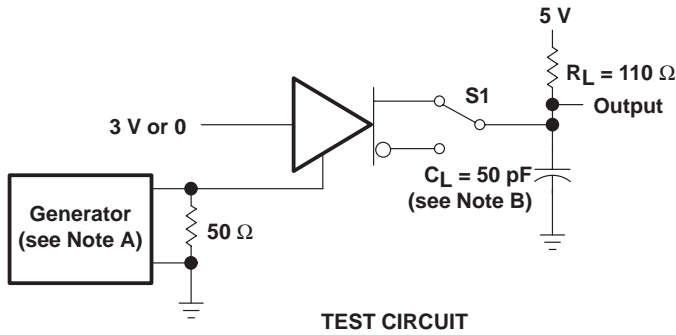
VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

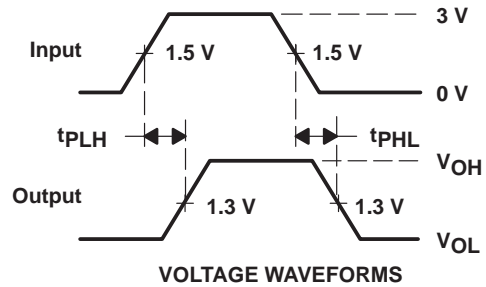
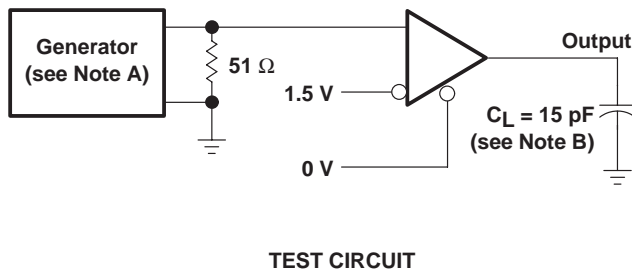
# SN75176A DIFFERENTIAL BUS TRANSCEIVER

SLLS100A – JUNE 1984 – REVISED MAY 1995



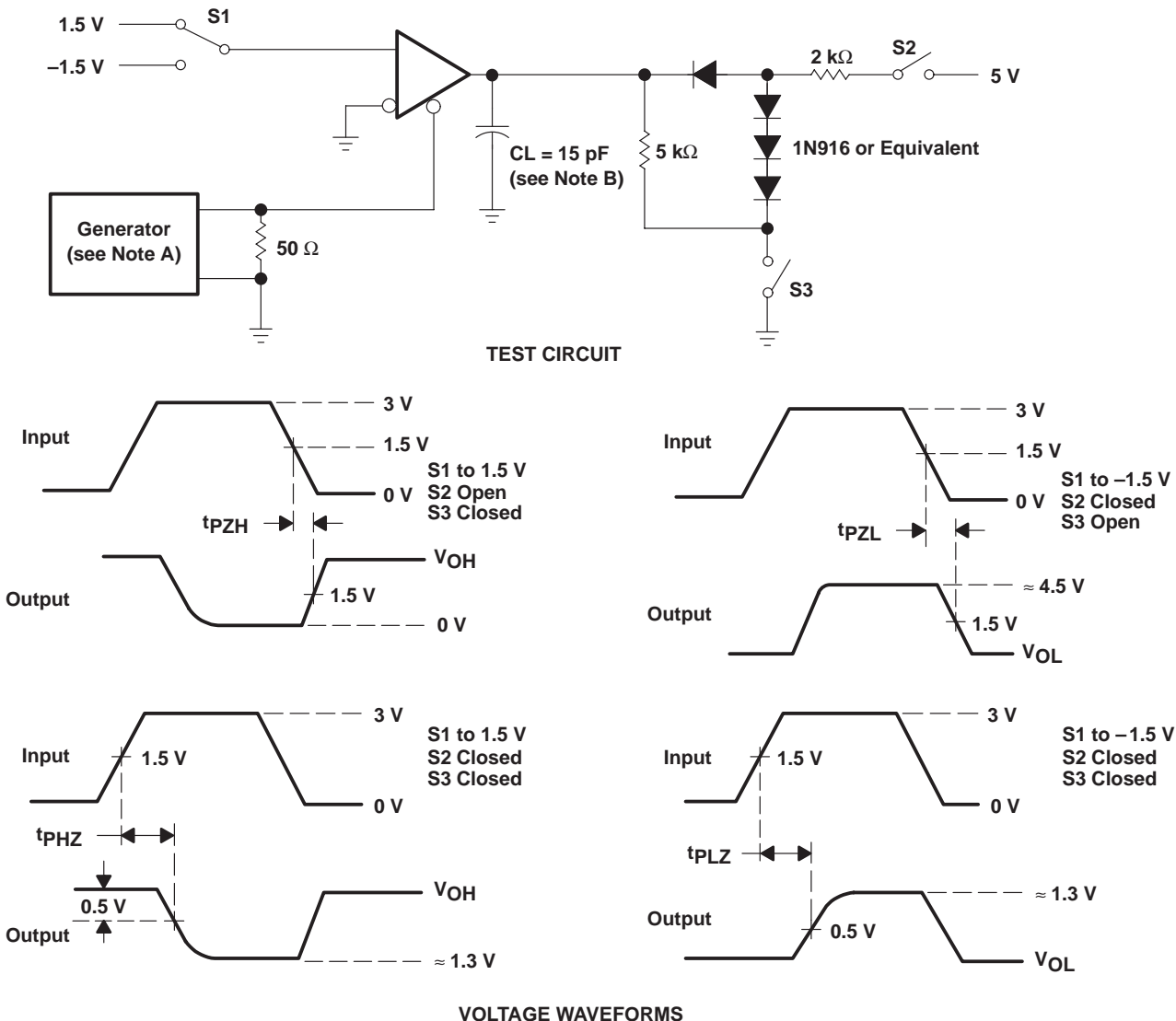
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

**Figure 5. Driver Test Circuit and Voltage Waveforms**



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

**Figure 6. Receiver Test Circuit and Voltage Waveforms**



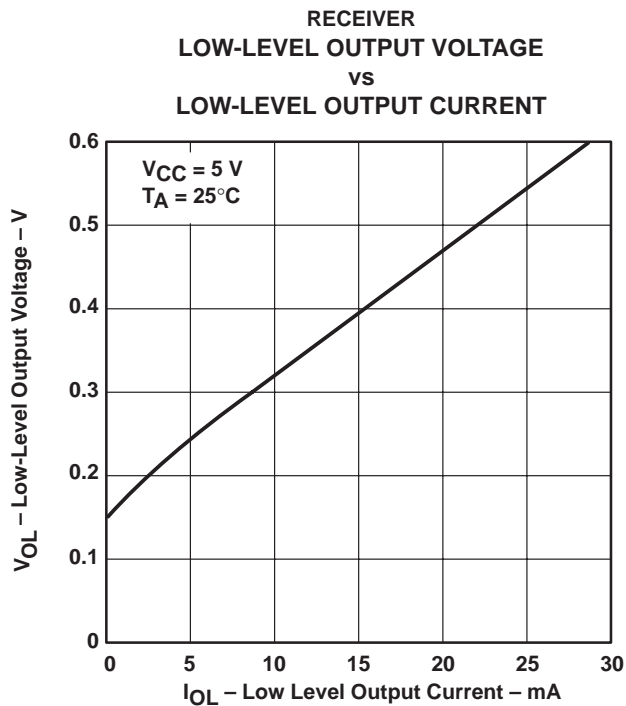
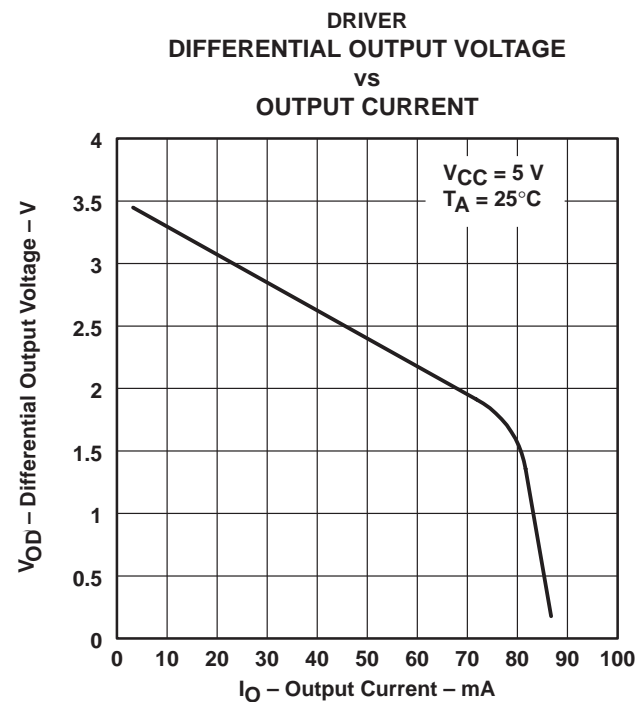
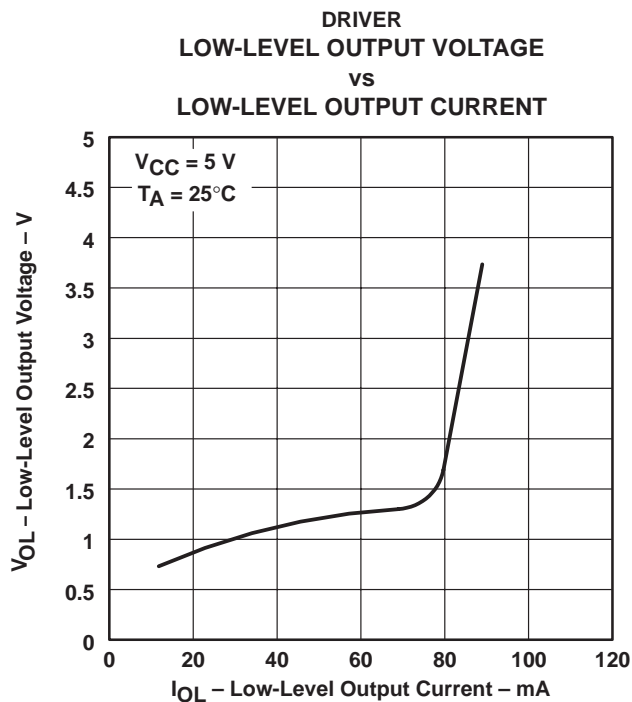
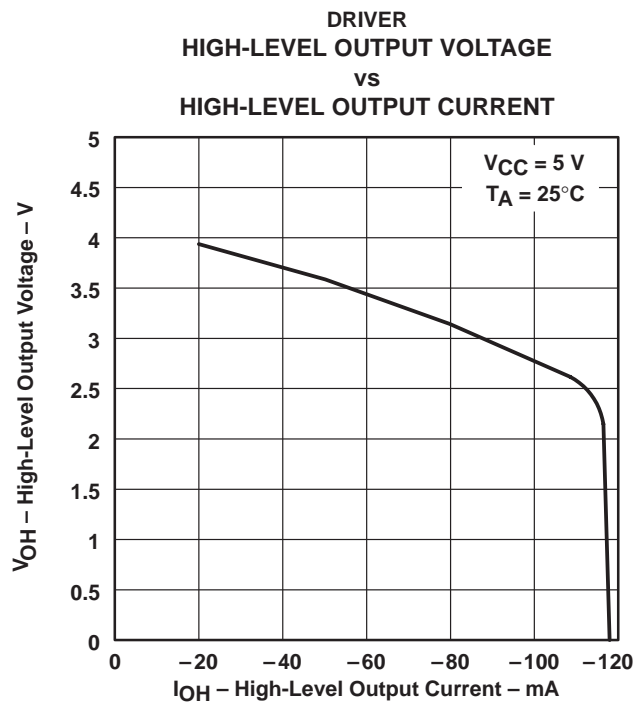
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

**Figure 7. Receiver Test Circuit and Voltage Waveforms**

# SN75176A DIFFERENTIAL BUS TRANSCEIVER

SLLS100A – JUNE 1984 – REVISED MAY 1995

## TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

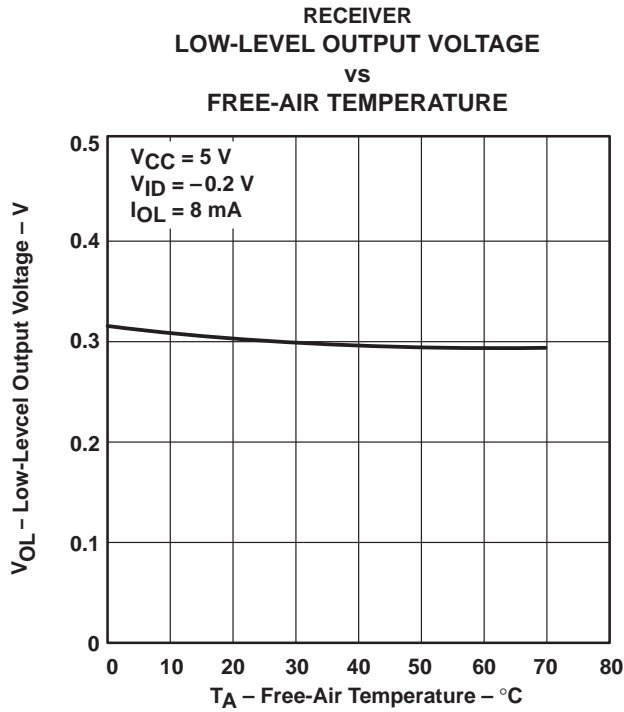


Figure 12

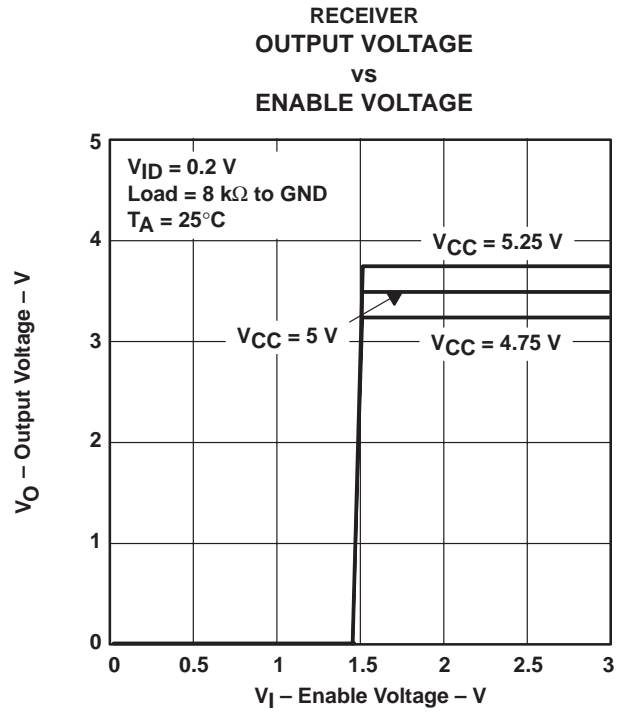


Figure 13

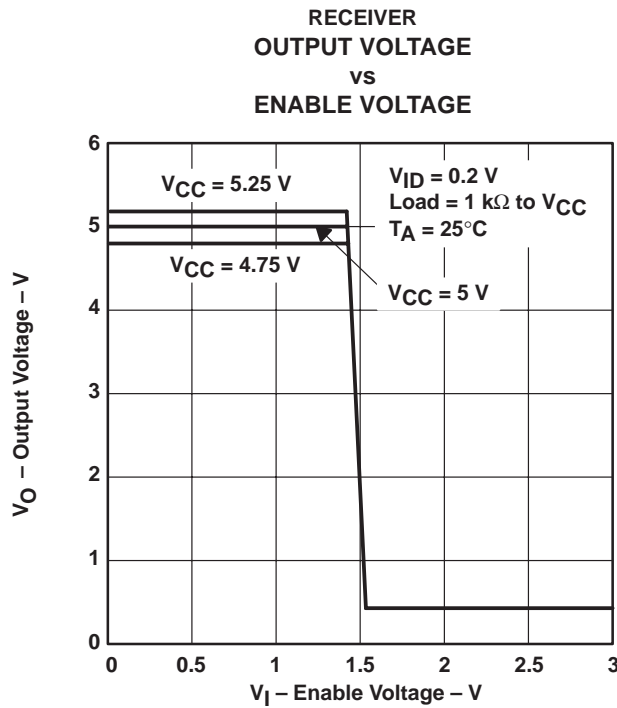
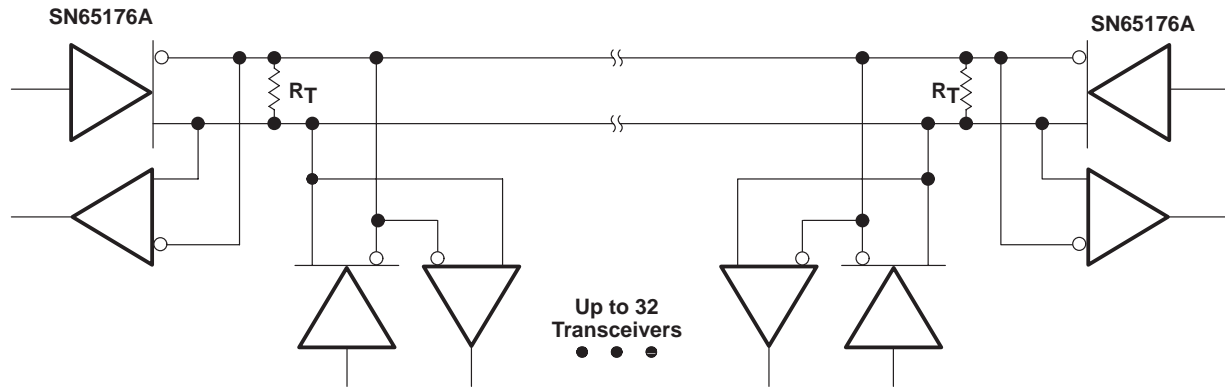


Figure 14

# SN75176A DIFFERENTIAL BUS TRANSCEIVER

SLLS100A – JUNE 1984 – REVISED MAY 1995

## APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ( $R_T = Z_0$ ). Stub lengths off the main line should be kept as short as possible.

Figure 15. Typical Application Circuit

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Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN75176AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75176ADE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75176ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75176ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75176ADRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75176ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75176AP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75176APE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

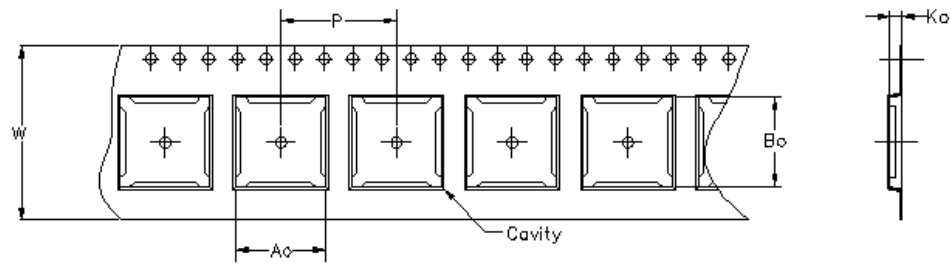
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

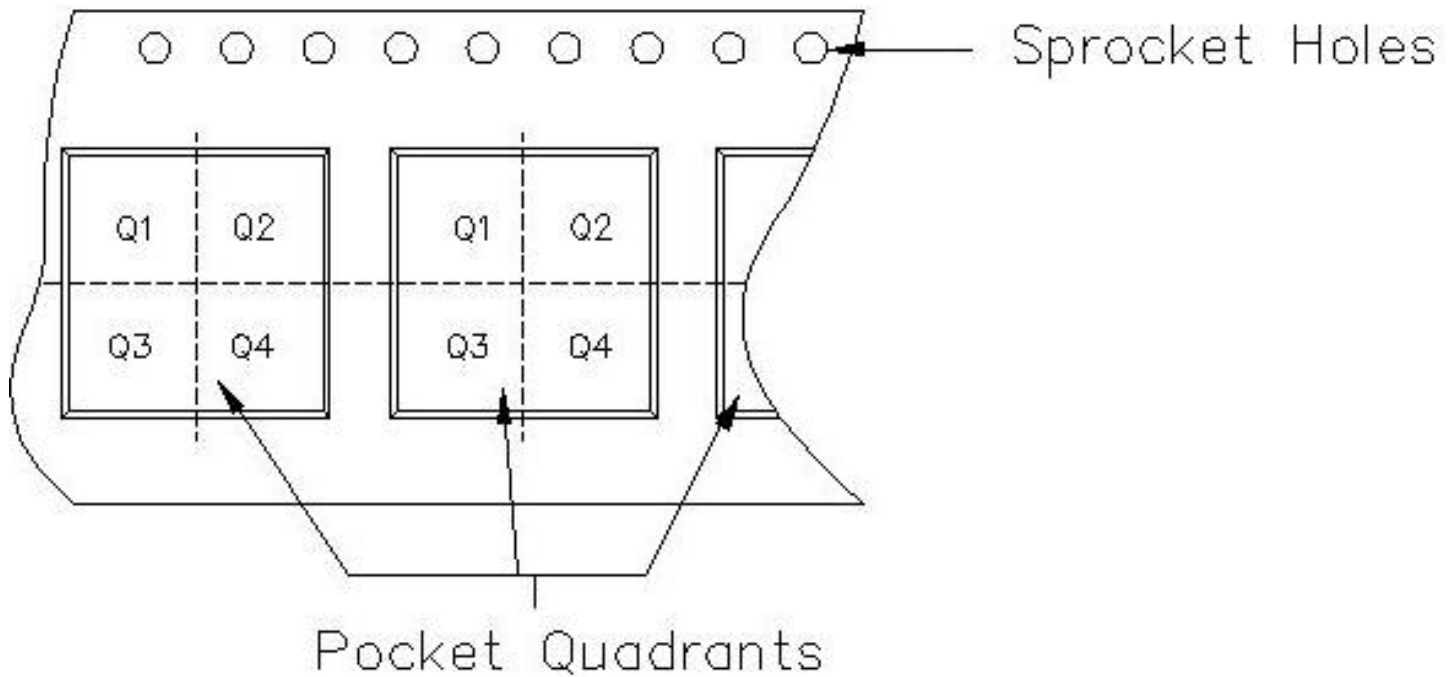
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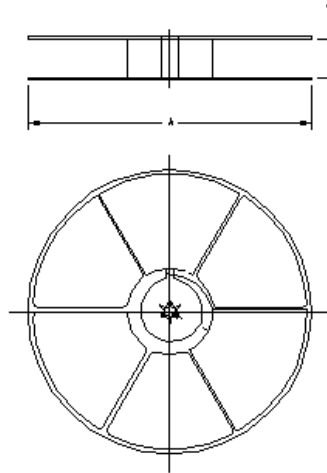
Carrier tape design is defined largely by the component length, width, and thickness.

$A_o$ = Dimension designed to accommodate the component width.
$B_o$ = Dimension designed to accommodate the component length.
$K_o$ = Dimension designed to accommodate the component thickness.
$W$ = Overall width of the carrier tape.
$P$ = Pitch between successive cavity centers.



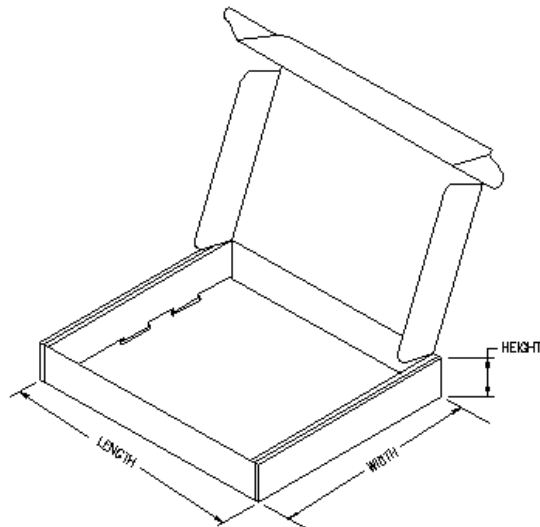
**TAPE AND REEL INFORMATION**

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75176ADR	D	8	FMX	330	12	6.4	5.2	2.1	8	12	Q1



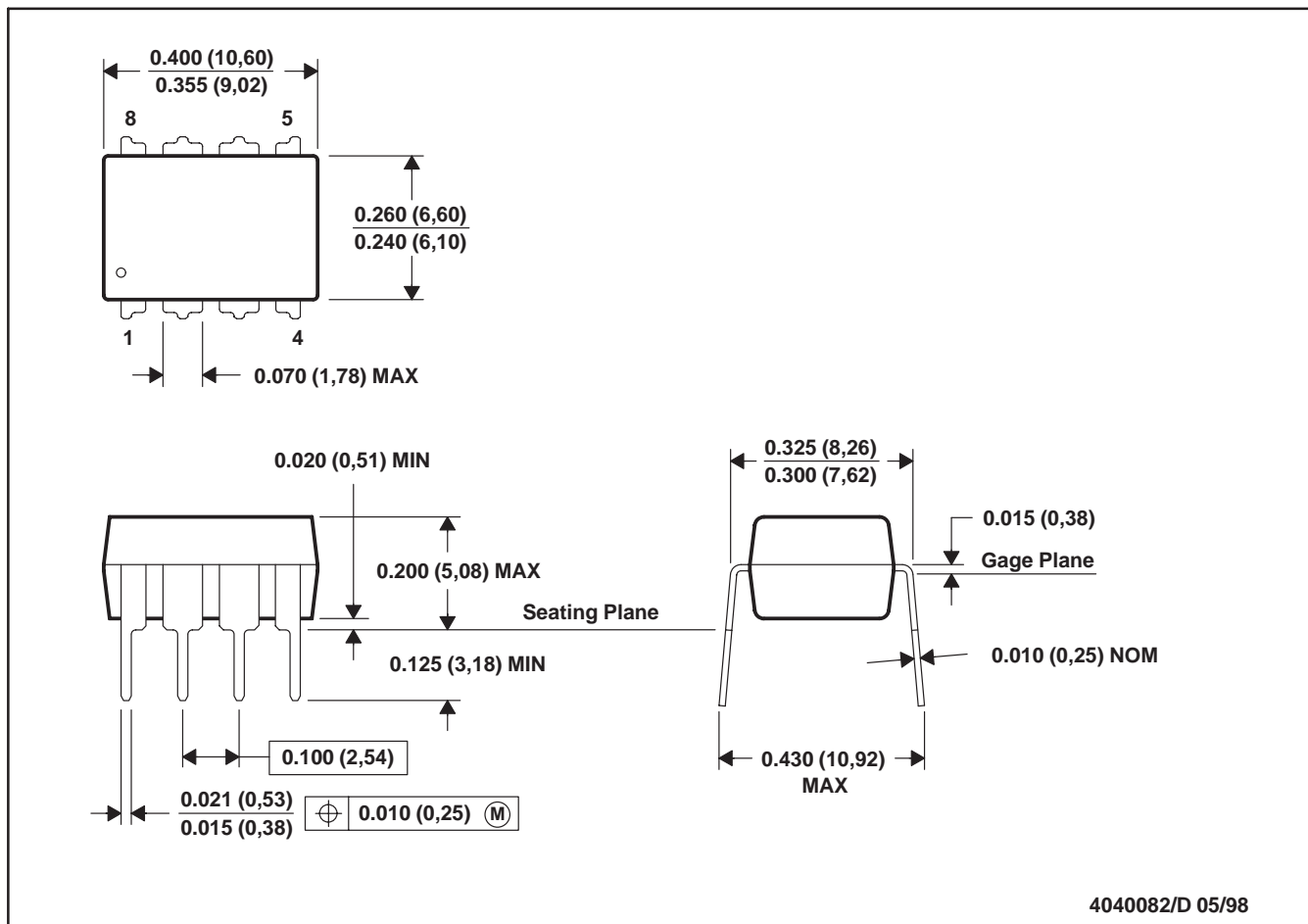
**TAPE AND REEL BOX INFORMATION**

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN75176ADR	D	8	FMX	342.9	336.6	20.64



P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE

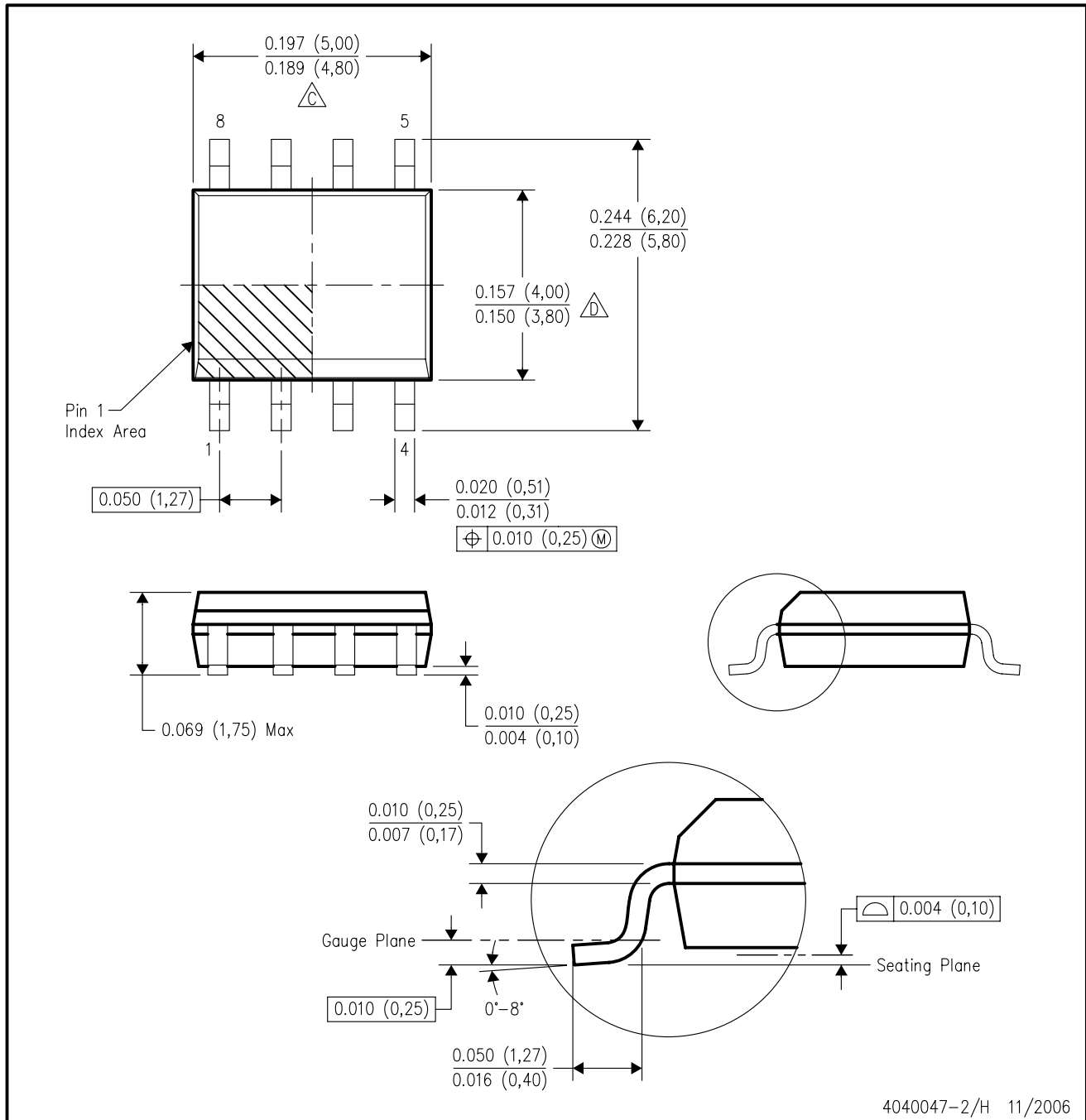


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001

For the latest package information, go to [http://www.ti.com/sc/docs/package/pkg\\_info.htm](http://www.ti.com/sc/docs/package/pkg_info.htm)

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
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  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AA.

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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