Hojas de datos usadas para la implementación

LM2596 SIMPLE SWITCHER® Power Converter 150-kHz 3-A Step-Down Voltage Regulator

1 Features

- 3.3-V, 5-V, 12-V, and Adjustable Output Versions
- Adjustable Version Output Voltage Range: 1.2-V to 37-V ± 4% Maximum Over Line and Load Conditions
- Available in TO-220 and TO-263 Packages
- 3-A Output Load Current
- Input Voltage Range Up to 40 V
- Requires Only 4 External Components
- Excellent Line and Load Regulation Specifications
- 150-kHz Fixed-Frequency Internal Oscillator
- TTL Shutdown Capability
- Low Power Standby Mode, I_Q, Typically 80 μA
- High Efficiency
- Uses Readily Available Standard Inductors
- Thermal Shutdown and Current-Limit Protection
- Create a Custom Design Using the LM2596 with the WEBENCH Power Designer

2 Applications

- Simple High-Efficiency Step-Down (Buck) Regulator
- On-Card Switching Regulators
- Positive to Negative Converter

3 Description

The LM2596 series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving a 3-A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3 V, 5 V, 12 V, and an adjustable output version.

Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensation, and a fixed-frequency oscillator.

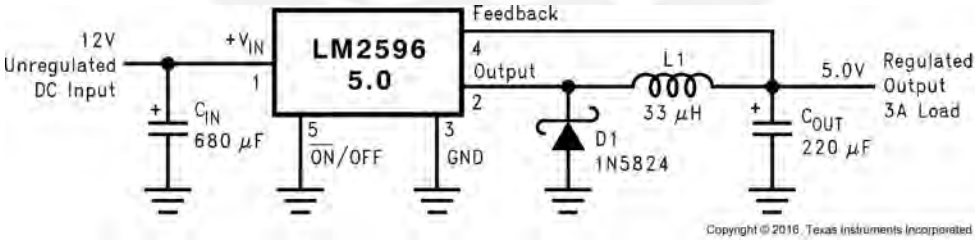
The LM2596 series operates at a switching frequency of 150 kHz, thus allowing smaller sized filter components than what would be required with lower frequency switching regulators. Available in a standard 7-pin TO-220 package with several different lead bend options, and a 7-pin TO-263 surface mount package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2596	TO-220 (7)	14.986 mm × 10.16 mm
	TO-263 (7)	10.10 mm × 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



(Fixed Output Voltage Versions)

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2013) to Revision D — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Removed all references to design software *Switchers Made Simple* ... 1

Changes from Revision B (April 2013) to Revision C — **Page**

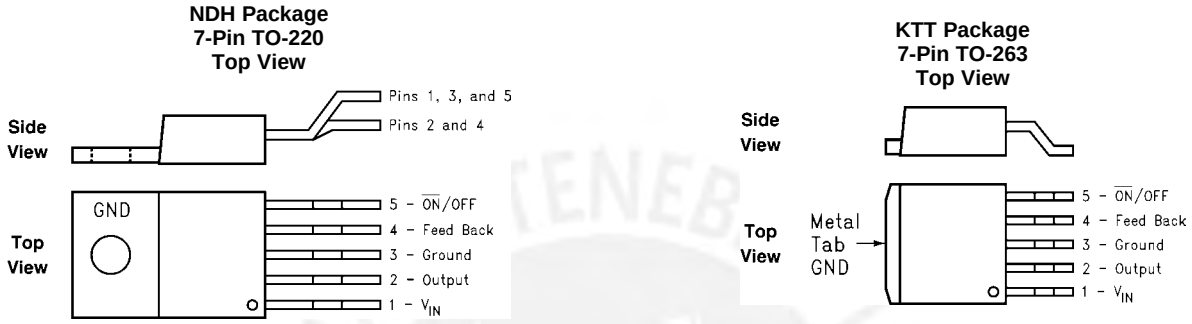
- Changed layout of National Semiconductor Data Sheet to TI format ... 10

5 Description (continued)

A standard series of inductors are available from several different manufacturers optimized for use with the LM2596 series. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a ±4% tolerance on output voltage under specified input voltage and output load conditions, and ±15% on the oscillator frequency. External shutdown is included, featuring typically 80 μA standby current. Self-protection features include a two stage frequency reducing current limit for the output switch and an overtemperature shutdown for complete protection under fault conditions.

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{IN}	I	This is the positive input supply for the IC switching regulator. A suitable input bypass capacitor must be present at this pin to minimize voltage transients and to supply the switching currents required by the regulator.
2	Output	O	Internal switch. The voltage at this pin switches between approximately ($+V_{IN} - V_{SAT}$) and approximately −0.5 V, with a duty cycle of V_{OUT} / V_{IN}. To minimize coupling to sensitive circuitry, the PCB copper area connected to this pin must be kept to a minimum.
3	Ground	—	Circuit ground.
4	Feedback	I	Senses the regulated output voltage to complete the feedback loop.
5	$\overline{ON}$/OFF	I	Allows the switching regulator circuit to be shut down using logic signals thus dropping the total input supply current to approximately 80 μA. Pulling this pin below a threshold voltage of approximately 1.3 V turns the regulator on, and pulling this pin above 1.3 V (up to a maximum of 25 V) shuts the regulator down. If this shutdown feature is not required, the $\overline{ON}$/OFF pin can be wired to the ground pin or it can be left open. In either case, the regulator will be in the ON condition.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
Maximum supply voltage (V_{IN})				45	V
$\overline{SD}$/SS pin input voltage(3)				6	V
Delay pin voltage(3)				1.5	V
Flag pin voltage			–0.3	45	V
Feedback pin voltage			–0.3	25	V
Output voltage to ground, steady-state				–1	V
Power dissipation			Internally limited		
Lead temperature	KTW package	Vapor phase (60 s)		215	°C
		Infrared (10 s)		245	
	NDZ package, soldering (10 s)			260	
Maximum junction temperature				150	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Voltage internally clamped. If clamp voltage is exceeded, limit current to a maximum of 1 mA.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Operating Conditions

	MIN	MAX	UNIT
Supply voltage	4.5	40	V
Temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)			LM2596		UNIT
			KTW (TO-263)	NDZ (TO-220)	
			7 PINS	7 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)(3)	See(4)	—	50	°C/W
		See(5)	50	—	
		See(6)	30	—	
		See(7)	20	—	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		2	2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance to JESD 51-7.
(3) Thermal Resistances were simulated on a 4-layer, JEDEC board.
(4) Junction to ambient thermal resistance (no external heat sink) for the package mounted TO-220 package mounted vertically, with the leads soldered to a printed circuit board with (1 oz.) copper area of approximately 1 in^2.
(5) Junction to ambient thermal resistance with the TO-263 package tab soldered to a single sided printed circuit board with 0.5 in^2 of 1-oz copper area.
(6) Junction to ambient thermal resistance with the TO-263 package tab soldered to a single sided printed circuit board with 2.5 in^2 of 1-oz copper area.
(7) Junction to ambient thermal resistance with the TO-263 package tab soldered to a double sided printed circuit board with 3 in^2 of 1-oz copper area on the LM2596S side of the board, and approximately 16 in^2 of copper on the other side of the PCB.

7.5 Electrical Characteristics – 3.3-V Version

Specifications are for T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
SYSTEM PARAMETERS(3) (see Figure 35 for test circuit)							
V_{OUT}	Output voltage	4.75 V ≤ V_{IN} ≤ 40 V, 0.2 A ≤ I_{LOAD} ≤ 3 A	T_J = 25°C	3.168	3.3	3.432	V
			–40°C ≤ T_J ≤ 125°C	3.135		3.465	
η	Efficiency	V_{IN} = 12 V, I_{LOAD} = 3 A			73%		

(1) All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2596 is used as shown in Figure 35, system performance is shown in the test conditions column.

7.6 Electrical Characteristics – 5-V Version

Specifications are for T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
SYSTEM PARAMETERS(3) (see Figure 35 for test circuit)							
V_{OUT}	Output voltage	7 V ≤ V_{IN} ≤ 40 V, 0.2 A ≤ I_{LOAD} ≤ 3 A	T_J = 25°C	4.8	5	5.2	V
			–40°C ≤ T_J ≤ 125°C	4.75		5.25	
η	Efficiency	V_{IN} = 12 V, I_{LOAD} = 3 A			80%		

(1) All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2596 is used as shown in Figure 35, system performance is shown in the test conditions column.

7.7 Electrical Characteristics – 12-V Version

Specifications are for T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
SYSTEM PARAMETERS(3) (see Figure 35 for test circuit)							
V_{OUT}	Output voltage	15 V ≤ V_{IN} ≤ 40 V, 0.2 A ≤ I_{LOAD} ≤ 3 A	T_J = 25°C	11.52	12	12.48	V
			–40°C ≤ T_J ≤ 125°C	11.4		12.6	
η	Efficiency	V_{IN} = 25 V, I_{LOAD} = 3 A			90%		

(1) All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2596 is used as shown in Figure 35, system performance is shown in the test conditions column.

7.8 Electrical Characteristics – Adjustable Voltage Version

Specifications are for T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
SYSTEM PARAMETERS(3) (see Figure 35 for test circuit)							
V_{FB}	Feedback voltage	4.5 V ≤ V_{IN} ≤ 40 V, 0.2 A ≤ I_{LOAD} ≤ 3 A			1.23		V
		V_{OUT} programmed for 3 V (see Figure 35 for test circuit)	T_J = 25°C	1.193		1.267	
			–40°C ≤ T_J ≤ 125°C	1.18		1.28	
η	Efficiency	V_{IN} = 12 V, V_{OUT} = 3 V, I_{LOAD} = 3 A			73%		

(1) All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2596 is used as shown in Figure 35, system performance is shown in the test conditions column.

7.9 Electrical Characteristics – All Output Voltage Versions

Specifications are for T_J = 25°C, I_{LOAD} = 500 mA, V_{IN} = 12 V for the 3.3-V, 5-V, and adjustable version, and V_{IN} = 24 V for the 12-V version (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
DEVICE PARAMETERS							
I_b	Feedback bias current	Adjustable version only, V_{FB} = 1.3 V	T_J = 25°C		10	50	nA
			–40°C ≤ T_J ≤ 125°C			100	
f_O	Oscillator frequency(3)	T_J = 25°C		127	150	173	kHz
		–40°C ≤ T_J ≤ 125°C		110		173	
V_{SAT}	Saturation voltage(4) (5)	I_{OUT} = 3 A	T_J = 25°C		1.16	1.4	V
			–40°C ≤ T_J ≤ 125°C			1.5	
DC	Max duty cycle (ON)(5)				100%		
	Min duty cycle (OFF)(6)				0%		
I_{CL}	Current limit(4) (5)	Peak current	T_J = 25°C	3.6	4.5	6.9	A
			–40°C ≤ T_J ≤ 125°C	3.4		7.5	
I_L	Output leakage current(4) (6)	Output = 0 V, V_{IN} = 40 V				50	µA
		Output = –1 V			2	30	mA
I_Q	Operating quiescent current(6)	See (6)			5	10	mA
I_{STBY}	Current standby quiescent	$\overline{ON}$/OFF pin = 5 V (OFF)(7)	T_J = 25°C		80	200	µA
			–40°C ≤ T_J ≤ 125°C			250	µA
$\overline{SHUTDOWN}$/SOFT-START CONTROL (see Figure 35 for test circuit)							
V_{IH}	$\overline{ON}$/OFF pin logic input threshold voltage	Low (regulator ON)	T_J = 25°C		1.3		V
			–40°C ≤ T_J ≤ 125°C			0.6	
V_{IL}		High (regulator OFF)	T_J = 25°C		1.3		V
			–40°C ≤ T_J ≤ 125°C	2			
I_H	$\overline{ON}$/OFF pin input current	V_{LOGIC} = 2.5 V (regulator OFF)			5	15	µA
I_L		V_{LOGIC} = 0.5 V (regulator ON)			0.02	5	µA

(1) All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) The switching frequency is reduced when the second stage current limit is activated. The amount of reduction is determined by the severity of current overload.
(4) No diode, inductor, or capacitor connected to output pin.
(5) Feedback pin removed from output and connected to 0 V to force the output transistor switch ON.
(6) Feedback pin removed from output and connected to 12 V for the 3.3-V, 5-V, and the adjustable versions, and 15 V for the 12-V version, to force the output transistor switch OFF.
(7) V_{IN} = 40 V.

7.10 Typical Characteristics

See Figure 35 for test circuit

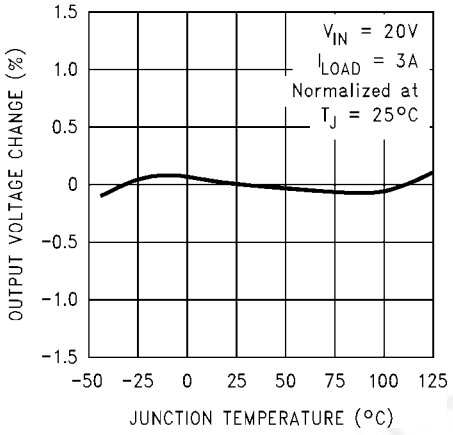


Figure 1. Normalized Output Voltage

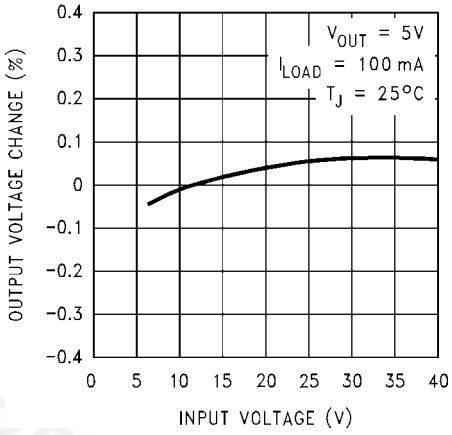


Figure 2. Line Regulation

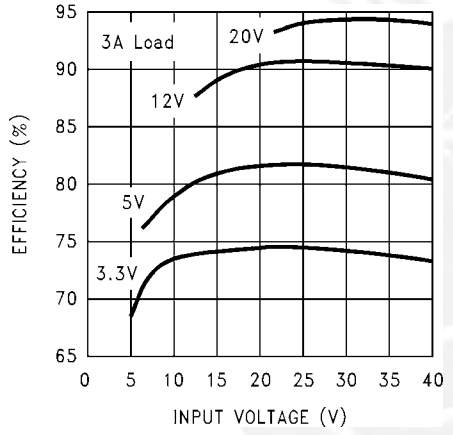


Figure 3. Efficiency

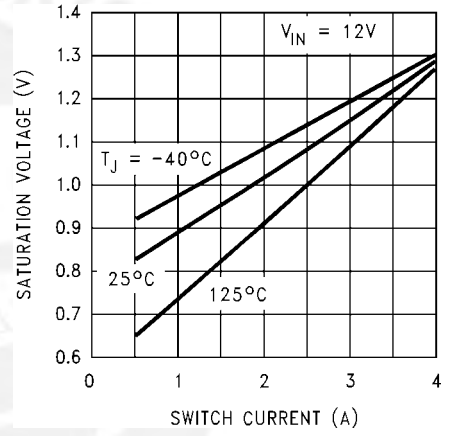


Figure 4. Switch Saturation Voltage

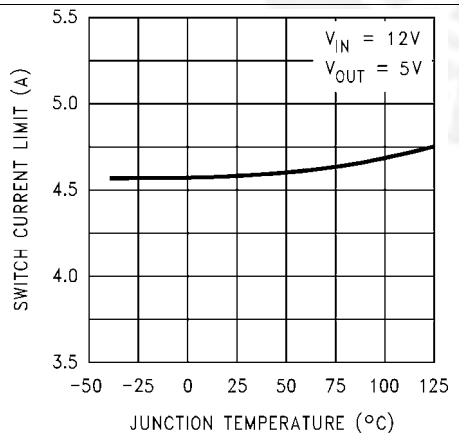


Figure 5. Switch Current Limit

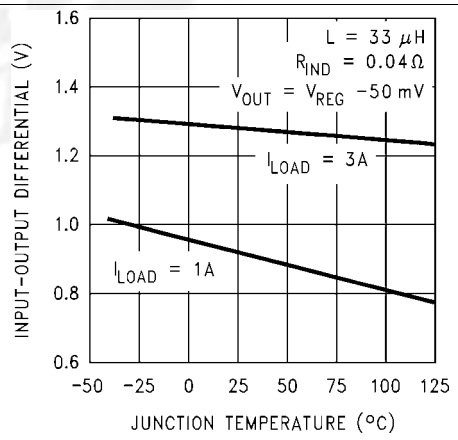


Figure 6. Dropout Voltage

Typical Characteristics (continued)

See Figure 35 for test circuit

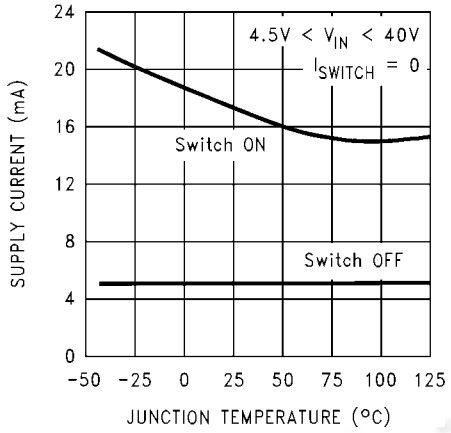


Figure 7. Operating Quiescent Current

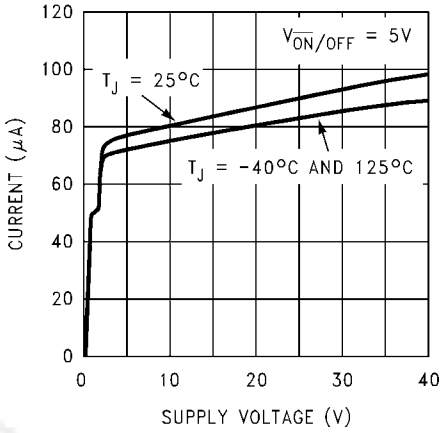


Figure 8. Shutdown Quiescent Current

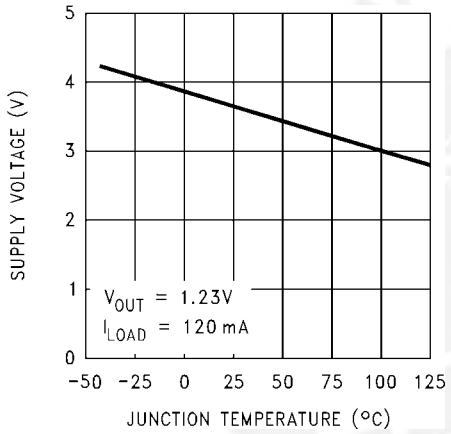


Figure 9. Minimum Operating Supply Voltage

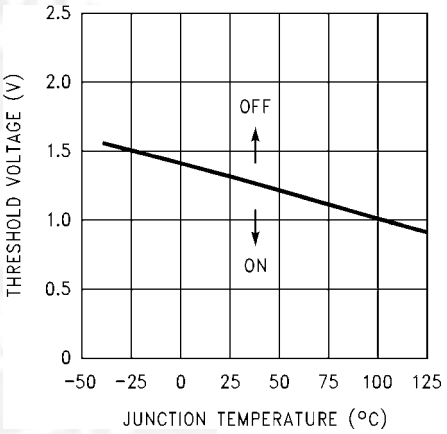


Figure 10. $\overline{ON}$/OFF Threshold Voltage

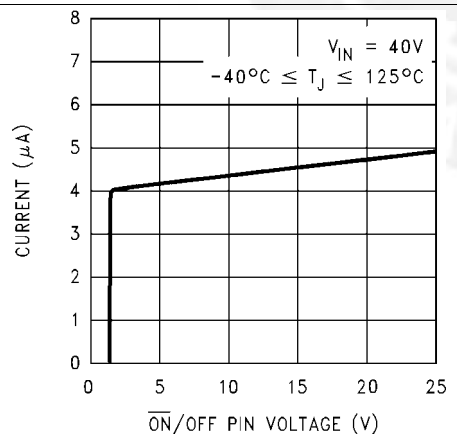


Figure 11. $\overline{ON}$/OFF Pin Current (Sinking)

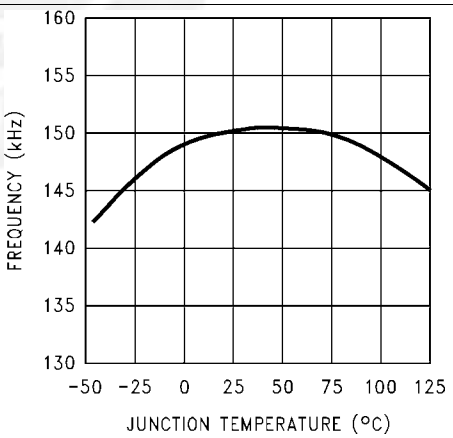


Figure 12. Switching Frequency

Typical Characteristics (continued)

See Figure 35 for test circuit

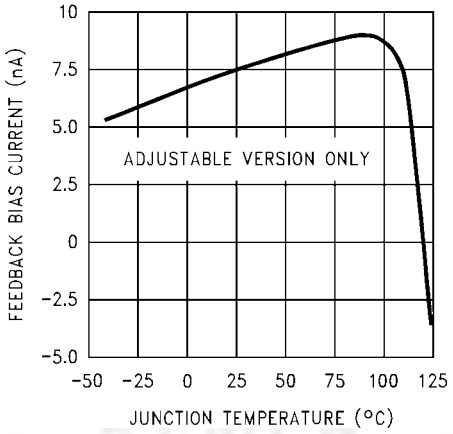


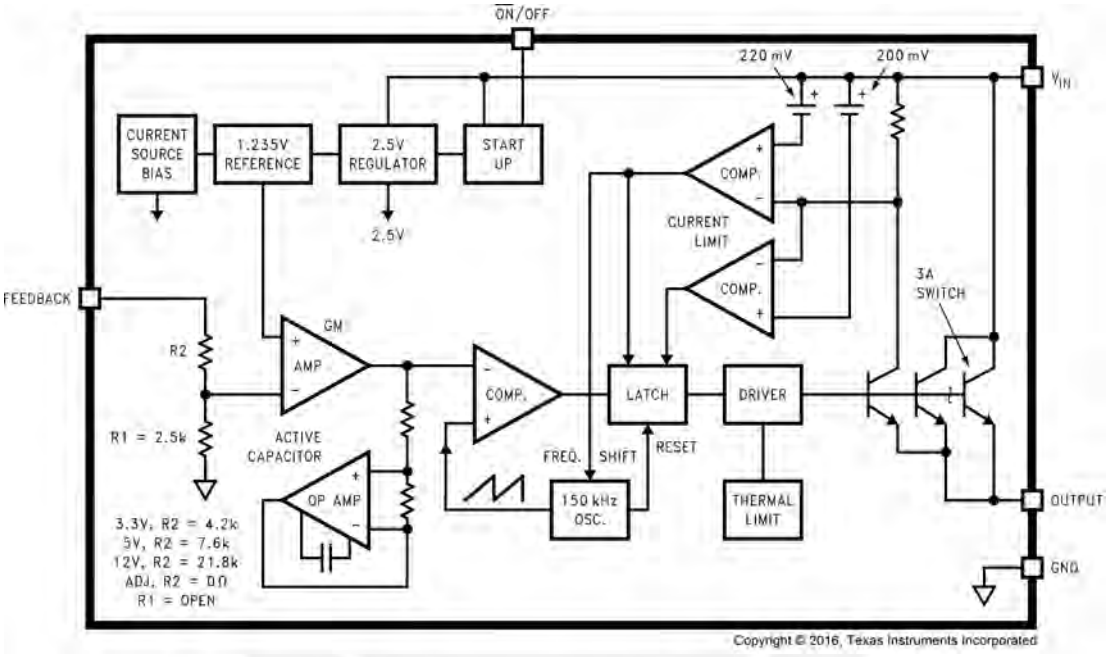
Figure 13. Feedback Pin Bias Current

8 Detailed Description

8.1 Overview

The LM2596 SIMPLE SWITCHER® regulator is an easy-to-use, nonsynchronous, step-down DC-DC converter with a wide input voltage range up to 40 V. The regulator is capable of delivering up to 3-A DC load current with excellent line and load regulation. These devices are available in fixed output voltages of 3.3-V, 5-V, 12-V and an adjustable output version. The family requires few external components, and the pin arrangement was designed for simple, optimum PCB layout.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Delayed Start-Up

The circuit in Figure 14 uses the ON/OFF pin to provide a time delay between the time the input voltage is applied and the time the output voltage comes up (only the circuitry pertaining to the delayed start-up is shown). As the input voltage rises, the charging of capacitor C1 pulls the ON/OFF pin high, keeping the regulator OFF. Once the input voltage reaches its final value and the capacitor stops charging, resistor R_2 pulls the ON/OFF pin low, thus allowing the circuit to start switching. Resistor R_1 is included to limit the maximum voltage applied to the ON/OFF pin (maximum of 25 V), reduces power supply noise sensitivity, and also limits the capacitor C1 discharge current. When high input ripple voltage exists, avoid long delay time, because this ripple can be coupled into the ON/OFF pin and cause problems.

This delayed start-up feature is useful in situations where the input power source is limited in the amount of current it can deliver. It allows the input voltage to rise to a higher voltage before the regulator starts operating. Buck regulators require less input current at higher input voltages.

Feature Description (continued)

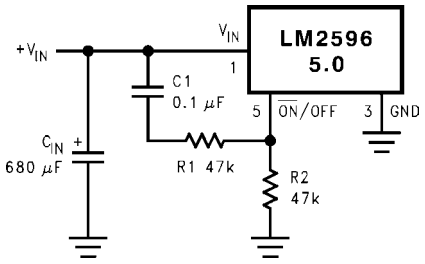


Figure 14. Delayed Start-Up

8.3.2 Undervoltage Lockout

Some applications require the regulator to remain off until the input voltage reaches a predetermined voltage. Figure 15 shows an undervoltage lockout feature applied to a buck regulator, while Figure 16 and Figure 17 apply the same feature to an inverting circuit. The circuit in Figure 16 features a constant threshold voltage for turnon and turnoff (Zener voltage plus approximately one volt). If hysteresis is required, the circuit in Figure 17 has a turnon voltage which is different than the turnoff voltage. The amount of hysteresis is approximately equal to the value of the output voltage. If Zener voltages greater than 25 V are used, an additional 47-kΩ resistor is required from the ON/OFF pin to the ground pin to stay within the 25 V maximum limit of the ON/OFF pin.

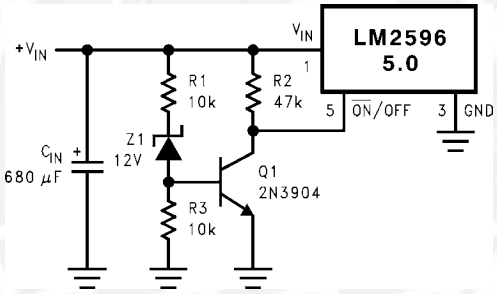
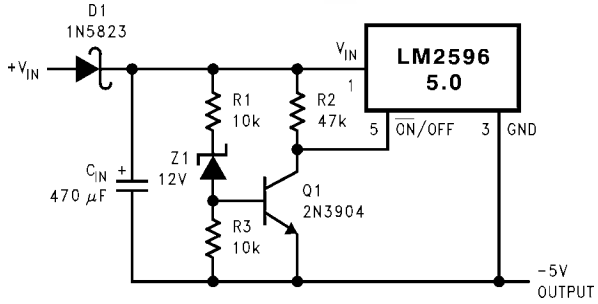


Figure 15. Undervoltage Lockout for Buck Regulator

8.3.3 Inverting Regulator

The circuit in Figure 18 converts a positive input voltage to a negative output voltage with a common ground. The circuit operates by bootstrapping the ground pin of the regulator to the negative output voltage, then grounding the feedback pin, the regulator senses the inverted output voltage and regulates it.



This circuit has an ON/OFF threshold of approximately 13 V.

Figure 16. Undervoltage Lockout for Inverting Regulator

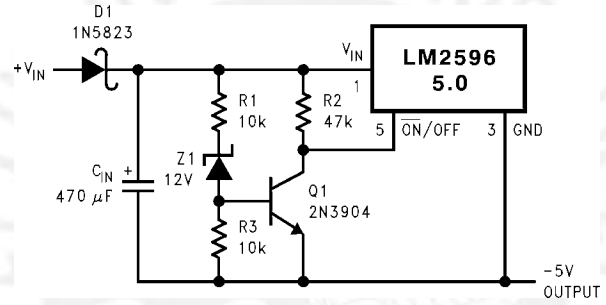
Feature Description (continued)

This example uses the LM2596-5.0 to generate a −5-V output, but other output voltages are possible by selecting other output voltage versions, including the adjustable version. Because this regulator topology can produce an output voltage that is either greater than or less than the input voltage, the maximum output current greatly depends on both the input and output voltage. Figure 19 provides a guide as to the amount of output load current possible for the different input and output voltage conditions.

The maximum voltage appearing across the regulator is the absolute sum of the input and output voltage, and this must be limited to a maximum of 40 V. For example, when converting +20 V to −12 V, the regulator would see 32 V between the input pin and ground pin. The LM2596 has a maximum input voltage spec of 40 V.

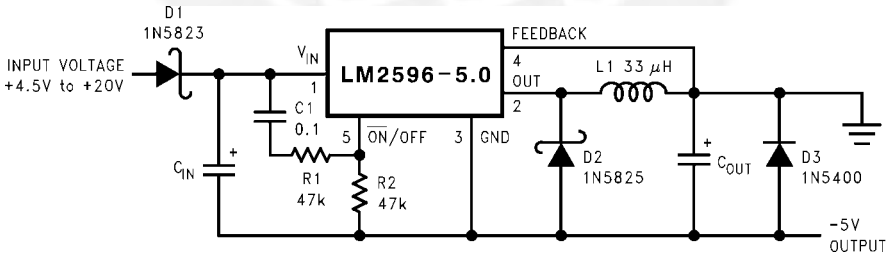
Additional diodes are required in this regulator configuration. Diode D1 is used to isolate input voltage ripple or noise from coupling through the C_{IN} capacitor to the output, under light or no load conditions. Also, this diode isolation changes the topology to closely resemble a buck configuration, thus providing good closed-loop stability. TI recommends using a Schottky diode for low input voltages, (because of its lower voltage drop) but for higher input voltages, a fast recovery diode could be used.

Without diode D3, when the input voltage is first applied, the charging current of C_{IN} can pull the output positive by several volts for a short period of time. Adding D3 prevents the output from going positive by more than a diode voltage.



This circuit has hysteresis
Regulator starts switching at V_{IN} = 13 V
Regulator stops switching at V_{IN} = 8 V

Figure 17. Undervoltage Lockout With Hysteresis for Inverting Regulator



C_{IN} — 68-µF, 25-V Tant. Sprague 595D
470 -µF, 50-V Elec. Panasonic HFQ
C_{OUT} — 47-µF, 20-V Tant. Sprague 595D
220-µF, 25-V Elec. Panasonic HFQ

Figure 18. Inverting −5-V Regulator With Delayed Start-Up

Feature Description (continued)

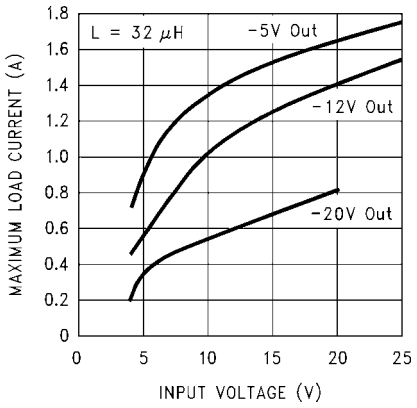


Figure 19. Inverting Regulator Typical Load Current

Because of differences in the operation of the inverting regulator, the standard design procedure is not used to select the inductor value. In the majority of designs, a 33-μH, 3.5-A inductor is the best choice. Capacitor selection can also be narrowed down to just a few values. Using the values shown in Figure 18 will provide good results in the majority of inverting designs.

This type of inverting regulator can require relatively large amounts of input current when starting up, even with light loads. Input currents as high as the LM2596 current limit (approximately 4.5 A) are required for at least 2 ms or more, until the output reaches its nominal output voltage. The actual time depends on the output voltage and the size of the output capacitor. Input power sources that are current limited or sources that can not deliver these currents without getting loaded down, may not work correctly. Because of the relatively high start-up currents required by the inverting topology, the delayed start-up feature (C1, R_1, and R_2) shown in Figure 18 is recommended. By delaying the regulator start-up, the input capacitor is allowed to charge up to a higher voltage before the switcher begins operating. A portion of the high input current required for start-up is now supplied by the input capacitor (C_{IN}). For severe start-up conditions, the input capacitor can be made much larger than normal.

8.3.4 Inverting Regulator Shutdown Methods

Using the $\overline{ON}$/OFF pin in a standard buck configuration is simple. To turn the regulator ON, pull the $\overline{ON}$/OFF pin below 1.3 V (at 25°C, referenced to ground). To turn the regulator OFF, pull the $\overline{ON}$/OFF pin above 1.3 V. With the inverting configuration, some level shifting is required, because the ground pin of the regulator is no longer at ground, but is now setting at the negative output voltage level. Two different shutdown methods for inverting regulators are shown in Figure 20 and Figure 21.

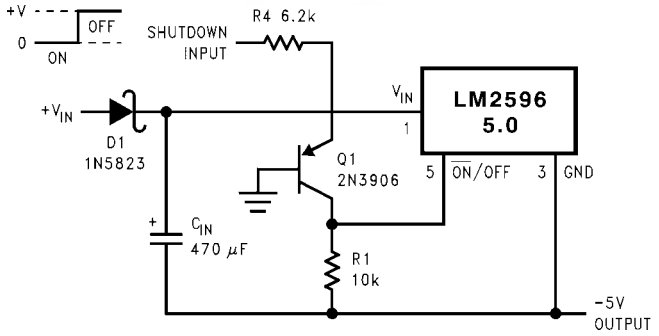


Figure 20. Inverting Regulator Ground Referenced Shutdown

Feature Description (continued)

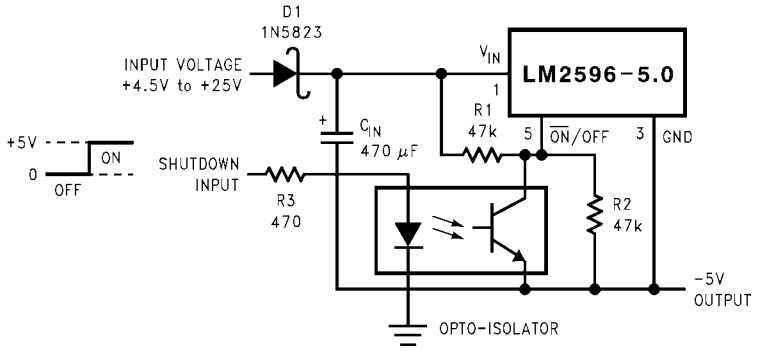


Figure 21. Inverting Regulator Ground Referenced Shutdown Using Opto Device

8.4 Device Functional Modes

8.4.1 Discontinuous Mode Operation

The selection guide chooses inductor values suitable for continuous mode operation, but for low current applications or high input voltages, a discontinuous mode design may be a better choice. A discontinuous mode design would use an inductor that would be physically smaller, and would require only one half to one third the inductance value required for a continuous mode design. The peak switch and inductor currents will be higher in a discontinuous design, but at these low load currents (1 A and below), the maximum switch current will still be less than the switch current limit.

Discontinuous operation can have voltage waveforms that are considerably different than a continuous design. The output pin (switch) waveform can have some damped sinusoidal ringing present (see Figure 36). This ringing is normal for discontinuous operation, and is not caused by feedback loop instabilities. In discontinuous operation, there is a period of time where neither the switch nor the diode are conducting, and the inductor current has dropped to zero. During this time, a small amount of energy can circulate between the inductor and the switch/diode parasitic capacitance causing this characteristic ringing. Normally this ringing is not a problem, unless the amplitude becomes great enough to exceed the input voltage, and even then, there is very little energy present to cause damage.

Different inductor types or core materials produce different amounts of this characteristic ringing. Ferrite core inductors have very little core loss and therefore produce the most ringing. The higher core loss of powdered iron inductors produce less ringing. If desired, a series RC could be placed in parallel with the inductor to dampen the ringing.

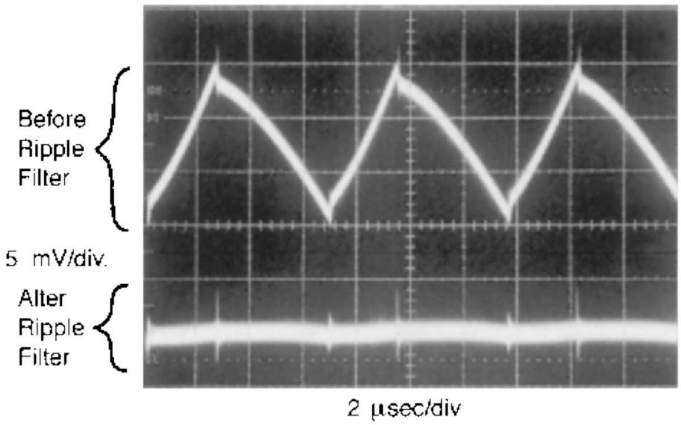


Figure 22. Post Ripple Filter Waveform

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Input Capacitor (C_{IN})

A low ESR aluminum or tantalum bypass capacitor is required between the input pin and ground pin. It must be placed near the regulator using short leads. This capacitor prevents large voltage transients from occuring at the input, and provides the instantaneous current required each time the switch turns ON.

The important parameters for the Input capacitor are the voltage rating and the RMS current rating. Because of the relatively high RMS currents flowing in a buck regulator's input capacitor, this capacitor must be chosen for its RMS current rating rather than its capacitance or voltage ratings, although the capacitance value and voltage rating are directly related to the RMS current rating.

The RMS current rating of a capacitor could be viewed as a capacitor's power rating. The RMS current flowing through the capacitors internal ESR produces power which causes the internal temperature of the capacitor to rise. The RMS current rating of a capacitor is determined by the amount of current required to raise the internal temperature approximately 10°C above an ambient temperature of 105°C. The ability of the capacitor to dissipate this heat to the surrounding air will determine the amount of current the capacitor can safely sustain. For a given capacitor value, a higher voltage electrolytic capacitor will be physically larger than a lower voltage capacitor, and thus be able to dissipate more heat to the surrounding air, and therefore will have a higher RMS current rating.

The consequences of operating an electrolytic capacitor above the RMS current rating is a shortened operating life. The higher temperature speeds up the evaporation of the capacitor's electrolyte, resulting in eventual failure.

Selecting an input capacitor requires consulting the manufacturers data sheet for maximum allowable RMS ripple current. For a maximum ambient temperature of 40°C, a general guideline would be to select a capacitor with a ripple current rating of approximately 50% of the DC load current. For ambient temperatures up to 70°C, a current rating of 75% of the DC load current would be a good choice for a conservative design. The capacitor voltage rating must be at least 1.25 times greater than the maximum input voltage, and often a much higher voltage capacitor is required to satisfy the RMS current requirements.

Figure 23 shows the relationship between an electrolytic capacitor value, its voltage rating, and the RMS current it is rated for. These curves were obtained from the Nichicon *PL* series of low-ESR, high-reliability electrolytic capacitors designed for switching regulator applications. Other capacitor manufacturers offer similar types of capacitors, but always check the capacitor data sheet.

Standard electrolytic capacitors typically have much higher ESR numbers, lower RMS current ratings and typically have a shorter operating lifetime.

Because of their small size and excellent performance, surface-mount solid tantalum capacitors are often used for input bypassing, but several precautions must be observed. A small percentage of solid tantalum capacitors can short if the inrush current rating is exceeded. This can happen at turnon when the input voltage is suddenly applied, and of course, higher input voltages produce higher inrush currents. Several capacitor manufacturers do a 100% surge current testing on their products to minimize this potential problem. If high turnon currents are expected, it may be necessary to limit this current by adding either some resistance or inductance before the tantalum capacitor, or select a higher voltage capacitor. As with aluminum electrolytic capacitors, the RMS ripple current rating must be sized to the load current.

Application Information (continued)

9.1.2 Feedforward Capacitor (C_{FF})

NOTE

For adjustable output voltage version only.

A feedforward capacitor, shown across R2 in Table 6, is used when the output voltage is greater than 10 V or when C_{OUT} has a very low ESR. This capacitor adds lead compensation to the feedback loop and increases the phase margin for better loop stability. For C_{FF} selection, see the *Detailed Design Procedure* section.

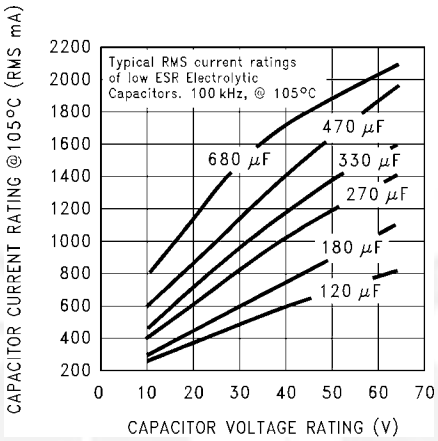


Figure 23. RMS Current Ratings for Low ESR Electrolytic Capacitors (Typical)

9.1.3 Output Capacitor (C_{OUT})

An output capacitor is required to filter the output and provide regulator loop stability. Low impedance or low-ESR electrolytic or solid tantalum capacitors designed for switching regulator applications must be used. When selecting an output capacitor, the important capacitor parameters are the 100-kHz ESR, the RMS ripple current rating, voltage rating, and capacitance value. For the output capacitor, the ESR value is the most important parameter.

The output capacitor requires an ESR value that has an upper and lower limit. For low output ripple voltage, a low ESR value is required. This value is determined by the maximum allowable output ripple voltage, typically 1% to 2% of the output voltage. But if the selected capacitor's ESR is extremely low, there is a possibility of an unstable feedback loop, resulting in an oscillation at the output. Using the capacitors listed in the tables, or similar types, will provide design solutions under all conditions.

If very low output ripple voltage (less than 15 mV) is required, see *Output Voltage Ripple and Transients* for a post ripple filter.

An aluminum electrolytic capacitor's ESR value is related to the capacitance value and its voltage rating. In most cases, higher voltage electrolytic capacitors have lower ESR values (see Figure 24). Often, capacitors with much higher voltage ratings may be required to provide the low ESR values required for low output ripple voltage.

The output capacitor for many different switcher designs often can be satisfied with only three or four different capacitor values and several different voltage ratings. See Table 3 and Table 4 for typical capacitor values, voltage ratings, and manufacturers capacitor types.

Electrolytic capacitors are not recommended for temperatures below −25°C. The ESR rises dramatically at cold temperatures and is typically 3 times as large at −25°C and as much as 10 times as large at −40°C. See Figure 25.

Solid tantalum capacitors have a much better ESR specifications for cold temperatures and are recommended for temperatures below −25°C.

Application Information (continued)

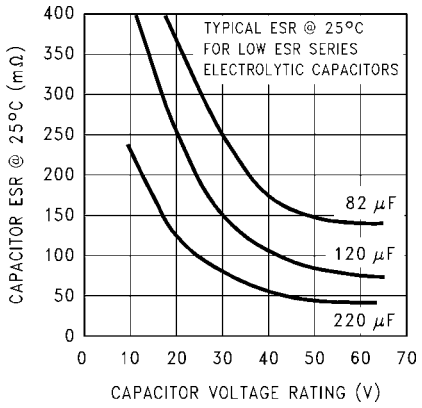


Figure 24. Capacitor ESR vs Capacitor Voltage Rating (Typical Low-ESR Electrolytic Capacitor)

9.1.4 Catch Diode

Buck regulators require a diode to provide a return path for the inductor current when the switch turns off. This must be a fast diode and must be placed close to the LM2596 using short leads and short printed-circuit traces.

Because of their very fast switching speed and low forward voltage drop, Schottky diodes provide the best performance, especially in low output voltage applications (5 V and lower). Ultra-fast recovery, or high-efficiency rectifiers are also a good choice, but some types with an abrupt turnoff characteristic may cause instability or EMI problems. Ultra-fast recovery diodes typically have reverse recovery times of 50 ns or less. Rectifiers such as the 1N5400 series are much too slow and should not be used.

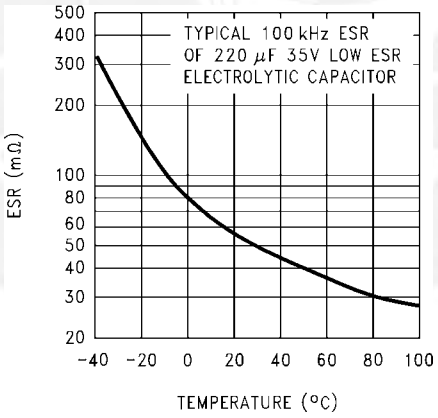


Figure 25. Capacitor ESR Change vs Temperature

9.1.5 Inductor Selection

All switching regulators have two basic modes of operation; continuous and discontinuous. The difference between the two types relates to the inductor current, whether it is flowing continuously, or if it drops to zero for a period of time in the normal switching cycle. Each mode has distinctively different operating characteristics, which can affect the regulators performance and requirements. Most switcher designs will operate in the discontinuous mode when the load current is low.

The LM2596 (or any of the SIMPLE SWITCHER™ family) can be used for both continuous or discontinuous modes of operation.

In many cases the preferred mode of operation is the continuous mode, which offers greater output power, lower peak switch, lower inductor and diode currents, and can have lower output ripple voltage. However, the continuous mode does require larger inductor values to keep the inductor current flowing continuously, especially at low output load currents or high input voltages.

Application Information (continued)

To simplify the inductor selection process, an inductor selection guide (nomograph) was designed (see Figure 27 through Figure 30). This guide assumes that the regulator is operating in the continuous mode, and selects an inductor that will allow a peak-to-peak inductor ripple current to be a certain percentage of the maximum design load current. This peak-to-peak inductor ripple current percentage is not fixed, but is allowed to change as different design load currents are selected (see Figure 26.)

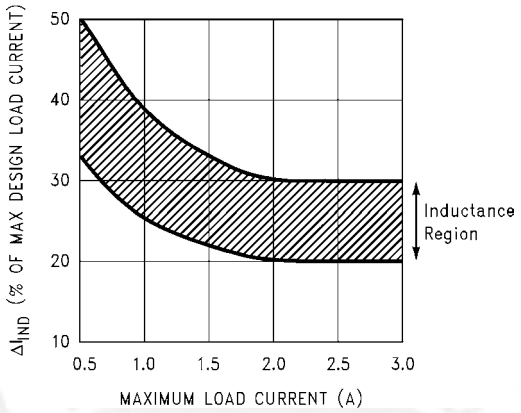


Figure 26. (ΔI_{IND}) Peak-to-Peak Inductor Ripple Current (as a Percentage of the Load Current) vs Load Current

By allowing the percentage of inductor ripple current to increase for low load currents, the inductor value and size can be kept relatively low.

When operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage), with the average value of this current waveform equal to the DC output load current.

Inductors are available in different styles such as pot core, toroid, E-core, bobbin core, and so forth, as well as different core materials, such as ferrites and powdered iron. The least expensive, the bobbin, rod or stick core, consists of wire wound on a ferrite bobbin. This type of construction makes for an inexpensive inductor, but because the magnetic flux is not completely contained within the core, it generates more Electro-Magnetic Interference (EMI). This magnetic flux can induce voltages into nearby printed-circuit traces, thus causing problems with both the switching regulator operation and nearby sensitive circuitry, and can give incorrect scope readings because of induced voltages in the scope probe (see *Open-Core Inductors*).

When multiple switching regulators are located on the same PCB, open-core magnetics can cause interference between two or more of the regulator circuits, especially at high currents. A torroid or E-core inductor (closed magnetic structure) should be used in these situations.

The inductors listed in the selection chart include ferrite E-core construction for Schottky, ferrite bobbin core for Renco and Coilcraft, and powdered iron toroid for Pulse Engineering.

Exceeding an inductor's maximum current rating may cause the inductor to overheat because of the copper wire losses, or the core may saturate. If the inductor begins to saturate, the inductance decreases rapidly and the inductor begins to look mainly resistive (the DC resistance of the winding). This can cause the switch current to rise very rapidly and force the switch into a cycle-by-cycle current limit, thus reducing the DC output load current. This can also result in overheating of the inductor or the LM2596. Different inductor types have different saturation characteristics, so consider this when selecting an inductor.

The inductor manufacturer's data sheets include current and energy limits to avoid inductor saturation.

For continuous mode operation, see the inductor selection graphs in Figure 27 through Figure 30.

Application Information (continued)

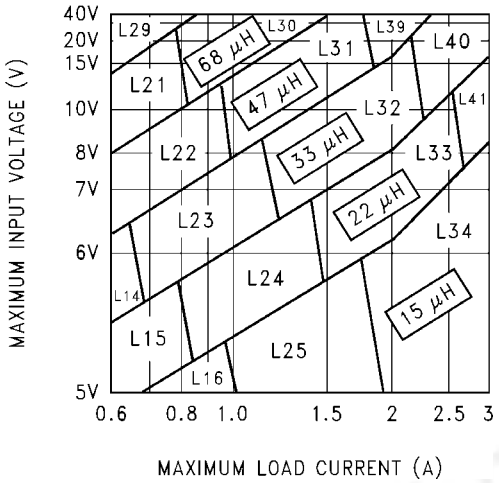


Figure 27. LM2596-3.3

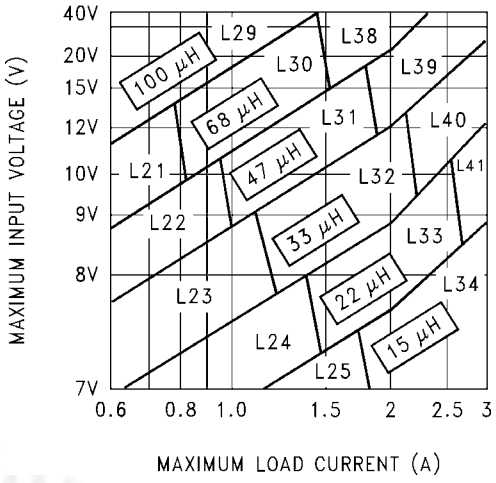


Figure 28. LM2596-5.0

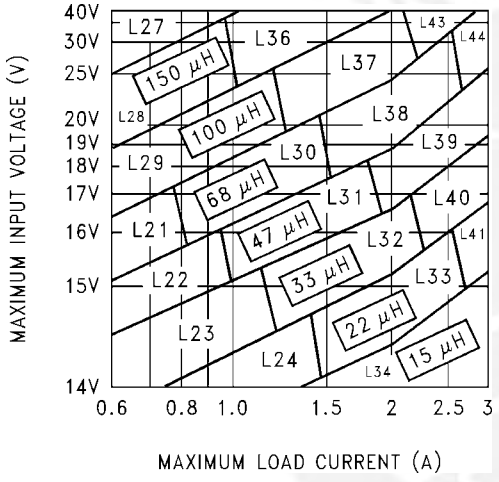


Figure 29. LM2596-12

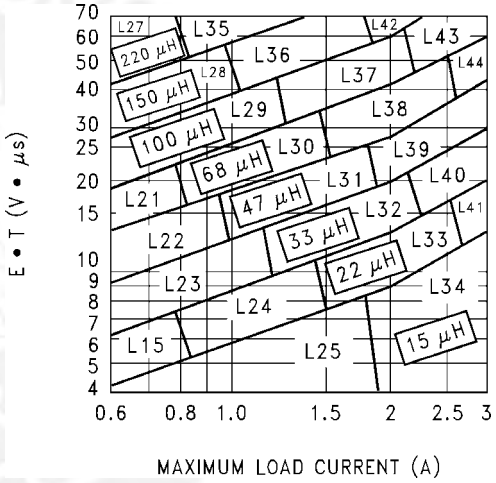


Figure 30. LM2596-ADJ

Table 1. Inductor Manufacturers Part Numbers

	INDUCTANCE (µH)	CURRENT (A)	SCHOTTKY		RENCO		PULSE ENGINEERING		COILCRAFT
			THROUGH-HOLE	SURFACE-MOUNT	THROUGH-HOLE	SURFACE-MOUNT	THROUGH-HOLE	SURFACE-MOUNT	SURFACE-MOUNT
L15	22	0.99	67148350	67148460	RL-1284-22-43	RL1500-22	PE-53815	PE-53815-S	DO3308-223
L21	68	0.99	67144070	67144450	RL-5471-5	RL1500-68	PE-53821	PE-53821-S	DO3316-683
L22	47	1.17	67144080	67144460	RL-5471-6	—	PE-53822	PE-53822-S	DO3316-473
L23	33	1.40	67144090	67144470	RL-5471-7	—	PE-53823	PE-53823-S	DO3316-333
L24	22	1.70	67148370	67148480	RL-1283-22-43	—	PE-53824	PE-53825-S	DO3316-223
L25	15	2.10	67148380	67148490	RL-1283-15-43	—	PE-53825	PE-53824-S	DO3316-153
L26	330	0.80	67144100	67144480	RL-5471-1	—	PE-53826	PE-53826-S	DO5022P-334
L27	220	1.00	67144110	67144490	RL-5471-2	—	PE-53827	PE-53827-S	DO5022P-224
L28	150	1.20	67144120	67144500	RL-5471-3	—	PE-53828	PE-53828-S	DO5022P-154
L29	100	1.47	67144130	67144510	RL-5471-4	—	PE-53829	PE-53829-S	DO5022P-104
L30	68	1.78	67144140	67144520	RL-5471-5	—	PE-53830	PE-53830-S	DO5022P-683
L31	47	2.20	67144150	67144530	RL-5471-6	—	PE-53831	PE-53831-S	DO5022P-473

Application Information (continued)

Table 1. Inductor Manufacturers Part Numbers (continued)

	INDUCTANCE (μH)	CURRENT (A)	SCHOTTKY		RENCO		PULSE ENGINEERING		COILCRAFT
			THROUGH-HOLE	SURFACE-MOUNT	THROUGH-HOLE	SURFACE-MOUNT	THROUGH-HOLE	SURFACE-MOUNT	SURFACE-MOUNT
L32	33	2.50	67144160	67144540	RL-5471-7	—	PE-53932	PE-53932-S	DO5022P-333
L33	22	3.10	67148390	67148500	RL-1283-22-43	—	PE-53933	PE-53933-S	DO5022P-223
L34	15	3.40	67148400	67148790	RL-1283-15-43	—	PE-53934	PE-53934-S	DO5022P-153
L35	220	1.70	67144170	—	RL-5473-1	—	PE-53935	PE-53935-S	—
L36	150	2.10	67144180	—	RL-5473-4	—	PE-54036	PE-54036-S	—
L37	100	2.50	67144190	—	RL-5472-1	—	PE-54037	PE-54037-S	—
L38	68	3.10	67144200	—	RL-5472-2	—	PE-54038	PE-54038-S	—
L39	47	3.50	67144210	—	RL-5472-3	—	PE-54039	PE-54039-S	—
L40	33	3.50	67144220	67148290	RL-5472-4	—	PE-54040	PE-54040-S	—
L41	22	3.50	67144230	67148300	RL-5472-5	—	PE-54041	PE-54041-S	—
L42	150	2.70	67148410	—	RL-5473-4	—	PE-54042	PE-54042-S	—
L43	100	3.40	67144240	—	RL-5473-2	—	PE-54043		—
L44	68	3.40	67144250	—	RL-5473-3	—	PE-54044		—

9.1.6 Output Voltage Ripple and Transients

The output voltage of a switching power supply operating in the continuous mode will contain a sawtooth ripple voltage at the switcher frequency, and may also contain short voltage spikes at the peaks of the sawtooth waveform.

The output ripple voltage is a function of the inductor sawtooth ripple current and the ESR of the output capacitor. A typical output ripple voltage can range from approximately 0.5% to 3% of the output voltage. To obtain low ripple voltage, the ESR of the output capacitor must be low; however, exercise caution when using extremely low ESR capacitors because they can affect the loop stability, resulting in oscillation problems. TI recommends a post ripple filter if very low output ripple voltage is required (less than 20 mV) (see Figure 32). The inductance required is typically between 1 μH and 5 μH, with low DC resistance, to maintain good load regulation. A low ESR output filter capacitor is also required to assure good dynamic load response and ripple reduction. The ESR of this capacitor may be as low as desired, because it is out of the regulator feedback loop. Figure 22 shows a typical output ripple voltage, with and without a post ripple filter.

When observing output ripple with a scope, it is essential that a short, low inductance scope probe ground connection be used. Most scope probe manufacturers provide a special probe terminator which is soldered onto the regulator board, preferably at the output capacitor. This provides a very short scope ground, thus eliminating the problems associated with the 3-inch ground lead normally provided with the probe, and provides a much cleaner and more accurate picture of the ripple voltage waveform.

The voltage spikes are caused by the fast switching action of the output switch and the diode, the parasitic inductance of the output filter capacitor, and its associated wiring. To minimize these voltage spikes, the output capacitor should be designed for switching regulator applications, and the lead lengths must be kept very short. Wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all contribute to the amplitude of these spikes.

When a switching regulator is operating in the continuous mode, the inductor current waveform ranges from a triangular to a sawtooth type of waveform (depending on the input voltage). For a given input and output voltage, the peak-to-peak amplitude of this inductor current waveform remains constant. As the load current increases or decreases, the entire sawtooth current waveform also rises and falls. The average value (or the center) of this current waveform is equal to the DC load current.

If the load current drops to a low enough level, the bottom of the sawtooth current waveform reaches zero, and the switcher smoothly changes from a continuous to a discontinuous mode of operation. Most switcher designs (regardless of how large the inductor value is) is forced to run discontinuous if the output is lightly loaded. This is a perfectly acceptable mode of operation.

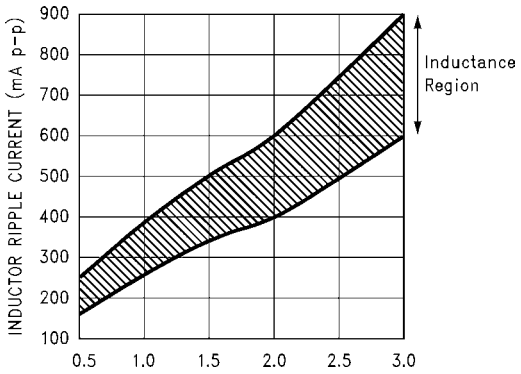


Figure 31. Peak-to-Peak Inductor Ripple Current vs Load Current

In a switching regulator design, knowing the value of the peak-to-peak inductor ripple current (ΔI_{IND}) can be useful for determining a number of other circuit parameters. Parameters such as peak inductor or peak switch current, minimum load current before the circuit becomes discontinuous, output ripple voltage, and output capacitor ESR can all be calculated from the peak-to-peak ΔI_{IND}. When the inductor nomographs in Figure 27 through *Figure 30* are used to select an inductor value, the peak-to-peak inductor ripple current can immediately be determined. Figure 31 shows the range of (ΔI_{IND}) that can be expected for different load currents. Figure 31 also shows how the peak-to-peak inductor ripple current (ΔI_{IND}) changes as you go from the lower border to the upper border (for a given load current) within an inductance region. The upper border represents a higher input voltage, while the lower border represents a lower input voltage.

These curves are only correct for continuous mode operation, and only if the inductor selection guides are used to select the inductor value.

Consider the following example:

V_{OUT} = 5 V, maximum load current of 2.5 A

V_{IN} = 12 V, nominal, varying between 10 V and 16 V.

The selection guide in Figure 28 shows that the vertical line for a 2.5-A load current and the horizontal line for the 12-V input voltage intersect approximately midway between the upper and lower borders of the 33-µH inductance region. A 33-µH inductor allows a peak-to-peak inductor current (ΔI_{IND}), which is a percentage of the maximum load current, to flow. In Figure 31, follow the 2.5-A line approximately midway into the inductance region, and read the peak-to-peak inductor ripple current (ΔI_{IND}) on the left hand axis (approximately 620 mAp-p).

As the input voltage increases to 16 V, approaching the upper border of the inductance region, the inductor ripple current increases. Figure 31shows that for a load current of 2.5 A, the peak-to-peak inductor ripple current (ΔI_{IND}) is 620 mA with 12 V_{IN}, and can range from 740 mA at the upper border (16 V_{IN}) to 500 mA at the lower border (10 V_{IN}).

Once the ΔI_{IND} value is known, use these equations to calculate additional information about the switching regulator circuit.

1. Peak Inductor or peak switch current $= \left(I_{LOAD} + \frac{\Delta I_{IND}}{2}\right) = \left(2.5A + \frac{0.62}{2}\right) = 2.81A$
2. Minimum load current before the circuit becomes discontinuous $= \frac{\Delta I_{IND}}{2} = \frac{0.62}{2} = 0.31A$
3. Output Ripple Voltage = (ΔI_{IND}) × (ESR of C_{OUT}) = 0.62 A × 0.1 Ω = 62 mVp-p
4. $$\text{ESR of } C_{OUT} = \frac{\text{Output Ripple Voltage } (\Delta V_{OUT})}{\Delta I_{IND}} = \frac{0.062V}{0.62A} = 0.1\Omega$$

9.1.7 Open-Core Inductors

Another possible source of increased output ripple voltage or unstable operation is from an open-core inductor. Ferrite bobbin or stick inductors have magnetic lines of flux flowing through the air from one end of the bobbin to the other end. These magnetic lines of flux will induce a voltage into any wire or PCB copper trace that comes within the inductor's magnetic field. The strength of the magnetic field, the orientation and location of the PC copper trace to the magnetic field, and the distance between the copper trace and the inductor determine the amount of voltage generated in the copper trace. Another way of looking at this inductive coupling is to consider the PCB copper trace as one turn of a transformer (secondary) with the inductor winding as the primary. Many millivolts can be generated in a copper trace located near an open-core inductor, which can cause stability problems or high output ripple voltage problems.

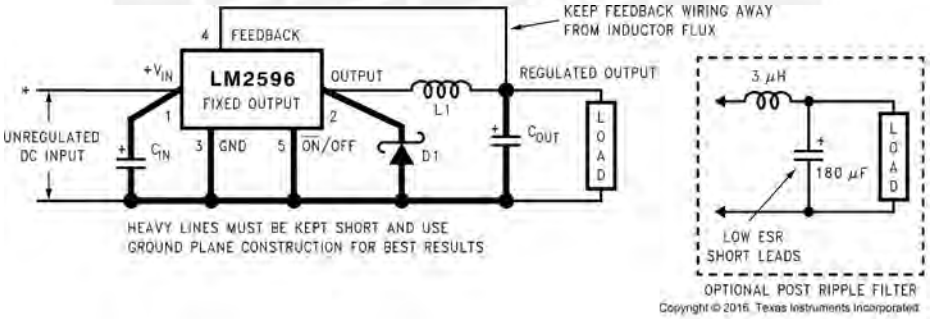
If unstable operation is seen, and an open-core inductor is used, it is possible that the location of the inductor with respect to other PC traces may be the problem. To determine if this is the problem, temporarily raise the inductor away from the board by several inches and then check circuit operation. If the circuit now operates correctly, then the magnetic flux from the open core inductor is causing the problem. Substituting a closed core inductor such as a torroid or E-core will correct the problem, or re-arranging the PC layout may be necessary. Magnetic flux cutting the IC device ground trace, feedback trace, or the positive or negative traces of the output capacitor should be minimized.

Sometimes, placing a trace directly beneath a bobbin inductor will provide good results, provided it is exactly in the center of the inductor (because the induced voltages cancel themselves out). However, problems could arise if the trace is off center one direction or the other. If flux problems are present, even the direction of the inductor winding can make a difference in some circuits.

This discussion on open core inductors is not to frighten users, but to alert users on what kind of problems to watch out for. Open-core bobbin or *stick* inductors are an inexpensive, simple way of making a compact, efficient inductor, and they are used by the millions in many different applications.

9.2 Typical Applications

9.2.1 LM2596 Fixed Output Series Buck Regulator



C_{IN} — 470-µF, 50-V, Aluminum Electrolytic Nichicon *PL Series*
C_{OUT} — 220-µF, 25-V Aluminum Electrolytic, Nichicon *PL Series*
D1 — 5-A, 40-V Schottky Rectifier, 1N5825
L1 — 68 µH, L38

Figure 32. Fixed Output Voltage Version

9.2.1.1 Design Requirements

Table 2 lists the design parameters for this example.

Table 2. Design Parameters

PARAMETER	EXAMPLE VALUE
Regulated Output Voltage (3.3 V, 5 V or 12 V), V_{OUT}	5 V
Maximum DC Input Voltage, V_{IN}(max)	12 V
Maximum Load Current, I_{LOAD}(max)	3 A

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Inductor Selection (L1)

1. Select the correct inductor value selection guide from Figure 27, Figure 28, or Figure 29 (output voltages of 3.3V, 5V, or 12V respectively). Use the inductor selection guide for the 5-V version shown in Figure 28.
2. From the inductor value selection guide, identify the inductance region intersected by the maximum input voltage line and the maximum load current line. Each region is identified by an inductance value and an inductor code (LXX). From the inductor value selection guide shown in Figure 28, the inductance region intersected by the 12-V horizontal line and the 3-A vertical line is 33 μH, and the inductor code is L40.
3. Select an appropriate inductor from the four manufacturer's part numbers listed in Table 1. The inductance value required is 33 μH. See row L40 of Table 1 and choose an inductor part number from any of the manufacturers shown. In most instances, both through-hole and surface-mount inductors are available.

9.2.1.2.2 Output Capacitor Selection (C_{OUT})

1. In the majority of applications, low ESR (Equivalent Series Resistance) electrolytic capacitors between 82 μF and 820 μF and low ESR solid tantalum capacitors between 10 μF and 470 μF provide the best results. This capacitor must be placed close to the IC using short capacitor leads and short copper traces. Do not use capacitors larger than 820 μF .

NOTE

For additional information, see section on output capacitors in Table 3.

2. To simplify the capacitor selection procedure, see Table 3 for quick design component selection. This table contains different input voltages, output voltages, and load currents, and lists various inductors and output capacitors that will provide the best design solutions.

   From Table 3, locate the 5-V output voltage section. In the load current column, choose the load current line that is closest to the current required for the application; for this example, use the 3-A line. In the maximum input voltage column, select the line that covers the input voltage required for the application; in this example, use the 15-V line. The rest of the line shows recommended inductors and capacitors that will provide the best overall performance.

Table 3. LM2596 Fixed Voltage Quick Design Component Selection Table

CONDITIONS			INDUCTOR		OUTPUT CAPACITOR			
					THROUGH-HOLE ELECTROLYTIC		SURFACE-MOUNT TANTALUM	
OUTPUT VOLTAGE (V)	LOAD CURRENT (A)	MAX INPUT VOLTAGE (V)	INDUCTANCE (μH)	INDUCTOR (#)	PANASONIC HFQ SERIES (μF/V)	NICHICON PL SERIES (μF/V)	AVX TPS SERIES (μF/V)	SPRAGUE 595D SERIES (μF/V)
3.3	3	5	22	L41	470/25	560/16	330/6.3	390/6.3
		7	22	L41	560/35	560/35	330/6.3	390/6.3
		10	22	L41	680/35	680/35	330/6.3	390/6.3
		40	33	L40	560/35	470/35	330/6.3	390/6.3
	2	6	22	L33	470/25	470/35	330/6.3	390/6.3
		10	33	L32	330/35	330/35	330/6.3	390/6.3
		40	47	L39	330/35	270/50	220/10	330/10
5	3	8	22	L41	470/25	560/16	220/10	330/10
		10	22	L41	560/25	560/25	220/10	330/10
		15	33	L40	330/35	330/35	220/10	330/10
		40	47	L39	330/35	270/35	220/10	330/10
	2	9	22	L33	470/25	560/16	220/10	330/10
		20	68	L38	180/35	180/35	100/10	270/10
		40	68	L38	180/35	180/35	100/10	270/10

Table 3. LM2596 Fixed Voltage Quick Design Component Selection Table (continued)

CONDITIONS			INDUCTOR		OUTPUT CAPACITOR			
					THROUGH-HOLE ELECTROLYTIC		SURFACE-MOUNT TANTALUM	
OUTPUT VOLTAGE (V)	LOAD CURRENT (A)	MAX INPUT VOLTAGE (V)	INDUCTANCE (µH)	INDUCTOR (#)	PANASONIC HFQ SERIES (µF/V)	NICHICON PL SERIES (µF/V)	AVX TPS SERIES (µF/V)	SPRAGUE 595D SERIES (µF/V)
12	3	15	22	L41	470/25	470/25	100/16	180/16
		18	33	L40	330/25	330/25	100/16	180/16
		30	68	L44	180/25	180/25	100/16	120/20
		40	68	L44	180/35	180/35	100/16	120/20
	2	15	33	L32	330/25	330/25	100/16	180/16
		20	68	L38	180/25	180/25	100/16	120/20
		40	150	L42	82/25	82/25	68/20	68/25

The capacitor list contains both through-hole electrolytic and surface-mount tantalum capacitors from four different capacitor manufacturers. TI recommends that both the manufacturers and the manufacturer's series that are listed in Table 3.

In this example aluminum electrolytic capacitors from several different manufacturers are available with the range of ESR numbers required.

– 330-µF, 35-V Panasonic HFQ Series
– 330-µF, 35-V Nichicon PL Series

3. The capacitor voltage rating for electrolytic capacitors should be at least 1.5 times greater than the output voltage, and often require much higher voltage ratings to satisfy the low ESR requirements for low output ripple voltage.

   For a 5-V output, a capacitor voltage rating of at least 7.5 V is required. But even a low ESR, switching grade, 220-µF, 10-V aluminum electrolytic capacitor would exhibit approximately 225 mΩ of ESR (see Figure 24 for the ESR vs voltage rating). This amount of ESR would result in relatively high output ripple voltage. To reduce the ripple to 1% or less of the output voltage, a capacitor with a higher value or with a higher voltage rating (lower ESR) must be selected. A 16-V or 25-V capacitor will reduce the ripple voltage by approximately half.

9.2.1.2.3 Catch Diode Selection (D1)

1. The catch diode current rating must be at least 1.3 times greater than the maximum load current. Also, if the power supply design must withstand a continuous output short, the diode must have a current rating equal to the maximum current limit of the LM2596. The most stressful condition for this diode is an overload or shorted output condition. See Table 4. In this example, a 5-A, 20-V, 1N5823 Schottky diode will provide the best performance, and will not be overstressed even for a shorted output.

Table 4. Diode Selection Table

VR	3-A DIODES				4-A TO 6-A DIODES			
	SURFACE-MOUNT		THROUGH-HOLE		SURFACE-MOUNT		THROUGH-HOLE	
	SCHOTTKY	ULTRA FAST RECOVERY	SCHOTTKY	ULTRA FAST RECOVERY	SCHOTTKY	ULTRA FAST RECOVERY	SCHOTTKY	ULTRA FAST RECOVERY
20 V		All of these diodes are rated to at least 50V.	1N5820	All of these diodes are rated to at least 50V.		All of these diodes are rated to at least 50V.	SR502	All of these diodes are rated to at least 50V.
	SK32		SR302				1N5823	
			MBR320				SB520	
30 V	30WQ03		1N5821					
	SK33		MBR330		50WQ03		SR503	
			31DQ03				1N5824	
			1N5822				SB530	
40 V	SK34		SR304		50WQ04		SR504	
	MBRS340		MBR340				1N5825	
	30WQ04	MURS320	31DQ04	MUR320		MURS620	SB540	MUR620
50 V	SK35	30WF10	SR305			50WF10		HER601
or	MBRS360		MBR350		50WQ05		SB550	
More	30WQ05		31DQ05				50SQ080	

2. The reverse voltage rating of the diode must be at least 1.25 times the maximum input voltage.
3. This diode must be fast (short reverse recovery time) and must be placed close to the LM2596 using short leads and short-printed circuit traces. Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best performance and efficiency, and must be the first choice, especially in low output voltage applications. Ultra-fast recovery, or high-efficiency rectifiers also provide good results. Ultra-fast recovery diodes typically have reverse recovery times of 50 ns or less. Rectifiers such as the 1N5400 series must not be used because they are too slow.

9.2.1.2.4 Input Capacitor (C_{IN})

A low ESR aluminum or tantalum bypass capacitor is required between the input pin and ground pin to prevent large voltage transients from appearing at the input. This capacitor must be placed close to the IC using short leads. In addition, the RMS current rating of the input capacitor should be selected to be at least ½ the DC load current. The capacitor manufacturers data sheet must be checked to assure that this current rating is not exceeded. Figure 23 shows typical RMS current ratings for several different aluminum electrolytic capacitor values.

For an aluminum electrolytic, the capacitor voltage rating must be approximately 1.5 times the maximum input voltage. Exercise caution if solid tantalum capacitors are used (see *Input Capacitor (C_{IN})*). The tantalum capacitor voltage rating should be 2 times the maximum input voltage and TI recommends that they be surge current tested by the manufacturer.

Use caution when using ceramic capacitors for input bypassing, because it may cause severe ringing at the V_{IN} pin.

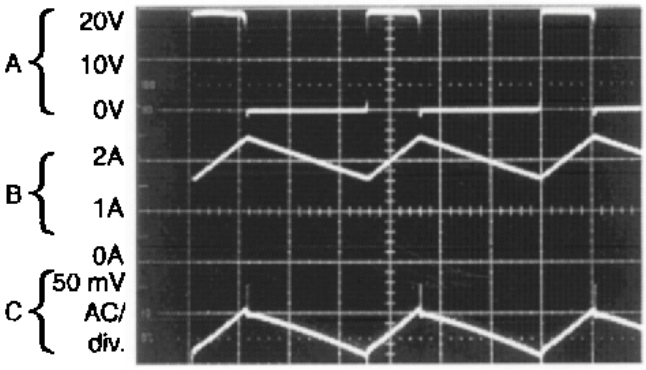
The important parameters for the Input capacitor are the input voltage rating and the RMS current rating. With a nominal input voltage of 12 V, an aluminum electrolytic capacitor with a voltage rating greater than 18 V ($1.5 \times V_{IN}$) is necessary. The next higher capacitor voltage rating is 25 V.

The RMS current rating requirement for the input capacitor in a buck regulator is approximately ½ the DC load current. In this example, with a 3-A load, a capacitor with a RMS current rating of at least 1.5 A is required. Figure 23 can be used to select an appropriate input capacitor. From the curves, locate the 35-V line and note which capacitor values have RMS current ratings greater than 1.5 A. A 680-μF, 35-V capacitor could be used.

For a through-hole design, a 680-μF, 35-V electrolytic capacitor (Panasonic HFQ series or Nichicon PL series or equivalent) would be adequate. Other types or other manufacturers' capacitors can be used provided the RMS ripple current ratings are adequate.

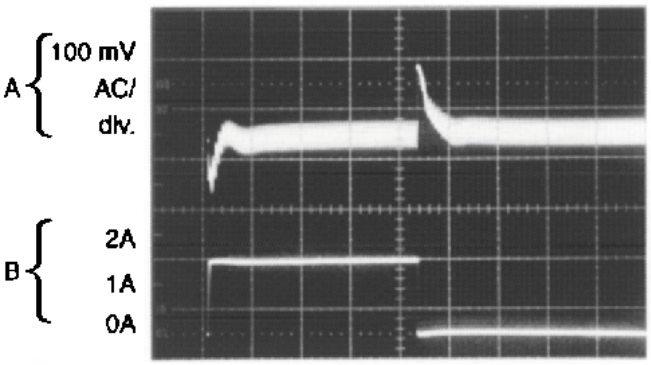
For surface-mount designs, solid tantalum capacitors can be used, but exercise caution with regard to the capacitor surge current rating (see *Input Capacitor (C_{IN})* in this data sheet). The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

9.2.1.3 Application Curves



Continuous Mode Switching Waveforms V_{IN} = 20 V, V_{OUT} = 5 V, I_{LOAD} = 2 A, L = 32 µH, C_{OUT} = 220 µF, C_{OUT} ESR = 50 mΩ
A: Output Pin Voltage, 10 V/div.
B: Inductor Current 1 A/div.
C: Output Ripple Voltage, 50 mV/div.

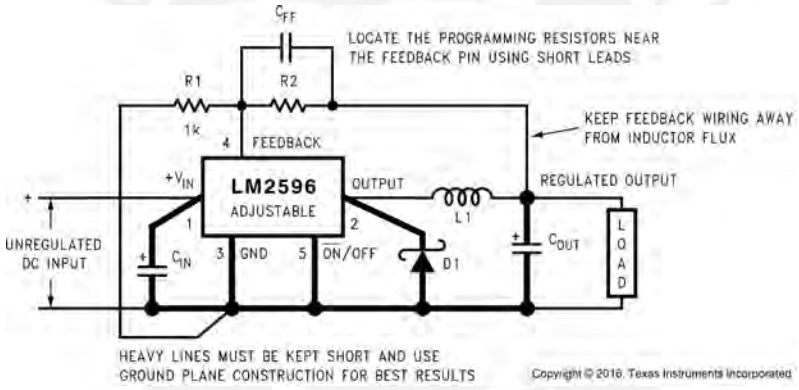
Figure 33. Horizontal Time Base: 2 µs/div



Load Transient Response for Continuous Mode V_{IN} = 20 V, V_{OUT} = 5 V, I_{LOAD} = 500 mA to 2 A, L = 32 µH, C_{OUT} = 220 µF, C_{OUT} ESR = 50 mΩ
A: Output Voltage, 100 mV/div. (AC)
B: 500-mA to 2-A Load Pulse

Figure 34. Horizontal Time Base: 100 µs/div

9.2.2 LM2596 Adjustable Output Series Buck Regulator



$$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right)$$

where V_{REF} = 1.23 V

$$R_2 = R_1\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

Select R_1 to be approximately 1 kΩ, use a 1% resistor for best stability.
C_{IN} — 470-µF, 50-V, Aluminum Electrolytic Nichicon *PL Series*
C_{OUT} — 220-µF, 35-V Aluminum Electrolytic, Nichicon *PL Series*
D1 — 5-A, 40-V Schottky Rectifier, 1N5825
L1 — 68 µH, L38
R1 — 1 kΩ, 1%
C_{FF} — See *Feedforward Capacitor (C_{FF})*

Figure 35. Adjustable Output Voltage Version

9.2.2.1 Design Requirements

Table 5 lists the design parameters for this example.

Table 5. Design Parameters

PARAMETER	EXAMPLE VALUE
Regulated output voltage (3.3V, 5V or 12V), V_{OUT}	20 V
Maximum DC input voltage, V_{IN}(max)	28 V
Maximum load current, I_{LOAD}(max)	3 A
Switching frequency, F	Fixed at a nominal 150 kHz

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the LM2596 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

9.2.2.2.2 Programming Output Voltage

Select R_1 and R_2, as shown in Table 6

Use Equation 1 to select the appropriate resistor values.

$$V_{OUT} = V_{REF}\left(1 + \frac{R_2}{R_1}\right) \quad \text{where } V_{REF} = 1.23V \tag{1}$$

Select a value for R_1 between 240 Ω and 1.5 kΩ. The lower resistor values minimize noise pickup in the sensitive feedback pin. (For the lowest temperature coefficient and the best stability with time, use 1% metal film resistors.). Calculate R_2 with Equation 2.

$$R_2 = R_1\left(\frac{V_{OUT}}{V_{REF}} - 1\right) \tag{2}$$

Select R_1 to be 1 kΩ, 1%. Solve for R_2 in Equation 3.

$$R_2 = R_1\left(\frac{V_{OUT}}{V_{REF}} - 1\right) = 1k\left(\frac{20V}{1.23V} - 1\right) \tag{3}$$

R_2 = 1k (16.26 − 1) = 15.26k, closest 1% value is 15.4 kΩ.

R_2 = 15.4 kΩ.

9.2.2.2.3 Inductor Selection (L1)

1. Calculate the inductor Volt • microsecond constant E × T (V × μs), with Equation 4:

$$E \bullet T = (V_{IN} - V_{OUT} - V_{SAT}) \bullet \frac{V_{OUT} + V_D}{V_{IN} - V_{SAT} + V_D} \bullet \frac{1000}{150\ kHz}\ (V \bullet \mu s) \tag{4}$$

where

- V_{SAT} = internal switch saturation voltage = 1.16 V
- V_D = diode forward voltage drop = 0.5 V

Calculate the inductor Volt • microsecond constant

(E × T),

$$E \bullet T = (28 - 20 - 1.16) \bullet \frac{20 + 0.5}{28 - 1.16 + 0.5} \bullet \frac{1000}{150} (V \bullet \mu s)$$

$$E \bullet T = (6.84) \bullet \frac{20.5}{27.34} \bullet 6.67 (V \bullet \mu s) = 34.2 (V \bullet \mu s) \quad (5)$$

2. Use the E × T value from the previous formula and match it with the E × T number on the vertical axis of the Inductor Value Selection Guide shown in Figure 30.

   E × T = 34.2 (V × μs)

3. On the horizontal axis, select the maximum load current.

   I_{LOAD}(max) = 3 A

4. Identify the inductance region intersected by the E × T value and the maximum load current value. Each region is identified by an inductance value and an inductor code (LXX). From the inductor value selection guide shown in Figure 30, the inductance region intersected by the 34 (V • μs) horizontal line and the 3-A vertical line is 47 μH, and the inductor code is L39.
5. Select an appropriate inductor from the manufacturers' part numbers listed in Table 1. From the table in *Table 1,* locate line L39, and select an inductor part number from the list of manufacturers part numbers.

9.2.2.2.4 Output Capacitor Selection (C_{OUT})

1. In the majority of applications, low ESR electrolytic or solid tantalum capacitors between 82 μF and 820 μF provide the best results. This capacitor must be placed close to the IC using short capacitor leads and short copper traces. Do not use capacitors larger than 820 μF.

NOTE

For additional information, see section on output capacitors in *Output Capacitor (C_{OUT})* section.

2. To simplify the capacitor selection procedure, see Table 6 for a quick design guide. This table contains different output voltages, and lists various output capacitors that will provide the best design solutions.

   From Table 6, locate the output voltage column. From that column, locate the output voltage closest to the output voltage in your application. In this example, select the 24-V line. Under the Output Capacitor (C_{OUT}) section, select a capacitor from the list of through-hole electrolytic or surface-mount tantalum types from four different capacitor manufacturers. TI recommends that both the manufacturers and the manufacturers' series that are listed in Table 6 be used.

   In this example, through hole aluminum electrolytic capacitors from several different manufacturers are available.
   – 220-μF, 35-V Panasonic HFQ Series
   – 150-μF, 35-V Nichicon PL Series
3. The capacitor voltage rating must be at least 1.5 times greater than the output voltage, and often much higher voltage ratings are required to satisfy the low ESR requirements required for low output ripple voltage.

   For a 20-V output, a capacitor rating of at least 30 V is required. In this example, either a 35-V or 50-V capacitor would work. A 35-V rating was chosen, although a 50-V rating could also be used if a lower output ripple voltage is required.

   Other manufacturers or other types of capacitors may also be used, provided the capacitor specifications (especially the 100-kHz ESR) closely match the types listed in Table 6. Refer to the capacitor manufacturers data sheet for this information.

9.2.2.2.5 Feedforward Capacitor (C_{FF})

See Table 6.

For output voltages greater than approximately 10 V, an additional capacitor is required. The compensation capacitor is typically between 100 pF and 33 nF, and is wired in parallel with the output voltage setting resistor, R_2. It provides additional stability for high output voltages, low input or output voltages, or very low ESR output capacitors, such as solid tantalum capacitors. Calculate the value for C_{FF} with Equation 6:

$$C_{FF} = \frac{1}{31 \times 10^3 \times R_2} \quad (6)$$

This capacitor type can be ceramic, plastic, silver mica, and so forth. Because of the unstable characteristics of ceramic capacitors made with Z5U material, they are not recommended.

Table 6 contains feedforward capacitor values for various output voltages. In this example, a 560-pF capacitor is required.

Table 6. Output Capacitor and Feedforward Capacitor Selection Table

OUTPUT VOLTAGE (V)	THROUGH-HOLE OUTPUT CAPACITOR			SURFACE-MOUNT OUTPUT CAPACITOR		
	PANASONIC HFQ SERIES (µF/V)	NICHICON PL SERIES (µF/V)	FEEDFORWARD CAPACITOR	AVX TPS SERIES (µF/V)	SPRAGUE 595D SERIES (µF/V)	FEEDFORWARD CAPACITOR
2	820/35	820/35	33 nF	330/6.3	470/4	33 nF
4	560/35	470/35	10 nF	330/6.3	390/6.3	10 nF
6	470/25	470/25	3.3 nF	220/10	330/10	3.3 nF
9	330/25	330/25	1.5 nF	100/16	180/16	1.5 nF
1 2	330/25	330/25	1 nF	100/16	180/16	1 nF
1 5	220/35	220/35	680 pF	68/20	120/20	680 pF
2 4	220/35	150/35	560 pF	33/25	33/25	220 pF
2 8	100/50	100/50	390 pF	10/35	15/50	220 pF

9.2.2.2.6 Catch Diode Selection (D1)

1. The catch diode current rating must be at least 1.3 times greater than the maximum load current. Also, if the power supply design must withstand a continuous output short, the diode must have a current rating equal to the maximum current limit of the LM2596. The most stressful condition for this diode is an overload or shorted output condition. See Table 4. Schottky diodes provide the best performance, and in this example a 5-A, 40-V, 1N5825 Schottky diode would be a good choice. The 5-A diode rating is more than adequate and will not be overstressed even for a shorted output.
2. The reverse voltage rating of the diode must be at least 1.25 times the maximum input voltage.
3. This diode must be fast (short reverse recovery time) and must be placed close to the LM2596 using short leads and short-printed circuit traces. Because of their fast switching speed and low forward voltage drop, Schottky diodes provide the best performance and efficiency, and must be the first choice, especially in low output voltage applications. Ultra-fast recovery or high-efficiency rectifiers are also good choices, but some types with an abrupt turnoff characteristic may cause instability or EMI problems. Ultra-fast recovery diodes typically have reverse recovery times of 50 ns or less. Rectifiers such as the 1N4001 series must not be used because they are too slow.

9.2.2.2.7 Input Capacitor (C_{IN})

A low ESR aluminum or tantalum bypass capacitor is required between the input pin and ground to prevent large voltage transients from appearing at the input. In addition, the RMS current rating of the input capacitor should be selected to be at least ½ the DC load current. The capacitor manufacturers data sheet must be checked to assure that this current rating is not exceeded. Figure 23 shows typical RMS current ratings for several different aluminum electrolytic capacitor values.

This capacitor must be placed close to the IC using short leads and the voltage rating must be approximately 1.5 times the maximum input voltage.

If solid tantalum input capacitors are used, TI recommends that they be surge current tested by the manufacturer.

Use caution when using a high dielectric constant ceramic capacitor for input bypassing, because it may cause severe ringing at the V_{IN} pin.

The important parameters for the input capacitor are the input voltage rating and the RMS current rating. With a nominal input voltage of 28 V, an aluminum electrolytic aluminum electrolytic capacitor with a voltage rating greater than 42 V (1.5 × V_{IN}) is required. Because the the next higher capacitor voltage rating is 50 V, a 50-V capacitor must be used. The capacitor voltage rating of (1.5 × V_{IN}) is a conservative guideline, and can be modified somewhat if desired.

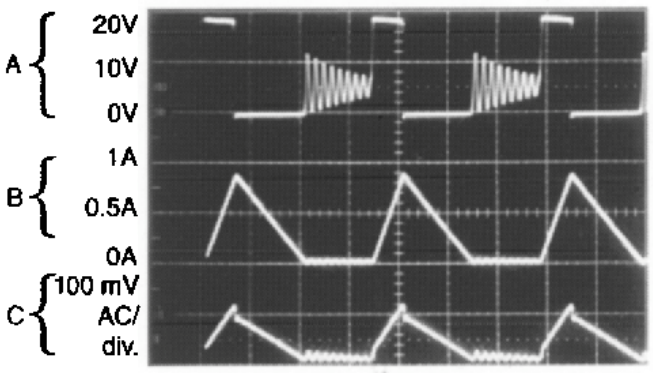
The RMS current rating requirement for the input capacitor of a buck regulator is approximately ½ the DC load current. In this example, with a 3-A load, a capacitor with a RMS current rating of at least 1.5 A is required.

Figure 23 can be used to select an appropriate input capacitor. From the curves, locate the 50-V line and note which capacitor values have RMS current ratings greater than 1.5 A. Either a 470 µF or 680 µF, 50-V capacitor could be used.

For a through hole design, a 680-µF, 50-V electrolytic capacitor (Panasonic HFQ series or Nichicon PL series or equivalent) would be adequate. Other types or other manufacturers' capacitors can be used provided the RMS ripple current ratings are adequate.

For surface mount designs, solid tantalum capacitors can be used, but exercise caution with regard to the capacitor surge current rating (see *Input Capacitor (C_{IN})* in this data sheet). The TPS series available from AVX, and the 593D series from Sprague are both surge current tested.

9.2.2.3 Application Curves



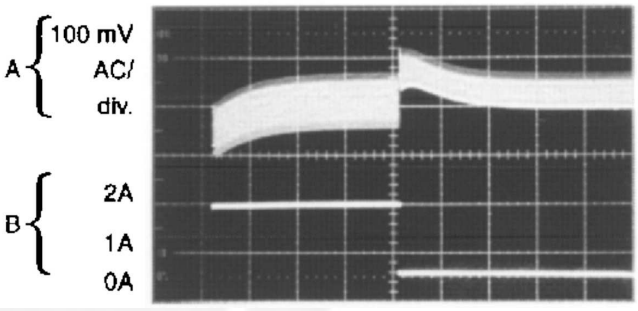
Discontinuous Mode Switching Waveforms V_{IN} = 20 V, V_{OUT} = 5 V, I_{LOAD} = 500 mA L = 10 µH, C_{OUT} = 330 µF, C_{OUT} ESR = 45 mΩ

A: Output Pin Voltage, 10 V/div.

B: Inductor Current 0.5 A/div.

C: Output Ripple Voltage, 100 mV/div.

Figure 36. Horizontal Time Base: 2 µs/div



Load Transient Response for Discontinuous Mode V_{IN} = 20 V, V_{OUT} = 5V, I_{LOAD} = 500 mA to 2 A, L = 10 µH, C_{OUT} = 330 µF, C_{OUT} ESR = 45 mΩ

A: Output Voltage, 100 mV/div. (AC)

B: 500-mA to 2-A Load Pulse

Figure 37. Horizontal Time Base: 200 µs/div

10 Power Supply Recommendations

The LM2596 is designed to operate from an input voltage supply up to 40 V. This input supply must be well regulated and able to withstand maximum input current and maintain a stable voltage.

11 Layout

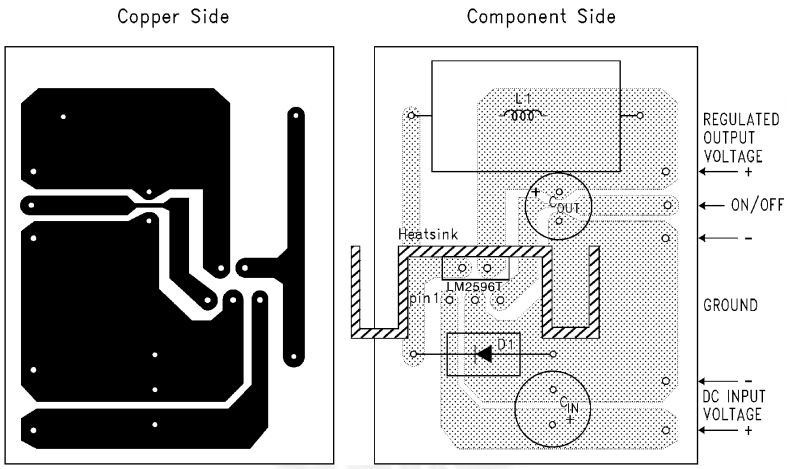
11.1 Layout Guidelines

As in any switching regulator, layout is very important. Rapidly switching currents associated with wiring inductance can generate voltage transients which can cause problems. For minimal inductance and ground loops, the wires indicated by heavy lines must be wide printed-circuit traces and must be kept as short as possible. For best results, external components must be placed as close to the switcher IC as possible using ground plane construction or single point grounding.

If open core inductors are used, take special care selecting the location and positioning of this type of inductor. Allowing the inductor flux to intersect sensitive feedback, IC groundpath and C_{OUT} wiring can cause problems.

When using the adjustable version, take special care selecting the location of the feedback resistors and the associated wiring. Physically place both resistors near the IC, and route the wiring away from the inductor, especially an open-core type of inductor (see *Open-Core Inductors* for more information).

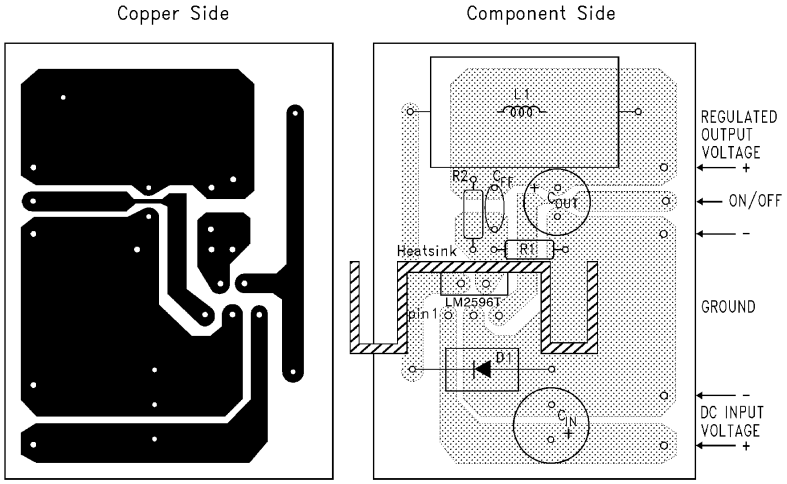
11.2 Layout Examples



C_{IN} — 470-µF, 50-V, Aluminum Electrolytic Panasonic, *HFQ Series*
C_{OUT} — 330-µF, 35-V, Aluminum Electrolytic Panasonic, *HFQ Series*
D1 — 5-A, 40-V Schottky Rectifier, 1N5825
L1 — 47-µH, L39, Renco, Through Hole
Thermalloy Heat Sink #7020

Figure 38. Typical Through-Hole PCB Layout, Fixed Output (1x Size), Double-Sided

Layout Examples (continued)



C_{IN}— 470-µF, 50-V, Aluminum Electrolytic Panasonic, *HFQ Series*
C_{OUT}—220-µF, 35-V Aluminum Electrolytic Panasonic, *HFQ Series*
D1—5-A, 40-V Schottky Rectifier, 1N5825
L1—47-µH, L39, Renco, Through Hole
R_1—1 kΩ, 1%
R_2—Use formula in Design Procedure
C_{FF}—See Table 6.
Thermalloy Heat Sink #7020

Figure 39. Typical Through-Hole PCB Layout, Adjustable Output (1x Size), Double-Sided

11.3 Thermal Considerations

The LM2596 is available in two packages: a 7-pin TO-220 (T) and a 7-pin surface mount TO-263 (S).

The TO-220 package requires a heat sink under most conditions. The size of the heat sink depends on the input voltage, the output voltage, the load current and the ambient temperature. Figure 40 shows the LM2596T junction temperature rises above ambient temperature for a 3-A load and different input and output voltages. The data for these curves was taken with the LM2596T (TO-220 package) operating as a buck switching regulator in an ambient temperature of 25°C (still air). These temperature rise numbers are all approximate and there are many factors that can affect these temperatures. Higher ambient temperatures require more heat sinking.

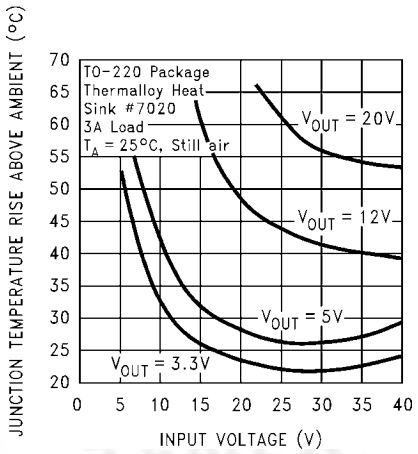
The TO-263 surface mount package tab is designed to be soldered to the copper on a printed-circuit board (PCB). The copper and the board are the heat sink for this package and the other heat producing components, such as the catch diode and inductor. The PCB copper area that the package is soldered to must be at least 0.4 in^2, and ideally must have 2 or more square inches of 2-oz. (0.0028 in.) copper. Additional copper area improves the thermal characteristics, but with copper areas greater than approximately 6 in^2, only small improvements in heat dissipation are realized. If further thermal improvements are required, TI recommends double-sided, multilayer PCB with large copper areas and airflow.

Figure 41 shows the LM2596S (TO-263 package) junction temperature rise above ambient temperature with a 2-A load for various input and output voltages. This data was taken with the circuit operating as a buck switching regulator with all components mounted on a PCB to simulate the junction temperature under actual operating conditions. This curve can be used for a quick check for the approximate junction temperature for various conditions, but be aware that there are many factors that can affect the junction temperature. When load currents higher than 2 A are used, double-sided or multilayer PCB with large copper areas or airflow might be required, especially for high ambient temperatures and high output voltages.

For the best thermal performance, wide copper traces and generous amounts of PCB copper must be used in the board layout. (One exception to this is the output (switch) pin, which should **not** have large areas of copper.) Large areas of copper provide the best transfer of heat (lower thermal resistance) to the surrounding air, and moving air lowers the thermal resistance even further.

Package thermal resistance and junction temperature rise numbers are all approximate, and there are many factors that will affect these numbers. Some of these factors include board size, shape, thickness, position, location, and even board temperature. Other factors are trace width, total printed-circuit copper area, copper thickness, single- or double-sided multilayer board, and the amount of solder on the board. The effectiveness of the PCB to dissipate heat also depends on the size, quantity, and spacing of other components on the board, as well as whether the surrounding air is still or moving. Furthermore, some of these components such as the catch diode will add heat to the PCB and the heat can vary as the input voltage changes. For the inductor, depending on the physical size, type of core material, and the DC resistance, it could either act as a heat sink taking heat away from the board, or it could add heat to the board.

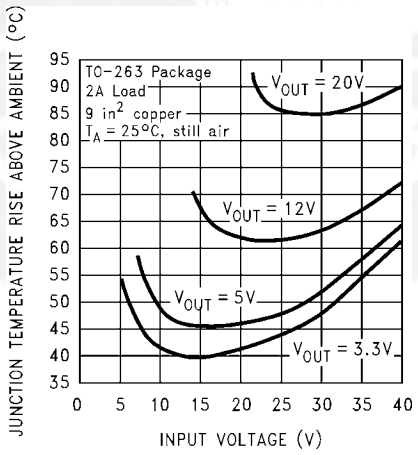
Thermal Considerations (continued)



CIRCUIT DATA FOR TEMPERATURE RISE CURVE TO-220 PACKAGE (T)

Capacitors	Through-hole electrolytic
Inductor	Through-hole, Renco
Diode	Through-hole, 5-A 40-V, Schottky
PCB	3-square inch, single-sided, 2-oz. copper (0.0028″)

Figure 40. Junction Temperature Rise, TO-220



CIRCUIT DATA FOR TEMPERATURE RISE CURVE TO-263 PACKAGE (S)

Capacitors	Surface-mount tantalum, molded *D* size
Inductor	Surface-mount, Pulse Engineering, 68 μH
Diode	Surface-mount, 5-A 40-V, Schottky
PCB	9-square inch, single-sided, 2-oz. copper (0.0028″)

Figure 41. Junction Temperature Rise, TO-263

12 Device and Documentation Support

12.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the LM2596 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2596S-12/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR		LM2596S -12 P+	Samples
LM2596S-3.3	NRND	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI		LM2596S -3.3 P+	
LM2596S-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR		LM2596S -3.3 P+	Samples
LM2596S-5.0	NRND	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI		LM2596S -5.0 P+	
LM2596S-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR		LM2596S -5.0 P+	Samples
LM2596S-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2596S -ADJ P+	Samples
LM2596SX-12/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR		LM2596S -12 P+	Samples
LM2596SX-3.3	NRND	DDPAK/ TO-263	KTT	5	500	TBD	Call TI	Call TI		LM2596S -3.3 P+	
LM2596SX-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR		LM2596S -3.3 P+	Samples
LM2596SX-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR		LM2596S -5.0 P+	Samples
LM2596SX-ADJ	NRND	DDPAK/ TO-263	KTT	5	500	TBD	Call TI	Call TI	-40 to 125	LM2596S -ADJ P+	
LM2596SX-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LM2596S -ADJ P+	Samples
LM2596T-12/LF03	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM2596T -12 P+	Samples
LM2596T-12/NOPB	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM2596T -12 P+	Samples
LM2596T-3.3/LF03	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM2596T -3.3 P+	Samples
LM2596T-3.3/NOPB	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM2596T -3.3 P+	Samples
LM2596T-5.0	NRND	TO-220	NDH	5	45	TBD	Call TI	Call TI		LM2596T -5.0 P+	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2596T-5.0/LF03	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM2596T -5.0 P+	Samples
LM2596T-5.0/NOPB	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM2596T -5.0 P+	Samples
LM2596T-ADJ	NRND	TO-220	NDH	5	45	TBD	Call TI	Call TI	-40 to 125	LM2596T -ADJ P+	
LM2596T-ADJ/LB05	NRND	TO-220	NEB	5	45	TBD	Call TI	Call TI		LM2596T -ADJ P+	
LM2596T-ADJ/LF02	ACTIVE	TO-220	NEB	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM		LM2596T -ADJ P+	Samples
LM2596T-ADJ/NOPB	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LM2596T -ADJ P+	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

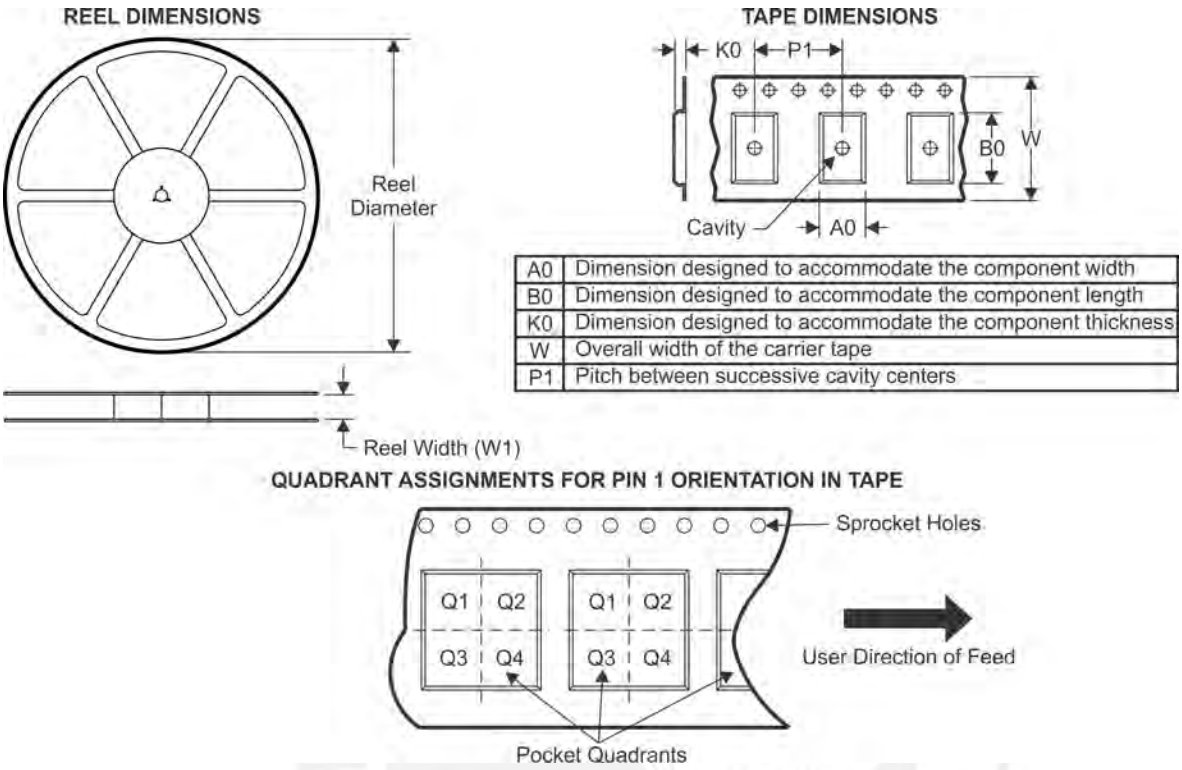
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

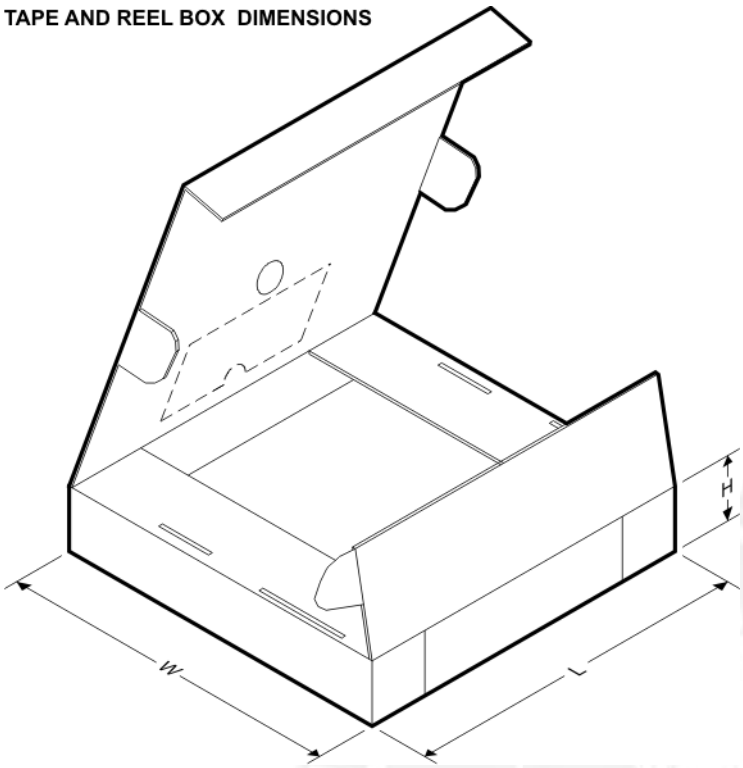


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2596SX-12/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM2596SX-3.3	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM2596SX-3.3/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM2596SX-5.0/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM2596SX-ADJ	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LM2596SX-ADJ/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2596SX-12/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LM2596SX-3.3	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LM2596SX-3.3/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LM2596SX-5.0/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LM2596SX-ADJ	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LM2596SX-ADJ/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0

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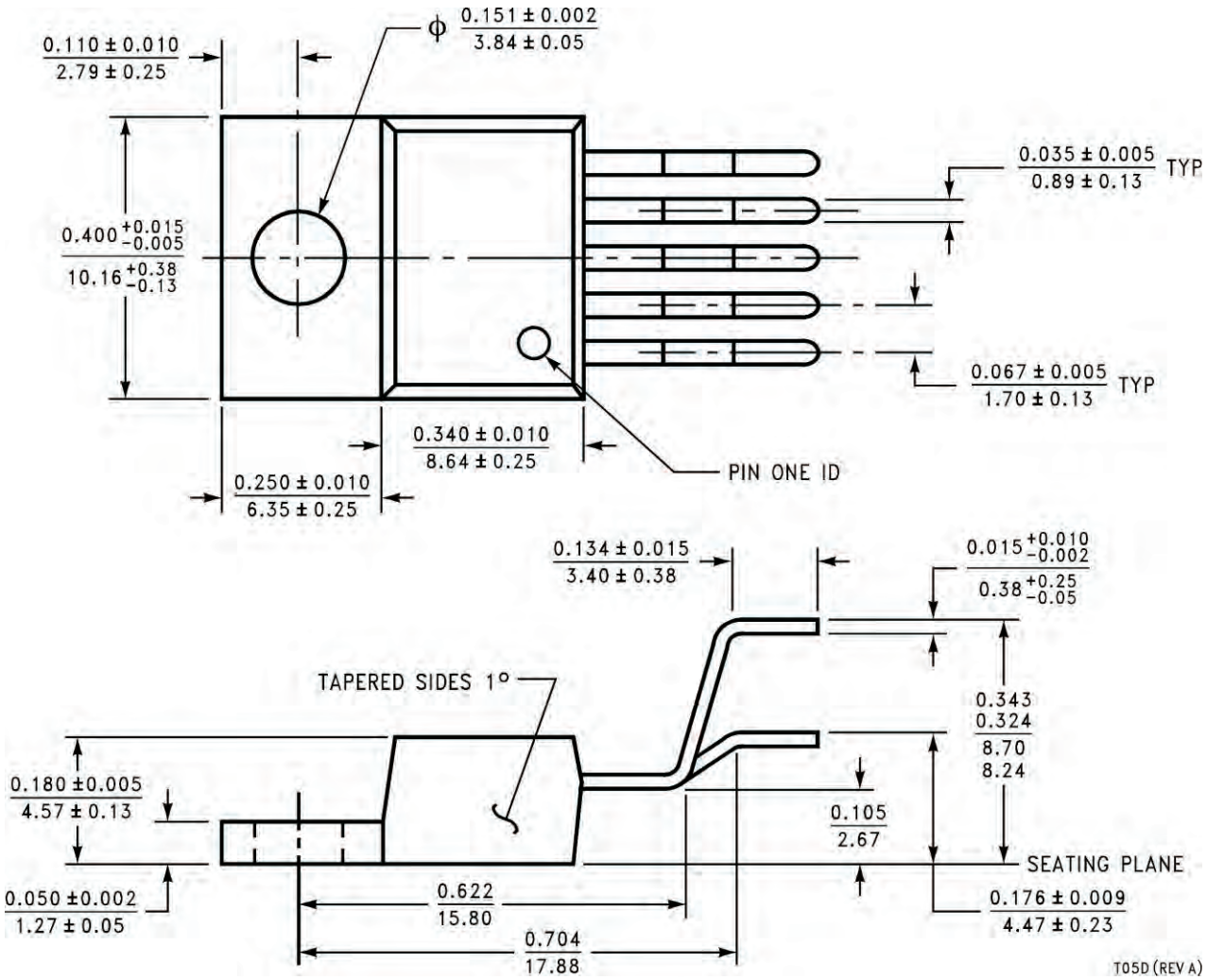

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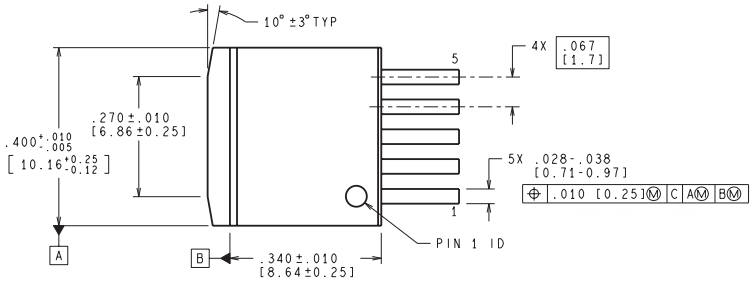
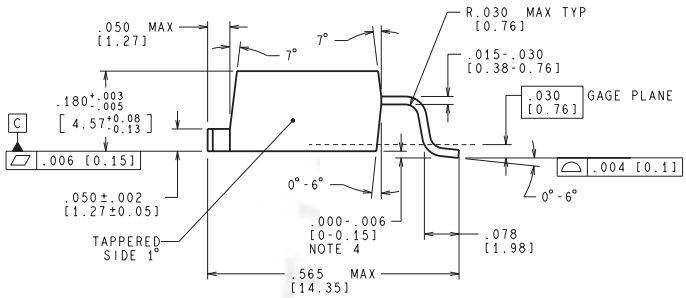
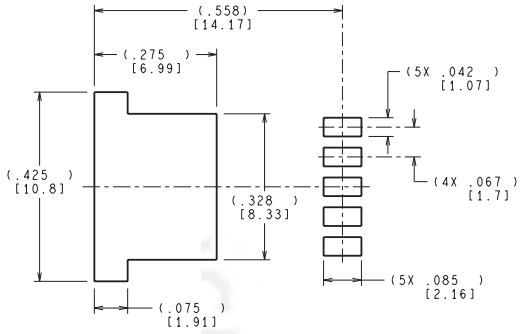
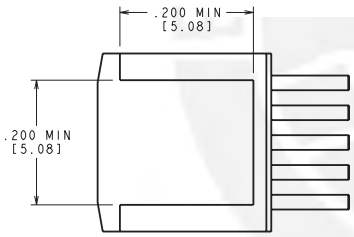






LAND PATTERN RECOMMENDATION



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CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

TS5B (Rev D)

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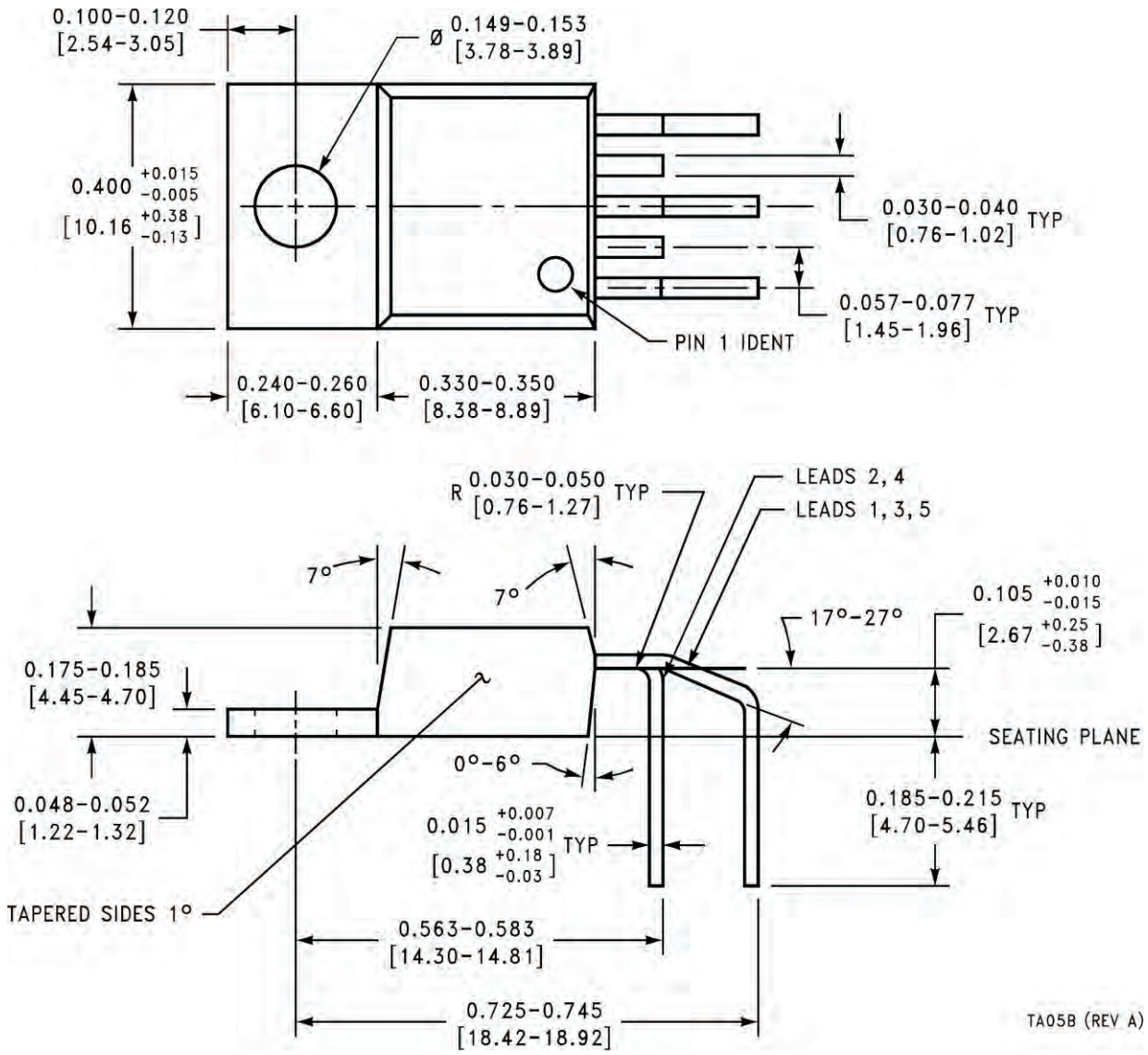

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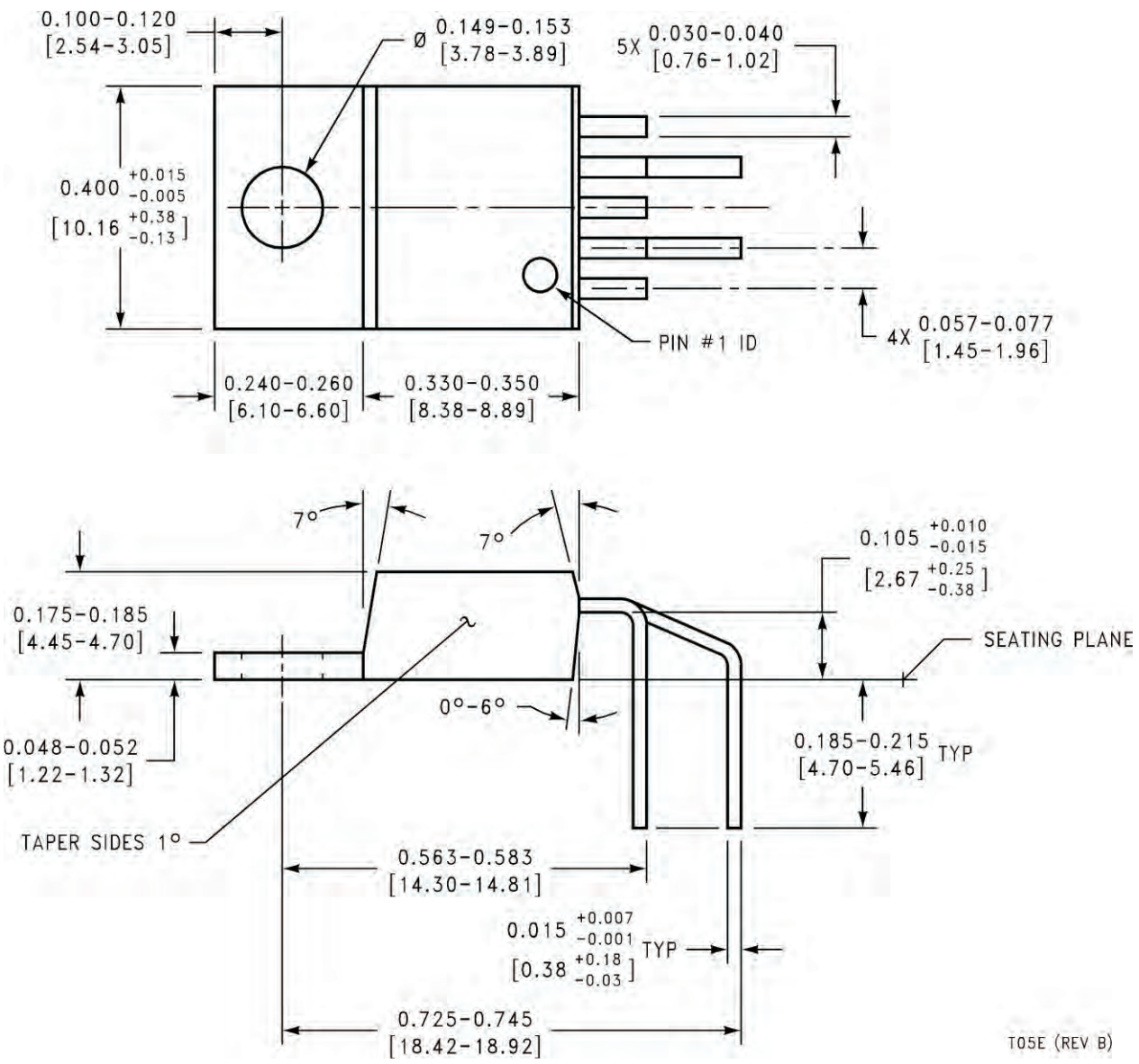

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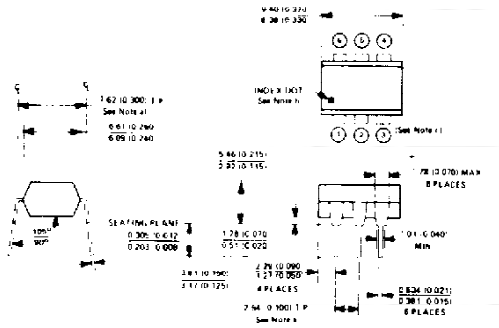
SOOS035 D2493 SEPTEMBER 1978 - REVISED MARCH 1983

COMPATIBLE WITH STANDARD TTL INTEGRATED CIRCUITS

- **Gallium Arsenide Diode Infrared Source Optically Coupled to a Silicon N-P-N Phototransistor**
- **High Direct-Current Transfer Ratio**
- **High-Voltage Electrical Isolation . . . 2.5-kV, 1.5-kV, or 0.5-kV Rating**
- **Plastic Dual-In-Line Package**
- **High-Speed Switching . . . t_r = 2 μs, t_f = 2 μs Typical**

mechanical data

The package consists of a gallium arsenide infrared-emitting diode and an n-p-n silicon phototransistor mounted on a 6-lead frame encapsulated within an electrically nonconductive plastic compound. The case will withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions. Unit weight is approximately 0.52 grams.



NOTES:
a. Leads are within 0,127 (0.005) radius of true position (T.P.) with maximum material condition and unit installed.
b. Pin 1 identified by index dot.
c. Terminal connections:
1. Anode } Infrared-emitting diode
2. Cathode
3. No internal connection
4. Emitter } Phototransistor
5. Collector
6. Base

FALLS WITHIN JEDEC MO-001AM DIMENSIONS
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

*Peak Input-to-Output Voltage: 4N25	±2.5 kV
4N26, 4N27	±1.5 kV
4N28	±0.5 kV
*Collector-Base Voltage	70 V
*Collector-Emitter Voltage (See Note 1)	30 V
*Emitter-Collector Voltage	7 V
Emitter-Base Voltage	7 V
*Input-Diode Reverse Voltage	3 V
*Input-Diode Continuous Forward Current at (or below) 25°C Free-Air Temperature (See Note 2)	80 mA
*Input-Diode Peak Forward Current (t_W = 300 μs, duty cycle = 2%)	3 A
*Continuous Power Dissipation at (or below) 25°C Free-Air Temperature:	
Infrared-Emitting Diode (See Note 3)	150 mW
Phototransistor (See Note 3)	150 mW
Total, Infrared-Emitting Diode plus Phototransistor (See Note 4)	250 mW
*Storage Temperature Range	−55°C to 150°C
*Lead Temperature 1,6 mm (1/16 inch) from Case for 10 Seconds	260°C

*JEDEC registered data. This data sheet contains all applicable JEDEC-registered data in effect at the time of publication.

NOTES: 1. This value applies when the base-emitter diode is open-circulated.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mA/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 2 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 3.33 mW/°C.

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electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	4N25, 4N26			4N27, 4N28			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
*$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 µA, I_E = 0, I_F = 0	70			70			V
*$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 1 mA, I_B = 0, I_F = 0	30			30			V
*$V_{(BR)ECO}$	Emitter-Collector Breakdown Voltage	I_E = 100 µA, I_B = 0, I_F = 0	7			7			V
*I_R	Input Diode Static Reverse Current	V_R = 3 V			100			100	µA
*$I_{C(on)}$	On-State Collector Current (Phototransistor Operation)	V_{CE} = 10 V, I_B = 0, I_F = 10 mA	2	5		1	3		mA
$I_{C(on)}$	On-State Collector Current (Photodiode Operation)	V_{CB} = 10 V, I_E = 0, I_F = 10 mA		20			20		µA
*$I_{C(off)}$	Off-State Collector Current (Phototransistor Operation)	V_{CE} = 10 V, I_B = 0, I_F = 0		1	50		1	50	nA
*$I_{C(off)}$	Off-State Collector current (Photodiode Operation)	V_{CB} = 10 V, I_E = 0, I_F = 0		0.1	20		0.1	20	nA
*V_F	Input Diode Static Forward Voltage	I_F = 10 mA		1.25	1.5		1.25	1.5	V
*$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_C = 2 mA, I_B = 0, I_F = 50 mA		0.25	0.5		0.25	0.5	V
r_{IO}	Input-to-Output Internal resistance	V_{in-out} = ±2.5 kV for 4N25, ±1.5 kV for 4N26, 4N27, ±0.5 kV for 4N28, See Note 5	10^{11}	10^{12}		10^{11}	10^{12}		Ω
C_{io}	Input-to-Output Capacitance	V_{in-out} = 0, f = 1 MHz, See Note 5		1			1		pF

*JEDEC registered data

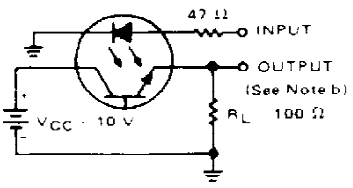
NOTE 5: These parameters are measured between both input diode leads shorted together and all the phototransistor leads shorted together

switching characteristics at 25°C free-air temperature

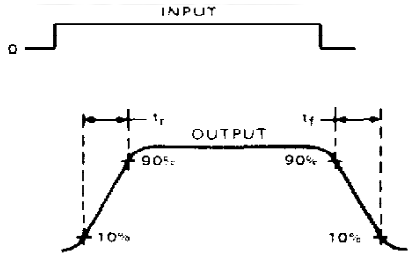
PARAMETER			TEST CONDITIONS	TYP	UNIT
t_r	Rise Time	Phototransistor Operation	V_{CC} = 10 V, I_B = 0, $I_{C(on)}$ = 2 mA, R_L = 100 Ω, See Test Circuit A of Figure 1	2	µs
t_f	Fall Time			2	
t_r	Rise Time	Photodiode Operation	V_{CC} = 10 V, I_E = 0, $I_{C(on)}$ = 20 µA, R_L = 1 kΩ, See Test Circuit B of Figure 1	1	µs
t_f	Fall Time			1	

PARAMETER MEASUREMENT INFORMATION

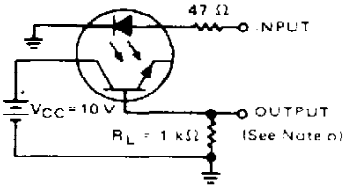
Adjust amplitude of input pulse for:
$I_{C(on)}$ = 2 mA (Test Circuit A) or
$I_{C(on)}$ = 20 µA (Test Circuit B)



TEST CIRCUIT A
PHOTOTRANSISTOR OPERATION



VOLTAGE WAVEFORMS



TEST CIRCUIT B
PHOTODIODE OPERATION

NOTES a. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω, t_r ≤ 15 ns, duty cycle ≈ 1%, t_w = 100 µs.
b. The output waveform is monitored on an oscilloscope with the following characteristics: t_r ≤ 12 ns, R_{in} ≥ 1 MΩ, C_{in} ≤ 20 pF.

FIGURE 1 – SWITCHING TIMES

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
4N25	OBSOLETE	PDIP	N	6		TBD	Call TI	Call TI
4N26	OBSOLETE	PDIP	N	6		TBD	Call TI	Call TI
4N27	OBSOLETE	PDIP	P	6		TBD	Call TI	Call TI
4N28	OBSOLETE	PDIP	N	6		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
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OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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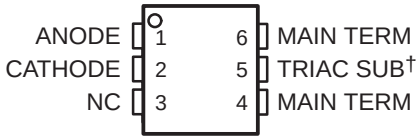
- **400 V Phototriac Driver Output**
- **Gallium-Arsenide-Diode Infrared Source and Optically-Coupled Silicon Traic Driver (Bilateral Switch)**
- **UL Recognized . . . File Number E65085**
- **High Isolation . . . 7500 V Peak**
- **Output Driver Designed for 220 Vac**
- **Standard 6-Terminal Plastic DIP**
- **Directly Interchangeable with Motorola MOC3020, MOC3021, MOC3022, and MOC3023**

typical 115/240 Vac(rms) applications

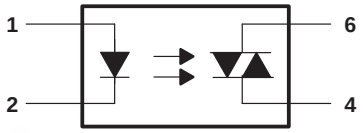
- **Solenoid/Valve Controls**
- **Lamp Ballasts**
- **Interfacing Microprocessors to 115/240 Vac Peripherals**
- **Motor Controls**
- **Incandescent Lamp Dimmers**

MOC3020 – MOC3023 . . . PACKAGE
(TOP VIEW)



† Do not connect this terminal
NC – No internal connection

logic diagram



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Input-to-output peak voltage, 5 s maximum duration, 60 Hz (see Note 1)	7.5 kV
Input diode reverse voltage	3 V
Input diode forward current, continuous	50 mA
Output repetitive peak off-state voltage	400 V
Output on-state current, total rms value (50-60 Hz, full sine wave): T_A = 25°C	100 mA
T_A = 70°C	50 mA
Output driver nonrepetitive peak on-state current (t_w = 10 ms, duty cycle = 10%, see Figure 7)	1.2 A
Continuous power dissipation at (or below) 25°C free-air temperature:	
Infrared-emitting diode (see Note 2)	100 mW
Phototriac (see Note 3)	300 mW
Total device (see Note 4)	330 mW
Operating junction temperature range, T_J	–40°C to 100°C
Storage temperature range, T_{stg}	–40°C to 150°C
Lead temperature 1,6 (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

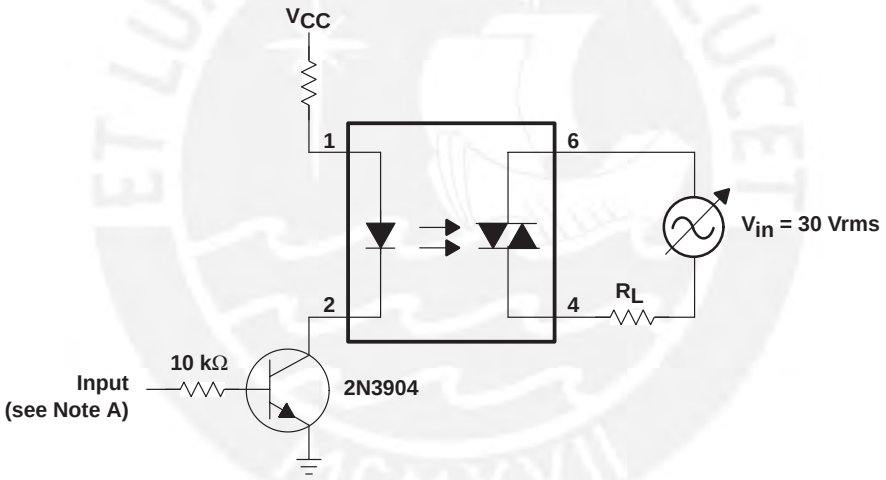
NOTES: 1. Input-to-output peak voltage is the internal device dielectric breakdown rating.
2. Derate linearly to 100°C free-air temperature at the rate of 1.33 mW/°C.
3. Derate linearly to 100°C free-air temperature at the rate of 4 mW/°C.
4. Derate linearly to 100°C free-air temperature at the rate of 4.4 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_R	Static reverse current		V_R = 3 V		0.05	100	μA
V_F	Static forward voltage		I_F = 10 mA		1.2	1.5	V
$I_{(DRM)}$	Repetitive off-state current, either direction		$V_{(DRM)}$ = 400 V, See Note 5		10	100	nA
dv/dt	Critical rate of rise of off-state voltage		See Figure 1		100		V/μs
dv/dt(c)	Critical rate of rise of commutating voltage		I_O = 15 mA, See Figure 1		0.15		V/μs
I_{FT}	Input trigger current, either direction	MOC3020	Output supply voltage = 3 V		15	30	mA
		MOC3021			8	15	
		MOC3022			5	10	
		MOC3023			3	5	
V_{TM}	Peak on-state voltage, either direction		I_{TM} = 100 mA		1.4	3	V
I_H	Holding current, either direction				100		μA

NOTE 5: Test voltage must be applied at a rate no higher than 12 V/μs.

PARAMETER MEASUREMENT INFORMATION



NOTE A. The critical rate of rise of off-state voltage, dv/dt, is measured with the input at 0 V. The frequency of V_{in} is increased until the phototriac turns on. This frequency is then used to calculate the dv/dt according to the formula:

$$dv/dt = 2\sqrt{2}\,\pi f V_{in}$$

The critical rate of rise of commutating voltage, dv/dt(c), is measured by applying occasional 5-V pulses to the input and increasing the frequency of V_{in} until the phototriac stays on (latches) after the input pulse has ceased. With no further input pulses, the frequency of V_{in} is then gradually decreased until the phototriac turns off. The frequency at which turn-off occurs may then be used to calculate the dv/dt(c) according to the formula shown above.

Figure 1. Critical Rate of Rise Test Circuit

TYPICAL CHARACTERISTICS

**EMITTING-DIODE TRIGGER CURRENT (NORMALIZED)
vs
FREE-AIR TEMPERATURE**

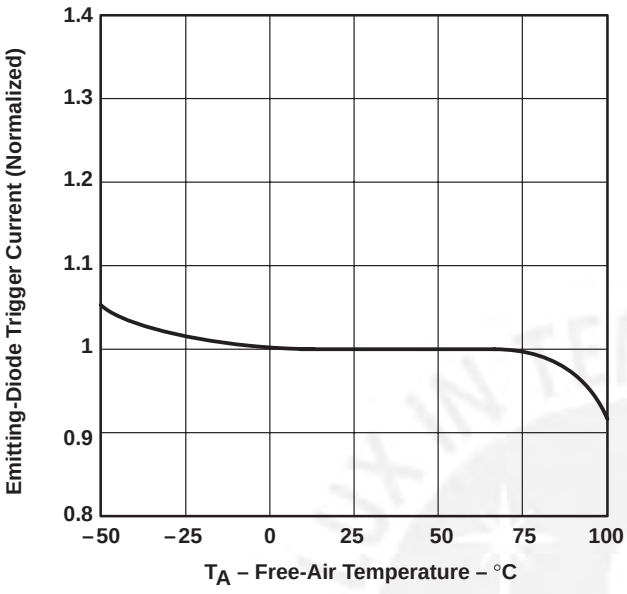


Figure 2

ON-STATE CHARACTERISTICS

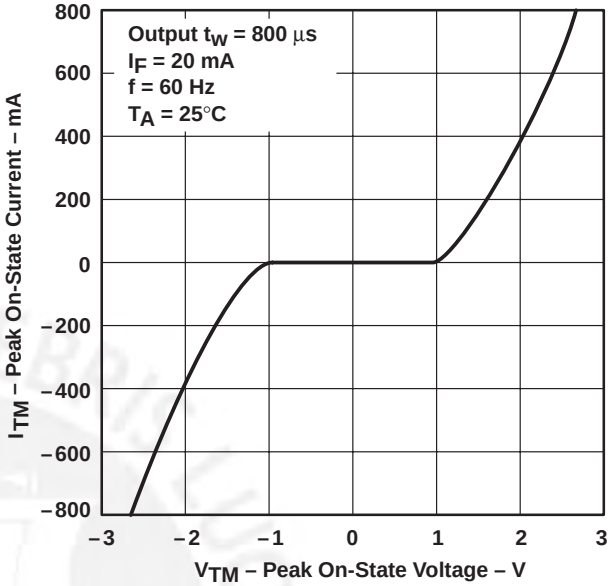


Figure 3

**NONREPETITIVE PEAK ON-STATE CURRENT
vs
PULSE DURATION**

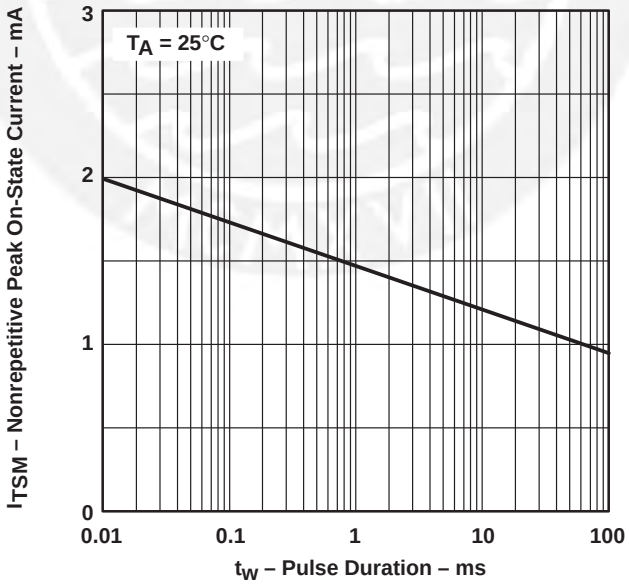


Figure 4

APPLICATIONS INFORMATION

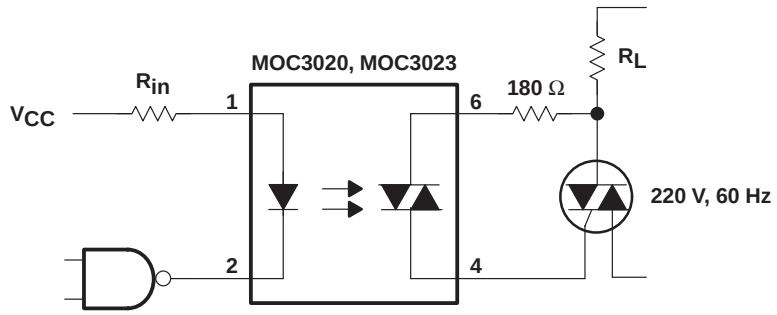


Figure 5. Resistive Load

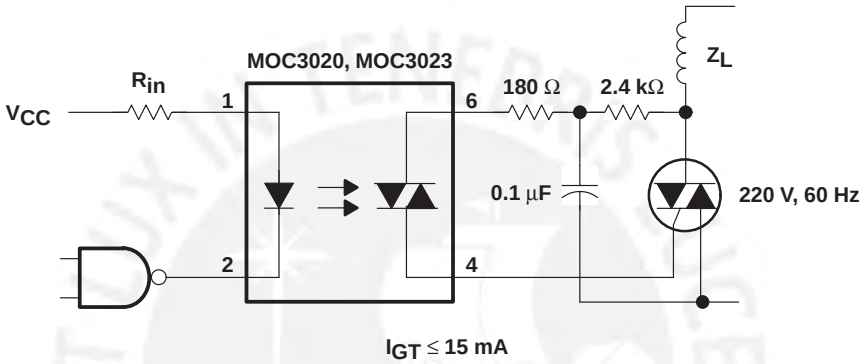


Figure 6. Inductive Load With Sensitive-Gate Triac

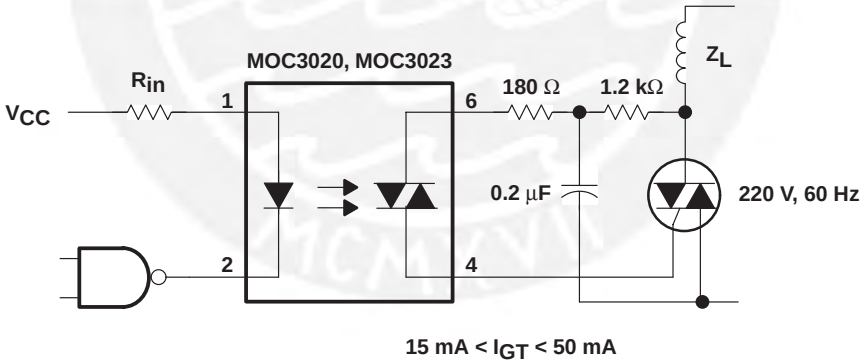
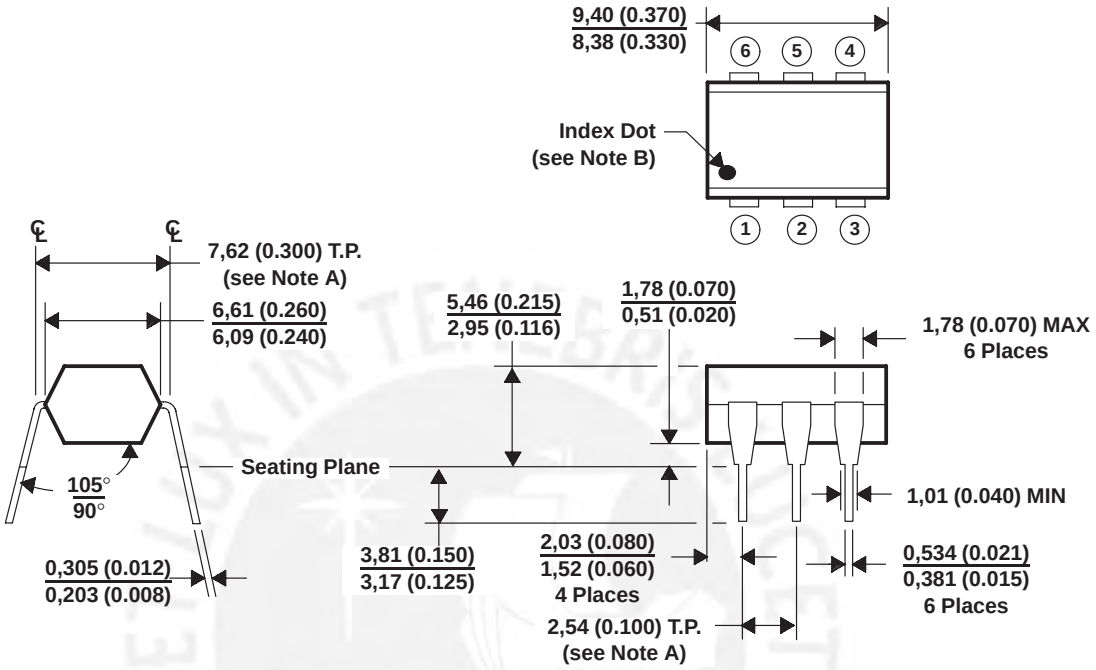


Figure 7. Inductive Load With Nonsensitive-Gate Triac

MECHANICAL INFORMATION

Each device consists of a gallium-arsenide infrared-emitting diode optically coupled to a silicon phototriac mounted on a 6-terminal lead frame encapsulated within an electrically nonconductive plastic compound. The case can withstand soldering temperature with no deformation and device performance characteristics remain stable when operated in high-humidity conditions.



NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) with maximum material condition and unit installed.
B. Pin 1 identified by index dot.
C. The dimensions given fall within JEDEC MO-001 AM dimensions.
D. All linear dimensions are given in millimeters and parenthetically given in inches.

Figure 8. Packaging Specifications

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
MOC3020	OBSOLETE	PDIP	N	6		TBD	Call TI	Call TI
MOC3021	OBSOLETE	PDIP	N	6		TBD	Call TI	Call TI
MOC3022	OBSOLETE	PDIP	N	6		TBD	Call TI	Call TI
MOC3023	OBSOLETE	PDIP	N	6		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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General Description

The DS18S20 digital thermometer provides 9-bit Celsius temperature measurements and has an alarm function with nonvolatile user-programmable upper and lower trigger points. The DS18S20 communicates over a 1-Wire bus that by definition requires only one data line (and ground) for communication with a central microprocessor. In addition, the DS18S20 can derive power directly from the data line (“parasite power”), eliminating the need for an external power supply.

Each DS18S20 has a unique 64-bit serial code, which allows multiple DS18S20s to function on the same 1-Wire bus. Thus, it is simple to use one microprocessor to control many DS18S20s distributed over a large area. Applications that can benefit from this feature include HVAC environmental controls, temperature monitoring systems inside buildings, equipment, or machinery, and process monitoring and control systems.

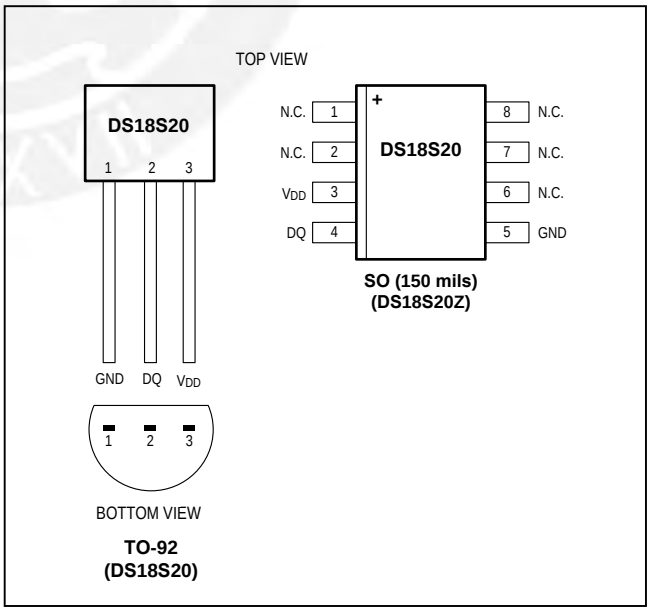
Applications

- Thermostatic Controls
- Industrial Systems
- Consumer Products
- Thermometers
- Thermally Sensitive Systems

Benefits and Features

- Unique 1-Wire® Interface Requires Only One Port Pin for Communication
- Maximize System Accuracy in Broad Range of Thermal Management Applications
  - Measures Temperatures from -55°C to +125°C (-67°F to +257°F)
  - ±0.5°C Accuracy from -10°C to +85°C
  - 9-Bit Resolution
  - No External Components Required
- Parasite Power Mode Requires Only 2 Pins for Operation (DQ and GND)
- Simplifies Distributed Temperature-Sensing Applications with Multidrop Capability
  - Each Device Has a Unique 64-Bit Serial Code Stored in On-Board ROM
- Flexible User-Definable Nonvolatile (NV) Alarm Settings with Alarm Search Command Identifies Devices with Temperatures Outside Programmed Limits
- Available in 8-Pin SO (150 mils) and 3-Pin TO-92 Packages

Pin Configurations



Ordering Information ***appears at end of data sheet.***

1-Wire is a registered trademark of Maxim Integrated Products, Inc.

19-5474; Rev 3; 4/15

Absolute Maximum Ratings

Voltage Range on Any Pin Relative to Ground ....-0.5V to +6.0V
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 5.9mW/°C above +70°C).....470.6mW
3-Pin TO-92 (derate 6.3mW/°C above +70°C).....500mW
Operating Temperature Range..... -55°C to +125°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering, 10s) .....+260°C
Soldering Temperature (reflow)
Lead(Pb)-free.....+260°C
Containing lead(Pb).....+240°C

These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC Electrical Characteristics

(V_{DD} = 3.0V to 5.5V, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	Local Power (Note 1)		+3.0		+5.5	V
Pullup Supply Voltage	V_{PU}	Parasite Power	(Note 1, 2)	+3.0		+5.5	V
		Local Power		+3.0		V_{DD}	
Thermometer Error	t_{ERR}	-10°C to +85°C	(Note 3)			±0.5	°C
		-55°C to +125°C				±2	
Input Logic-Low	V_{IL}	(Note 1, 4, 5)		-0.3		+0.8	V
Input Logic-High	V_{IH}	Local Power	(Note 1, 6)	+2.2		The lower of 5.5 or V_{DD} + 0.3	V
		Parasite Power		+3.0			
Sink Current	I_L	$V_{I/O}$ = 0.4V (Note 1)		4.0			mA
Standby Current	I_{DDS}	(Note 7, 8)			750	1000	nA
Active Current	I_{DD}	V_{DD} = 5V (Note 9)			1	1.5	mA
DQ Input Current	I_{DQ}	(Note 10)			5		µA
Drift		(Note 11)			±0.2		°C

Note 1: All voltages are referenced to ground.
Note 2: The Pullup Supply Voltage specification assumes that the pullup device is ideal, and therefore the high level of the pullup is equal to V_{PU}. In order to meet the V_{IH} spec of the DS18S20, the actual supply rail for the strong pullup transistor must include margin for the voltage drop across the transistor when it is turned on; thus: $V_{PU\_ACTUAL} = V_{PU\_IDEAL} + V_{TRANSISTOR}$.
Note 3: See typical performance curve in Figure 1.
Note 4: Logic-low voltages are specified at a sink current of 4mA.
Note 5: To guarantee a presence pulse under low voltage parasite power conditions, VILMAX may have to be reduced to as low as 0.5V.
Note 6: Logic-high voltages are specified at a source current of 1mA.
Note 7: Standby current specified up to +70°C. Standby current typically is 3µA at +125°C.
Note 8: To minimize I_{DDS}, DQ should be within the following ranges: GND ≤ DQ ≤ GND + 0.3V or V_{DD} – 0.3V ≤ DQ ≤ V_{DD}.
Note 9: Active current refers to supply current during active temperature conversions or EEPROM writes.
Note 10: DQ line is high (“high-Z” state).
Note 11: Drift data is based on a 1000-hour stress test at +125°C with V_{DD} = 5.5V.

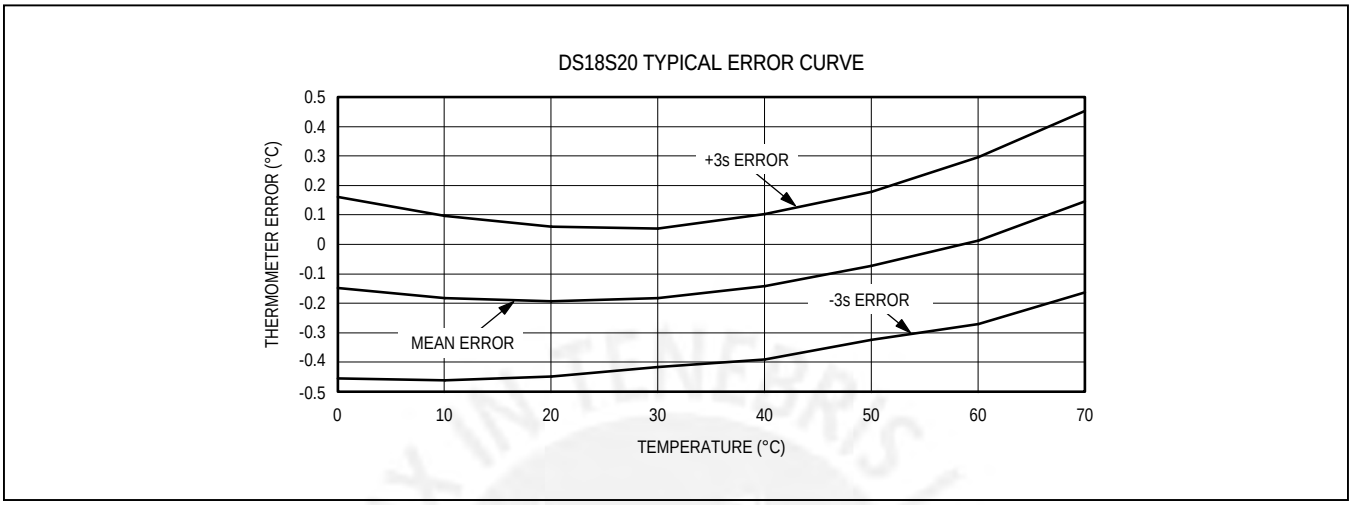


Figure 1. Typical Performance Curve

AC Electrical Characteristics—NV Memory

(V_{DD} = 3.0V to 5.5V, T_A = -55°C to +100°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
NV Write Cycle Time	t_{WR}			2	10	ms
EEPROM Writes	N_{EEWR}	-55°C to +55°C	50k			writes
EEPROM Data Retention	t_{EEDR}	-55°C to +55°C	10			years

AC Electrical Characteristics

(V_{DD} = 3.0V to 5.5V; T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Temperature Conversion Time	t_{CONV}	(Note 12)			750	ms
Time to Strong Pullup On	t_{SPON}	Start Convert T Command Issued			10	µs
Time Slot	t_{SLOT}	(Note 12)	60		120	µs
Recovery Time	t_{REC}	(Note 12)	1			µs
Write 0 Low Time	t_{LOW0}	(Note 12)	60		120	µs
Write 1 Low Time	t_{LOW1}	(Note 12)	1		15	µs
Read Data Valid	t_{RDV}	(Note 12)			15	µs
Reset Time High	t_{RSTH}	(Note 12)	480			µs
Reset Time Low	t_{RSTL}	(Note 12, 13)	480			µs
Presence-Detect High	t_{PDHIGH}	(Note 12)	15		60	µs
Presence-Detect Low	t_{PDLOW}	(Note 12)	60		240	µs
Capacitance	$C_{IN/OUT}$				25	pF

Note 12: See the timing diagrams in Figure 2.
Note 13: Under parasite power, if t_{RSTL} > 960µs, a power-on reset may occur.

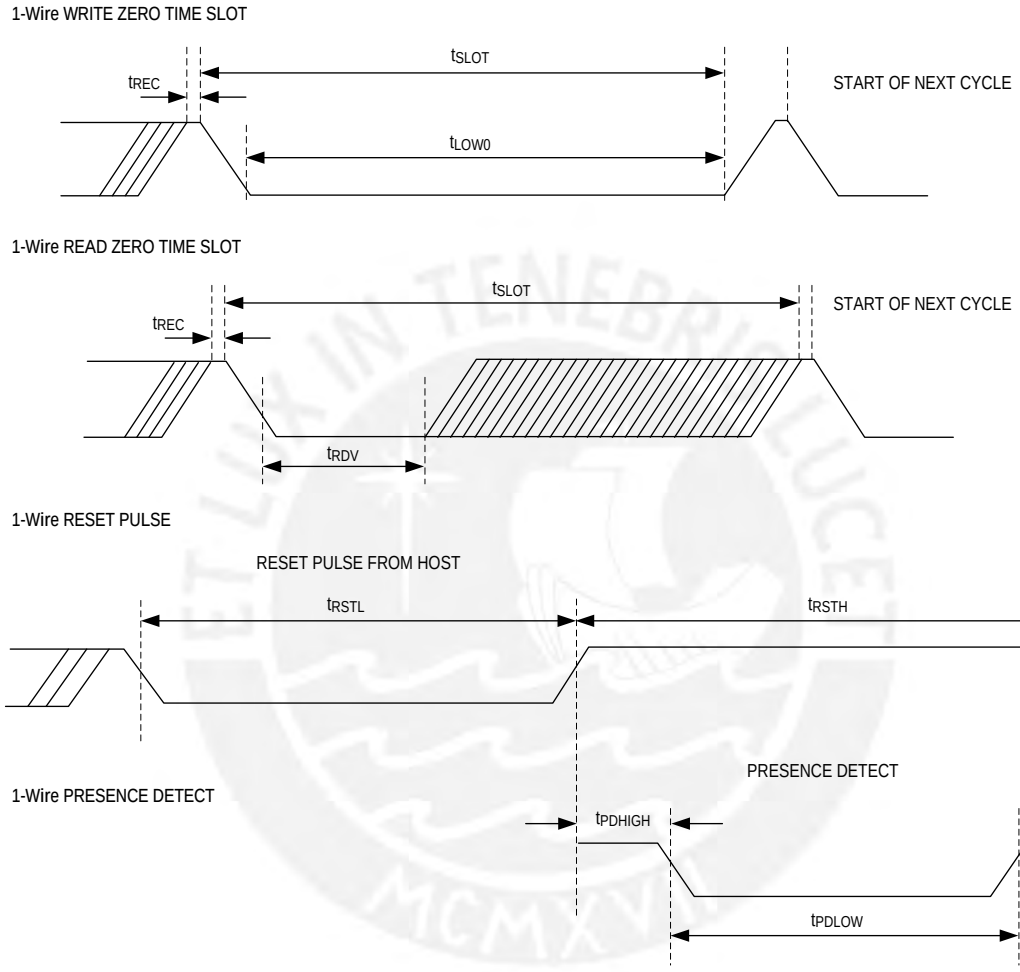


Figure 2. Timing Diagrams

Pin Description

PIN		NAME	FUNCTION
TO-92	SO		
1	5	GND	Ground
2	4	DQ	Data Input/Output. Open-drain 1-Wire interface pin. Also provides power to the device when used in parasite power mode (see the *Powering the DS18S20* section.)
3	3	V_{DD}	Optional V_{DD}. V_{DD} must be grounded for operation in parasite power mode.
—	1, 2, 6, 7, 8	N.C.	No Connection

Overview

Figure 3 shows a block diagram of the DS18S20, and pin descriptions are given in the *Pin Description* table. The 64-bit ROM stores the device's unique serial code. The scratchpad memory contains the 2-byte temperature register that stores the digital output from the temperature sensor. In addition, the scratchpad provides access to the 1-byte upper and lower alarm trigger registers (T_H and T_L). The T_H and T_L registers are nonvolatile (EEPROM), so they will retain data when the device is powered down.

The DS18S20 uses Maxim's exclusive 1-Wire bus protocol that implements bus communication using one control signal. The control line requires a weak pullup resistor since all devices are linked to the bus via a 3-state or open-drain port (the DQ pin in the case of the DS18S20). In this bus system, the microprocessor (the master device) identifies and addresses devices on the bus using each device's unique 64-bit code. Because each device has a unique code, the number of devices that can be addressed on one bus is virtually unlimited. The 1-Wire bus protocol, including detailed explanations of the commands and "time slots," is covered in the *1-Wire Bus System* section.

Another feature of the DS18S20 is the ability to operate without an external power supply. Power is instead supplied through the 1-Wire pullup resistor via the DQ pin when the bus is high. The high bus signal also charges an internal capacitor (C_{PP}), which then supplies power to the device when the bus is low. This method of deriving power from the 1-Wire bus is referred to as "parasite power." As an alternative, the DS18S20 may also be powered by an external supply on V_{DD}.

Operation—Measuring Temperature

The core functionality of the DS18S20 is its direct-to-digital temperature sensor. The temperature sensor output has 9-bit resolution, which corresponds to 0.5°C steps. The DS18S20 powers-up in a low-power idle state; to initiate a temperature measurement and A-to-D conversion, the master must issue a Convert T [44h] command. Following the conversion, the resulting thermal data is stored in the 2-byte temperature register in the scratchpad memory and the DS18S20 returns to its idle state. If the DS18S20 is powered by an external supply, the master can issue "read-time slots" (see the *1-Wire Bus System* section) after the Convert T command and the DS18S20 will respond by transmitting 0 while the temperature conversion is in progress and 1 when the conversion is done. If the DS18S20 is powered with parasite power, this notification technique cannot be used since the bus must be pulled high by a strong pullup during the entire temperature conversion. The bus requirements for parasite power are explained in detail in the *Powering The DS18S20* section.

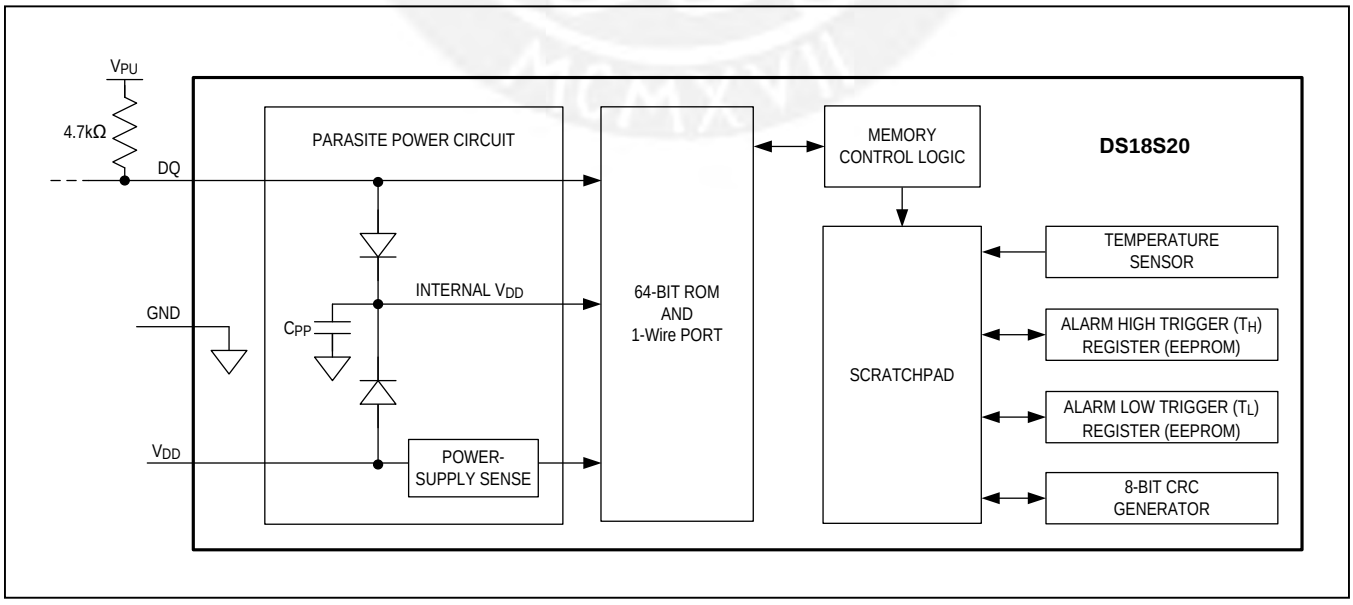


Figure 3. DS18S20 Block Diagram

The DS18S20 output data is calibrated in degrees centigrade; for Fahrenheit applications, a lookup table or conversion routine must be used. The temperature data is stored as a 16-bit sign-extended two's complement number in the temperature register (see Figure 4). The sign bits (S) indicate if the temperature is positive or negative: for positive numbers S = 0 and for negative numbers S = 1. Table 1 gives examples of digital output data and the corresponding temperature reading.

Resolutions greater than 9 bits can be calculated using the data from the temperature, COUNT REMAIN and COUNT PER °C registers in the scratchpad. Note that the COUNT PER °C register is hard-wired to 16 (10h). After reading the scratchpad, the TEMP_READ value is obtained by truncating the 0.5°C bit (bit 0) from the temperature data (see Figure 4). The extended resolution temperature can then be calculated using the following equation:

$$\text{TEMPERATURE} = \text{TEMP\_READ} - 0.25 + \frac{\text{COUNT\_PER\_C} - \text{COUNT\_REMAIN}}{\text{COUNT\_PER\_C}}$$

Operation—Alarm Signaling

After the DS18S20 performs a temperature conversion, the temperature value is compared to the user-defined two's complement alarm trigger values stored in the 1-byte T_H and T_L registers (see Figure 5). The sign bit (S) indicates if the value is positive or negative: for positive numbers S = 0 and for negative numbers S = 1. The T_H and T_L registers are nonvolatile (EEPROM) so they will retain data when the device is powered down. T_H and T_L can be accessed through bytes 2 and 3 of the scratchpad as explained in the *Memory* section.

Only bits 8 through 1 of the temperature register are used in the T_H and T_L comparison since T_H and T_L are 8-bit registers. If the measured temperature is lower than or equal to T_L or higher than T_H, an alarm condition exists and an alarm flag is set inside the DS18S20. This flag is updated after every temperature measurement; therefore, if the alarm condition goes away, the flag will be turned off after the next temperature conversion.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LS BYTE	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}
	BIT 15	**BIT 14**	**BIT 13**	**BIT 12**	**BIT 11**	**BIT 10**	**BIT 9**	**BIT 8**
MS BYTE	S	S	S	S	S	S	S	S

S = SIGN

Figure 4. Temperature Register Format

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
S	2^6	2^5	2^5	2^5	2^2	2^1	2^0

Figure 5. T_H and T_L Register Format

Table 1. Temperature/Data Relationship

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	DIGITAL OUTPUT (HEX)
+85.0*	0000 0000 1010 1010	00AAh
+25.0	0000 0000 0011 0010	0032h
+0.5	0000 0000 0000 0001	0001h
0	0000 0000 0000 0000	0000h
-0.5	1111 1111 1111 1111	FFFFh
-25.0	1111 1111 1100 1110	FFCEh
-55.0	1111 1111 1001 0010	FF92h

**The power-on reset value of the temperature register is +85°C.*

The master device can check the alarm flag status of all DS18S20s on the bus by issuing an Alarm Search [ECh] command. Any DS18S20s with a set alarm flag will respond to the command, so the master can determine exactly which DS18S20s have experienced an alarm condition. If an alarm condition exists and the T_H or T_L settings have changed, another temperature conversion should be done to validate the alarm condition.

Powering The DS18S20

The DS18S20 can be powered by an external supply on the V_{DD} pin, or it can operate in "parasite power" mode, which allows the DS18S20 to function without a local external supply. Parasite power is very useful for applications that require remote temperature sensing or those with space constraints. Figure 3 shows the DS18S20's parasite-power control circuitry, which "steals" power from the 1-Wire bus via the DQ pin when the bus is high. The stolen charge powers the DS18S20 while the bus is high, and some of the charge is stored on the parasite power capacitor (C_{PP}) to provide power when the bus is low. When the DS18S20 is used in parasite power mode, the V_{DD} pin must be connected to ground.

In parasite power mode, the 1-Wire bus and C_{PP} can provide sufficient current to the DS18S20 for most operations as long as the specified timing and voltage requirements are met (see the *DC Electrical Characteristics* and the *AC Electrical Characteristics*). However, when the DS18S20 is performing temperature conversions or copying data from the scratchpad memory to EEPROM, the operating current can be as high as 1.5mA. This current can cause an unacceptable voltage drop across the weak 1-Wire pullup resistor and is more current than can be supplied by C_{PP}. To assure that the DS18S20 has sufficient supply current, it is necessary to provide a strong pullup on the 1-Wire bus whenever temperature conversions are taking place or data is being copied from the scratchpad to EEPROM. This can be accomplished by using a MOSFET to pull the bus directly to the rail as shown in Figure 6. The 1-Wire bus must be switched to the strong pullup within 10µs (max) after a Convert T [44h] or Copy Scratchpad [48h] command is issued, and the bus must be held high by the pullup for the duration of the conversion (t_{CONV}) or data transfer (t_{WR} = 10ms). No other activity can take place on the 1-Wire bus while the pullup is enabled.

The DS18S20 can also be powered by the conventional method of connecting an external power supply to the V_{DD} pin, as shown in Figure 7. The advantage of this method is that the MOSFET pullup is not required, and the 1-Wire bus is free to carry other traffic during the temperature conversion time.

The use of parasite power is not recommended for temperatures above 100°C since the DS18S20 may not be able to sustain communications due to the higher leakage currents that can exist at these temperatures. For applications in which such temperatures are likely, it is strongly recommended that the DS18S20 be powered by an external power supply.

In some situations the bus master may not know whether the DS18S20s on the bus are parasite powered or powered by external supplies. The master needs this information to determine if the strong bus pullup should be used during temperature conversions. To get this information, the master can issue a Skip ROM [CCh] command followed by a Read Power Supply [B4h] command followed by a "read-time slot". During the read-time slot, parasite powered DS18S20s will pull the bus low, and externally powered DS18S20s will let the bus remain high. If the bus is pulled low, the master knows that it must supply the strong pullup on the 1-Wire bus during temperature conversions.

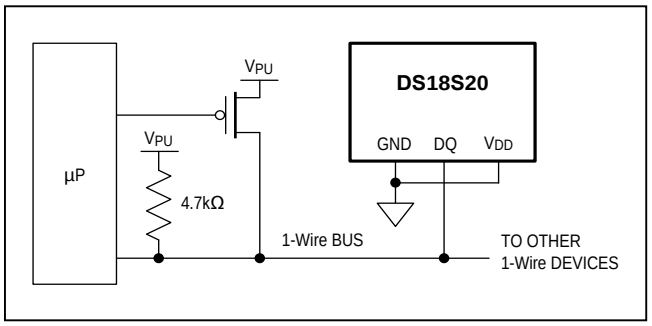


Figure 6. Supplying the Parasite-Powered DS18S20 During Temperature Conversions

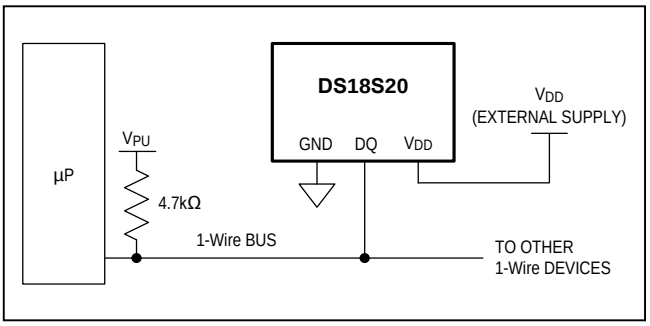


Figure 7. Powering the DS18S20 with an External Supply

64-Bit Lasered ROM Code

Each DS18S20 contains a unique 64-bit code (see Figure 8) stored in ROM. The least significant 8 bits of the ROM code contain the DS18S20's 1-Wire family code: 10h. The next 48 bits contain a unique serial number. The most significant 8 bits contain a cyclic redundancy check (CRC) byte that is calculated from the first 56 bits of the ROM code. A detailed explanation of the CRC bits is provided in the *CRC Generation* section. The 64-bit ROM code and associated ROM function control logic allow the DS18S20 to operate as a 1-Wire device using the protocol detailed in the *1-Wire Bus System* section.

Memory

The DS18S20's memory is organized as shown in Figure 9. The memory consists of an SRAM scratchpad with nonvolatile EEPROM storage for the high and low alarm trigger registers (T_H and T_L). Note that if the DS18S20 alarm function is not used, the T_H and T_L registers can serve as general-purpose memory. All memory commands are described in detail in the *DS18S20 Function Commands* section.

Byte 0 and byte 1 of the scratchpad contain the LSB and the MSB of the temperature register, respectively. These bytes are read-only. Bytes 2 and 3 provide access to T_H and T_L registers. Bytes 4 and 5 are reserved for internal use by the device and cannot be overwritten; these bytes will return all 1s when read. Bytes 6 and 7 contain the COUNT REMAIN and COUNT PER ºC registers, which can be used to calculate extended resolution results as explained in the *Operation—Measuring Temperature* section.

Byte 8 of the scratchpad is read-only and contains the CRC code for bytes 0 through 7 of the scratchpad. The DS18S20 generates this CRC using the method described in the *CRC Generation* section.

Data is written to bytes 2 and 3 of the scratchpad using the Write Scratchpad [4Eh] command; the data must be transmitted to the DS18S20 starting with the least significant bit of byte 2. To verify data integrity, the scratchpad can be read (using the Read Scratchpad [BEh] command) after the data is written. When reading the scratchpad, data is transferred over the 1-Wire bus starting with the least significant bit of byte 0. To transfer the T_H and T_L data from the scratchpad to EEPROM, the master must issue the Copy Scratchpad [48h] command.

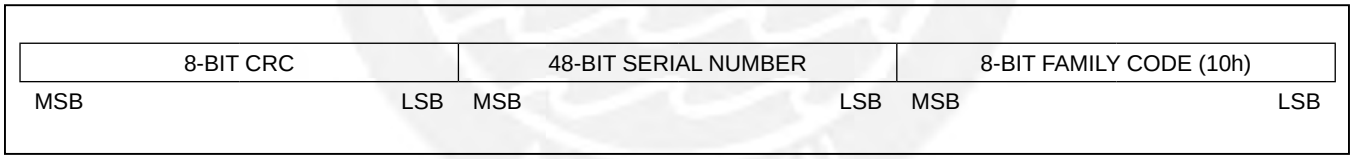


Figure 8. 64-Bit Lasered ROM Code

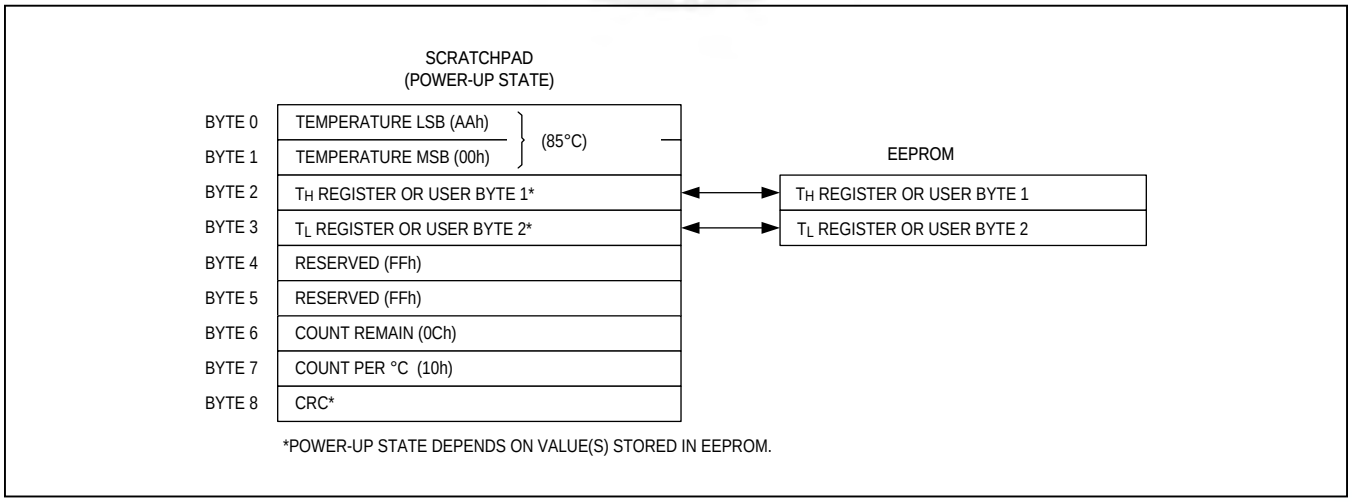


Figure 9. DS18S20 Memory Map

Data in the EEPROM registers is retained when the device is powered down; at power-up the EEPROM data is reloaded into the corresponding scratchpad locations. Data can also be reloaded from EEPROM to the scratchpad at any time using the Recall E^2 [B8h] command. The master can issue “read-time slots” (see the *1-Wire Bus System* section) following the Recall E^2 command and the DS18S20 will indicate the status of the recall by transmitting 0 while the recall is in progress and 1 when the recall is done.

CRC Generation

CRC bytes are provided as part of the DS18S20’s 64-bit ROM code and in the 9th byte of the scratchpad memory. The ROM code CRC is calculated from the first 56 bits of the ROM code and is contained in the most significant byte of the ROM. The scratchpad CRC is calculated from the data stored in the scratchpad, and therefore it changes when the data in the scratchpad changes. The CRCs provide the bus master with a method of data validation when data is read from the DS18S20. To verify that data has been read correctly, the bus master must re-calculate the CRC from the received data and then compare this value to either the ROM code CRC (for ROM reads) or to the scratchpad CRC (for scratchpad reads). If the calculated CRC matches the read CRC, the data has been received error free. The comparison of CRC values and the decision to continue with an operation are determined entirely by the bus master. There is no circuitry inside the DS18S20 that prevents a command sequence from proceeding if the DS18S20 CRC (ROM or scratchpad) does not match the value generated by the bus master.

The equivalent polynomial function of the CRC (ROM or scratchpad) is:

$$CRC = X^8 + X^5 + X^4 + 1$$

The bus master can re-calculate the CRC and compare it to the CRC values from the DS18S20 using the polynomial generator shown in Figure 10. This circuit consists of a shift register and XOR gates, and the shift register bits are initialized to 0. Starting with the least significant bit of the ROM code or the least significant bit of byte 0 in the scratchpad, one bit at a time should shifted into the shift register. After shifting in the 56th bit from the ROM or the most significant bit of byte 7 from the scratchpad, the polynomial generator will contain the re-calculated CRC. Next, the 8-bit ROM code or scratchpad CRC from the DS18S20 must be shifted into the circuit. At this point, if the re-calculated CRC was correct, the shift register will contain all 0s. Additional information about the Maxim 1-Wire cyclic redundancy check is available in *Application Note 27: Understanding and Using Cyclic Redundancy Checks with Maxim ¡Button Products*.

1-Wire Bus System

The 1-Wire bus system uses a single bus master to control one or more slave devices. The DS18S20 is always a slave. When there is only one slave on the bus, the system is referred to as a “single-drop” system; the system is “multidrop” if there are multiple slaves on the bus.

All data and commands are transmitted least significant bit first over the 1-Wire bus.

The following discussion of the 1-Wire bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing).

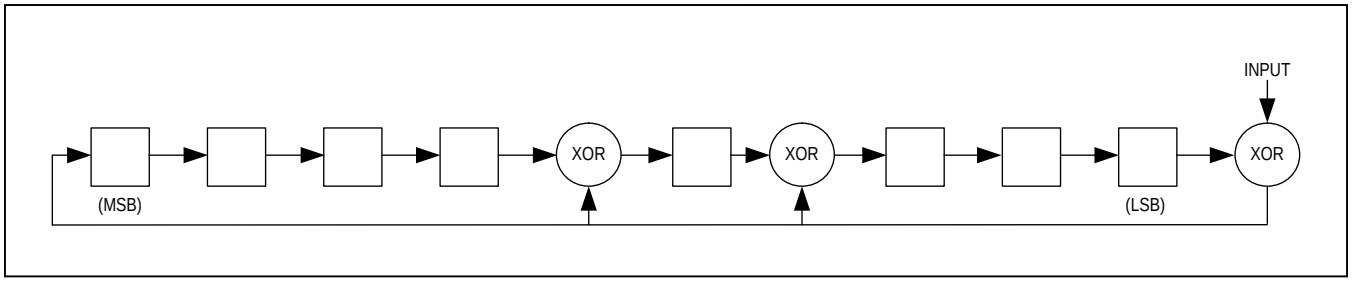


Figure 10. CRC Generator

Hardware Configuration

The 1-Wire bus has by definition only a single data line. Each device (master or slave) interfaces to the data line via an open drain or 3-state port. This allows each device to "release" the data line when the device is not transmitting data so the bus is available for use by another device. The 1-Wire port of the DS18S20 (the DQ pin) is open drain with an internal circuit equivalent to that shown in Figure 11.

The 1-Wire bus requires an external pullup resistor of approximately 5kΩ; thus, the idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. Infinite recovery time can occur between bits so long as the 1-Wire bus is in the inactive (high) state during the recovery period. If the bus is held low for more than 480µs, all components on the bus will be reset.

Transaction Sequence

The transaction sequence for accessing the DS18S20 is as follows:

Step 1. Initialization

Step 2. ROM Command (followed by any required data exchange)

Step 3. DS18S20 Function Command (followed by any required data exchange)

It is very important to follow this sequence every time the DS18S20 is accessed, as the DS18S20 will not respond if any steps in the sequence are missing or out of order. Exceptions to this rule are the Search ROM [F0h] and Alarm Search [ECh] commands. After issuing either of these ROM commands, the master must return to Step 1 in the sequence.

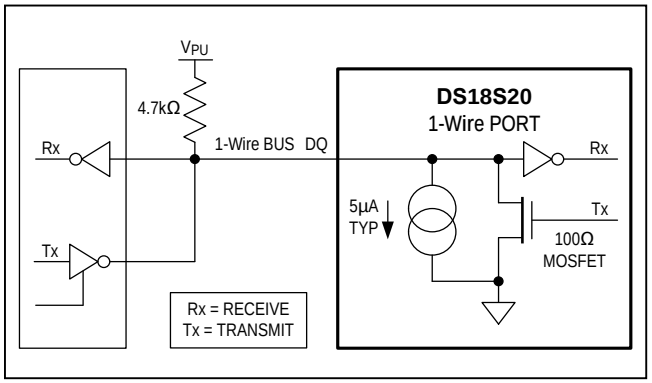


Figure 11. Hardware Configuration

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that slave devices (such as the DS18S20) are on the bus and are ready to operate. Timing for the reset and presence pulses is detailed in the *1-Wire Signaling* section.

ROM Commands

After the bus master has detected a presence pulse, it can issue a ROM command. These commands operate on the unique 64-bit ROM codes of each slave device and allow the master to single out a specific device if many are present on the 1-Wire bus. These commands also allow the master to determine how many and what types of devices are present on the bus or if any device has experienced an alarm condition. There are five ROM commands, and each command is 8 bits long. The master device must issue an appropriate ROM command before issuing a DS18S20 function command. A flowchart for operation of the ROM commands is shown in Figure 16.

Search Rom [F0h]

When a system is initially powered up, the master must identify the ROM codes of all slave devices on the bus, which allows the master to determine the number of slaves and their device types. The master learns the ROM codes through a process of elimination that requires the master to perform a Search ROM cycle (i.e., Search ROM command followed by data exchange) as many times as necessary to identify all of the slave devices. If there is only one slave on the bus, the simpler Read ROM command (see below) can be used in place of the Search ROM process. For a detailed explanation of the Search ROM procedure, refer to the *iButton® Book of Standards* at **www.maximintegrated.com/ibuttonbook**. After every Search ROM cycle, the bus master must return to Step 1 (Initialization) in the transaction sequence.

Read ROM [33h]

This command can only be used when there is one slave on the bus. It allows the bus master to read the slave's 64-bit ROM code without using the Search ROM procedure. If this command is used when there is more than one slave present on the bus, a data collision will occur when all the slaves attempt to respond at the same time.

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Match ROM [55h]

The match ROM command followed by a 64-bit ROM code sequence allows the bus master to address a specific slave device on a multidrop or single-drop bus. Only the slave that exactly matches the 64-bit ROM code sequence will respond to the function command issued by the master; all other slaves on the bus will wait for a reset pulse.

Skip ROM [CCh]

The master can use this command to address all devices on the bus simultaneously without sending out any ROM code information. For example, the master can make all DS18S20s on the bus perform simultaneous temperature conversions by issuing a Skip ROM command followed by a Convert T [44h] command.

Note that the Read Scratchpad [BEh] command can follow the Skip ROM command only if there is a single slave device on the bus. In this case, time is saved by allowing the master to read from the slave without sending the device's 64-bit ROM code. A Skip ROM command followed by a Read Scratchpad command will cause a data collision on the bus if there is more than one slave since multiple devices will attempt to transmit data simultaneously.

Alarm Search [ECh]

The operation of this command is identical to the operation of the Search ROM command except that only slaves with a set alarm flag will respond. This command allows the master device to determine if any DS18S20s experienced an alarm condition during the most recent temperature conversion. After every Alarm Search cycle (i.e., Alarm Search command followed by data exchange), the bus master must return to Step 1 (Initialization) in the transaction sequence. See the *Operation—Alarm Signaling* section for an explanation of alarm flag operation.

DS18S20 Function Commands

After the bus master has used a ROM command to address the DS18S20 with which it wishes to communicate, the master can issue one of the DS18S20 function commands. These commands allow the master to write to and read from the DS18S20's scratchpad memory, initiate temperature conversions and determine the power supply mode. The DS18S20 function commands, which are described below, are summarized in Table 2 and illustrated by the flowchart in Figure 17.

Table 2. DS18S20 Function Command Set

COMMAND	DESCRIPTION	PROTOCOL	1-Wire BUS ACTIVITY AFTER COMMAND IS ISSUED	NOTES
TEMPERATURE CONVERSION COMMANDS				
Convert T	Initiates temperature conversion.	44h	DS18S20 transmits conversion status to master (not applicable for parasite-powered DS18S20s).	1
MEMORY COMMANDS				
Read Scratchpad	Reads the entire scratchpad including the CRC byte.	BEh	DS18S20 transmits up to 9 data bytes to master.	2
Write Scratchpad	Writes data into scratchpad bytes 2 and 3 (T_H and T_L).	4Eh	Master transmits 2 data bytes to DS18S20.	3
Copy Scratchpad	Copies T_H and T_L data from the scratchpad to EEPROM.	48h	None	1
Recall E^2	Recalls T_H and T_L data from EEPROM to the scratchpad.	B8h	DS18S20 transmits recall status to master.	
Read Power Supply	Signals DS18S20 power supply mode to the master.	B4h	DS18S20 transmits supply status to master.	

Note 1: For parasite-powered DS18S20s, the master must enable a strong pullup on the 1-Wire bus during temperature conversions and copies from the scratchpad to EEPROM. No other bus activity may take place during this time.
Note 2: The master can interrupt the transmission of data at any time by issuing a reset.
Note 3: Both bytes must be written before a reset is issued.

Convert T [44h]

This command initiates a single temperature conversion. Following the conversion, the resulting thermal data is stored in the 2-byte temperature register in the scratchpad memory and the DS18S20 returns to its low-power idle state. If the device is being used in parasite power mode, within 10µs (max) after this command is issued the master must enable a strong pullup on the 1-Wire bus for the duration of the conversion (t_{CONV}) as described in the *Powering The DS18S20* section. If the DS18S20 is powered by an external supply, the master can issue read-time slots after the Convert T command and the DS18S20 will respond by transmitting 0 while the temperature conversion is in progress and 1 when the conversion is done. In parasite power mode this notification technique cannot be used since the bus is pulled high by the strong pullup during the conversion.

Write Scratchpad [4Eh]

This command allows the master to write 2 bytes of data to the DS18S20's scratchpad. The first byte is written into the T_H register (byte 2 of the scratchpad), and the second byte is written into the T_L register (byte 3 of the scratchpad). Data must be transmitted least significant bit first. Both bytes MUST be written before the master issues a reset, or the data may be corrupted.

Read Scratchpad [BEh]

This command allows the master to read the contents of the scratchpad. The data transfer starts with the least significant bit of byte 0 and continues through the scratchpad until the 9th byte (byte 8 – CRC) is read. The master may issue a reset to terminate reading at any time if only part of the scratchpad data is needed.

Copy Scratchpad [48h]

This command copies the contents of the scratchpad T_H and T_L registers (bytes 2 and 3) to EEPROM. If the device is being used in parasite power mode, within 10µs (max) after this command is issued the master must enable a strong pullup on the 1-Wire bus for at least 10ms as described in the *Powering The DS18S20* section.

Recall E^2 [B8h]

This command recalls the alarm trigger values (T_H and T_L) from EEPROM and places the data in bytes 2 and 3, respectively, in the scratchpad memory. The master device can issue read-time slots following the Recall E^2 command and the DS18S20 will indicate the status of the recall by transmitting 0 while the recall is in progress and 1 when the recall is done. The recall operation happens automatically at power-up, so valid data is available in the scratchpad as soon as power is applied to the device.

Read Power Supply [B4h]

The master device issues this command followed by a read-time slot to determine if any DS18S20s on the bus are using parasite power. During the read-time slot, parasite powered DS18S20s will pull the bus low, and externally powered DS18S20s will let the bus remain high. See the *Powering The DS18S20* section for usage information for this command.

1-Wire Signaling

The DS18S20 uses a strict 1-Wire communication protocol to ensure data integrity. Several signal types are defined by this protocol: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. All these signals, with the exception of the presence pulse, are initiated by the bus master.

Initialization Procedure—Reset And Presence Pulses

All communication with the DS18S20 begins with an initialization sequence that consists of a reset pulse from the master followed by a presence pulse from the DS18S20. This is illustrated in Figure 12. When the DS18S20 sends the presence pulse in response to the reset, it is indicating to the master that it is on the bus and ready to operate.

During the initialization sequence the bus master transmits (Tx) the reset pulse by pulling the 1-Wire bus low for a minimum of 480µs. The bus master then releases the bus and goes into receive mode (Rx). When the bus is released, the 5kΩ pullup resistor pulls the 1-Wire bus high. When the DS18S20 detects this rising edge, it waits 15µs to 60µs and then transmits a presence pulse by pulling the 1-Wire bus low for 60µs to 240µs.

Read/Write Time Slots

The bus master writes data to the DS18S20 during write time slots and reads data from the DS18S20 during read-time slots. One bit of data is transmitted over the 1-Wire bus per time slot.

Write Time Slots

There are two types of write time slots: “Write 1” time slots and “Write 0” time slots. The bus master uses a Write 1 time slot to write a logic 1 to the DS18S20 and a Write 0 time slot to write a logic 0 to the DS18S20. All write time slots must be a minimum of 60µs in duration with a minimum of a 1µs recovery time between individual write slots. Both types of write time slots are initiated by the master pulling the 1-Wire bus low (see Figure 13).

To generate a Write 1 time slot, after pulling the 1-Wire bus low, the bus master must release the 1-Wire bus within 15µs. When the bus is released, the 5kΩ pullup resistor will pull the bus high. To generate a Write 0 time slot, after pulling the 1-Wire bus low, the bus master must continue to hold the bus low for the duration of the time slot (at least 60µs). The DS18S20 samples the 1-Wire bus during a window that lasts from 15µs to 60µs after the master initiates the write time slot. If the bus is high during the sampling window, a 1 is written to the DS18S20. If the line is low, a 0 is written to the DS18S20.

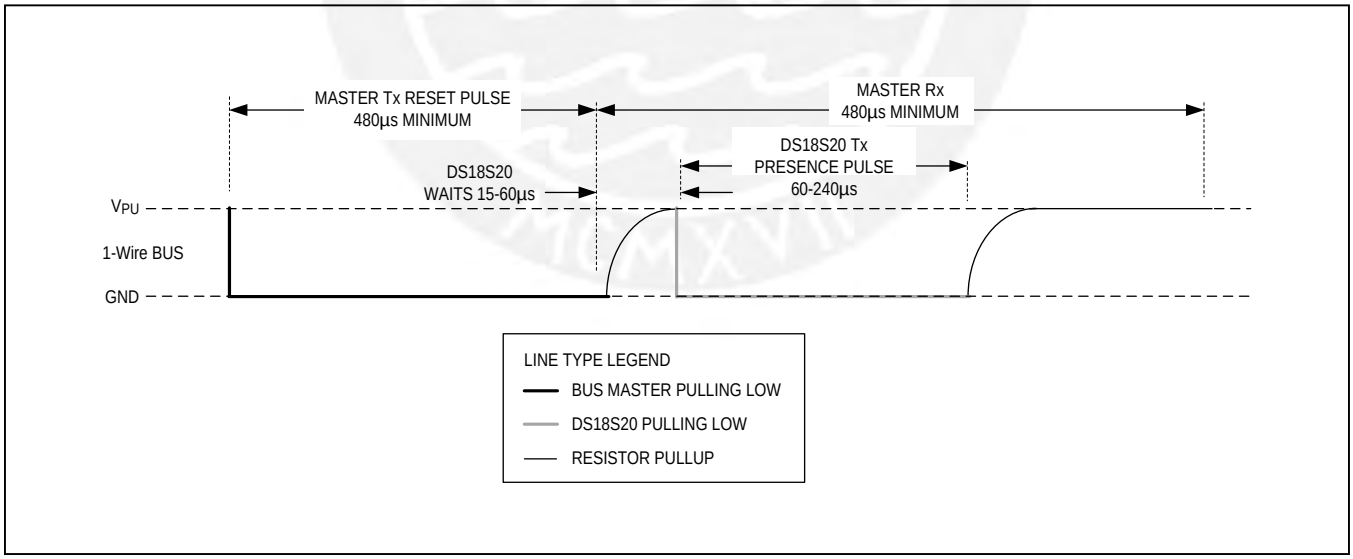


Figure 12. Initialization Timing

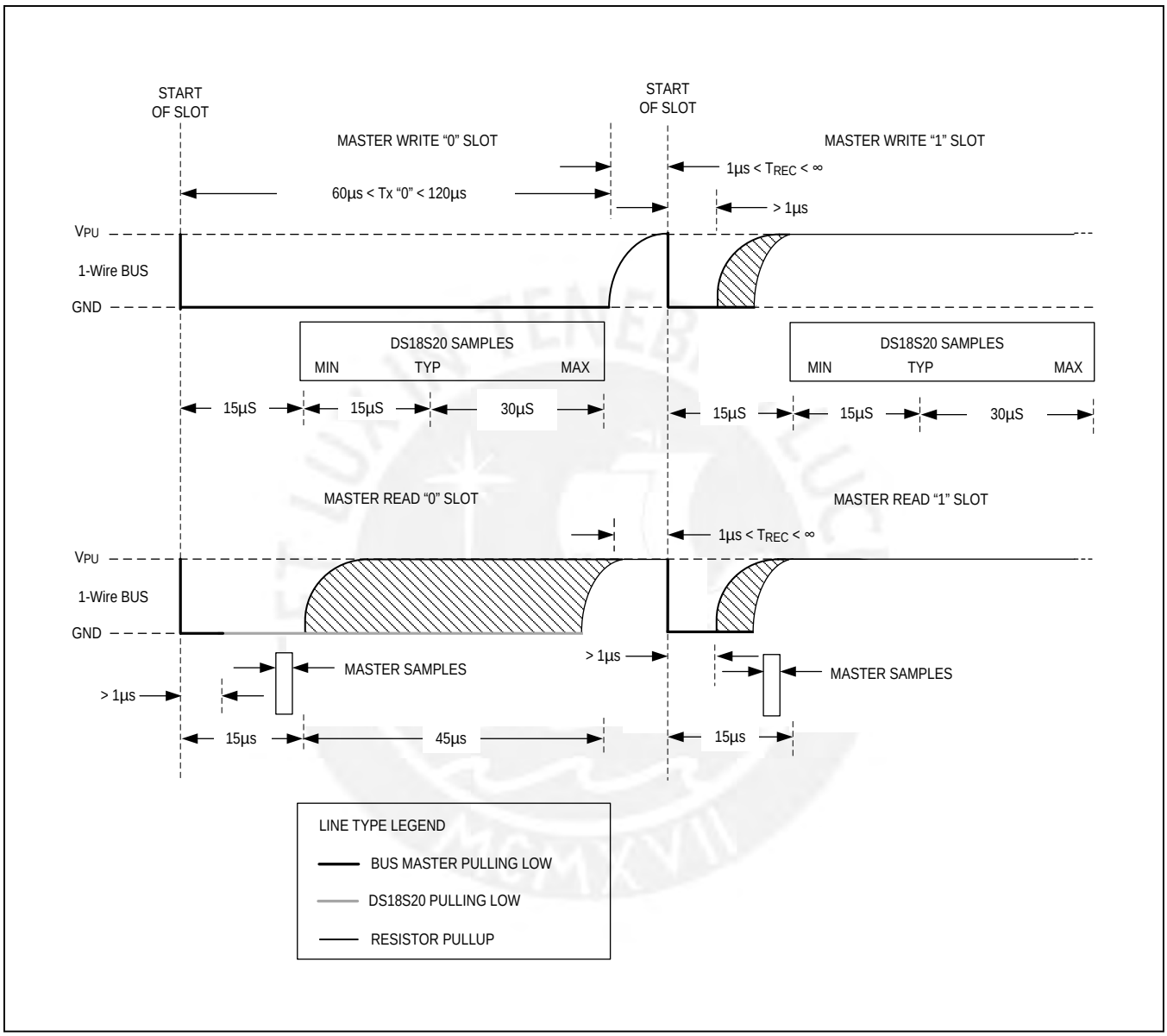


Figure 13. Read/Write Time Slot Timing Diagram

Read-Time Slots

The DS18S20 can only transmit data to the master when the master issues read-time slots. Therefore, the master must generate read-time slots immediately after issuing a Read Scratchpad [BEh] or Read Power Supply [B4h] command, so that the DS18S20 can provide the requested data. In addition, the master can generate read-time slots after issuing Convert T [44h] or Recall E^2 [B8h] commands to find out the status of the operation as explained in the *DS18S20 Function Commands* section.

All read-time slots must be a minimum of 60µs in duration with a minimum of a 1µs recovery time between slots. A read-time slot is initiated by the master device pulling the 1-Wire bus low for a minimum of 1µs and then releasing the bus (see Figure 13). After the master initiates the read-time slot, the DS18S20 will begin transmitting a 1 or 0 on bus. The DS18S20 transmits a 1 by leaving the bus high and transmits a 0 by pulling the bus low. When transmitting a 0, the DS18S20 will release the bus by the end of the time slot, and the bus will be pulled back to its high idle state by the pullup resister. Output data from the DS18S20 is valid for 15µs after the falling edge that initiated the read-time slot. Therefore, the master must release the bus and then sample the bus state within 15µs from the start of the slot.

Figure 14 illustrates that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15µs for a read-time slot. Figure 15 shows that system timing margin is maximized by keeping T_{INIT} and T_{RC} as short as possible and by locating the master sample time during read-time slots towards the end of the 15µs period.

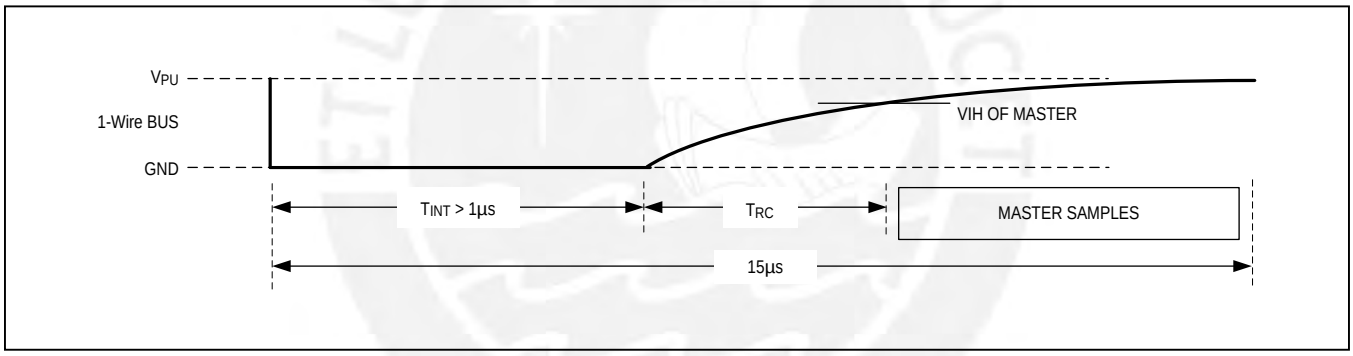


Figure 14. Detailed Master Read 1 Timing

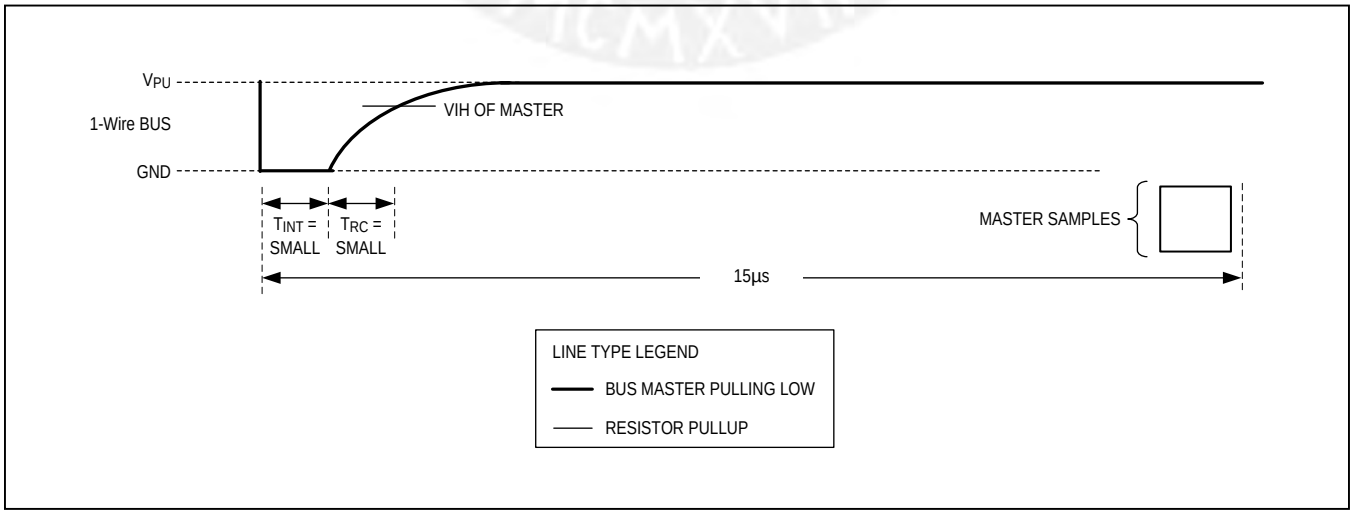


Figure 15. Recommended Master Read 1 Timing

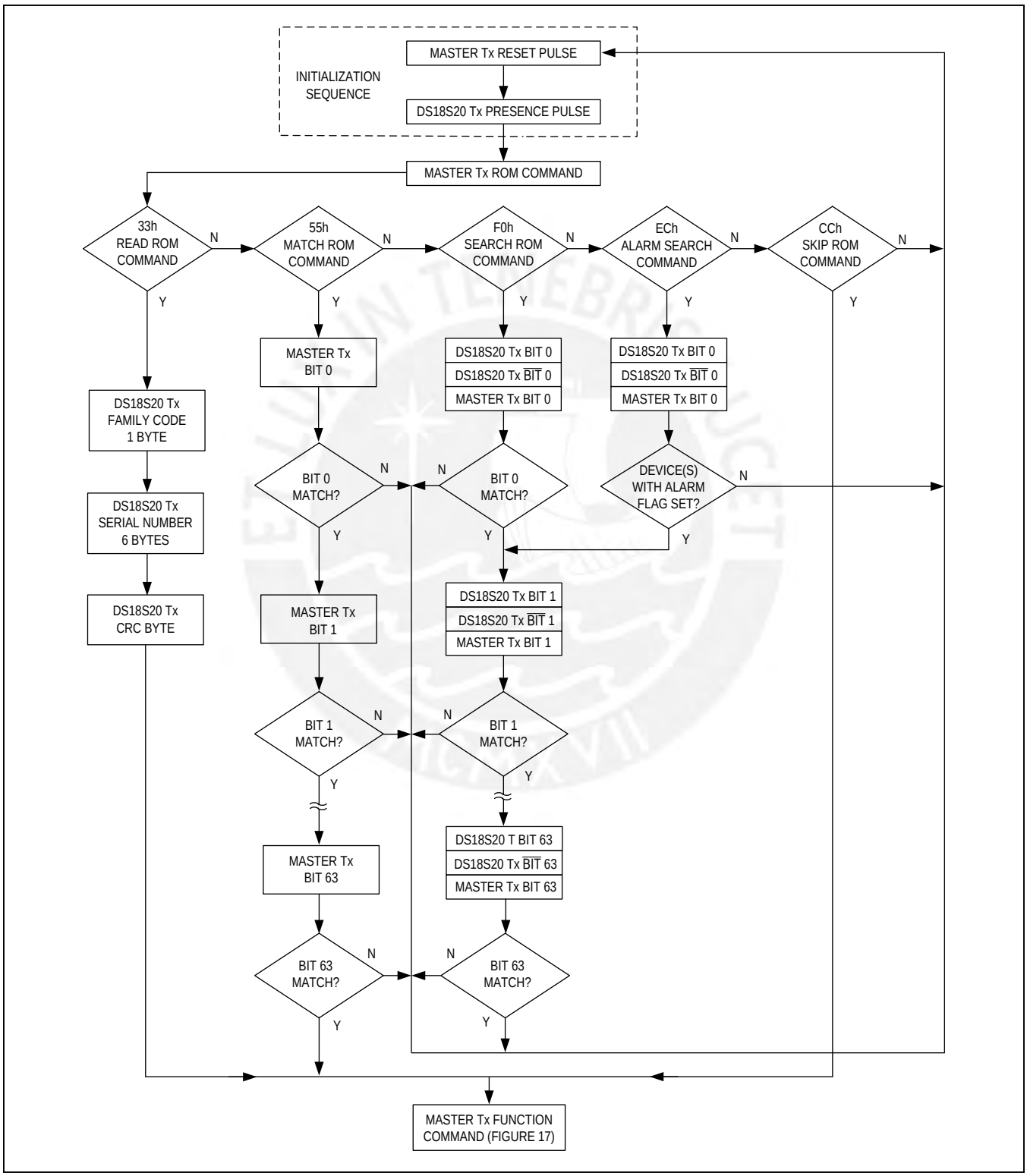


Figure 16. ROM Commands Flowchart

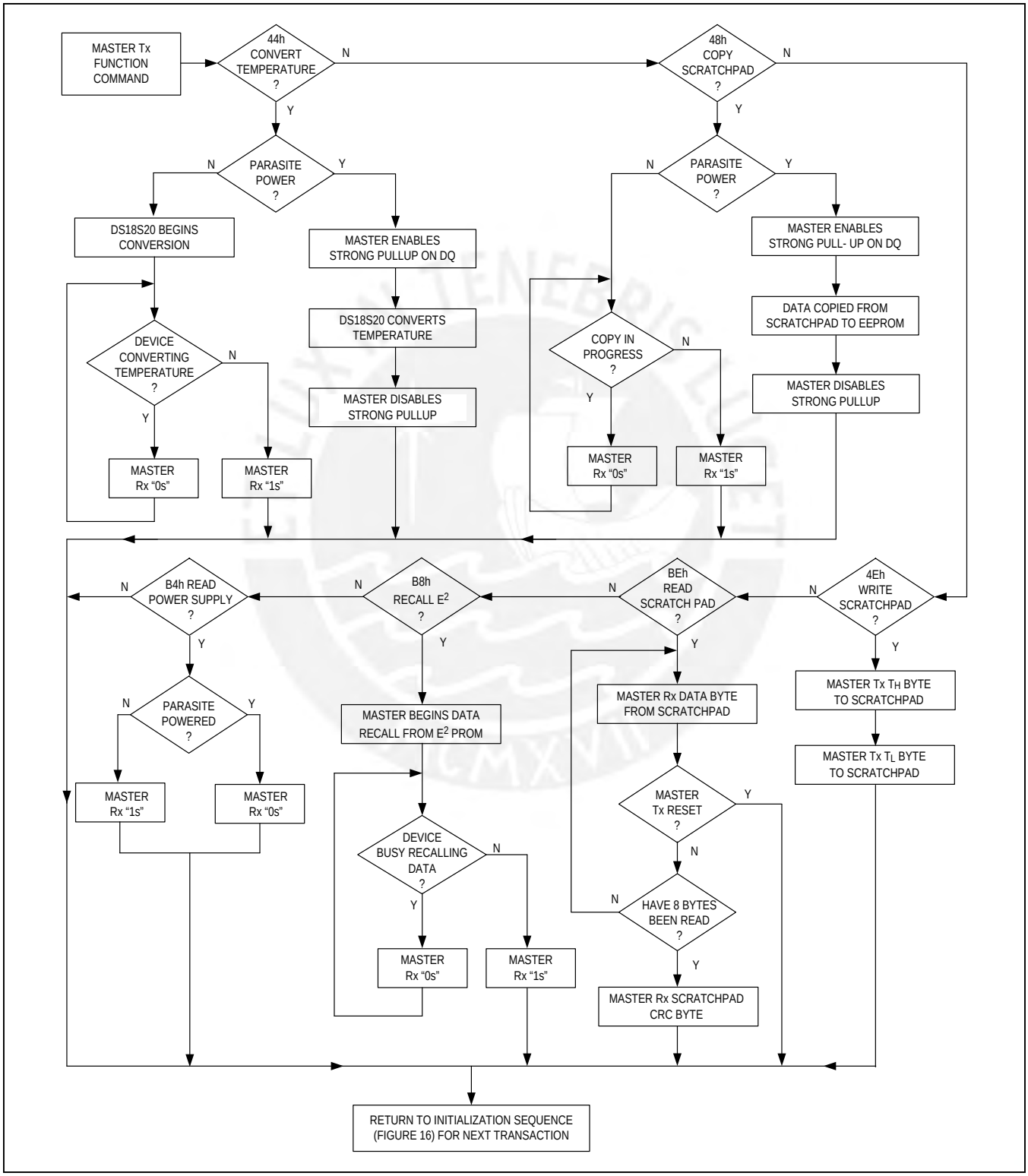


Figure 17. DS18S20 Function Commands Flowchart

Ds18S20 Operation Example 1

In this example there are multiple DS18S20s on the bus and they are using parasite power. The bus master initiates a temperature conversion in a specific DS18S20 and then reads its scratchpad and recalculates the CRC to verify the data.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
Tx	Reset	Master issues reset pulse.
Rx	Presence	DS18S20s respond with presence pulse.
Tx	55h	Master issues Match ROM command.
Tx	64-bit ROM code	Master sends DS18S20 ROM code.
Tx	44h	Master issues Convert T command.
Tx	DQ line held high by strong pullup	Master applies strong pullup to DQ for the duration of the conversion (t_{CONV}).
Tx	Reset	Master issues reset pulse.
Rx	Presence	DS18S20s respond with presence pulse.
Tx	55h	Master issues Match ROM command.
Tx	64-bit ROM code	Master sends DS18S20 ROM code.
Tx	BEh	Master issues Read Scratchpad command.
Rx	9 data bytes	Master reads entire scratchpad including CRC. The master then recalculates the CRC of the first eight data bytes from the scratchpad and compares the calculated CRC with the read CRC (byte 9). If they match, the master continues; if not, the read operation is repeated.

DS18S20 Operation Example 2

In this example there is only one DS18S20 on the bus and it is using parasite power. The master writes to the T_H and T_L registers in the DS18S20 scratchpad and then reads the scratchpad and recalculates the CRC to verify the data. The master then copies the scratchpad contents to EEPROM.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
Tx	Reset	Master issues reset pulse.
Rx	Presence	DS18S20 responds with presence pulse.
Tx	CCh	Master issues Skip ROM command.
Tx	4Eh	Master issues Write Scratchpad command.
Tx	2 data bytes	Master sends two data bytes to scratchpad (T_H and T_L)
Tx	Reset	Master issues reset pulse.
Rx	Presence	DS18S20 responds with presence pulse.
Tx	CCh	Master issues Skip ROM command.
Tx	BEh	Master issues Read Scratchpad command.
Rx	9 data bytes	Master reads entire scratchpad including CRC. The master then recalculates the CRC of the first eight data bytes from the scratchpad and compares the calculated CRC with the read CRC (byte 9). If they match, the master continues; if not, the read operation is repeated.
Tx	Reset	Master issues reset pulse.
Rx	Presence	DS18S20 responds with presence pulse.
Tx	CCh	Master issues Skip ROM command.
Tx	48h	Master issues Copy Scratchpad command.
Tx	DQ line held high by strong pullup	Master applies strong pullup to DQ for at least 10ms while copy operation is in progress.

DS18S20 Operation Example 3

In this example there is only one DS18S20 on the bus and it is using parasite power. The bus master initiates a temperature conversion then reads the DS18S20 scratchpad and calculates a higher resolution result using the data from the temperature, COUNT REMAIN and COUNT PER °C registers.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
Tx	Reset	Master issues reset pulse.
Tx	Presence	DS18S20 responds with presence pulse.
Tx	CCh	Master issues Skip ROM command.
Tx	44h	Master issues Convert T command.
Tx	DQ line held high by strong pullup	Master applies strong pullup to DQ for the duration of the conversion (t_{CONV}).
Tx	Reset	Master issues reset pulse.
Rx	Presence	DS18S20 responds with presence pulse.
Tx	CCh	Master issues Skip ROM command.
Tx	BEh	Master issues Read Scratchpad command.
Rx	9 data bytes	Master reads entire scratchpad including CRC. The master then recalculates the CRC of the first eight data bytes from the scratchpad and compares the calculated CRC with the read CRC (byte 9). If they match, the master continues; if not, the read operation is repeated. The master also calculates the TEMP_READ value and stores the contents of the COUNT REMAIN and Count Per °C registers.
Tx	Reset	Master issues reset pulse.
Rx	Presence	DS18S20 responds with presence pulse.
—	—	CPU calculates extended resolution temperature using the equation in the *Operation—Measuring Temperature* section.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS18S20+	–55°C to +125°C	3 TO-92
DS18S20+T&R	–55°C to +125°C	3 TO-92 (2000 Piece)
DS18S20-SL+T&R	–55°C to +125°C	3 TO-92 (2000 Piece)*
DS18S20Z	–55°C to +125°C	8 SO
DS18S20Z+	–55°C to +125°C	8 SO
DS18S20Z/T&R	–55°C to +125°C	8 SO (2500 Piece)
DS18S20Z+T&R	–55°C to +125°C	8 SO (2500 Piece)

+Denotes a lead(Pb)-free/RoHS-compliant package. A "+" appears on the top mark of lead(Pb)-free packages.

T&R = Tape and reel.

**TO-92 packages in tape and reel can be ordered with straight or formed leads. Choose "SL" for straight leads. Bulk TO-92 orders are straight leads only.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SO	S8-2	21-0041	90-0096
3 TO-92 (straight leads)	Q3-1	21-0248	—
3 TO-92 (formed leads)	Q3-4	21-0250	—

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/08	In the *Ordering Information* table, added TO-92 straight-lead packages and included a note that the TO-92 package in tape and reel can be ordered with either formed or straight leads	2
1	8/10	Removed the Top Mark column from the *Ordering Information* table; added the continuous power dissipation and lead and soldering temperatures to the *Absolute Maximum Ratings* section	2, 20
2	1/15	Updated *General Description* and *Benefits and Features* section and added *Applications* section	1
3	4/15	Revised *Pin Configuration* and *Ordering Information*	1, 20

Digole

128x64Dots Serial/Parallel LCD

ST7920 Chinese Fonts built in LCD controller/driver

Main Features

- Operation Voltage Range:
  - 4.5V to 5.5V
- Support 8-bit, 4-bit and serial bus MPU interface
- 64 x 16-bit display RAM (DDRAM)
  - Supports 16 words x 4 lines (Max)
  - LCD display range 16 words x 2 lines
- 64 x 256-bit Graphic Display RAM (GDRAM)
- 2M-bits Character Generation ROM (CGROM):
  Support 8192 Chinese words (16x16 dot matrix)
- 16K-bit half-width Character Generation ROM (HCGROM):
  Supports 126 characters (16x8 dot matrix)
- 32-common x 64-segment (2 lines of character) LCD drivers
- Automatic power on reset (POR)
- External reset pin (XRESET)
- With the extension segment drivers, the display area can up to 16x2 lines
- Built-in RC oscillator:
  Frequency is adjusted by an external resistor
- Low power consumption design
  - Normal mode (450uA Typ VDD=5V)
  - Standby mode (30uA Max VDD=5V)
- VLCD (V0 to V_{SS}): max 7V
- Graphic and character mixed display mode
- Multiple instructions:
  - Display Clear
  - Return Home
  - Display ON/OFF
  - Cursor ON/OFF
  - Display Character Blink
  - Cursor Shift
  - Display Shift
  - Vertical Line Scroll
  - Reverse Display (by line)
  - Standby Mode
- Built-in voltage booster (2 times)
  VOUT: max 7V
- 1/33 Duty (with ICON)

Function Description

ST7920 LCD controller/driver IC can display alphabets, numbers, Chinese fonts and self-defined characters. It supports 3 kinds of bus interface, namely 8-bit, 4-bit and serial. All functions, including display RAM, Character Generation ROM, LCD display drivers and control circuits are all in a one-chip solution. With a minimum system configuration, a Chinese character display system can be easily achieved.

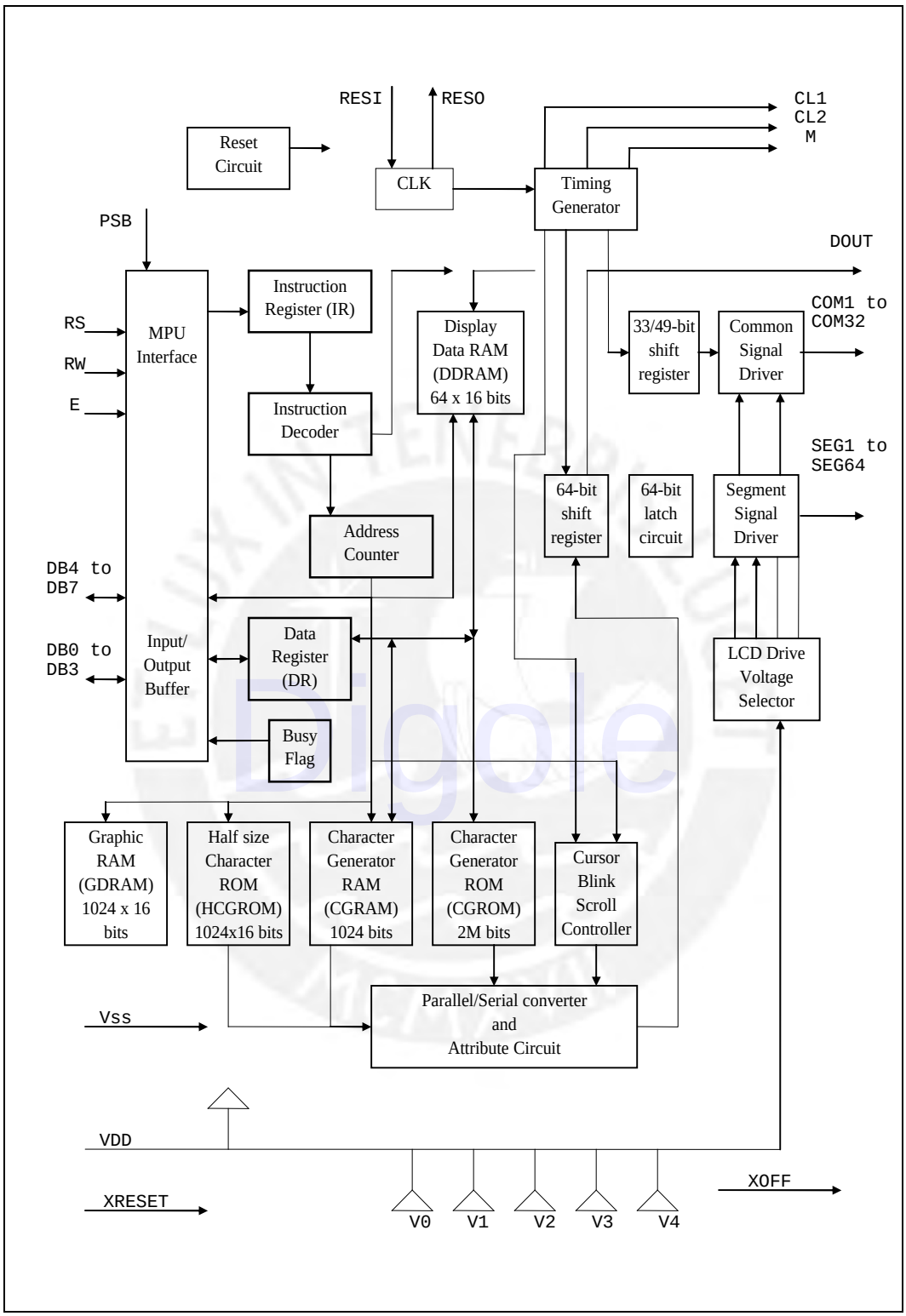
ST7920 includes character ROM with 8192 16x16 dots Chinese fonts and 126 16x8 dots half-width alphanumerical fonts. Besides, it supports 64x256 dots graphic display area for graphic display (GDRAM). Mix-mode display with both character and graphic data is possible. ST7920 has built-in CGRAM and provide 4 sets software programmable 16x16 fonts.

ST7920 has wide operating voltage range (2.7V to 5.5V). It also has low power consumption. So ST7920 is suitable for battery-powered portable device.

ST7920 LCD driver consists of 32-common and 64-segment. Company with the extension segment driver (ST7921) ST7920 can support up to 32-common x 256-segment display.

Part Number	Font Code
ST7920-0A	BIG-5 Code Set (Traditional Chinese)
ST7920-0B	GB Code Set (Simplified Chinese)
ST7920-0C	Chinese (Traditional/Simplified) & Japanese
ST7920-0F	Chinese (Traditional/Simplified), Japanese & Korean

System Block Diagram



Pin Description

Name	No.	I/O	Connects to	Function
RST	17	I	—	System reset input (low active).
PSB	15	I	—	Interface selection: 0: serial mode; 1: 8/4-bit parallel bus mode.
RS(CS*)	4	I	MPU	**Parallel Mode:** Register select. 0: Select instruction register (write) or busy flag, address counter (read); 1: Select data register (write/read). **Serial mode:** Chip select. 1: chip enabled; 0: chip disabled. When chip is disabled, SID and SCLK should be set as “H” or “L”. Transcient of SID and SCLK is not allowed.
RW(SID*)	5	I	MPU	**Parallel Mode:** Read/Write control. 0: Write; 1: Read. **Serial Mode:** Sserial data input.
E(SCLK*)	6	I	MPU	**Parallel Mode:** 1: Enable trigger. **Serial Mode:** Serial clock.
D4 to D7	11~14	I/O	MPU	Higher nibble data bus of 8-bit interface and data bus for 4-bit interface
D0 to D3	7~10	I/O	MPU	Lower nibble data bus of 8-bit interface.
V_{DD}	2	I	Power	V_{DD} : 4.5V to 5.5V.
Vss	1	I	Power	VSS: 0V.
VOUT	18	O	Resistors	LCD voltage doubler output. VOUT ≦ 7V.

Function Description

System interface

ST7920 supports 3 kinds of bus interface to communicate with MPU: 8-bit parallel, 4-bit parallel and clock synchronized serial interface. Parallel interface is selected by PSB=”1” and serial interface is by PSB=”0”. 8-bit / 4-bit interface is selected by function set instruction DL bit.

Two 8-bit registers (Data Register DR and Instruction Register IR) are used in ST7920 to access DRAM or Register. Data Register (DR) can access DDRAM, CGRAM and GDRAM through the address pointer implemented by Address Counter (AC). Instruction Register (IR) stores the instruction sent by MPU to ST7920.

4 kinds of parallel interface access mode can be selected through RS and RW:

RS	RW	Description
L	**L**	MPU write instruction to instruction register (IR)
L	**H**	MPU read busy flag (BF) and address counter (AC)
H	**L**	MPU write data to data register (DR)
H	**H**	MPU read data from data register (DR)

* The serial interface access modes do not have Read operation.

Busy Flag (BF)

ST7920 needs a process time for any received instruction. Before finishing the received instruction, any further instruction is not accepted. The process time of each instruction is not equal and the internal process is finished or not can be determined by the BF. Internal operation is in progress while BF=”1”, that means ST7920 is in busy state. No further instructions will be accepted until BF=”0”. MPU must check BF to determine whether the internal operation is finished or not before issuing instruction.

Address Counter (AC)

Address Counter (AC) is used as the address pointer of DDRAM, CGRAM and GDRAM. (AC) can be set by instruction. After that, accesses (Read/Write operations) to the memories, such as DDRAM, CGRAM or GDRAM, (AC) will be increased or decreased by 1 (according to the setting in “Entry Mode Set” Register). When RS=”0”, RW=”1” and E=”1” the value of (AC) will be output to DB6~DB0.

Character Generation ROM (CGROM) and Half-width Character Generation ROM (HCGROM)

ST7920 is built in a Character Generation ROM (CGROM) to provide 8192 16x16 character fonts and a Half-width Character Generation ROM to provide 126 8x16 alphanumeric characters. It is easy to support multi-language applications such as Chinese and English. Two consecutive bytes are used to specify one 16x16 character or two 8x16 half-width characters. Character codes are written into DDRAM and the corresponding fonts are mapped from CGROM or HCGROM to the display drivers.

Character Generation RAM (CGRAM)

ST7920 is built in a Character Generation RAM (CGRAM) to support user-defined fonts. Four sets of 16x16 bit-maped RAM spaces are available. These user-defined fonts are displayed the same ways as CGROM fonts by writing the related character code into the DDRAM.

Display Data RAM (DDRAM)

There are 64x2 bytes RAM spaces for the Display Data RAM. It can store display data such as 16 characters (16x16) by 4 lines or 32 characters (8x16) by 4 lines. However, only 2 character-lines (maximum 32 common outputs) can be displayed at one time. Character codes stored in DDRAM will refer to the fonts specified by CGROM, HCGROM and CGRAM.

ST7920 can display half-width HCGROM fonts, user-defined CGRAM fonts and full 16x16 CGROM fonts. The character codes in 0000H~0006H will use user-defined fonts in CGRAM. The character codes in 02H~7FH will use half-width alpha numeric fonts. The character code larger than A1H will be treated as 16x16 fonts and will be combined with the next byte automatically. The 16x16 BIG5 fonts are stored in A140H~D75FH while the 16x16 GB fonts are stored in A1A0H~F7FFH. In short:

1. To display HCGROM fonts:
   Write 2 bytes of data into DDRAM to display two 8x16 fonts. Each byte represents 1 character.
   The data is among 02H~7FH.
2. To display CGRAM fonts:
   Write 2 bytes of data into DDRAM to display one 16x16 font.
   Only 0000H, 0002H, 0004H and 0006H are acceptable.
3. To display CGROM fonts:
   Write 2 bytes of data into DDRAM to display one 16x16 font.
   A140H~D75FH are BIG5 code, A1A0H~F7FFH are GB code.

The higher byte (D15~D8) is written first and the lower byte (D7~D0) is the next.

Please refer to Table 5 for the relationship between DDRAM and the address/data of CGRAM.

CGRAM fonts and CGROM fonts can only be displayed in the start position of each address. (Refer toTable 4)

80		81		82		83		84		85		86		87		88		89		8A		8B		8C		8D		8E		8F	
H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
S	**i**	**t**	**r**	**o**	**n**	**i**	**x**		**S**	**T**	**7**	**9**	**2**	**0**																	
矽		創		電		子		**.**	**.**	中		文		編		碼			**(**	正		確		**)**							
矽		創		電		子		**.**	**.**	**.**	中		文		編		碼														

Table 4

Incorrect start position

Graphic RAM (GDRAM)

Graphic Display RAM has 64x256 bits bit-mapped memory space. GDRAM address is set by writing 2 consecutive bytes of vertical address and horizontal address. Two-byte data (16 bits) configures one GDRAM horizontal address. The Address Counter (AC) will be increased by one automatically after receiving the 16-bit data for the next operation. After the horizontal address reaching 0FH, the horizontal address will be set to 00H and the vertical address will not change. The procedure is summarized below:

1. Set vertical address (Y) for GDRAM
2. Set horizontal address (X) for GDRAM
3. Write D15~D8 to GDRAM (first byte)
4. Write D7~D0 to GDRAM (second byte)

Please refer to Table 7 for Graphic Display RAM mapping.

LCD driver

ST7920 embedded LCD driver has 33 commons and 64 segments to drive the LCD panel. Segment data from CGRAM, CGROM and HCGROM are shifted into the 64 bits segment latche to display. Extended segment driver (ST7921) can be used to extend the segment outputs upto 256 segments.

DDRAM data (char. code)					CGRAM Addr.						CGRAM data (higher byte)								CGRAM data (lower byte)							
B15~ B4	B3	B2	B1	B0	B5	B4	B3	B2	B1	B0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	X	00		X	00		0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0
							0	0	0	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0
							0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0
							0	0	1	1	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	0
							0	1	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	1	0	0
							0	1	0	1	0	0	1	1	1	1	0	0	1	0	0	0	0	1	0	0
							0	1	1	0	0	1	1	0	0	1	0	1	0	1	0	0	1	0	0	0
							0	1	1	1	1	0	1	0	0	1	1	0	0	1	0	0	1	0	0	0
							1	0	0	0	0	0	1	0	0	1	0	0	0	1	0	1	0	0	0	0
							1	0	0	1	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0
							1	0	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	0	0
							1	0	1	1	0	0	1	1	1	1	0	0	0	0	1	0	0	0	0	0
							1	1	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0
							1	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
							1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
							1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	X	01		X	01		0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	
							0	0	0	1	0	0	0	1	1	0	1	0	0	0	0	0	0	1	0	0
							0	0	1	0	0	0	1	0	0	0	0	1	0	0	1	1	0	1	0	0
							0	0	1	1	0	1	0	1	1	1	0	1	1	0	1	0	0	1	0	0
							0	1	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0
							0	1	0	1	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0
							0	1	1	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1	0	0
							0	1	1	1	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0
							1	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1	0	0
							1	0	0	1	0	1	1	1	1	1	1	1	0	0	1	0	0	1	0	0
							1	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	0
							1	0	1	1	0	1	1	1	1	1	1	1	1	0		0	0	1	0	0
							1	1	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	1	0	0
							1	1	0	1	1	0	1	1	1	1	1	1	1	0	0	1	1	1	0	0
							1	1	1	0	1	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0
							1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5: DDRAM data (character code) vs. CGRAM data/address map

Note:

1. DDRAM data (character code) bit1 and bit2 are identical with CGRAM address bit4 and bit5.
2. CGRAM address bit0 to bit3 specify total 16 rows. Row-16 is for cursor display. The data in Row-16 will be logically OR to the cursor.
3. CGRAM data for each address is 16 bits.
4. To select the CGRAM font, the bit4 through bit15 of DDRAM data must be “0” while bit0 and bit3 are “don’t care”.

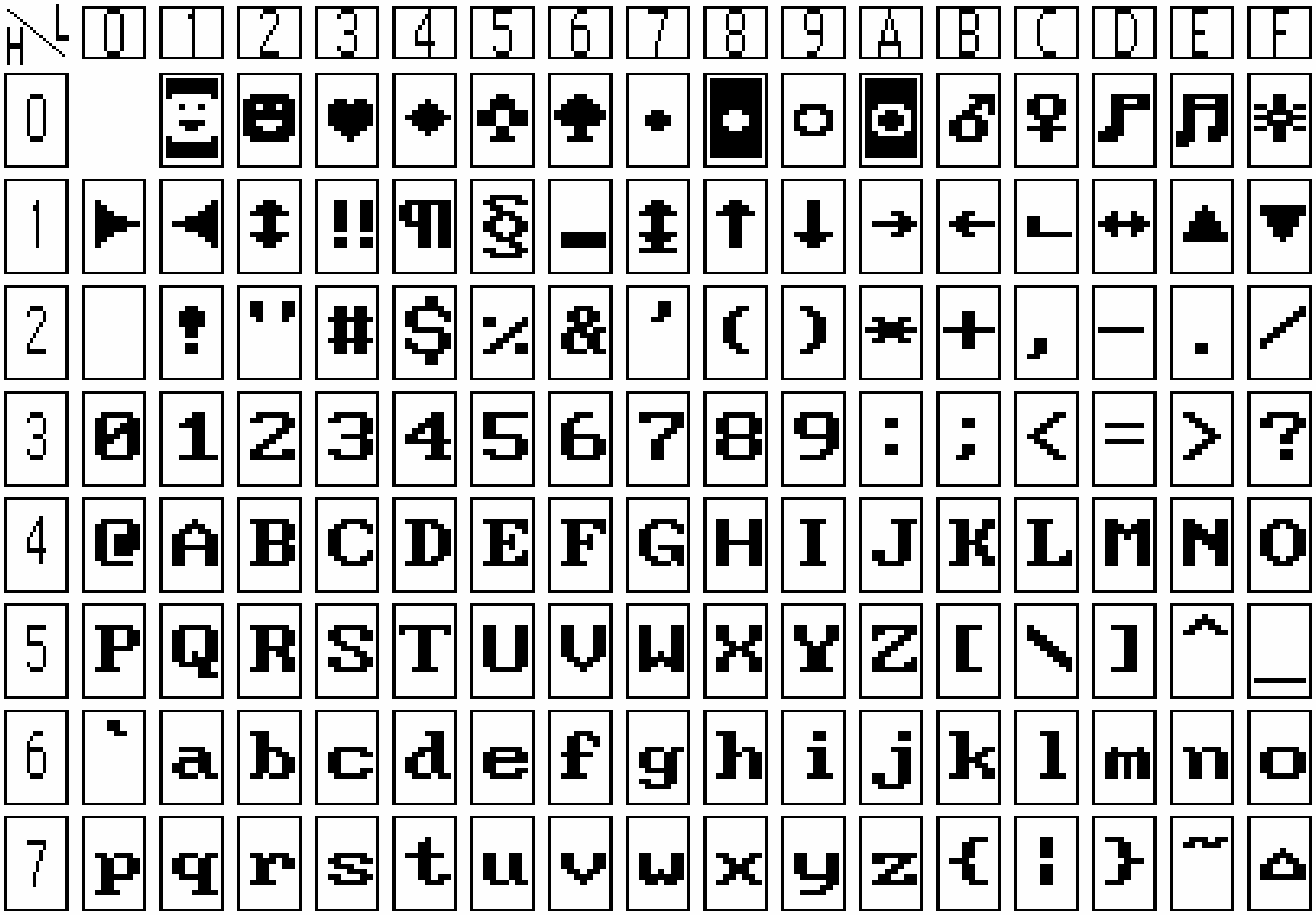


Table 6 16x8 half-width characters

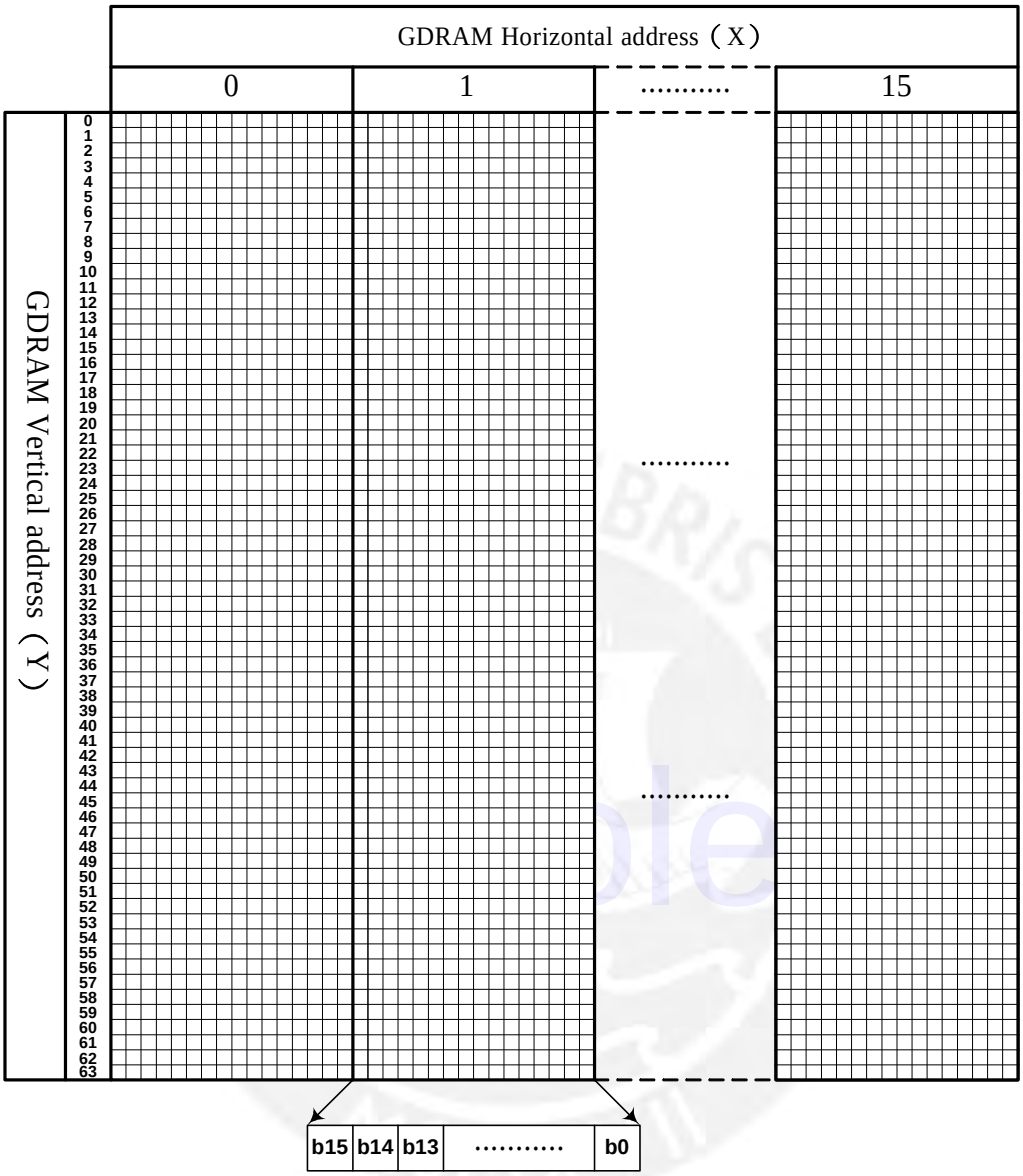


Table 7 GDRAM display coordinates and corresponding address

Instructions

ST7920 offers basic instruction set and extended instruction set:

Instruction Set 1: (RE=0: Basic Instruction)

Inst.	Code										Description	Exec time (540KHZ)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Display Clear	0	0	0	0	0	0	0	0	0	1	Fill DDRAM with "20H" and set DDRAM address counter (AC) to "00H".	1.6 ms
Return Home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address counter (AC) to "00H", and put cursor to origin ；the content of DDRAM are not changed	72 us
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Set cursor position and display shift when doing write or read operation	72 us
Display Control	0	0	0	0	0	0	1	D	C	B	D=1: Display ON C=1: Cursor ON B=1: Character Blink ON	72 us
Cursor Display Control	0	0	0	0	0	1	S/C	R/L	X	X	Cursor position and display shift control; the content of DDRAM are not changed	72 us
Function Set	0	0	0	0	1	DL	X	0 RE	X	X	DL=1 8-bit interface DL=0 4-bit interface **RE=1: extended instruction** **RE=0: basic instruction**	72 us
Set CGRAM Address.	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address to address counter (AC) **Make sure that in extended instruction SR=0 (scroll or RAM address select)**	72 us
Set DDRAM Address.	0	0	1	0 AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address to address counter (AC) AC6 is fixed to 0	72 us
Read Busy Flag (BF) & AC.	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read busy flag (BF) for completion of internal operation, also Read out the value of address counter (AC)	0 us
Write RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to internal RAM (DDRAM/CGRAM/GDRAM)	72 us
Read RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/GDRAM)	72 us

Instruction set 2: (RE=1: extended instruction)

Inst.	Code										Description	Exec time (540KHZ)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Standby	0	0	0	0	0	0	0	0	0	1	Enter standby mode, any other instruction can terminate. COM1…32 are halted.	72 us
Scroll or RAM Address. Select	0	0	0	0	0	0	0	0	1	SR	SR=1: enable vertical scroll position SR=0: enable CGRAM address **(basic instruction)**	72 us
Reverse (by line)	0	0	0	0	0	0	0	1	R1	R0	Select 1 out of 4 line (in DDRAM) and decide whether to reverse the display by toggling this instruction **R1,R0 initial value is 0,0**	72 us
Extended Function Set	0	0	0	0	1	DL	X	1 RE	G	0	DL=1 :8-bit interface DL=0 :4-bit interface **RE=1: extended instruction set** **RE=0: basic instruction set** G=1 :graphic display ON G=0 :graphic display OFF	72 us
Set Scroll Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	SR=1: AC5~AC0 the address of vertical scroll	72 us
Set Graphic Display RAM Address	0	0	1	0 0	0 AC5	0 AC4	AC3 AC3	AC2 AC2	AC1 AC1	AC0 AC0	Set GDRAM address to address counter (AC) Set the vertical address first and followed the horizontal address by consecutive writings Vertical address range: AC5…AC0 Horizontal address range: AC3…AC0	72 us

Note:

1. Make sure that ST7920 is not in busy state by reading the busy flag before sending instruction or data. If using delay loop instead, please make sure the delay time is enough. Please refer to the instruction execution time.
2. “RE” is the selection bit of basic and extended instruction set. After setting the RE bit, the value will be kept. So that the software doesn’t have to set RE every time when using the same instruction set.

Initial Setting (Register flag) (RE=0: basic instruction)

Inst.	Code										Description
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Cursor move to right ,DDRAM address counter (AC) plus 1
									1	**0**	
Display Control	0	0	0	0	0	0	1	D	C	B	Display, cursor and blink are ALL OFF
								0	**0**	**0**	
CURSOR DISPLAY SHIFT	0	0	0	0	0	1	S/C	R/L	X	X	No cursor or display shift operation
							X	**X**			
FUNCTION SET	0	0	0	0	1	DL	X	0 RE	X	X	**8-bit** MPU interface , basic instruction set
						1		**0**			

Initial Setting (Register flag) (RE=1: extended instruction set)

Inst.	Code										Description
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
SCROLL OR RAM ADDR. SELECT	0	0	0	0	0	0	0	0	1	SR	Allow vertical scroll or set CGRAM address
										0	
REVERSE	0	0	0	0	0	0	0	1	R1	R0	Begin with normal and toggle to reverse
									0	0	
EXTENDED FUNCTION SET	0	0	0	0	1	DL	X	1 RE	G	0	Graphic display OFF
									0		

Description of basic instruction set

- Display Clear

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

This instruction will change the following items:

1. Fill DDRAM with "20H"(space code).
2. Set DDRAM address counter (AC) to"00H".
3. Set Entry Mode I/D bit to be "1". Cursor moves right and AC adds 1 after write or read operation.

- Return Home

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	X

Set address counter (AC) to "00H". Cursor moves to origin. Then content of DDRAM is not changed.

- Enry Mode Set

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I/D	S

Set the cursor movement and display shift direction when doing write or read operation.

I/D: Address Counter Control: (Increase/Decrease)

When I/D = "1", cursor moves right, address counter (AC) is increased by 1.

When I/D = "0", cursor moves left, address counter (AC) is decreased by 1.

S: Display Shift Control: (Shift Left/Right)

S	I/D	DESCRIPTION
H	H	Entire display shift left by 1
H	L	Entire display shift right by 1

- Display Control

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

Controls display, cursor and blink ON/OFF.
D: Display ON/OFF control bit
When D = "1", display ON
When D = "0", display OFF, the content of DDRAM is not changed
C: Cursor ON/OFF control bit
When C = "1", cursor ON.
When C = "0", cursor OFF.
B: Character Blink ON/OFF control bit
When B = "1", cursor position blink ON. Then display data (character) in cursor position will blink.
When B = "0", cursor position blink OFF

- Cursor/Display Shift Control

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S/C	R/L	X	X

This instruction configures the cursor moving direction or the display shifting direction. The content of DDRAM is not changed.

S/C	R/L	Description	AC Value
L	L	Cursor moves left by 1 position	AC=AC-1
L	H	Cursor moves right by 1 position	AC=AC+1
H	L	Display shift left by 1, cursor also follows to shift.	AC=AC
H	H	Display shift right by 1, cursor also follows to shift.	AC=AC

- Function Set

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	X	RE	X	X

DL: 4/8-bit interface control bit
When DL = "1", 8-bit MPU bus interface
When DL = "0", 4-bit MPU bus interface
RE: extended instruction set control bit
When RE = "1", extended instruction set
When RE = "0", basic instruction set

In same instruction cannot alter DL and RE at once. Make sure that change DL first then RE.

- Set CGRAM Address

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address into address counter (AC)
AC range is 00H…3FH
Make sure that in extended instruction SR=0 (scroll address or RAM address select)

- Set DDRAM Address

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address into address counter (AC).
First line AC range is 80H…8FH
Second line AC range is 90H…9FH
Third line AC range is A0H…AFH
Fourth line AC range is B0H…BFH
Please note that only 2 lines can be display with one ST7920.

- Read Busy Flag (BF) and Address

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Read busy flag (BF) can check whether the internal operation is finished or not. At the same time, the value of address counter (AC) is also read. When BF = “1”, further instruction(s) will not be accepted until BF = “0”.

- Write Data to RAM

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write data to the internal RAM and increase/decrease the (AC) by 1
Each RAM address (CGRAM, DDRAM and GDRAM…) must write 2 consecutive bytes for 16-bit data. After receiving the second byte, the address counter will increase or decrease by 1 according to the entry mode set control bit.

- Read RAM Data

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read data from the internal RAM and increase/decrease the (AC) by 1
After the operation mode changed to Read (CGRAM, DDRAM and GDRAM…), a “Dummy Read” is required. There is no need to add a “Dummy Read” for the following bytes unless a new address set instruction is issued.

Description of extended instruction set

- Standby

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

This Instruction will set ST7920 entering the standby mode. Any other instruction follows this instruction will terminate the standby mode.
The content of DDRAM remains the same.

- Vertical Scroll or RAM Address Select

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	SR

When SR = "1", the Vertical Scroll mode is enabled.
When SR = "0", “Set CGRAM Address” instruction **(basic instruction)** is enabled.

- Reverse

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	R1	R0

Select 1 out of 4 lines to reverse the display and to toggle the reverse condition by repeating this instruction.
R1, R0 initial vale is 00. The first time issuing this instruction, the display will be reversed while the second time will return the display become normal.

R1	R0	Description
L	L	First line normal or reverse
L	H	Second line normal or reverse
H	L	Third line normal or reverse
H	H	Fourth line normal or reverse

Please note that only 2 lines out of 4 lines of display data can be displayed with one ST7920.

- Extended Function Set

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	X	RE	G	X

DL: 4/8-bit interface control bit
When DL = "1", 8-bit MPU interface.
When DL = "0", 4-bit MPU interface.
RE: extended instruction set control bit
When RE = "1", extended instruction set
When RE = "0", basic instruction set
G: Graphic display control bit
When G = "1", Graphic Display ON
When G = "0", Graphic Display OFF

In same instruction cannot alter DL, RE and G at once. Make sure that change DL or G first and then RE.

- Set Scroll Address

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

SR=1: AC5~AC0 is vertical scroll displacement address

- Set Graphic RAM Address

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	0	AC5	AC4	AC3	AC2	AC1	AC0

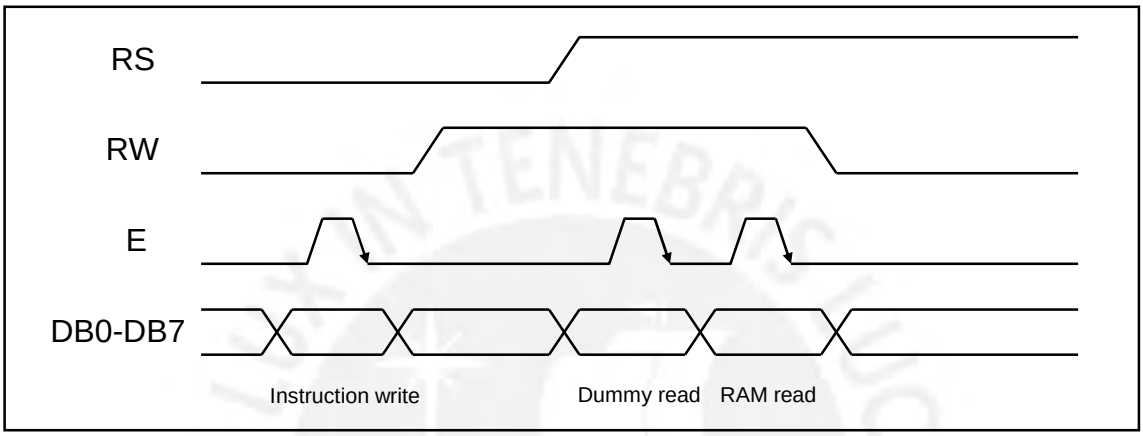
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	0	0	0	AC3	AC2	AC1	AC0

Set GDRAM address into address counter (AC). This is a 2-byte instruction.
The first instruction sets the vertical address while the second one sets the horizontal address (write 2 consecutive bytes to complete the vertical and horizontal address setting).
Vertical address range is AC5...AC0
Horizontal address range is AC3…AC0
The address counter (AC) of graphic RAM (GRAM) will be increased automatically after the vertical and horizontal addresses are set. After horizontal address is increased upto 0FH, it will automatically return to 00H. However, the vertical address will not increase as the result of the same action.

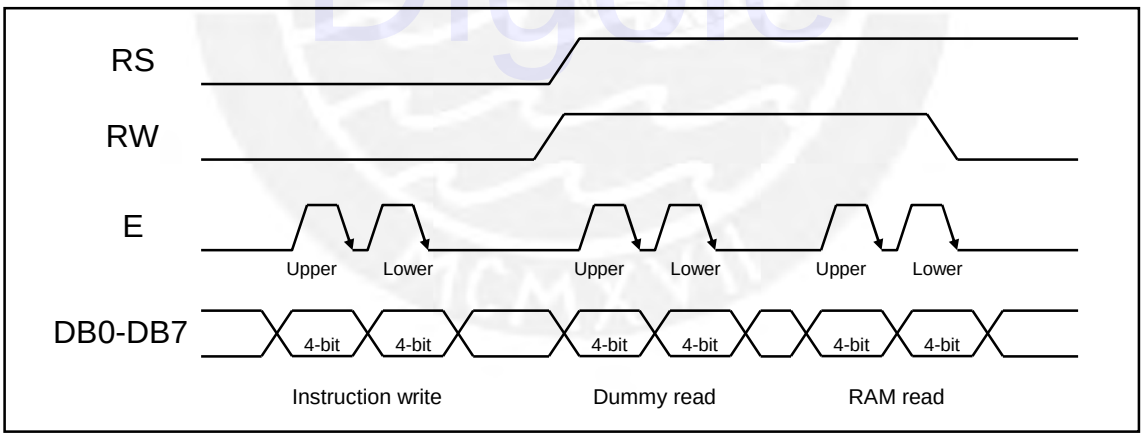
Parallel interface:

ST7920 is in parallel mode by pulling up PSB pin. ST7920 can select 8-bit or 4-bit bus interface by setting the DL control bit in “Function Set” instruction. MPU can control RS, RW, E and DB0…DB7 pins to complete the data transmission.

In 4-bit transfer mode, every 8-bit data or instruction is separated into 2 parts. The higher 4 bits (bit-7~bit-4) data will be transfered first through data pins (DB7~DB4). The lower 4 bits (bit-3~bit-0) data will be transfered second through data pins (DB7~DB4). The (DB3~DB0) data pins are not used during 4-bit transfer mode.



Timing Diagram of 8-bit Parallel Bus Mode Data Transfer



Timing Diagram of 4-bit Parallel Bus Mode Data Transfer

Serial interface:

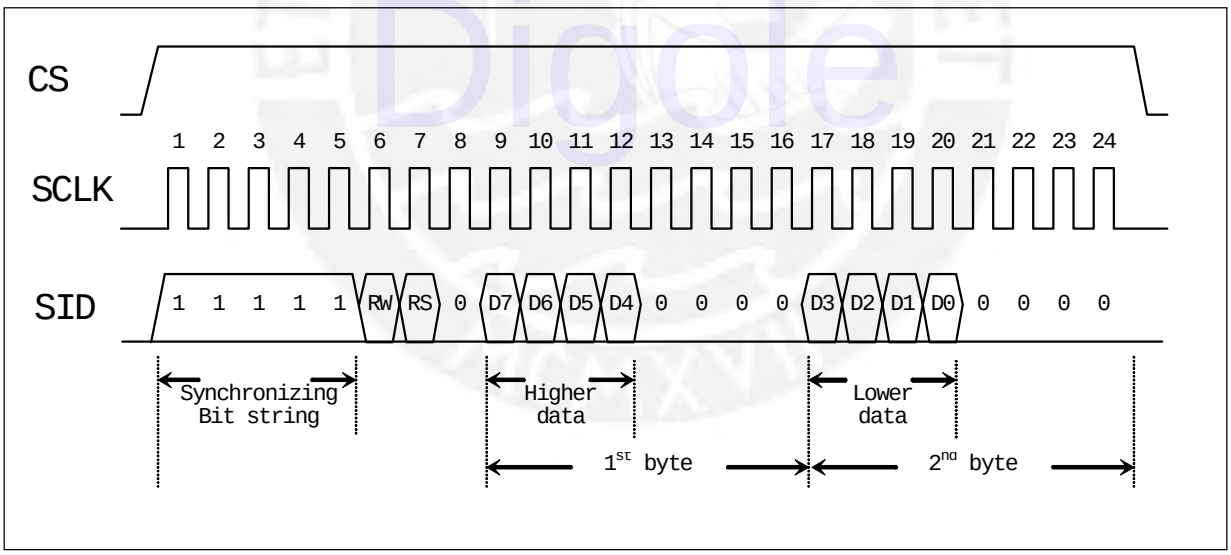
ST7920 is in serial interface mode when pulling down PSB pin. Two pins (SCLK and SID) are used to complete the data transfer. Only write data is available in the serial interface mode.

When chip select (CS) is low, ST7920 serial clock counter and serial data will be reset. Serial transfer counter is set to the first bit and data register is cleared. After CS is “L”, any further change on SID or SCLK is not allowed. It is recommended to keep SCLK at “L” and SID at the last status before set CS to “L”. For a minimal system with only one ST7920 and one MPU, only SCLK and SID pins are necessary. CS pin should pull to high.

ST7920’s serial clock (SCLK) is asynchronous to the internal clock and is generated by MPU. When multiple instruction/data is transferred, the instruction execution time must be considered. MPU must wait till the previous instruction is finished and then send the next instruction. ST7920 has no internal instruction buffer area.

When starting a transmission, a start byte is required. It consists of 5 consecutive “1” (sync character). Serial transfer counter will be reset and synchronized. Followed by 2-bit flag that indicates: read/write (RW) and register/data selected (RS) operation. Last 4 bits are filled by “0”.

After receiving the sync character, RW and RS bits, every 8 bits instruction/data will be separated into 2 groups. Higher 4 bits (DB7~DB4) will be placed in the first section followed by 4 “0”s. And lower 4 bits (DB3~DB0) will be placed in the second section followed by 4 “0”s.



Timing Diagram of Serial Mode Data Transfer

8051 demo program for serial interface

```
;-------------------------------------------------------------
;   Write data from A into INSTRUCTION Register
;-------------------------------------------------------------
WRINS:
        SETB    CS
        SETB    SID         ; SID = 1
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        CLR     SID         ; SID = 0
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        MOVBIT  SID, A.7    ; SID = A.7
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        MOVBIT  SID, A.6    ; SID = A.6
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        MOVBIT  SID, A.5    ; SID = A.5
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        MOVBIT  SID, A.4    ; SID = A.4
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        CLR     SID         ; SID = 0
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        MOVBIT  SID, A.3    ; SID = A.3
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        MOVBIT  SID, A.2    ; SID = A.2
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        MOVBIT  SID, A.1    ; SID = A.1
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        MOVBIT  SID, A.0    ; SID = A.0
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        CLR     SID         ; SID = 0
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        CLR     CS
        CALL    DLY8
        RET
```

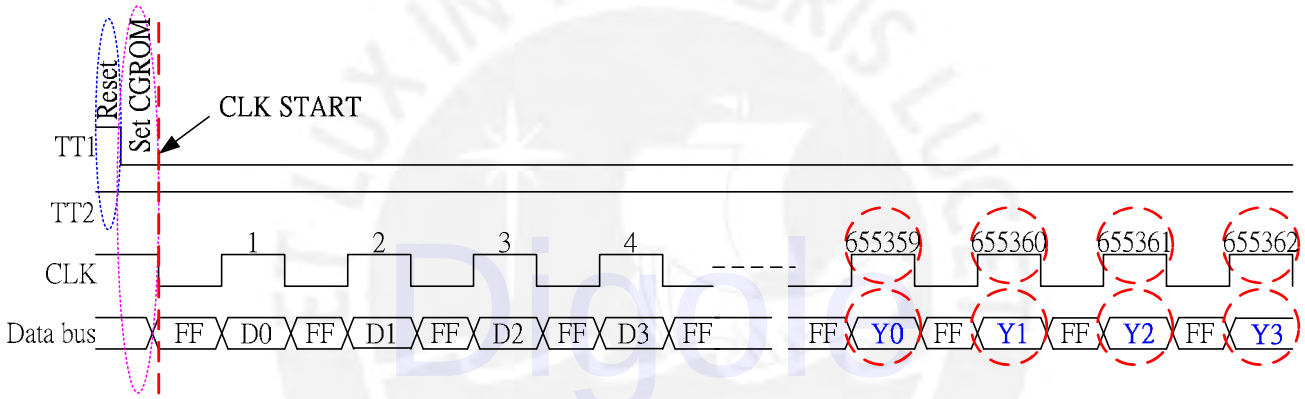
```
;-------------------------------------------------
;   Write data from A into DATA Register
;-------------------------------------------------
WRDATA:
        SETB    CS
        SETB    SID         ; SID = 1
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        CLR     SID         ; SID = 0
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SID         ; SID = 1
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        CLR     SID         ; SID = 0
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        MOVBIT  SID, A.7    ; SID = A.7
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        MOVBIT  SID, A.6    ; SID = A.6
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        MOVBIT  SID, A.5    ; SID = A.5
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        MOVBIT  SID, A.4    ; SID = A.4
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        CLR     SID         ; SID = 0
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        MOVBIT  SID, A.3    ; SID = A.3
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        MOVBIT  SID, A.2    ; SID = A.2
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        MOVBIT  SID, A.1    ; SID = A.1
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        MOVBIT  SID, A.0    ; SID = A.0
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        CLR     SID         ; SID = 0
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        SETB    SCLK        ; READ DATA FROM SID
        CLR     SCLK
        CLR     CS
        CALL    DLY8
        RET
```

Application circuit for testing CGROM and HCGROM:

We can use the function of “CHECK SUM” to check the CGROM is right or error.
See the following notes: Useing IC Pad (Pin4 **à** CLK, Pin5 **à** TT1, Pin6 **à** TT2) to do the “CHECK SUM” function.
The application circuit is at Page49.

Timing Diagram for checking CGROM (TT1=0, TT2=1)

The ST7920 check sum process: (DDRAM must be cleared by 0x00 before this process)
In the first place: Resetting the internal counter (set TT1 and TT2 to Height)
In the second place: Setting CGROM mode (set TT1 to Low, TT2 to Height).
In the third place: CLK starts to count 655362 times.
In the final place: Finishing the counting, read the last four bytes to CHECK SUM (reading only when the CLK is Height).
ST7920 check sum circuit: Data is available when CLK is height; if CLK is low then the data is always FFH. The last four bytes are Y0, Y1, Y2, and Y3.



The fatest execution time is: tCYC=1us (1MHz at 5V).

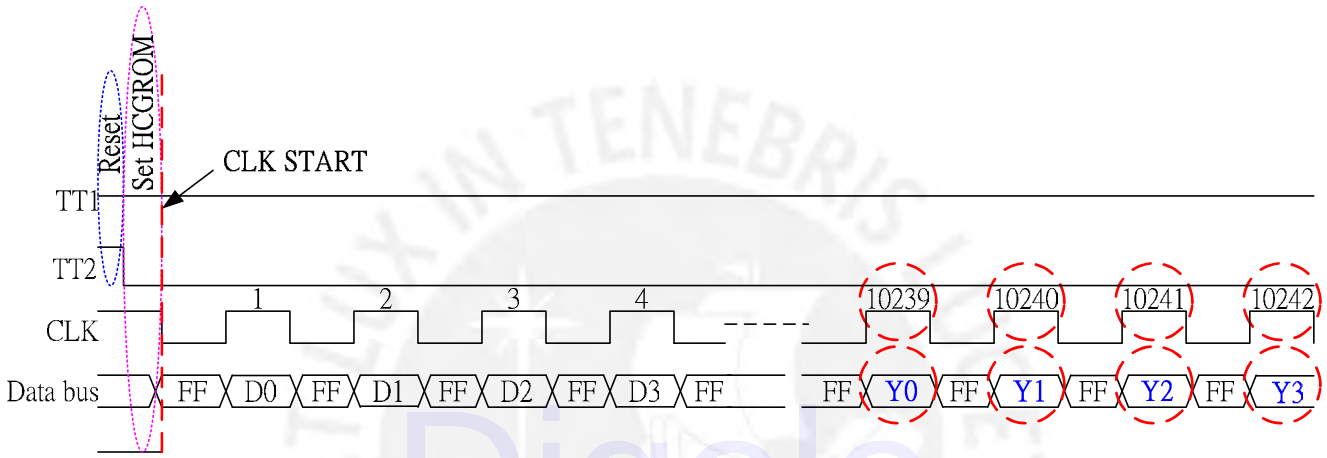
The table below is a comparing table of CGROM for different versions.

	Version (Font)	CGROM Last four bytes			
		Y0	Y1	Y2	Y3
1	Big5 (0A)	38	88	CC	F1
2	GB (0B)	9D	81	79	29
3	0C	FD	6F	B5	85

Timing Diagram for checking HCGROM (TT1=1, TT2=0)

The ST7920 check sum process: (DDRAM must be cleared by 0x00 before this process)
In the first place: Resetting the internal counter (set TT1 and TT2 to Height)
In the second place: Setting CGROM mode (set TT1 to Height, TT2 to Low).
In the third place: CLK starts to count 10242 times.
In the final place: Finishing the counting, read the last four bytes to CHECK SUM (reading only when the CLK is Height).

ST7920 check sum circuit: Data is available when CLK is height; if CLK is low then the data is always FFH. The last four bytes are Y0, Y1, Y2, and Y3.



The fatest execution time is: tCYC=2us (0.5MHz at 5V).

The table below is a comparing table of HCGROM for different versions.

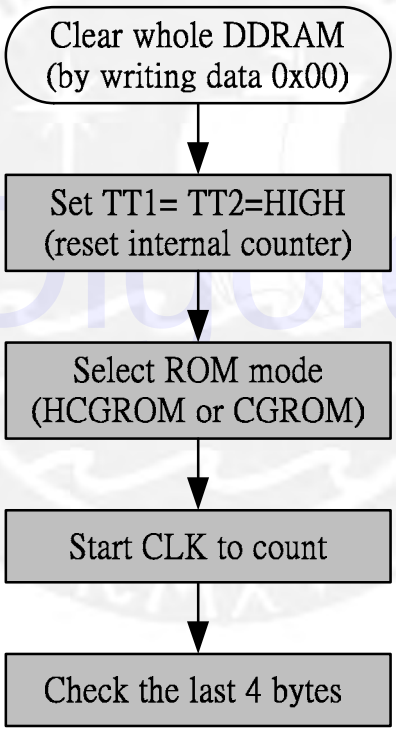
	Version (Font)	HCGROM last four bytes			
		Y0	Y1	Y2	Y3
1	Big5 (0A)	B5	11	B5	11
2	GB (0B)	B5	11	B5	11
3	0C	B5	11	B5	11

Testing Step:

1. Clear whole DDRAM area by writing data 0x00.
2. Composing TT1 and TT2 to make the 'Reset' action, and clear the internal counter.
3. Selecting the test mode by setting TT1 and TT2 (CGROM or HCGROM).
4. After setp1 and setp2, entering some impulse signals through Pin4 (CLK).
5. Reading the CHECK SUM data through D0 to D7.
6. Comparing CHECK SUM with the Code Table (upper table) to check if the data is correct or not.

TT1	TT2	No. of counts	Status
1	1	--	RESET
0	1	655362	CGROM
1	0	10242	HGROM

Test process flow:



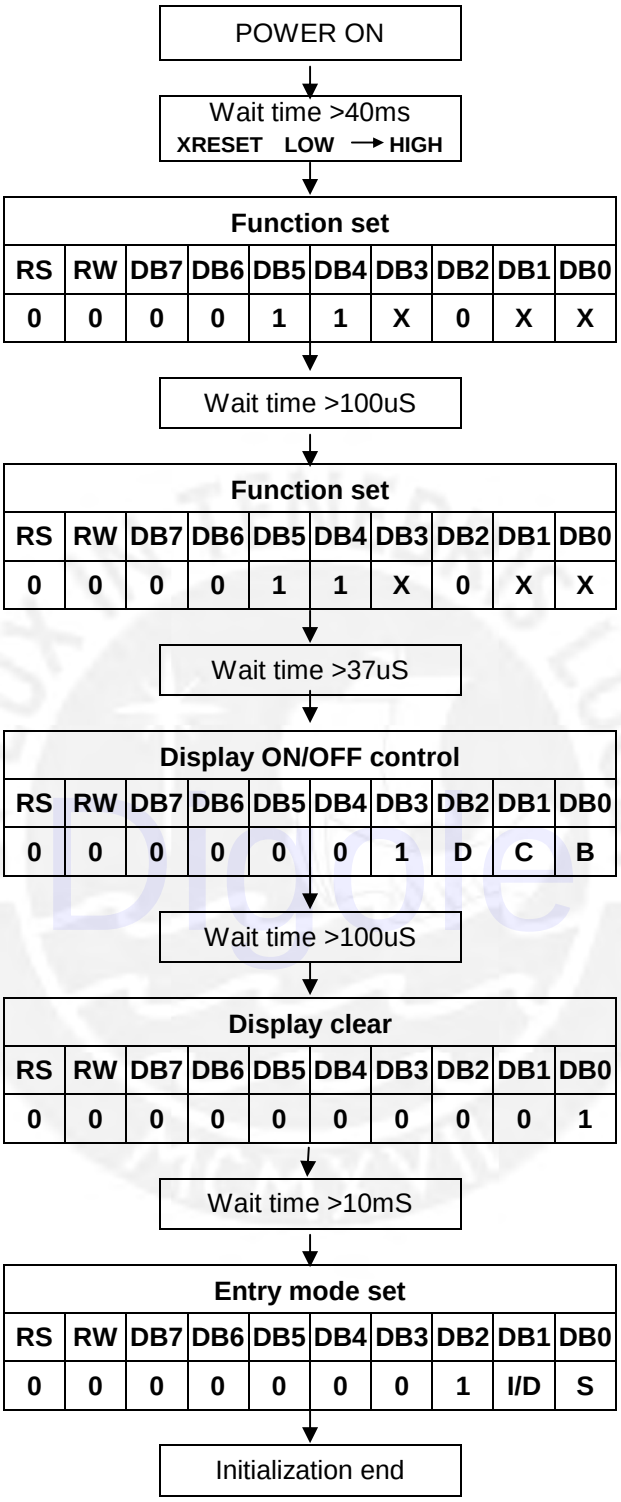
8051 CGROM、HCGROM illustrative test program

```
        ;*******************************;
        ;*      CHECK_ROM              *;
        ;*******************************;
        ;*******************************;
        ;*   Definition of outside Pin *;
        ;*******************************;
CLK     REG     P3.5                    ;
TT1     REG     P3.0                    ;
TT2     REG     P3.1                    ;
TT3     REG     P3.2                    ;CHECK CGROM FLAG
TT4     REG     P3.3                    ;CHECK HCGROM FLAG
TT5     REG     P3.4                    ;ERROR FLAG
        ;*******************************;
        ;*  Definition of internal RAM *;
        ;*******************************;
STACK           EQU     6FH             ;
FUNC            EQU     20H             ;
        ;*******************************;
        ;         Interrupt set        *;
        ;*******************************;
        ORG     00H                     ;
        AJMP    RESET                   ;
        ;*******************************;
        ;*      PROGRAM START          *;
        ;*******************************;
RESET:  MOV     SP,#STACK               ;
        MOV     P1,#FFH                 ;
        MOV     P3,#FFH                 ;
        ;*******************************;
        ;*      CHECK_CGROM            *;
        ;*******************************;
        ;*******************************;
        ;*      Initial DDRAM          *;
        ;*******************************;
        CALL    WR0x00                  ;Write 0x00 to whole DDRAM
        ;*******************************;
        ;*     Initial setting         *;
        ;*******************************;
CGROM:  SETB    TT1                     ;
        SETB    TT2                     ;TT1,TT2 SET HIGH (RESET)
        CALL    DELAY_100US             ;Wait Reset 100us
        CLR     TT1                     ;TT1=LOW TT2=HIGH ( CHECK CGROM)
        SETB    CLK                     ;
        CALL    DELAY_100US             ;
        ;*******************************;
        ;*      start counter          *;
        ;*******************************;
        MOV     R3,#9                   ;
CN4:    MOV     R2,#0                   ;<----
CN3:    MOV     R1,#0                   ;     |
CN2:    CLR     CLK                     ;     |
        SETB    CLK                     ;     |
        DJNZ    R1,CN2                  ;     |
        DJNZ    R2,CN3                  ;     |
        DJNZ    R3,CN4                  ;     |
                                        ;     |
        MOV     R3,#0                   ;     |
CN5:    MOV     R2,#255                 ;     |
CN6:    CLR     CLK                     ;     |
        SETB    CLK                     ;     |
        DJNZ    R2,CN6                  ;     |
        DJNZ    R3,CN5                  ;     |
                                        ;     |
```

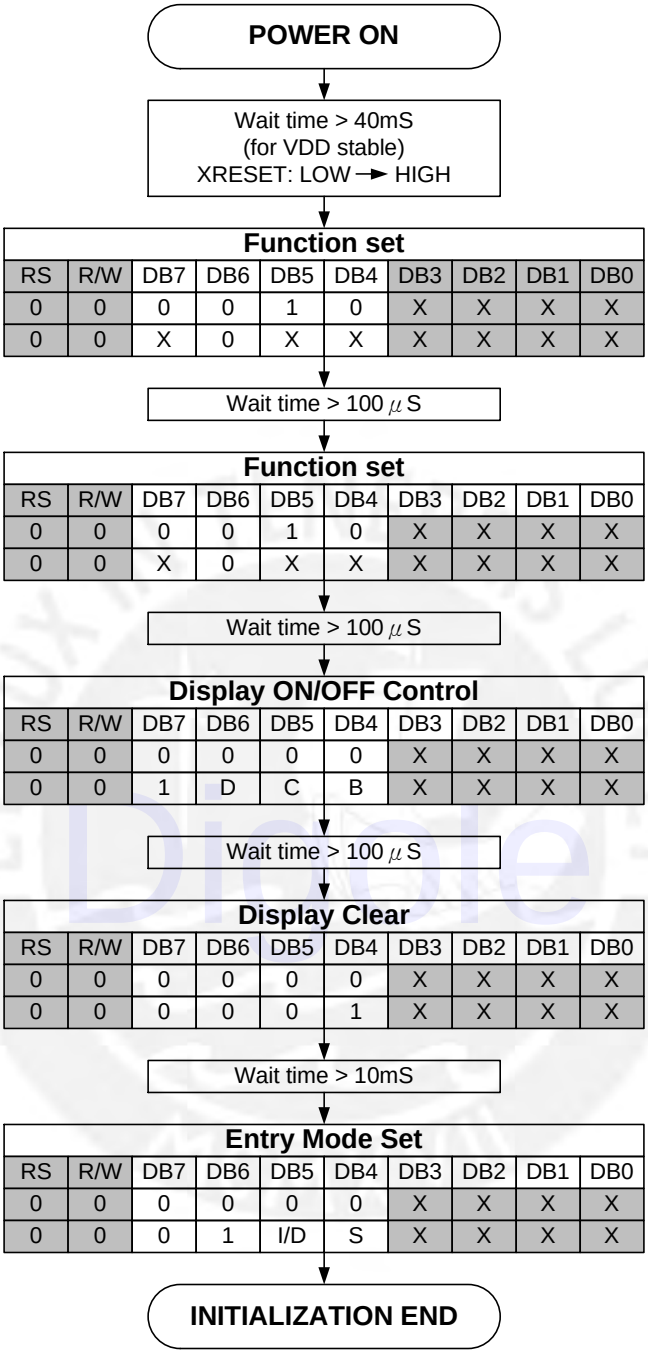
```
        MOV     R3,#63                  ;     |
CN7:    MOV     R2,#2                   ;     |
CN8:    MOV     R1,#2                   ;     |
CN9:    CLR     CLK                     ;     |
        SETB    CLK                     ;     |
        DJNZ    R1,CN9                  ;     |
        DJNZ    R2,CN8                  ;     |
        DJNZ    R3,CN7                  ;     |
        CLR     CLK                     ;     |
        SETB    CLK                     ;     |
        CLR     CLK                     ;     |
        SETB    CLK                     ;<----  Counter 655356
        ;-----------------------------;
        CLR     CLK                     ;Counter 655357
        SETB    CLK                     ;
        MOV     A,P1                    ;A=Y0
        CJNE    A,#FDH,ERRORC           ;COMPARE Y0 DATA
        CLR     CLK                     ;Counter 655358
        SETB    CLK                     ;
        MOV     A,P1                    ;A=Y1
        CJNE    A,#6FH,ERRORC           ;COMPARE Y1 DATA
        CLR     CLK                     ;Counter 655359
        SETB    CLK                     ;
        MOV     A,P1                    ;A=Y2
        CJNE    A,#B5H,ERRORC           ;COMPARE Y2 DATA

        CLR     CLK                     ;Counter 655360
        SETB    CLK                     ;
        MOV     A,P1                    ;A=Y3
        CJNE    A,#85H,ERRORC           ;COMPARE Y3 DATA
        CLR     CLK                     ;
        CLR     TT3                     ;IF OK CLR TT3
        CALL    HCGROM                  ;
ERRORC:                                 ;
        CLR     TT5                     ;IF CGROM CHECK ERROR CLR TT5
;---------------------------------------;
        ;*******************************;
        ;*      CHECK_HCGROM           *;
        ;*******************************;
        ;*******************************;
        ;*      Initial setting        *;
        ;*******************************;
HCGROM: SETB    TT1                     ;
        SETB    TT2                     ;TT1,TT2 SET HIGH (RESET)
        CALL    DELAY_100US             ;Wait Reset 100us
        CLR     TT2                     ;TT2=LOW TT1=HIGH ( CHECK HCGROM)
        SETB    CLK                     ;
        CALL    DELAY_100US             ;
        ;*******************************;
        ;*      start counter          *;
        ;*******************************;
        MOV     R3,#9                   ;
N4:     MOV     R2,#32                  ;<----
N3:     MOV     R1,#32                  ;     |
N2:     CLR     CLK                     ;     |
        SETB    CLK                     ;     |
        DJNZ    R1,N2                   ;     |
        DJNZ    R2,N3                   ;     |
        DJNZ    R3,N4                   ;     |
                                        ;     |
        MOV     R3,#32                  ;     |
N5:     MOV     R2,#31                  ;     |
N6:     CLR     CLK                     ;     |
        SETB    CLK                     ;     |
        DJNZ    R2,N6                   ;     |
        DJNZ    R3,N5                   ;     |
                                        ;     |
        MOV     R2,#30                  ;     |
```

```
N7:     CLR     CLK                     ;     |
        SETB    CLK                     ;     |
        DJNZ    R2,N7                   ;     |
;---------------------------------------;<----  Counter 10236
        CLR     CLK                     ;Counter 10237
        SETB    CLK                     ;
        MOV     A,P1                    ;A=Y0
        CJNE    A,#B5H,ERROR            ;COMPARE Y0 DATA
        CLR     CLK                     ;Counter 10238
        SETB    CLK                     ;
        MOV     A,P1                    ;A=Y1
        CJNE    A,#11H,ERROR            ;COMPARE Y1 DATA
        CLR     CLK                     ;Counter 10239
        SETB    CLK                     ;
        MOV     A,P1                    ;A=Y2
        CJNE    A,#B5H,ERROR            ;COMPARE Y2 DATA
        CLR     CLK                     ;Counter 10240
        SETB    CLK                     ;
        MOV     A,P1                    ;A=Y3
        CJNE    A,#11H,ERROR            ;COMPARE Y3 DATA
        CLR     CLK                     ;
        CLR     TT4                     ;IF HCGROM CHECK OK THEN CLR TT4
        AJMP    $                       ;
ERROR:                                  ;
        CLR     TT5                     ;IF HCGROM CHECK ERROR THEN CLR TT5
        AJMP    $                       ;
        ;*******************************;
        ;*      DELAY TIME 100US       *;
        ;*******************************;
DELAY_100US                             ;
DEL_10  MOV     R6,#5                   ;
DEL_9   MOV     R7,#3                   ;
        DJNZ    R7,$                    ;
        DJNZ    R6,DEL_9                ;
        RET                             ;
END                                     ;
```

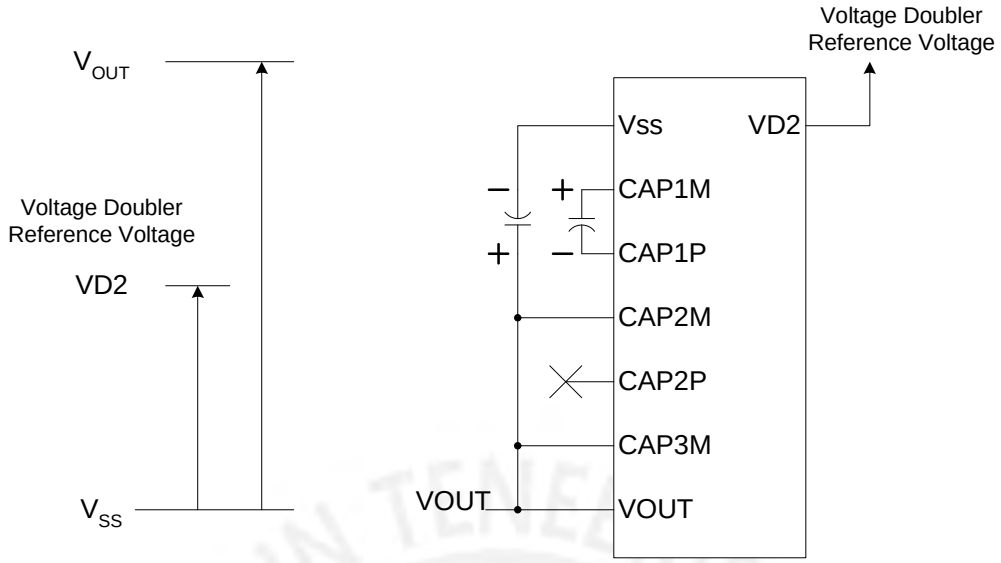
8-bit interface:



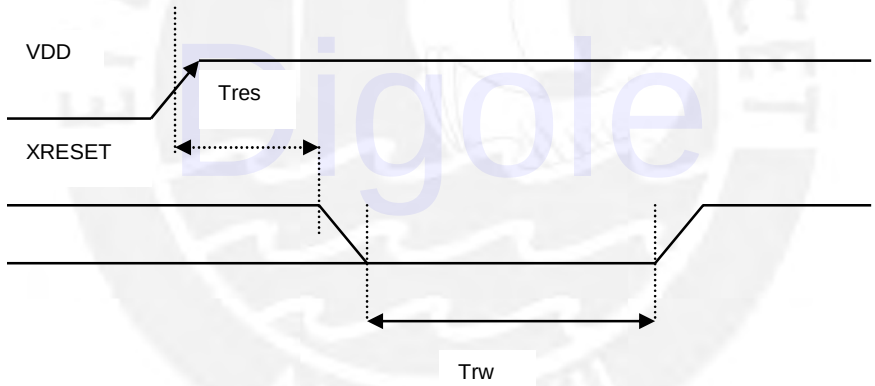
4-bit interface:



Built in voltage booster



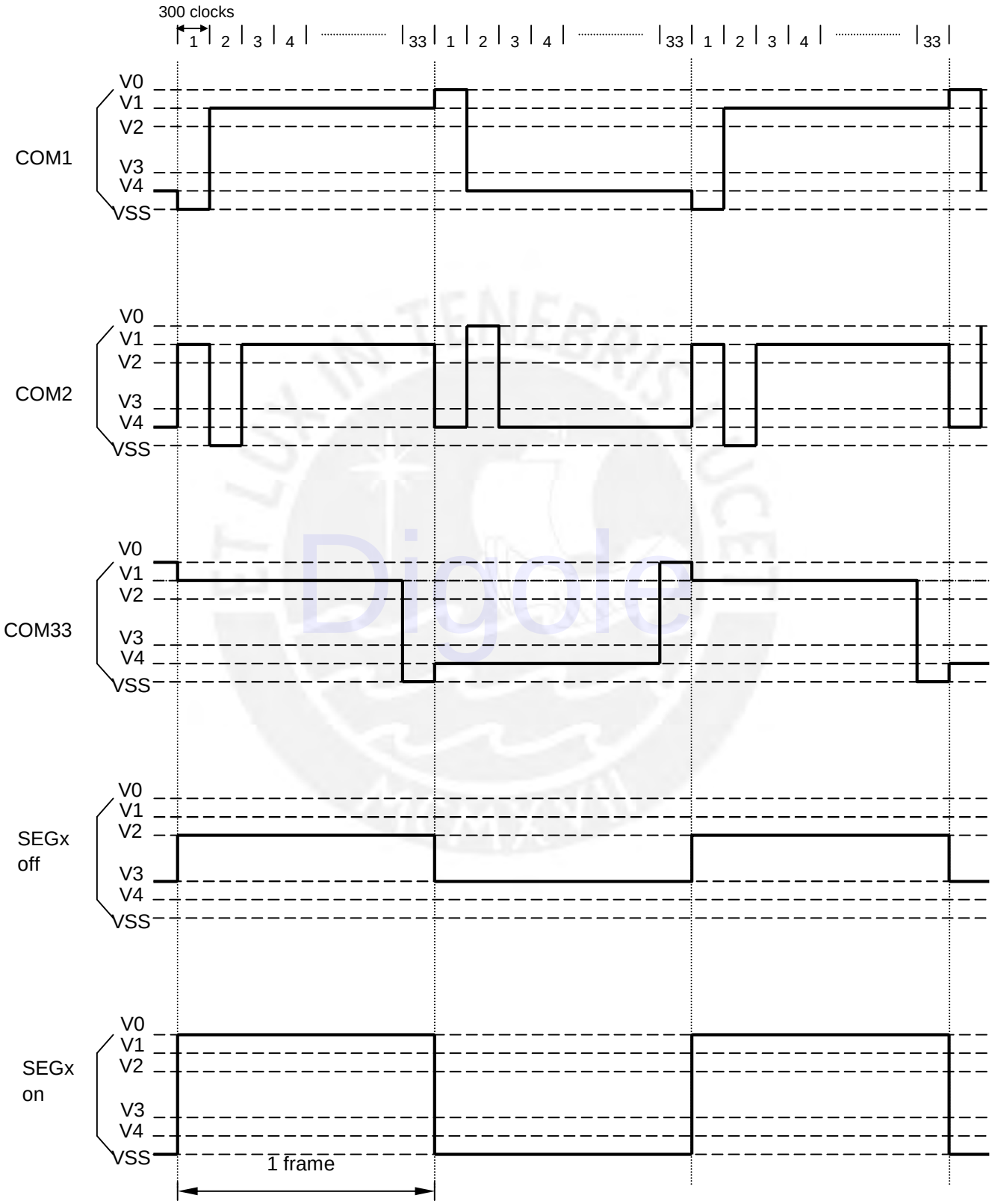
External reset timing



XRESET pulse width	Trw	10us
RESET start time	Tres	50ns

LCD driving wave form (1/33 duty, 1/5 bias)

When oscillation frequency is 540KHZ, 1 clock cycle time = 1.85us
1 frame = 1.85us x 300 x 33 = 18315us=18.3ms



Absolute Maximum Ratings

Characteristics	Symbol	Value
Power Supply Voltage	V_{DD}	-0.3V to +6.0V
LCD Driver Voltage	V_{LCD} or V0	-0.3V to +7.0V
Voltage Doubler Output	V_{OUT}	-0.3V to +7.0V
Input Voltage	V_{IN}	-0.3V to V_{DD}+0.3V
Operating Temperature	T_A	-30℃ to + 85℃
Storage Temperature	T_{STO}	-65℃ to + 150℃

DC Characteristics (T_A = -30℃ ~ 85℃, V_{DD} = 2.7 V - 4.5 V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	-	2.7	-	5.5	V
V_{LCD}	LCD Voltage	V0-VSS	3.0	-	7	V
I_{CC}	Power Supply Current	f_{OSC} = 530KHz, V_{DD}=3.0V Rf=18KΩ	-	0.20	0.45	mA
V_{IH1}	Input High Voltage (Except OSC1)	-	0.7V_{DD}	-	V_{DD}	V
V_{IL1}	Input Low Voltage (Except OSC1)	-	- 0.3	-	0.6	V
V_{IH2}	Input High Voltage (OSC1)	-	V_{DD} – 1	-	V_{DD}	V
V_{IL2}	Input Low Voltage (OSC1)	-	-	-	1.0	V
V_{OH1}	Output High Voltage (DB0 - DB7)	I_{OH} = -0.1mA	0.8V_{DD}	-	V_{DD}	V
V_{OL1}	Output Low Voltage (DB0 - DB7)	I_{OL} = 0.1mA	-	-	0.1	V
V_{OH2}	Output High Voltage (Except DB0 - DB7)	I_{OH} = -0.04mA	0.8V_{DD}	-	V_{DD}	V
V_{OL2}	Output Low Voltage (Except DB0 - DB7)	I_{OL} = 0.04mA	-	-	0.1V_{DD}	V
I_{LEAK}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-1	-	1	µA
I_{PUP}	Pull Up MOS Current	V_{DD} = 3V	22	27	32	µA

DC Characteristics (T_A = -30℃ ~ 85℃, V_{DD} = 4.5 V - 5.5 V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	-	4.5	-	5.5	V
V_{LCD}	LCD Voltage	V0-V_{SS}	3.0	-	7	V
I_{CC}	Power Supply Current	f_{OSC} = 540KHz, V_{DD}=5V Rf=33KΩ	-	0.45	0.75	mA
V_{IH1}	Input High Voltage (Except OSC1)	-	0.7V_{DD}	-	V_{DD}	V
V_{IL1}	Input Low Voltage (Except OSC1)	-	-0.3	-	0.6	V
V_{IH2}	Input High Voltage (OSC1)	-	V_{DD}-1	-	V_{DD}	V
V_{IL2}	Input Low Voltage (OSC1)	-	-	-	1.0	V
V_{OH1}	Output High Voltage (DB0 - DB7)	I_{OH} = -0.1mA	0.8V_{DD}	-	V_{DD}	V
V_{OL1}	Output Low Voltage (DB0 - DB7)	I_{OL} = 0.1mA	-	-	0.4	V
V_{OH2}	Output High Voltage (Except DB0 - DB7)	I_{OH} = -0.04mA	0.8V_{DD}	-	V_DD	V
V_{OL2}	Output Low Voltage (Except DB0 - DB7)	I_{OL} = 0.04mA	-	-	0.1V_{DD}	V
I_{LEAK}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-1	-	1	µA
I_{PUP}	Pull Up MOS Current	V_{DD} = 5V	75	80	85	µA

AC Characteristics (T_A = -30℃ ~ 85℃, V_{DD} = 4.5V) Parallel Mode Interface

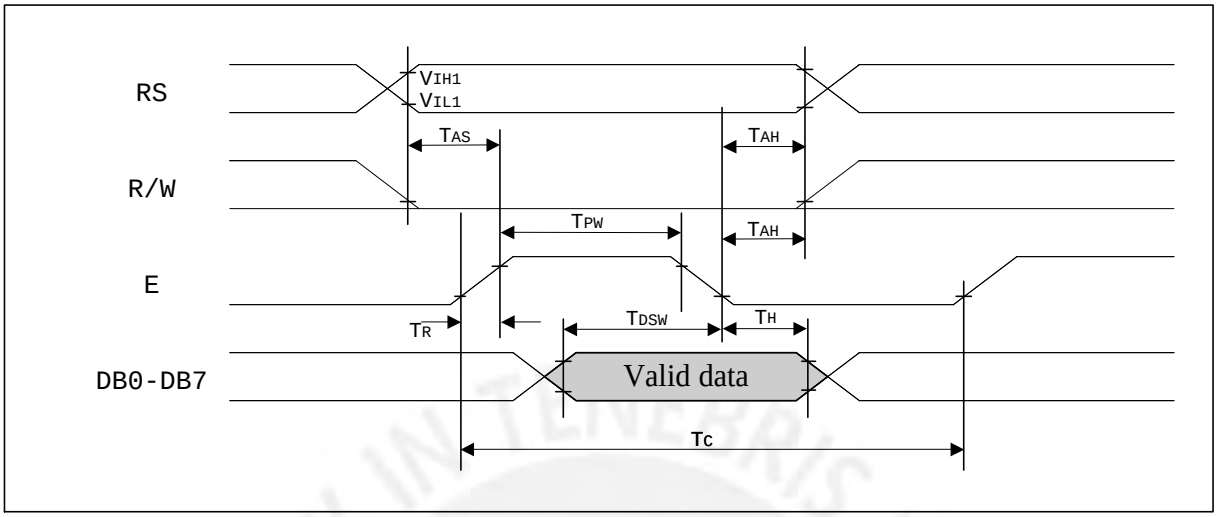
Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R = 33KΩ	480	540	600	KHz
External Clock Operation						
f_{EX}	External Frequency	-	480	540	600	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	μs
Write Mode (Writing data from MPU to ST7920)						
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	140	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	10	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	20	-	-	ns
T_{DSW}	Data Setup Time	Pins: DB0 - DB7	40	-	-	ns
T_H	Data Hold Time	Pins: DB0 - DB7	20	-	-	ns
Read Mode (Reading Data from ST7920 to MPU)						
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	140	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	10	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	20	-	-	ns
T_{DDR}	Data Delay Time	Pins: DB0 - DB7	-	-	100	ns
T_H	Data Hold Time	Pins: DB0 - DB7	20	-	-	ns
Interface Mode with LCD Driver(ST7921)						
T_{CWH}	Clock Pulse with High	Pins: CL1, CL2	800	-	-	ns
T_{CWL}	Clock Pulse with Low	Pins: CL1, CL2	800	-	-	ns
T_{CST}	Clock Setup Time	Pins: CL1, CL2	500	-	-	ns
T_{SU}	Data Setup Time	Pin: D	300	-	-	ns
T_{DH}	Data Hold Time	Pin: D	300	-	-	ns
T_{DM}	M Delay Time	Pin: M	-1000	-	1000	ns

AC Characteristics (T_A = -30℃ ~ 85℃, V_{DD} = 2.7V) Parallel Mode Interface

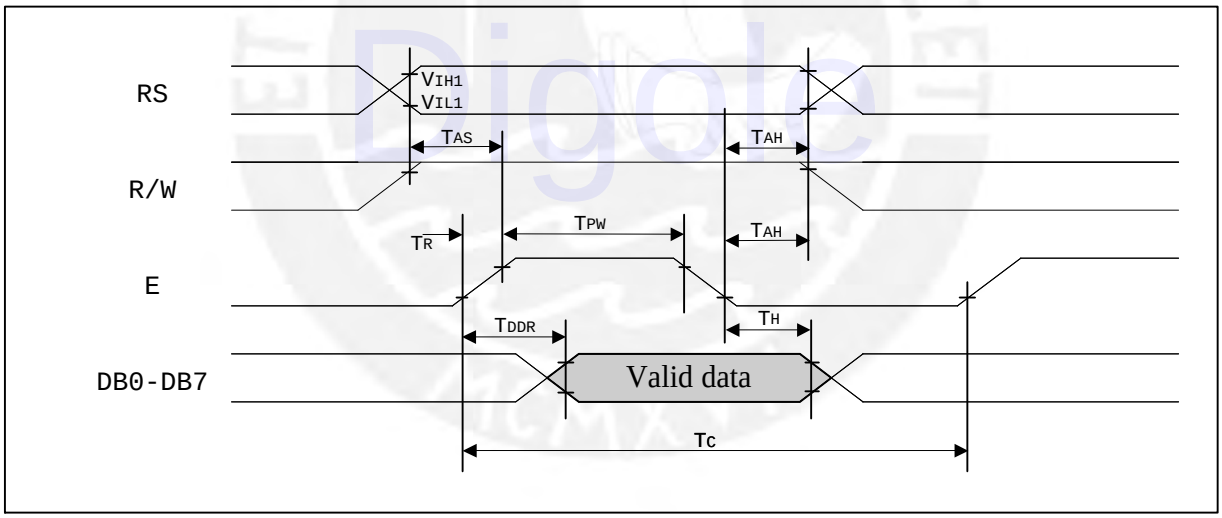
Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R = 18KΩ	470	530	590	KHz
External Clock Operation						
f_{EX}	External Frequency	-	470	530	590	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	μs
Write Mode (Writing data from MPU to ST7920)						
T_C	Enable Cycle Time	Pin E	1800	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	160	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	10	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	20	-	-	ns
T_{DSW}	Data Setup Time	Pins: DB0 - DB7	40	-	-	ns
T_H	Data Hold Time	Pins: DB0 - DB7	20	-	-	ns
Read Mode (Reading Data from ST7920 to MPU)						
T_C	Enable Cycle Time	Pin E	1800	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	320	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	10	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	20	-	-	ns
T_{DDR}	Data Delay Time	Pins: DB0 - DB7	-	-	260	ns
T_H	Data Hold Time	Pins: DB0 - DB7	20	-	-	ns
Interface Mode with LCD Driver(ST7921)						
T_{CWH}	Clock Pulse with High	Pins: CL1, CL2	800	-	-	ns
T_{CWL}	Clock Pulse with Low	Pins: CL1, CL2	800	-	-	ns
T_{CST}	Clock Setup Time	Pins: CL1, CL2	500	-	-	ns
T_{SU}	Data Setup Time	Pin: D	300	-	-	ns
T_{DH}	Data Hold Time	Pin: D	300	-	-	ns
T_{DM}	M Delay Time	Pin: M	-1000	-	1000	ns

8-bit interface timing diagram

- MPU write data to ST7920



- MPU read data from ST7920



AC Characteristics (T_A = -30℃ ~ 85℃, V_{DD} = 4.5V) Serial Mode Interface

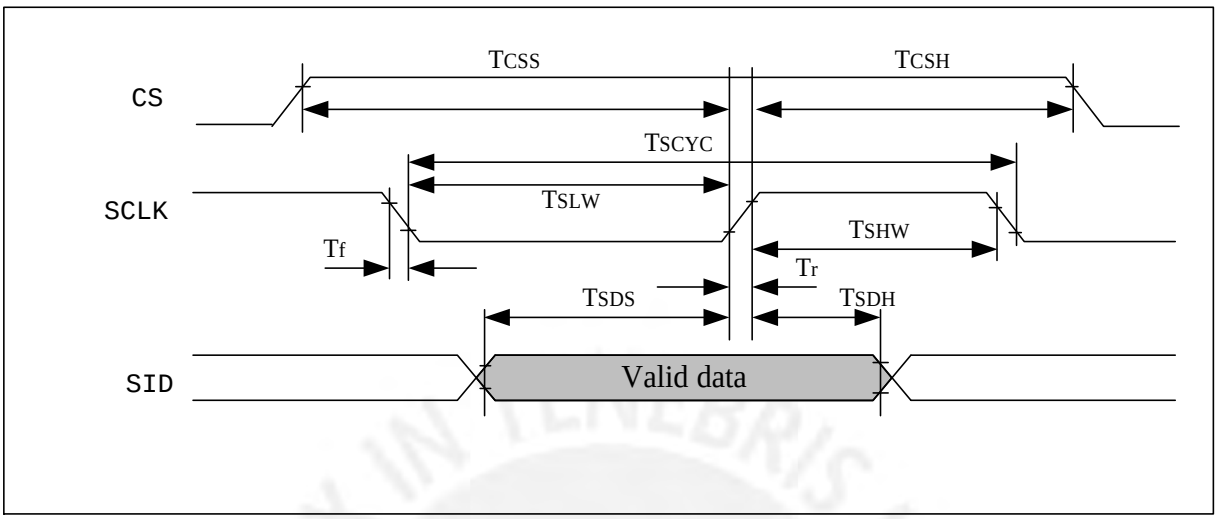
Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R = 33KΩ	470	530	590	KHz
External Clock Operation						
f_{EX}	External Frequency	-	470	530	590	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	μs
T_{SCYC}	Serial clock cycle	Pin E	400	-	-	ns
T_{SHW}	SCLK high pulse width	Pin E	200	-	-	ns
T_{SLW}	SCLK low pulse width	Pin E	200	-	-	ns
T_{SDS}	SID data setup time	Pins RW	40	-	-	ns
T_{SDH}	SID data hold time	Pins RW	40	-	-	ns
T_{CSS}	CS setup time	Pins RS	60	-	-	ns
T_{CSH}	CS hold time	Pins RS	60	-	-	ns

AC Characteristics (T_A = -30℃ ~ 85℃, V_{DD} = 2.7V) Serial Mode Interface

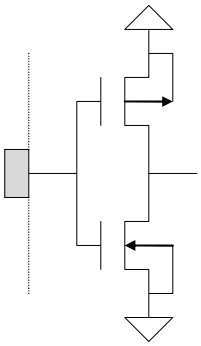
Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R = 18KΩ	470	530	590	KHz
External Clock Operation						
f_{EX}	External Frequency	-	470	530	590	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	μs
T_{SCYC}	Serial clock cycle	Pin E	600	-	-	ns
T_{SHW}	SCLK high pulse width	Pin E	300	-	-	ns
T_{SLW}	SCLK low pulse width	Pin E	300	-	-	ns
T_{SDS}	SID data setup time	Pins RW	40	-	-	ns
T_{SDH}	SID data hold time	Pins RW	40	-	-	ns
T_{CSS}	CS setup time	Pins RS	60	-	-	ns
T_{CSH}	CS hold time	Pins RS	60	-	-	ns

Serial interface timing diagram

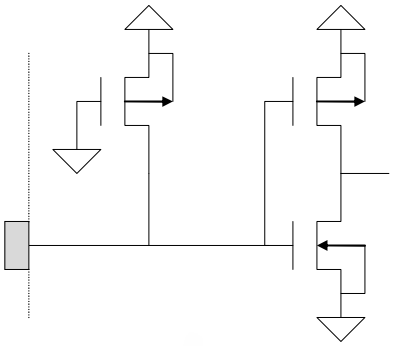
- MPU write data to ST7920



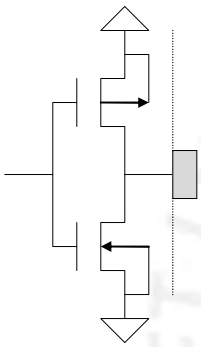
I/O pin diagram



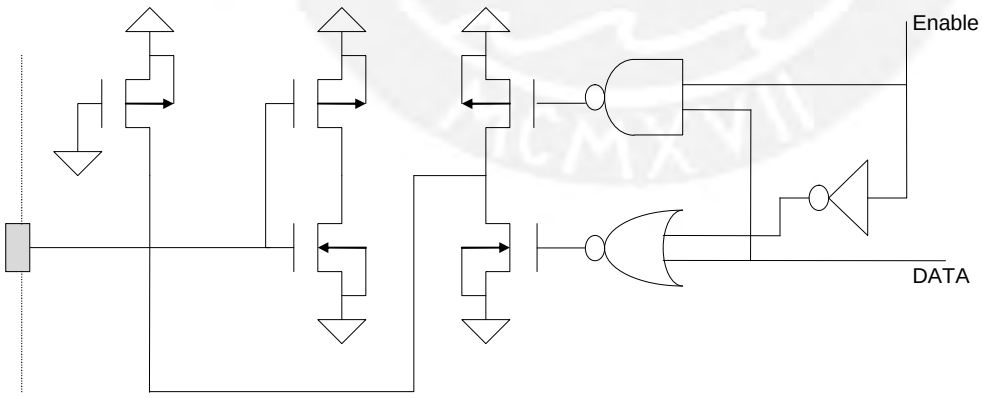
Input PAD: E (No Pull-up)



Input PAD: RS, RW (with Pull-up)

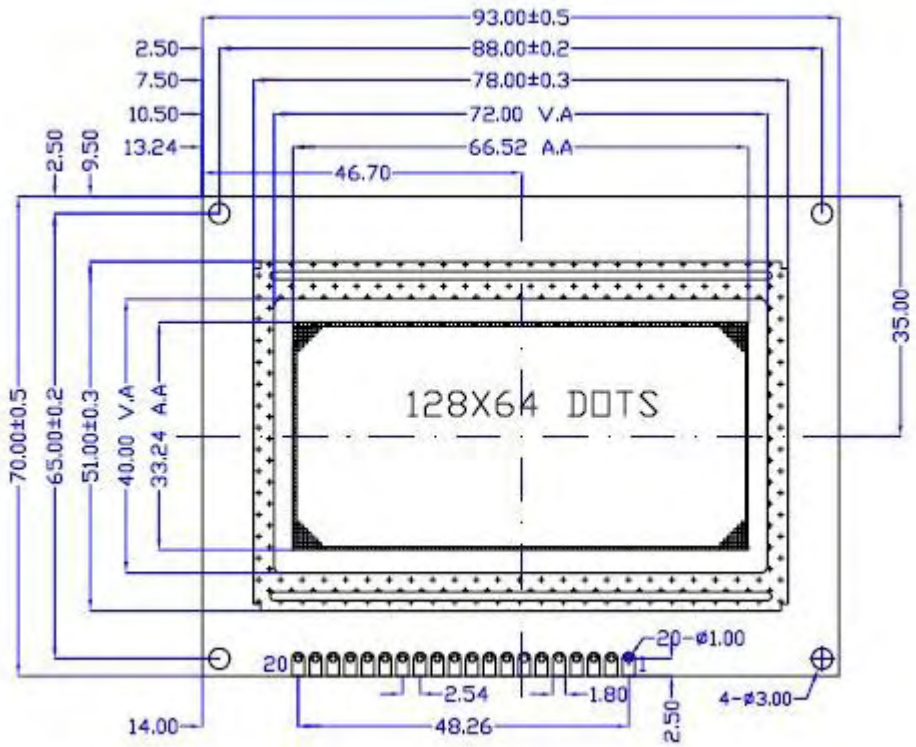


Output PAD: CL1, CL2, M, D



I/O PAD: DB0 – DB7

Digole 12864ZW Module



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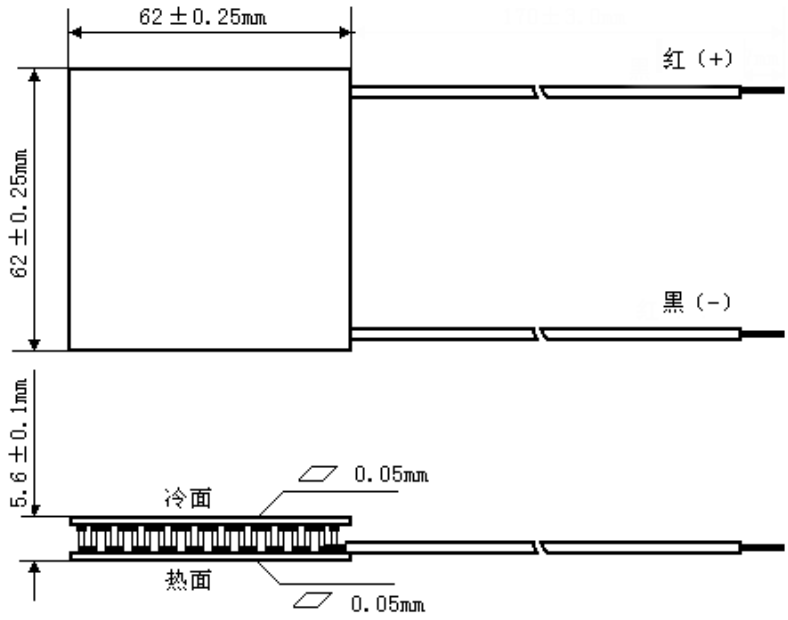
URL: www.everredtronics.com E-mail: sales@everredtronics.com

SPECIFICATIONS

Thermoelectric Module: TEC1-12709T125 62*62*5.6mm

1. Dimensions



2. Electrical Parameters

Specifications		Conditions
I_{max}	9.0A	Th=30℃
V_{max}	16.0V	Th=30℃
ΔT_{max}	≥67℃	Qc=0, Th=30℃
Q_{cmax}	80.0W	ΔT=0℃, Th=30℃
T_R	-50~100℃	
Wire	18AWG, Length: 150mm	

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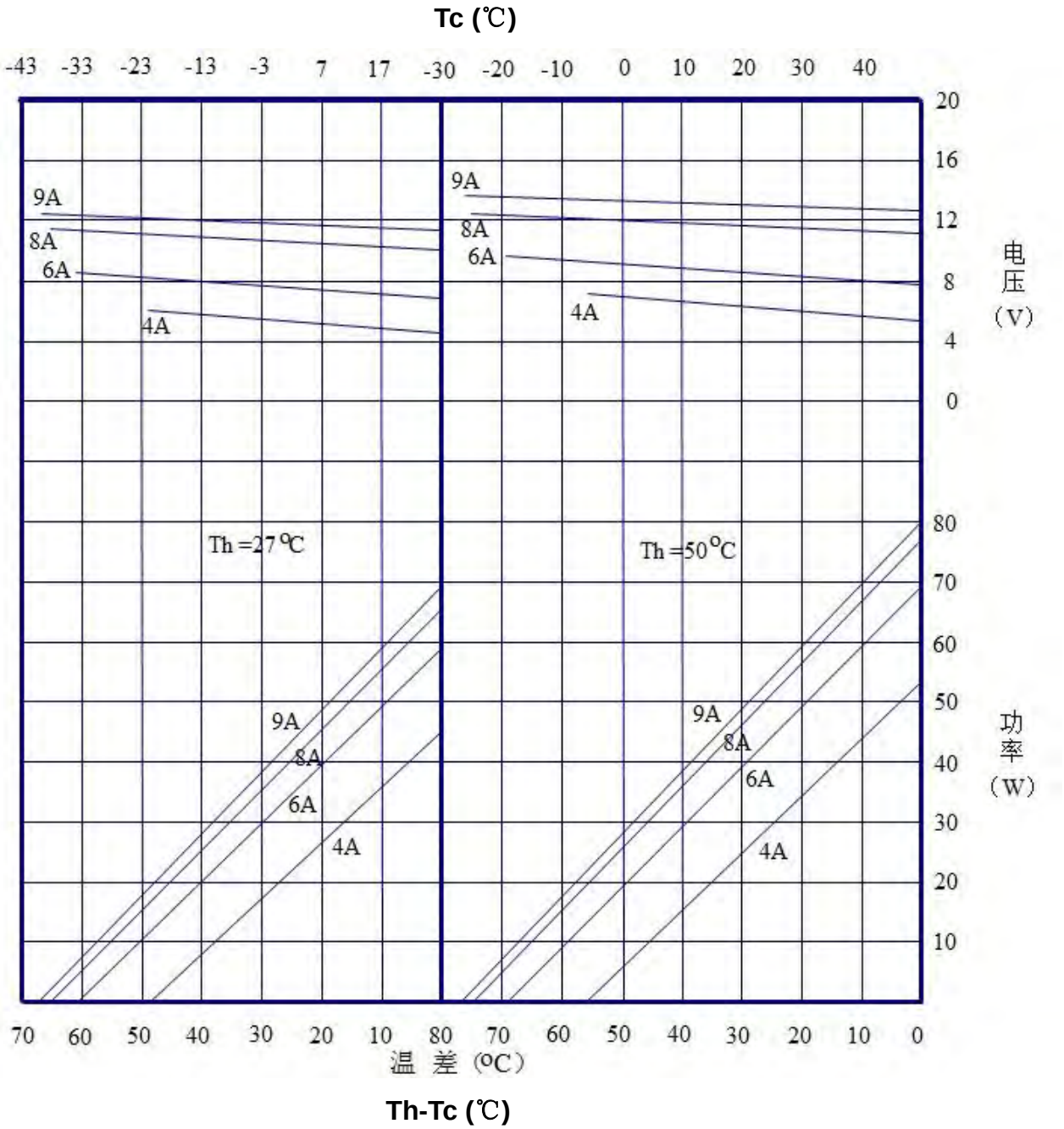
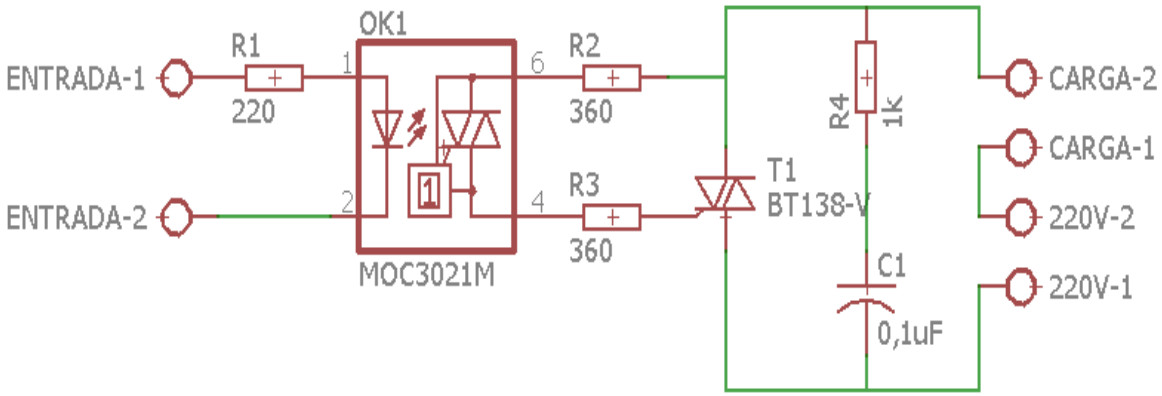
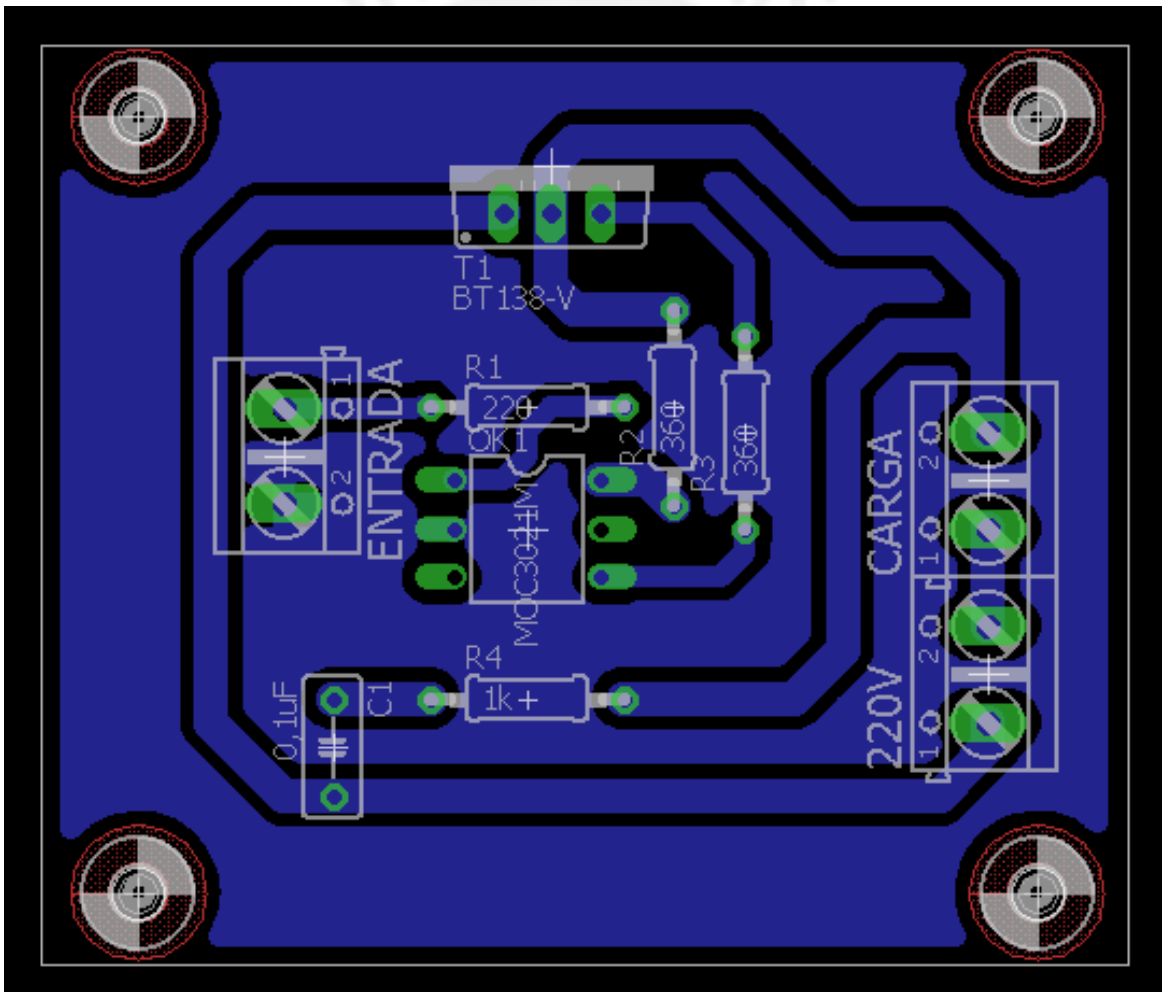
3. Performance Curves



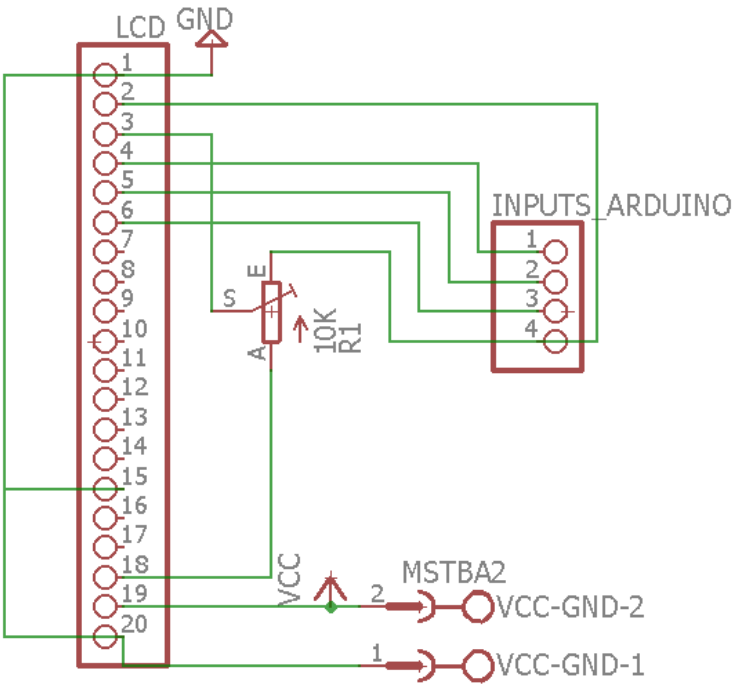
Esquemáticos y circuitos impresos

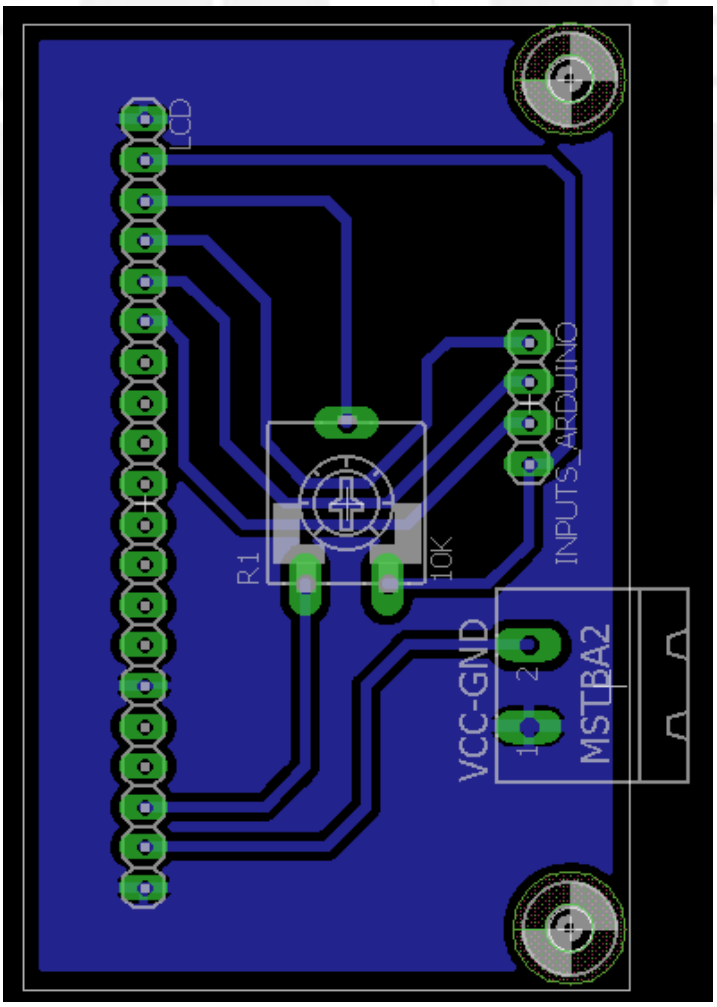
Circuito de Activación de la resistencia



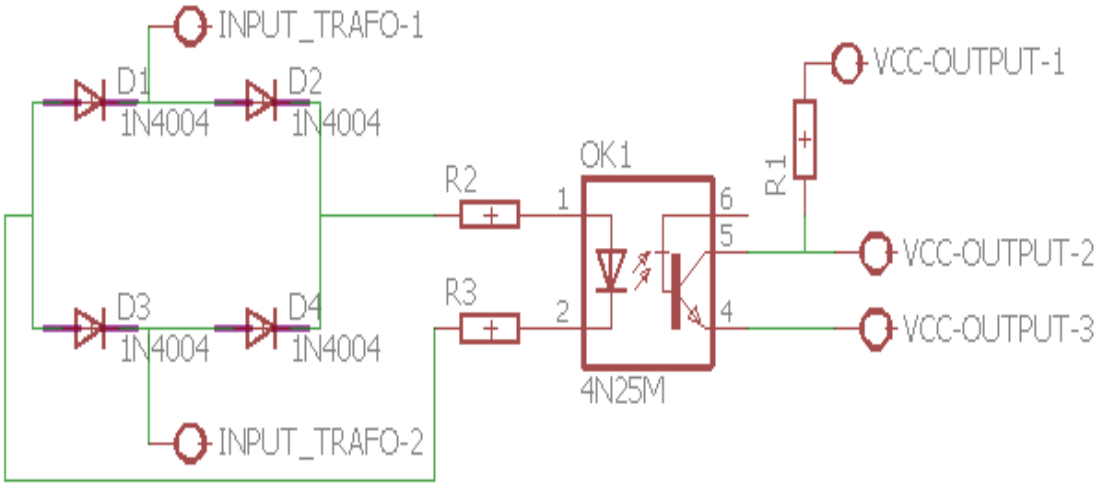


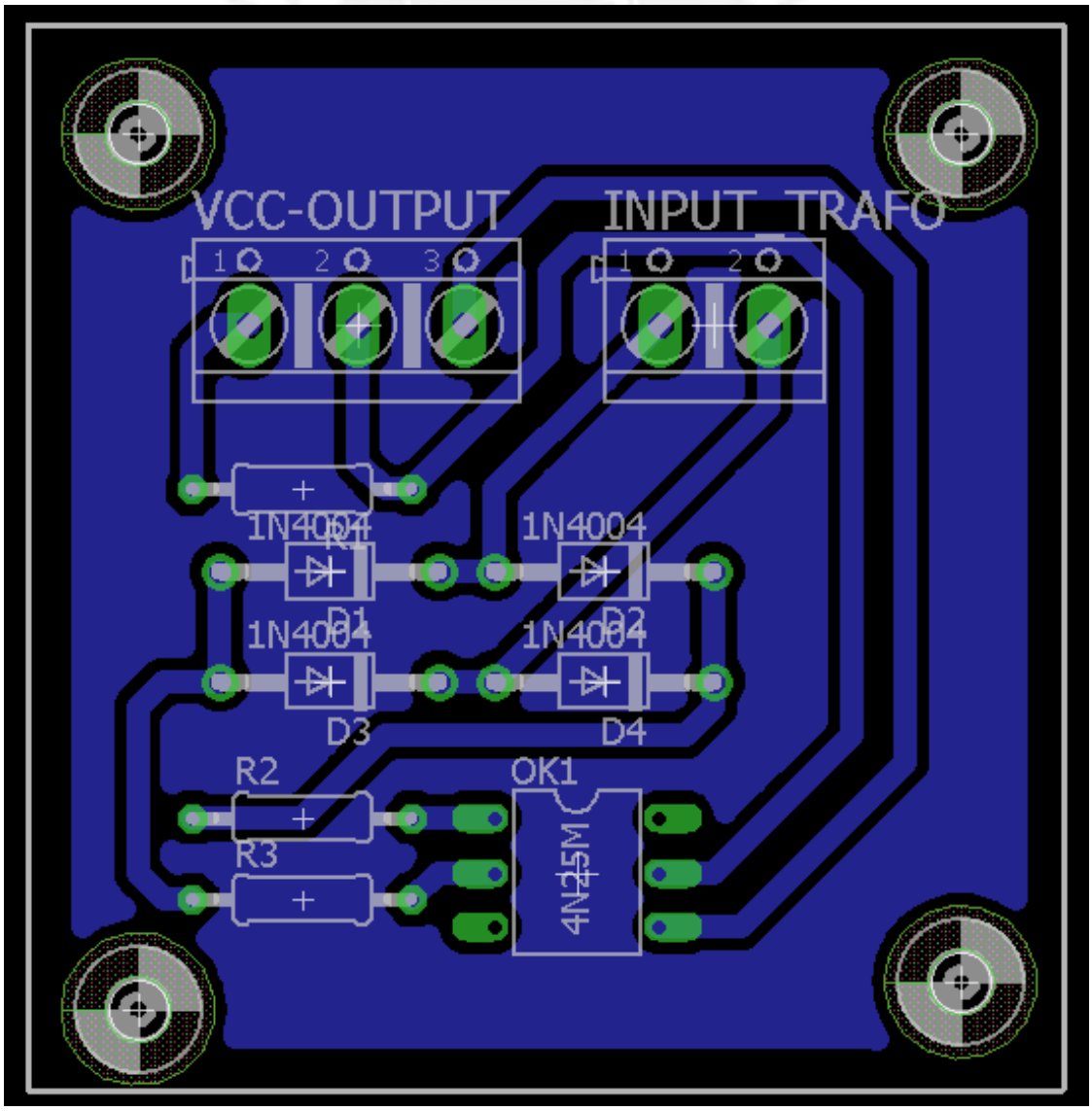
Circuito de la pantalla LCD



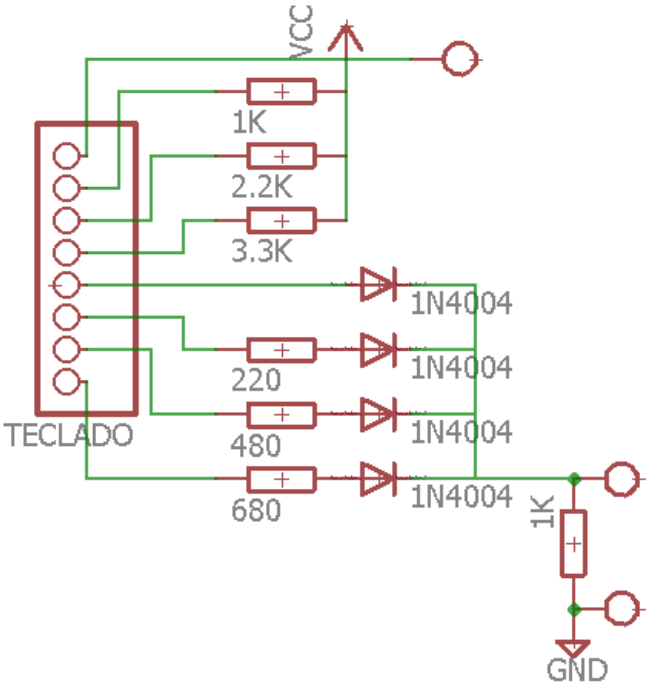


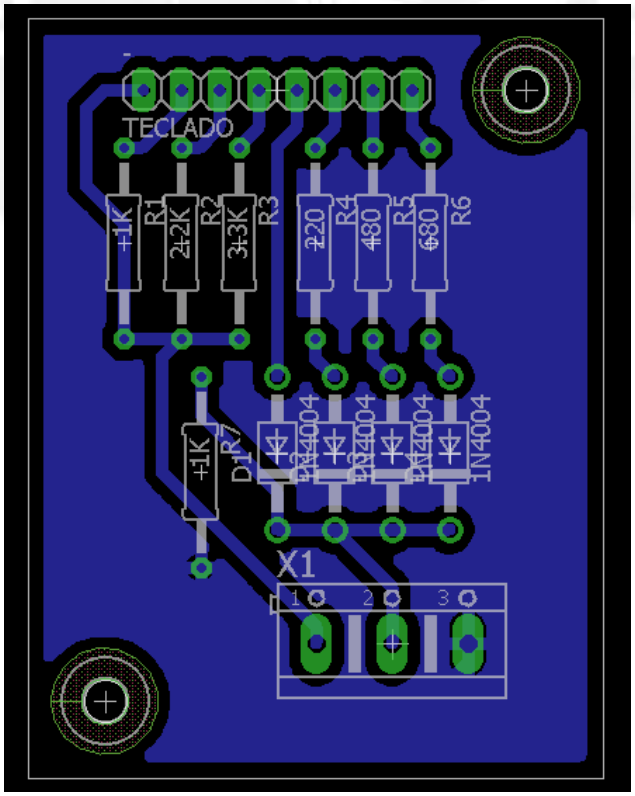
Circuito de cruce por cero



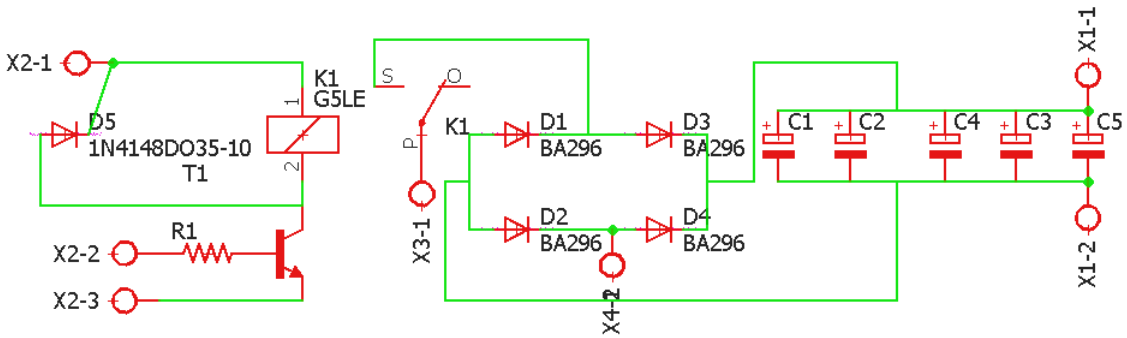


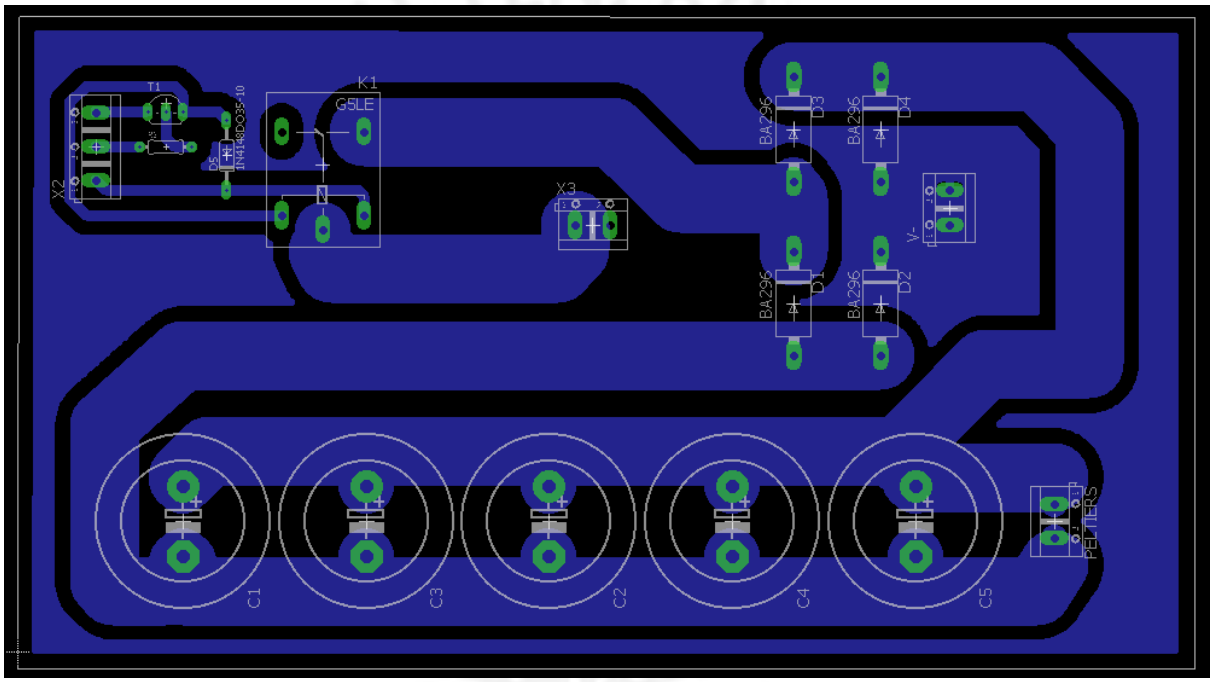
Circuito del teclado matricial



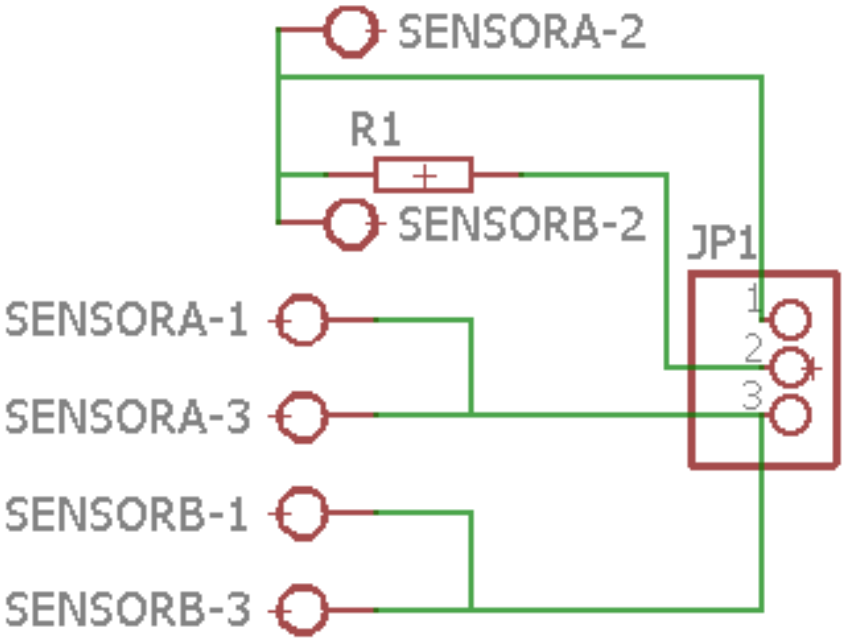


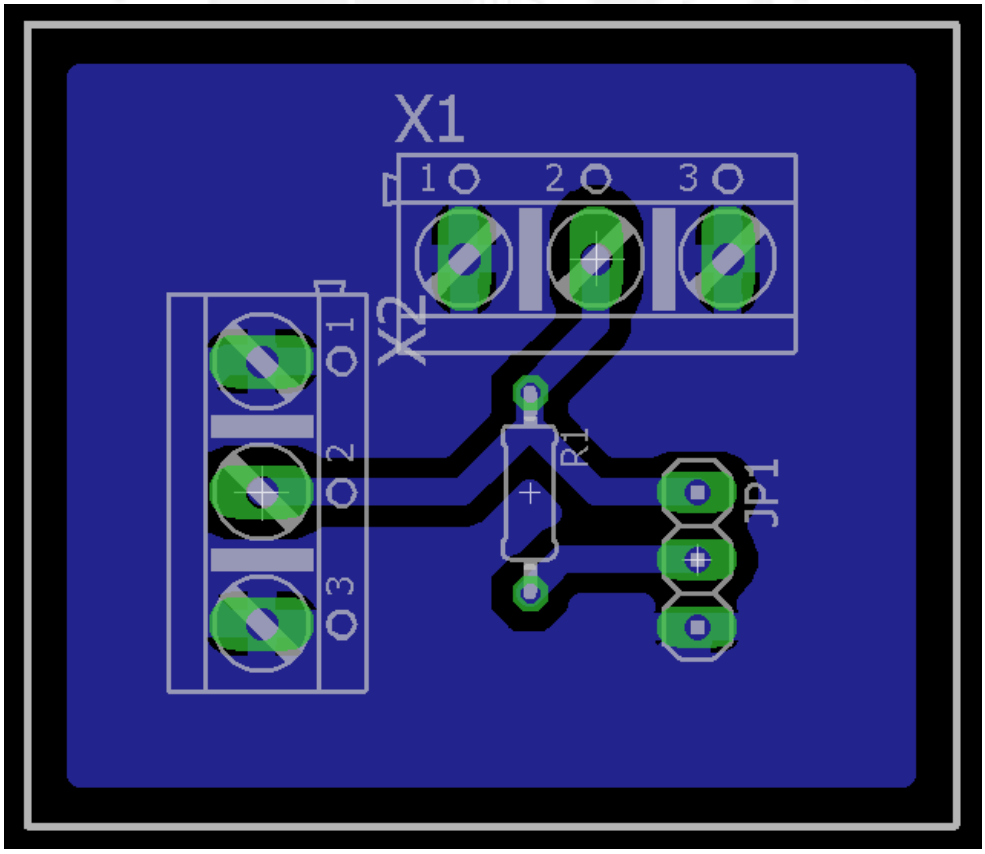
Rectificador de onda completa con filtro para celdas peltier





Circuito para sensores de temperatura DS18B20





Circuito con relés