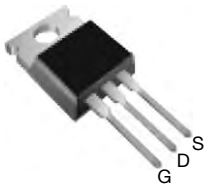
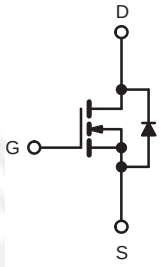
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	100	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.16
Q_g (Max.) (nC)	26	
Q_{gs} (nC)	5.5	
Q_{gd} (nC)	11	
Configuration	Single	

TO-220AB





N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- 175 °C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

Available
RoHS* COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF530PbF
	SiHF530-E3
SnPb	IRF530
	SiHF530

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

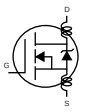
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	100	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	14	A
		T_C = 100 °C		10	
Pulsed Drain Current[a]			I_{DM}	56	
Linear Derating Factor				0.59	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	69	mJ
Repetitive Avalanche Current[a]			I_{AR}	14	A
Repetitive Avalanche Energy[a]			E_{AR}	8.8	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	88	W
Peak Diode Recovery dV/dt[c]			dV/dt	5.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 25 V, starting T_J = 25 °C, L = 528 µH, R_g = 25 Ω, I_{AS} = 14 A (see fig. 12).
c. I_{SD} ≤ 14 A, dI/dt ≤ 140 A/µs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.7	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	100	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.12	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	-	-	25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 150 °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 8.4 A[b]	-	-	0.16	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 8.4 A[b]	5.1	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	670	-	pF
Output Capacitance	C_{oss}		-	250	-	
Reverse Transfer Capacitance	C_{rss}		-	60	-	
Total Gate Charge	Q_g	V_{GS} = 10 V; I_D = 14 A, V_{DS} = 80 V, see fig. 6 and 13[b]	-	-	26	nC
Gate-Source Charge	Q_{gs}		-	-	5.5	
Gate-Drain Charge	Q_{gd}		-	-	11	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 14 A, R_g = 12 Ω, R_D = 3.6 Ω, see fig. 10[b]	-	10	-	ns
Rise Time	t_r		-	34	-	
Turn-Off Delay Time	$t_{d(off)}$		-	23	-	
Fall Time	t_f		-	24	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	14	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	56	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 14 A, V_{GS} = 0 V[b]	-	-	2.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 14 A, dI/dt = 100 A/µs[b]	-	150	280	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	0.85	1.7	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

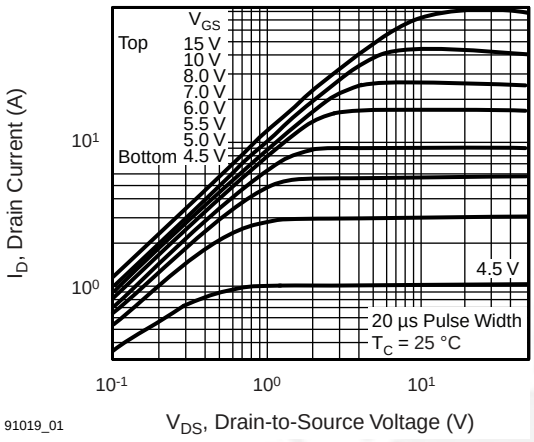


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

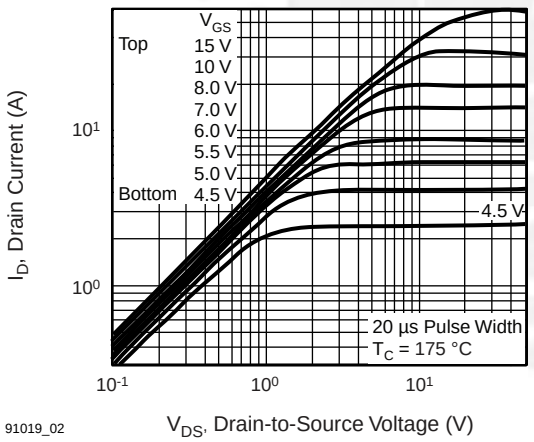


Fig. 2 - Typical Output Characteristics, T_C = 175 °C

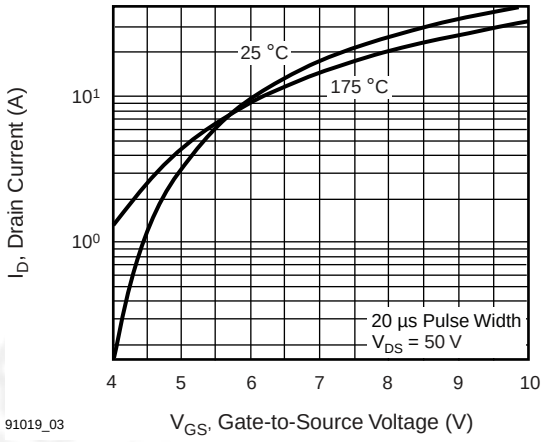


Fig. 3 - Typical Transfer Characteristics

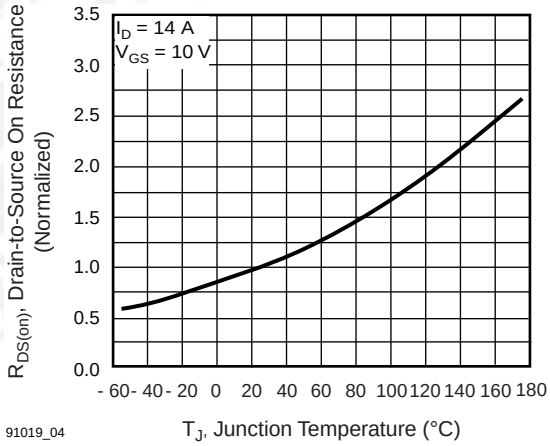


Fig. 4 - Normalized On-Resistance vs. Temperature

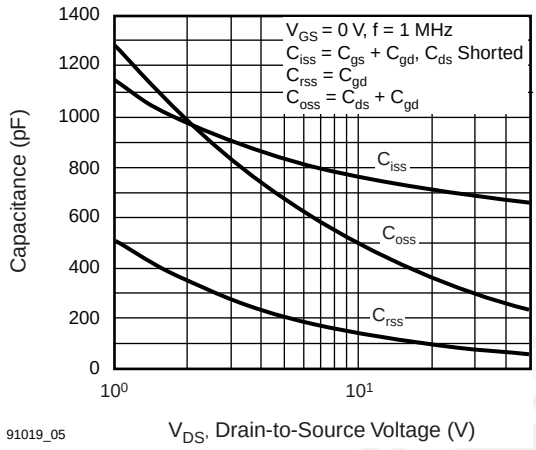


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

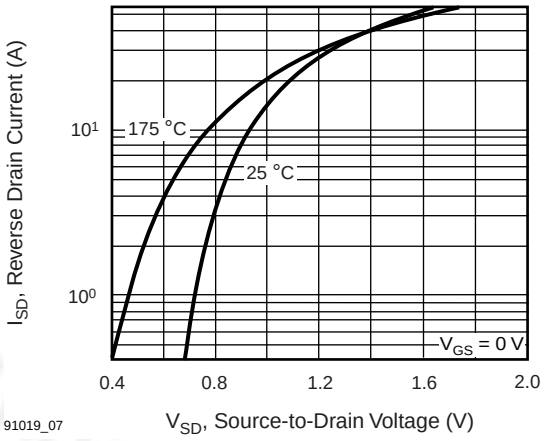


Fig. 7 - Typical Source-Drain Diode Forward Voltage

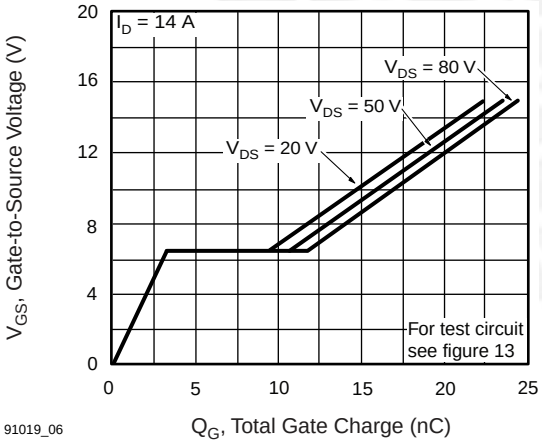


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

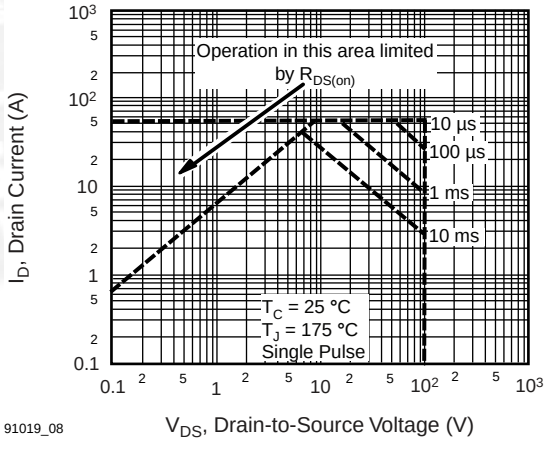


Fig. 8 - Maximum Safe Operating Area

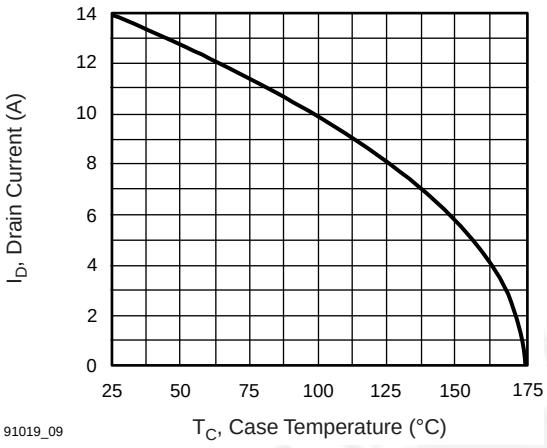


Fig. 9 - Maximum Drain Current vs. Case Temperature

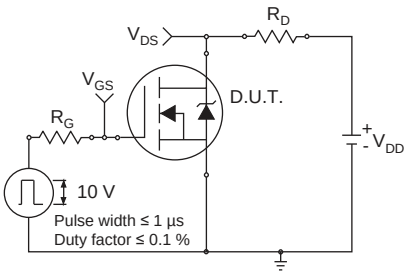


Fig. 10a - Switching Time Test Circuit

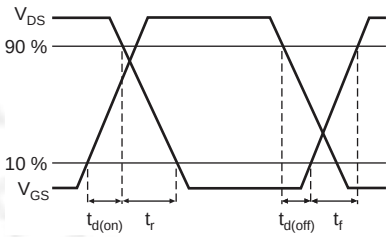


Fig. 10b - Switching Time Waveforms

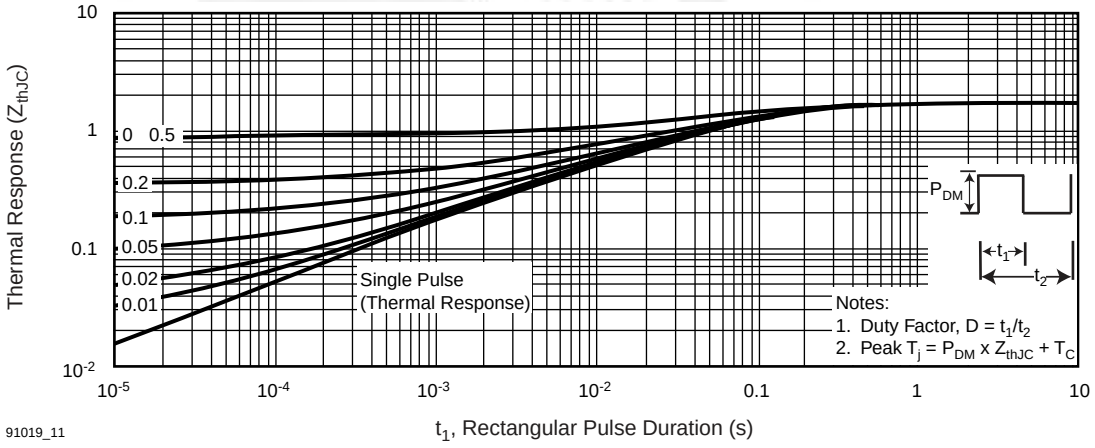


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

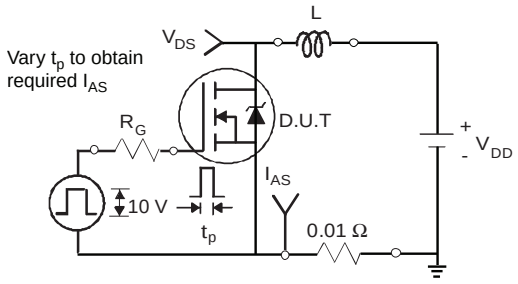


Fig. 12a - Unclamped Inductive Test Circuit

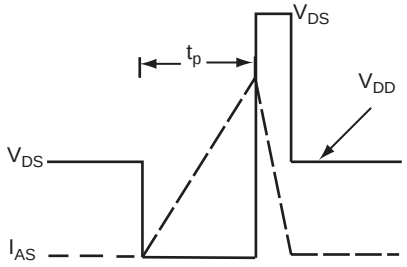


Fig. 12b - Unclamped Inductive Waveforms

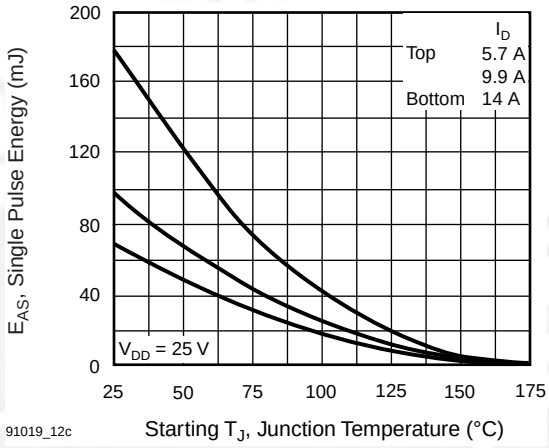


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

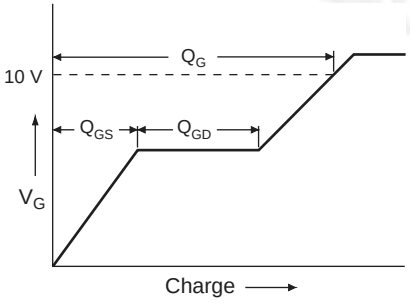


Fig. 13a - Basic Gate Charge Waveform

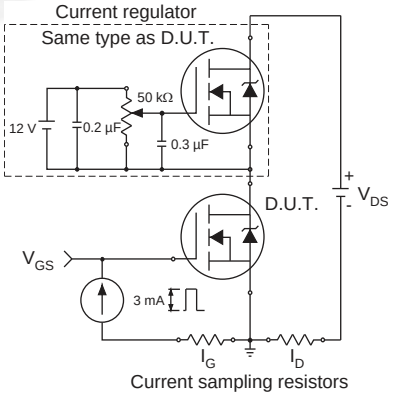
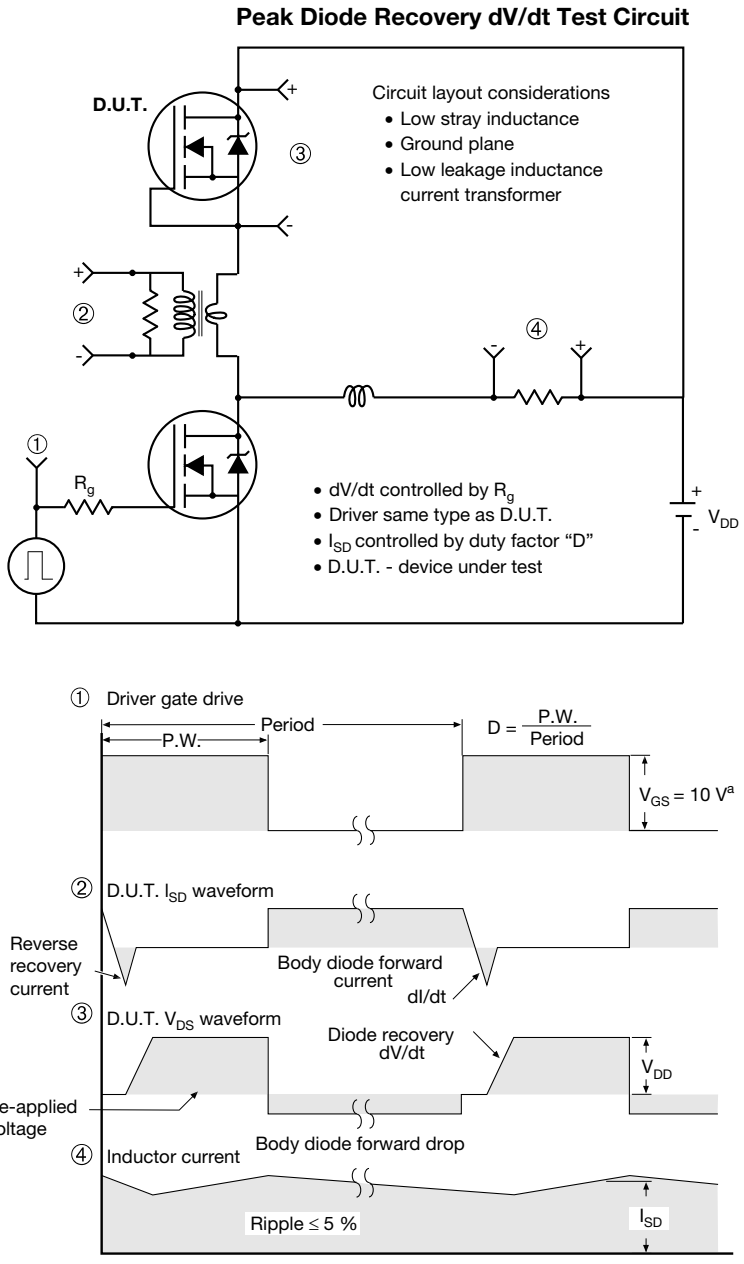


Fig. 13b - Gate Charge Test Circuit



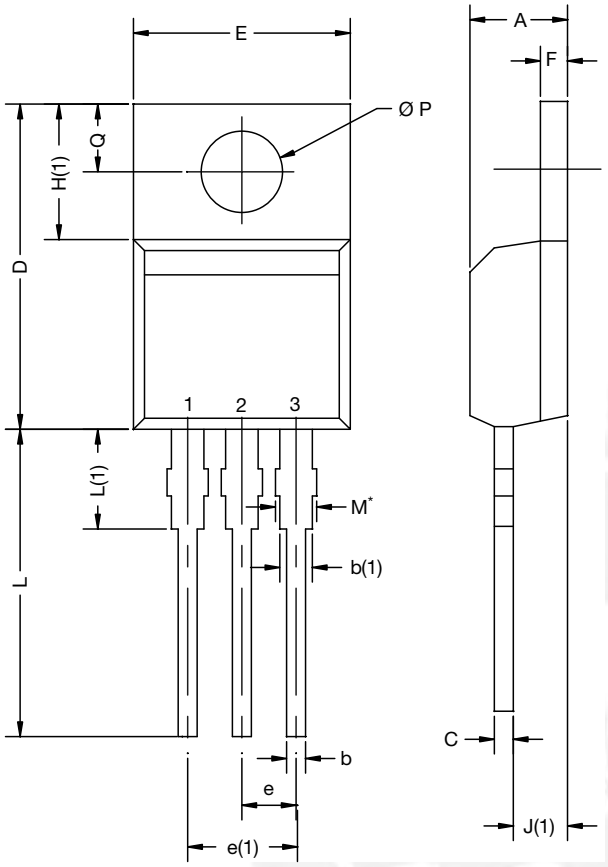
Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91019.

TO-220-1

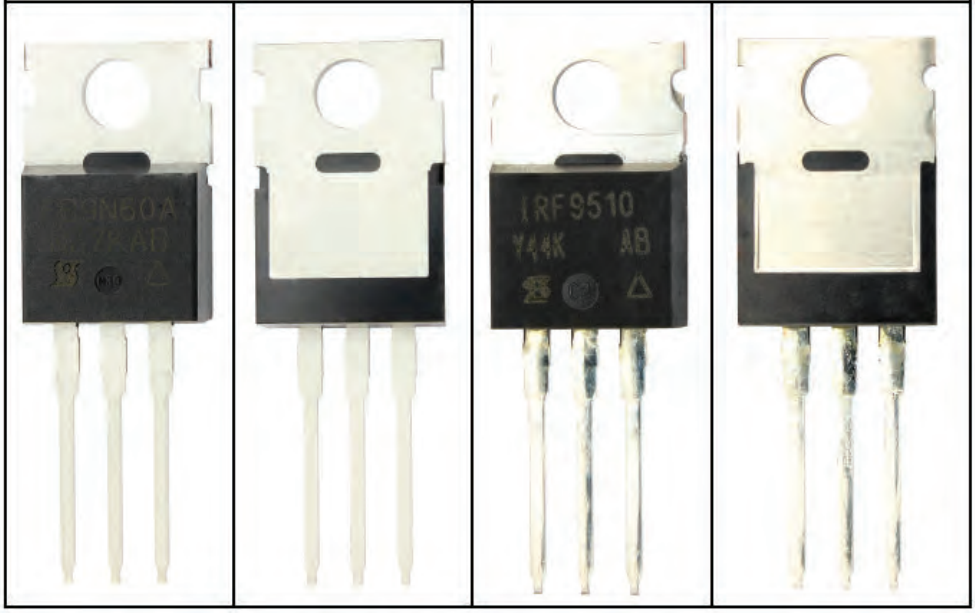


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118
ECN: X15-0364-Rev. C, 14-Dec-15 DWG: 6031				

Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

Package Picture	
ASE	Xi'an



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Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

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Radio Receiver Included

Mega ARM Tower

Models:

MADCBB, MATDCBB, MASDCBB & MASTDCBB

(MEGA ARM, MEGA ARM TOWER, MEGA SPRINT & MEGA SPRINT TOWER)

1/2 HP COMMERCIAL DUTY PARKING GATE OPERATOR

INSTALLATION AND SERVICE MANUAL

IMPORTANT: Read and understand Warranty Page first.
Batteries (included) MUST be connected for proper operation of unit.
Use (2) LiftMaster 12Vdc 7AH (Part # MBAT).

TABLE OF CONTENTS

INTRODUCTION

⚠ WARNING

Mechanical

⚠ WARNING

Electrical

CAUTION

When you see these Safety Symbols and Signal Words on the following pages, they will alert you to the possibility of ***serious injury*** or ***death*** if you do not comply with the warnings that accompany them. The hazard may come from something mechanical or from electric shock. Read the warnings carefully.

When you see this Signal Word on the following pages, it will alert you to the possibility of damage to your gate and/or the gate operator if you do not comply with the cautionary statements that accompany it. Read them carefully.

IMPORTANT NOTE

- BEFORE attempting to install, operate or maintain the operator, you must read and fully understand this manual and follow all safety instructions.
- DO NOT attempt repair or service of your commercial door and gate operator unless you are an Authorized Service Technician.

TOOLS NEEDED FOR INSTALLATION

During assembly, installation and adjustment of the operator the tools listed below may be needed.

- Wrench or Socket Set
- Phillips Head Screwdriver
- C Clamps
- Level
- Small Screwdriver
- T25 Torx Head Screwdriver

UNIT OVERVIEW

The LiftMaster model MEGA ARM barrier style parking gate operator is unique in the industry. Setting the MEGA ARM apart are many features that make it the front runner in its class:

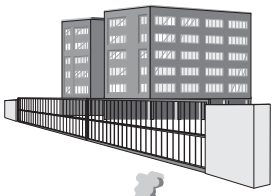
- Built in battery run - inherent 24 Vdc backup power with regulated 24 Vdc for accessories.
- High torque 24 volt Permanent Magnet DC motor.
- Full service controller with eight inputs and LED indicators for loops, card reader, radio, etc.
- Reversible arm direction for right or left handed operation.
- Instant Reverse Device (IRD) monitor senses obstructions during motion.
- Automatic open of gate arm when power is lost if desired (with 15 sec. delay selection).
- Raise gate input memory will memorize multiple vehicles – ideal for bar code scanners and AVI.
- Ability to STOP arm in close travel if tail-gating is sensed at close loop.
- Anti-tail gate alarm - fires K1 relay to trigger a warning device when tail-gating is sensed.
- SAMS with “memory” - allows Mega Arm to open a slide/swing gate first then raises arm.
- Break away mount design for the 12-15' x 3" tubular aluminum boom arm.
- Dynamic motor braking to preserve arm positioning.
- All rust proof aluminum construction with white powder coat baked on enamel.
- Molded Polyethylene UV stabilized cover never needs wax or paint (excludes towers).
- Direct drive gear reducer eliminates many parts that might otherwise fail.
- State of the art MOSFET motor drive technology, NO contactors or relays.
- Soft start and stop in open and close travel motions.
- No limit switches to fail - uses magnetic (Hall Effect) sensors to monitor arm position.
- Maximum Run Timer for motor with anti-tamper protection in closing direction.
- Each unit configurable as master or second operator.
- Safe 24 Vdc low voltage motor and control wiring.
- LED diagnostics for easy trouble shooting.
- Closing timer adjustable from 1-31 seconds with on/off selection.
- Transient voltage protection on all inputs.
- Capable of being powered from 120 or 230 Vac, or UL Listed Class 2 Solar Power.
- On 120 Vac installations, unswitched duplex outlet gives convenient supply for 120 Vac accessories.
- 10 year perforation warranty on cover and chassis with 2 years on electronics and mechanism.

NOTE: *If the operator is installed in a region where temperatures regularly go below 30˚ F then it is recommended that the optional heater is installed. Refer to the accessory page.*

UL325 MODEL CLASSIFICATIONS

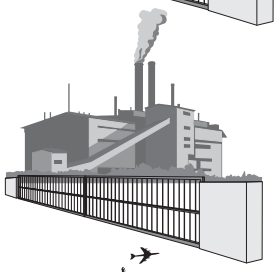
CLASS I – RESIDENTIAL VEHICULAR GATE OPERATOR

A vehicular gate operator (or system) intended for use in a home of one-to four single family dwellings, or a garage or parking area associated therewith.



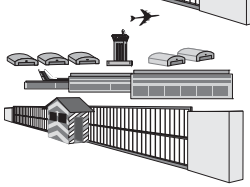
CLASS II – COMMERCIAL/GENERAL ACCESS VEHICULAR GATE OPERATOR

A vehicular gate operator (or system) intended for use in a commercial location or building such as a multi-family housing unit (five or more single family units) hotel, garage, retail store or other building servicing the general public.



CLASS III – INDUSTRIAL/LIMITED ACCESS VEHICULAR GATE OPERATOR

A vehicular gate operator (or system) intended for use in a industrial location or building such as a factory or loading dock area or other location not intended to service the general public.



CLASS IV – RESTRICTED ACCESS VEHICULAR GATE OPERATOR

A vehicular gate operator (or system) intended for use in a guarded industrial location or building such as an airport security area or other restricted access locations not servicing the general public, in which unauthorized access is prevented via supervision by security personnel.

SAFETY ACCESSORY SELECTION

All UL325 compliant LiftMaster gate operators will accept external entrapment protection devices to protect people from motorized gate systems. UL325 requires that the type of entrapment protection correctly matches each gate application. Below are the six types of entrapment protection systems recognized by UL325 for use on this operator.

ENTRAPMENT PROTECTION TYPES

Type A: Inherent obstruction sensing system, self-contained within the operator. This system must sense and initiate the reverse of the gate within two seconds of contact with a solid object.

Type B1: Connections provided for a non-contact device, such as a photoelectric eye can be used as a secondary protection.

Type B2: Connections provided for a contact sensor. A contact device such as a gate edge can be used for secondary protection.

Type C: Inherent adjustable clutch or pressure relief valve.

Type D: Connections provided for a control requiring continuous pressure to operate the operator open and close.

Type E: Built-in audio alarm. Examples include sirens, horns or buzzers.

NOTE: *UL requires that all installations must have warning signs placed in plain view on both sides of the gate to warn pedestrians of the dangers of motorized gate systems.*

UL325 ENTRAPMENT PROTECTION REQUIREMENTS

GATE OPERATOR ENTRAPMENT PROTECTION

UL325 Installation Class	Slide Gate Operator		Swing & Gate Barrier (Arm) Operator	
	Primary Type	Secondary Type	Primary Type	Secondary Type
Class I & II	A	B1, B2 or D	A or C	A, B1, B2, or C
Class III	A, B1 or B2	A, B1, B2, D or E	A, B1, B2 or C	A, B1, B2, C, D or E
Class IV	A, B1, B2 or D	A, B1, B2, D or E	A, B1, B2, C or D	A, B1, B2, C, D or E

The chart above illustrates the entrapment protection requirements for each of the four UL325 classes.

In order to complete a proper installation you must satisfy the entrapment protection chart shown above. That means that the installation must have one primary means of entrapment protection and one independent secondary means of entrapment protection. Both primary and secondary entrapment protection methods must be designed, arranged or configured to protect against entrapments in both the open and close directions of gate travel.

For Example: For a slide gate system that is installed on a single-family residence (UL325 Class I) you must provide the following: As your primary type of entrapment protection you must provide Type A inherent (built into the operator) entrapment sensing and at least one of the following as your secondary entrapment protection: Type B1- Non-contact sensors such as photoelectric eyes, Type B2- Contact sensors such as gate edges or Type D- Constant pressure control.

SAFETY INSTALLATION INFORMATION

1. Vehicular gate systems provide convenience and security. Gate systems are comprised of many component parts. The gate operator is only one component. Each gate system is specifically designed for an individual application.

2. Gate operating system designers, installers and users must take into account the possible hazards associated with each individual application. Improperly designed, installed or maintained systems can create risks for the user as well as the bystander. Gate systems design and installation must reduce public exposure to potential hazards.

3. A gate operator can create high levels of force in its function as a component part of a gate system. Therefore, safety features must be incorporated into every design. Specific safety features include:
   - Gate Edges
   - Guards for Exposed Rollers
   - Photoelectric Sensors
   - Screen Mesh
   - Vertical Posts
   - Instructional and Precautionary Signage

4. Install the gate operator only when:
   a. The operator is appropriate for the construction and the usage class of the gate.
   b. All openings of a horizontal slide gate are guarded or screened from the bottom of the gate to a minimum of 4' (1.2 m) above the ground to prevent a 2 1/4" (6 cm) diameter sphere from passing through the openings anywhere in the gate, and in that portion of the adjacent fence that the gate covers in the open position.
   c. All exposed pinch points are eliminated or guarded, and guarding is supplied for exposed rollers.

5. The operator is intended for installation only on gates used for vehicles. Pedestrians must be supplied with a separate access opening. The pedestrian access opening shall be designed to promote pedestrian usage. Locate the gate such that persons will not come in contact with the vehicular gate during the entire path of travel of the vehicular gate.

6. The gate must be installed in a location so that enough clearance is supplied between the gate and adjacent structures when opening and closing to reduce the risk of entrapment. Swinging gates shall not open into public access areas.

7. The gate must be properly installed and work freely in both directions prior to the installation of the gate operator.

8 Controls intended for user activation must be located at least six feet (6') away from any moving part of the gate and where the user is prevented from reaching over, under, around or through the gate to operate the controls. Outdoor or easily accessible controls shall have a security feature to prevent unauthorized use.

9. The Stop and/or Reset (if provided separately) must be located in the line-of-sight of the gate. Activation of the reset control shall not cause the operator to start.

10. A minimum of two (2) WARNING SIGNS shall be installed, one on each side of the gate where easily visible.

11. For a gate operator utilizing a non-contact sensor:
    a. Reference owner's manual regarding placement of non-contact sensor for each type of application.
    b. Care shall be exercised to reduce the risk of nuisance tripping, such as when a vehicle trips the sensor while the gate is still moving.
    c. One or more non-contact sensors shall be located where the risk of entrapment or obstruction exists, such as the perimeter reachable by a moving gate or barrier.

12. For a gate operator utilizing a contact sensor such as an edge sensor:
    a. One or more contact sensors shall be located where the risk of entrapment or obstruction exists, such as at the leading edge, trailing edge and post mounted both inside and outside of a vehicular horizontal slide gate.
    b. One or more contact sensors shall be located at the bottom edge of a vehicular vertical lift gate.
    c. A hard wired contact sensor shall be located and its wiring arranged so the communication between the sensor and the gate operator is not subject to mechanical damage.
    d. A wireless contact sensor such as the one that transmits radio frequency (RF) signals to the gate operator for entrapment protection functions shall be located where the transmission of the signals are not obstructed or impeded by building structures, natural landscaping or similar obstruction. A wireless contact sensor shall function under the intended end-use conditions.
    e. One or more contact sensors shall be located on the inside and outside leading edge of a swing gate. Additionally, if the bottom edge of a swing gate is greater than 6" (152 mm) above the ground at any point in its arc of travel, one or more contact sensors shall be located on the bottom edge.
    f. One or more contact sensors shall be located at the bottom edge of a vertical barrier (arm).

INSTALLATION

CONCRETE PAD

The concrete pad for operator mounting should be approximately 24"x24"x24" in order to provide adequate weight and structure to insure proper and stable operation. Pad should be 6" above finished grade or even with top of curb if one is present. ***(NOTE:*** *Pad should always extend below frost line in regions where ground will freeze.)*

ANCHORS (MOUNTING UNIT)

Proper anchors for fastening operator to pad will be a 1/2"x6" wedge anchor patterned to match the mounting base of the unit. They should be installed with approximately 1 1/4" showing above concrete surface in order to allow for the 1/2" thick base plate as well as washers for leveling.

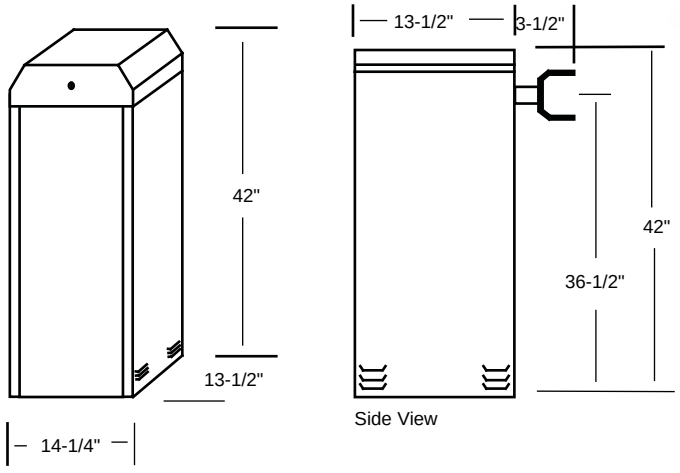
NOTES:

- *For automotive use only, no motorcycles, bicycles or pedestrians.*
- *Heater option MUST be used if temperature is 30°or below.*
- *Heater option available for 120 Vac units only. See accessory page for heater part number.*

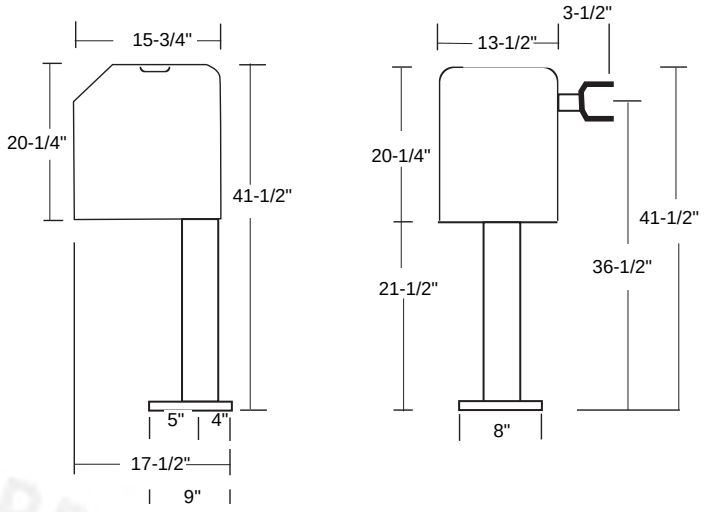
CONDUITS

Conduits should be restricted to fit the 3 1/2"x3 1/2" opening in pedestal base and 10 1/4" x 8 1/4" for the tower base. Location on pad should be centered and spaced approximately 6" from edge of pad on drive way side (in order to get the most reach out of arm). Separate conduits to be included should be 120/230 Vac main power, low voltage control wiring and one or two extra for loop sensor leads. Conduit size should be limited to 1/2" when possible to reduce crowding if more than four are needed. All conduits must be UL approved.

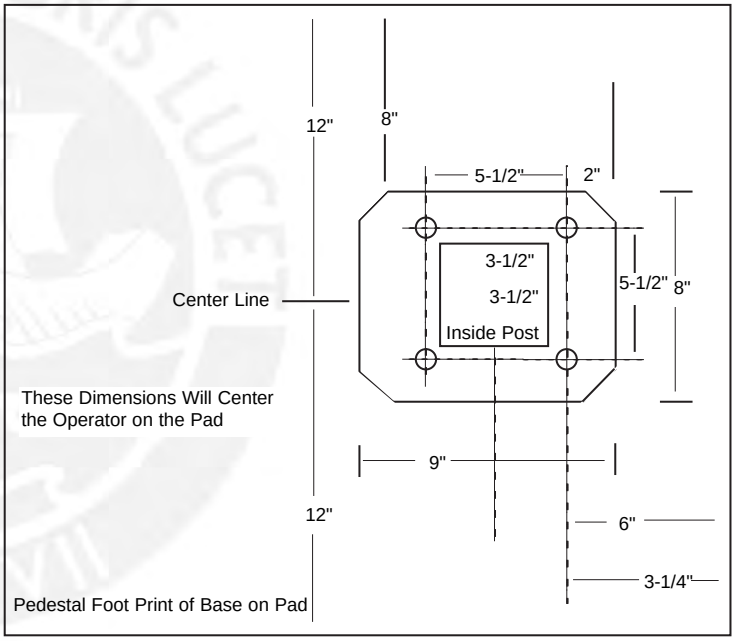
TOWER CABINET DIMENSIONS



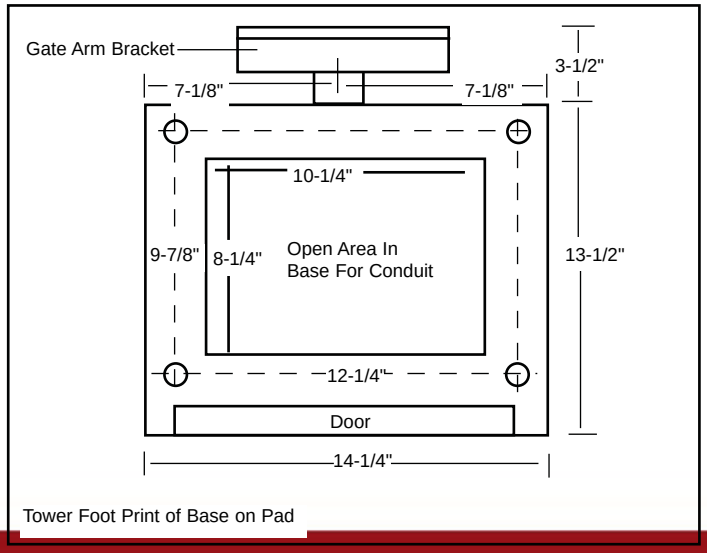
UNIT DIMENSIONS



Pad (24"x24")



Pad (24" x 24" x 24")



WIRING AND HOOKUP

⚠ WARNING

To reduce the risk of SEVERE INJURY or DEATH:

- ANY maintenance to the operator or in the area near the operator MUST not be performed until disconnecting the electrical power and locking-out the power via the operator power switch. Upon completion of maintenance the area MUST be cleared and secured, at that time the unit may be returned to service.
- Disconnecting power at the fuse box BEFORE proceeding. Operator MUST be properly grounded and connected in accordance with local electrical codes. ***NOTE:*** *The operator should be on a separate fused line of adequate capacity.*
- ALL electrical connections MUST be made by a qualified individual.
- DO NOT install any wiring or attempt to run the operator without consulting the wiring diagram. We recommend that you Install an optional reversing edge BEFORE proceeding with the control station installation.
- ALL power wiring should be on a dedicated circuit and well protected. The location of the power disconnect should be visible and clearly labeled.
- ALL power and control wiring MUST be run in separate conduit.
- BEFORE installing power wiring or control stations be sure to follow all specifications and warnings described below. Failure to do so may result in SEVERE INJURY to persons and/or damage to operator.

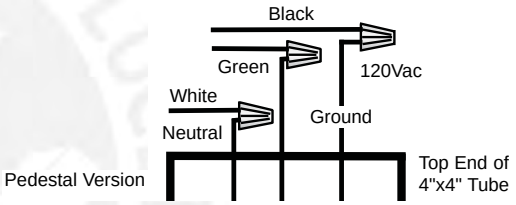
AC POWER HOOKUP (120/230 Vac)

Be sure your main power is OFF before attempting to hook up the AC power. The AC wiring should be attached to the wires exiting the conduit or pedestal post. Only use U.L. approved 14AWG (or larger) 600 volt insulated wire.

NOTE: *Do not connect any of the AC power wires directly to the electronic control board. Connect the batteries after the AC power is restored.*

120 Vac

Connect the BLACK wire to the incoming 120 Vac hot lead and connect the WHITE wire to the incoming neutral lead. Connect the GREEN wire to the ground.



120 Vac

230 Vac

Please purchase the 120 to 230 Vac conversion kit for 230 Vac operation. See Accessory page.

INPUT COMMANDS CONNECTIONS

Use common and normally open contacts from devices connected to these inputs. Control wire connections at low voltage terminal strip will be at the top of the electronic control board. Make connections to the appropriate points for the desired operation, see Control Board Layout page 18. Wires should be UL approved 600 volt rated and at least 18 AWG. They are to be routed through the upper grommet in chassis to avoid chafing. All external control devices must have normally open dry contacts.

CAUTION: DO NOT CONNECT ANY DEVICE WHICH WOULD DELIVER ANY VOLTAGE OF ANY KIND TO THESE TERMINALS.

Terminals 9, 10, 11, 12 are the commons (0 Vdc) used to activate the following inputs:

1, 2, 3 OPEN: These inputs will trigger gate open when pulsed or hold gate open with maintained contact. When released gate will close if closing timer is on or if close input is given.

4, AUXILIARY OPEN: Same as 1, 2 and 3 with S2 switch 6 off. With S2 switch 6 on, this input will memorize multiple vehicles and not allow gate to close until the final vehicle in memory crosses the close loop. Use with laser scanners or card readers and (transmitters with timed anti-pass back). With S1 switch 5 on, this input becomes a momentary **pulse open, pulse close.**

5, SAFETY: This input is generally not used with the MEGA ARM. If used its function is to make gate reverse and go back to the open position if it was closing. Input is disabled when gate is closed.

6, CLOSE: When used with a vehicle detector, it is recommended that the presence contacts (N.O. & C.) be used for the close input. This input will close gate after input is applied and then removed. It will stop the open cycle and reverse gate to close. (Example: Car crosses over close loop before arm reaches full open position- gate will reverse and close). *(**NOTE:** The close input also acts as a safety-stop in that if gate is closing and a tailgater is sensed at the close input, the gate WILL STOP its closing motion and not continue to close until the close input is removed or gate is re-opened).*

7, BACK-AWAY (FREE EXIT INPUT): This input is used as a free exit input to open gate. When input is active, gate will open and close immediately once input is removed. (EXAMPLE: Car pulls up to exit loop, gate opens; car "backs-away" from exit loop and gate closes).

8, SHADOW (SAMS): Used to monitor an auxiliary open limit switch of another operator in the same lane. SAMS with memory feature, see page 18.

9, 10, 11,12 - COMMON: These are the commons (0 Vdc) to be used to activate above inputs.

NOTE: *Above inputs are tied to LED indicators to show input command activity.*

ACCESSORY AND RELAY CONNECTIONS

These terminals will provide battery backed power to 24 Vdc devices and are located at the bottom of the electronic control board at J4 terminals 1 and 2. Terminal 1 is 24 Vdc (+) and number 2 is 0 Vdc (-). Peripheral CLASS 2 low voltage devices that require 24 Vdc power maybe connected here (500 ma. maximum). EXAMPLE: Vehicle detector, radio receiver.

RELAY OUTPUT K1 - (OPTION)

S1-6 off S1-8 off, relay will fire (latch) when gate is not closed.

S1-6 on S1-8 off, relay will fire when arm is pushed up off of limit switch (use with slip clutch option) and fires relay when a tail-gate is detected by the close loop - ANTI TAIL-GATE ALARM.

S1-6 off S1-8 on, relay will pulse relay when arm reaches full open position.

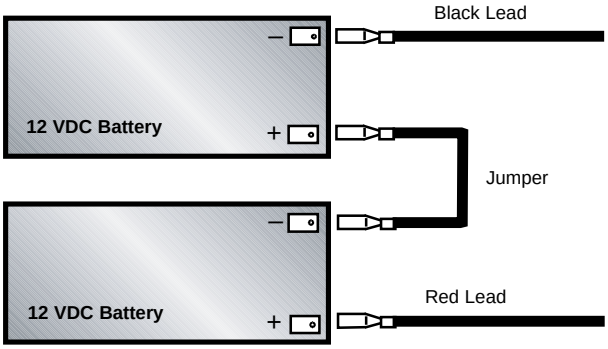
S1-6 on S1-8 on, relay will only pulse when input is given to J5 1,2,3 inputs. (see page 10).

BATTERY INSTALLATION

HOOKING UP BATTERY LEADS - **ALWAYS HOOKUP AND TURN ON AC POWER BEFORE INSTALLING BATTERIES.** After turning on AC power, install two new, fully charged 12 volt DC batteries on shelf next to motor. Connect red lead from operator to the positive (RED +) terminal of one battery and black lead from the operator to the (BLACK -) terminal of the OTHER battery. Place the supplied jumper between the remaining terminals of each battery if one is not already in place (Figure 1). (Use LiftMaster MBAT or 29-NP712 for replacement batteries.) Replace in pairs.

WARNING: *Do not run operator without installing the batteries.*

FIGURE 1



Failure to install batteries correctly will cause damage and will not be covered by warranty.

MASTER/SECOND WIRING

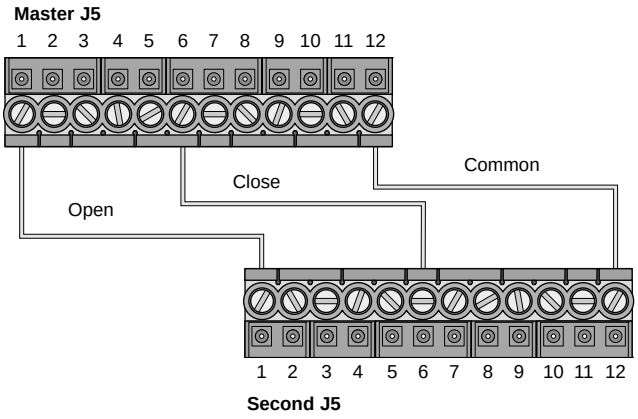
STEP 1: In a master/second configuration, either unit can be the master. Choose one unit to be the master and then direct all control wiring to it (also install vehicle detectors and receivers in it).

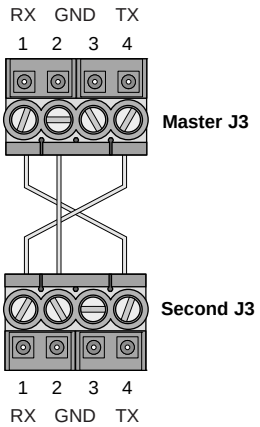
STEP 2: At the MASTER, any input (at J5) with control (detectors, receivers, keypads, timers, etc.) wires to it must also be run to the same terminals of the second. Along with these control wires, both operators MUST share a common ground connection from chassis to chassis (or from common to common, i.e., master gate J5 terminal #12 to second gate J5 terminal #12).

EXAMPLE: If only open and close are used at master then three wires will run between gates (Figure 2).

STEP 3: If it is required that if one gate senses an obstruction, the other reverses also, then 3 additional wires must be run between the master **J3** and second **J3** (Figure 3). These connections are for transmitting IRD (obstruction signals) between both units. This will allow the master or second to inform the other that a closing obstruction has occurred and for it to reverse and open. **SET** switches on **S2**, **1-8** the same on both gates.

FIGURE 2





IRD - Obstruction Signal Connections
Terminal 1 of Master must go to terminal 4 of Second and terminal 1 of Second must go to terminal 4 of Master. Terminal 2 of Master must go to terminal 2 of Second.

REVERSING ARM DIRECTION

REVERSING THE DIRECTION OF THE ARM

The MEGA ARM allows for the "handing" or reversing of the arm's direction of movement in relation to the unit's normal operation. This allows for mounting in tight places or when it is desired to have the arm, when across the driveway, to be in front of the unit or behind the unit when viewed from the traffic flow direction (Figure 1).

WARNING: POWER MUST BE OFF AND NO ARM INSTALLED BEFORE MAKING THESE CHANGES.

STEP 1: Before power up, switch bank S1 switch #7 must be on (Figure 1).

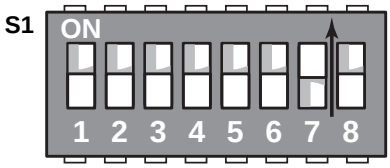
STEP 2: Next, the motor wires on the control board must be reversed. At J4 on the bottom of PCB, the last 2 wires on the right (J4-7, J4-8) normally are blue then orange. They must be reversed to be (J4-7) orange then (J4-8) blue (Figure 2).

STEP 3: After completing the steps above, the cam arm which adjusts the limiting points of the arm's travel must be turned 90 degrees to the left when viewed while standing in front of the control board (Figure 3) (cam arrow now points in the direction of the arm and is level with mount bracket, note the small limit sensors on the back of the PCB).

STEP 4: Now check to make sure that S1 #7 is on (Figure 1), motor wires are reversed, the cam is adjusted, and that the manual open/close switch (S3) is set to close. Next, turn on the AC power and connect the batteries. Now run the gate open and close with the S3 manual switch making sure that the mechanism travels in the proper 90 degrees desired. Once you are totally sure you have the correct operation, you can install the arm

INSTALLATION NOTE: ARMS LONGER THAN 12' MUST USE THE PROPER COUNTER WEIGHT.

FIGURE 1



S1, #7 to be turned ON before power up to enable reverse of arm.

FIGURE 2

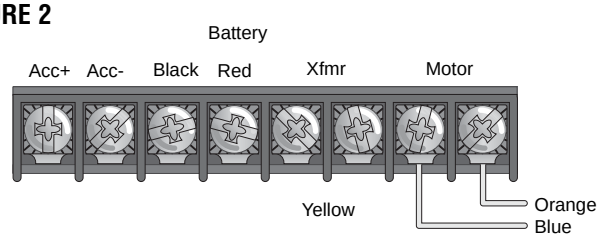
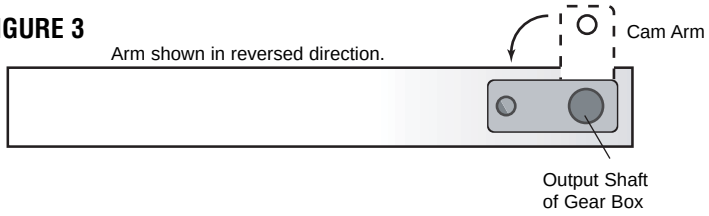


FIGURE 3



TIMERS AND MODE SELECTIONS S1 & S2

MODE SELECTIONS - SWITCH PACK S1 (5-8)

SWITCH 5: ON -Will allow J5 input #4 to operate as a pulse open/pulse close function.

SWITCH 6: ON -Will fire relay if gate is pushed UP from closed limit, used with clutch option. Also

ANTI TAIL-GATE ALARM, if tailgating is detected by close loop, K1 relay will fire. When using clutch option, turning on S1-6 & S2-7, gate will close by timer whenever forced up.

SWITCH 7: Used to enable arm to work in reverse direction, see page 9.

SWITCH 8: Off will make K1 relay activate during open cycle (use with buzzers, counters, etc.). On will pulse K1 relay when OPEN LIMIT (OLS) is reached (activates a swing or slide gate its lane).

See also page 18, ***RELAY OUTPUT-K1***

FAST RUN TIMER - SWITCH PACK S1 (1-4)

The fast run timer sets the time that the operator runs at full speed. The slow start ramp time is fixed. The slow stop ramp time is fixed but can be overrun by the fast run time if not adjusted properly. When adjusting make sure the slow stop ramp completes before the close limit. With all switches off, the default fast run time is 1.5 seconds. Changing settings will adjust fast run timer by 1/8 second increments. (Example: #2 on equals .25 seconds, #4 on equals 1 second. #2 and #4 on equals 1.25 seconds, etc.)

CLOSE TIMER - SWITCH PACK S2 (1-5)

NOTE: *Default setting is off.*

On the MEGA ARM the switches 1-5 on S2 are for the closing time delay to select the period of time that the gate stays open after the obstruction sensor has reversed and re-opened the arm or if the S2-7 timer to close is turned on. The default will keep the gate up for 4 seconds to allow the vehicle to be moved from the gate arm path. Changing settings 1 - 5 will increase or decrease this hold open time. The default of ***3 ON and 1, 2, 4, 5 OFF*** will provide a 4 second close time delay.

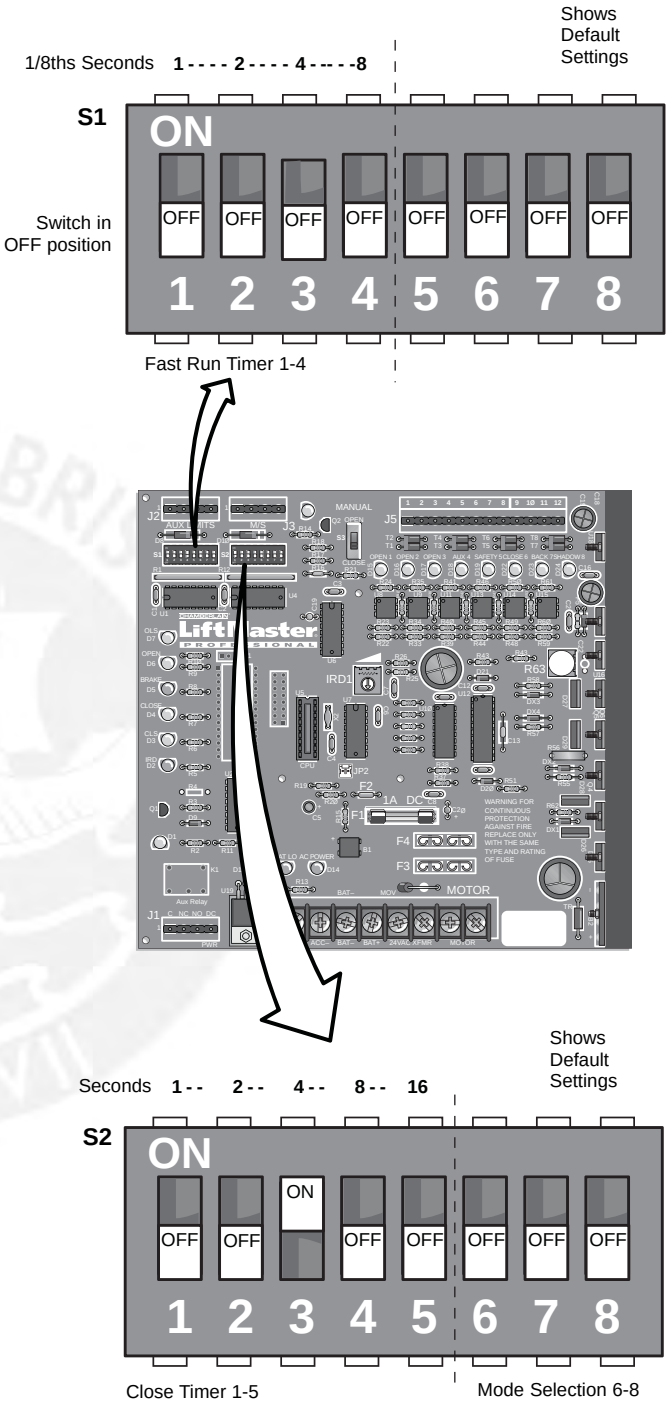
MODE SELECTIONS - SWITCH PACK S2 (6-8)

SWITCH 6 - INPUT MEMORY: Activates multiple vehicle memory at auxiliary input terminal #4 on J5.

SWITCH 7 - AUTO CLOSE TIMER: Default is **OFF**. On will close gate by timer when all inputs are cleared. Time is set by using S2 1-5 switches. (WARNING: Special care should be used to avoid arm from closing on cars. Use safety loops, stop loops, photo beams and a long enough time delay.)

NOTE: *Can be used with multiple vehicle memory buffer to allow gate to close and reset count memory to zero. When using clutch option, turning on S1-6 & S2-7, gate will close by timer whenever forced up.*

SWITCH 8 - AUTO OPEN ON POWER FAILURE: When switch number 8 is in the **ON** position, the operator will automatically open the gate approximately 15 seconds after the loss of power. Once power is restored the operator will resume normal operation after the first car passes closing loop or if close timer S2-7 in turned on (it is recommended to allow the gate to close by loop, not by timer).



INSTALL THE RECEIVER

⚠ WARNING

To prevent possible SERIOUS INJURY or DEATH from a moving gate or garage door:

- ALWAYS keep remote controls out of reach of children. NEVER permit children to operate, or play with remote control transmitters.
- Activate gate or door ONLY when it can be seen clearly, is properly adjusted, and there are no obstructions to door travel.
- ALWAYS keep gate or garage door in sight until completely closed NEVER permit anyone to cross path of moving gate or door.

NOTICE: To comply with FCC and or Industry Canada (IC) rules, adjustment or modifications of this receiver and/or transmitter are prohibited, except for changing the code setting or replacing the battery. THERE ARE NO OTHER USER SERVICEABLE PARTS.

Tested to Comply with FCC Standards FOR HOME OR OFFICE USE. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

WIRING THE RECEIVER

Contacts 1 and 2 on the receiver terminal strip are for power. The power terminals are unpolarized. Connect terminals 1 and 2 to the accessory power terminals on the J4 terminal strip at the bottom of the logic board (Figure 1).

Contacts 3 and 4 on the receiver terminal strip are for a common and a relay. Connect terminals 3 and 4 to terminals 1 and 10 on the J5 terminal strip at the top of the logic board.

NOTE: *Auxiliary Pin 4 can be used for push to open/push to close functionality.*

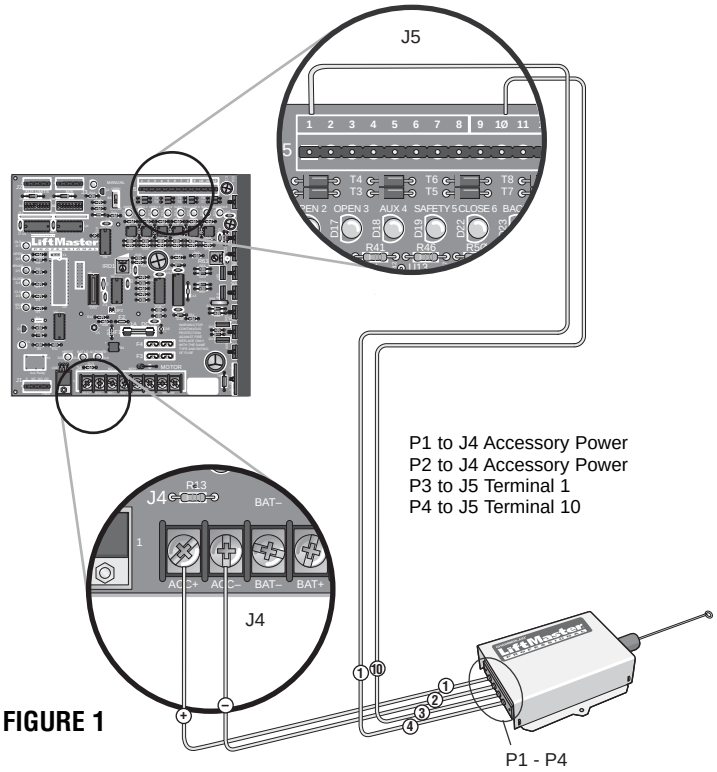


FIGURE 1

SET SECURITY MODE

The Universal Receiver can be used with up to 15 rolling code remotes or passwords in HIGH security mode. Alternately, it can be used with up to 31 of any type remote in NORMAL security mode, including any combination of rolling code, billion code (390Mhz only), or dip switch remotes.

The jumper must be set at the HIGH position for the receiver to operate in HIGH security mode. It must be set at NORMAL position to operate at the NORMAL mode (Figure 2).

When changing from NORMAL to HIGH security mode, any previous remote codes must be erased. Repeat Steps 2 and 3 in the Programming Section below to reprogram the receiver for each remote control in use.

The receiver is factory set at HIGH.

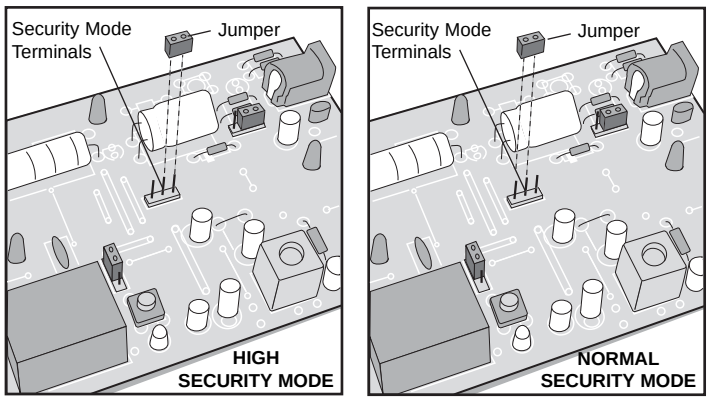


FIGURE 2

PROGRAMMING THE REMOTE TO THE RECEIVER

STEP 1: Pry open the front panel of receiver case with a coin or a screwdriver. Re-connect power to opener (Figure 3).

STEP 2: Press and release the "learn" button on the receiver. The learn indicator light will glow steadily for 30 seconds.

STEP 3: Within 30 seconds, press and hold the button on the hand-held remote that you wish to operate your gate.

The opener will now operate when the push button on either the receiver or the remote control is pressed.

Repeat Steps 2 and 3 for each remote control that will be used to operate the gate.

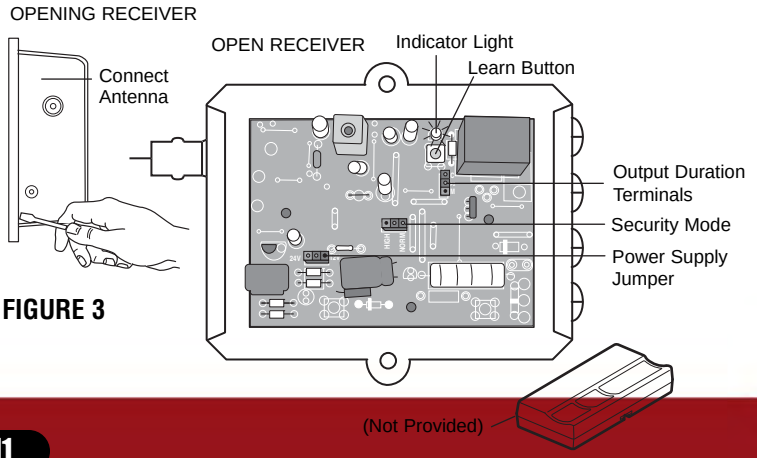


FIGURE 3

TO ERASE ALL REMOTE CONTROL CODES

Press and hold the "learn" button on the receiver panel until the indicator light turns off (about 6 seconds). All remote codes are now erased. Then follow the steps above to reprogram each remote control.

ADJUSTMENTS

INSTANT REVERSE DEVICE (IRD)

The reverse device is an internal circuit that continuously monitors the motors current for increased draw. Turning the IRD1 right (CW more sensitive), or left (CCW less sensitive) in small increments will allow sensitivity adjustments (IF ARM DOES NOT REVERSE, DO NOT CONTINUE TO FORCE). The obstruction that you apply should STOP the arm. Adjust sensitivity so that consistent reversal occurs. If the gate stops while opening then the ***IRD*** is TOO sensitive.

Some slight adjustment either way may be needed so that the gate only reverses when obstructed. If gate is obstructed while closing, the gate will reverse to the open position, time out (using the time delay set at S-2 switches 1-5) and then close. If gate is opening when obstructed, gate will stop its open travel, then will time out and close using the same delay set at S-2.

If S-2 switch number 8 is off (you have programmed the unit to **NOT AUTO RAISE** when power fails), then recheck your adjustments with AC power off to be sure proper operation will be maintained.

NOTES: *Instant reverse device (IRD) should be tested monthly to insure proper operation. If adjustments are required, refer to above paragraph.*

Adjustments to be done by qualified service persons only.

⚠ WARNING

To reduce the risk of SERIOUS INJURY or DEATH:

- Disconnect power BEFORE performing ANY adjustments near drive shaft.

GATE ARM INSTALLATION AND LEVELING

Install arm in gate arm bracket by lining up holes in arm with the slotted holes in bracket. Insert the bolts through the arm and through the bracket. Next install the flat washers then the nylon nuts. (It is recommended the only nylon nuts be used to attach arms).

The magnetic limit cam is pre-adjusted for near proper arm travel, however if leveling of the arm is required this can be done through adjustment to the magnetic cam arm. Note that limit range can be impacted from 85 to 89 degrees by sliding the main board up and down in its slot. Always adjust for a level arm in the **HORIZONTAL POSITION**. There is a small set screw in the side of the cam arm which can be loosened to allow the cam arm magnet to reach the close limit sensor (located on back of controller, H2) earlier or later in its travel.

Continue to open and close the gate while adjusting until a satisfactory horizontal stopping point can be maintained. Afterwards re-secure set screw in cam arm. ***NOTE:*** *In some cases additional adjustments may be required after the belt wears in.* When stopping in the open position, the arm will stop just before the full vertical position.

NOTE: *To prevent entrapment, allow for two (2) feet minimum clearance past end of arm when in down position.*

OPERATION AND MAINTENANCE

IMPORTANT SAFETY INSTRUCTIONS

⚠ ⚠ WARNING

To reduce the risk of SEVERE INJURY or DEATH:

1. READ AND FOLLOW ALL INSTRUCTIONS.
2. NEVER let children operate or play with gate controls. Keep the remote control away from children.
3. ALWAYS keep people and objects away from the gate. NO ONE SHOULD CROSS THE PATH OF THE MOVING GATE.
4. Test the gate operator monthly. The gate MUST reverse on contact with a rigid object or stop when an object activates the non-contact sensors. After adjusting the force or the limit of travel, retest the gate operator. Failure to adjust and retest the gate operator properly can increase the risk of INJURY or DEATH.
5. Use the emergency release ONLY when the gate is not moving.
6. KEEP GATES PROPERLY MAINTAINED. Read the owner's manual. Have a qualified service person make repairs to gate hardware.
7. The entrance is for vehicles ONLY. Pedestrians MUST use separate entrance.
8. Disconnect ALL power BEFORE performing ANY maintenance.
9. ALL maintenance MUST be performed by a LiftMaster professional.
10. **SAVE THESE INSTRUCTIONS.**

OPERATION AND MAINTENANCE

Check at the intervals listed in the following chart:

ITEM	PROCEDURE	EVERY 3 MONTHS	EVERY 6 MONTHS	EVERY 12 MONTHS	EVERY 24 MONTHS
Fasteners	Check and tighten as required.		●	◆	
Bearings & Shafts	Check for wear and lubricate.	●		◆	
Battery Maintenance	Replace batteries.				●

♦ **Repeat ALL procedures.**

GENERAL SERVICE

1. Belt loose or needs replacement, adjust with 4 bolts that support motor to allow 1/4" play.
2. Charge voltage for batteries should be 27.5 +0.05, -0 Vdc with batteries disconnected (set with R63, shown on the Control Board Layout page).
3. Replace batteries with Liftmaster P/N MBAT batteries. Replace in pairs.

SHEAR PIN REPLACEMENT

If gate arm is vandalized and the tapered pin in the output shaft has been sheared, it must be replaced correctly and with the right pin type. Replacement must be done by always punching out the pin (or pieces) from the small end only. If drilling is required, DO NOT DAMAGE THE SHAFT, use a drill bit smaller than the small hole size of the pin. (Correct pin (P/N MA013) is a 2" pin with a number 6 taper only.)

***NEVER* USE A BOLT AS A TEMPORARY FIX, *THIS WILL DAMAGE* THE SHAFT AND COLLAR**

1. Use S-3 to rotate bracket to up position
2. Turn off AC power and disconnect batteries small end first.
3. Remove gate arm bracket and pieces in collar
4. Drive out pin pieces with hammer and punch (Solid sharp blows are better than light ones)
5. Reinstall gate arm bracket
6. Lightly oil the new pin then insert into collar
7. Fully seat pin in shaft by taping on large end
8. Reinstall the arm if required
9. Turn on AC power and connect batteries
10. Turn off S-3 to put gate into operation

⚠ WARNING

To avoid SERIOUS PERSONAL INJURY or DEATH from electrocution, disconnect ALL electric power BEFORE performing ANY maintenance.

BATTERY DISPOSAL

Replaced batteries must be treated as a hazardous waste and disposed of in accordance with State, Local and Federal Regulations. See the battery manufacturer's Material Safety Data Sheets (01-30839 "MSDS Sheets, Battery, Standard").

BATTERY REPLACEMENT

Service Kits are available for battery replacement. Please contact Technical Support (see back of this document for contact information).

BATTERY MAINTENANCE / TESTING

The batteries are maintenance free. However, to insure proper and safe operation, it is recommended that the batteries be replaced every two years. Battery testing is conducted automatically. See the Battery Test Description section for manually initiating the battery test.

BATTERY HANDLING / STORAGE

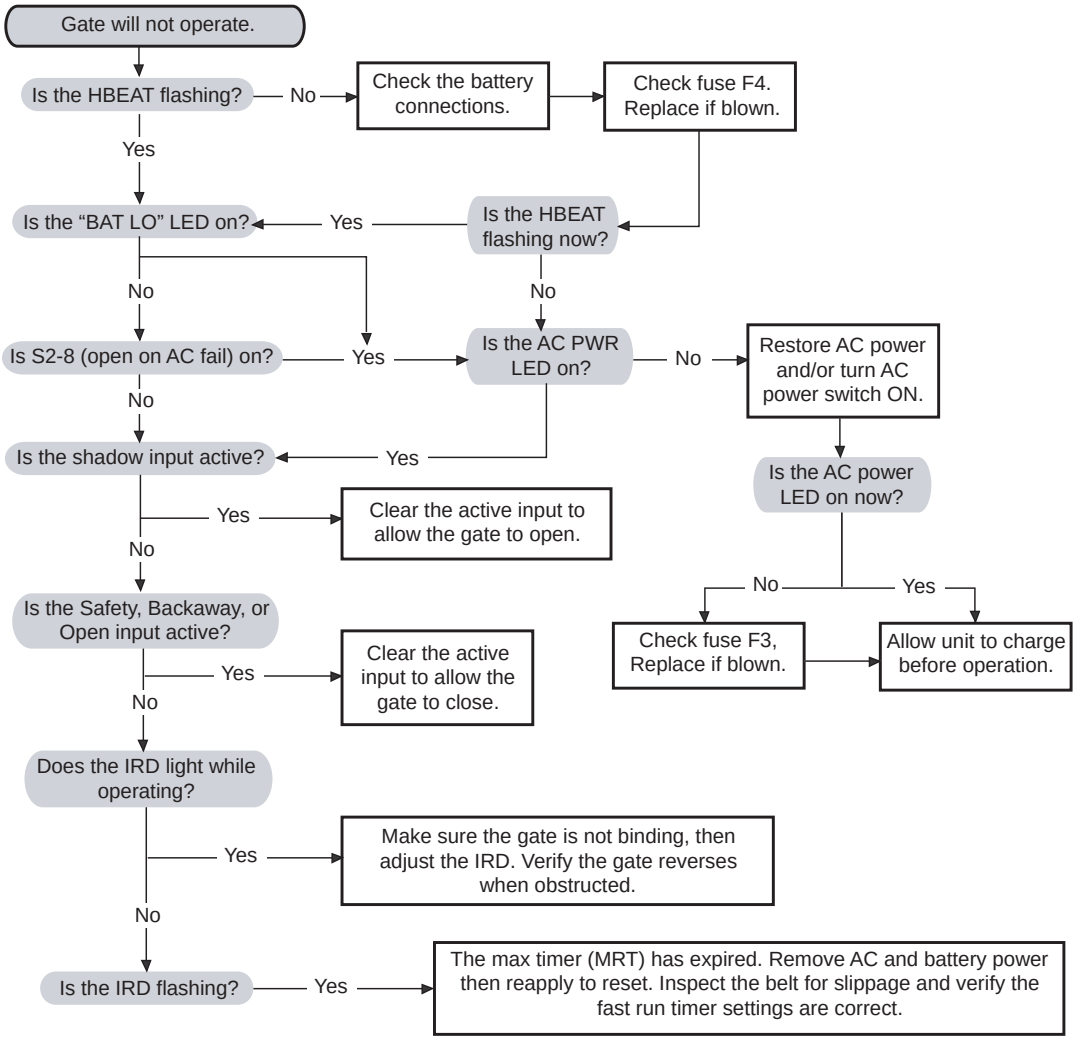
Refer to the battery manufacturer's Material Safety Data Sheets (01-30839 "MSDS Sheets, Battery, Standard"). LiftMaster does not recommend storage of batteries in the field. Batteries are intended for immediate use.

WARNING - DISCONNECT BATTERIES AND AC POWER BEFORE SERVICING ANY MECHANICAL OR MOVING COMPONENTS.

BATTERY CHECKOUT

When the batteries become weak the gate will begin to run noticeably slower. ***NOTE:*** *Batteries should only be checked when you are sure they have had adequate time to fully charge.* Turn off the AC power and run gate for 5 to 10 cycles while observing low battery indicator LED D12. If LED 12 comes ON, batteries are too weak to function properly. If LED 12 does not light, then voltage should be checked as they still maybe near failure. Correct voltage is approximately 24.5Vdc. ***NOTE:*** *If LED D12 does light, gate will open to conserve batteries in this test or in a real power loss, even if mode switch 8 on S2 is off.* Return of AC power will clear low battery indicator. Correct charge voltage is 27.5 Vdc with batteries not connected (set with R63, shown on the Control Board Layout page).

GATE NOT OPERATING



SUGGESTED LOOP SENSOR LOCATIONS

FREE EXIT ON VEHICLE APPROACH

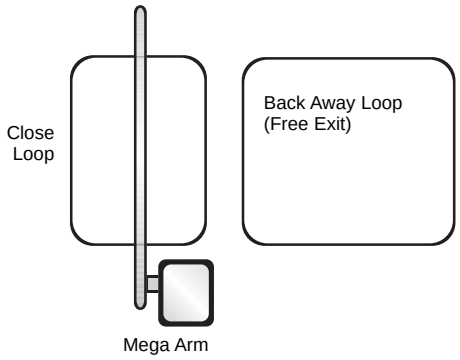
Gate will open when sensed by exit loop and then close once the close loop is cleared. If the vehicle pulls up to the exit loop and then backs away, it will close (Figure 1).

Space between loops will be 4' to 10'.

Terminal #7 is backaway (free exit).

Terminal #6 is close input.

FIGURE 1



ENTRY WITH ACCESS CONTROL DEVICE

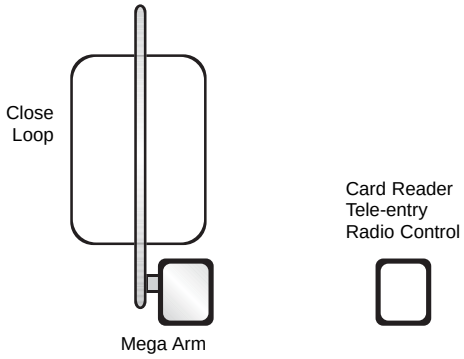
Gate will open when activated by an access control device. When vehicle passes and clears close loop, gate will close (Figure 2).

NOTE: *If a second vehicle tail-gates and is sensed at the close loop, gate will stop its closing motion until loop is cleared again.*

Terminal #6 is close input.

Terminals #1, 2, and 3 are open inputs.

FIGURE 2



DUAL DIRECTION AS ENTRY OR FREE EXIT

Dual direction is a combination of both of the above configurations to provide the ability for traffic to enter or exit in the same lane (Figure 3).

Space between loops will be 4' to 10'.

DO NOT ALLOW CONTROL DEVICES TO BE WITHIN 10' OF GATE OR OPERATOR

RECOMMENDATION 1: If vehicle detectors are used to open or close the gate, use of the presence contacts are recommended. Using the pulse contacts will **REDUCE** the gate's safe operation.

RECOMMENDATION 2: If closing timer is to be used, use **ONLY** on a dedicated free exit.

RECOMMENDATION 3: Close loop must be centered under gate arm.

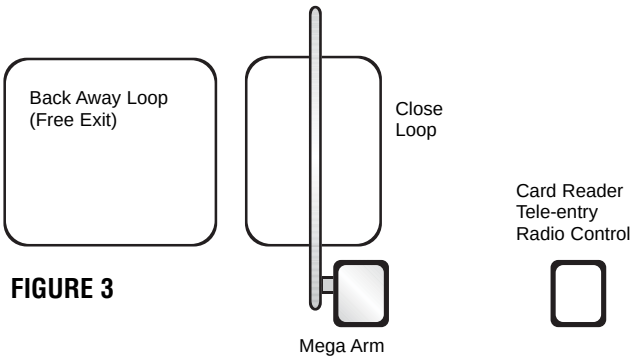


FIGURE 3

TRAP INSTRUCTIONS

INSTALL THE K1 AUXILIARY RELAY AND CONNECTOR AT MEGA ARM CONNECTED TO THE ACCESS DEVICE

1. Press the relay into the K1 location ensuring the pins are properly aligned.
2. Press the connector into the J1 connector pins.

INSTALL THE K1 AUXILIARY RELAY AND CONNECTOR AT THE SECOND

1. Press the relay into the K1 location ensuring the pins are properly aligned.
2. Press the connector into the J1 connector pins.

WIRE THE CONNECTIONS BETWEEN THE OPERATORS

1. Connect the Normally open output (NO) of the K1 relay on the trap unit to the OPEN input (J5 - term#2) of the second unit.
2. Connect the common output (C) of the K1 relay of the trap unit to the common of the second unit (J5 - term#12).
3. Connect the Normally open output (NO) of the K1 relay on the second unit to the INTERLOCK input of the trap unit (J5 - term#8).
4. Connect the common output (C) (J5 - term#12) of the second unit to the common of the trap unit (J5 - term#12).

SET THE DIP SWITCHES AT THE TRAP OPERATOR

1. Set switch bank S1 to 00100001 where 1 is up and 0 is down.
2. Set switch bank S2 to 00100010 where 1 is up and 0 is down.

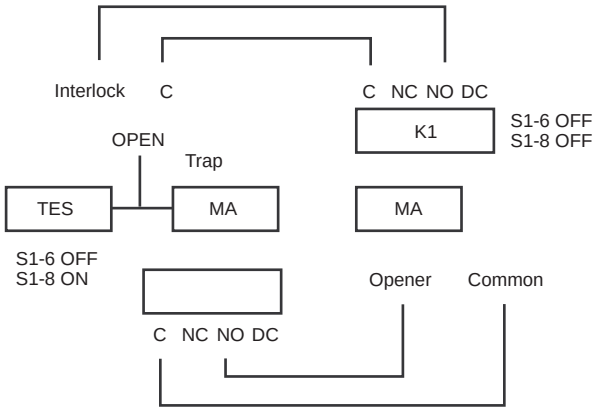
SET THE DIP SWITCHES AT THE SECOND OPERATOR

1. Set switch bank S1 to 00100000 where 1 is up and 0 is down.
2. Set switch bank S2 to 00100010 where 1 is up and 0 is down.

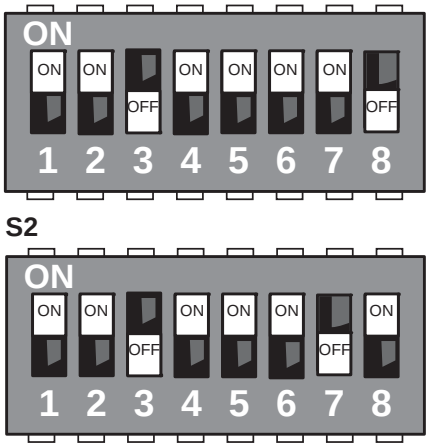
RECONNECT THE POWER AND TEST

1. Reconnect the DC power by replacing the neutral (Black) wire to the battery terminal.
2. Reconnect the AC Power to the operator.
3. To test, activate the following sequence of inputs:
   a. Open the trap gate using the access device.
   b. When the trap gate is open, activate the close loop on the trap operator. The trap gate will close and the second gate should open.
   c. When the second gate is open, activate the close loop on the second operator. The second gate should close.

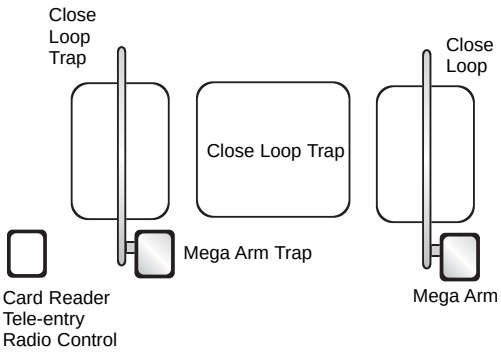
TRAP SET UP



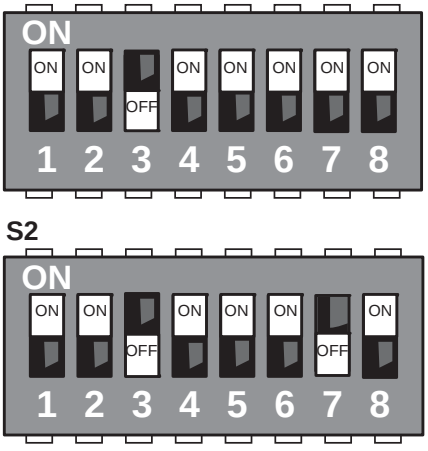
Trap Operator



TRAP CONFIGURATION
Must use trap kit. See Mega Arm Options Parts List



Mega ARM Operator



SEQUENCE ACCESS MANAGEMENT SYSTEM (SAMS) WITH "MEMORY"

SAMS WITH OTHER OPERATORS

REQUIRES THE K1 RELAY OPTION (Order SAMS KIT)

This feature allows a logical interface between the MEGA ARM barrier gate and a swing, slide, etc. gate operator (or MTC-31). All that is required is 4 wires between the MEGA ARM barrier gate and the other operator. It will be necessary to have one set of dedicated/isolated dry contacts - {C. and N.C.} COMMON and NORMALLY CLOSED be available at the other operator's OPEN LIMIT SWITCH. Most units will require that this EXTRA limit switch be added to their open limit switch assembly (Figure 1).

OPERATION: A one second pulse from access control device to the MEGA ARM will energize its K1 relay sending an open signal to the other operator causing it to open. However, the MEGA ARM's boom will not raise yet. When the other operator reaches its full open limit switch, this will open the COMMON and NORMALLY CLOSED contact on the EXTRA open limit switch. This will allow the original signal from your access control device (that was stored in memory) to now raise the gate arm. As long as the other operator is in the full open position, any additional open pulse sent will in turn energize the MEGA ARM's K1 relay to send another open signal to the other operator as well as cause the arm to raise again if it has closed via a car crossing the MEGA ARM's close loop.

WIRING: Run 2 wires from the other operator's isolated common & normally closed contacts of its open limit switch to the MEGA ARM J5#8 and one of the commons J5, #9-12. Next, run 2 wires from the MEGA ARM's K1 relay (common & normally open) to the other operators common and open input. (WARNING: max of 30 VOLTS at .5 amps through relay). J5 #8 was the unused SHADOW LOOP input on the MEGA ARM.

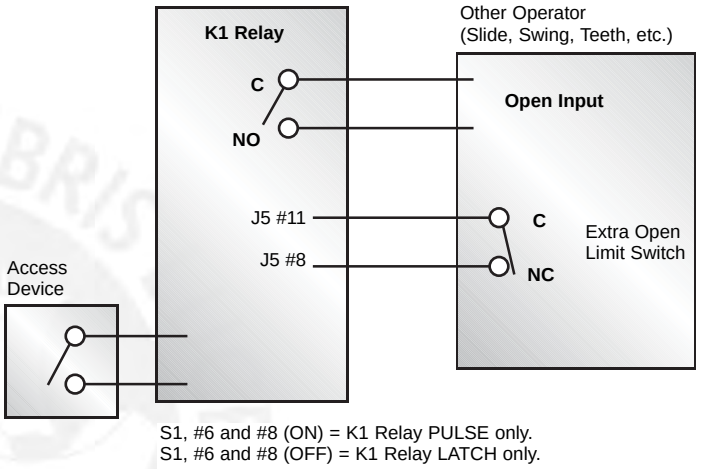
NOTE: *A separate open device (24 hour timer, toggle switch) can be run to the other operator to control it without raising the gate arm. Tampering with the other operator's safety loops, safety edges and reverse sensors WILL NOT cause the arm to raise if one tripped. The arm will only raise if an intended open signal was sent to the MEGA ARM.*

NOTES: *For motorized teeth, vertical pivot or overhead operator, leave S1-6, S1-8 OFF (this will keep the K1 relay latched down until the arm reaches the down position. This will keep the other gate operator locked open or teeth locked down until the arm closes completely).*

In this mode, if the arm senses an impact, the K1 relay will stay energized holding open (or teeth down) the other operator until the arm times out and closes.

NOTE: *Insert a jumper across the JP2 terminal to allow the SAMS feature to work with the multiple vehicle memory count selection, use the K1 relay to open the sequenced gate (S1-5 off, S2-6 on, jumper across JP2). This allows gate to store input counts via J5 #4 but not raise the arm until the sequenced slide or swing gate has fully opened.*

FIGURE 1



S1, #6 and #8 (ON) = K1 Relay PULSE only.
S1, #6 and #8 (OFF) = K1 Relay LATCH only.

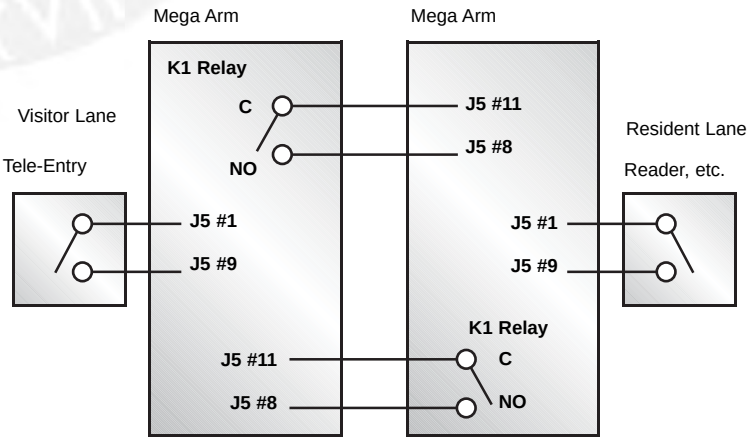
SAMS TWO MEGA ARMS WITH "MEMORY"

REQUIRES THE K1 RELAY OPTION (Order SAMS KIT)

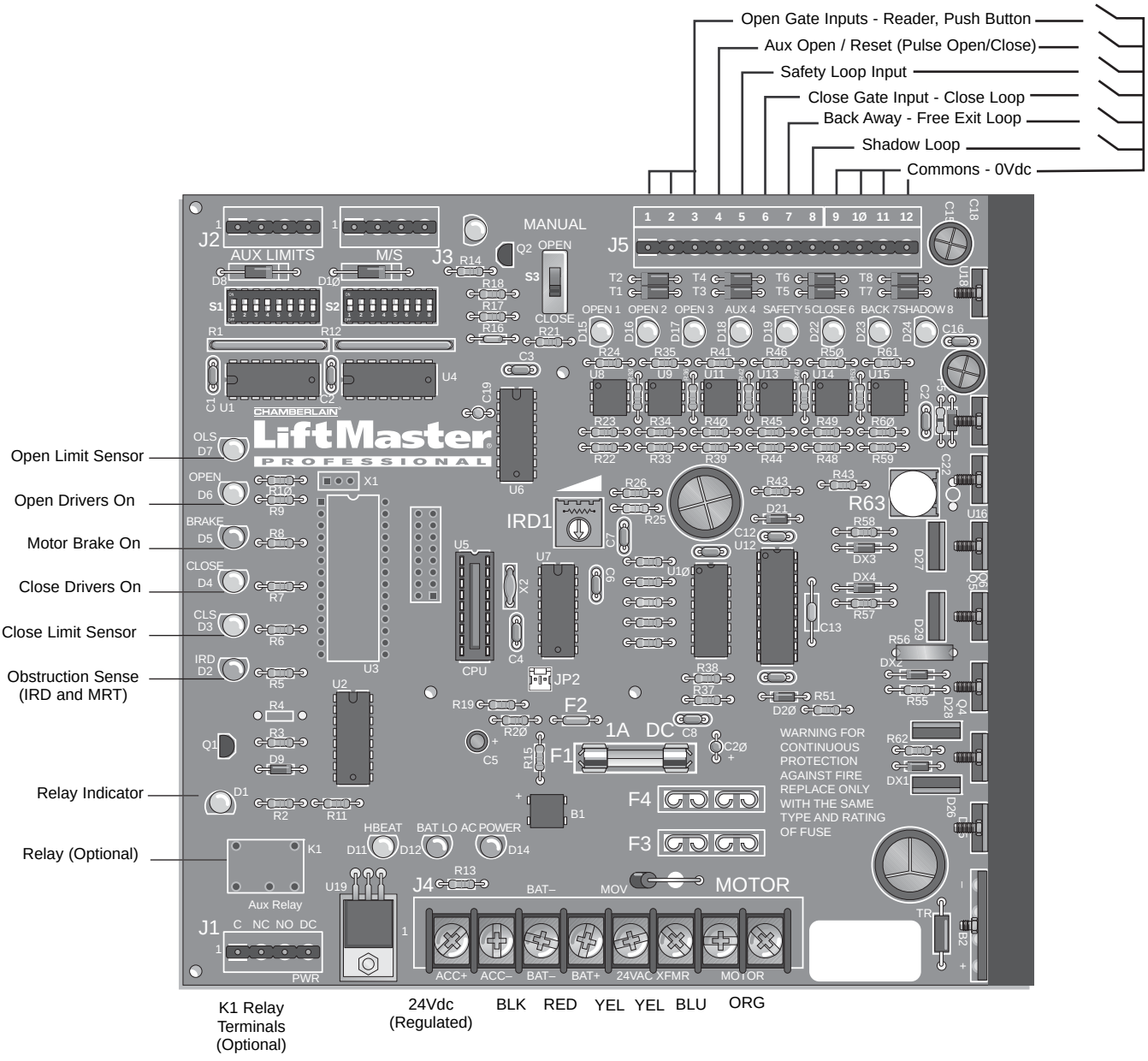
NOTE: *Can be used when you have two entry gates that you want to* ***SEQUENCE*** *with each other. This is when you can only have* ***ONE*** *gate raised at a time (bottle neck or gates at a cross street). In this case, which ever one raises first will get first priority, while if the other gets an open signal, it will be* ***HELD IN MEMORY****, then raise once the first gate closes. This will work if either gate has a telephone entry unit or access device (AVI, prox, etc.).*

Connect the K1 relay C and N.O. of each gate to the SHADOW LOOP J5 #8 input and common of the other (Figure 2). (Leave S1-6 and 8 OFF to allow relay to stay latched.)

FIGURE 2



CONTROL BOARD LAYOUT



INPUT LOCATIONS

Accessory power is 24Vdc regulated rated at 500 ma. [1/2 amp].

NOTE: *J5 #8 is now the SAMS with memory input (see page 12).*

D11: Heart beat. Shows that processor and program are running properly.

D12: Battery status. See diagnostic procedures.

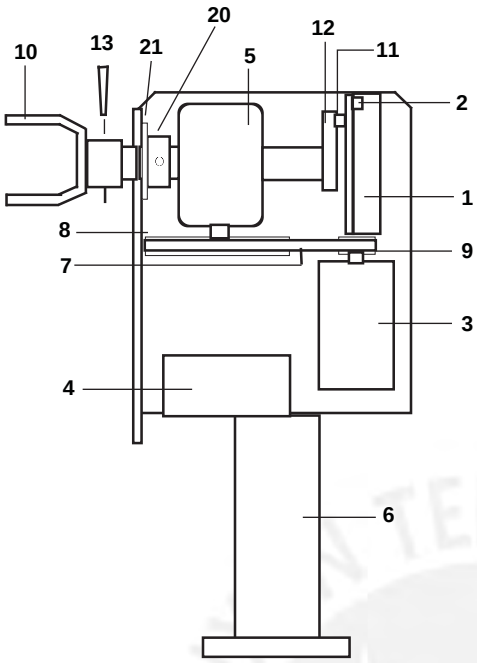
D14: AC power indicator. Shows that AC power is present.

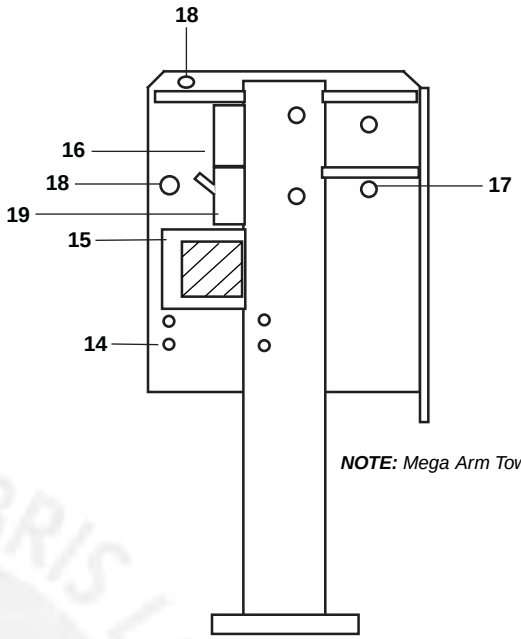
S3: Manual open. To allow gate to be opened or closed during service of unit. Keep in the "Close" position for normal operation.

F3: 10 amp ATO type fuse for 24Vac input power. (UL listed fuse only.)

F4: 15 amp ATO type fuse for 24Vdc battery input power. (UL listed fuse only.)

MEGA ARM UL PARTS LIST





NOTE: *Mega Arm Tower not shown*

PART NUMBERS AND DESCRIPTIONS

ITEM	PART NUMBER	DESCRIPTION
1	MA001	Controller
2	MA002	Removable Connector
3	MA003	DC Motor - 24 Vdc
4	MBAT	12Vdc 7AH Battery 2 required
5	MA005	Gear Reducer 60:1
6	MA006	Aluminum Chassis
7	MA007	Drive Belt
8	MA008	Reducer Pulley
9	MA009	Motor Pulley
10	MA010	Gate Arm Bracket
11	MA011	Magnet
12	MA012	Cam Arm
13	MA013	Shear Pin

ITEM	PART NUMBER	DESCRIPTION
14	MA014	Bolt and Nut (4) Motor
15	MA015	Transformer
16	MA016	120 Vac Duplex Outlet (120 Vac Only)
17	MA017	Bolt and Nut (4) Reducer
19	MA019	On/Off Switch
*	MA020	Unit Cover for Mega Arm (Not Tower)
*	MA021	Nylon Arm Nuts (2)
*	MA022	Arm Bolts (2)
*	MA023	Gate Arm - 12'
*	73A3	Filter Module
*	74-31243	Surge Suppressor
20	MA036	Collar
21	MA037	Nylon Washer

(*) parts not shown

PARTS SHIPPED

ITEM	QTY
MEGA ARM Operator	1
Controller	1
Unit Cover	1
Installation and Service Manual	1
Arm Bolts with Washers	2
Nylon Nuts	10
7AH Batteries	2

MEGA ARM TOWER UNIQUE PARTS LIST

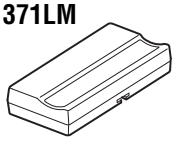
ITEM	PART NUMBER	DESCRIPTION
*	MA020T	Unit Cover for Mega Arm Tower
*	MA020D	Unit Door for Mega Arm Tower

MEGA ARM OPTIONS PARTS LIST

ITEM	PART NUMBER	DESCRIPTION
*	71-TRAP	Trap option
*	71-SPRINT	Sprint option
*	71-TRAPSP	Sprint Trap option

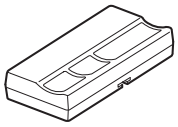
ACCESSORIES FOR DC BARRIER ARM OPERATORS

371LM



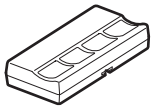
SECURITY+® Single Button Remote Control: Includes visor clip.

373LM



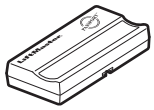
SECURITY+® 3-Button Remote Control: Includes visor clip.

374LM



SECURITY+® 4-Button Remote Control: Includes visor clip.

CPT13



Passport™ 1-Button Remote Control: Includes visor clip.

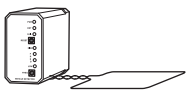
CPT33

Passport™ 3-Button Remote Control: Includes visor clip.

CPT43

Passport™ 4-Button Remote Control: Includes visor clip.

A24



24Vdc Loop Detector

A57 **Wiring Harness:** For the A24.

MA201 **Heater Kit:** 150 watt with thermostat (MA and MAS only).

UN201 **Heater Kit:** 500 watt with thermostat (MAT and MATS only).

MA005C **Slip Clutch Option:** For Mega Arm Gear Box.

MA200 **K1 Relay Output Option**

Sprint Units Only:

SP8 **Sprint Gate Arm:** 8' Padded Safety Arm, yellow.

SP8 TUBE **Replacement Arm Tube**

SP8 PAD **Replacement Pad:** Yellow.

MA023 **Aluminum Arm:** White, 12' x 3" diameter with warning labels.

MA024 **Aluminum Arm:** 12' x 3" diameter with yellow/black stripes.

MA024R (Highly Recommended) **Aluminum Arm:** 12' x 3" diameter with reflective yellow/black stripes.

MA021 **Nylon Arm Nuts:** (Pkg. of 50).

MA021A **Nylon Arm Nuts:** (Pkg. of 50), thin.

MA031 **Adapter Collars:** For padded arm option (2 included).

MA025 **Round Padded Arm:** 12' x 4" diameter, yellow (requires MA031).

MA026 **Replacement Pad:** 12' x 4" diameter, yellow.

MA027 **Replacement Arm Tube:** 12' x 2" diameter.

MA028 **Round Padded Arm:** 14' x 4" diameter, yellow (requires MA031).

MA029 **Replacement Pad:** 14' x 4", yellow.

MA030 **Replacement Arm Tube:** 14' x 4".

MA117 **Counter Weight:** Required for all 15' arms.

MA115 **Aluminum Gate Arm:** White, 15' x 3" (requires MA117).

MA116 **Aluminum Gate Arm:** 15' x 3" with yellow/black stripes (requires MA117).

MA116R **Aluminum Gate Arm:** 15' x 3" with reflective yellow/black stripes (requires MA117).

MA034 (Highly Recommended) **Articulating PVC (folding) Arm:** 9' with hardware kit.

MA033 **Hardware Kit:** (Only for MA034).

MA035 **PVC Arm:** 9' (Only for MA034).

MA024-10 **Articulation Aluminum (folding) Arm:** 10' without hardware kit, with yellow/black stripes.

SAMSKIT Includes required relay and limits.

MA230VKIT Includes surge suppressor, wire jumper, duplex box covers and detailed instructions.

OPERATOR NOTES

OPERATOR NOTES

WARRANTY POLICY

(You must read, understand and agree with all items in the limited warranty)

LiftMaster warrants the **MEGA ARM-UL** to be free of defects in workmanship and materials for a period of 2 years for electronics and mechanical components and includes a 10 year corrosion perforation warranty on the cover and chassis. Warranty will begin from the date of purchase.

LiftMaster reserves the right of final determination as to the existence and causes of any defect or failure. Any part or parts found to be defective and are returned to LiftMaster within the warranty period, shall at our option be repaired or replaced free of charge F.O.B. the factory. Freight is not included at any time on gate arms and chassis. ONLY UPS ground freight is included during the first year of warranty.

The warranty will not apply the following circumstances which are considered beyond our control.

Mis-use, vandalism, accident, neglect, unauthorized repairs or modifications, acts of God (lightning, floods, insect damage, etc.), power surges, units subjected to corrosive environments, incorrect installation or application, the batteries or incorrect battery installation, operation without or failure to use correct battery type, damage to arm bracket and/or gear reducer due to use of incorrect arm.

The warranty set forth above is entirely exclusive and no other warranty whether written or oral, is expressed or implied. LiftMaster specifically disclaims any and all implied warranties, merchantability or fitness for a particular purpose. It is the purchasers sole and exclusive responsibility to determine whether or not the equipment will be suitable for a particular purpose. In no event shall LiftMaster, inc. be held liable for direct, indirect, incidental, special, consequential damages or loss of profits whether based on contract, tort, or any other legal theory during the course of the warranty or at any time there after. The installer and/or end user agree to assume all responsibility for all liability in use of this product, releasing LiftMaster of all liability.

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MFRC522

Standard performance MIFARE and NTAG frontend

Rev. 3.9 — 27 April 2016
112139

Product data sheet
COMPANY PUBLIC

1. Introduction

This document describes the functionality and electrical specifications of the contactless reader/writer MFRC522.

Remark: The MFRC522 supports all variants of the MIFARE Mini, MIFARE 1K, MIFARE 4K, MIFARE Ultralight, MIFARE DESFire EV1 and MIFARE Plus RF identification protocols. To aid readability throughout this data sheet, the MIFARE Mini, MIFARE 1K, MIFARE 4K, MIFARE Ultralight, MIFARE DESFire EV1 and MIFARE Plus products and protocols have the generic name MIFARE.

1.1 Differences between version 1.0 and 2.0

The MFRC522 is available in two versions:

- MFRC52201HN1, hereafter referred to version 1.0 and
- MFRC52202HN1, hereafter referred to version 2.0.

The MFRC522 version 2.0 is fully compatible to version 1.0 and offers in addition the following features and improvements:

- Increased stability of the reader IC in rough conditions
- An additional timer prescaler, see Section 8.5.
- A corrected CRC handling when RX Multiple is set to 1

This data sheet version covers both versions of the MFRC522 and describes the differences between the versions if applicable.

2. General description

The MFRC522 is a highly integrated reader/writer IC for contactless communication at 13.56 MHz. The MFRC522 reader supports ISO/IEC 14443 A/MIFARE and NTAG.

The MFRC522's internal transmitter is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443 A/MIFARE cards and transponders without additional active circuitry. The receiver module provides a robust and efficient implementation for demodulating and decoding signals from ISO/IEC 14443 A/MIFARE compatible cards and transponders. The digital module manages the complete ISO/IEC 14443 A framing and error detection (parity and CRC) functionality.

The MFRC522 supports MF1xxS20, MF1xxS70 and MF1xxS50 products. The MFRC522 supports contactless communication and uses MIFARE higher transfer speeds up to 848 kBd in both directions.

The following host interfaces are provided:

- Serial Peripheral Interface (SPI)
- Serial UART (similar to RS232 with voltage levels dependant on pin voltage supply)
- I^2C-bus interface

3. Features and benefits

- Highly integrated analog circuitry to demodulate and decode responses
- Buffered output drivers for connecting an antenna with the minimum number of external components
- Supports ISO/IEC 14443 A/MIFARE and NTAG
- Typical operating distance in Read/Write mode up to 50 mm depending on the antenna size and tuning
- Supports MF1xxS20, MF1xxS70 and MF1xxS50 encryption in Read/Write mode
- Supports ISO/IEC 14443 A higher transfer speed communication up to 848 kBd
- Supports MFIN/MFOUT
- Additional internal power supply to the smart card IC connected via MFIN/MFOUT
- Supported host interfaces
  - SPI up to 10 Mbit/s
  - I^2C-bus interface up to 400 kBd in Fast mode, up to 3400 kBd in High-speed mode
  - RS232 Serial UART up to 1228.8 kBd, with voltage levels dependant on pin voltage supply
- FIFO buffer handles 64 byte send and receive
- Flexible interrupt modes
- Hard reset with low power function
- Power-down by software mode
- Programmable timer
- Internal oscillator for connection to 27.12 MHz quartz crystal
- 2.5 V to 3.3 V power supply
- CRC coprocessor
- Programmable I/O pins
- Internal self-test

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	analog supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
V_{DDD}	digital supply voltage			2.5	3.3	3.6	V
$V_{DD(TVDD)}$	TVDD supply voltage			2.5	3.3	3.6	V
$V_{DD(PVDD)}$	PVDD supply voltage		[3]	1.6	1.8	3.6	V
$V_{DD(SVDD)}$	SVDD supply voltage	$V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V		1.6	-	3.6	V

Table 1. Quick reference data *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{pd}	power-down current	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)} = 3$ V					
		hard power-down; pin NRSTPD set LOW	[4]	-	-	5	µA
		soft power-down; RF level detector on	[4]	-	-	10	µA
I_{DDD}	digital supply current	pin DVDD; $V_{DDD} = 3$ V		-	6.5	9	mA
I_{DDA}	analog supply current	pin AVDD; $V_{DDA} = 3$ V, CommandReg register's RcvOff bit = 0		-	7	10	mA
		pin AVDD; receiver switched off; $V_{DDA} = 3$ V, CommandReg register's RcvOff bit = 1		-	3	5	mA
$I_{DD(PVDD)}$	PVDD supply current	pin PVDD	[5]	-	-	40	mA
$I_{DD(TVDD)}$	TVDD supply current	pin TVDD; continuous wave	[6][7][8]	-	60	100	mA
T_{amb}	ambient temperature	HVQFN32		–25	-	+85	°C

[1] Supply voltages below 3 V reduce the performance in, for example, the achievable operating distance.

[2] V_{DDA}, V_{DDD} and $V_{DD(TVDD)}$ must always be the same voltage.

[3] $V_{DD(PVDD)}$ must always be the same or lower voltage than V_{DDD}.

[4] I_{pd} is the total current for all supplies.

[5] $I_{DD(PVDD)}$ depends on the overall load at the digital pins.

[6] $I_{DD(TVDD)}$ depends on $V_{DD(TVDD)}$ and the external circuit connected to pins TX1 and TX2.

[7] During typical circuit operation, the overall current is below 100 mA.

[8] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between pins TX1 and TX2 at 13.56 MHz.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
MFRC52201HN1/TRAYB[1]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
MFRC52201HN1/TRAYBM[2]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
MFRC52202HN1/TRAYB[1]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
MFRC52202HN1/TRAYBM[2]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1

[1] Delivered in one tray.

[2] Delivered in five trays.

6. Block diagram

The analog interface handles the modulation and demodulation of the analog signals.

The contactless UART manages the protocol requirements for the communication protocols in cooperation with the host. The FIFO buffer ensures fast and convenient data transfer to and from the host and the contactless UART and vice versa.

Various host interfaces are implemented to meet different customer requirements.

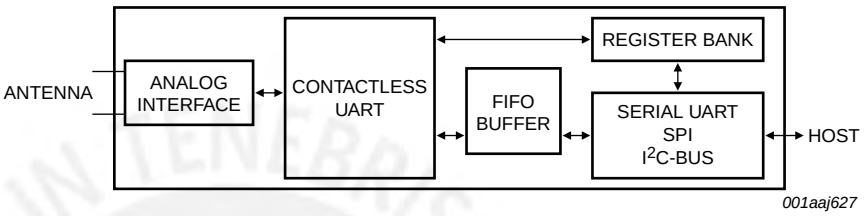


Fig 1. Simplified block diagram of the MFRC522

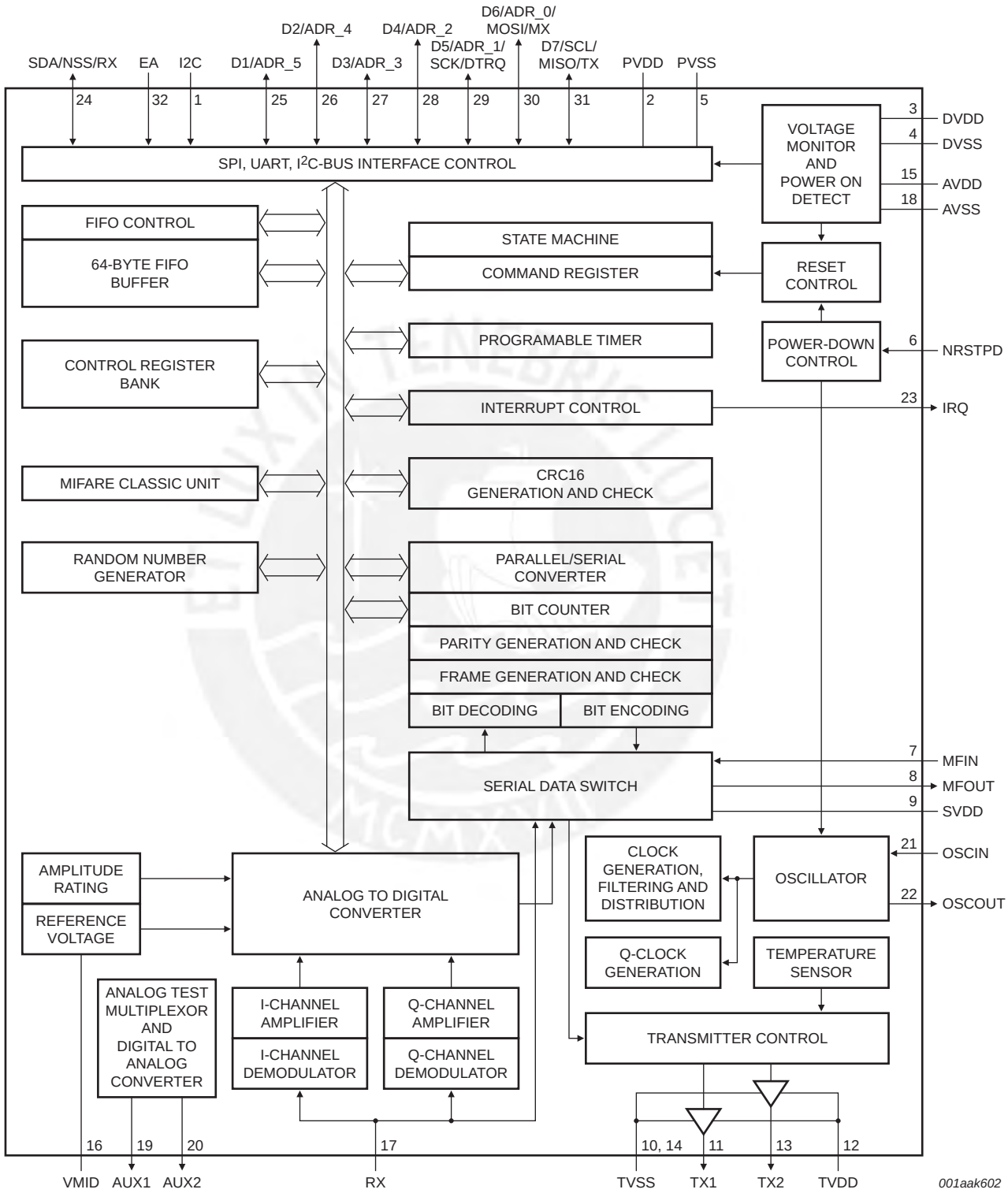


Fig 2. Detailed block diagram of the MFRC522

7. Pinning information

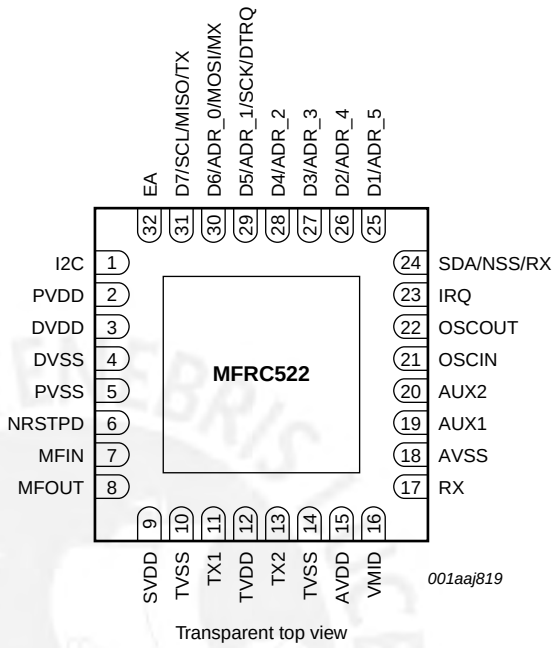


Fig 3. Pinning configuration HVQFN32 (SOT617-1)

7.1 Pin description

Table 3. Pin description

Pin	Symbol	Type[1]	Description
1	I2C	I	I^2C-bus enable input[2]
2	PVDD	P	pin power supply
3	DVDD	P	digital power supply
4	DVSS	G	digital ground[3]
5	PVSS	G	pin power supply ground
6	NRSTPD	I	reset and power-down input: power-down: enabled when LOW; internal current sinks are switched off, the oscillator is inhibited and the input pins are disconnected from the outside world reset: enabled by a positive edge
7	MFIN	I	MIFARE signal input
8	MFOUT	O	MIFARE signal output
9	SVDD	P	MFIN and MFOUT pin power supply
10	TVSS	G	transmitter output stage 1 ground
11	TX1	O	transmitter 1 modulated 13.56 MHz energy carrier output
12	TVDD	P	transmitter power supply: supplies the output stage of transmitters 1 and 2
13	TX2	O	transmitter 2 modulated 13.56 MHz energy carrier output
14	TVSS	G	transmitter output stage 2 ground
15	AVDD	P	analog power supply

Table 3. Pin description *...continued*

Pin	Symbol	Type[1]	Description
16	VMID	P	internal reference voltage
17	RX	I	RF signal input
18	AVSS	G	analog ground
19	AUX1	O	auxiliary outputs for test purposes
20	AUX2	O	auxiliary outputs for test purposes
21	OSCIN	I	crystal oscillator inverting amplifier input; also the input for an externally generated clock (f_{clk} = 27.12 MHz)
22	OSCOUT	O	crystal oscillator inverting amplifier output
23	IRQ	O	interrupt request output: indicates an interrupt event
24	SDA	I/O	I^2C-bus serial data line input/output[2]
	NSS	I	SPI signal input[2]
	RX	I	UART address input[2]
25	D1	I/O	test port[2]
	ADR_5	I/O	I^2C-bus address 5 input[2]
26	D2	I/O	test port
	ADR_4	I	I^2C-bus address 4 input[2]
27	D3	I/O	test port
	ADR_3	I	I^2C-bus address 3 input[2]
28	D4	I/O	test port
	ADR_2	I	I^2C-bus address 2 input[2]
29	D5	I/O	test port
	ADR_1	I	I^2C-bus address 1 input[2]
	SCK	I	SPI serial clock input[2]
	DTRQ	O	UART request to send output to microcontroller[2]
30	D6	I/O	test port
	ADR_0	I	I^2C-bus address 0 input[2]
	MOSI	I/O	SPI master out, slave in[2]
	MX	O	UART output to microcontroller[2]
31	D7	I/O	test port
	SCL	I/O	I^2C-bus clock input/output[2]
	MISO	I/O	SPI master in, slave out[2]
	TX	O	UART data output to microcontroller[2]
32	EA	I	external address input for coding I^2C-bus address[2]

[1] Pin types: I = Input, O = Output, I/O = Input/Output, P = Power and G = Ground.

[2] The pin functionality of these pins is explained in Section 8.1 “Digital interfaces”.

[3] Connection of heatsink pad on package bottom side is not necessary. Optional connection to pin DVSS is possible.

8. Functional description

The MFRC522 transmission module supports the Read/Write mode for ISO/IEC 14443 A/MIFARE using various transfer speeds and modulation protocols.

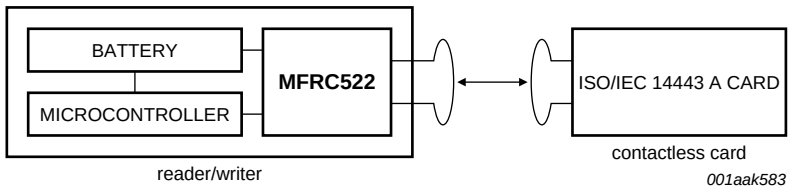
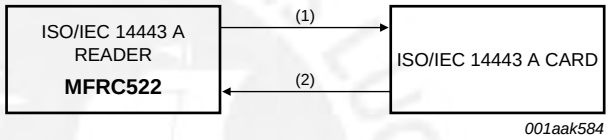


Fig 4. MFRC522 Read/Write mode

The physical level communication is shown in Figure 5.



(1) Reader to card 100 % ASK, Miller encoded, transfer speed 106 kBd to 848 kBd.

(2) Card to reader subcarrier load modulation, Manchester encoded or BPSK, transfer speed 106 kBd to 848 kBd.

Fig 5. ISO/IEC 14443 A/MIFARE Read/Write mode communication diagram

The physical parameters are described in Table 4.

Table 4. Communication overview for ISO/IEC 14443 A/MIFARE reader/writer

Communication direction	Signal type	Transfer speed			
		106 kBd	212 kBd	424 kBd	848 kBd
Reader to card (send data from the MFRC522 to a card)	reader side modulation	100 % ASK	100 % ASK	100 % ASK	100 % ASK
	bit encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding
	bit length	128 (13.56 μs)	64 (13.56 μs)	32 (13.56 μs)	16 (13.56 μs)
Card to reader (MFRC522 receives data from a card)	card side modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz / 16	13.56 MHz / 16	13.56 MHz / 16	13.56 MHz / 16
	bit encoding	Manchester encoding	BPSK	BPSK	BPSK

The MFRC522's contactless UART and dedicated external host must manage the complete ISO/IEC 14443 A/MIFARE protocol. Figure 6 shows the data coding and framing according to ISO/IEC 14443 A/MIFARE.

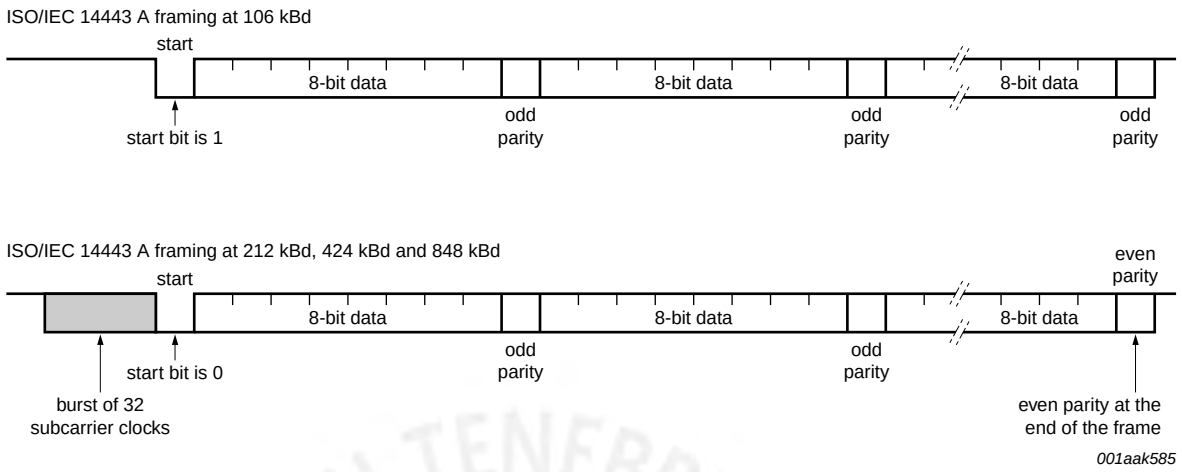


Fig 6. Data coding and framing according to ISO/IEC 14443 A

The internal CRC coprocessor calculates the CRC value based on ISO/IEC 14443 A part 3 and handles parity generation internally according to the transfer speed. Automatic parity generation can be switched off using the MfRxReg register's ParityDisable bit.

8.1 Digital interfaces

8.1.1 Automatic microcontroller interface detection

The MFRC522 supports direct interfacing of hosts using SPI, I^2C-bus or serial UART interfaces. The MFRC522 resets its interface and checks the current host interface type automatically after performing a power-on or hard reset. The MFRC522 identifies the host interface by sensing the logic levels on the control pins after the reset phase. This is done using a combination of fixed pin connections. Table 5 shows the different connection configurations.

Table 5. Connection protocol for detecting different interface types

Pin	Interface type		
	UART (input)	**SPI (output)**	**I^2C-bus (I/O)**
SDA	RX	NSS	SDA
I2C	0	0	1
EA	0	1	EA
D7	TX	MISO	SCL
D6	MX	MOSI	ADR_0
D5	DTRQ	SCK	ADR_1
D4	-	-	ADR_2
D3	-	-	ADR_3
D2	-	-	ADR_4
D1	-	-	ADR_5

8.1.2 Serial Peripheral Interface

A serial peripheral interface (SPI compatible) is supported to enable high-speed communication to the host. The interface can handle data speeds up to 10 Mbit/s. When communicating with a host, the MFRC522 acts as a slave, receiving data from the external host for register settings, sending and receiving data relevant for RF interface communication.

An interface compatible with SPI enables high-speed serial communication between the MFRC522 and a microcontroller. The implemented interface is in accordance with the SPI standard.

The timing specification is given in Section 14.1 on page 78.

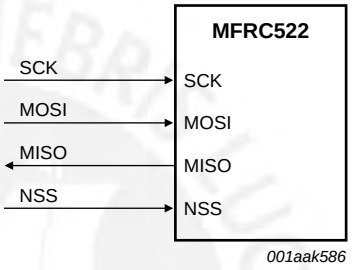


Fig 7. SPI connection to host

The MFRC522 acts as a slave during SPI communication. The SPI clock signal SCK must be generated by the master. Data communication from the master to the slave uses the MOSI line. The MISO line is used to send data from the MFRC522 to the master.

Data bytes on both MOSI and MISO lines are sent with the MSB first. Data on both MOSI and MISO lines must be stable on the rising edge of the clock and can be changed on the falling edge. Data is provided by the MFRC522 on the falling clock edge and is stable during the rising clock edge.

8.1.2.1 SPI read data

Reading data using SPI requires the byte order shown in Table 6 to be used. It is possible to read out up to n-data bytes.

The first byte sent defines both the mode and the address.

Table 6. MOSI and MISO byte order

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n + 1
MOSI	address 0	address 1	address 2	...	address n	00
MISO	X[1]	data 0	data 1	...	data n – 1	data n

[1] X = Do not care.

Remark: The MSB must be sent first.

8.1.2.2 SPI write data

To write data to the MFRC522 using SPI requires the byte order shown in Table 7. It is possible to write up to n data bytes by only sending one address byte.

The first send byte defines both the mode and the address byte.

Table 7. MOSI and MISO byte order

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n + 1
MOSI	address 0	data 0	data 1	...	data n – 1	data n
MISO	X[1]	X[1]	X[1]	...	X[1]	X[1]

[1] X = Do not care.

Remark: The MSB must be sent first.

8.1.2.3 SPI address byte

The address byte must meet the following format.

The MSB of the first byte defines the mode used. To read data from the MFRC522 the MSB is set to logic 1. To write data to the MFRC522 the MSB must be set to logic 0. Bits 6 to 1 define the address and the LSB is set to logic 0.

Table 8. Address byte 0 register; address MOSI

7 (MSB)	6	5	4	3	2	1	0 (LSB)
1 = read 0 = write	address						0

8.1.3 UART interface

8.1.3.1 Connection to a host

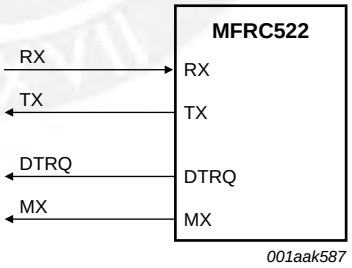


Fig 8. UART connection to microcontrollers

Remark: Signals DTRQ and MX can be disabled by clearing TestPinEnReg register's RS232LineEn bit.

8.1.3.2 Selectable UART transfer speeds

The internal UART interface is compatible with an RS232 serial interface.

The default transfer speed is 9.6 kBd. To change the transfer speed, the host controller must write a value for the new transfer speed to the SerialSpeedReg register. Bits BR_T0[2:0] and BR_T1[4:0] define the factors for setting the transfer speed in the SerialSpeedReg register.

The BR_T0[2:0] and BR_T1[4:0] settings are described in Table 9. Examples of different transfer speeds and the relevant register settings are given in Table 10.

Table 9. BR_T0 and BR_T1 settings

BR_Tn	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
BR_T0 factor	1	1	2	4	8	16	32	64
BR_T1 range	1 to 32	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64

Table 10. Selectable UART transfer speeds

Transfer speed (kBd)	SerialSpeedReg value		Transfer speed accuracy (%)[1]
	Decimal	Hexadecimal	
7.2	250	FAh	–0.25
9.6	235	EBh	0.32
14.4	218	DAh	–0.25
19.2	203	CBh	0.32
38.4	171	ABh	0.32
57.6	154	9Ah	–0.25
115.2	122	7Ah	–0.25
128	116	74h	–0.06
230.4	90	5Ah	–0.25
460.8	58	3Ah	–0.25
921.6	28	1Ch	1.45
1228.8	21	15h	0.32

[1] The resulting transfer speed error is less than 1.5 % for all described transfer speeds.

The selectable transfer speeds shown in Table 10 are calculated according to the following equations:

If BR_T0[2:0] = 0:

$$transfer\ speed = \frac{27.12 \times 10^6}{(BR\_T0 + 1)} \quad (1)$$

If BR_T0[2:0] > 0:

$$transfer\ speed = \left(\frac{27.12 \times 10^6}{(BR\_T1 + 33)} \right) \Big/ 2^{(BR\_T0 - 1)} \quad (2)$$

Remark: Transfer speeds above 1228.8 kBd are not supported.

8.1.3.3 UART framing

Table 11. UART framing

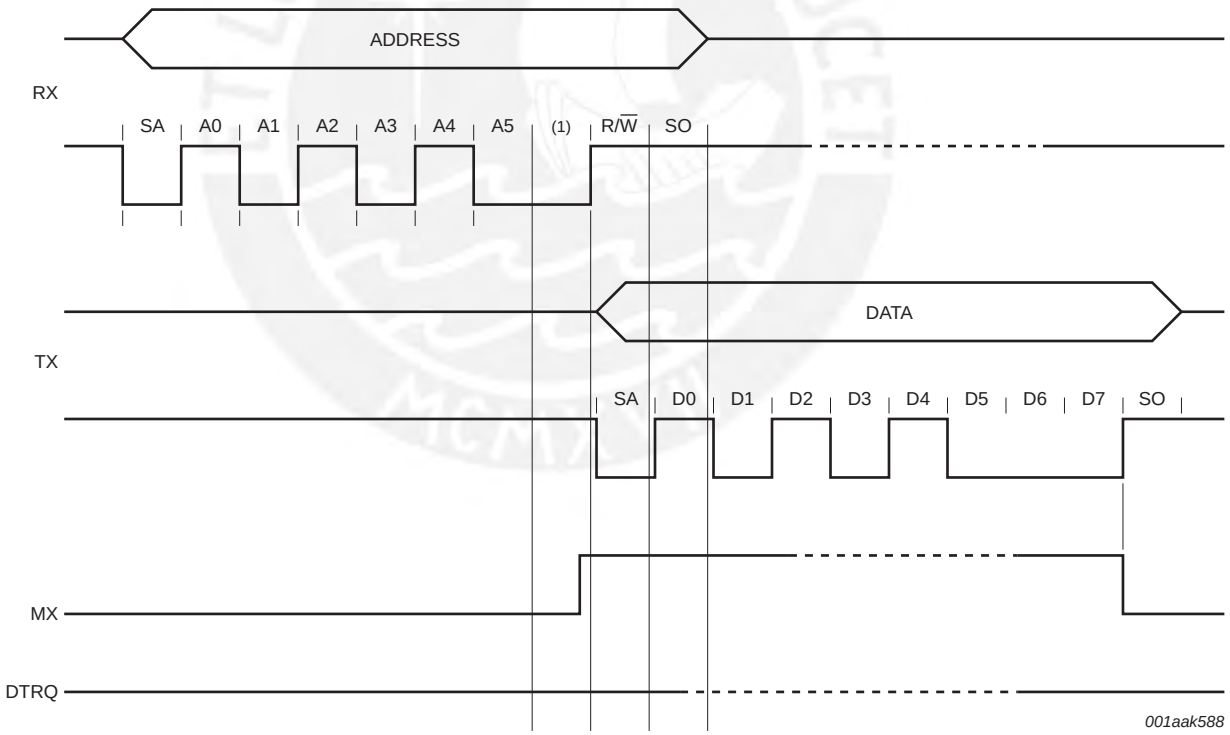
Bit	Length	Value
Start	1-bit	0
Data	8 bits	data
Stop	1-bit	1

Remark: The LSB for data and address bytes must be sent first. No parity bit is used during transmission.

Read data: To read data using the UART interface, the flow shown in Table 12 must be used. The first byte sent defines both the mode and the address.

Table 12. Read data byte order

Pin	Byte 0	Byte 1
RX (pin 24)	address	-
TX (pin 31)	-	data 0



(1) Reserved.

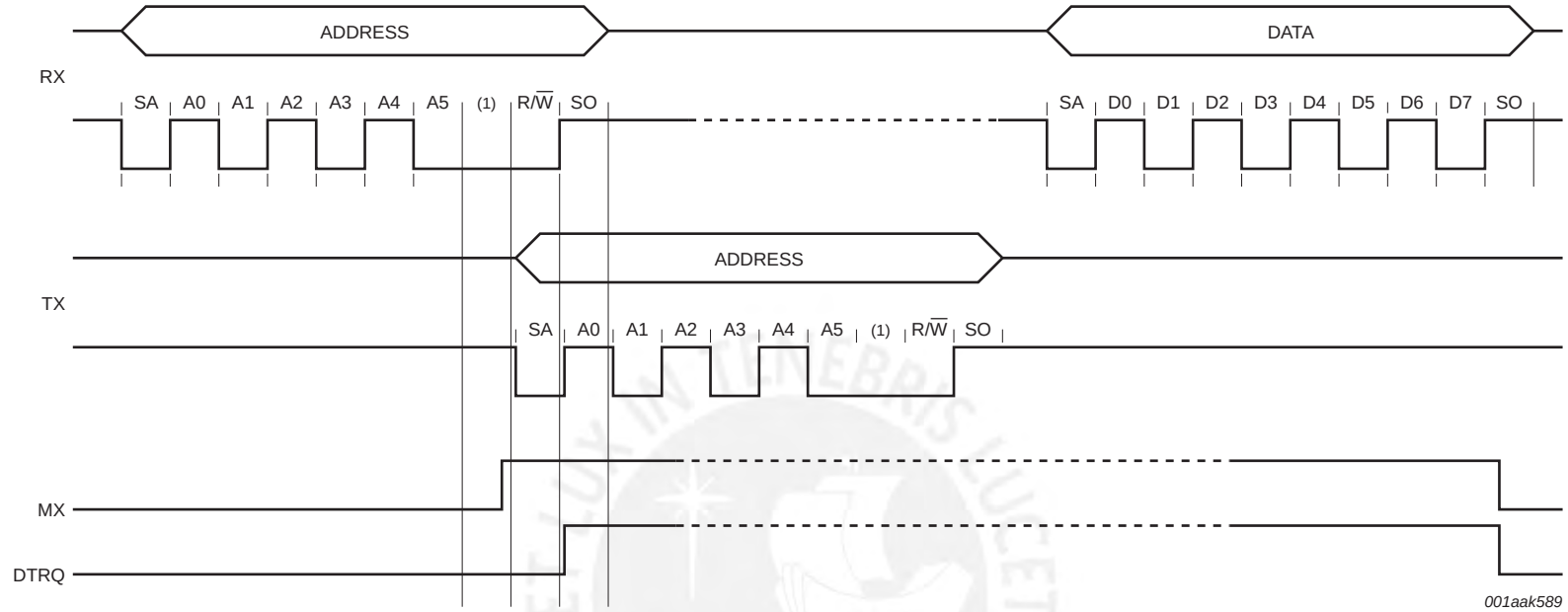
Fig 9. UART read data timing diagram

Write data: To write data to the MFRC522 using the UART interface, the structure shown in Table 13 must be used.

The first byte sent defines both the mode and the address.

Table 13. Write data byte order

Pin	Byte 0	Byte 1
RX (pin 24)	address 0	data 0
TX (pin 31)	-	address 0



(1) Reserved.

Fig 10. UART write data timing diagram

Remark: The data byte can be sent directly after the address byte on pin RX.

Address byte: The address byte has to meet the following format:

The MSB of the first byte sets the mode used. To read data from the MFRC522, the MSB is set to logic 1. To write data to the MFRC522 the MSB is set to logic 0. Bit 6 is reserved for future use, and bits 5 to 0 define the address; see Table 14.

Table 14. Address byte 0 register; address MOSI

7 (MSB)	6	5	4	3	2	1	0 (LSB)
1 = read 0 = write	reserved	address					

8.1.4 I²C-bus interface

An I²C-bus (Inter-IC) interface is supported to enable a low-cost, low pin count serial bus interface to the host. The I²C-bus interface is implemented according to NXP Semiconductors' *I²C-bus interface specification, rev. 2.1, January 2000*. The interface can only act in Slave mode. Therefore the MFRC522 does not implement clock generation or access arbitration.

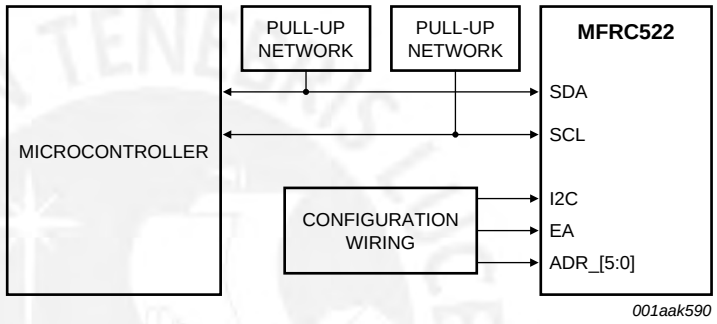


Fig 11. I²C-bus interface

The MFRC522 can act either as a slave receiver or slave transmitter in Standard mode, Fast mode and High-speed mode.

SDA is a bidirectional line connected to a positive supply voltage using a current source or a pull-up resistor. Both SDA and SCL lines are set HIGH when data is not transmitted. The MFRC522 has a 3-state output stage to perform the wired-AND function. Data on the I²C-bus can be transferred at data rates of up to 100 kBd in Standard mode, up to 400 kBd in Fast mode or up to 3.4 Mbit/s in High-speed mode.

If the I²C-bus interface is selected, spike suppression is activated on lines SCL and SDA as defined in the I²C-bus interface specification.

See Table 155 on page 79 for timing requirements.

8.1.4.1 Data validity

Data on the SDA line must be stable during the HIGH clock period. The HIGH or LOW state of the data line must only change when the clock signal on SCL is LOW.

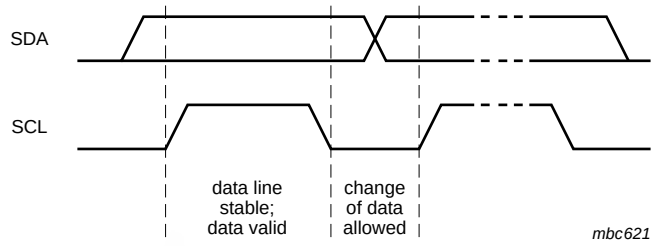


Fig 12. Bit transfer on the I²C-bus

8.1.4.2 START and STOP conditions

To manage the data transfer on the I²C-bus, unique START (S) and STOP (P) conditions are defined.

- A START condition is defined with a HIGH-to-LOW transition on the SDA line while SCL is HIGH.
- A STOP condition is defined with a LOW-to-HIGH transition on the SDA line while SCL is HIGH.

The I²C-bus master always generates the START and STOP conditions. The bus is busy after the START condition. The bus is free again a certain time after the STOP condition.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. The START (S) and repeated START (Sr) conditions are functionally identical. Therefore, S is used as a generic term to represent both the START (S) and repeated START (Sr) conditions.

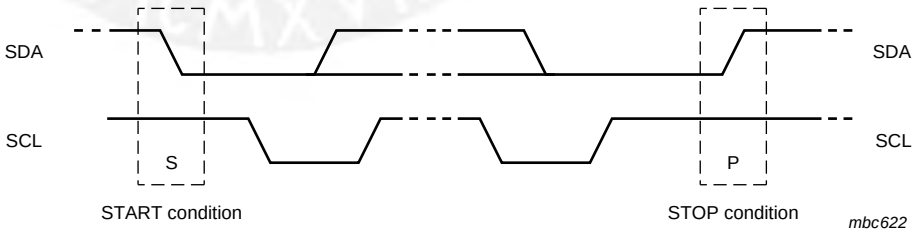


Fig 13. START and STOP conditions

8.1.4.3 Byte format

Each byte must be followed by an acknowledge bit. Data is transferred with the MSB first; see Figure 16. The number of transmitted bytes during one data transfer is unrestricted but must meet the read/write cycle format.

8.1.4.4 Acknowledge

An acknowledge must be sent at the end of one data byte. The acknowledge-related clock pulse is generated by the master. The transmitter of data, either master or slave, releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver pulls down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.

The master can then generate either a STOP (P) condition to stop the transfer or a repeated START (Sr) condition to start a new transfer.

A master-receiver indicates the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out by the slave. The slave-transmitter releases the data line to allow the master to generate a STOP (P) or repeated START (Sr) condition.

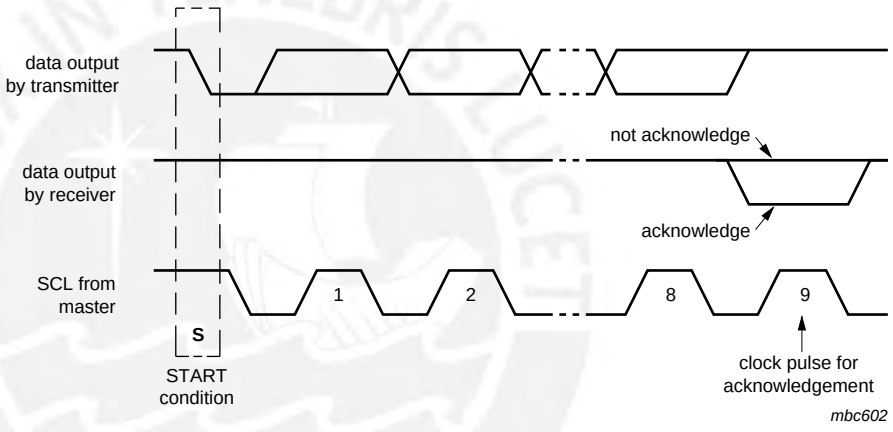


Fig 14. Acknowledge on the I²C-bus

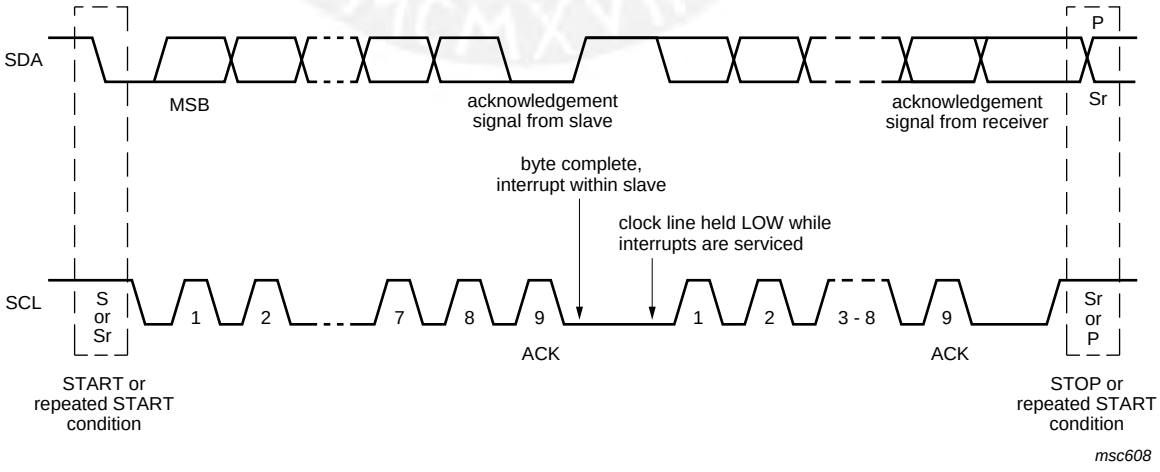


Fig 15. Data transfer on the I²C-bus

8.1.4.5 7-Bit addressing

During the I²C-bus address procedure, the first byte after the START condition is used to determine which slave will be selected by the master.

Several address numbers are reserved. During device configuration, the designer must ensure that collisions with these reserved addresses cannot occur. Check the *I²C-bus specification* for a complete list of reserved addresses.

The I²C-bus address specification is dependent on the definition of pin EA. Immediately after releasing pin NRSTPD or after a power-on reset, the device defines the I²C-bus address according to pin EA.

If pin EA is set LOW, the upper 4 bits of the device bus address are reserved by NXP Semiconductors and set to 0101b for all MFRC522 devices. The remaining 3 bits (ADR_0, ADR_1, ADR_2) of the slave address can be freely configured by the customer to prevent collisions with other I²C-bus devices.

If pin EA is set HIGH, ADR_0 to ADR_5 can be completely specified at the external pins according to Table 5 on page 9. ADR_6 is always set to logic 0.

In both modes, the external address coding is latched immediately after releasing the reset condition. Further changes at the used pins are not taken into consideration. Depending on the external wiring, the I²C-bus address pins can be used for test signal outputs.

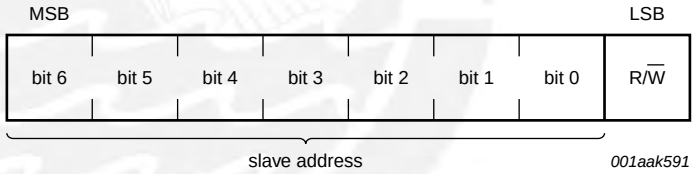


Fig 16. First byte following the START procedure

8.1.4.6 Register write access

To write data from the host controller using the I²C-bus to a specific register in the MFRC522 the following frame format must be used.

- The first byte of a frame indicates the device address according to the I²C-bus rules.
- The second byte indicates the register address followed by up to n-data bytes.

In one frame all data bytes are written to the same register address. This enables fast FIFO buffer access. The Read/Write (R/$\overline{W}$) bit is set to logic 0.

8.1.4.7 Register read access

To read out data from a specific register address in the MFRC522, the host controller must use the following procedure:

- Firstly, a write access to the specific register address must be performed as indicated in the frame that follows
- The first byte of a frame indicates the device address according to the I²C-bus rules
- The second byte indicates the register address. No data bytes are added
- The Read/Write bit is 0

After the write access, read access can start. The host sends the device address of the MFRC522. In response, the MFRC522 sends the content of the read access register. In one frame all data bytes can be read from the same register address. This enables fast FIFO buffer access or register polling.

The Read/Write (R/W) bit is set to logic 1.

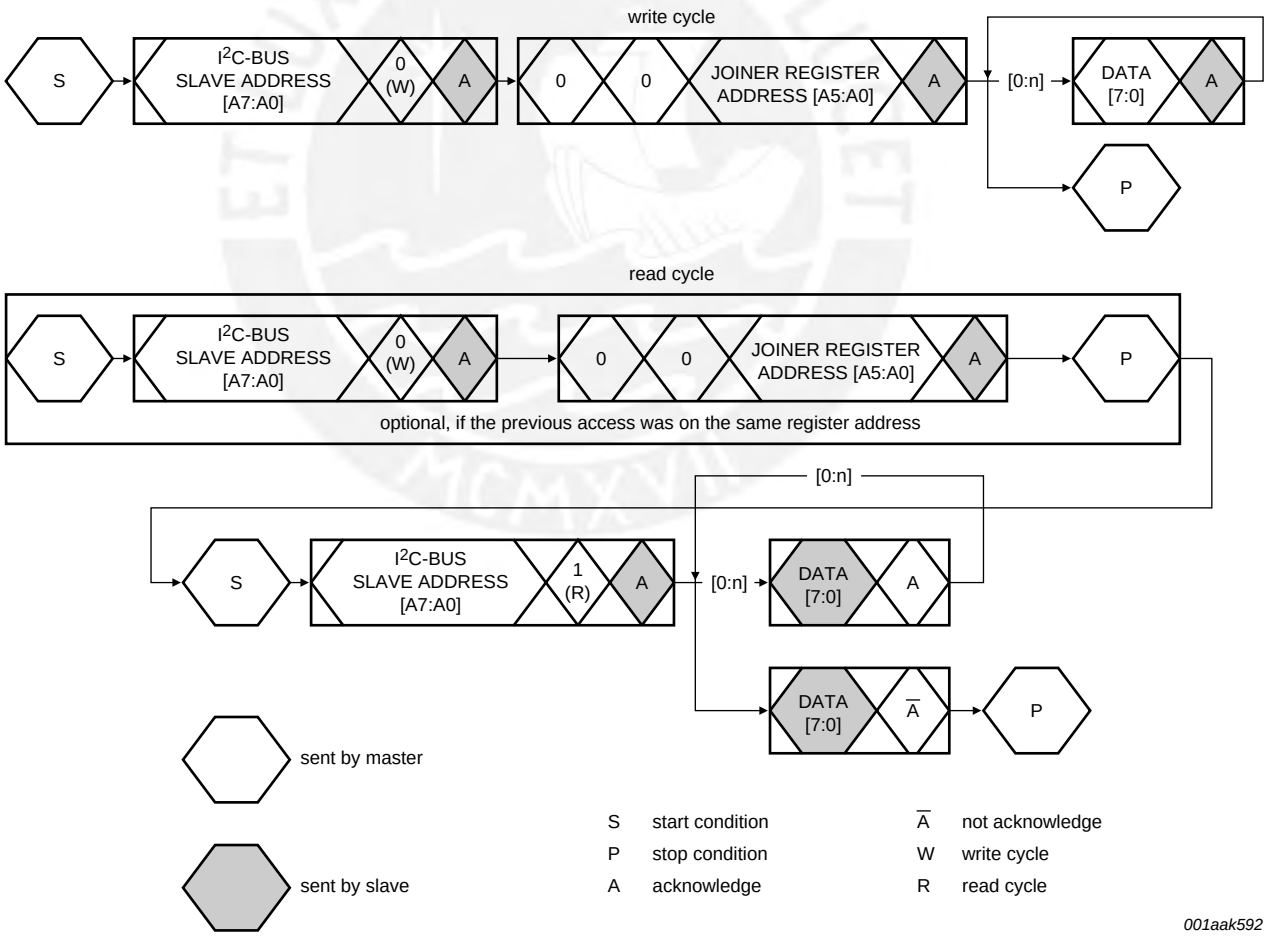


Fig 17. Register read and write access

8.1.4.8 High-speed mode

In High-speed mode (HS mode), the device can transfer information at data rates of up to 3.4 Mbit/s, while remaining fully downward-compatible with Fast or Standard mode (F/S mode) for bidirectional communication in a mixed-speed bus system.

8.1.4.9 High-speed transfer

To achieve data rates of up to 3.4 Mbit/s the following improvements have been made to I^2C-bus operation.

- The inputs of the device in HS mode incorporate spike suppression, a Schmitt trigger on the SDA and SCL inputs and different timing constants when compared to F/S mode
- The output buffers of the device in HS mode incorporate slope control of the falling edges of the SDA and SCL signals with different fall times compared to F/S mode

8.1.4.10 Serial data transfer format in HS mode

The HS mode serial data transfer format meets the Standard mode I^2C-bus specification. HS mode can only start after all of the following conditions (all of which are in F/S mode):

1. START condition (S)
2. 8-bit master code (00001XXXb)
3. Not-acknowledge bit ($\overline{A}$)

When HS mode starts, the active master sends a repeated START condition (Sr) followed by a 7-bit slave address with a R/W bit address and receives an acknowledge bit (A) from the selected MFRC522.

Data transfer continues in HS mode after the next repeated START (Sr), only switching back to F/S mode after a STOP condition (P). To reduce the overhead of the master code, a master links a number of HS mode transfers, separated by repeated START conditions (Sr).

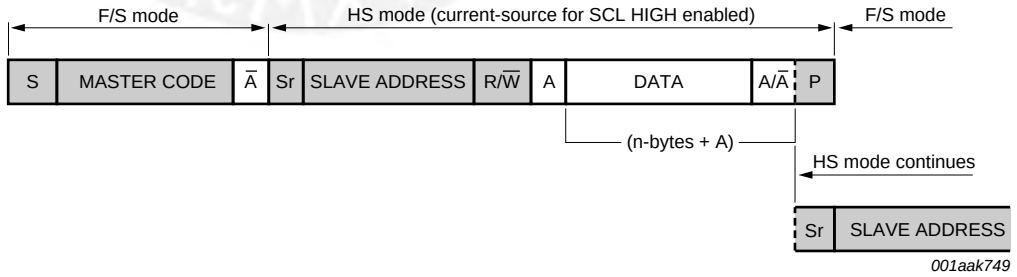


Fig 18. I^2C-bus HS mode protocol switch

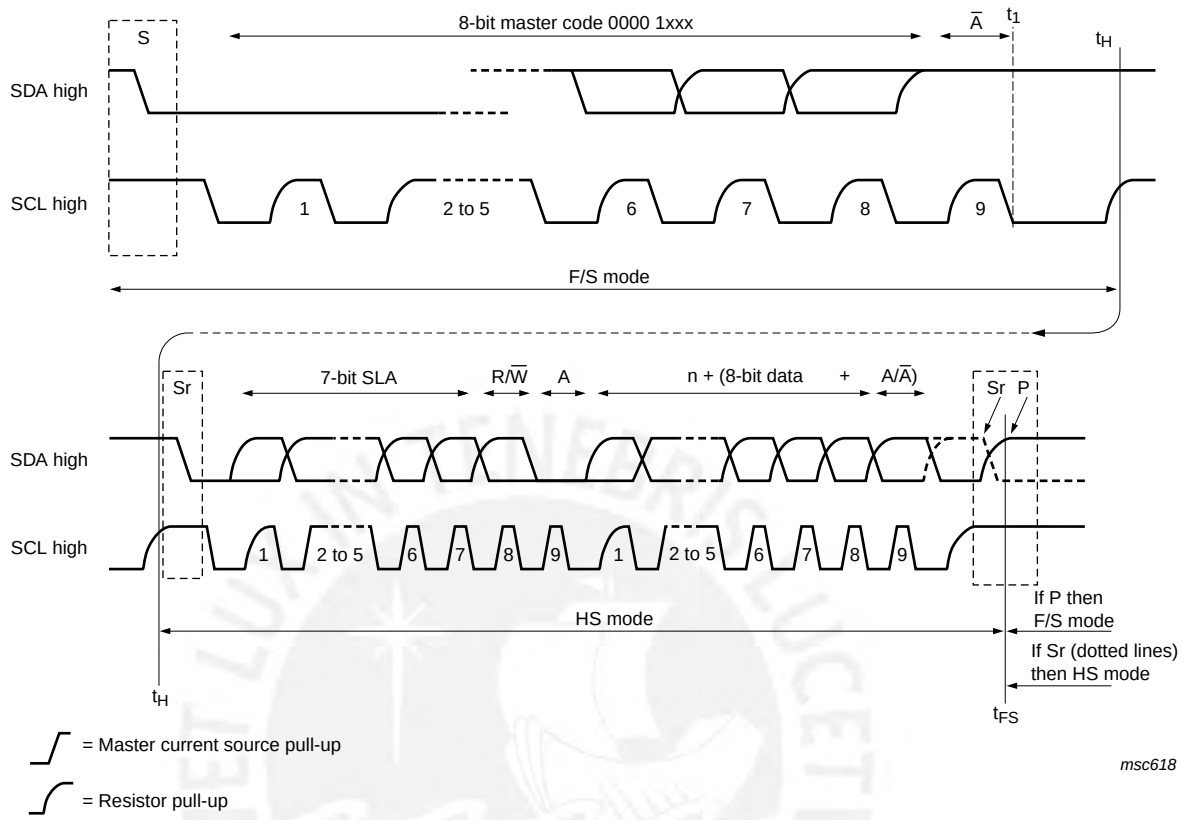


Fig 19. I²C-bus HS mode protocol frame

8.1.4.11 Switching between F/S mode and HS mode

After reset and initialization, the MFRC522 is in Fast mode (which is in effect F/S mode as Fast mode is downward-compatible with Standard mode). The connected MFRC522 recognizes the “S 00001XXX A” sequence and switches its internal circuitry from the Fast mode setting to the HS mode setting.

The following actions are taken:

1. Adapt the SDA and SCL input filters according to the spike suppression requirement in HS mode.
2. Adapt the slope control of the SDA output stages.

It is possible for system configurations that do not have other I^2C-bus devices involved in the communication to switch to HS mode permanently. This is implemented by setting Status2Reg register’s I^2CForceHS bit to logic 1. In permanent HS mode, the master code is not required to be sent. This is not defined in the specification and must only be used when no other devices are connected on the bus. In addition, spikes on the I^2C-bus lines must be avoided because of the reduced spike suppression.

8.1.4.12 MFRC522 at lower speed modes

MFRC522 is fully downward-compatible and can be connected to an F/S mode I^2C-bus system. The device stays in F/S mode and communicates at F/S mode speeds because a master code is not transmitted in this configuration.

8.2 Analog interface and contactless UART

8.2.1 General

The integrated contactless UART supports the external host online with framing and error checking of the protocol requirements up to 848 kBd. An external circuit can be connected to the communication interface pins MFIN and MFOUT to modulate and demodulate the data.

The contactless UART handles the protocol requirements for the communication protocols in cooperation with the host. Protocol handling generates bit and byte-oriented framing. In addition, it handles error detection such as parity and CRC, based on the various supported contactless communication protocols.

Remark: The size and tuning of the antenna and the power supply voltage have an important impact on the achievable operating distance.

8.2.2 TX p-driver

The signal on pins TX1 and TX2 is the 13.56 MHz energy carrier modulated by an envelope signal. It can be used to drive an antenna directly using a few passive components for matching and filtering; see Section 15 on page 81. The signal on pins TX1 and TX2 can be configured using the TxControlReg register; see Section 9.3.2.5 on page 50.

The modulation index can be set by adjusting the impedance of the drivers. The impedance of the p-driver can be configured using registers CWGsPReg and ModGsPReg. The impedance of the n-driver can be configured using the GsNReg register. The modulation index also depends on the antenna design and tuning.

The TxModeReg and TxSelReg registers control the data rate and framing during transmission and the antenna driver setting to support the different requirements at the different modes and transfer speeds.

Table 15. Register and bit settings controlling the signal on pin TX1

Bit Tx1RFEn	Bit Force 100ASK	Bit InvTx1RFOn	Bit InvTx1RFOff	Envelope	Pin TX1	GSPMos	GSNMos	Remarks
0	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	not specified if RF is switched off
1	0	0	X[1]	0	RF	pMod	nMod	100 % ASK: pin TX1 pulled to logic 0, independent of the InvTx1RFOff bit
				1	RF	pCW	nCW	
	0	1	X[1]	0	RF	pMod	nMod	
				1	RF	pCW	nCW	
	1	1	X[1]	0	0	pMod	nMod	
				1	RF_n	pCW	nCW	

[1] X = Do not care.

Table 16. Register and bit settings controlling the signal on pin TX2

Bit Tx1RFEn	Bit Force 100ASK	Bit Tx2CW	Bit InvTx2RFOn	Bit InvTx2RFOff	Envelope	Pin TX2	GSPMos	GSNMos	Remarks
0	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	not specified if RF is switched off
1	0	0	0	X[1]	0	RF	pMod	nMod	-
					1	RF	pCW	nCW	
			1	X[1]	0	RF_n	pMod	nMod	
					1	RF_n	pCW	nCW	
		1	0	X[1]	X[1]	RF	pCW	nCW	conductance always CW for the Tx2CW bit
			1	X[1]	X[1]	RF_n	pCW	nCW	
	1	0	0	X[1]	0	0	pMod	nMod	100 % ASK: pin TX2 pulled to logic 0 (independent of the InvTx2RFOn/InvTx2RFOff bits)
					1	RF	pCW	nCW	
			1	X[1]	0	0	pMod	nMod	
					1	RF_n	pCW	nCW	
		1	0	X[1]	X[1]	RF	pCW	nCW	
			1	X[1]	X[1]	RF_n	pCW	nCW	

[1] X = Do not care.

The following abbreviations have been used in Table 15 and Table 16:

- RF: 13.56 MHz clock derived from 27.12 MHz quartz crystal oscillator divided by 2
- RF_n: inverted 13.56 MHz clock
- GSPMos: conductance, configuration of the PMOS array
- GSNMos: conductance, configuration of the NMOS array
- pCW: PMOS conductance value for continuous wave defined by the CWGsPReg register
- pMod: PMOS conductance value for modulation defined by the ModGsPReg register
- nCW: NMOS conductance value for continuous wave defined by the GsNReg register's CWGsN[3:0] bits
- nMod: NMOS conductance value for modulation defined by the GsNReg register's ModGsN[3:0] bits
- X = do not care.

Remark: If only one driver is switched on, the values for CWGsPReg, ModGsPReg and GsNReg registers are used for both drivers.

8.2.3 Serial data switch

Two main blocks are implemented in the MFRC522. The digital block comprises the state machines, encoder/decoder logic. The analog block comprises the modulator and antenna drivers, the receiver and amplifiers. It is possible for the interface between these two blocks to be configured so that the interfacing signals are routed to pins MFIN and MFOUT.

This topology allows the analog block of the MFRC522 to be connected to the digital block of another device.

The serial signal switch is controlled by the TxSelReg and RxSelReg registers.

Figure 20 shows the serial data switch for p-driver TX1 and TX2.

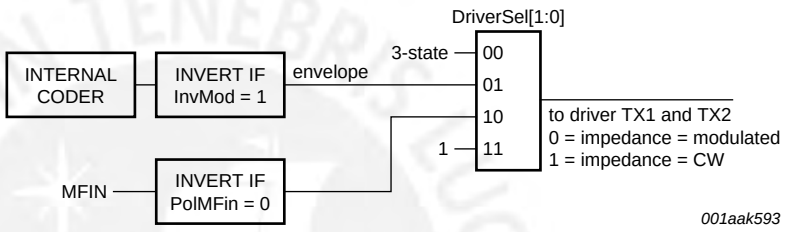


Fig 20. Serial data switch for p-driver TX1 and TX2

8.2.4 MFIN and MFOUT interface support

The MFRC522 is divided into a digital circuit block and an analog circuit block. The digital block contains state machines, encoder and decoder logic and so on. The analog block contains the modulator and antenna drivers, receiver and amplifiers. The interface between these two blocks can be configured so that the interfacing signals can be routed to pins MFIN and MFOUT; see Figure 21 on page 28. This configuration is implemented using TxSelReg register's MFOutSel[3:0] and DriverSel[1:0] bits and RxSelReg register's UARTSel[1:0] bits.

This topology allows some parts of the analog block to be connected to the digital block of another device.

Switch MFOutSel in the TxSelReg register can be used to measure MIFARE and ISO/IEC14443 A related signals. This is especially important during the design-in phase or for test purposes as it enables checking of the transmitted and received data.

The most important use of pins MFIN and MFOUT is found in the active antenna concept. An external active antenna circuit can be connected to the MFRC522's digital block. Switch MFOutSel must be configured so that the internal Miller encoded signal is sent to pin MFOUT (MFOutSel = 100b). UARTSel[1:0] must be configured to receive a Manchester signal with subcarrier from pin MFIN (UARTSel[1:0] = 01).

It is possible to connect a passive antenna to pins TX1, TX2 and RX (using the appropriate filter and matching circuit) and an active antenna to pins MFOUT and MFIN at the same time. In this configuration, two RF circuits can be driven (one after another) by a single host processor.

Remark: Pins MFIN and MFOUT have a dedicated supply on pin SVDD with the ground on pin PVSS. If pin MFIN is not used it must be connected to either pin SVDD or pin PVSS. If pin SVDD is not used it must be connected to either pin DVDD, pin PVDD or any other voltage supply pin.

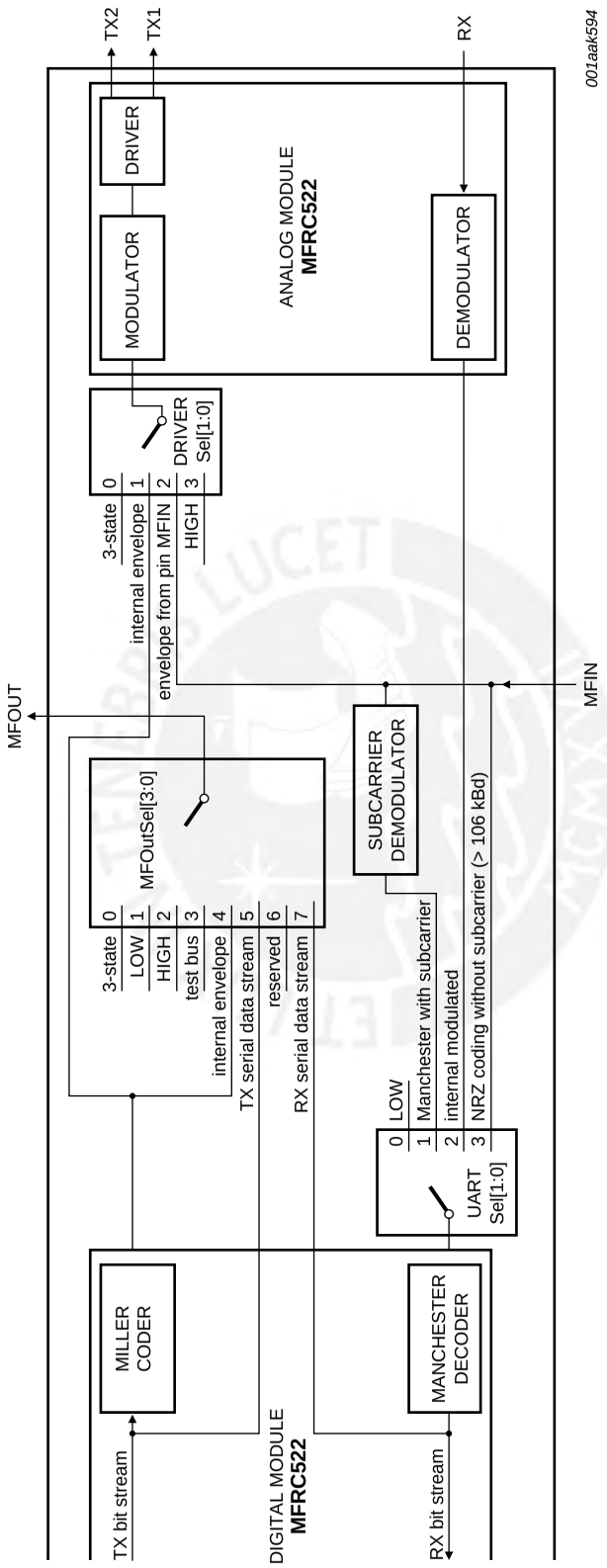


Fig 21. Overview of MFIN and MFOUT signal routing

8.2.5 CRC coprocessor

The following CRC coprocessor parameters can be configured:

- The CRC preset value can be either 0000h, 6363h, A671h or FFFFh depending on the ModeReg register's CRCPreset[1:0] bits setting
- The CRC polynomial for the 16-bit CRC is fixed to $x^{16} + x^{12} + x^5 + 1$
- The CRCResultReg register indicates the result of the CRC calculation. This register is split into two 8-bit registers representing the higher and lower bytes.
- The ModeReg register's MSBFirst bit indicates that data will be loaded with the MSB first.

Table 17. CRC coprocessor parameters

Parameter	Value
CRC register length	16-bit CRC
CRC algorithm	algorithm according to ISO/IEC 14443 A and ITU-T
CRC preset value	0000h, 6363h, A671h or FFFFh depending on the setting of the ModeReg register's CRCPreset[1:0] bits

8.3 FIFO buffer

An 8 × 64 bit FIFO buffer is used in the MFRC522. It buffers the input and output data stream between the host and the MFRC522's internal state machine. This makes it possible to manage data streams up to 64 bytes long without the need to take timing constraints into account.

8.3.1 Accessing the FIFO buffer

The FIFO buffer input and output data bus is connected to the FIFODataReg register. Writing to this register stores one byte in the FIFO buffer and increments the internal FIFO buffer write pointer. Reading from this register shows the FIFO buffer contents stored in the FIFO buffer read pointer and decrements the FIFO buffer read pointer. The distance between the write and read pointer can be obtained by reading the FIFOLevelReg register.

When the microcontroller starts a command, the MFRC522 can, while the command is in progress, access the FIFO buffer according to that command. Only one FIFO buffer has been implemented which can be used for input and output. The microcontroller must ensure that there are not any unintentional FIFO buffer accesses.

8.3.2 Controlling the FIFO buffer

The FIFO buffer pointers can be reset by setting FIFOLevelReg register's FlushBuffer bit to logic 1. Consequently, the FIFOLevel[6:0] bits are all set to logic 0 and the ErrorReg register's BufferOvfl bit is cleared. The bytes stored in the FIFO buffer are no longer accessible allowing the FIFO buffer to be filled with another 64 bytes.

8.3.3 FIFO buffer status information

The host can get the following FIFO buffer status information:

- Number of bytes stored in the FIFO buffer: FIFOLevelReg register's FIFOLevel[6:0]
- FIFO buffer almost full warning: Status1Reg register's HiAlert bit

- FIFO buffer almost empty warning: Status1Reg register's LoAlert bit
- FIFO buffer overflow warning: ErrorReg register's BufferOvfl bit. The BufferOvfl bit can only be cleared by setting the FIFOLevelReg register's FlushBuffer bit.

The MFRC522 can generate an interrupt signal when:

- ComIEnReg register's LoAlertIEn bit is set to logic 1. It activates pin IRQ when Status1Reg register's LoAlert bit changes to logic 1.
- ComIEnReg register's HiAlertIEn bit is set to logic 1. It activates pin IRQ when Status1Reg register's HiAlert bit changes to logic 1.

If the maximum number of WaterLevel bytes (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the HiAlert bit is set to logic 1. It is generated according to Equation 3:

$$HiAlert = (64 - FIFOLength) \leq WaterLevel \quad (3)$$

If the number of WaterLevel bytes (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the LoAlert bit is set to logic 1. It is generated according to Equation 4:

$$LoAlert = FIFOLength \leq WaterLevel \quad (4)$$

8.4 Interrupt request system

The MFRC522 indicates certain events by setting the Status1Reg register's IRq bit and, if activated, by pin IRQ. The signal on pin IRQ can be used to interrupt the host using its interrupt handling capabilities. This allows the implementation of efficient host software.

8.4.1 Interrupt sources overview

Table 18 shows the available interrupt bits, the corresponding source and the condition for its activation. The ComIrqReg register's TimerIRq interrupt bit indicates an interrupt set by the timer unit which is set when the timer decrements from 1 to 0.

The ComIrqReg register's TxIRq bit indicates that the transmitter has finished. If the state changes from sending data to transmitting the end of the frame pattern, the transmitter unit automatically sets the interrupt bit. The CRC coprocessor sets the DivIrqReg register's CRCIRq bit after processing all the FIFO buffer data which is indicated by CRCReady bit = 1.

The ComIrqReg register's RxIRq bit indicates an interrupt when the end of the received data is detected. The ComIrqReg register's IdleIRq bit is set if a command finishes and the Command[3:0] value in the CommandReg register changes to idle (see Table 149 on page 70).

The ComIrqReg register's HiAlertIRq bit is set to logic 1 when the Status1Reg register's HiAlert bit is set to logic 1 which means that the FIFO buffer has reached the level indicated by the WaterLevel[5:0] bits.

The ComIrqReg register's LoAlertIRq bit is set to logic 1 when the Status1Reg register's LoAlert bit is set to logic 1 which means that the FIFO buffer has reached the level indicated by the WaterLevel[5:0] bits.

The ComIrqReg register's ErrIRq bit indicates an error detected by the contactless UART during send or receive. This is indicated when any bit is set to logic 1 in register ErrorReg.

Table 18. Interrupt sources

Interrupt flag	Interrupt source	Trigger action
IRq	timer unit	the timer counts from 1 to 0
TxIRq	transmitter	a transmitted data stream ends
CRCIRq	CRC coprocessor	all data from the FIFO buffer has been processed
RxIRq	receiver	a received data stream ends
IdleIRq	ComIrqReg register	command execution finishes
HiAlertIRq	FIFO buffer	the FIFO buffer is almost full
LoAlertIRq	FIFO buffer	the FIFO buffer is almost empty
ErrIRq	contactless UART	an error is detected

8.5 Timer unit

The MFRC522A has a timer unit which the external host can use to manage timing tasks. The timer unit can be used in one of the following timer/counter configurations:

- Timeout counter
- Watchdog counter
- Stop watch
- Programmable one shot
- Periodical trigger

The timer unit can be used to measure the time interval between two events or to indicate that a specific event occurred after a specific time. The timer can be triggered by events explained in the paragraphs below. The timer does not influence any internal events, for example, a time-out during data reception does not automatically influence the reception process. Furthermore, several timer-related bits can be used to generate an interrupt.

The timer has an input clock of 13.56 MHz derived from the 27.12 MHz quartz crystal oscillator. The timer consists of two stages: prescaler and counter.

The prescaler (TPrescaler) is a 12-bit counter. The reload values (TReloadVal_Hi[7:0] and TReloadVal_Lo[7:0]) for TPrescaler can be set between 0 and 4095 in the TModeReg register's TPrescaler_Hi[3:0] bits and TPrescalerReg register's TPrescaler_Lo[7:0] bits.

The reload value for the counter is defined by 16 bits between 0 and 65535 in the TReloadReg register.

The current value of the timer is indicated in the TCounterValReg register.

When the counter reaches 0, an interrupt is automatically generated, indicated by the ComIrqReg register's TimerIRq bit setting. If enabled, this event can be indicated on pin IRQ. The TimerIRq bit can be set and reset by the host. Depending on the configuration, the timer will stop at 0 or restart with the value set in the TReloadReg register.

The timer status is indicated by the Status1Reg register's TRunning bit.

The timer can be started manually using the ControlReg register's TStartNow bit and stopped using the ControlReg register's TStopNow bit.

The timer can also be activated automatically to meet any dedicated protocol requirements by setting the TModeReg register's TAuto bit to logic 1.

The delay time of a timer stage is set by the reload value + 1. The total delay time (t_{d1}) is calculated using Equation 5:

$$t_{d1} = \frac{(TPrescaler \times 2 + 1) \times (TReloadVal + 1)}{13.56\ MHz} \quad (5)$$

An example of calculating total delay time (t_d) is shown in Equation 6, where the TPrescaler value = 4095 and TReloadVal = 65535:

$$39.59\ s = \frac{(4095 \times 2 + 1) \times (65535 + 1)}{13.56\ MHz} \quad (6)$$

Example: To give a delay time of 25 μs requires 339 clock cycles to be counted and a TPrescaler value of 169. This configures the timer to count up to 65535 time-slots for every 25 μs period.

The MFRC522 version 2.0 offers in addition a second prescaler timer. Due to the fact that the prescaler counts down to 0 the prescaler period always count an odd number of clocks (1, 3, 5, ..). This may lead to inaccuracy. The second available prescaler timer implements the possibility to change the prescaler reload value to odd numbers, which results in an even prescaler period. This new prescaler can be enabled only in version 2.0 using the register bit DemodeReg, see Table 72. Within this option, the total delay time (t_{d2}) is calculated using Equation 5:

$$t_{d2} = \frac{(TPrescaler \times 2 + 2) \times (TReloadVal + 1)}{13.56\ MHz} \quad (7)$$

8.6 Power reduction modes

8.6.1 Hard power-down

Hard power-down is enabled when pin NRSTPD is LOW. This turns off all internal current sinks including the oscillator. All digital input buffers are separated from the input pins and clamped internally (except pin NRSTPD). The output pins are frozen at either a HIGH or LOW level.

8.6.2 Soft power-down mode

Soft Power-down mode is entered immediately after the CommandReg register's PowerDown bit is set to logic 1. All internal current sinks are switched off, including the oscillator buffer. However, the digital input buffers are not separated from the input pins and keep their functionality. The digital output pins do not change their state.

During soft power-down, all register values, the FIFO buffer content and the configuration keep their current contents.

After setting the PowerDown bit to logic 0, it takes 1024 clocks until the Soft power-down mode is exited indicated by the PowerDown bit. Setting it to logic 0 does not immediately clear it. It is cleared automatically by the MFRC522 when Soft power-down mode is exited.

Remark: If the internal oscillator is used, you must take into account that it is supplied by pin AVDD and it will take a certain time (t_{osc}) until the oscillator is stable and the clock cycles can be detected by the internal logic. It is recommended for the serial UART, to first send the value 55h to the MFRC522. The oscillator must be stable for further access to the registers. To ensure this, perform a read access to address 0 until the MFRC522 answers to the last read command with the register content of address 0. This indicates that the MFRC522 is ready.

8.6.3 Transmitter power-down mode

The Transmitter Power-down mode switches off the internal antenna drivers thereby, turning off the RF field. Transmitter power-down mode is entered by setting either the TxControlReg register's Tx1RFEn bit or Tx2RFEn bit to logic 0.

8.7 Oscillator circuit

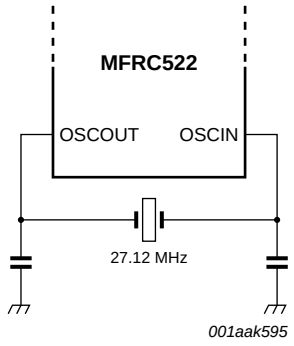


Fig 22. Quartz crystal connection

The clock applied to the MFRC522 provides a time basis for the synchronous system's encoder and decoder. The stability of the clock frequency, therefore, is an important factor for correct operation. To obtain optimum performance, clock jitter must be reduced as much as possible. This is best achieved using the internal oscillator buffer with the recommended circuitry.

If an external clock source is used, the clock signal must be applied to pin OSCIN. In this case, special care must be taken with the clock duty cycle and clock jitter and the clock quality must be verified.

8.8 Reset and oscillator start-up time

8.8.1 Reset timing requirements

The reset signal is filtered by a hysteresis circuit and a spike filter before it enters the digital circuit. The spike filter rejects signals shorter than 10 ns. In order to perform a reset, the signal must be LOW for at least 100 ns.

8.8.2 Oscillator start-up time

If the MFRC522 has been set to a Power-down mode or is powered by a V_{DDX} supply, the start-up time for the MFRC522 depends on the oscillator used and is shown in Figure 23.

The time ($t_{startup}$) is the start-up time of the crystal oscillator circuit. The crystal oscillator start-up time is defined by the crystal.

The time (t_d) is the internal delay time of the MFRC522 when the clock signal is stable before the MFRC522 can be addressed.

The delay time is calculated by:

$$t_d = \frac{1024}{27\ \mu s} = 37.74\ \mu s \tag{8}$$

The time (t_{osc}) is the sum of t_d and $t_{startup}$.

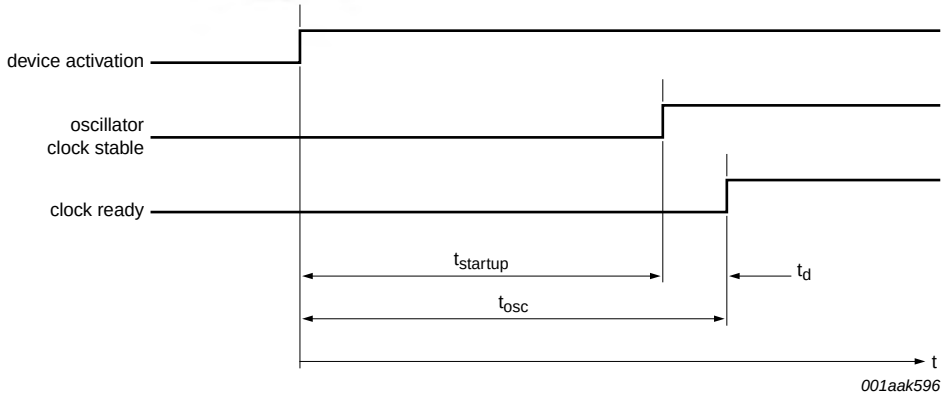


Fig 23. Oscillator start-up time

9. MFRC522 registers

9.1 Register bit behavior

Depending on the functionality of a register, the access conditions to the register can vary. In principle, bits with same behavior are grouped in common registers. The access conditions are described in Table 19.

Table 19. Behavior of register bits and their designation

Abbreviation	Behavior	Description
R/W	read and write	These bits can be written and read by the microcontroller. Since they are used only for control purposes, their content is not influenced by internal state machines, for example the ComIEnReg register can be written and read by the microcontroller. It will also be read by internal state machines but never changed by them.
D	dynamic	These bits can be written and read by the microcontroller. Nevertheless, they can also be written automatically by internal state machines, for example the CommandReg register changes its value automatically after the execution of the command.
R	read only	These register bits hold values which are determined by internal states only, for example the CRCReady bit cannot be written externally but shows internal states.
W	write only	Reading these register bits always returns zero.
reserved	-	These registers are reserved for future use and must not be changed. In case of a write access, it is recommended to always write the value “0”.
RFT	-	These register bits are reserved for future use or are for production tests and must not be changed.

9.2 Register overview

Table 20. MFRC522 register overview

Address (hex)	Register name	Function	Refer to
Page 0: Command and status			
00h	Reserved	reserved for future use	Table 21 on page 38
01h	CommandReg	starts and stops command execution	Table 23 on page 38
02h	ComlEnReg	enable and disable interrupt request control bits	Table 25 on page 38
03h	DivlEnReg	enable and disable interrupt request control bits	Table 27 on page 39
04h	ComIrqReg	interrupt request bits	Table 29 on page 39
05h	DivIrqReg	interrupt request bits	Table 31 on page 40
06h	ErrorReg	error bits showing the error status of the last command executed	Table 33 on page 41
07h	Status1Reg	communication status bits	Table 35 on page 42
08h	Status2Reg	receiver and transmitter status bits	Table 37 on page 43
09h	FIFODataReg	input and output of 64 byte FIFO buffer	Table 39 on page 44
0Ah	FIFOLevelReg	number of bytes stored in the FIFO buffer	Table 41 on page 44
0Bh	WaterLevelReg	level for FIFO underflow and overflow warning	Table 43 on page 44
0Ch	ControlReg	miscellaneous control registers	Table 45 on page 45
0Dh	BitFramingReg	adjustments for bit-oriented frames	Table 47 on page 46
0Eh	CollReg	bit position of the first bit-collision detected on the RF interface	Table 49 on page 46
0Fh	Reserved	reserved for future use	Table 51 on page 47
Page 1: Command			
10h	Reserved	reserved for future use	Table 53 on page 47
11h	ModeReg	defines general modes for transmitting and receiving	Table 55 on page 48
12h	TxModeReg	defines transmission data rate and framing	Table 57 on page 48
13h	RxModeReg	defines reception data rate and framing	Table 59 on page 49
14h	TxControlReg	controls the logical behavior of the antenna driver pins TX1 and TX2	Table 61 on page 50
15h	TxASKReg	controls the setting of the transmission modulation	Table 63 on page 51
16h	TxSelReg	selects the internal sources for the antenna driver	Table 65 on page 51
17h	RxSelReg	selects internal receiver settings	Table 67 on page 52
18h	RxThresholdReg	selects thresholds for the bit decoder	Table 69 on page 53
19h	DemodReg	defines demodulator settings	Table 71 on page 53
1Ah	Reserved	reserved for future use	Table 73 on page 54
1Bh	Reserved	reserved for future use	Table 75 on page 54
1Ch	MfTxReg	controls some MIFARE communication transmit parameters	Table 77 on page 55
1Dh	MfRxReg	controls some MIFARE communication receive parameters	Table 79 on page 55
1Eh	Reserved	reserved for future use	Table 81 on page 55
1Fh	SerialSpeedReg	selects the speed of the serial UART interface	Table 83 on page 55
Page 2: Configuration			
20h	Reserved	reserved for future use	Table 85 on page 57

Table 20. MFRC522 register overview *...continued*

Address (hex)	Register name	Function	Refer to
21h	CRCResultReg	shows the MSB and LSB values of the CRC calculation	Table 87 on page 57
22h			Table 89 on page 57
23h	Reserved	reserved for future use	Table 91 on page 58
24h	ModWidthReg	controls the ModWidth setting	Table 93 on page 58
25h	Reserved	reserved for future use	Table 95 on page 58
26h	RFCfgReg	configures the receiver gain	Table 97 on page 59
27h	GsNReg	selects the conductance of the antenna driver pins TX1 and TX2 for modulation	Table 99 on page 59
28h	CWGsPReg	defines the conductance of the p-driver output during periods of no modulation	Table 101 on page 60
29h	ModGsPReg	defines the conductance of the p-driver output during periods of modulation	Table 103 on page 60
2Ah	TModeReg	defines settings for the internal timer	Table 105 on page 60
2Bh	TPrescalerReg		Table 107 on page 61
2Ch	TReloadReg	defines the 16-bit timer reload value	Table 109 on page 62
2Dh			Table 111 on page 62
2Eh	TCounterValReg	shows the 16-bit timer value	Table 113 on page 63
2Fh			Table 115 on page 63
Page 3: Test register			
30h	Reserved	reserved for future use	Table 117 on page 63
31h	TestSel1Reg	general test signal configuration	Table 119 on page 63
32h	TestSel2Reg	general test signal configuration and PRBS control	Table 121 on page 64
33h	TestPinEnReg	enables pin output driver on pins D1 to D7	Table 123 on page 64
34h	TestPinValueReg	defines the values for D1 to D7 when it is used as an I/O bus	Table 125 on page 65
35h	TestBusReg	shows the status of the internal test bus	Table 127 on page 65
36h	AutoTestReg	controls the digital self test	Table 129 on page 66
37h	VersionReg	shows the software version	Table 131 on page 66
38h	AnalogTestReg	controls the pins AUX1 and AUX2	Table 133 on page 67
39h	TestDAC1Reg	defines the test value for TestDAC1	Table 135 on page 68
3Ah	TestDAC2Reg	defines the test value for TestDAC2	Table 137 on page 68
3Bh	TestADCReg	shows the value of ADC I and Q channels	Table 139 on page 68
3Ch to 3Fh	Reserved	reserved for production tests	Table 141 to Table 147 on page 69

9.3 Register descriptions

9.3.1 Page 0: Command and status

9.3.1.1 Reserved register 00h

Functionality is reserved for future use.

Table 21. Reserved register (address 00h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 22. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	-	reserved

9.3.1.2 CommandReg register

Starts and stops command execution.

Table 23. CommandReg register (address 01h); reset value: 20h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol:	reserved		RcvOff	PowerDown	Command[3:0]			
Access:	-		R/W	D	D			

Table 24. CommandReg register bit descriptions

Bit	Symbol	Value	Description
7 to 6	reserved	-	reserved for future use
5	RcvOff	1	analog part of the receiver is switched off
4	PowerDown	1	Soft power-down mode entered
		0	MFRC522 starts the wake up procedure during which this bit is read as a logic 1; it is read as a logic 0 when the MFRC522 is ready; see Section 8.6.2 on page 33 **Remark:** The PowerDown bit cannot be set when the SoftReset command is activated
3 to 0	Command[3:0]	-	activates a command based on the Command value; reading this register shows which command is executed; see Section 10.3 on page 70

9.3.1.3 ComIEnReg register

Control bits to enable and disable the passing of interrupt requests.

Table 25. ComIEnReg register (address 02h); reset value: 80h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IRqInv	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn	ErrIEn	TimerIEn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 26. ComIEnReg register bit descriptions

Bit	Symbol	Value	Description
7	IRqInv	1	signal on pin IRQ is inverted with respect to the Status1Reg register's IRq bit
		0	signal on pin IRQ is equal to the IRq bit; in combination with the DivIEnReg register's IRqPushPull bit, the default value of logic 1 ensures that the output level on pin IRQ is 3-state
6	TxIEn	-	allows the transmitter interrupt request (TxIRq bit) to be propagated to pin IRQ
5	RxIEn	-	allows the receiver interrupt request (RxIRq bit) to be propagated to pin IRQ
4	IdleIEn	-	allows the idle interrupt request (IdleIRq bit) to be propagated to pin IRQ
3	HiAlertIEn	-	allows the high alert interrupt request (HiAlertIRq bit) to be propagated to pin IRQ
2	LoAlertIEn	-	allows the low alert interrupt request (LoAlertIRq bit) to be propagated to pin IRQ
1	ErrIEn	-	allows the error interrupt request (ErrIRq bit) to be propagated to pin IRQ
0	TimerIEn	-	allows the timer interrupt request (TimerIRq bit) to be propagated to pin IRQ

9.3.1.4 DivIEnReg register

Control bits to enable and disable the passing of interrupt requests.

Table 27. DivIEnReg register (address 03h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IRQPushPull	reserved		MfinActIEn	reserved	CRCIEn	reserved	
Access	R/W	-		R/W	-	R/W	-	

Table 28. DivIEnReg register bit descriptions

Bit	Symbol	Value	Description
7	IRQPushPull	1	pin IRQ is a standard CMOS output pin
		0	pin IRQ is an open-drain output pin
6 to 5	reserved	-	reserved for future use
4	MfinActIEn	-	allows the MFIN active interrupt request to be propagated to pin IRQ
3	reserved	-	reserved for future use
2	CRCIEn	-	allows the CRC interrupt request, indicated by the DivIrqReg register's CRCIRq bit, to be propagated to pin IRQ
1 to 0	reserved	-	reserved for future use

9.3.1.5 ComIrqReg register

Interrupt request bits.

Table 29. ComIrqReg register (address 04h); reset value: 14h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Set1	TxIRq	RxIRq	IdleIRq	HiAlertIRq	LoAlertIRq	ErrIRq	TimerIRq
Access	W	D	D	D	D	D	D	D

Table 30. ComIrqReg register bit descriptions

All bits in the ComIrqReg register are cleared by software.

Bit	Symbol	Value	Description
7	Set1	1	indicates that the marked bits in the ComIrqReg register are set
		0	indicates that the marked bits in the ComIrqReg register are cleared
6	TxIRq	1	set immediately after the last bit of the transmitted data was sent out
5	RxIRq	1	receiver has detected the end of a valid data stream if the RxModeReg register's RxNoErr bit is set to logic 1, the RxIRq bit is only set to logic 1 when data bytes are available in the FIFO
4	IdleIRq	1	If a command terminates, for example, when the CommandReg changes its value from any command to the Idle command (see Table 149 on page 70) if an unknown command is started, the CommandReg register Command[3:0] value changes to the idle state and the IdleIRq bit is set The microcontroller starting the Idle command does not set the IdleIRq bit
3	HiAlertIRq	1	the Status1Reg register's HiAlert bit is set in opposition to the HiAlert bit, the HiAlertIRq bit stores this event and can only be reset as indicated by the Set1 bit in this register
2	LoAlertIRq	1	Status1Reg register's LoAlert bit is set in opposition to the LoAlert bit, the LoAlertIRq bit stores this event and can only be reset as indicated by the Set1 bit in this register
1	ErrIRq	1	any error bit in the ErrorReg register is set
0	TimerIRq	1	the timer decrements the timer value in register TCounterValReg to zero

9.3.1.6 DivIrqReg register

Interrupt request bits.

Table 31. DivIrqReg register (address 05h); reset value: x0h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Set2	reserved		MfinActIRq	reserved	CRCIRq	reserved	
Access	W	-		D	-	D	-	

Table 32. DivIrqReg register bit descriptions

All bits in the DivIrqReg register are cleared by software.

Bit	Symbol	Value	Description
7	Set2	1	indicates that the marked bits in the DivIrqReg register are set
		0	indicates that the marked bits in the DivIrqReg register are cleared
6 to 5	reserved	-	reserved for future use
4	MfinActIRq	1	MFIN is active this interrupt is set when either a rising or falling signal edge is detected
3	reserved	-	reserved for future use
2	CRCIRq	1	the CalcCRC command is active and all data is processed
1 to 0	reserved	-	reserved for future use

9.3.1.7 ErrorReg register

Error bit register showing the error status of the last command executed.

Table 33. ErrorReg register (address 06h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WrErr	TempErr	reserved	BufferOvfl	CollErr	CRCErr	ParityErr	ProtocolErr
Access	R	R	-	R	R	R	R	R

Table 34. ErrorReg register bit descriptions

Bit	Symbol	Value	Description
7	WrErr	1	data is written into the FIFO buffer by the host during the MFAuthent command or if data is written into the FIFO buffer by the host during the time between sending the last bit on the RF interface and receiving the last bit on the RF interface
6	TempErr[1]	1	internal temperature sensor detects overheating, in which case the antenna drivers are automatically switched off
5	reserved	-	reserved for future use
4	BufferOvfl	1	the host or a MFRC522's internal state machine (e.g. receiver) tries to write data to the FIFO buffer even though it is already full
3	CollErr	1	a bit-collision is detected cleared automatically at receiver start-up phase only valid during the bitwise anticollision at 106 kBd always set to logic 0 during communication protocols at 212 kBd, 424 kBd and 848 kBd
2	CRCErr	1	the RxModeReg register's RxCRCEn bit is set and the CRC calculation fails automatically cleared to logic 0 during receiver start-up phase
1	ParityErr	1	parity check failed automatically cleared during receiver start-up phase only valid for ISO/IEC 14443 A/MIFARE communication at 106 kBd
0	ProtocolErr	1	set to logic 1 if the SOF is incorrect automatically cleared during receiver start-up phase bit is only valid for 106 kBd during the MFAuthent command, the ProtocolErr bit is set to logic 1 if the number of bytes received in one data stream is incorrect

[1] Command execution clears all error bits except the TempErr bit. Cannot be set by software.

9.3.1.8 Status1Reg register

Contains status bits of the CRC, interrupt and FIFO buffer.

Table 35. Status1Reg register (address 07h); reset value: 21h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	CRCOk	CRCReady	IRq	TRunning	reserved	HiAlert	LoAlert
Access	-	R	R	R	R	-	R	R

Table 36. Status1Reg register bit descriptions

Bit	Symbol	Value	Description
7	reserved	-	reserved for future use
6	CRCOk	1	the CRC result is zero for data transmission and reception, the CRCOk bit is undefined: use the ErrorReg register's CRCErr bit indicates the status of the CRC coprocessor, during calculation the value changes to logic 0, when the calculation is done correctly the value changes to logic 1
5	CRCReady	1	the CRC calculation has finished only valid for the CRC coprocessor calculation using the CalcCRC command
4	IRq	-	indicates if any interrupt source requests attention with respect to the setting of the interrupt enable bits: see the ComIEnReg and DivIEnReg registers
3	TRunning	1	MFRC522's timer unit is running, i.e. the timer will decrement the TCounterValReg register with the next timer clock **Remark:** in gated mode, the TRunning bit is set to logic 1 when the timer is enabled by TModeReg register's TGated[1:0] bits; this bit is not influenced by the gated signal
2	reserved	-	reserved for future use
1	HiAlert	1	the number of bytes stored in the FIFO buffer corresponds to equation: $HiAlert = (64 - FIFOLength) \leq WaterLevel$ example: FIFO length = 60, WaterLevel = 4 $\rightarrow$ HiAlert = 1 FIFO length = 59, WaterLevel = 4 $\rightarrow$ HiAlert = 0
0	LoAlert	1	the number of bytes stored in the FIFO buffer corresponds to equation: $LoAlert = FIFOLength \leq WaterLevel$ example: FIFO length = 4, WaterLevel = 4 $\rightarrow$ LoAlert = 1 FIFO length = 5, WaterLevel = 4 $\rightarrow$ LoAlert = 0

9.3.1.9 Status2Reg register

Contains status bits of the receiver, transmitter and data mode detector.

Table 37. Status2Reg register (address 08h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TempSensClear	I²CForceHS	reserved		MFCrypto1On	ModemState[2:0]		
Access	R/W	R/W	-		D	R		

Table 38. Status2Reg register bit descriptions

Bit	Symbol	Value	Description
7	TempSensClear	1	clears the temperature error if the temperature is below the alarm limit of 125 °C
6	I²CForceHS		I²C-bus input filter settings:
		1	the I²C-bus input filter is set to the High-speed mode independent of the I²C-bus protocol
		0	the I²C-bus input filter is set to the I²C-bus protocol used
5 to 4	reserved	-	reserved
3	MFCrypto1On	-	indicates that the MIFARE Crypto1 unit is switched on and therefore all data communication with the card is encrypted can only be set to logic 1 by a successful execution of the MFAuthent command only valid in Read/Write mode for MIFARE standard cards this bit is cleared by software
2 to 0	ModemState[2:0]	-	shows the state of the transmitter and receiver state machines:
		000	idle
		001	wait for the BitFramingReg register's StartSend bit
		010	TxWait: wait until RF field is present if the TModeReg register's TxWaitRF bit is set to logic 1 the minimum time for TxWait is defined by the TxWaitReg register
		011	transmitting
		100	RxWait: wait until RF field is present if the TModeReg register's TxWaitRF bit is set to logic 1 the minimum time for RxWait is defined by the RxWaitReg register
		101	wait for data
		110	receiving

9.3.1.10 FIFODataReg register

Input and output of 64 byte FIFO buffer.

Table 39. FIFODataReg register (address 09h); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FIFOData[7:0]							
Access	D							

Table 40. FIFODataReg register bit descriptions

Bit	Symbol	Description
7 to 0	FIFOData[7:0]	data input and output port for the internal 64-byte FIFO buffer FIFO buffer acts as parallel in/parallel out converter for all serial data stream inputs and outputs

9.3.1.11 FIFOLevelReg register

Indicates the number of bytes stored in the FIFO.

Table 41. FIFOLevelReg register (address 0Ah); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FlushBuffer	FIFOLevel[6:0]						
Access	W	R						

Table 42. FIFOLevelReg register bit descriptions

Bit	Symbol	Value	Description
7	FlushBuffer	1	immediately clears the internal FIFO buffer's read and write pointer and ErrorReg register's BufferOvfl bit reading this bit always returns 0
6 to 0	FIFOLevel [6:0]	-	indicates the number of bytes stored in the FIFO buffer writing to the FIFODataReg register increments and reading decrements the FIFOLevel value

9.3.1.12 WaterLevelReg register

Defines the level for FIFO under- and overflow warning.

Table 43. WaterLevelReg register (address 0Bh); reset value: 08h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		WaterLevel[5:0]					
Access	-		R/W					

Table 44. WaterLevelReg register bit descriptions

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	WaterLevel [5:0]	defines a warning level to indicate a FIFO buffer overflow or underflow: Status1Reg register's HiAlert bit is set to logic 1 if the remaining number of bytes in the FIFO buffer space is equal to, or less than the defined number of WaterLevel bytes Status1Reg register's LoAlert bit is set to logic 1 if equal to, or less than the WaterLevel bytes in the FIFO buffer **Remark:** to calculate values for HiAlert and LoAlert see Section 9.3.1.8 on page 42.

9.3.1.13 ControlReg register

Miscellaneous control bits.

Table 45. ControlReg register (address 0Ch); reset value: 10h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TStopNow	TStartNow	reserved			RxLastBits[2:0]		
Access	W	W	-			R		

Table 46. ControlReg register bit descriptions

Bit	Symbol	Value	Description
7	TStopNow	1	timer stops immediately reading this bit always returns it to logic0
6	TStartNow	1	timer starts immediately reading this bit always returns it to logic 0
5 to 3	reserved	-	reserved for future use
2 to 0	RxLastBits[2:0]	-	indicates the number of valid bits in the last received byte if this value is 000b, the whole byte is valid

9.3.1.14 BitFramingReg register

Adjustments for bit-oriented frames.

Table 47. BitFramingReg register (address 0Dh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	StartSend	RxAlign[2:0]			reserved	TxLastBits[2:0]		
Access	W	R/W			-	R/W		

Table 48. BitFramingReg register bit descriptions

Bit	Symbol	Value	Description
7	StartSend	1	starts the transmission of data only valid in combination with the Transceive command
6 to 4	RxAlign[2:0]		used for reception of bit-oriented frames: defines the bit position for the first bit received to be stored in the FIFO buffer example:
		0	LSB of the received bit is stored at bit position 0, the second received bit is stored at bit position 1
		1	LSB of the received bit is stored at bit position 1, the second received bit is stored at bit position 2
		7	LSB of the received bit is stored at bit position 7, the second received bit is stored in the next byte that follows at bit position 0 These bits are only to be used for bitwise anticollision at 106 kBd, for all other modes they are set to 0
3	reserved	-	reserved for future use
2 to 0	TxLastBits[2:0]	-	used for transmission of bit oriented frames: defines the number of bits of the last byte that will be transmitted 000b indicates that all bits of the last byte will be transmitted

9.3.1.15 CollReg register

Defines the first bit-collision detected on the RF interface.

Table 49. CollReg register (address 0Eh); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ValuesAfterColl	reserved	CollPosNotValid	CollPos[4:0]				
Access	R/W	-	R	R				

Table 50. CollReg register bit descriptions

Bit	Symbol	Value	Description
7	ValuesAfterColl	0	all received bits will be cleared after a collision only used during bitwise anticollision at 106 kBd, otherwise it is set to logic 1
6	reserved	-	reserved for future use
5	CollPosNotValid	1	no collision detected or the position of the collision is out of the range of CollPos[4:0]

Table 50. CollReg register bit descriptions *...continued*

Bit	Symbol	Value	Description
4 to 0	CollPos[4:0]	-	shows the bit position of the first detected collision in a received frame only data bits are interpreted example:
		00h	indicates a bit-collision in the 32nd bit
		01h	indicates a bit-collision in the 1st bit
		08h	indicates a bit-collision in the 8th bit These bits will only be interpreted if the CollPosNotValid bit is set to logic 0

9.3.1.16 Reserved register 0Fh

Functionality is reserved for future use.

Table 51. Reserved register (address 0Fh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 52. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.2 Page 1: Communication

9.3.2.1 Reserved register 10h

Functionality is reserved for future use.

Table 53. Reserved register (address 10h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 54. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.2.2 ModeReg register

Defines general mode settings for transmitting and receiving.

Table 55. ModeReg register (address 11h); reset value: 3Fh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MSBFirst	reserved	TxWaitRF	reserved	PolMFin	reserved	CRCPreset[1:0]	
Access	R/W	-	R/W	-	R/W	-	R/W	

Table 56. ModeReg register bit descriptions

Bit	Symbol	Value	Description
7	MSBFirst	1	CRC coprocessor calculates the CRC with MSB first in the CRCResultReg register the values for the CRCResultMSB[7:0] bits and the CRCResultLSB[7:0] bits are bit reversed **Remark:** during RF communication this bit is ignored
6	reserved	-	reserved for future use
5	TxWaitRF	1	transmitter can only be started if an RF field is generated
4	reserved	-	reserved for future use
3	PolMFin		defines the polarity of pin MFIN **Remark:** the internal envelope signal is encoded active LOW, changing this bit generates a MFinActIRq event
		1	polarity of pin MFIN is active HIGH
		0	polarity of pin MFIN is active LOW
2	reserved	-	reserved for future use
1 to 0	CRCPreset [1:0]		defines the preset value for the CRC coprocessor for the CalcCRC command **Remark:** during any communication, the preset values are selected automatically according to the definition of bits in the RxModeReg and TxModeReg registers
		00	0000h
		01	6363h
		10	A671h
		11	FFFFh

9.3.2.3 TxModeReg register

Defines the data rate during transmission.

Table 57. TxModeReg register (address 12h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TxCRCEn	TxSpeed[2:0]			InvMod	reserved		
Access	R/W	D			R/W	-		

Table 58. TxModeReg register bit descriptions

Bit	Symbol	Value	Description
7	TxCRCEn	1	enables CRC generation during data transmission **Remark:** can only be set to logic 0 at 106 kBd
6 to 4	TxSpeed[2:0]		defines the bit rate during data transmission the MFRC522 handles transfer speeds up to 848 kBd
		000	106 kBd
		001	212 kBd
		010	424 kBd
		011	848 kBd
		100	reserved
		101	reserved
		110	reserved
		111	reserved
3	InvMod	1	modulation of transmitted data is inverted
2 to 0	reserved	-	reserved for future use

9.3.2.4 RxModeReg register

Defines the data rate during reception.

Table 59. RxModeReg register (address 13h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RxCRCEn	RxSpeed[2:0]			RxNoErr	RxMultiple	reserved	
Access	R/W	D			R/W	R/W	-	

Table 60. RxModeReg register bit descriptions

Bit	Symbol	Value	Description
7	RxCRCEn	1	enables the CRC calculation during reception **Remark:** can only be set to logic 0 at 106 kBd
6 to 4	RxSpeed[2:0]		defines the bit rate while receiving data the MFRC522 handles transfer speeds up to 848 kBd
		000	106 kBd
		001	212 kBd
		010	424 kBd
		011	848 kBd
		100	reserved
		101	reserved
		110	reserved
		111	reserved
3	RxNoErr	1	an invalid received data stream (less than 4 bits received) will be ignored and the receiver remains active

Table 60. RxModeReg register bit descriptions *...continued*

Bit	Symbol	Value	Description
2	RxMultiple	0	receiver is deactivated after receiving a data frame
		1	able to receive more than one data frame only valid for data rates above 106 kBd in order to handle the polling command after setting this bit the Receive and Transceive commands will not terminate automatically. Multiple reception can only be deactivated by writing any command (except the Receive command) to the CommandReg register, or by the host clearing the bit if set to logic 1, an error byte is added to the FIFO buffer at the end of a received data stream which is a copy of the ErrorReg register value. For the MFRC522 version 2.0 the CRC status is reflected in the signal CRCOk, which indicates the actual status of the CRC coprocessor. For the MFRC522 version 1.0 the CRC status is reflected in the signal CRCErr.
1 to 0	reserved	-	reserved for future use

9.3.2.5 TxControlReg register

Controls the logical behavior of the antenna driver pins TX1 and TX2.

Table 61. TxControlReg register (address 14h); reset value: 80h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	InvTx2RF On	InvTx1RF On	InvTx2RF Off	InvTx1RF Off	Tx2CW	reserved	Tx2RFEn	Tx1RFEn
Access	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W

Table 62. TxControlReg register bit descriptions

Bit	Symbol	Value	Description
7	InvTx2RFOn	1	output signal on pin TX2 inverted when driver TX2 is enabled
6	InvTx1RFOn	1	output signal on pin TX1 inverted when driver TX1 is enabled
5	InvTx2RFOff	1	output signal on pin TX2 inverted when driver TX2 is disabled
4	InvTx1RFOff	1	output signal on pin TX1 inverted when driver TX1 is disabled
3	Tx2CW	1	output signal on pin TX2 continuously delivers the unmodulated 13.56 MHz energy carrier
		0	Tx2CW bit is enabled to modulate the 13.56 MHz energy carrier
2	reserved	-	reserved for future use
1	Tx2RFEn	1	output signal on pin TX2 delivers the 13.56 MHz energy carrier modulated by the transmission data
0	Tx1RFEn	1	output signal on pin TX1 delivers the 13.56 MHz energy carrier modulated by the transmission data

9.3.2.6 TxASKReg register

Controls transmit modulation settings.

Table 63. TxASKReg register (address 15h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	Force100ASK	reserved					
Access	-	R/W	-					

Table 64. TxASKReg register bit descriptions

Bit	Symbol	Value	Description
7	reserved	-	reserved for future use
6	Force100ASK	1	forces a 100 % ASK modulation independent of the ModGsPReg register setting
5 to 0	reserved	-	reserved for future use

9.3.2.7 TxSelReg register

Selects the internal sources for the analog module.

Table 65. TxSelReg register (address 16h); reset value: 10h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol:	reserved		DriverSel[1:0]		MFOutSel[3:0]			
Access:	-		R/W		R/W			

Table 66. TxSelReg register bit descriptions

Bit	Symbol	Value	Description
7 to 6	reserved	-	reserved for future use
5 to 4	DriverSel [1:0]	-	selects the input of drivers TX1 and TX2
		00	3-state; in soft power-down the drivers are only in 3-state mode if the DriverSel[1:0] value is set to 3-state mode
		01	modulation signal (envelope) from the internal encoder, Miller pulse encoded
		10	modulation signal (envelope) from pin MFIN
		11	HIGH; the HIGH level depends on the setting of bits InvTx1RFOn/InvTx1RFOff and InvTx2RFOn/InvTx2RFOff

Table 66. TxSelReg register bit descriptions *...continued*

Bit	Symbol	Value	Description
3 to 0	MFOutSel [3:0]		selects the input for pin MFOUT
		0000	3-state
		0001	LOW
		0010	HIGH
		0011	test bus signal as defined by the TestSel1Reg register's TstBusBitSel[2:0] value
		0100	modulation signal (envelope) from the internal encoder, Miller pulse encoded
		0101	serial data stream to be transmitted, data stream before Miller encoder
		0110	reserved
		0111	serial data stream received, data stream after Manchester decoder
		1000 to 1111	reserved

9.3.2.8 RxSelReg register

Selects internal receiver settings.

Table 67. RxSelReg register (address 17h); reset value: 84h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	UARTSel[1:0]		RxWait[5:0]					
Access	R/W		R/W					

Table 68. RxSelReg register bit descriptions

Bit	Symbol	Value	Description
7 to 6	UARTSel [1:0]		selects the input of the contactless UART
		00	constant LOW
		01	Manchester with subcarrier from pin MFIN
		10	modulated signal from the internal analog module, default
		11	NRZ coding without subcarrier from pin MFIN which is only valid for transfer speeds above 106 kBd
5 to 0	RxWait [5:0]	-	after data transmission the activation of the receiver is delayed for RxWait bit-clocks, during this 'frame guard time' any signal on pin RX is ignored this parameter is ignored by the Receive command all other commands, such as Transceive, MFAuthent use this parameter the counter starts immediately after the external RF field is switched on

9.3.2.9 RxThresholdReg register

Selects thresholds for the bit decoder.

Table 69. RxThresholdReg register (address 18h); reset value: 84h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MinLevel[3:0]				reserved	CollLevel[2:0]		
Access	R/W				-	R/W		

Table 70. RxThresholdReg register bit descriptions

Bit	Symbol	Description
7 to 4	MinLevel [3:0]	defines the minimum signal strength at the decoder input that will be accepted if the signal strength is below this level it is not evaluated
3	reserved	reserved for future use
2 to 0	CollLevel [2:0]	defines the minimum signal strength at the decoder input that must be reached by the weaker half-bit of the Manchester encoded signal to generate a bit-collision relative to the amplitude of the stronger half-bit

9.3.2.10 DemodReg register

Defines demodulator settings.

Table 71. DemodReg register (address 19h); reset value: 4Dh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	AddIQ[1:0]		FixIQ	TPrescal Even	TauRcv[1:0]		TauSync[1:0]	
Access	R/W		R/W	R/W	R/W		R/W	

Table 72. DemodReg register bit descriptions

Bit	Symbol	Value	Description
7 to 6	AddIQ [1:0]	-	defines the use of I and Q channel during reception **Remark:** the FixIQ bit must be set to logic 0 to enable the following settings:
		00	selects the stronger channel
		01	selects the stronger channel and freezes the selected channel during communication
		10	reserved
		11	reserved
5	FixIQ	1	if AddIQ[1:0] are set to X0b, the reception is fixed to I channel if AddIQ[1:0] are set to X1b, the reception is fixed to Q channel

Table 72. DemodReg register bit descriptions *…continued*

Bit	Symbol	Value	Description
4	TPrescalEven	R/W	Available on RC522 version 1.0 and version 2.0: If set to logic 0 the following formula is used to calculate the timer frequency of the prescaler: f_{timer} = 13.56 MHz / (2*TPreScaler+1). Only available on version 2.0: If set to logic 1 the following formula is used to calculate the timer frequency of the prescaler: f_{timer} = 13.56 MHz / (2*TPreScaler+2). Default TPrescalEven bit is logic 0, find more information on the prescaler in Section 8.5.
3 to 2	TauRcv[1:0]	-	changes the time-constant of the internal PLL during data reception **Remark:** if set to 00b the PLL is frozen during data reception
1 to 0	TauSync[1:0]	-	changes the time-constant of the internal PLL during burst

9.3.2.11 Reserved register 1Ah

Functionality is reserved for future use.

Table 73. Reserved register (address 1Ah); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 74. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.2.12 Reserved register 1Bh

Functionality is reserved for future use.

Table 75. Reserved register (address 1Bh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 76. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.2.13 MfTxReg register

Controls some MIFARE communication transmit parameters.

Table 77. MfTxReg register (address 1Ch); reset value: 62h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						TxWait[1:0]	
Access	-						R/W	

Table 78. MfTxReg register bit descriptions

Bit	Symbol	Description
7 to 2	reserved	reserved for future use
1 to 0	TxWait	defines the additional response time 7 bits are added to the value of the register bit by default

9.3.2.14 MfRxReg register

Table 79. MfRxReg register (address 1Dh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ParityDisable	reserved			
Access	-			R/W	-			

Table 80. MfRxReg register bit descriptions

Bit	Symbol	Value	Description
7 to 5	reserved	-	reserved for future use
4	ParityDisable	1	generation of the parity bit for transmission and the parity check for receiving is switched off the received parity bit is handled like a data bit
3 to 0	reserved	-	reserved for future use

9.3.2.15 Reserved register 1Eh

Functionality is reserved for future use.

Table 81. Reserved register (address 1Eh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 82. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.2.16 SerialSpeedReg register

Selects the speed of the serial UART interface.

Table 83. SerialSpeedReg register (address 1Fh); reset value: EBh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	BR_T0[2:0]			BR_T1[4:0]				
Access	R/W			R/W				

Table 84. SerialSpeedReg register bit descriptions

Bit	Symbol	Description
7 to 5	BR_T0[2:0]	factor BR_T0 adjusts the transfer speed: for description, see Section 8.1.3.2 on page 12
4 to 0	BR_T1[4:0]	factor BR_T1 adjusts the transfer speed: for description, see Section 8.1.3.2 on page 12

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9.3.3.1 Reserved register 20h

Functionality is reserved for future use.

Table 85. Reserved register (address 20h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-							
Access	reserved							

Table 86. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.3.2 CRCResultReg registers

Shows the MSB and LSB values of the CRC calculation.

Remark: The CRC is split into two 8-bit registers.

Table 87. CRCResultReg (higher bits) register (address 21h); reset value: FFh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CRCResultMSB[7:0]							
Access	R							

Table 88. CRCResultReg register higher bit descriptions

Bit	Symbol	Description
7 to 0	CRCResultMSB [7:0]	shows the value of the CRCResultReg register's most significant byte only valid if Status1Reg register's CRCReady bit is set to logic 1

Table 89. CRCResultReg (lower bits) register (address 22h); reset value: FFh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CRCResultLSB[7:0]							
Access	R							

Table 90. CRCResultReg register lower bit descriptions

Bit	Symbol	Description
7 to 0	CRCResultLSB [7:0]	shows the value of the least significant byte of the CRCResultReg register only valid if Status1Reg register's CRCReady bit is set to logic 1

9.3.3.3 Reserved register 23h

Functionality is reserved for future use.

Table 91. Reserved register (address 23h); reset value: 88h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 92. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.3.4 ModWidthReg register

Sets the modulation width.

Table 93. ModWidthReg register (address 24h); reset value: 26h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ModWidth[7:0]							
Access	R/W							

Table 94. ModWidthReg register bit descriptions

Bit	Symbol	Description
7 to 0	ModWidth[7:0]	defines the width of the Miller modulation as multiples of the carrier frequency (ModWidth + 1 / f_{clk}) the maximum value is half the bit period

9.3.3.5 Reserved register 25h

Functionality is reserved for future use.

Table 95. Reserved register (address 25h); reset value: 87h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 96. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.3.6 RFCfgReg register

Configures the receiver gain.

Table 97. RFCfgReg register (address 26h); reset value: 48h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	RxGain[2:0]			reserved			
Access	-	R/W			-			

Table 98. RFCfgReg register bit descriptions

Bit	Symbol	Value	Description
7	reserved	-	reserved for future use
6 to 4	RxGain [2:0]		defines the receiver's signal voltage gain factor:
		000	18 dB
		001	23 dB
		010	18 dB
		011	23 dB
		100	33 dB
		101	38 dB
		110	43 dB
		111	48 dB
3 to 0	reserved	-	reserved for future use

9.3.3.7 GsNReg register

Defines the conductance of the antenna driver pins TX1 and TX2 for the n-driver when the driver is switched on.

Table 99. GsNReg register (address 27h); reset value: 88h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CWGsN[3:0]				ModGsN[3:0]			
Access	R/W				R/W			

Table 100. GsNReg register bit descriptions

Bit	Symbol	Description
7 to 4	CWGsN [3:0]	defines the conductance of the output n-driver during periods without modulation which can be used to regulate the output power and subsequently current consumption and operating distance **Remark:** the conductance value is binary-weighted during soft Power-down mode the highest bit is forced to logic 1 value is only used if driver TX1 or TX2 is switched on
3 to 0	ModGsN [3:0]	defines the conductance of the output n-driver during periods without modulation which can be used to regulate the modulation index **Remark:** the conductance value is binary weighted during soft Power-down mode the highest bit is forced to logic 1 value is only used if driver TX1 or TX2 is switched on

9.3.3.8 CWGsPReg register

Defines the conductance of the p-driver output during periods of no modulation.

Table 101. CWGsPReg register (address 28h); reset value: 20h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		CWGsP[5:0]					
Access	-		R/W					

Table 102. CWGsPReg register bit descriptions

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	CWGsP[5:0]	defines the conductance of the p-driver output which can be used to regulate the output power and subsequently current consumption and operating distance **Remark:** the conductance value is binary weighted during soft Power-down mode the highest bit is forced to logic 1

9.3.3.9 ModGsPReg register

Defines the conductance of the p-driver output during modulation.

Table 103. ModGsPReg register (address 29h); reset value: 20h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		ModGsP[5:0]					
Access	-		R/W					

Table 104. ModGsPReg register bit descriptions

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	ModGsP[5:0]	defines the conductance of the p-driver output during modulation which can be used to regulate the modulation index **Remark:** the conductance value is binary weighted during soft Power-down mode the highest bit is forced to logic 1 if the TxASKReg register's Force100ASK bit is set to logic 1 the value of ModGsP has no effect

9.3.3.10 TModeReg and TPrescalerReg registers

These registers define the timer settings.

Remark: The TPrescaler setting higher 4 bits are in the TModeReg register and the lower 8 bits are in the TPrescalerReg register.

Table 105. TModeReg register (address 2Ah); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TAuto	TGated[1:0]		TAutoRestart	TPrescaler_Hi[3:0]			
Access	R/W	R/W		R/W	R/W			

Table 106. TModeReg register bit descriptions

Bit	Symbol	Value	Description
7	TAuto	1	timer starts automatically at the end of the transmission in all communication modes at all speeds if the RxModeReg register's RxMultiple bit is not set, the timer stops immediately after receiving the 5th bit (1 start bit, 4 data bits) if the RxMultiple bit is set to logic 1 the timer never stops, in which case the timer can be stopped by setting the ControlReg register's TStopNow bit to logic 1
		0	indicates that the timer is not influenced by the protocol
6 to 5	TGated[1:0]		internal timer is running in gated mode **Remark:** in gated mode, the Status1Reg register's TRunning bit is logic 1 when the timer is enabled by the TModeReg register's TGated[1:0] bits this bit does not influence the gating signal
		00	non-gated mode
		01	gated by pin MFIN
		10	gated by pin AUX1
		11	-
4	TAutoRestart	1	timer automatically restarts its count-down from the 16-bit timer reload value instead of counting down to zero
		0	timer decrements to 0 and the ComIrqReg register's TimerIRq bit is set to logic 1
3 to 0	TPrescaler_Hi[3:0]	-	defines the higher 4 bits of the TPrescaler value The following formula is used to calculate the timer frequency if the DemodReg register's TPrescalEven bit in Demot Regis set to logic 0: f_{timer} = 13.56 MHz / (2*TPreScaler+1). Where TPreScaler = [TPrescaler_Hi:TPrescaler_Lo] (TPrescaler value on 12 bits) (Default TPrescalEven bit is logic 0) The following formula is used to calculate the timer frequency if the DemodReg register's TPrescalEven bit is set to logic 1: f_{timer} = 13.56 MHz / (2*TPreScaler+2). See Section 8.5 "Timer unit".

Table 107. TPrescalerReg register (address 2Bh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TPrescaler_Lo[7:0]							
Access	R/W							

Table 108. TPrescalerReg register bit descriptions

Bit	Symbol	Description
7 to 0	TPrescaler_Lo[7:0]	defines the lower 8 bits of the TPrescaler value The following formula is used to calculate the timer frequency if the DemodReg register's TPrescalEven bit is set to logic 0: f_{timer} = 13.56 MHz / (2*TPreScaler+1). Where TPreScaler = [TPrescaler_Hi:TPrescaler_Lo] (TPrescaler value on 12 bits) (Default TPrescalEven bit is logic 0) The following formula is used to calculate the timer frequency if the DemodReg register's TPrescalEven bit inDemoReg is set to logic 1: f_{timer} = 13.56 MHz / (2*TPreScaler+2). See Section 8.5 "Timer unit".

9.3.3.11 TReloadReg register

Defines the 16-bit timer reload value.

Remark: The reload value bits are contained in two 8-bit registers.

Table 109. TReloadReg (higher bits) register (address 2Ch); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TReloadVal_Hi[7:0]							
Access	R/W							

Table 110. TReloadReg register higher bit descriptions

Bit	Symbol	Description
7 to 0	TReloadVal_Hi[7:0]	defines the higher 8 bits of the 16-bit timer reload value on a start event, the timer loads the timer reload value changing this register affects the timer only at the next start event

Table 111. TReloadReg (lower bits) register (address 2Dh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TReloadVal_Lo[7:0]							
Access	R/W							

Table 112. TReloadReg register lower bit descriptions

Bit	Symbol	Description
7 to 0	TReloadVal_Lo[7:0]	defines the lower 8 bits of the 16-bit timer reload value on a start event, the timer loads the timer reload value changing this register affects the timer only at the next start event

9.3.3.12 TCounterValReg register

Contains the timer value.

Remark: The timer value bits are contained in two 8-bit registers.

Table 113. TCounterValReg (higher bits) register (address 2Eh); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TCounterVal_Hi[7:0]							
Access	R							

Table 114. TCounterValReg register higher bit descriptions

Bit	Symbol	Description
7 to 0	TCounterVal_Hi[7:0]	timer value higher 8 bits

Table 115. TCounterValReg (lower bits) register (address 2Fh); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TCounterVal_Lo[7:0]							
Access	R							

Table 116. TCounterValReg register lower bit descriptions

Bit	Symbol	Description
7 to 0	TCounterVal_Lo[7:0]	timer value lower 8 bits

9.3.4 Page 3: Test

9.3.4.1 Reserved register 30h

Functionality is reserved for future use.

Table 117. Reserved register (address 30h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 118. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.4.2 TestSel1Reg register

General test signal configuration.

Table 119. TestSel1Reg register (address 31h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved					TstBusBitSel[2:0]		
Access	-					R/W		

Table 120. TestSel1Reg register bit descriptions

Bit	Symbol	Description
7 to 3	reserved	reserved for future use
2 to 0	TstBusBitSel [2:0]	selects a test bus signal which is output at pin MFOUT if AnalogSelAux2[3:0] = FFh in AnalogTestReg register, test bus signal is also output at pins AUX1 or AUX2

9.3.4.3 TestSel2Reg register

General test signal configuration and PRBS control.

Table 121. TestSel2Reg register (address 32h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TstBusFlip	PRBS9	PRBS15	TestBusSel[4:0]				
Access	R/W	R/W	R/W	R/W				

Table 122. TestSel2Reg register bit descriptions

Bit	Symbol	Value	Description
7	TstBusFlip	1	test bus is mapped to the parallel port in the following order: TstBusBit4,TstBusBit3, TstBusBit2, TstBusBit6, TstBusBit5, TstBusBit0; see Section 16.1 on page 82
6	PRBS9	-	starts and enables the PRBS9 sequence according to ITU-TO150 **Remark:** all relevant registers to transmit data must be configured before entering PRBS9 mode the data transmission of the defined sequence is started by the Transmit command
5	PRBS15	-	starts and enables the PRBS15 sequence according to ITU-TO150 **Remark:** all relevant registers to transmit data must be configured before entering PRBS15 mode the data transmission of the defined sequence is started by the Transmit command
4 to 0	TestBusSel[4:0]	-	selects the test bus; see Section 16.1 “Test signals”

9.3.4.4 TestPinEnReg register

Enables the test bus pin output driver.

Table 123. TestPinEnReg register (address 33h); reset value: 80h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RS232LineEn	TestPinEn[5:0]						reserved
Access	R/W	R/W						-

Table 124. TestPinEnReg register bit descriptions

Bit	Symbol	Value	Description
7	RS232LineEn	0	serial UART lines MX and DTRQ are disabled
6 to 1	TestPinEn [5:0]	-	enables the output driver on one of the data pins D1 to D7 which outputs a test signal **Example:** setting bit 1 to logic 1 enables pin D1 output setting bit 5 to logic 1 enables pin D5 output **Remark:** If the SPI is used, only pins D1 to D4 can be used. If the serial UART interface is used and the RS232LineEn bit is set to logic 1 only pins D1 to D4 can be used.
0	reserved	-	reserved for future use

9.3.4.5 TestPinValueReg register

Defines the HIGH and LOW values for the test port D1 to D7 when it is used as I/O.

Table 125. TestPinValueReg register (address 34h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	UseIO	TestPinValue[5:0]						reserved
Access	R/W	R/W						-

Table 126. TestPinValueReg register bit descriptions

Bit	Symbol	Value	Description
7	UseIO	1	enables the I/O functionality for the test port when one of the serial interfaces is used the input/output behavior is defined by value TestPinEn[5:0] in the TestPinEnReg register the value for the output behavior is defined by TestPinValue[5:0]
6 to 1	TestPinValue [5:0]	-	defines the value of the test port when it is used as I/O and each output must be enabled by TestPinEn[5:0] in the TestPinEnReg register **Remark:** Reading the register indicates the status of pins D6 to D1 if the UseIO bit is set to logic 1. If the UseIO bit is set to logic 0, the value of the TestPinValueReg register is read back.
0	reserved	-	reserved for future use

9.3.4.6 TestBusReg register

Shows the status of the internal test bus.

Table 127. TestBusReg register (address 35h); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TestBus[7:0]							
Access	R							

Table 128. TestBusReg register bit descriptions

Bit	Symbol	Description
7 to 0	TestBus[7:0]	shows the status of the internal test bus the test bus is selected using the TestSel2Reg register; see Section 16.1 on page 82

9.3.4.7 AutoTestReg register

Controls the digital self-test.

Table 129. AutoTestReg register (address 36h); reset value: 40h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	AmpRcv	RFT		SelfTest[3:0]			
Access	-	R/W	-		R/W			

Table 130. AutoTestReg register bit descriptions

Bit	Symbol	Value	Description
7	reserved	-	reserved for production tests
6	AmpRcv	1	internal signal processing in the receiver chain is performed non-linearly which increases the operating distance in communication modes at 106 kBd **Remark:** due to non-linearity, the effect of the RxThresholdReg register's MinLevel[3:0] and the CollLevel[2:0] values is also non-linear
5 to 4	RFT	-	reserved for production tests
3 to 0	SelfTest[3:0]	-	enables the digital self test the self test can also be started by the CalcCRC command; see Section 10.3.1.4 on page 71 the self test is enabled by value 1001b **Remark:** for default operation the self test must be disabled by value 0000b

9.3.4.8 VersionReg register

Shows the MFRC522 software version.

Table 131. VersionReg register (address 37h); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Version[7:0]							
Access	R							

Table 132. VersionReg register bit descriptions

Bit	Symbol	Description
7 to 4	Chiptype	'9' stands for MFRC522
3 to 0	Version	'1' stands for MFRC522 version 1.0 and '2' stands for MFRC522 version 2.0.

MFRC522 version 1.0 software version is: 91h.

MFRC522 version 2.0 software version is: 92h.

9.3.4.9 AnalogTestReg register

Determines the analog output test signal at, and status of, pins AUX1 and AUX2.

Table 133. AnalogTestReg register (address 38h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	AnalogSelAux1[3:0]				AnalogSelAux2[3:0]			
Access	R/W				R/W			

Table 134. AnalogTestReg register bit descriptions

Bit	Symbol	Value	Description
7 to 4	AnalogSelAux1 [3:0]		controls pin AUX1
		0000	3-state
		0001	output of TestDAC1 (AUX1), output of TestDAC2 (AUX2)[1]
		0010	test signal Corr1[1]
		0011	reserved
		0100	DAC: test signal MinLevel[1]
		0101	DAC: test signal ADC_I[1]
		0110	DAC: test signal ADC_Q[1]
		0111	reserved
		1000	reserved, test signal for production test[1]
		1001	reserved
		1010	HIGH
		1011	LOW
		1100	TxActive: at 106 kBd: HIGH during Start bit, Data bit, Parity and CRC at 212 kBd: 424 kBd and 848 kBd: HIGH during data and CRC
		1101	RxActive: at 106 kBd: HIGH during Data bit, Parity and CRC at 212 kBd: 424 kBd and 848 kBd: HIGH during data and CRC
		1110	subcarrier detected: 106 kBd: not applicable 212 kBd: 424 kBd and 848 kBd: HIGH during last part of data and CRC
		1111	test bus bit as defined by the TestSel1Reg register's TstBusBitSel[2:0] bits **Remark:** all test signals are described in Section 16.1 on page 82
3 to 0	AnalogSelAux2 [3:0]	-	controls pin AUX2 (see bit descriptions for AUX1)

[1] **Remark:** Current source output; the use of 1 kΩ pull-down resistor on AUXn is recommended.

9.3.4.10 TestDAC1Reg register

Defines the test value for TestDAC1.

Table 135. TestDAC1Reg register (address 39h); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		TestDAC1[5:0]					
Access	-		R/W					

Table 136. TestDAC1Reg register bit descriptions

Bit	Symbol	Description
7	reserved	reserved for production tests
6	reserved	reserved for future use
5 to 0	TestDAC1[5:0]	defines the test value for TestDAC1 output of DAC1 can be routed to AUX1 by setting value AnalogSelAux1[3:0] to 0001b in the AnalogTestReg register

9.3.4.11 TestDAC2Reg register

Defines the test value for TestDAC2.

Table 137. TestDAC2Reg register (address 3Ah); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		TestDAC2[5:0]					
Access	-		R/W					

Table 138. TestDAC2Reg register bit descriptions

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	TestDAC2[5:0]	defines the test value for TestDAC2 output of DAC2 can be routed to AUX2 by setting value AnalogSelAux2[3:0] to 0001b in the AnalogTestReg register

9.3.4.12 TestADCReg register

Shows the values of ADC I and Q channels.

Table 139. TestADCReg register (address 3Bh); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ADC_I[3:0]				ADC_Q[3:0]			
Access	R				R			

Table 140. TestADCReg register bit descriptions

Bit	Symbol	Description
7 to 4	ADC_I[3:0]	ADC I channel value
3 to 0	ADC_Q[3:0]	ADC Q channel value

9.3.4.13 Reserved register 3Ch

Functionality reserved for production test.

Table 141. Reserved register (address 3Ch); reset value: FFh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RFT							
Access	-							

Table 142. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

Table 143. Reserved register (address 3Dh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RFT							
Access	-							

Table 144. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

Table 145. Reserved register (address 3Eh); reset value: 03h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RFT							
Access	-							

Table 146. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

Table 147. Reserved register (address 3Fh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 148. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

10. MFRC522 command set

10.1 General description

The MFRC522 operation is determined by a state machine capable of performing a set of commands. A command is executed by writing a command code (see Table 149) to the CommandReg register.

Arguments and/or data necessary to process a command are exchanged via the FIFO buffer.

10.2 General behavior

- Each command that needs a data bit stream (or data byte stream) as an input immediately processes any data in the FIFO buffer. An exception to this rule is the Transceive command. Using this command, transmission is started with the BitFramingReg register's StartSend bit.
- Each command that needs a certain number of arguments, starts processing only when it has received the correct number of arguments from the FIFO buffer.
- The FIFO buffer is not automatically cleared when commands start. This makes it possible to write command arguments and/or the data bytes to the FIFO buffer and then start the command.
- Each command can be interrupted by the host writing a new command code to the CommandReg register, for example, the Idle command.

10.3 MFRC522 command overview

Table 149. Command overview

Command	Command code	Action
Idle	0000	no action, cancels current command execution
Mem	0001	stores 25 bytes into the internal buffer
Generate RandomID	0010	generates a 10-byte random ID number
CalcCRC	0011	activates the CRC coprocessor or performs a self test
Transmit	0100	transmits data from the FIFO buffer
NoCmdChange	0111	no command change, can be used to modify the CommandReg register bits without affecting the command, for example, the PowerDown bit
Receive	1000	activates the receiver circuits
Transceive	1100	transmits data from FIFO buffer to antenna and automatically activates the receiver after transmission
-	1101	reserved for future use
MFAuthent	1110	performs the MIFARE standard authentication as a reader
SoftReset	1111	resets the MFRC522

10.3.1 MFRC522 command descriptions

10.3.1.1 Idle

Places the MFRC522 in Idle mode. The Idle command also terminates itself.

10.3.1.2 Mem

Transfers 25 bytes from the FIFO buffer to the internal buffer.

To read out the 25 bytes from the internal buffer the Mem command must be started with an empty FIFO buffer. In this case, the 25 bytes are transferred from the internal buffer to the FIFO.

During a hard power-down (using pin NRSTPD), the 25 bytes in the internal buffer remain unchanged and are only lost if the power supply is removed from the MFRC522.

This command automatically terminates when finished and the Idle command becomes active.

10.3.1.3 Generate RandomID

This command generates a 10-byte random number which is initially stored in the internal buffer. This then overwrites the 10 bytes in the internal 25-byte buffer. This command automatically terminates when finished and the MFRC522 returns to Idle mode.

10.3.1.4 CalcCRC

The FIFO buffer content is transferred to the CRC coprocessor and the CRC calculation is started. The calculation result is stored in the CRCResultReg register. The CRC calculation is not limited to a dedicated number of bytes. The calculation is not stopped when the FIFO buffer is empty during the data stream. The next byte written to the FIFO buffer is added to the calculation.

The CRC preset value is controlled by the ModeReg register's CRCPreset[1:0] bits. The value is loaded in to the CRC coprocessor when the command starts.

This command must be terminated by writing a command to the CommandReg register, such as, the Idle command.

If the AutoTestReg register's SelfTest[3:0] bits are set correctly, the MFRC522 enters Self Test mode. Starting the CalcCRC command initiates a digital self test. The result of the self test is written to the FIFO buffer.

10.3.1.5 Transmit

The FIFO buffer content is immediately transmitted after starting this command. Before transmitting the FIFO buffer content, all relevant registers must be set for data transmission.

This command automatically terminates when the FIFO buffer is empty. It can be terminated by another command written to the CommandReg register.

10.3.1.6 NoCmdChange

This command does not influence any running command in the CommandReg register. It can be used to manipulate any bit except the CommandReg register Command[3:0] bits, for example, the RcvOff bit or the PowerDown bit.

10.3.1.7 Receive

The MFRC522 activates the receiver path and waits for a data stream to be received. The correct settings must be chosen before starting this command.

This command automatically terminates when the data stream ends. This is indicated either by the end of frame pattern or by the length byte depending on the selected frame type and speed.

Remark: If the RxModeReg register's RxMultiple bit is set to logic 1, the Receive command will not automatically terminate. It must be terminated by starting another command in the CommandReg register.

10.3.1.8 Transceive

This command continuously repeats the transmission of data from the FIFO buffer and the reception of data from the RF field. The first action is transmit and after transmission the command is changed to receive a data stream.

Each transmit process must be started by setting the BitFramingReg register's StartSend bit to logic 1. This command must be cleared by writing any command to the CommandReg register.

Remark: If the RxModeReg register's RxMultiple bit is set to logic 1, the Transceive command never leaves the receive state because this state cannot be cancelled automatically.

10.3.1.9 MFAuthent

This command manages MIFARE authentication to enable a secure communication to any MIFARE Mini, MIFARE 1K and MIFARE 4K card. The following data is written to the FIFO buffer before the command can be activated:

- Authentication command code (60h, 61h)
- Block address
- Sector key byte 0
- Sector key byte 1
- Sector key byte 2
- Sector key byte 3
- Sector key byte 4
- Sector key byte 5
- Card serial number byte 0
- Card serial number byte 1
- Card serial number byte 2
- Card serial number byte 3

In total 12 bytes are written to the FIFO.

Remark: When the MFAuthent command is active all access to the FIFO buffer is blocked. However, if there is access to the FIFO buffer, the ErrorReg register's WrErr bit is set.

This command automatically terminates when the MIFARE card is authenticated and the Status2Reg register's MFCrypto1On bit is set to logic 1.

This command does not terminate automatically if the card does not answer, so the timer must be initialized to automatic mode. In this case, in addition to the IdleIRq bit, the TimerIRq bit can be used as the termination criteria. During authentication processing, the RxIRq bit and TxIRq bit are blocked. The Crypto1On bit is only valid after termination of the MFAuthent command, either after processing the protocol or writing Idle to the CommandReg register.

If an error occurs during authentication, the ErrorReg register's ProtocolErr bit is set to logic 1 and the Status2Reg register's Crypto1On bit is set to logic 0.

10.3.1.10 SoftReset

This command performs a reset of the device. The configuration data of the internal buffer remains unchanged. All registers are set to the reset values. This command automatically terminates when finished.

Remark: The SerialSpeedReg register is reset and therefore the serial data rate is set to 9.6 kBd.

11. Limiting values

Table 150. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	analog supply voltage		–0.5	+4.0	V
V_{DDD}	digital supply voltage		–0.5	+4.0	V
$V_{DD(PVDD)}$	PVDD supply voltage		–0.5	+4.0	V
$V_{DD(TVDD)}$	TVDD supply voltage		–0.5	+4.0	V
$V_{DD(SVDD)}$	SVDD supply voltage		–0.5	+4.0	V
V_I	input voltage	all input pins except pins MFIN and RX	$V_{SS(PVSS)}$ – 0.5	$V_{DD(PVDD)}$ + 0.5	V
		pin MFIN	$V_{SS(PVSS)}$ – 0.5	$V_{DD(SVDD)}$ + 0.5	V
P_{tot}	total power dissipation	per package; and V_{DDD} in shortcut mode	-	200	mW
T_j	junction temperature		-	100	°C
V_{ESD}	electrostatic discharge voltage	HBM; 1500 Ω, 100 pF; JESD22-A114-B	-	2000	V
		MM; 0.75 μH, 200 pF; JESD22-A114-A	-	200	V
		Charged device model; JESD22-C101-A			
		on all pins	-	200	V
		on all pins except SVDD in TFBGA64 package	-	500	V

12. Recommended operating conditions

Table 151. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	analog supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
V_{DDD}	digital supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
$V_{DD(TVDD)}$	TVDD supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
$V_{DD(PVDD)}$	PVDD supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[3]	1.6	1.8	3.6	V
$V_{DD(SVDD)}$	SVDD supply voltage	$V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V		1.6	-	3.6	V
T_{amb}	ambient temperature	HVQFN32		–25	-	+85	°C

[1] Supply voltages below 3 V reduce the performance (the achievable operating distance).

[2] V_{DDA}, V_{DDD} and $V_{DD(TVDD)}$ must always be the same voltage.

[3] $V_{DD(PVDD)}$ must always be the same or lower voltage than V_{DDD}.

13. Thermal characteristics

Table 152. Thermal characteristics

Symbol	Parameter	Conditions		Package	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in still air with exposed pin soldered on a 4 layer JEDEC PCB		HVQFN32	40	K/W

14. Characteristics

Table 153. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input characteristics							
Pins EA, I2C and NRSTPD							
I_{LI}	input leakage current			–1	-	+1	µA
V_{IH}	HIGH-level input voltage			$0.7V_{DD(PVDD)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(PVDD)}$	V
Pin MFIN							
I_{LI}	input leakage current			–1	-	+1	µA
V_{IH}	HIGH-level input voltage			$0.7V_{DD(SVDD)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(SVDD)}$	V
Pin SDA							
I_{LI}	input leakage current			–1	-	+1	µA
V_{IH}	HIGH-level input voltage			$0.7V_{DD(PVDD)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(PVDD)}$	V
Pin RX[1]							
V_i	input voltage			–1	-	V_{DDA} +1	V
C_i	input capacitance	V_{DDA} = 3 V; receiver active; $V_{RX(p-p)}$ = 1 V; 1.5 V (DC) offset		-	10	-	pF
R_i	input resistance	V_{DDA} = 3 V; receiver active; $V_{RX(p-p)}$ = 1 V; 1.5 V (DC) offset		-	350	-	Ω
Input voltage range; see Figure 24							
$V_{i(p-p)(min)}$	minimum peak-to-peak input voltage	Manchester encoded; V_{DDA} = 3 V		-	100	-	mV
$V_{i(p-p)(max)}$	maximum peak-to-peak input voltage	Manchester encoded; V_{DDA} = 3 V		-	4	-	V
Input sensitivity; see Figure 24							
V_{mod}	modulation voltage	minimum Manchester encoded; V_{DDA} = 3 V; RxGain[2:0] = 111b (48 dB)		-	5	-	mV
Pin OSCIN							
I_{LI}	input leakage current			–1	-	+1	µA
V_{IH}	HIGH-level input voltage			$0.7V_{DDA}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DDA}$	V

Table 153. Characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_i	input capacitance	V_{DDA} = 2.8 V; DC = 0.65 V; AC = 1 V (p-p)		-	2	-	pF
Input/output characteristics							
pins D1, D2, D3, D4, D5, D6 and D7							
I_{LI}	input leakage current			−1	-	+1	μA
V_{IH}	HIGH-level input voltage			$0.7V_{DD(PVDD)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(PVDD)}$	V
V_{OH}	HIGH-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA		$V_{DD(PVDD)}$ − 0.4	-	$V_{DD(PVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA		$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OH}	HIGH-level output current	$V_{DD(PVDD)}$ = 3 V		-	-	4	mA
I_{OL}	LOW-level output current	$V_{DD(PVDD)}$ = 3 V		-	-	4	mA
Output characteristics							
Pin MFOUT							
V_{OH}	HIGH-level output voltage	$V_{DD(SVDD)}$ = 3 V; I_O = 4 mA		$V_{DD(SVDD)}$ − 0.4	-	$V_{DD(SVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(SVDD)}$ = 3 V; I_O = 4 mA		$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OL}	LOW-level output current	$V_{DD(SVDD)}$ = 3 V		-	-	4	mA
I_{OH}	HIGH-level output current	$V_{DD(SVDD)}$ = 3 V		-	-	4	mA
Pin IRQ							
V_{OH}	HIGH-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA		$V_{DD(PVDD)}$ − 0.4	-	$V_{DD(PVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA		$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OL}	LOW-level output current	$V_{DD(PVDD)}$ = 3 V		-	-	4	mA
I_{OH}	HIGH-level output current	$V_{DD(PVDD)}$ = 3 V		-	-	4	mA
Pins AUX1 and AUX2							
V_{OH}	HIGH-level output voltage	V_{DDD} = 3 V; I_O = 4 mA		V_{DDD} − 0.4	-	V_{DDD}	V
V_{OL}	LOW-level output voltage	V_{DDD} = 3 V; I_O = 4 mA		$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OL}	LOW-level output current	V_{DDD} = 3 V		-	-	4	mA
I_{OH}	HIGH-level output current	V_{DDD} = 3 V		-	-	4	mA
Pins TX1 and TX2							

Table 153. Characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_{DD(TVDD)}$ = 3 V; $I_{DD(TVDD)}$ = 32 mA; CWGsP[5:0] = 3Fh		$V_{DD(TVDD)}$ − 0.15	-	-	V
		$V_{DD(TVDD)}$ = 3 V; $I_{DD(TVDD)}$ = 80 mA; CWGsP[5:0] = 3Fh		$V_{DD(TVDD)}$ − 0.4	-	-	V
		$V_{DD(TVDD)}$ = 2.5 V; $I_{DD(TVDD)}$ = 32 mA; CWGsP[5:0] = 3Fh		$V_{DD(TVDD)}$ − 0.24	-	-	V
		$V_{DD(TVDD)}$ = 2.5 V; $I_{DD(TVDD)}$ = 80 mA; CWGsP[5:0] = 3Fh		$V_{DD(TVDD)}$ − 0.64	-	-	V
V_{OL}	LOW-level output voltage	$V_{DD(TVDD)}$ = 3 V; $I_{DD(TVDD)}$ = 32 mA; CWGsP[5:0] = 0Fh		-	-	0.15	V
		$V_{DD(TVDD)}$ = 3 V; $I_{DD(TVDD)}$ = 80 mA; CWGsP[5:0] = 0Fh		-	-	0.4	V
		$V_{DD(TVDD)}$ = 2.5 V; $I_{DD(TVDD)}$ = 32 mA; CWGsP[5:0] = 0Fh		-	-	0.24	V
		$V_{DD(TVDD)}$ = 2.5 V; $I_{DD(TVDD)}$ = 80 mA; CWGsP[5:0] = 0Fh		-	-	0.64	V
Current consumption							
I_{pd}	power-down current	V_{DDA} = V_{DDD} = $V_{DD(TVDD)}$ = $V_{DD(PVDD)}$ = 3 V					
		hard power-down; pin NRSTPD set LOW	[2]	-	-	5	µA
		soft power-down; RF level detector on	[2]	-	-	10	µA
I_{DDD}	digital supply current	pin DVDD; V_{DDD} = 3 V		-	6.5	9	mA
I_{DDA}	analog supply current	pin AVDD; V_{DDA} = 3 V; CommandReg register's bit RcvOff = 0		-	7	10	mA
		pin AVDD; receiver switched off; V_{DDA} = 3 V; CommandReg register's bit RcvOff = 1		-	3	5	mA
$I_{DD(PVDD)}$	PVDD supply current	pin PVDD	[3]	-	-	40	mA
$I_{DD(TVDD)}$	TVDD supply current	pin TVDD; continuous wave	[4][5][6]	-	60	100	mA
$I_{DD(SVDD)}$	SVDD supply current	pin SVDD	[7]	-	-	4	mA
Clock frequency							
f_{clk}	clock frequency			-	27.12	-	MHz
δ_{clk}	clock duty cycle			40	50	60	%
t_{jit}	jitter time	RMS		-	-	10	ps
Crystal oscillator							

Table 153. Characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	pin OSCOUT		-	1.1	-	V
V_{OL}	LOW-level output voltage	pin OSCOUT		-	0.2	-	V
C_i	input capacitance	pin OSCOUT		-	2	-	pF
		pin OSCIN		-	2	-	pF
Typical input requirements							
f_{xtal}	crystal frequency			-	27.12	-	MHz
ESR	equivalent series resistance			-	-	100	Ω
C_L	load capacitance			-	10	-	pF
P_{xtal}	crystal power dissipation			-	50	100	mW

[1] The voltage on pin RX is clamped by internal diodes to pins AVSS and AVDD.

[2] I_{pd} is the total current for all supplies.

[3] $I_{DD(PVDD)}$ depends on the overall load at the digital pins.

[4] $I_{DD(TVDD)}$ depends on $V_{DD(TVDD)}$ and the external circuit connected to pins TX1 and TX2.

[5] During typical circuit operation, the overall current is below 100 mA.

[6] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between pins TX1 and TX2 at 13.56 MHz.

[7] $I_{DD(SVDD)}$ depends on the load at pin MFOUT.

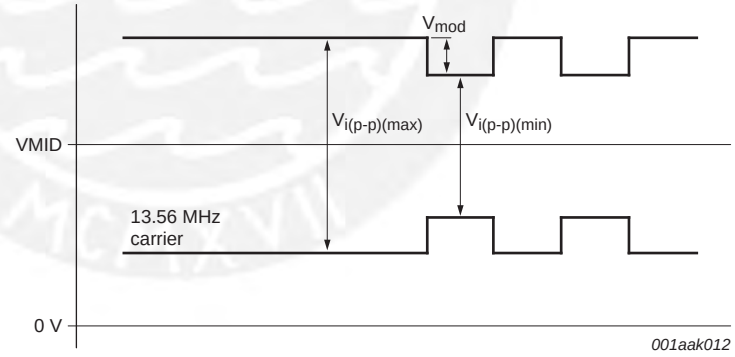


Fig 24. Pin RX input voltage range

14.1 Timing characteristics

Table 154. SPI timing characteristics

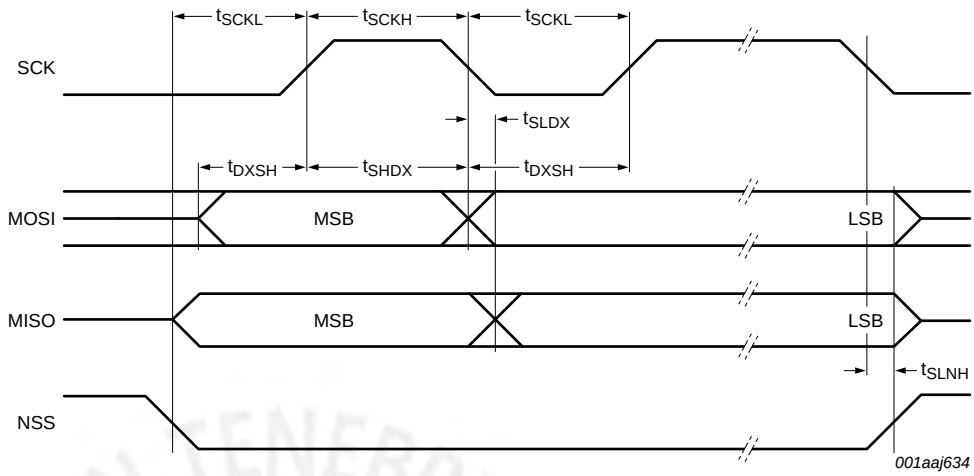
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{WL}	pulse width LOW	line SCK		50	-	-	ns
t_{WH}	pulse width HIGH	line SCK		50	-	-	ns
$t_{h(SCKH-D)}$	SCK HIGH to data input hold time	SCK to changing MOSI		25	-	-	ns

Table 154. SPI timing characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{su(D-SCKH)}$	data input to SCK HIGH set-up time	changing MOSI to SCK		25	-	-	ns
$t_{h(SCKL-Q)}$	SCK LOW to data output hold time	SCK to changing MISO		-	-	25	ns
$t_{(SCKL-NSSH)}$	SCK LOW to NSS HIGH time			0	-	-	ns
t_{NHNL}	NSS high before communication			50	-	-	ns

Table 155. I^2C-bus timing in Fast mode

Symbol	Parameter	Conditions	Fast mode		High-speed mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	400	0	3400	kHz
$t_{HD;STA}$	hold time (repeated) START condition	after this period, the first clock pulse is generated	600	-	160	-	ns
$t_{SU;STA}$	set-up time for a repeated START condition		600	-	160	-	ns
$t_{SU;STO}$	set-up time for STOP condition		600	-	160	-	ns
t_{LOW}	LOW period of the SCL clock		1300	-	160	-	ns
t_{HIGH}	HIGH period of the SCL clock		600	-	60	-	ns
$t_{HD;DAT}$	data hold time		0	900	0	70	ns
$t_{SU;DAT}$	data set-up time		100	-	10	-	ns
t_r	rise time	SCL signal	20	300	10	40	ns
t_f	fall time	SCL signal	20	300	10	40	ns
t_r	rise time	SDA and SCL signals	20	300	10	80	ns
t_f	fall time	SDA and SCL signals	20	300	10	80	ns
t_{BUF}	bus free time between a STOP and START condition		1.3	-	1.3	-	µs



Remark: The signal NSS must be LOW to be able to send several bytes in one data stream. To send more than one data stream NSS must be set HIGH between the data streams.

Fig 25. Timing diagram for SPI

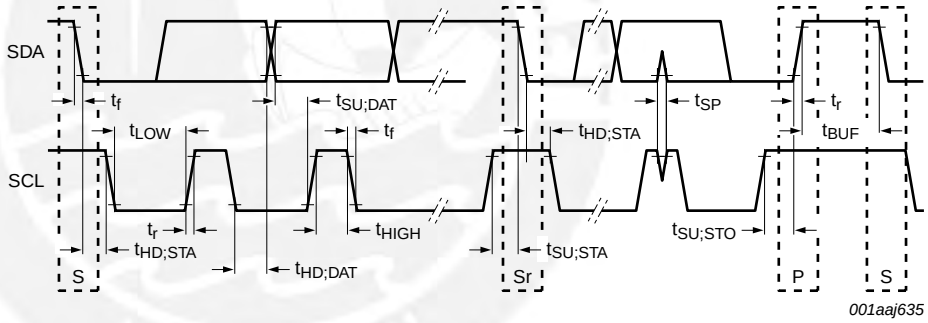


Fig 26. Timing for Fast and Standard mode devices on the I^2C-bus

15. Application information

A typical application diagram using a complementary antenna connection to the MFRC522 is shown in Figure 27.

The antenna tuning and RF part matching is described in the application note Ref. 1 and Ref. 2.

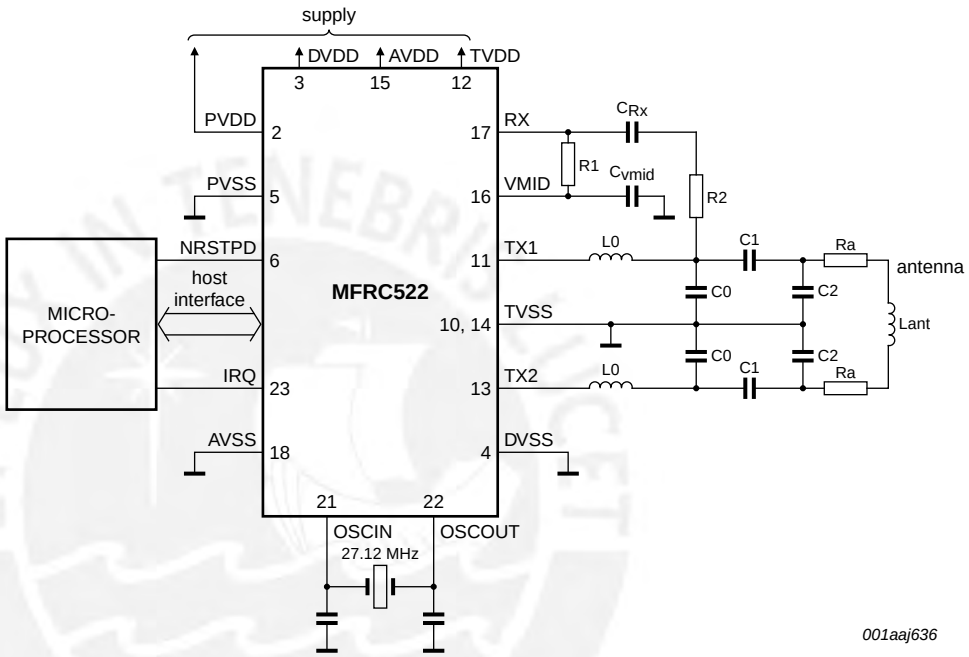


Fig 27. Typical application diagram

16. Test information

16.1 Test signals

16.1.1 Self test

The MFRC522 has the capability to perform a digital self test. The self test is started by using the following procedure:

1. Perform a soft reset.
2. Clear the internal buffer by writing 25 bytes of 00h and implement the Config command.
3. Enable the self test by writing 09h to the AutoTestReg register.
4. Write 00h to the FIFO buffer.
5. Start the self test with the CalcCRC command.
6. The self test is initiated.
7. When the self test has completed, the FIFO buffer contains the following 64 bytes:

FIFO buffer byte values for MFRC522 version 1.0:

00h, C6h, 37h, D5h, 32h, B7h, 57h, 5Ch,
C2h, D8h, 7Ch, 4Dh, D9h, 70h, C7h, 73h,
10h, E6h, D2h, AAh, 5Eh, A1h, 3Eh, 5Ah,
14h, AFh, 30h, 61h, C9h, 70h, DBh, 2Eh,
64h, 22h, 72h, B5h, BDh, 65h, F4h, ECh,
22h, BCh, D3h, 72h, 35h, CDh, AAh, 41h,
1Fh, A7h, F3h, 53h, 14h, DEh, 7Eh, 02h,
D9h, 0Fh, B5h, 5Eh, 25h, 1Dh, 29h, 79h

FIFO buffer byte values for MFRC522 version 2.0:

00h, EBh, 66h, BAh, 57h, BFh, 23h, 95h,
D0h, E3h, 0Dh, 3Dh, 27h, 89h, 5Ch, DEh,
9Dh, 3Bh, A7h, 00h, 21h, 5Bh, 89h, 82h,
51h, 3Ah, EBh, 02h, 0Ch, A5h, 00h, 49h,
7Ch, 84h, 4Dh, B3h, CCh, D2h, 1Bh, 81h,
5Dh, 48h, 76h, D5h, 71h, 061h, 21h, A9h,
86h, 96h, 83h, 38h, CFh, 9Dh, 5Bh, 6Dh,
DCh, 15h, BAh, 3Eh, 7Dh, 95h, 03Bh, 2Fh

16.1.2 Test bus

The test bus is used for production tests. The following configuration can be used to improve the design of a system using the MFRC522. The test bus allows internal signals to be routed to the digital interface. The test bus comprises two sets of test signals which are selected using their subaddress specified in the TestSel2Reg register's TestBusSel[4:0] bits. The test signals and their related digital output pins are described in Table 156 and Table 157.

Table 156. Test bus signals: TestBusSel[4:0] = 07h

Pins	Internal signal name	Description
D6	s_data	received data stream
D5	s_coll	bit-collision detected (106 kBd only)
D4	s_valid	s_data and s_coll signals are valid
D3	s_over	receiver has detected a stop condition
D2	RCV_reset	receiver is reset
D1	-	reserved

Table 157. Test bus signals: TestBusSel[4:0] = 0Dh

Pins	Internal test signal name	Description
D6	clkstable	oscillator output signal
D5	clk27/8	oscillator output signal divided by 8
D4 to D3	-	reserved
D2	clk27	oscillator output signal
D1	-	reserved

16.1.3 Test signals on pins AUX1 or AUX2

The MFRC522 allows the user to select internal signals for measurement on pins AUX1 or AUX2. These measurements can be helpful during the design-in phase to optimize the design or used for test purposes.

Table 158 shows the signals that can be switched to pin AUX1 or AUX2 by setting AnalogSelAux1[3:0] or AnalogSelAux2[3:0] in the AnalogTestReg register.

Remark: The DAC has a current output, therefore it is recommended that a 1 kΩ pull-down resistor is connected to pin AUX1 or AUX2.

Table 158. Test signal descriptions

AnalogSelAux1[3:0] or AnalogSelAux2[3:0] value	Signal on pin AUX1 or pin AUX2
0000	3-state
0001	DAC: register TestDAC1 or TestDAC2
0010	DAC: test signal Corr1
0011	reserved
0100	DAC: test signal MinLevel
0101	DAC: test signal ADC_I
0110	DAC: test signal ADC_Q
0111 to 1001	reserved
1010	HIGH
1011	LOW
1100	TxActive

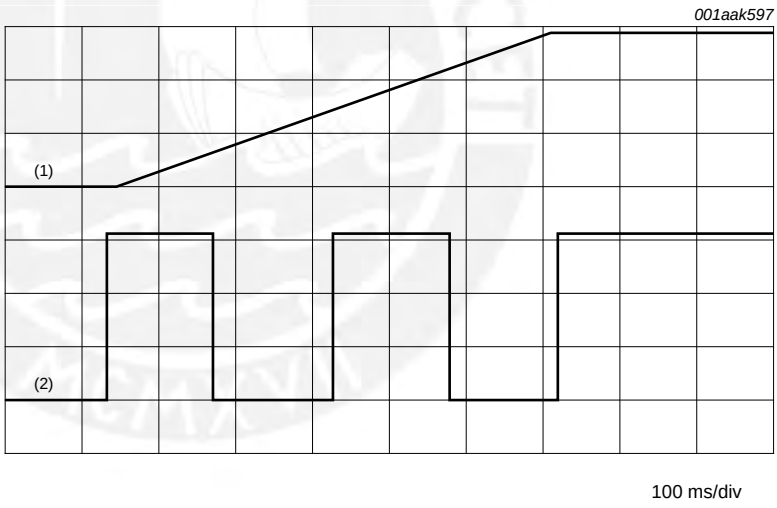
Table 158. Test signal descriptions *...continued*

AnalogSelAux1[3:0] or AnalogSelAux2[3:0] value	Signal on pin AUX1 or pin AUX2
1101	RxActive
1110	subcarrier detected
1111	TstBusBit

16.1.3.1 Example: Output test signals TestDAC1 and TestDAC2

The AnalogTestReg register is set to 11h. The output on pin AUX1 has the test signal TestDAC1 and the output on pin AUX2 has the test signal TestDAC2. The signal values of TestDAC1 and TestDAC2 are controlled by the TestDAC1Reg and TestDAC2Reg registers.

Figure 28 shows test signal TestDAC1 on pin AUX1 and TestDAC2 on pin AUX2 when the TestDAC1Reg register is programmed with a slope defined by values 00h to 3Fh and the TestDAC2Reg register is programmed with a rectangular signal defined by values 00h and 3Fh.

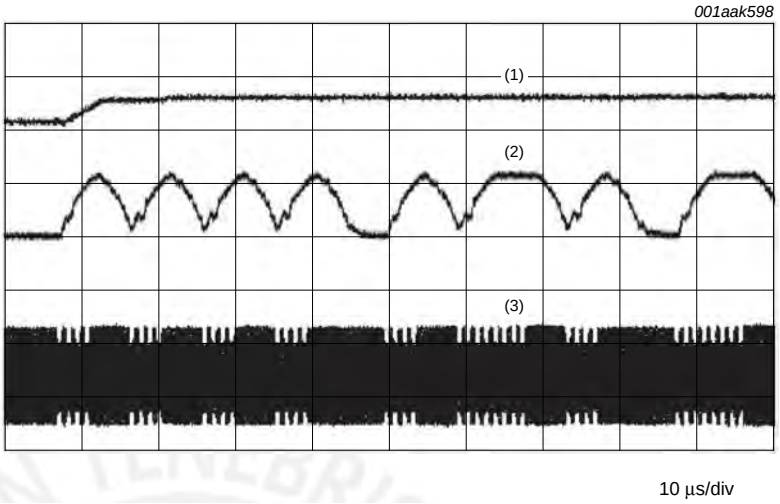


(1) TestDAC1 (500 mV/div) on pin AUX1.
(2) TestDAC2 (500 mV/div) on pin AUX2.

Fig 28. Output test signals TestDAC1 on pin AUX1 and TestDAC2 on pin AUX2

16.1.3.2 Example: Output test signals Corr1 and MinLevel

Figure 29 shows test signals Corr1 and MinLevel on pins AUX1 and AUX2, respectively. The AnalogTestReg register is set to 24h.

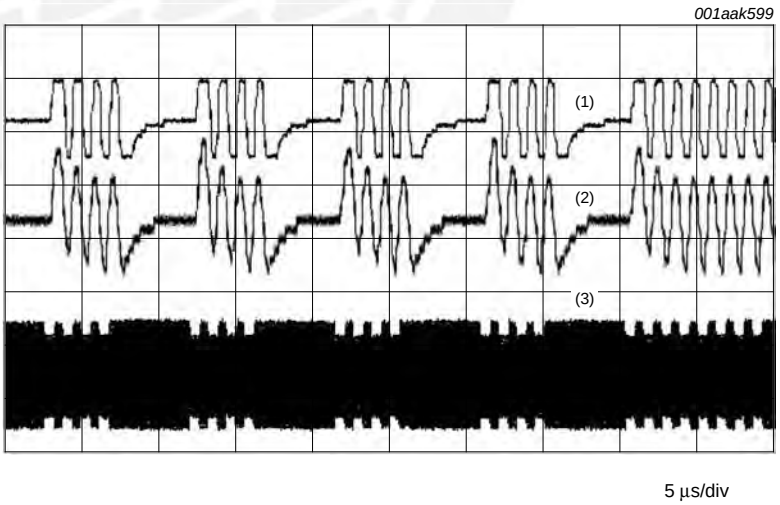


(1) MinLevel (1 V/div) on pin AUX2.
(2) Corr1 (1 V/div) on pin AUX1.
(3) RF field.

Fig 29. Output test signals Corr1 on pin AUX1 and MinLevel on pin AUX2

16.1.3.3 Example: Output test signals ADC channel I and ADC channel Q

Figure 30 shows the channel behavior test signals ADC_I and ADC_Q on pins AUX1 and AUX2, respectively. The AnalogTestReg register is set to 56h.



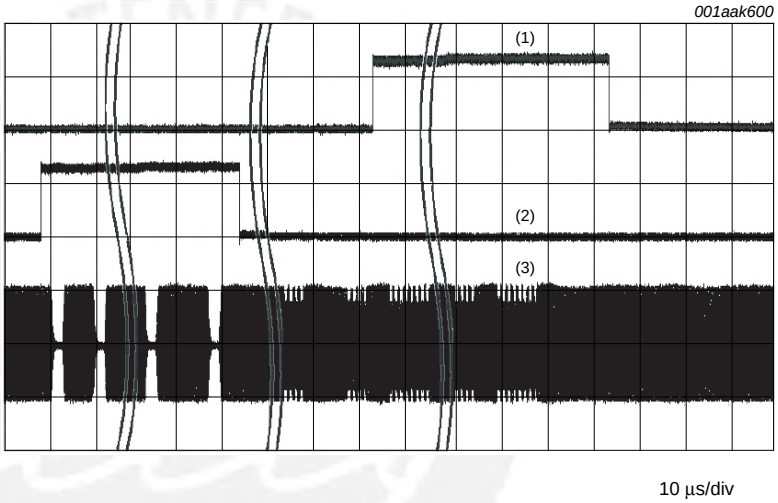
(1) ADC_I (1 V/div) on pin AUX1.
(2) ADC_Q (500 mV/div) on pin AUX2.
(3) RF field.

Fig 30. Output ADC channel I on pin AUX1 and ADC channel Q on pin AUX2

16.1.3.4 Example: Output test signals RxActive and TxActive

Figure 31 shows the RxActive and TxActive test signals relating to RF communication. The AnalogTestReg register is set to CDh.

- At 106 kBd, RxActive is HIGH during data bits, parity and CRC reception. Start bits are not included
- At 106 kBd, TxActive is HIGH during start bits, data bits, parity and CRC transmission
- At 212 kBd, 424 kBd and 848 kBd, RxActive is HIGH during data bits and CRC reception. Start bits are not included
- At 212 kBd, 424 kBd and 848 kBd, TxActive is HIGH during data bits and CRC transmission

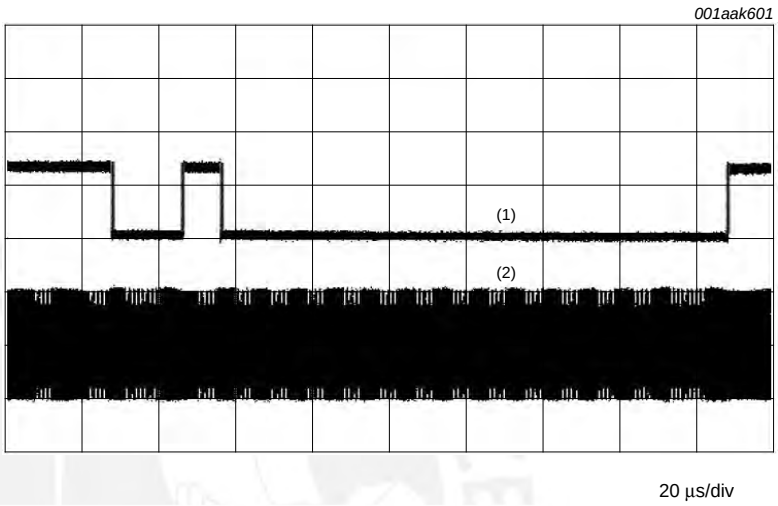


(1) RxActive (2 V/div) on pin AUX1.
(2) TxActive (2 V/div) on pin AUX2.
(3) RF field.

Fig 31. Output RxActive on pin AUX1 and TxActive on pin AUX2

16.1.3.5 Example: Output test signal RX data stream

Figure 32 shows the data stream that is currently being received. The TestSel2Reg register's TestBusSel[4:0] bits are set to 07h to enable test bus signals on pins D1 to D6; see Section 16.1.2 on page 82. The TestSel1Reg register's TstBusBitSel[2:0] bits are set to 06h (pin D6 = s_data) and AnalogTestReg register is set to FFh (TstBusBit) which outputs the received data stream on pins AUX1 and AUX2.



(1) s_data (received data stream) (2 V/div).

(2) RF field.

Fig 32. Received data stream on pins AUX1 and AUX2

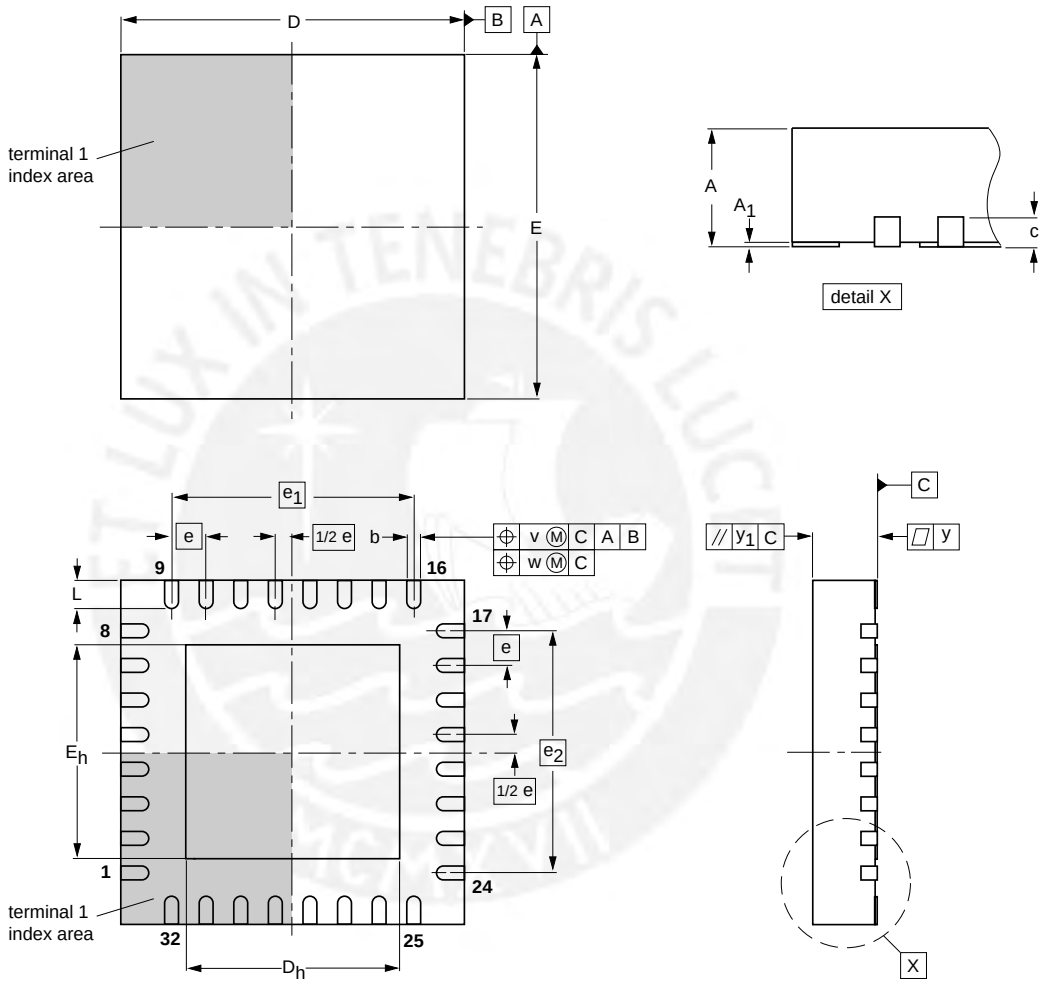
16.1.3.6 PRBS

The pseudo-random binary sequences PRBS9 and PRBS15 are based on ITU-TO150 and are defined with the TestSel2Reg register. Transmission of either data stream is started by the Transmit command. The preamble/sync byte/start bit/parity bit are automatically generated depending on the mode selected.

Remark: All relevant registers for transmitting data must be configured in accordance with ITU-TO150 before selecting PRBS transmission.

17. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

Fig 33. Package outline SOT617-1 (HVQFN32)

Detailed package information can be found at:
http://www.nxp.com/package/SOT617-1.html.

18. Handling information

Moisture Sensitivity Level (MSL) evaluation has been performed according to *SNW-FQ-225B rev.04/07/07 (JEDEC J-STD-020C)*. MSL for this package is level 1 which means 260 °C convection reflow temperature.

Dry pack is not required.

Unlimited out-of-pack floor life at maximum ambient 30 °C/85 % RH.

19. Packing information

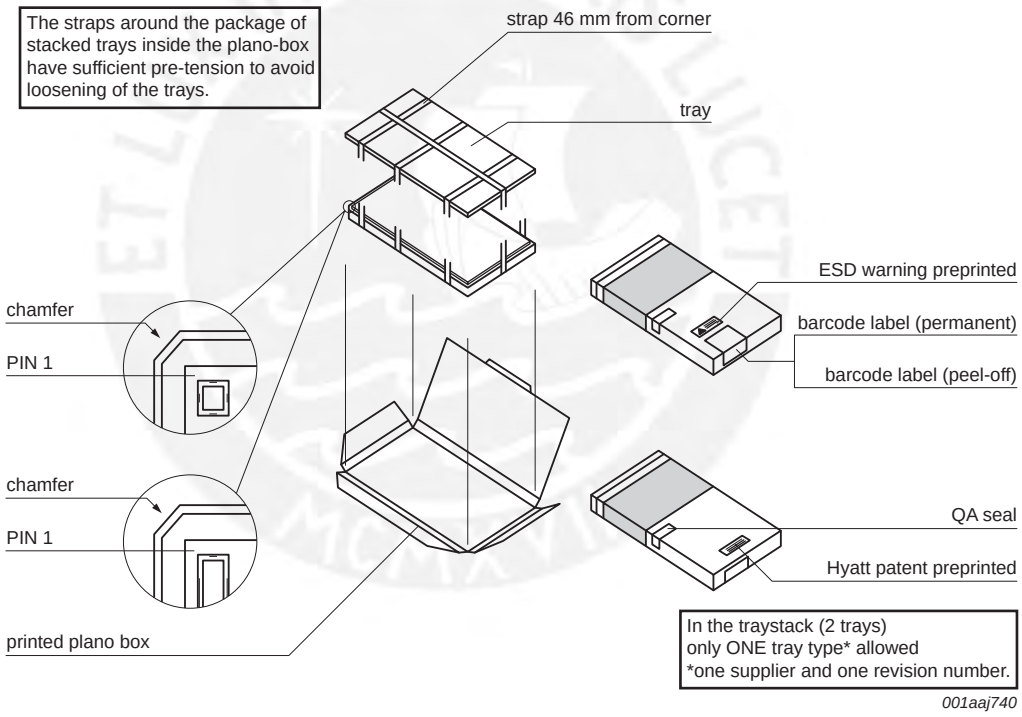


Fig 34. Packing information 1 tray

20. Abbreviations

Table 159. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
BPSK	Binary Phase Shift Keying
CRC	Cyclic Redundancy Check
CW	Continuous Wave
DAC	Digital-to-Analog Converter
HBM	Human Body Model
I^2C	Inter-integrated Circuit
LSB	Least Significant Bit
MISO	Master In Slave Out
MM	Machine Model
MOSI	Master Out Slave In
MSB	Most Significant Bit
NRZ	Not Return to Zero
NSS	Not Slave Select
PLL	Phase-Locked Loop
PRBS	Pseudo-Random Bit Sequence
RX	Receiver
SOF	Start Of Frame
SPI	Serial Peripheral Interface
TX	Transmitter
UART	Universal Asynchronous Receiver Transmitter

21. References

[1] **Application note —** *MFRC52x Reader IC Family Directly Matched Antenna Design*

[2] **Application note —** *MIFARE (ISO/IEC 14443 A) 13.56 MHz RFID Proximity Antennas*

22. Revision history

Table 160. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MFRC522 v.3.9	20160427	Product data sheet	-	MFRC522 v.3.8
Modifications:	• Section 1 “Introduction” and Section 2 “General description”: updated and NTAG functionality added • Descriptive title updated			
MFRC522 v.3.8	20140917	Product data sheet	-	MFRC522 v.3.7
Modifications:	• Table 150 “Limiting values”: updated			
MFRC522 v.3.7	20140326	Product data sheet	-	MFRC522 v.3.6
Modifications:	• Change of descriptive title • Section 23.4 “Licenses” removed			
MFRC522 v.3.6	20111214	Product data sheet	-	MFRC522_35
Modifications:	• Section 1.1 “Differences between version 1.0 and 2.0” on page 1: added • Table 2 “Ordering information” on page 3: updated • Section 9.3.2.10 “DemodReg register” on page 53: register updated and add reference to Timer unit • Section 8.5 “Timer unit” on page 31: Pre Scaler Information for version 2.0 added • Section 9.3.4.8 “VersionReg register” on page 66: version information structured in chip information and version information updated, including version 1.0 and 2.0 • Section 16.1 “Test signals” on page 82: selftest result including values for version 1.0 and 2.0			
MFRC522_35	20100621	Product data sheet		MFRC522_34
Modifications:	• Section 9.3.2.10 “DemodReg register” on page 53: register updated • Section 9.3.3.10 “TModeReg and TPrescalerReg registers” on page 60: register updated • Section 8.5 “Timer unit” on page 31: timer calculation updated • Section 9.3.4.8 “VersionReg register” on page 66: version B2h updated • Section 16.1 “Test signals” on page 82: selftest result updated			
MFRC522_34	20100305	Product data sheet		MFRC522_33
Modifications:	• Section 8.5 “Timer unit”: information added • Table 106 “TModeReg register bit descriptions”: bit 7 updated • Table 154 “SPI timing characteristics”: row added			
MFRC522_33	20091026	Product data sheet	-	112132

23. Legal information

23.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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24. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

25. Contents

continued >>

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Date of release: 27 April 2016
112139

OMRON

Solid State Relay
G3MB

Low cost Subminiature PCB mounting 2 amp Single in-line package (SIP) SSR

- Bottom is approximately 3 times smaller than G3M.
- Low cost “SIP” package switches up to 2A loads.
- Built in Snubber circuit and input resistor as option.
- Two footprints available for design flexibility.
- The G3MB-202PEG-4-DC20MA crosses directly to the Motorola M0C2A-60 series power triac.

Ordering Information

To Order: Specify input voltage at end of part number. Example: G3MB-202P-*DC24*

Isolation	Output terminal pitch	Zero cross	Input resistor	Built-in snubber circuit	Rated output load	Rated input voltage	Model
Phototriac	7.62 mm	Yes	Yes	Yes	2 A at 100 to 240 VAC	5 VDC	**G3MB-202P**
						12 VDC	
						24 VDC	
		No			2 A at 100 to 240 VAC	5 VDC	**G3MB-202PL**
						12 VDC	
						24 VDC	
	5.08 mm	Yes			2 A at 100 to 240 VAC	5 VDC	**G3MB-202P-4**
						12 VDC	
						24 VDC	
		No			2 A at 100 to 240 VAC	5 VDC	**G3MB-202PL-4**
						12 VDC	
						24 VDC	
		Yes	No	No	2 A at 100 to 240 VAC	N/A *(See Note)	**G3MB-202PEG-4-DC20MA**
		No			2 A at 100 to 240 VAC	N/A *(See Note)	**G3MB-202PLEG-4-DC20MA**

Note: 1. For versions without input voltage specified, a current limiting resistor must be placed in series with the input. See LED drive specifications and recommendations below.

2. TUV versions available. Contact your local Omron representative.

Specifications

■ Input Rating

Models with Input Resistor

Rated voltage	Operating range	Input impedance
5 VDC	4 to 6 VDC	440 Ω ±20%
12 VDC	9.60 to 14.40 VDC	1k Ω ±20%
24 VDC	19.20 to 28.80 VDC	2.20k Ω ±20%

■ Output Rating

Model	Rated load voltage	Load voltage range	Load current	Surge current
G3MB-202	100 to 240 VAC	75 to 264 VAC	0.10 to 2 A	30 A (60 Hz, 1 cycle)

■ LED Drive Data

Models without Input Resistor

LED forward current	50 mA max.
Repetitive peak LED forward current	1 A max.
LED reverse voltage	5 V max.

■ Recommended LED Operating Conditions

Models without Input Resistor

	Min.	Standard	Max.
LED forward current	5 mA	10 mA	20 mA
Must drop voltage	0	—	1 V

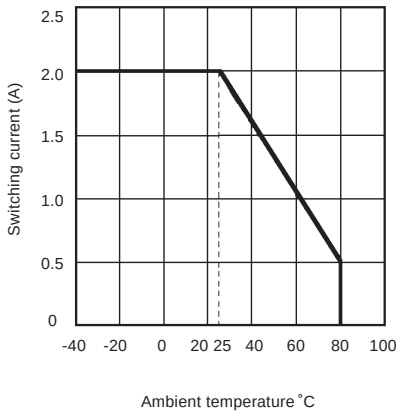
■ Characteristics

Type		G3MB-202P G3MB-202PEG	G3MB-202PL G3MB-202PLEG
Operate time		1/2 of load power source cycle + 1 ms max.	1 ms max.
Release time		1/2 of load power source cycle + 1 ms max.	
Output ON voltage drop		1.60 V (RMS) max.	
Leakage current		1 mA max. at 100 VAC, 1.50 mA at 200 VAC	
Non-repetitive peak surge		30 A	
Output	**PIV (V_{DRM})**	600 V	
	di/dt	40 A/μs	
	dv/dt	100 V/μs	
	I^2t	4 A^2s	
Junction temperature (Tj)		125°C (257°F) max.	
Insulation resistance		1,000 MΩ min. at 500 VDC	
Dielectric strength		2500 VAC, 50/60 Hz for 1 minute; 3750 VAC max., 1 second	
Vibration	**Malfunction**	10 to 55 Hz, 0.75 mm (0.03 in) double amplitude, approx. 5 G	
Shock	**Malfunction**	Approx. 100 G	
Ambient temperature	**Operating**	-30° to 80°C (-22° to 176°F) with no icing	
	Storage	-30° to 100°C (-22° to 212°F) with no icing	
Humidity	**Operating**	45% to 85% RH	
Weight		Approx. 5 g (0.18 oz)	

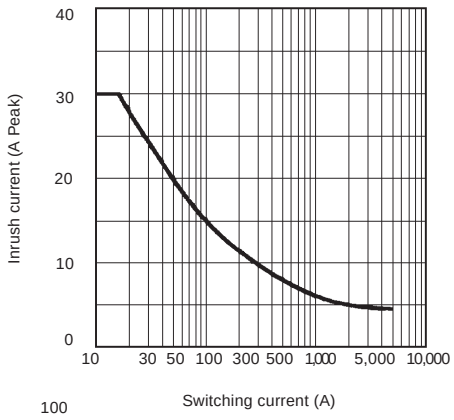
Note: Data shown are of initial value.

■ Characteristic Data

Load current vs. ambient temperature characteristics



Inrush current resistivity
Non-repetitive (Keep the inrush current to half the rated value if it occurs repetitively.)

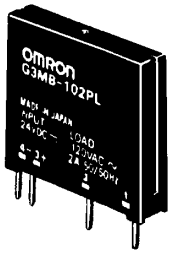


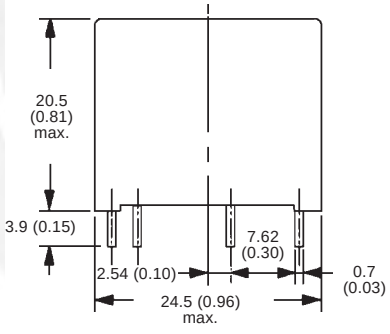
100

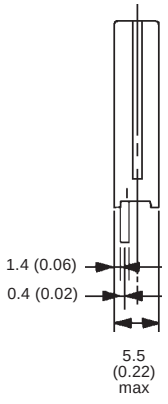
Dimensions

Unit: mm (inch)

■ Relays

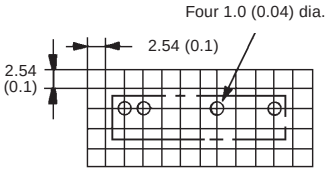




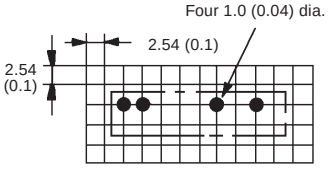


PCB Dimensions
(Bottom view)

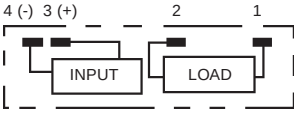
G3MB



G3MB (-4)



Terminal Arrangement/ Internal Connections
(Bottom view)



■ Approvals

UL (File No. E64562)

SSR Type	Input voltage	Load type	Load ratings
G3MB-102P	5 to 24 VDC	General purpose	2 A, 120 VAC
		Tungsten	1 A, 120 VAC
		Motor	1.60 FLA/9.60 LRA, 120 VAC
G3MB-202P		General purpose	2 A, 240 VAC
G3MB-202PL		Tungsten	1 A, 240 VAC
G3MB-202PEG		Motor	1.60 FLA/9.60 LRA, 240 VAC
G3MB-202PLEG			

CSA (File No. LR35535)

SSR Type	Input voltage	Load type	Load ratings
G3MB-102P	5 to 24 VDC	General purpose	2 A, 120 VAC
		Tungsten	1 A, 120 VAC
		Motor	1.60 FLA/8.60 LRA, 120 VAC
G3MB-202P		General purpose	2 A, 240 VAC
G3MB-202PL		Tungsten	1 A, 240 VAC
		Motor	1.60 FLA/8.60 LRA, 240 VAC

Note: 1. The rated values approved by each of the safety standards (e.g., UL and CSA) may be different from the performance characteristics individually defined in this catalog.

2. In the interest of product improvement, specifications are subject to change.

Precautions

See General Information Section near the back of this catalog for Solid State Precautions.

Soldering must be completed within 10 seconds at 260°C or less.

Make sure that the space between the bottom of the relay and the PCB is 0.1 mm or less. When making holes on the PCB for the relay's edge terminals, the hole diameters should be slightly smaller than the actual diameters of the edge terminals. This will reduce unnecessary space between the bottom of the relay and the PCB.

To use the SSR output for phase control, select a model that does not incorporate a zero-cross function.

The SSR case serves to dissipate heat. When mounting more than three SSRs as a group, pay attention to the ambient temperature rise and install the Relays so that they are adequately ventilated. If poor ventilation is unavoidable, reduce the load current by half.

Protective Component

The input circuitry does not incorporate a circuit protecting the SSR from being damaged due to a reversed connection. Make sure that the polarity is correct when connecting the input lines.

ALL DIMENSIONS SHOWN ARE IN MILLIMETERS. To convert millimeters into inches, divide by 25.4

ALL DIMENSIONS SHOWN ARE IN MILLIMETERS. To convert millimeters into inches, divide by 25.4

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Canada - http://www.omron.ca

Cat. No. GC RLY8 5/03 Specifications subject to change without notice Printed in USA

Features

- **Contactless Read/Write Data Transmission**
- **Radio Frequency f_{RF} from 100 kHz to 150 kHz**
- **e5550 Binary Compatible or T5557 Extended Mode**
- **Small Size, Configurable for ISO/IEC 11784/785 Compatibility**
- **75 pF On-chip Resonant Capacitor (Mask Option)**
- **7 × 32-bit EEPROM Data Memory Including 32-bit Password**
- **Separate 64-bit memory for Traceability Data**
- **32-bit Configuration Register in EEPROM to Setup:**
  - **Data Rate**
    - **RF/2 to RF/128, Binary Selectable or**
    - **Fixed e5550 Data Rates**
  - **Modulation/Coding**
    - **FSK, PSK, Manchester, Biphase, NRZ**
  - **Other Options**
    - **Password Mode**
    - **Max Block Feature**
    - **Answer-On-Request (AOR) Mode**
    - **Inverse Data Output**
    - **Direct Access Mode**
    - **Sequence Terminator(s)**
    - **Write Protection (Through Lock-bit per Block)**
    - **Fast Write Method (5 kbps versus 2 kbps)**
    - **OTP Functionality**
    - **POR Delay up to 67 ms**

Multifunctional 330-bit Read/Write RF-Identification IC

T5557

Description

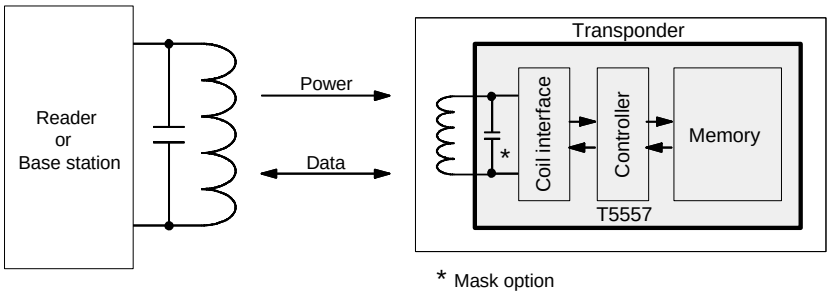
The T5557 is a contactless R/W IDentification IC (IDIC®) for applications in the 125 kHz frequency range. A single coil, connected to the chip, serves as the IC's power supply and bi-directional communication interface. The antenna and chip together form a transponder or tag.

The on-chip 330-bit EEPROM (10 blocks, 33 bits each) can be read and written block-wise from a reader. Block 0 is reserved for setting the operation modes of the T5557 tag. Block 7 may contain a password to prevent unauthorized writing.

Data is transmitted from the IDIC using load modulation. This is achieved by damping the RF field with a resistive load between the two terminals Coil 1 and Coil 2. The IC receives and decodes 100% amplitude modulated (OOK) pulse interval encoded bit streams from the base station or reader.

System Block Diagram

Figure 1. RFID System Using T5557 Tag

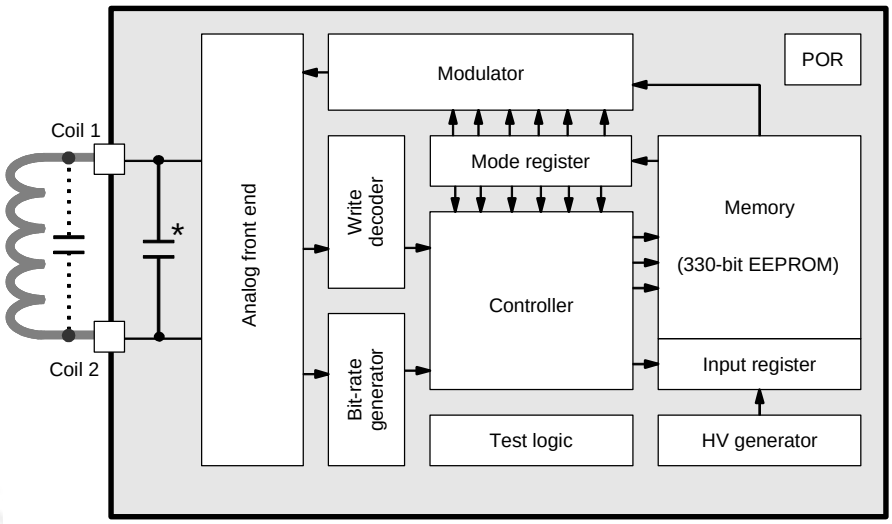


* Mask option

Rev. 4517G–RFID–10/04

T5557 – Building Blocks

Figure 2. Block Diagram



* Mask option

Analog Front End (AFE)

The AFE includes all circuits which are directly connected to the coil. It generates the IC's power supply and handles the bi-directional data communication with the reader. It consists of the following blocks:

- Rectifier to generate a DC supply voltage from the AC coil voltage
- Clock extractor
- Switchable load between Coil 1/Coil 2 for data transmission from tag to the reader
- Field gap detector for data transmission from the base station to the tag
- ESD protection circuitry

Data-rate Generator

The data rate is binary programmable to operate at any data rate between RF/2 and RF/128 or equal to any of the fixed e5550/e5551 and T5554 bitrates (RF/8, RF/16, RF/32, RF/40, RF/50, RF/64, RF/100 and RF/128).

Write Decoder

This function decodes the write gaps and verifies the validity of the data stream according to the Atmel e555x write method (pulse interval encoding).

HV Generator

This on-chip charge pump circuit generates the high voltage required for programming of the EEPROM.

DC Supply

Power is externally supplied to the IDIC via the two coil connections. The IC rectifies and regulates this RF source and uses it to generate its supply voltage.

Power-On Reset (POR)

This circuit delays the IDIC functionality until an acceptable voltage threshold has been reached.

Clock Extraction

The clock extraction circuit uses the external RF signal as its internal clock source.

Controller

The control-logic module executes the following functions:

- Load-mode register with configuration data from EEPROM block 0 after power-on and also during reading
- Control memory access (read, write)
- Handle write data transmission and write error modes
- The first two bits of the reader to tag data stream are the opcode, e.g., write, direct access or reset
- In password mode, the 32 bits received after the opcode are compared with the password stored in memory block 7

Mode Register

The mode register stores the configuration data from the EEPROM block 0. It is continually refreshed at the start of every block read and (re-)loaded after any POR event or reset command. On delivery the mode register is preprogrammed with the value ‘0014 8000’h which corresponds to continuous read of block 0, Manchester coded, RF/64.

Figure 3. Block 0 Configuration Mapping – e5550 Compatibility Mode

L	1 2 3 4	5 6 7 8	9 10 11 12	13 14 15 16	17 18 19 20	21 22 23 24	25 26 27 28	29 30 31 32
	0 1 1 0	0 0 0 0	0 0 0	0		0		0 0
Lock Bit	**Safer Key** Note 1), 2)		**Data Bit Rate**	**Modulation**	**PSK-CF**	**AOR**	**MAX-BLOCK**	**PWD** / **ST-Sequence Terminator** / **POR delay**

Lock Bit

0	Unlocked
1	Locked

Data Bit Rate

RF/8	0	0	0
RF/16	0	0	1
RF/32	0	1	0
RF/40	0	1	1
RF/50	1	0	0
RF/64	1	0	1
RF/100	1	1	0
RF/128	1	1	1

PSK-CF

0	0	RF/2
0	1	RF/4
1	0	RF/8
1	1	Res.

Modulation

0	0	0	0	0	Direct
0	0	0	0	1	PSK1
0	0	0	1	0	PSK2
0	0	0	1	1	PSK3
0	0	1	0	0	FSK1
0	0	1	0	1	FSK2
0	0	1	1	0	FSK1a
0	0	1	1	1	FSK2a
0	1	0	0	0	Manchester
1	0	0	0	0	Biphase('50)
1	1	0	0	0	Reserved

1) If Master Key = 6 then test mode write commands are ignored
2) If Master Key <> 6 or 9 then extended function mode is disabled

Modulator

The modulator consists of data encoders for the following basic types of modulation:

Table 1. Types of e5550-compatible Modulation Modes

Mode	Direct Data Output		
FSK1a[1]	FSK/8-/5	'0' = rf/8;	'1' = rf/5
FSK2a[1]	FSK/8-/10	'0' = rf/8;	'1' = rf/10
FSK1[1]	FSK/5-/8	'0' = rf/5;	'1' = rf/8
FSK2[1]	FSK/10-/8	'0' = rf/10;	1' = rf/8
PSK1[2]	Phase change when input changes		
PSK2[2]	Phase change on bit clock if input high		
PSK3[2]	Phase change on rising edge of input		
Manchester	'0' = falling edge, '1' = rising edge		
Biphase	'1' creates an additional mid-bit change		
NRZ	'1' = damping on, '0' = damping off		

Notes: 1. A common multiple of bitrate and FSK frequencies is recommended.
2. In PSK mode the selected data rate has to be an integer multiple of the PSK sub-carrier frequency.

Memory

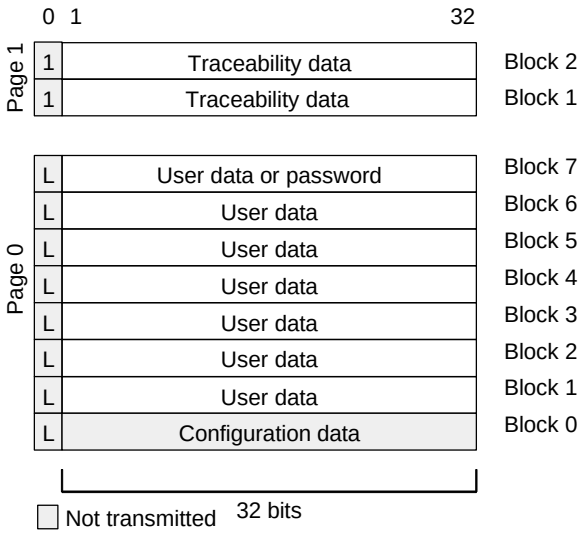
The memory is a 330-bit EEPROM, which is arranged in 10 blocks of 33 bits each. All 33 bits of a block, including the lock bit, are programmed simultaneously.

Block 0 of page 0 contains the mode/configuration data, which is not transmitted during regular-read operations. Block 7 of page 0 may be used as a write protection password.

Bit 0 of every block is the lock bit for that block. Once locked, the block (including the lock bit itself) is not re-programmable through the RF field again.

Blocks 1 and 2 of page 1 contain traceability data and are transmitted with the modulation parameters defined in the configuration register after the opcode '11' is issued by the reader (see Figure 11 on page 9). These tracebility data blocks are programmed and locked by Atmel.

Figure 4. Memory Map

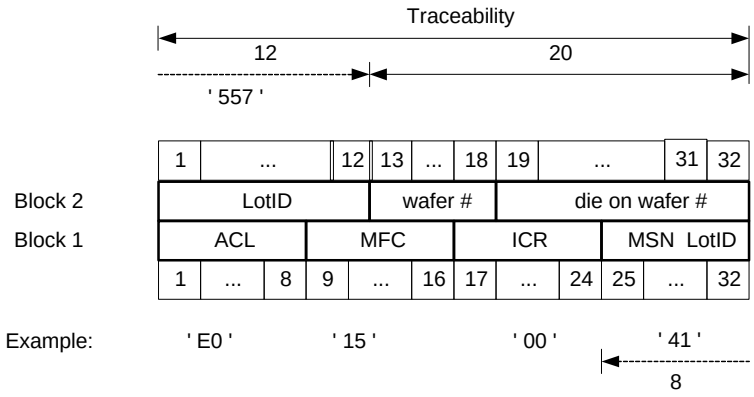


Traceability Data Structure

Blocks 1 and 2 of page 1 contain the traceability data and are programmed and locked by Atmel during production testing. The most significant byte of block 1 is fixed to ‘E0’hex, the allocation class (ACL) as defined in ISO/IEC 15963-1. The second byte is therefore defined as the manufacturer’s ID of Atmel (= ‘15’hex). The following 8 bits are used as IC reference byte (ICR - Bits 47 to 40). The 3 most significant bits define the IC and/or foundry version of the T5557. The lower 5 bits are by default reset (=00) as the Atmel standard value. Other values may be assigned on request to high volume customers as tag issuer identification.

The lower 40 bits of the data encode the traceability information of Atmel and conform to a unique numbering system. These 40 data bits are divided in two sub-groups, a 5-digit lot ID number, the binary wafer number (5 bit) concatenated with the sequential die number per wafer.

Figure 5. T5557 Traceability Data Structure



ACL Allocation class as defined in ISO/IEC 15963-1 = E0h
MFC Manufacturer code of Atmel Corporation as defined in ISO/IEC 7816-6 = 15h
ICR IC reference of silicon and/or tag manufacturer
Top 3 bits define IC revision
Lower 5 bits may contain a customer ID code on request
MSN Manufacturer serial number consists of:
LotID 5-digit lot number, e.g., ’38765’
DPW 20 bits encoded as sequential die per wafer number (with top 5 bits = wafer#)

Operating the T5557

Initialization and POR Delay

The Power-On-Reset (POR) circuit remains active until an adequate voltage threshold has been reached. This in turn triggers the default start-up delay sequence. During this configuration period of about 192 field clocks, the T5557 is initialized with the configuration data stored in EEPROM block 0. During initialization of the configuration block 0, all T55570x variants the load damping is active permanently (see Figure 10 on page 9). The T55571x types (without damping option) achieve a longer read range based on the lower activation field strength.

If the POR-delay bit is reset, no additional delay is observed after the configuration period. Tag modulation in regular-read mode will be observed about 3 ms after entering the RF field. If the POR delay bit is set, the T5557 remains in a permanent damping state until 8190 internal field clocks have elapsed.

$$T_{INIT} = (192 + 8190 \times \text{POR delay}) \times T_C \approx 67 \text{ ms} ; \quad T_C = 8 \text{ µs at } 125 \text{ kHz}$$

Any field gap occurring during this initialization phase will restart the complete sequence. After this initialization time the T5557 enters regular-read mode and modulation starts automatically using the parameters defined in the configuration register.

Tag to Reader Communication

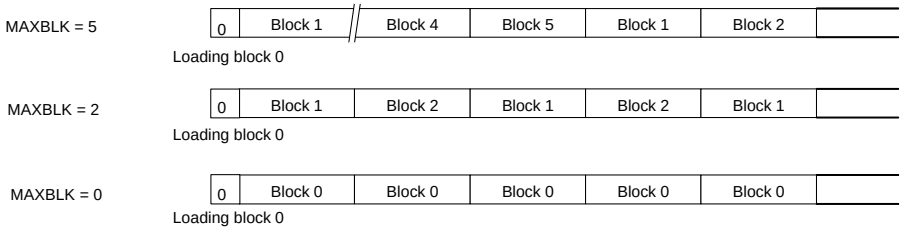
During normal operation, the data stored within the EEPROM is cycled and the Coil 1, Coil 2 terminals are load modulated. This resistive load modulation can be detected at the reader module.

Regular-read Mode

In regular-read mode data from the memory is transmitted serially, starting with block 1, bit 1, up to the last block (e.g., 7), bit 32. The last block which will be read is defined by the mode parameter field MAXBLK in EEPROM block 0. When the data block addressed by MAXBLK has been read, data transmission restarts with block 1, bit 1.

The user may limit the cyclic datastream in regular-read mode by setting the MAXBLK between 0 and 7 (representing each of the 8 data blocks). If set to 7, blocks 1 through 7 can be read. If set to 1, only block 1 is transmitted continously. If set to 0, the contents of the configuration block (normally not transmitted) can be read. In the case of MAXBLK = 0 or 1, regular-read mode can not be distinguished from block-read mode.

Figure 6. Examples for Different MAXBLK Settings



Every time the T5557 enters regular- or block-read mode, the first bit transmitted is a logical ‘0’. The data stream starts with block 1, bit 1, continues through MAXBLK, bit 32, and cycles continuously if in regular-read mode.

Note: This behavior is different from the original e555x and helps to decode PSK-modulated data.

Block-read Mode

With the direct access command, the addressed block is repetitively read only. This mode is called block-read mode. Direct access is entered by transmitting the page access opcode (‘10’ or ‘11’), a single ‘0’ bit and the requested 3-bit block address when the tag is in normal mode.

In password mode (PWD bit set), the direct access to a single block needs the valid 32-bit password to be transmitted after the page access opcode whereas a ‘0’ bit and the 3-bit block address follow afterwards. In case the transmitted password does not match with the contents of block 7, the T5557 tag returns to the regular-read mode.

Note: A direct access to block 0 of page 1 will read the configuration data of block 0, page 0. A direct access to bock 3 .. 7 of page 1 reads all data bits as zero.

e5550 Sequence Terminator

The sequence terminator ST is a special damping pattern which is inserted before the first block and may be used to synchronize the reader. This e5550-compatible sequence terminator consists of 4 bit periods with underlaying data values of ‘1’. During the second and the fourth bit period, modulation is switched off (Manchester encoding – switched on). Biphase modulated data blocks need fixed leading and trailing bits in combination with the sequence terminator to be identified reliable.

The sequence terminator may be individually enabled by setting of mode bit 29 (ST = ‘1’) in the e5550-compatibility mode (X-mode = ‘0’).

In the regular-read mode, the sequence terminator is inserted at the start of each MAXBLK-limited read data stream.

In block-read mode – after any block-write or direct access command – or if MAXBLK was set to 0 or 1, the sequence terminator is inserted before the transmission of the selected block.

Especially this behavior is different to former e5550 – compatible ICs (T5551, T5554).

Figure 7. Read Data Stream with Sequence Terminator

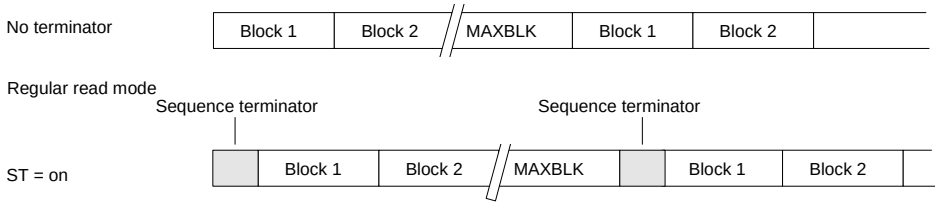
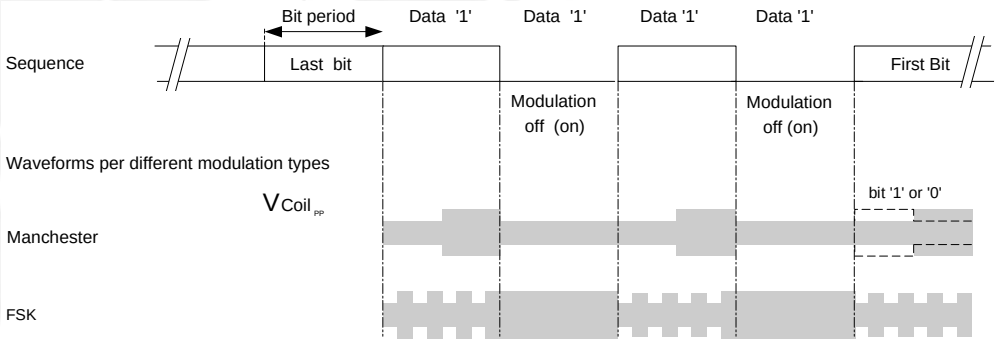


Figure 8. e5550-compatible Sequence Terminator Waveforms



Sequence terminator not suitable for Biphase or PSK modulation

Reader to Tag Communication

Data is written to the tag by interrupting the RF field with short field gaps (on-off keying) in accordance with the e5550 write method. The time between two gaps encodes the ‘0/1’ information to be transmitted (pulse interval encoding). The duration of the gaps is usually 50 µs to 150 µs. The time between two gaps is nominally 24 field clocks for a ‘0’ and 54 field clocks for a ‘1’. When there is no gap for more than 64 field clocks after a previous gap, the T5557 exits the write mode. The tag starts with the command execution if the correct number of bits were received. If there is a failure detected the T5557 does not continue and will enter regular-read mode.

Start Gap

The initial gap is referred to as the start gap. This triggers the reader to tag communication. During this mode of operation, the receive damping is permanently enabled to ease gap detection. The start gap may need to be longer than subsequent gaps in order to be detected reliably.

A start gap will be accepted at any time after the mode register has been loaded (≥ 3 ms). A single gap will not change the previously selected page (by former opcode ‘10’ or ‘11’).

Figure 9. Start of Reader to Tag Communication

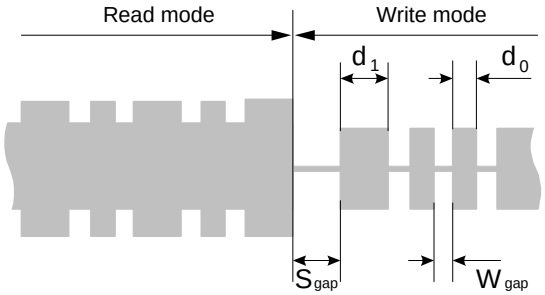


Table 2. Write Data Decoding Scheme

Parameters	Remark	Symbol	Min.	Max.	Unit
Start gap		S_{gap}	10	50	FC
Write gap	Normal write mode	W_{gap}	8	30	FC
Write data in normal mode	‘0’ data	d_0	16	31	FC
	‘1’ data	d_1	48	63	FC

Write Data Protocol

The T5557 expects to receive a dual bit opcode as the first two bits of a reader command sequence. There are three valid opcodes:

- The opcodes ‘10’ and ‘11’ precede all block write and direct access operations for page 0 and page 1
- The RESET opcode ‘00’ initiates a POR cycle
- The opcode ‘01’ precedes all test mode write operations. Any test mode access is ignored after master key (bits 1..4) in block 0 has been set to ‘6’. Any further modifications of the master key are prohibited by setting the lock bit of block 0 or the OTP bit.

Writing has to follow these rules:

- Standard write needs the opcode, the lock bit, 32 data bits and the 3-bit address (38 bits total)
- Protected write (PWD bit set) requires a valid 32-bit password between opcode and data, address bits
- For the AOR wake-up command an opcode and a valid password are necessary to select and activate a specific tag

Note: The data bits are read in the same order as written.

If the transmitted command sequence is invalid, the T5557 enters regular-read mode with the previously selected page (by former opcode ‘10’ or ‘11’).

Figure 10. Complete Writing Sequence

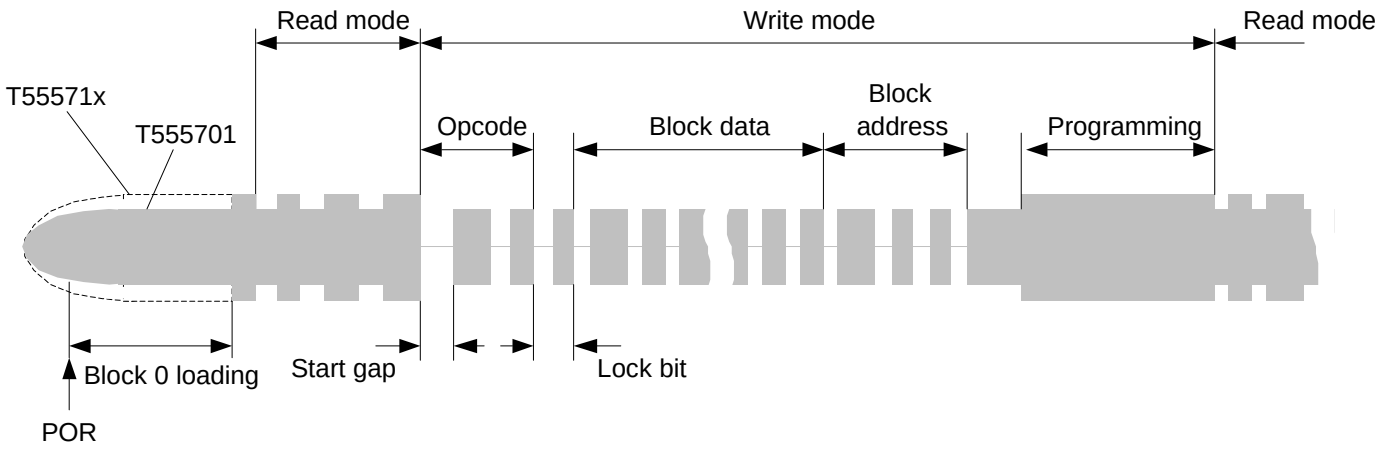
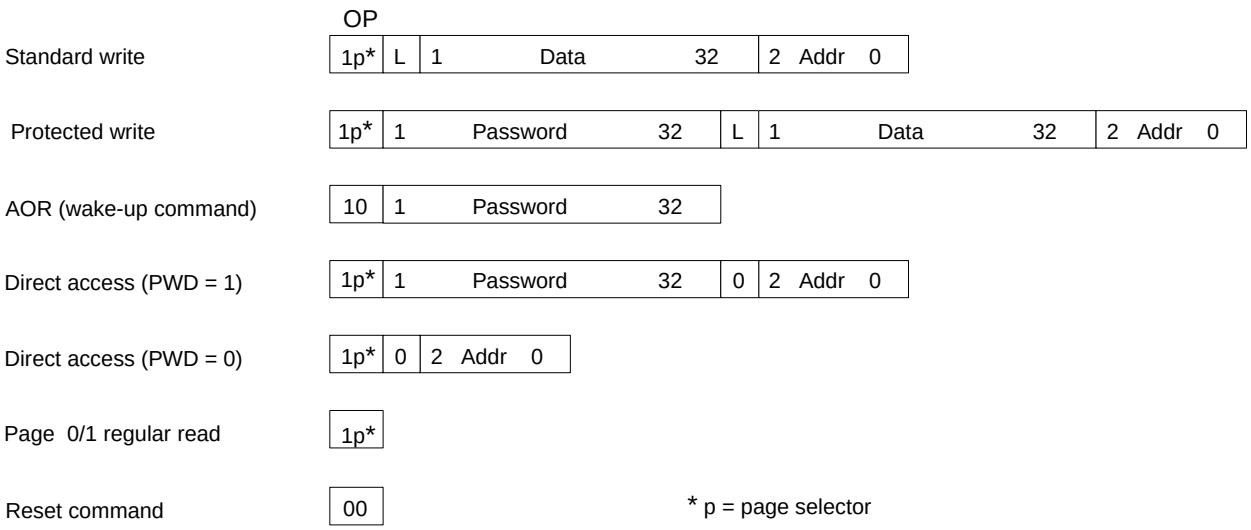


Figure 11. T5557 Command Formats



Password

When password mode is active (PWD = 1), the first 32 bits after the opcode are regarded as the password. They are compared bit by bit with the contents of block 7, starting at bit 1. If the comparison fails, the T5557 will not program the memory, instead it will restart in regular-read mode once the command transmission is finished.

Note: In password mode, MAXBLK should be set to a value below 7 to prevent the password from being transmitted by the T5557.

Each transmission of the direct access command (two opcode bits, 32 bits password, ‘0’ bit plus 3 address bits = 38 bits) needs about 18 ms. Testing all possible combinations (about 4.3 billion) takes about two years.

Answer-On-Request (AOR) Mode

When the AOR bit is set, the T5557 does not start modulation in the regular-read mode after loading configuration block 0. The tag waits for a valid AOR data stream (“wake-up command”) from the reader before modulation is enabled. The wake-up command consists of the opcode (‘10‘) followed by a valid password. The selected tag will remain active until the RF field is turned off or a new command with a different password is transmitted which may address another tag in the RF field.

Table 3. T5557 — Modes of Operation

PWD	AOR	Behavior of Tag after Reset Command or POR	De-activate Function
1	1	Answer-On-Request (AOR) mode: • Modulation starts after wake-up with a matching password • Programming needs valid password	Command with non-matching password deactivates the selected tag
1	0	Password mode: • Modulation in regular-read mode starts after reset • Programming and direct access needs valid password	
0	--	Normal mode: • Modulation in regular-read mode starts after reset • Programming and direct access without password	

Figure 12. Answer-On-Request (AOR) Mode

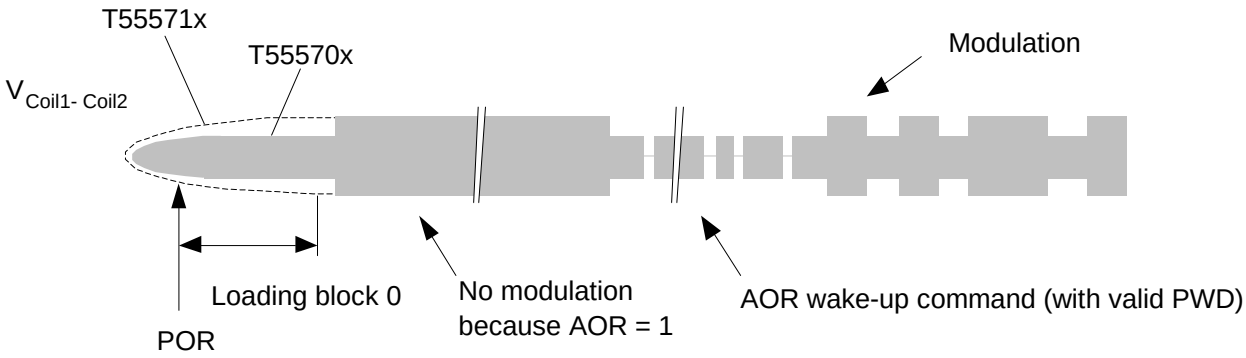


Figure 13. Coil Voltage after Programming of a Memory Block

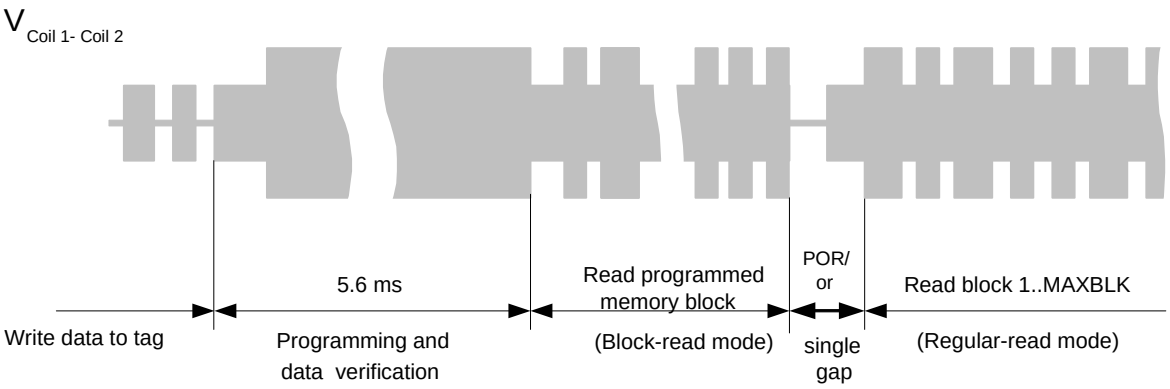
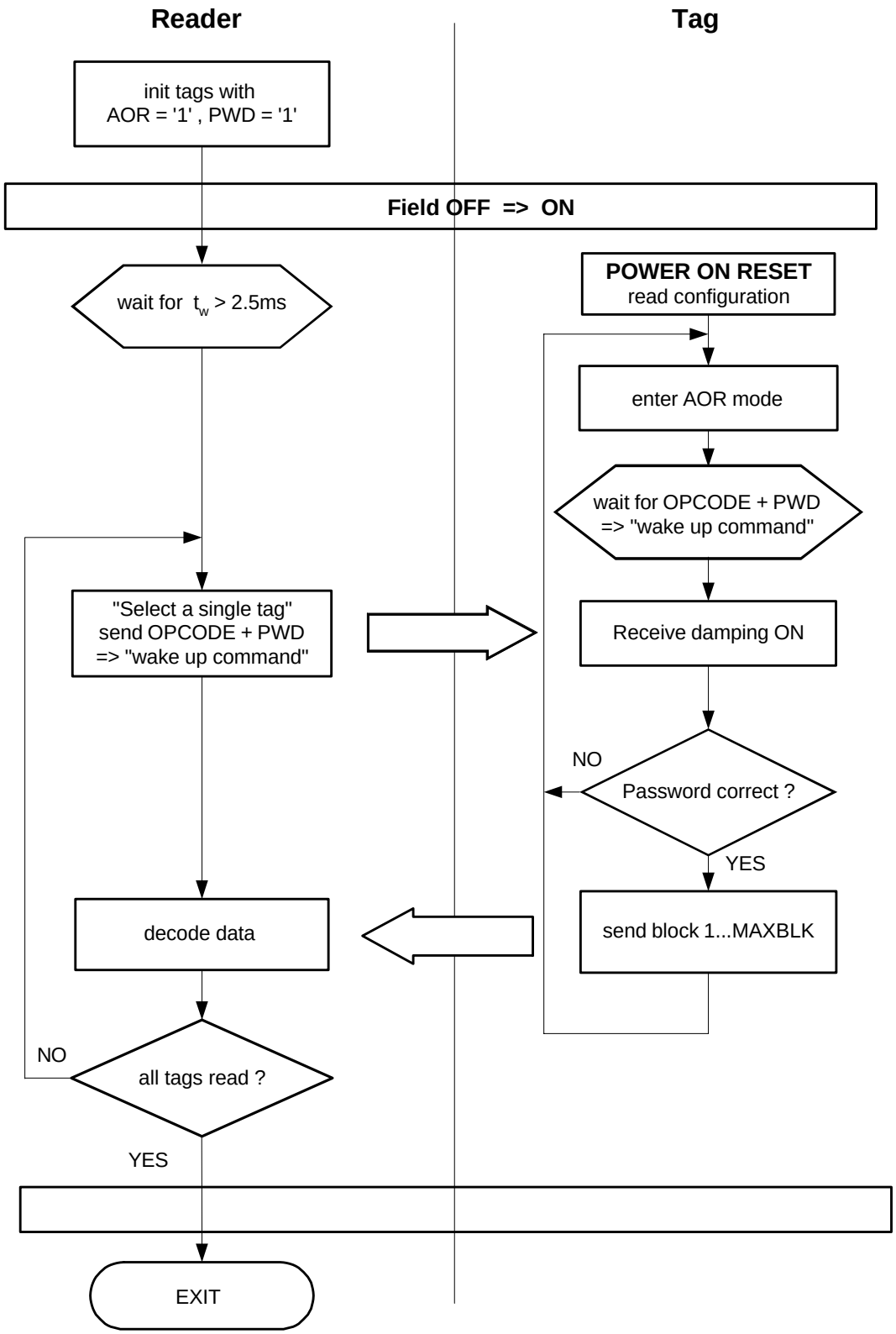


Figure 14. Anticollision Procedure Using AOR Mode



Programming

When all necessary information has been received by the T5557, programming may proceed. There is a clock delay between the end of the writing sequence and the start of programming.

Typical programming time is 5.6 ms. This cycle includes a data verification read to grant secure and correct programming. After programming was executed successfully, the T5557 enters block-read mode transmitting the block just programmed (see Figure 13 on page 10).

Note: This timing and behavior is different from the e555x-family predecessors.

Error Handling

Several error conditions can be detected to ensure that only valid bits are programmed into the EEPROM. There are two error types, which lead to two different actions.

Errors During Writing

The following detectable errors could occur during writing data into the T5557:

- Wrong number of field clocks between two gaps (i.e., not a valid ‘1’ or ‘0’ pulse stream)
- Password mode is activated and the password does not match the contents of block 7
- The number of bits received in the command sequence is incorrect

Valid bit counts accepted by the T5557 are:

Password write	70 bits	(PWD = 1)
Standard write	38 bits	(PWD = 0)
AOR wake up	34 bits	(PWD = 1)
Direct access with PWD	38 bits	(PWD = 1)
Direct access	6 bits	(PWD = 0)
Reset command	2 bits	
Page 0/1 regular-read	2 bits	

If any of these erroneous conditions were detected, the T5557 enters regular-read mode, starting with block 1 of the page defined in the command sequence.

Errors Before/During Programming

If the command sequence was received successfully, the following error could still prevent programming:

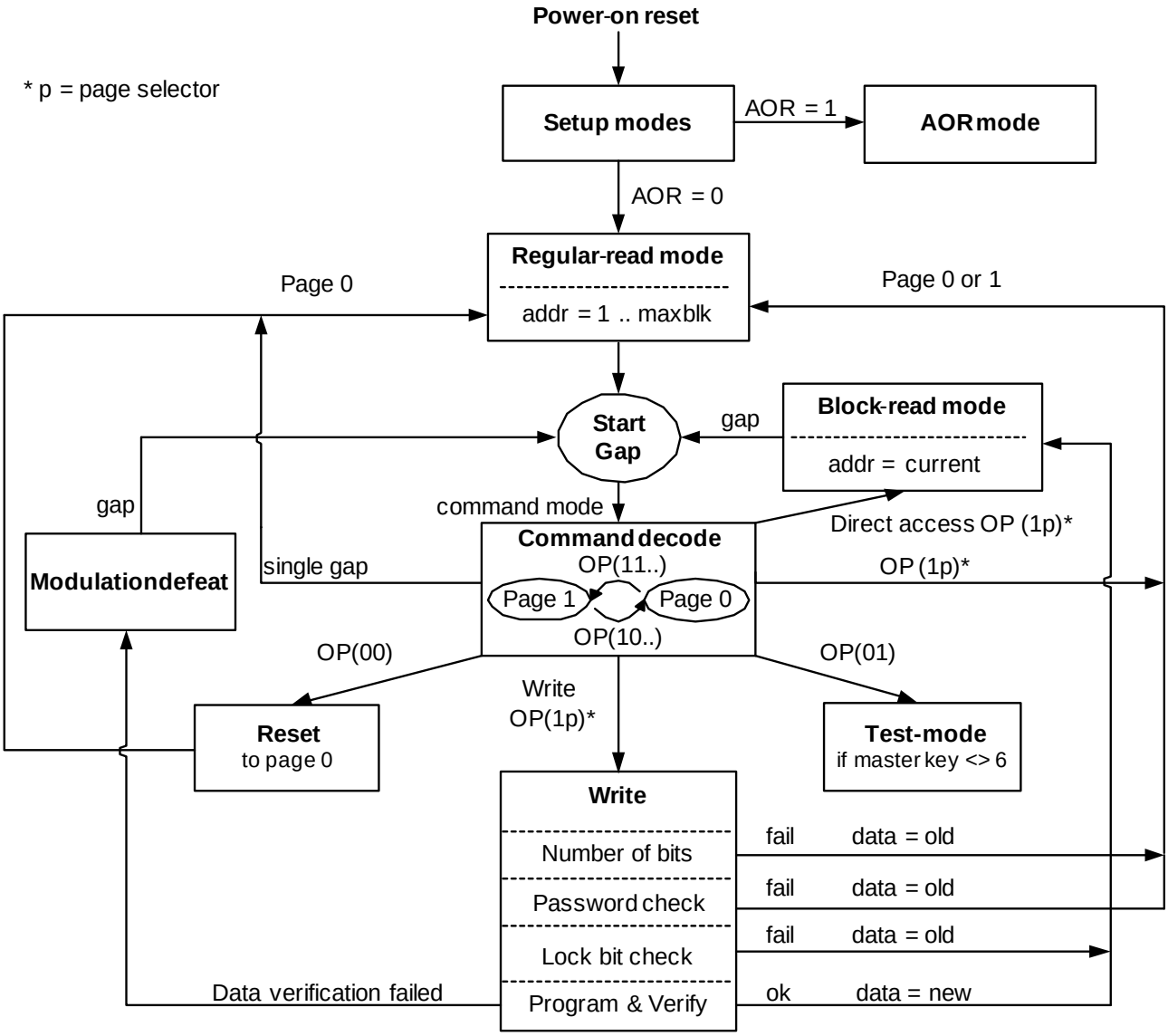
- The lock bit of the addressed block is set already
- In case of a locked block, programming mode will not be entered. The T5557 reverts to block-read mode continuously transmitting the currently addressed block.

If the command sequence is validated and the addressed block is not write protected, the new data will be programmed into the EEPROM memory. The new state of the block write protection bit (lock bit) will be programmed at the same time accordingly.

Each programming cycle consists of 4 consecutive steps: erase block, erase verification (data = ‘0’), programming, write verification (corresponding data bits = ‘1’).

- If a data verification error is detected after an executed data block programming, the tag will stop modulation (modulation defeat) until a new command is transmitted.

Figure 15. T5557 Functional Diagram



T5557 in Extended Mode (X-mode)

In general, the block 0 setting of the master key (bits 1 to 4) to the value ‘6’ or ‘9’ together with the X-mode bit will enable the extended mode functions.

- Master key = ‘9’: Test mode access and extended mode are both enabled.
- Master key = ‘6’: Any test mode access will be denied but the extended mode is still enabled.

Any other master key setting will prevent the activation of the T5557 extended mode options, even when the X-mode bit is set.

Binary Bit-rate Generator

In extended mode the data rate is binary programmable to operate at any data rate between RF/2 and RF/128 as given in the formula below.

Data rate = RF/(2n+2)

OTP Functionality

If the OTP bit is set to ‘1’, all memory blocks are write protected and behave as if all lock bits are set to 1. If the master key is set to ‘6’ additionally, the T5557 mode of operation is locked forever (= OTP functionality).

If the master key is set to ‘9’, the test-mode access allows the re-configuration of the tag again.

Figure 16. Block 0 — Configuration Map in Extended Mode (X-mode)

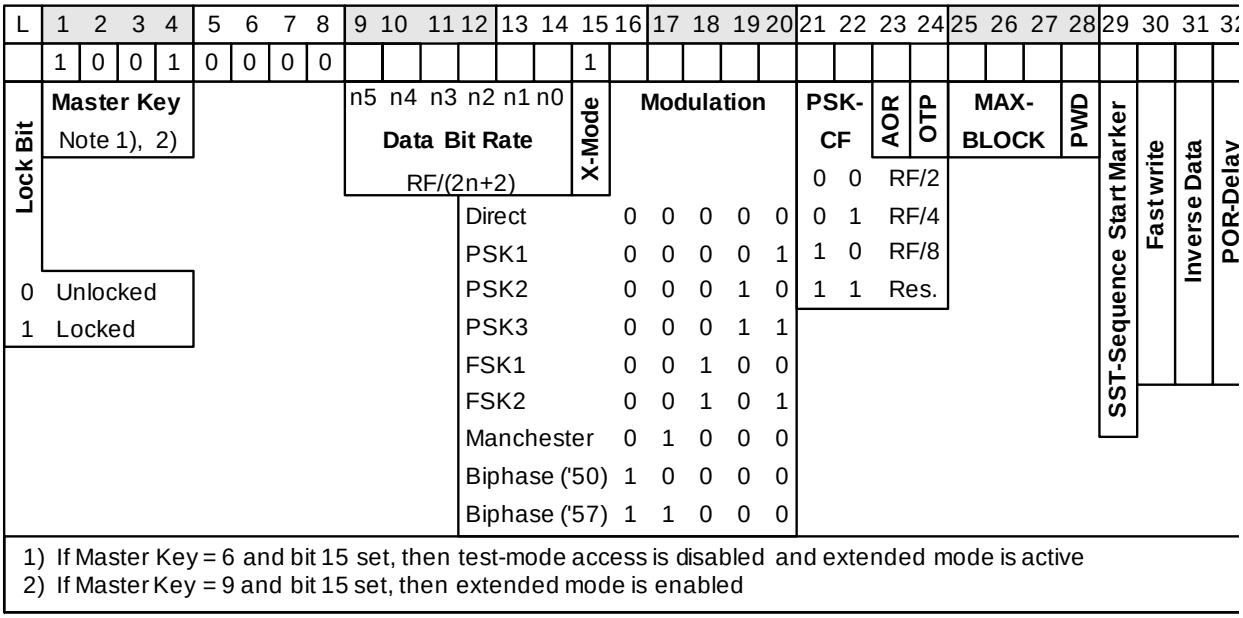


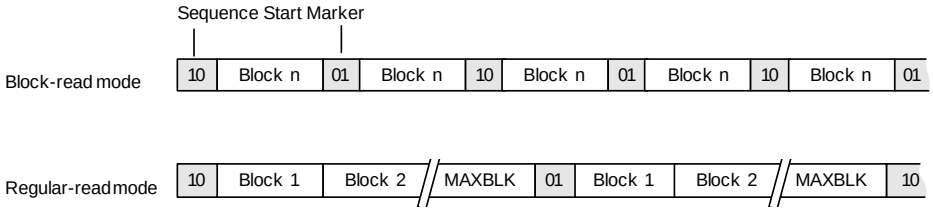
Table 4. T5557 Types of Modulation in Extended Mode

Mode	Direct Data Output Encoding	Inverse Data Output Encoding
FSK1[1]	FSK/5-/8 ‘0’ = RF/5; ‘1’ = RF/8	FSK/8-/5 ‘0’ = RF/8; ‘1’ = RF/5 (= FSK1a)
FSK2[1]	FSK/10-/8 ‘0’ = RF/10; ‘1’ = RF/8	FSK/8-/10 ‘0’ = RF/8; ‘1’ = RF/10 (= FSK2a)
PSK1[2]	Phase change when input changes	Phase change when input changes
PSK2[2]	Phase change on bit clock if input high	Phase change on bit clock if input low
PSK3[2]	Phase change on rising edge of input	Phase change on falling edge of input
Manchester	‘0’ = falling edge, ‘1’= rising edge on mid-bit	‘1’ = falling edge, ‘1’= rising edge on mid-bit
Biphase 1 (’50)	‘1’ creates an additional mid-bit change	‘0’ creates an additional mid-bit change
Biphase 2 (’57)	‘0’ creates an additional mid-bit change	‘1’ creates an additional mid-bit change
NRZ	‘1’= damping on, ‘0’= damping off	‘0’= damping on, ‘1’= damping off

Notes: 1. A common multiple of bitrate and FSK frequencies is recommended.
2. In PSK mode the selected data rate has to be an integer multiple of the PSK sub-carrier frequency.

Sequence Start Marker

Figure 17. T5557 Sequence Start Marker in Extended Mode

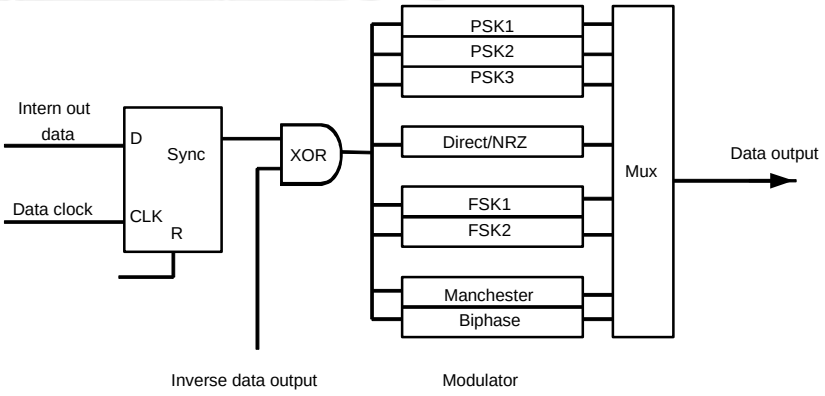


The T5557 sequence start marker is a special damping pattern, which may be used to synchronize the reader. The sequence start marker consists of two bits (‘01’ or ‘10’) which are inserted as header before the first block to be transmitted if the bit 29 in extended mode ist set. At the start of a new block sequence, the value of the two bits is inverted.

Inverse Data Output

The T5557 supports in its extended mode (X-mode) an inverse data output option. If inverse data is enabled, the modulator as shown in Figure 18 works on inverted data (see Table 4 on page 14). This function is supported for all basic types of encoding.

Figure 18. Data Encoder for Inverse Data Output



Fast Write

In the optional fast write mode the time between two gaps is nominally 12 field clocks for a ‘0’ and 27 field clocks for a ‘1’. When there is no gap for more than 32 field clocks after a previous gap, the T5557 will exit the write mode. Please refer to Table 5 and Figure 8 on page 7.

Table 5. Fast Write Data Decoding Schemes

Parameters	Remark	Symbol	Min.	Max.	Unit
Start gap	–	S_{gap}	10	50	FC
Write gap	Normal write mode	Wn_{gap}	8	30	FC
	Fast write mode	Wf_{gap}	8	20	FC
Write data in normal mode	‘0’ data	d_0	16	31	FC
	‘1’ data	d_1	48	63	FC
Write data in fast mode	‘0’ data	d_0	8	15	FC
	‘1’ data	d_1	24	31	FC

Figure 19. Example of Manchester Coding with Data Rate RF/16

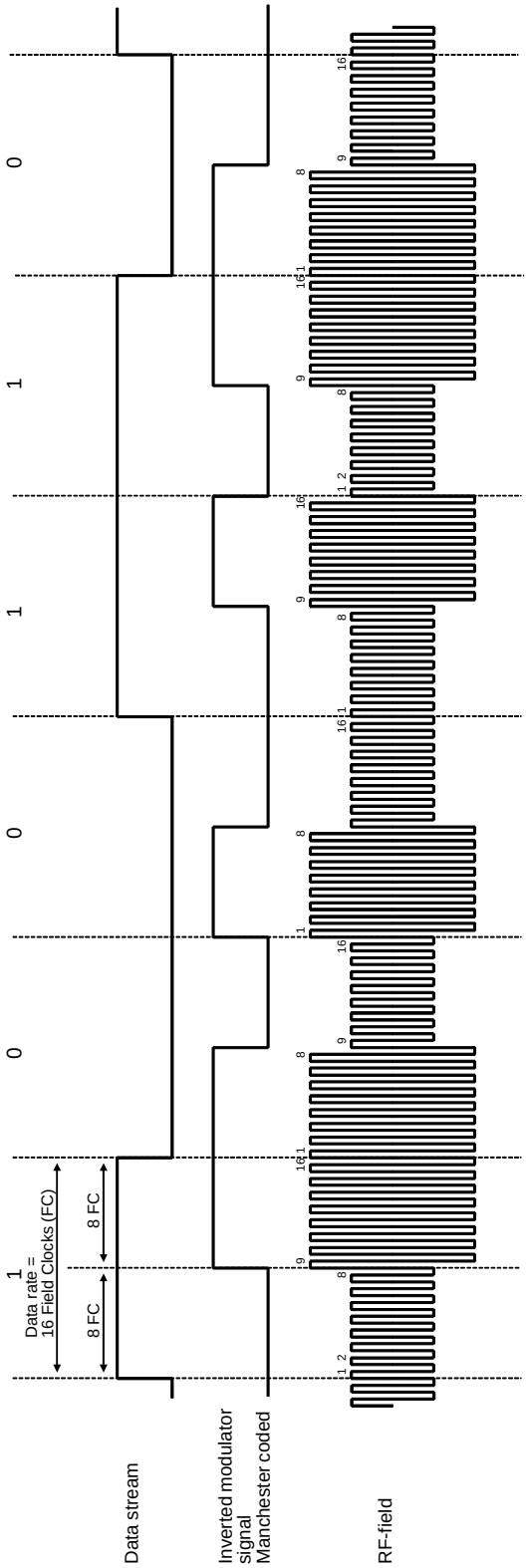


Figure 20. Example of Biphase Coding with Data Rate RF/16

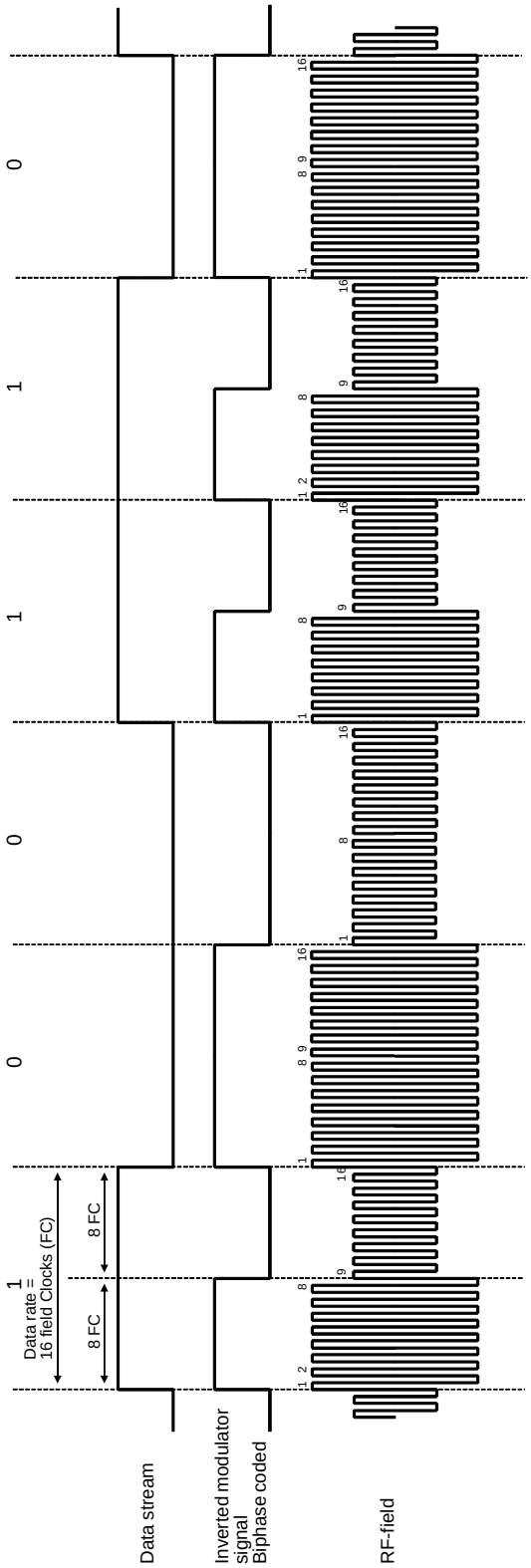


Figure 21. Example: FSK1a Coding with Data Rate RF/40, Subcarrier f_0 = RF/8, f_1 = RF/5

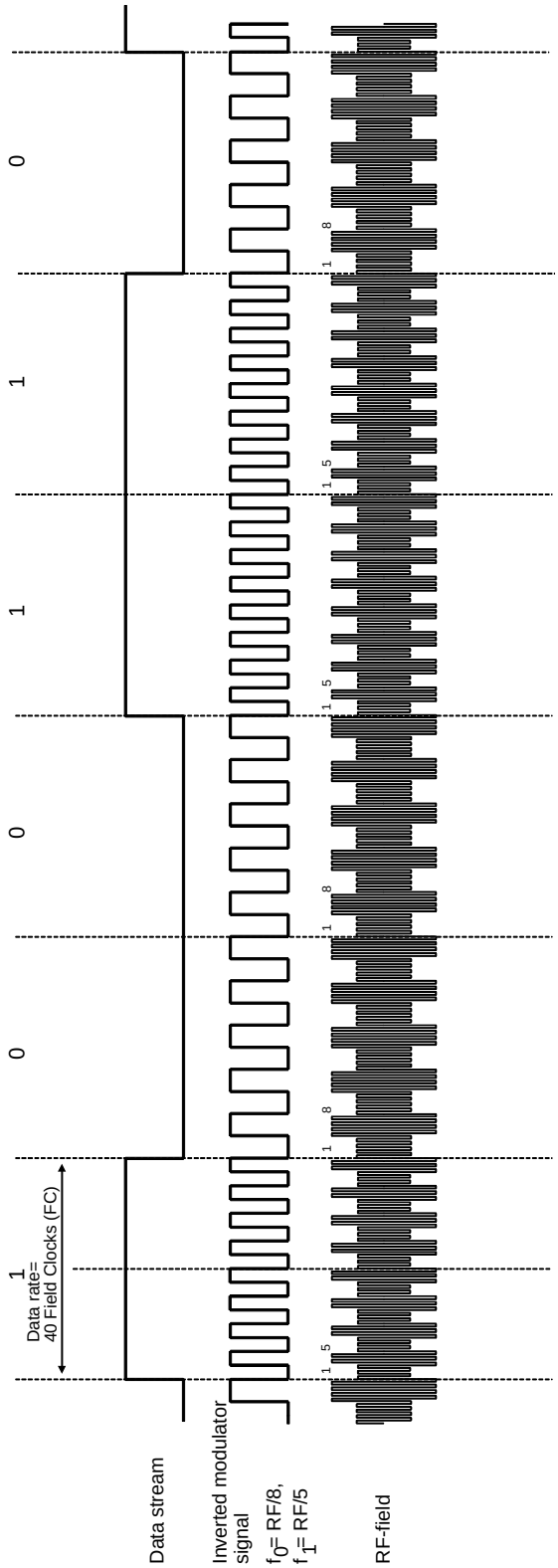


Figure 22. Example of PSK1 Coding with Data Rate RF/16

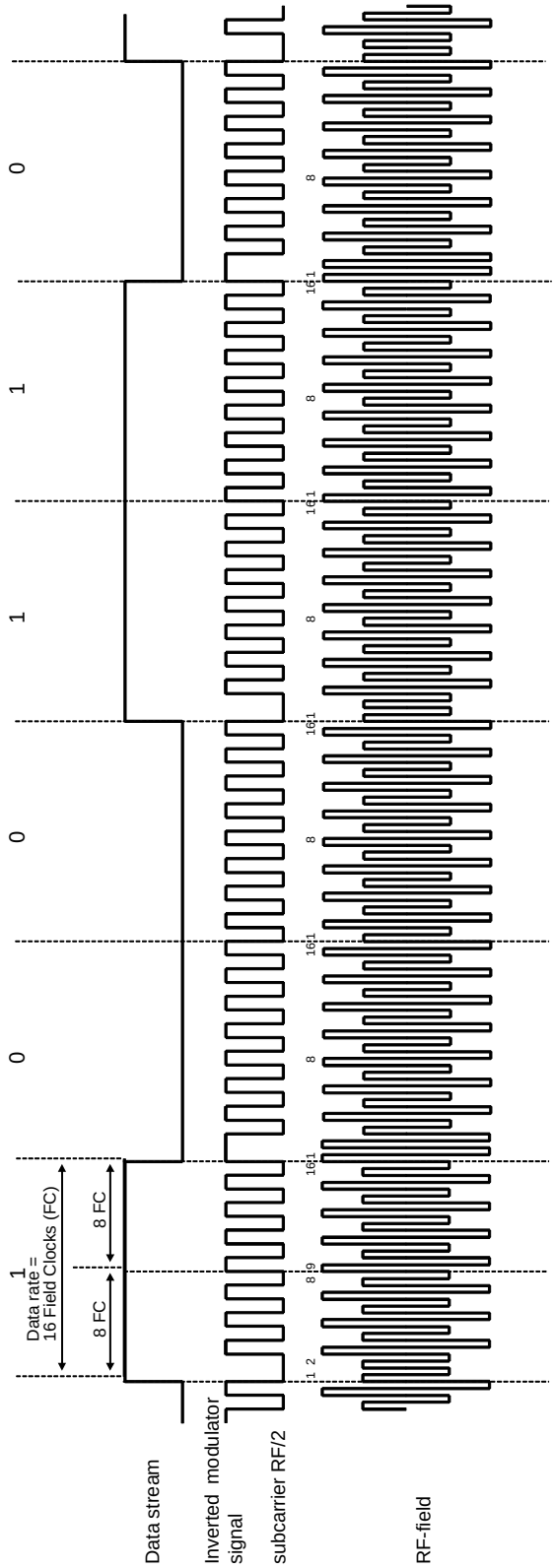


Figure 23. Example of PSK2 Coding with Data Rate RF/16

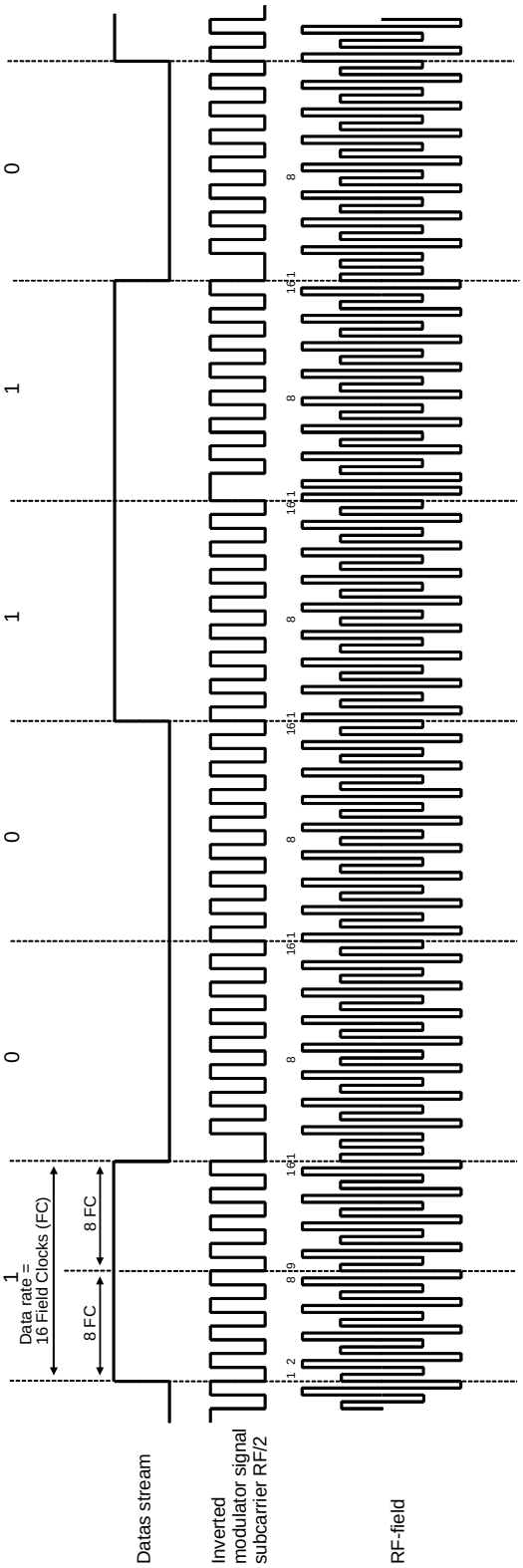
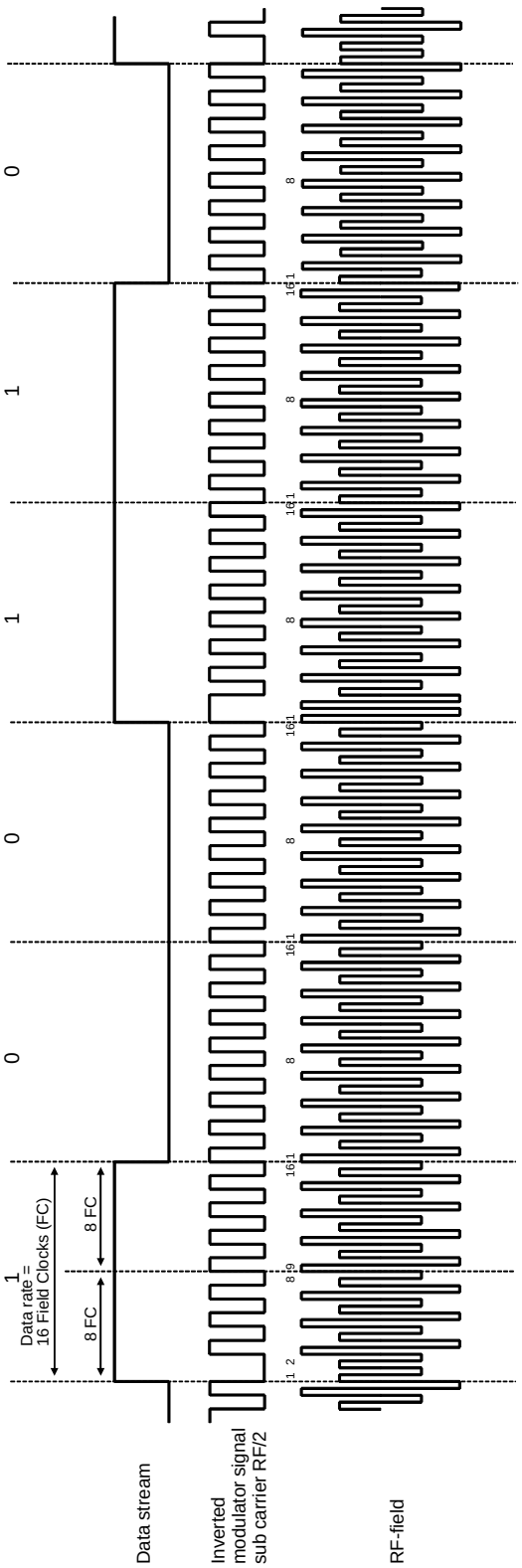


Figure 24. Example of PSK3 Coding with Data Rate RF/16



Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Maximum DC current into Coil 1/Coil 2	I_{coil}	20	mA
Maximum AC current into Coil 1/Coil 2 f = 125 kHz	$I_{coil\ p}$	20	mA
Power dissipation (dice) (free-air condition, time of application: 1 s)	P_{tot}	100	mW
Electrostatic discharge maximum to MIL-Standard 883 C method 3015	V_{max}	4000	V
Operating ambient temperature range	T_{amb}	-40 to +85	°C
Storage temperature range (data retention reduced)	T_{stg}	-40 to +150	°C

Electrical Characteristics

T_{amb} = +25° C; f_{coil} = 125 kHz; unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	Type*
1	RF frequency range		f_{RF}	100	125	150	kHz	
2.1	Supply current (without current consumed by the external LC tank circuit)	T_{amb} = 25° C(1) (see Figure 24 on page 18)	I_{DD}		1.5	3	µA	T
2.2		Read – full temperature range			2	4	µA	Q
2.3		Programming full temperature range			25	40	µA	Q
3.1	Coil voltage (AC supply)	POR threshold (50 mV hysteresis)	$V_{coil\ pp}$	3.2	3.6	4.0	V	Q
3.2		Read mode and write command(2)		6		V_{clamp}	V	Q
3.3		Program EEPROM (2)		8		V_{clamp}	V	Q
4	Start-up time	$V_{coil\ pp}$ = 6 V	$t_{startup}$		2.5	3	ms	Q
5	Clamp voltage	10 mA current into Coil 1/2	V_{clamp}	17		23	V	T

*) Type means: T: directly or indirectly tested during production; Q: guaranteed based on initial product qualification data

Notes:
1. I_{DD} measurement setup R = 100 k; V_{CLK} = V_{coil} = 5 V: EEPROM programmed to 00 ... 000 (erase all); chip in modulation defeat. I_{DD} = (V_{OUTmax} - V_{CLK})/R
2. Current into Coil 1/Coil 2 is limited to 10 mA. The damping circuitry has the same structure as the e5550. The damping characteristics are defined by the internally limited supply voltage (= minimum AC coil voltage)
3. V_{mod} measurement setup: R = 2.3 k; V_{CLK} = 3 V; setup with modulation enabled (see Figure 25 on page 20).
4. Since EEPROM performance is influenced by assembly processes, Atmel confirms the parameters for DOW (tested dice on uncutted wafer) delivery.
5. The tolerance of the on-chip resonance capacitor C_r is ±10% at 3σ over whole production. The capacitor tolerance is ±3% at 3σ on a wafer basis.
6. The tolerance of the microcodule resonance capacitor C_r is ±5% at 3σ over whole production.

Electrical Characteristics

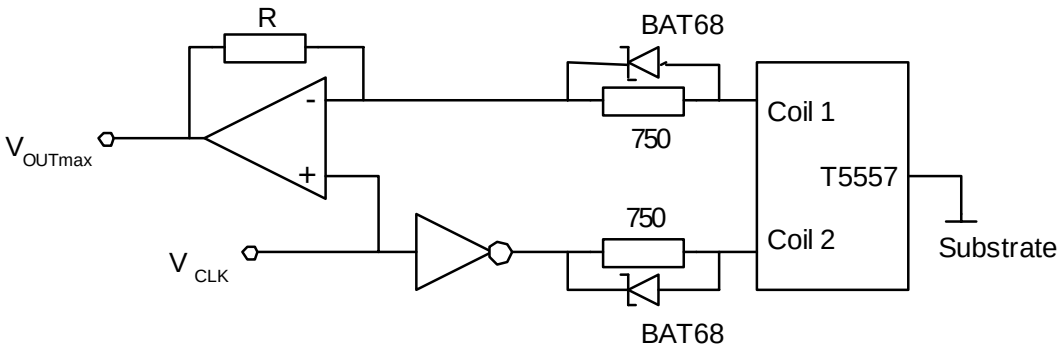
T_{amb} = +25° C; f_{coil} = 125 kHz; unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	Type*
6.1	Modulation parameters	V_{coilpp} = 6 V on test circuit generator and modulation ON(3)	$V_{mod\ pp}$		4.2	4.8	V	T
6.2			$I_{mod\ pp}$	400	600		µA	T
6.3		Thermal stability	V_{mod}/T_{amb}		-6		mV/° C	Q
7	Programming time	From last command gap to re-enter read mode (64 + 648 internal clocks)	T_{prog}	5	5.7	6	ms	T
8	Endurance	Erase all / Write all(4)	n_{cycle}	100000			Cycles	Q
9.1	Data retention	Top = 55° C(4)	$t_{retention}$	10	20	50	Years	
9.2		Top = 150° C(4)	$t_{retention}$	96			hrs	T
9.3		Top = 250° C(4)	$t_{retention}$	24			hrs	Q
10	Resonance capacitor	Mask option(5)	C_r	70	78	86	pF	T
11.1	Microdule capacitor parameters	Capacitance tolerance T_{amb}	C_r	313.5	330	346.5	pF	T
11.2		Temperature coefficient	TBD	TBD	TBD	TBD	TBD	TBD
11.3			TBD	TBD	TBD	TBD	TBD	TBD

*) Type means: T: directly or indirectly tested during production; Q: guaranteed based on initial product qualification data

Notes:
1. I_{DD} measurement setup R = 100 k; $V_{CLK} = V_{coil}$ = 5 V: EEPROM programmed to 00 ... 000 (erase all); chip in modulation defeat. $I_{DD} = (V_{OUTmax} - V_{CLK})/R$
2. Current into Coil 1/Coil 2 is limited to 10 mA. The damping circuitry has the same structure as the e5550. The damping characteristics are defined by the internally limited supply voltage (= minimum AC coil voltage)
3. V_{mod} measurement setup: R = 2.3 k; V_{CLK} = 3 V; setup with modulation enabled (see Figure 25 on page 20).
4. Since EEPROM performance is influenced by assembly processes, Atmel confirms the parameters for DOW (tested dice on uncutted wafer) delivery.
5. The tolerance of the on-chip resonance capacitor C_r is ±10% at 3σ over whole production. The capacitor tolerance is ±3% at 3σ on a wafer basis.
6. The tolerance of the microcodule resonance capacitor C_r is ±5% at 3σ over whole production.

Figure 25. Measurement Setup for I_{DD} and V_{mod}



Ordering Information[2]

T 5 5 5 7	a b	M c c	- x x x	Package		Drawing
				- DDW	- Dice on wafer, 6” un-sawn wafer, thickness 300 µm	
				- DDT	- Dice in tray (waffle pack), thickness 300 µm	
				- DBW	- Dice on solder bumped wafer, thickness 390 µm Sn63Pb37 on 5 µm Ni/Au, height 70 µm	Figure 27 on page 23 Figure 28 on page 23
				- TAS	- SO8 package	Figure 31 on page 26
				- PAE	- MOA2 mocro-module	Figure 29 on page 24
				Customer ID[1]		
					- Atmel standard (corresponds to “0”)	
				M01	- Customer “X” unique ID code[1]	
				11	- 2 pads withput on-chip C	Figure 26 on page 22
				14	- 4 pads with on-chip 75 pF	Figure 27 on page 23
				15	- Micro-module with 330 pF	Figure 29 on page 24
				01	- 2 pads without C, damping during initialization	Figure 26 on page 22

Notes: 1. Unique customer ID code programming according to Figure 5 is linked to a minimum order quantity of 1 Mio parts per year.
2. For available order codes refer to Atmel Sales/Marketing.

Ordering Examples (Recommended)

T555711-DDW — Tested dice on unsawn 6” wafer, thickness 300 µm, no on-chip capacitor, no damping during POR initialisation; especially for ISO 11784/785 and access control applications

Available Order Codes

T555711-DDW, DDT, TAS
T555714-DDW, DBW, TAS
T555715-PAE

New order codes will be done on customer request if order quantities are upside 250k pieces.

Figure 26. 2 Pad Layout for Wire Bonding

Dimensions in µm

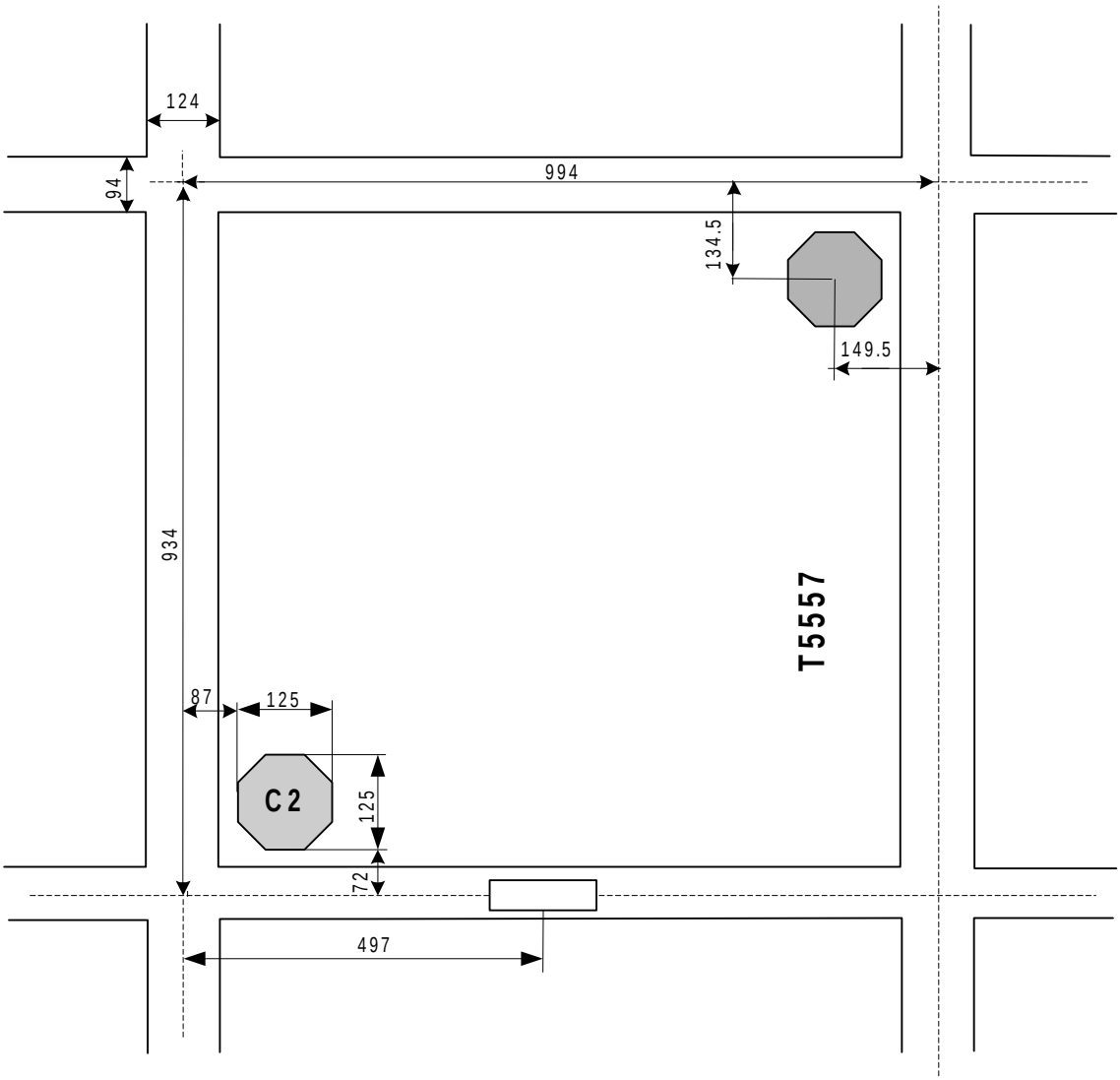


Figure 27. 4 Pad Flip-chip Version with 70 µm Solder Bumps

Dimensions in µm

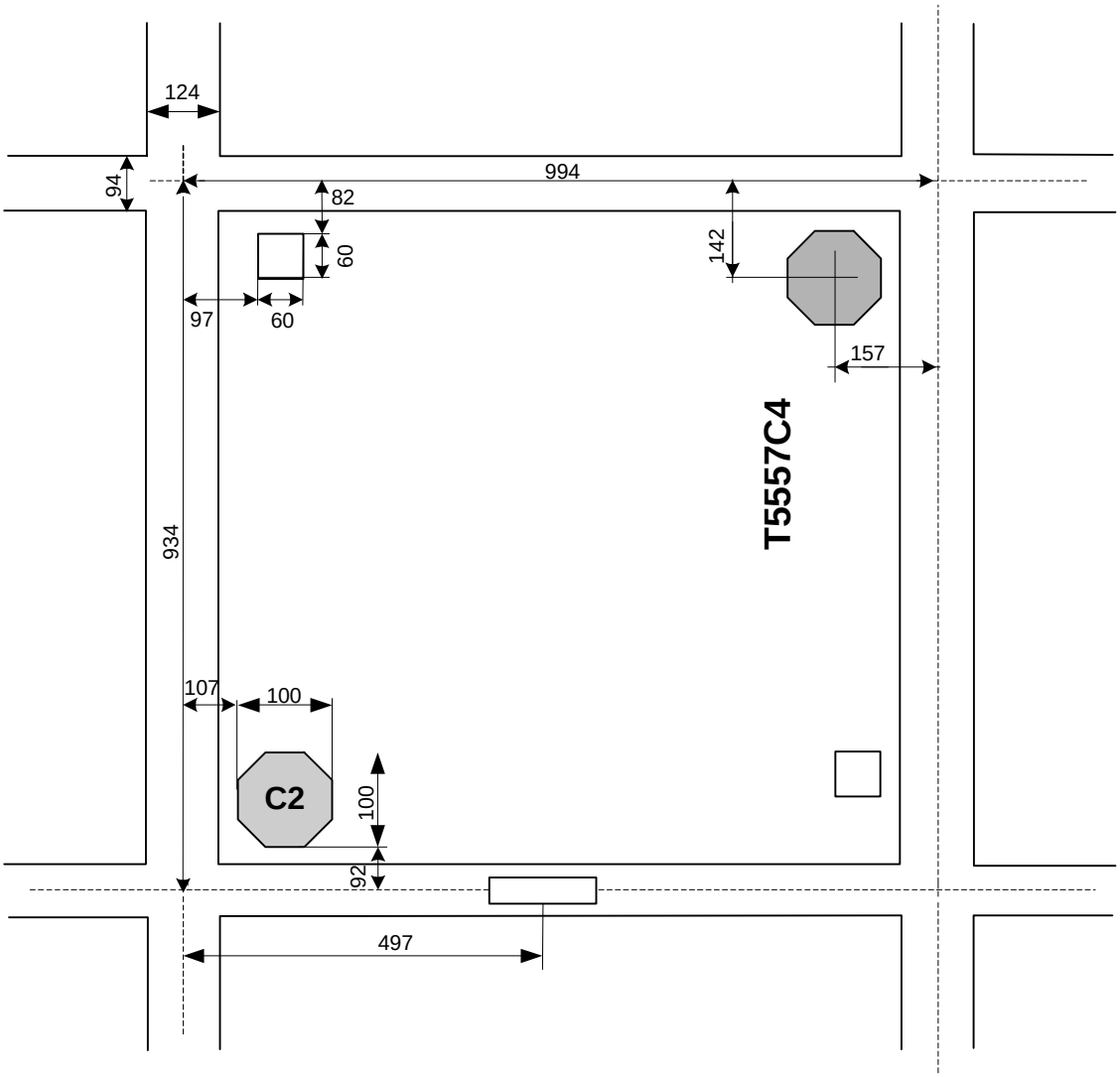


Figure 28. Solder bump on NiAu

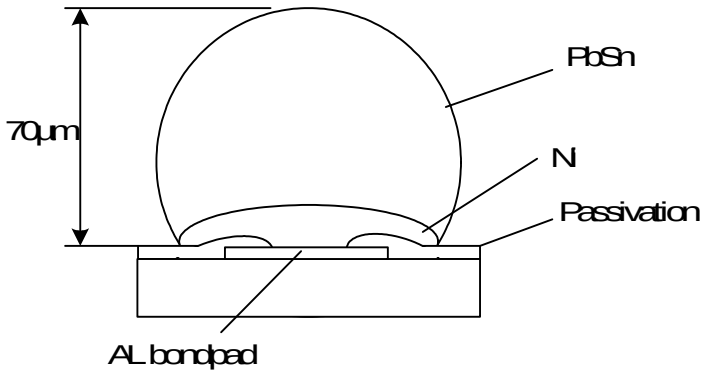
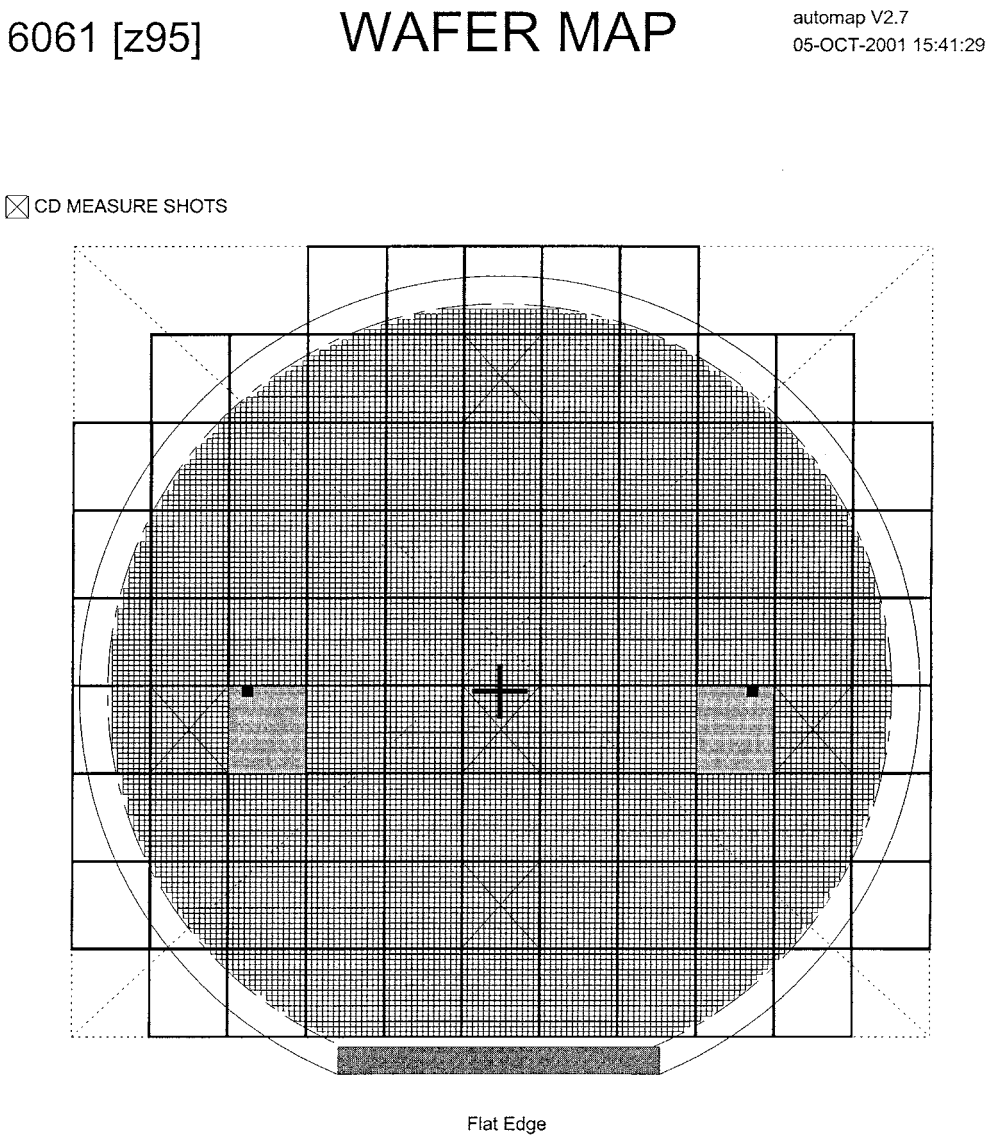


Figure 29. Wafer Map



Failed Die Identification

Every die on the wafer not passing Atmel test sequence is marked with inch. The inch dot specification:

- Dot size: 200 µm
- Position: center of die
- Color: black

Figure 30. NOA2 Micromodule

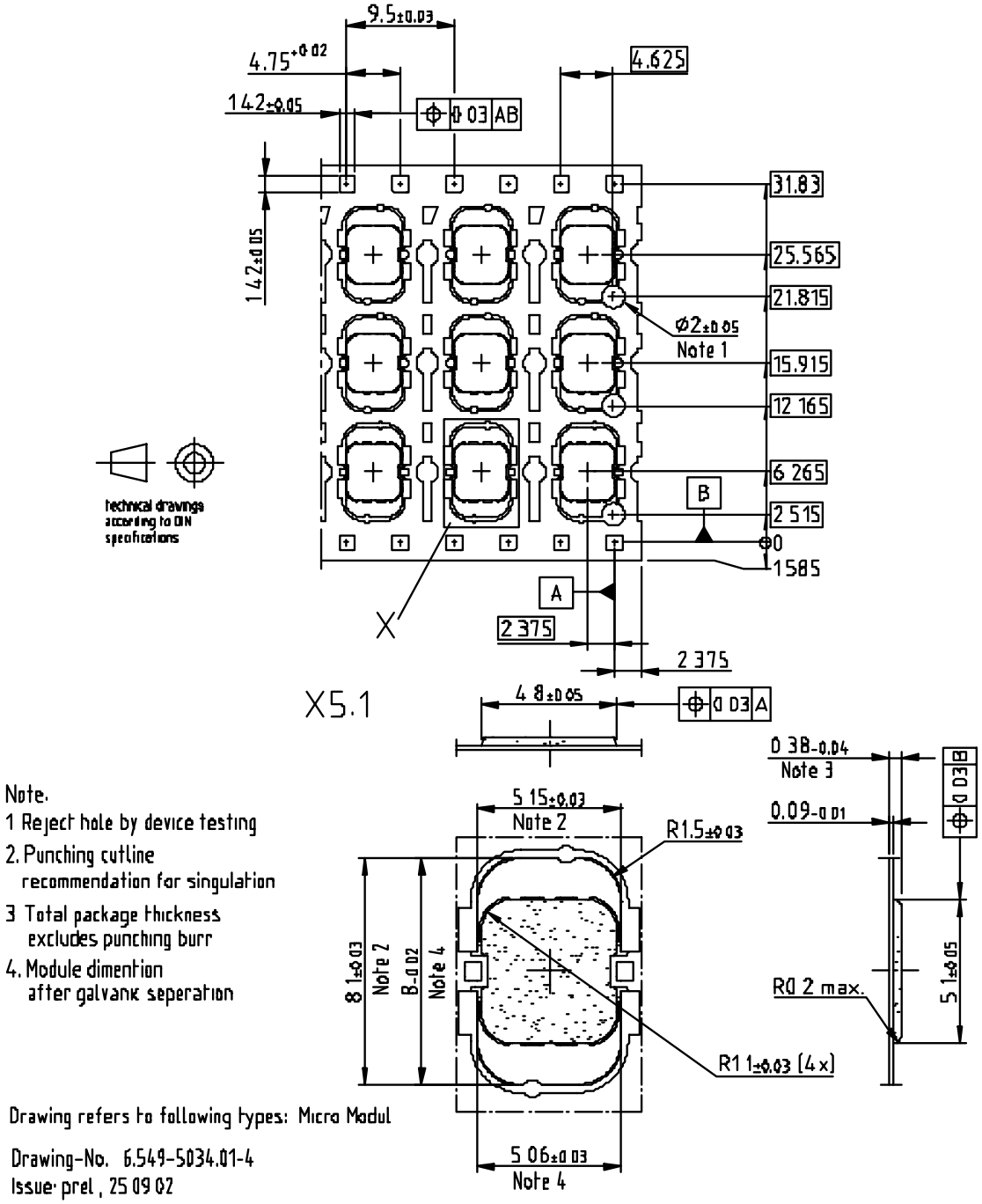


Figure 31. Shipping Reel

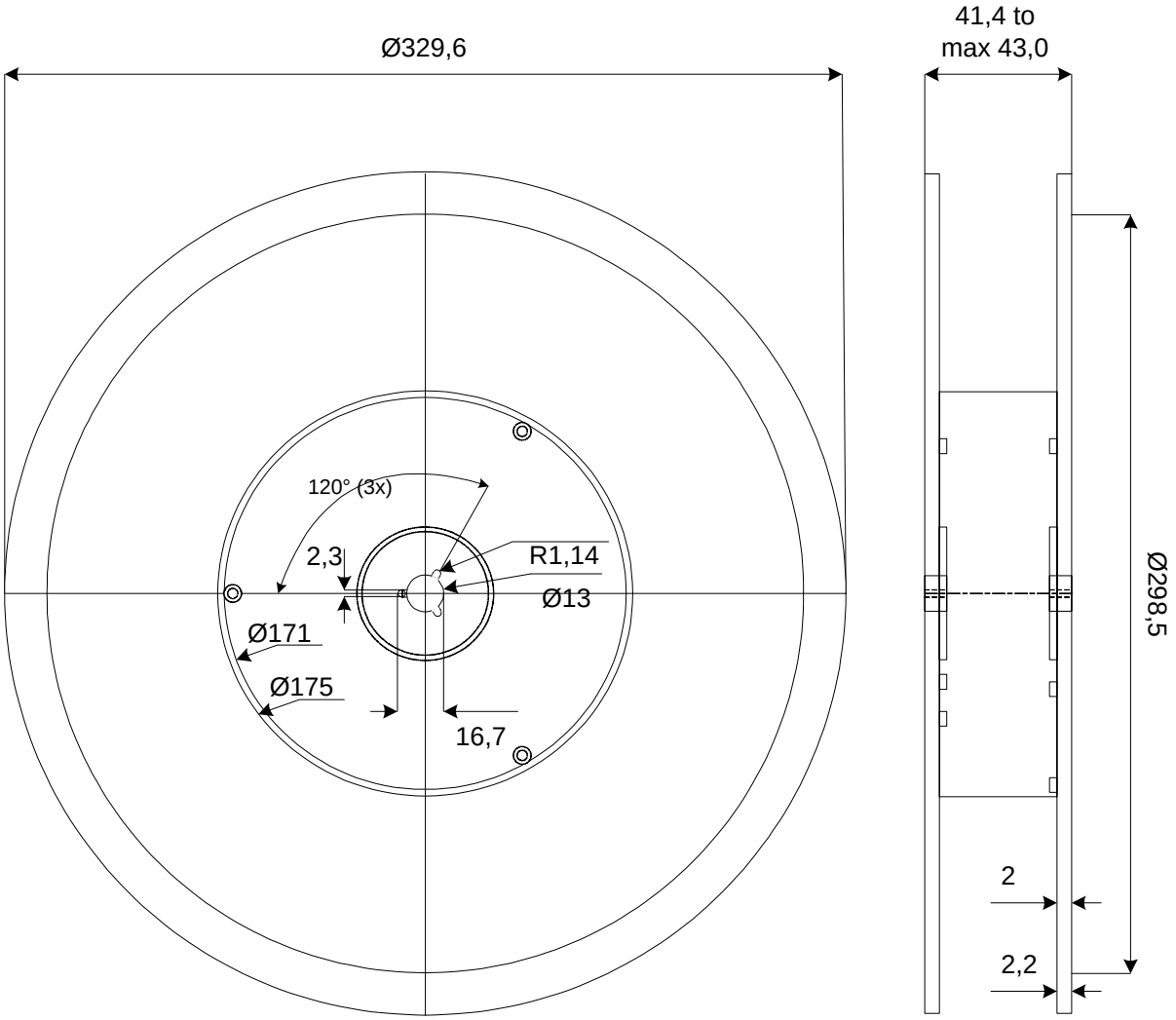


Figure 32. SO8 Package

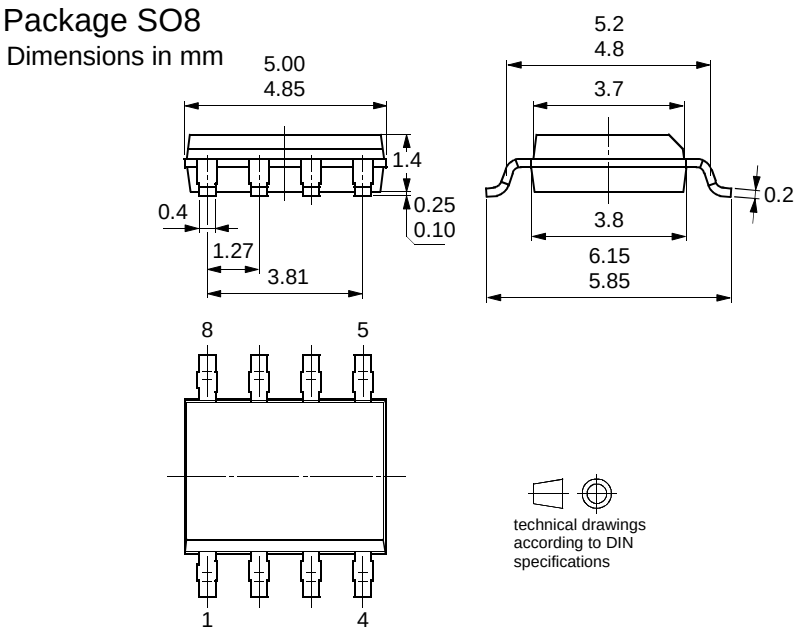
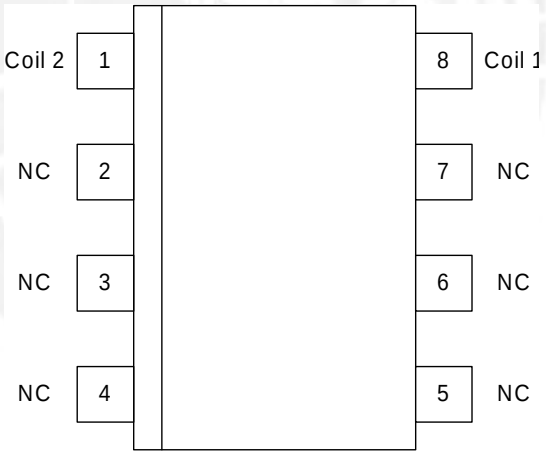


Figure 33. Pinning SO8



Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Changes from Rev. 4517F-RFID-11/03 to Rev. 4517G-RFID-10/04

1. Page 21: Heading “Available Order Codes”: Sentence added

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High Speed Converters/RF Datacom

Avenue de Rochepleine
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Fax: (33) 4-76-58-34-80

Literature Requests
www.atmel.com/literature

4517G–RFID–10/04

TIRA FLEXIBLE CAMBO RGB
CAMBO RGB FLEXIBLE STRIP
Ref.: **2015**

Lámpara / Lamp: LED RGB 150x0,24w
Equipos / Equipment: 12v DC/600 mA
Watios / Watt: 36W/5m
Vida útil / Life span: 40000 h.

Grado de protección / Protection degree: IP65

DESCRIPCIÓN / **DESCRIPTION**

Cinta adhesiva de film de poliéster de máxima estabilidad térmica y química con envoltura de silicona.
Ópticas incorporadas en las lámparas.
Equipo electrónico de 12v de corriente continua y 600 mA (no incluido).
Tiras flexibles RGB compuestas por 30 LEDs por metro de 0,24W en color blanco, cálido 3000 K° o frío 6500 K°.

Adhesive tape made in thermal and chemical stability polyester film with a silicone wrapper.
Built-in-lamp opctics.
12V / 24V electronic equipment with direct power and 600 mA (not included).
Flexible RGB LED strips composed by 30 LEDs 0,24W per meter in warm white 3000k° or cold 6500°.

INSTALACIÓN / **INSTALLATION**

La cara posterior de la tira flexible contiene adhesivo 3M para instalar directamente a soportes metálicos preferiblemente. En caso de instalar en otro tipo de superficies, se recomienda utilizar la Plancha de aluminio disipadora de calor (Ref. 2088) para reducir la temperatura de trabajo de la tira flexible. Su flexibilidad y la dotación de accesorios permiten su aplicación en infinidad de diseños de iluminación decorativa. Las tiras flexibles CAMBO se pueden unir entre sí mediante conectores. Para realizar esta acción es necesario eliminar en los extremos la envoltura de silicona. No seguir las instrucciones de montaje puede acortar la vida útil de la luminaria.

Back side of the strip contains 3M adhesive to install directly on metal brackets preferably. If you try to install in others surfaces types, we recommended the use of a heatsink sheet aluminium (Ref 2088) to try to minimize the heat. It can be use in a lot of styles thanks to his flexibility.
The CAMBO flexible strips offer the posibility of being connected to each other thought connectors. To make this, it is necessary removes the silicone wrapper.
Failure to follow the instructions may result in shorter luminaire life spam.

DIMENSIONES / **MEASURES**

Ancho / Width: 14 mm.
Alto / Heigth: 5 mm.

Polígono Industrial la Estrella.
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www.secom.es secom@secom.es

INCLUYE / **INCLUDES**

Tira Flexible Cambo RGB / **Cambo RGB Flexible Strip** Ref.: **2015**

ACCESORIOS / **ACCESSORIES**

2081 Driver IP65 para tira LED max. 12V DC 60W / Driver IP65 LED max. 12 DC 60W

GARANTÍA / **GUARANTEE:** 2 años observando las condiciones de venta de nuestro Catálogo General / *2 years watching to the conditions of sales of our General Catalog.*

FOTOMETRÍAS / **PHOTOMETRY**

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DECLARACIÓN DE CONFORMIDAD
CONFORMITY DECLARATION

Referencia del producto: **2015 Tira Flexible Cambo RGB**
Product reference: ***2015 Cambo RGB Flexible Strip***

Secom Iluminación S.L. como fabricante declara que el producto mencionado ha sido fabricado de acuerdo con las directivas europeas que se citan a través del cumplimiento de las siguientes normas:

Secom Iluminacion S.L. *as manufacturer, declares that the above mentioned product has been manufactured according to the following European directives and regulations and satisfy the following rules:*

Nº	Directiva	*Directive*
2006/95/CE	**Equipo eléctrico para ser utilizado dentro de unos valores de tensión limitados.** **Directiva de Baja Tensión.**	***Electrical equipment for use within certain voltage limits.*** ***Low Voltage Directive.***
Normas / Generic standard: EN 60598-2-2-:97 + A1:98, EN 60598-1:09+A1:11:09		
Nº	Directiva	*Directive*
2004/108/CE	**Compatibilidad electromagnética.** **Directiva EMC.**	***Electromagnetic compatibility.*** ***EMC directive.***
Normas / *Generic standard*: EN 55015, EN61000-3-2, EN 61000-3-3		

Molina de Segura, 1 de Febrero de 2013

José Antonio Fernández Giménez
RESP. CONTROL DE CALIDAD

Manuel Ramírez Sarrías
RESP. DE PRODUCCIÓN

José María Sandoval Barnuevo
DIRECTOR GENERAL

Esta declaración certifica el cumplimiento con las directivas mencionadas sin detallar las características. Deben observarse las indicaciones de seguridad indicadas en las instrucciones de uso del producto y que forman parte del suministro.

This declaration certifies compliance with the above directives without detailing the features. Must be observed safety instructions given in the instructions for use of the product and that are part of the supply.

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RECOMENDACIONES DE INSTALACIÓN DE TIRAS LED

- Asegurarse que la tira escogida es la idónea para el uso al que se quiere dar, y que la temperatura de trabajo no supere el rango que indica el fabricante. Los tiempos de vida están calculados para trabajar a una temperatura de 25 ºC. Temperaturas superiores a este valor reducirán el tiempo de vida de los LEDs.

- Las características técnicas del producto están referidas a rollos de 5m. Para montajes inferiores se pueden realizar cortes a determinadas distancias (según modelo varía desde 5 a 20cm) para adaptarlo a las necesidades.

- Para montajes superiores a 5m, hay que tener en cuenta que la longitud máxima que recomendamos para poner en paralelo o mediante amplificadores, es de 10m.

- Recomendamos escoger correctamente el voltaje de las fuentes de alimentación, ya que si superamos el valor nominal de la tira, este exceso de voltaje recaería directamente al LED, dañándolo y reduciendo su vida considerablemente.

- La potencia de las fuentes de alimentación tienen que ser sobredimensionadas al consumo real del montaje de las tiras. Se recomienda un mínimo del 20% superior. En instalaciones con muchos metros de tiras, recomendamos repartir con varias fuentes la instalación y evitar poner solo una fuente alimentación con mucha potencia.

- Recomendamos que las F.A. estén lo más cerca posible a la tira. Cuanto más alejadas se encuentren, más pérdidas habrá, lo que provocará tener menos voltaje de alimentación y por consiguiente, menos luminosidad en la tira.

- Aunque se trate de una tira flexible, no es un cable eléctrico y por tanto, su manipulación es más delicada. Si no se tiene cuidado, los golpes pueden causar daños físicos en el epoxy o daños al propio LED.

- Doblar la tira en ángulos de 90º o superiores puede llegar a causar rotura del epoxy o roturas de soldadura del LED.

- Aconsejamos realizar montajes con tiras del mismo lote de suministro. EL LED presenta tolerancias (BIN CODE) que pueden ser visibles en instalaciones donde se proyecta la luz.

- Evitar ubicar las tiras en zonas con temperatura elevada o luz directa del sol. Se recomienda el uso de perfiles de aluminio para reducir la temperatura de trabajo. Para tiras superiores a 70W es obligatorio poner perfil o superficie de aluminio.

- No colocar las tiras en el suelo a menos que dispongan de una estanqueidad IP67.

- Para configuraciones RGB mayores de 20m, es aconsejable que consulte a los expertos de SECOM ILUMINACION.

RECOMMENDATIONS FOR LED STRIP INSTALLATION

• Ensure that the strip selected is the ideal for the use you want, and that the temperature does not exceed the range specified by the manufacturer. The span life is calculated with a work temperature of 25 ° C. Temperatures above this value will reduce the lifetime of the LED.

• The technical characteristics of the product are referred to 5m rolls. For lower mounts cuts can be made at certain distances (depending on the model varies from 5 to 20cm) to suit the needs.

• For assemblies exceeds 5m, should be noted that the maximum length recommended is 10m, for parallel or through amplifiers.

• We recommend choosing the correct voltage power supplies, because when exceeded the nominal value of the strip, this excess would affect directly to the LED voltage, damaging it and reducing its life considerably.

• The power of the power supply used should to be oversized to the strips consumption mounting. We recommend a minimum of 20% higher. In installations with many meters of LED strips, it's recommend installing several supply sources and avoids putting only one power supply with plenty of power.

• We recommend that the driver should be as close as possible to the LED strip, the farther apart they are, more losses will have causing less supply voltage and consequently less light.

• Although it is a flexible strip it isn't a wire and therefore needs a delicate handling. The inadequate care may cause physical damage on the strip or damage the LED itself.

• Bend the strip at angles of 90 ° or more can lead to breakage of epoxy or LED.

• We recommend making montages with LED strips of the same delivery lot. The LED has a certain tolerance (BIN CODE) that may be visible in installations where the light is projected.

• Avoid placing the strips in areas with high temperatures or direct sunlight. It's recommended the use of aluminum to reduce the temperature. To strips to 70W is imperative the use of any profile or other aluminum surface.

• Do not place the strips directly on the floor unless you have an IP67.

• For RGB settings over 20m, it is advisable to consult experts SECOM LIGHTING.

EM4102

Read Only Contactless Identification Device

Description

The EM4102 (previously named H4102) is a CMOS integrated circuit for use in electronic Read Only RF Transponders. The circuit is powered by an external coil placed in an electromagnetic field, and gets its master clock from the same field via one of the coil terminals. By turning on and off the modulation current, the chip will send back the 64 bits of information contained in a factor programmed memory array.

The programming of the chip is performed by laser fusing of polysilicon links in order to store a unique code on each chip.

The EM4102 has several metal options which are used to define the code type and data rate. Data rates of 64, 32 and 16 periods of carrier frequency per data bit are available. Data can be coded as Manchester, Biphase or PSK.

Due to low power consumption of the logic core, no supply buffer capacitor is required. Only an external coil is needed to obtain the chip function. A parallel resonance capacitor of 78 pF is also integrated.

Features

- 64 bit memory array laser programmable
- Several options of data rate and coding available
- On chip resonance capacitor
- On chip supply buffer capacitor
- On chip voltage limiter
- Full wave rectifier on chip
- Large modulation depth due to a low impedance modulation device
- Operating frequency 100 - 150 kHz
- Very small chip size convenient for implantation
- Very low power consumption

Applications

- Animal implantable transponder
- Animal ear tag
- Industrial transponder

Typical Operating Configuration

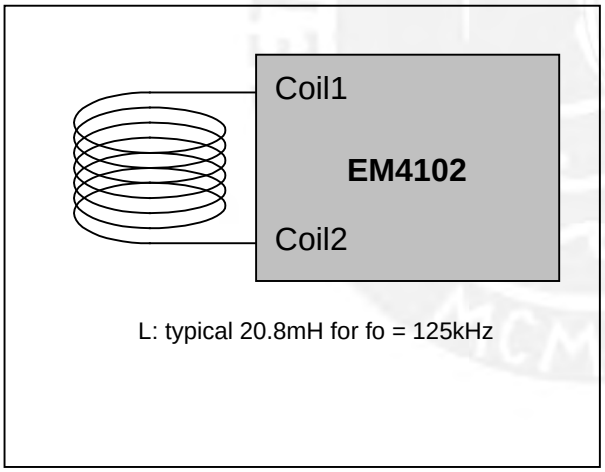


Fig. 1

Pin Assignment

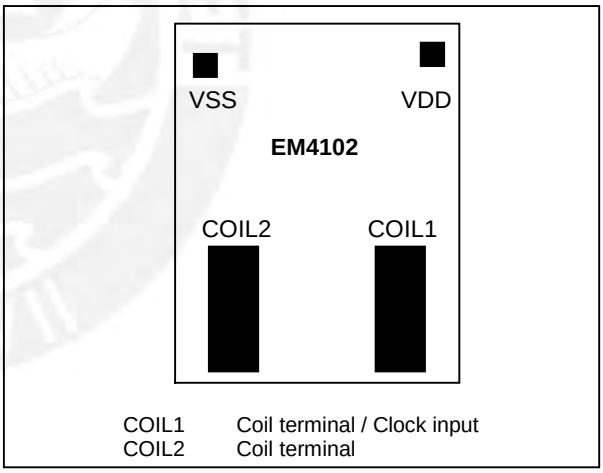


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum DC Current forced on COIL1 & COIL2	I_{COIL}	±30mA
Power Supply	V_{DD}	-0.3 to 7.5V
Storage Temp. Die form	T_{store}	-55 to +200°C
Storage Temp. PCB form	T_{store}	-55 to +125°C
Electrostatic discharge maximum to MIL-STD-883C method 3015	V_{ESD}	2000V

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Operating Temp.	T_{op}	-40		+85	°C
Maximum Coil Current	I_{COIL}	-10		10	mA
AC Voltage on Coil	V_{coil}	3	14*		Vpp
Supply Frequency	f_{coil}	100		150	kHz

*) The AC Voltage on Coil is limited by the on chip voltage limitation circuitry. This is according to the parameter I_{coil} in the absolute maximum ratings.

System Principle

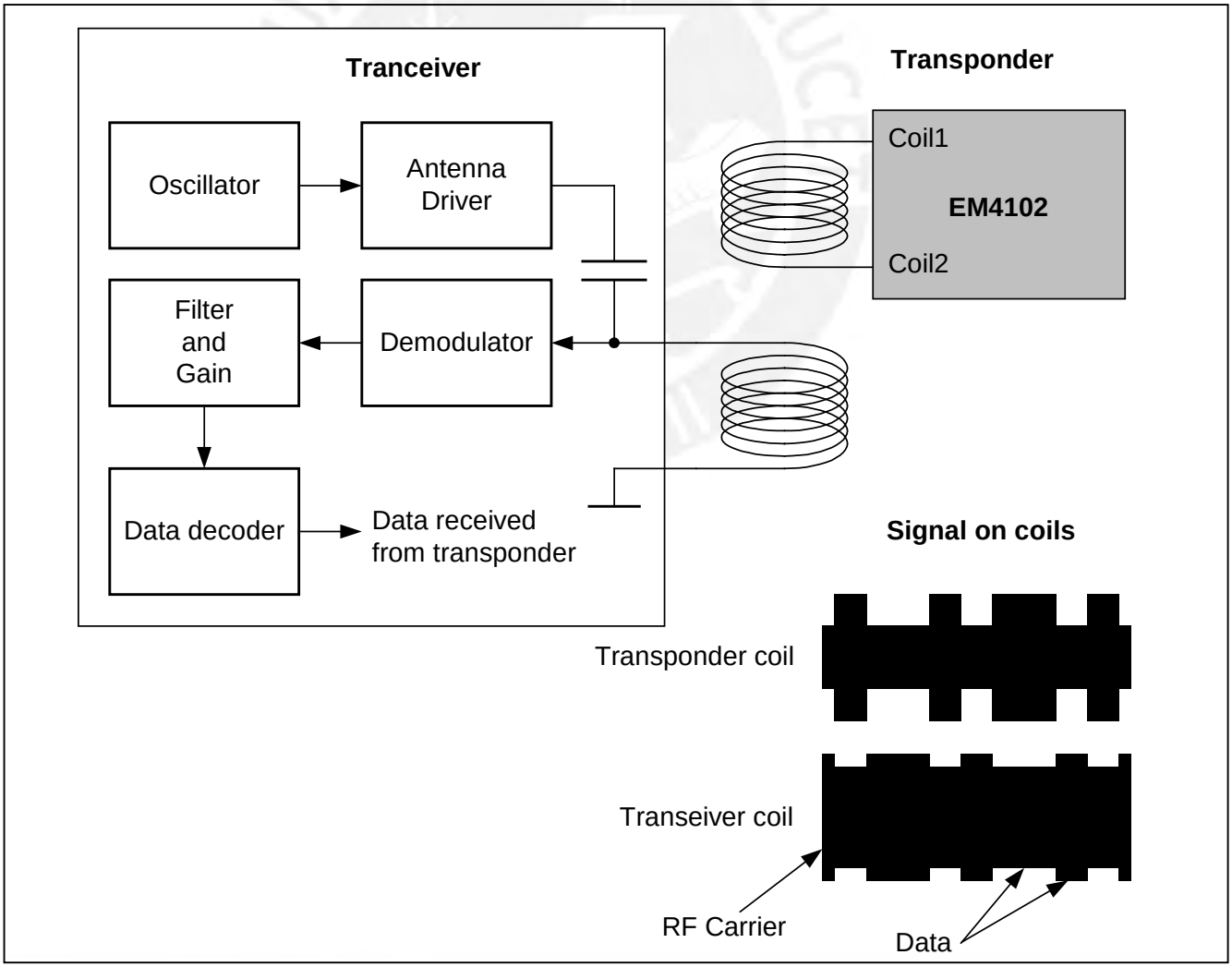


Fig. 3

Electrical Characteristics

V_{DD} = 1.5V, V_{SS} = 0V, f_{C1} = 134kHz square wave, T_a = 25°C
V_{C1} = 1.0V with positive peak at V_{DD} and negative peak at V_{DD} -1V unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}		1.5		1)	V
Rectified Supply Voltage	V_{DDREC}	V_{COIL1} - V_{COIL2} = 2.8 VDC Modulator switch = "ON"	1.5			V
Coil1 - Coil2 Capacitance	C_{res}	V_{coil}=100mVRMS f=10kHz		78 2)		pF
Power Supply Capacitor	C_{sup}			125		pF
Manchester and biphase versions						
Supply Current	I_{DD}			0.6	1.5	µA
C2 pad Modulator ON voltage drop	V_{ONC2}	V_{DD}=5.0V I_{VDDC2}=1mA with ref. to V_{DD}	150	220	280	mV
PSK version						
Supply Current	I_{DDPSK}			0.9	2.0	µA
C2 pad Modulator ON voltage drop	$V_{ONC2PSK}$	V_{DD}=5.0V I_{VDDC2}=100µA with ref. to V_{DD}	500	650	800	mV

Note 1) The maximum voltage is defined by forcing 10mA on COIL1 - COIL2
Note 2) The tolerance of the resonant capacitor is ± 15% over the whole production.
On a wafer basis, the tolerance is ± 2%

Timing Characteristics

V_{DD} = 1.5V, V_{SS} = 0V, f_{coil} = 134kHz square wave, T_a = 25°C
V_{C1} = 1.0V with positive peak at V_{DD} and negative peak at V_{DD} -1V unless otherwise specified
Timings are derived from the field frequency and are specified as a number of RF periods.

Parameter	Symbol	Test Conditions	Value	Units
Read Bit Period	T_{rdb}	depending on option	64, 32, 16	RF periods

Timing Waveforms

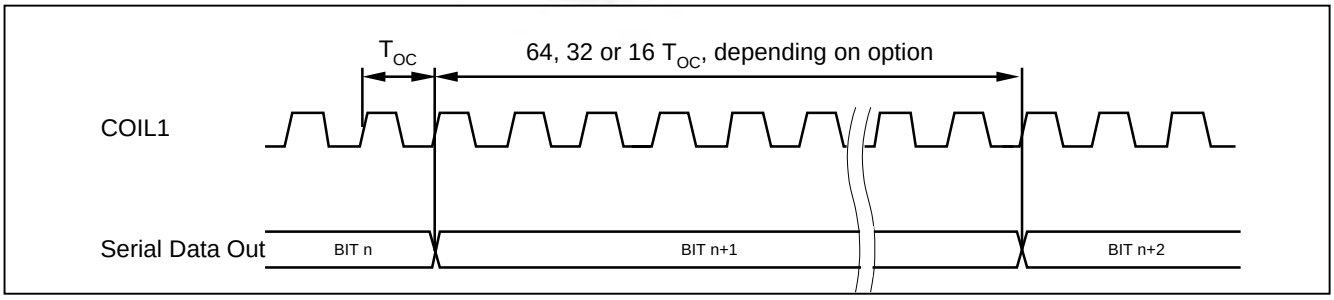


Fig. 4

Block Diagram

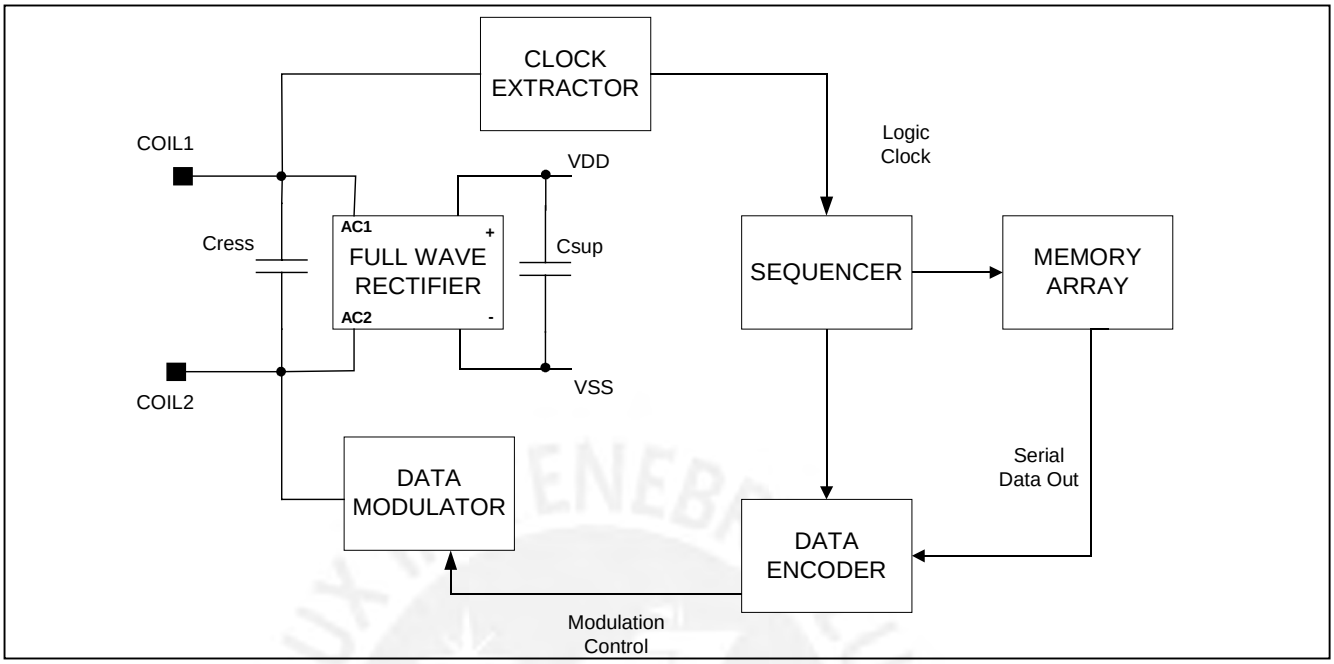


Fig. 5

Functional Description

General

The EM4102 is supplied by means of an electromagnetic field induced on the attached coil. The AC voltage is rectified in order to provide a DC internal supply voltage. When the last bit is sent, the chip will continue with the first bit until the power goes off.

Full Wave Rectifier

The AC input induced in the external coil by an incident magnetic field is rectified by a Graetz bridge. The bridge will limit the internal DC voltage to avoid malfunction in strong fields.

Clock Extractor

One of the coil terminals (COIL1) is used to generate the master clock for the logic function. The output of the clock extractor drives a sequencer.

Sequencer

The sequencer provides all necessary signals to address the memory array and to encode the serial data out.
Three mask programmed encoding versions of logic are available. These three encoding types are Manchester, biphase and PSK. The bit rate for the first and the second type can be 64 or 32 periods of the field frequency. For the PSK version, the bit rate is 16.
The sequencer receives its clock from the COIL1 clock extractor and generates every internal signal controlling the memory and the data encoder logic.

Data Modulator

The data modulator is controlled by the signal Modulation Control in order to induce a high current in the coil. The coil 2 transistor drives this high current. This will affect the magnetic field according to the data stored in the memory array.

Memory Array for Manchester & Bi-Phase encoding ICs

The EM4102 contains 64 bits divided in five groups of information. 9 bits are used for the header, 10 row parity bits (P0-P9), 4 column parity bits (PC0-PC3), 40 data bits (D00-D93), and 1 stop bit set to logic 0.

1	1	1	1	1	1	1	1	1	9 header bits
8 version bits or customer ID				D00	D01	D02	D03	P0	
				D10	D11	D12	D13	P1	
32 data bits				D20	D21	D22	D23	P2	
				D30	D31	D32	D33	P3	
				D40	D41	D42	D43	P4	
				D50	D51	D52	D53	P5	
				D60	D61	D62	D63	P6	
				D70	D71	D72	D73	P7	
				D80	D81	D82	D83	P8	
				D90	D91	D92	D93	P9	10 line parity bits
				PC0	PC1	PC2	PC3	S0	
				4 column parity bits					

The header is composed of the 9 first bits which are all programmed to "1". Due to the data and parity organisation, this sequence cannot be reproduced in the data string. The header is followed by 10 groups of 4 data bits allowing 100 billion combinations and 1 even row parity bit. Then, the last group consists of 4 event column parity bits without row parity bit. S0 is a stop bit which is written to "0"
Bits D00 to D03 and bits D10 to D13 are customer specific identification.
These 64 bits are outputted serially in order to control the modulator. When the 64 bits data string is outputted, the output sequence is repeated continuously until power goes off.

Memory Array for PSK encoding ICs
The PSK coded IC's are programmed with odd parity for P0 and P1 and always with a logic zero.
The parity bits from P2 to P9 are even.
The column parity PC0 to PC3 are calculated including the version bits and are even parity bits.

Code Description
Manchester
There is always a transition from ON to OFF or from OFF to ON in the middle of bit period. At the transition from logic bit “1” to logic bit “0” or logic bit “0” to logic bit “1” the phase change. Value high of data stream presented below modulator switch OFF, low represents switch ON (see Fig. 6).

Biphase Code
At the beginning of each bit, a transition will occur. A logic bit “1” will keep its state for the whole bit duration and a logic bit “0” will show a transition in the middle of the bit duration (see Fig. 7).

PSK Code
Modulation switch goes ON and OFF alternately every period of carrier frequency. When a phase shift occurs, a logical "0" is read from the memory. If no shift phase occurs after a data rate cycle, a logical "1" is read (see Fig. 8).

Manchester Code

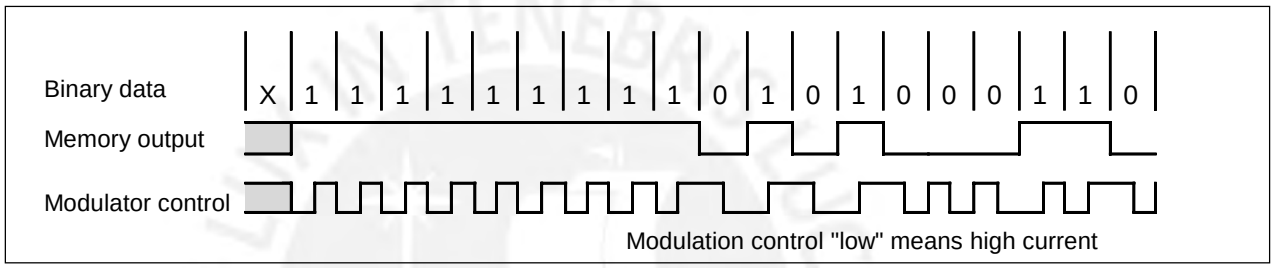


Fig. 6

Biphase Code

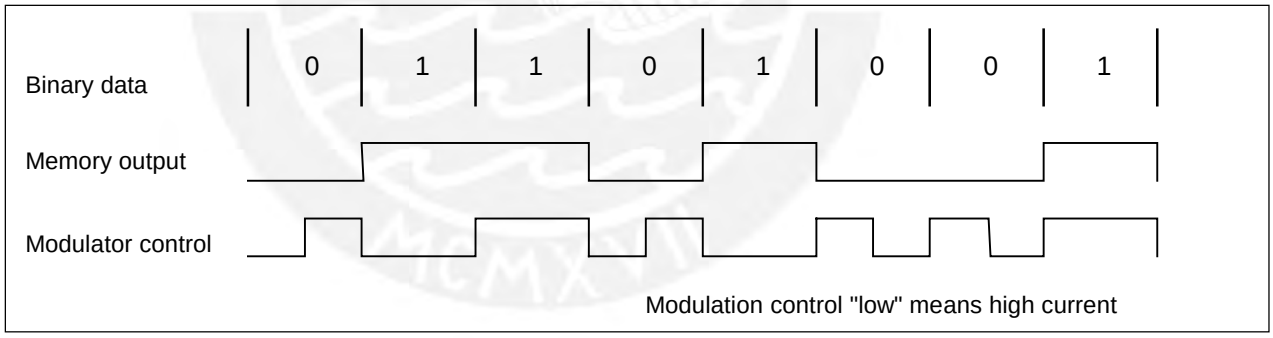


Fig. 7

PSK Code

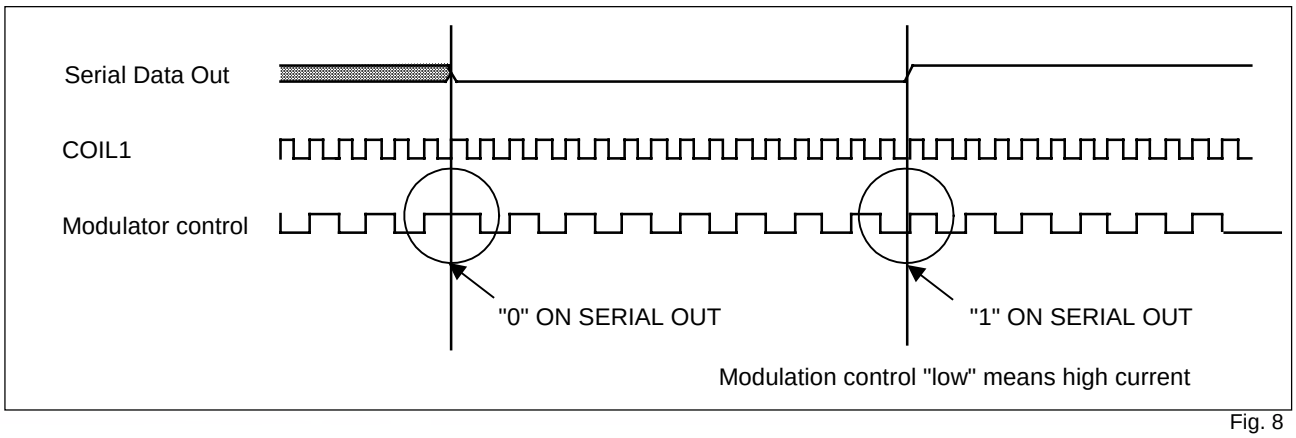
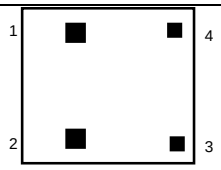


Fig. 8

Pad Description

Pad	Name	Function
1	COIL2	Coil terminal 2 / data output
2	COIL1	Coil terminal 1 / clock input
3	VDD	Positive internal supply voltage
4	VSS	Negative internal supply voltage



CHIP Dimensions

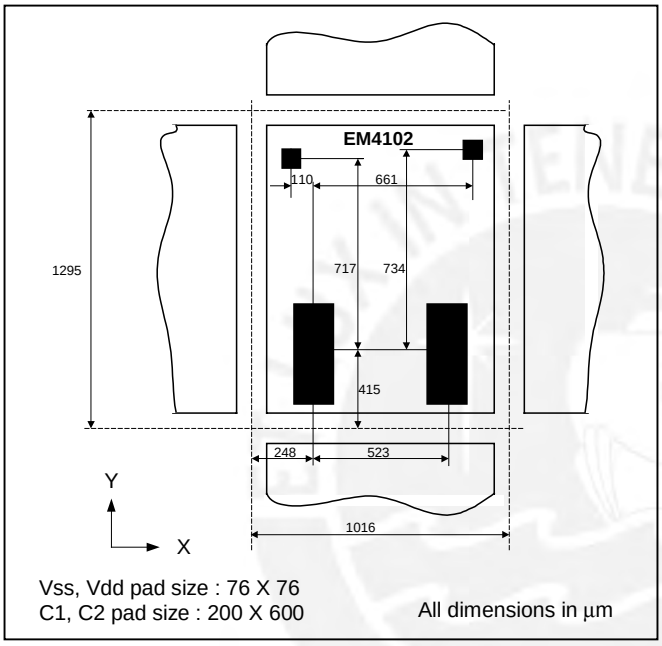


Fig. 9

Ordering Information

Die Form

EM4102 A6 WS 11 E - %%%

Version:
A6 = Manchester, 64 clocks per bit
A5 = Manchester, 32 clocks per bit
B6 = Bi-Phase, 64 clocks per bit
B5 = Bi-Phase, 32 clocks per bit
C4 = PSK, 16 clocks per bit

Die form:
WW = Wafer
WS = Sawn Wafer/Frame
WT = Sticky Tape
WP = Waffle Pack (note 1)

Thickness:
7 = 7 mils (178um)
11 = 11 mils (280um)

Bumping:
" " (blank) = no bumps
E = with Gold Bumps

Customer Version:
%%% = only for custom specific version

This chart shows general offering; for detailed Part Number to order, please see the table “Standard Versions” below.

Card Form

This chart shows general offering; for detailed Part Number to order, please see the table “Standard Versions” below.

EM4102 A6 CX - %%%

Version:
A6 = Manchester, 64 clocks per bit
A5 = Manchester, 32 clocks per bit
B6 = Bi-Phase, 64 clocks per bit
B5 = Bi-Phase, 32 clocks per bit
C4 = PSK, 16 clocks per bit

Card form:
CX = Card without magnetic strip, GLOSS
CY = Card without magnetic strip, MATT
CM = Card with magnetic strip, GLOSS
CN = Card with magnetic strip, MATT

Customer Version:
%%% = only for custom specific version

Remarks:

- For ordering please use table of “Standard Version” table below.
- For specifications of Delivery Form, including gold bumps, tape and bulk, as well as possible other delivery form or packages, please contact EM Microelectronic-Marin S.A. Sales office.
- **Note 1:** This is a non-standard package. Please contact EM Microelectronic-Marin S.A Sales office for availability.

Standard Versions:

The versions below are considered standards and should be readily available. For other versions or other delivery form, please contact EM Microelectronic-Marin S.A. Please make sure to give complete part number when ordering, without spacing.

Part Number	Bit coding	Cycle/bit	Card / Die Form	Delivery Form / bumping	For EM internal use only	
					old version	OPS#
EM4102 A6 CM	Manchester	64	card with magnetic strip, GLOSS	-	001	2973
EM4102 A6 CX	Manchester	64	card wihtout magnetic strip, GLOSS	-	001	2972
EM4102 A6 CY	Manchester	64	card wihtout magnetic strip, MATT	-	001	2971
EM4102 A6 WP11E	Manchester	64	Die in waffle pack, 11 mils	with gold bumps	001	3199
EM4102 A6 WS11E	Manchester	64	Sawn wafer/Frame, 11 mils	with gold bumps	001	4019
EM4102 A6 WT11E	Manchester	64	Die on sticky tape, 11 mils	with gold bumps	001	2881
EM4102 A6 WW11E	Manchester	64	Unsawn wafer, 11 mils	with gold bumps	001	3711
EM4102 XX YYY-%%%	custom	custom	custom	custom	%%%	

Product Support

Check our Web Site under Products/RF Identification section.
Questions can be sent to cid@emmicroelectronic.com

Pruebas de Sistema de acceso vehicular PUCP

N° de pruebas : 70