PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

FACULTAD DE CIENCIAS E INGENIERÍA

DISEÑO DE UN SISTEMA ELECTRÓNICO PARA LOS MOVIMIENTOS DE UN CAÑÓN ANTIAÉREO A ESCALA

ANEXOS

Tesis para optar el Título de Ingeniero Electrónico, que presenta el alumno:

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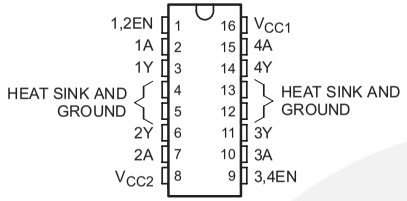
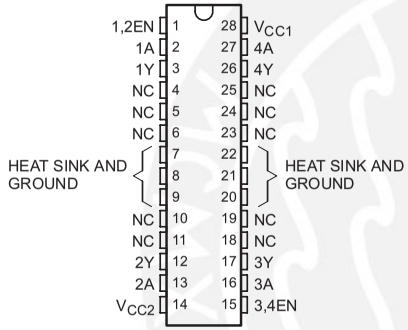
Lima, Agosto del 2009

- **Featuring Unitrode L293 and L293D Products Now From Texas Instruments**
- **Wide Supply-Voltage Range: 4.5 V to 36 V**
- **Separate Input-Logic Supply**
- **Internal ESD Protection**
- **Thermal Shutdown**
- **High-Noise-Immunity Inputs**
- **Functionally Similar to SGS L293 and SGS L293D**
- **Output Current 1 A Per Channel (600 mA for L293D)**
- **Peak Output Current 2 A Per Channel (1.2 A for L293D)**
- **Output Clamp Diodes for Inductive Transient Suppression (L293D)**

L293 . . . N OR NE PACKAGE
L293D . . . NE PACKAGE
(TOP VIEW)



L293 . . . DWP PACKAGE
(TOP VIEW)



description/ordering information

The L293 and L293D are quadruple high-current half-H drivers. The L293 is designed to provide bidirectional drive currents of up to 1 A at voltages from 4.5 V to 36 V. The L293D is designed to provide bidirectional drive currents of up to 600-mA at voltages from 4.5 V to 36 V. Both devices are designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are TTL compatible. Each output is a complete totem-pole drive circuit, with a Darlington transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs, with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled, and their outputs are active and in phase with their inputs. When the enable input is low, those drivers are disabled, and their outputs are off and in the high-impedance state. With the proper data inputs, each pair of drivers forms a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	HSOP (DWP)	Tube of 20	L293DWP	L293DWP
	PDIP (N)	Tube of 25	L293N	L293N
	PDIP (NE)	Tube of 25	L293NE	L293NE
		Tube of 25	L293DNE	L293DNE

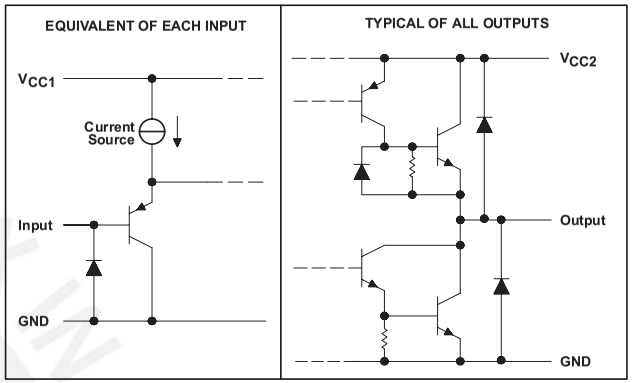
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

L293, L293D
QUADRUPLE HALF-H DRIVERS

SLRS008C – SEPTEMBER 1986 – REVISED NOVEMBER 2004

schematics of inputs and outputs (L293D)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC1} (see Note 1) . . . . . 36 V
Output supply voltage, V_{CC2} . . . . . 36 V
Input voltage, V_I . . . . . 7 V
Output voltage range, V_O . . . . . −3 V to V_{CC2} + 3 V
Peak output current, I_O (nonrepetitive, t ≤ 5 ms): L293 . . . . . ±2 A
Peak output current, I_O (nonrepetitive, t ≤ 100 µs): L293D . . . . . ±1.2 A
Continuous output current, I_O: L293 . . . . . ±1 A
Continuous output current, I_O: L293D . . . . . ±600 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DWP package . . . . . TBD°C/W
N package . . . . . 67°C/W
NE package . . . . . TBD°C/W
Maximum junction temperature, T_J . . . . . 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
	Supply voltage	V_{CC1}	4.5	7	V
		V_{CC2}	V_{CC1}	36	
V_{IH}	High-level input voltage	$V_{CC1} \le 7$ V	2.3	V_{CC1}	V
		$V_{CC1} \ge 7$ V	2.3	7	V
V_{IL}	Low-level output voltage		−0.3†	1.5	V
T_A	Operating free-air temperature		0	70	°C

† The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for logic voltage levels.

electrical characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		L293: I_{OH} = −1 A L293D: I_{OH} = −0.6 A		V_{CC2} − 1.8	V_{CC2} − 1.4		V
V_{OL}	Low-level output voltage		L293: I_{OL} = 1 A L293D: I_{OL} = 0.6 A			1.2	1.8	V
V_{OKH}	High-level output clamp voltage		L293D: I_{OK} = −0.6 A			V_{CC2} + 1.3		V
V_{OKL}	Low-level output clamp voltage		L293D: I_{OK} = 0.6 A			1.3		V
I_{IH}	High-level input current	A	V_I = 7 V			0.2	100	µA
		EN				0.2	10	
I_{IL}	Low-level input current	A	V_I = 0			−3	−10	µA
		EN				−2	−100	
I_{CC1}	Logic supply current		I_O = 0	All outputs at high level		13	22	mA
				All outputs at low level		35	60	
				All outputs at high impedance		8	24	
I_{CC2}	Output supply current		I_O = 0	All outputs at high level		14	24	mA
				All outputs at low level		2	6	
				All outputs at high impedance		2	4	

switching characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	L293NE, L293DNE			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output from A input	C_L = 30 pF, See Figure 1		800		ns
t_{PHL}	Propagation delay time, high-to-low-level output from A input			400		ns
t_{TLH}	Transition time, low-to-high-level output			300		ns
t_{THL}	Transition time, high-to-low-level output			300		ns

switching characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	L293DWP, L293N L293DN			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output from A input	C_L = 30 pF, See Figure 1		750		ns
t_{PHL}	Propagation delay time, high-to-low-level output from A input			200		ns
t_{TLH}	Transition time, low-to-high-level output			100		ns
t_{THL}	Transition time, high-to-low-level output			350		ns

L293, L293D
QUADRUPLE HALF-H DRIVERS

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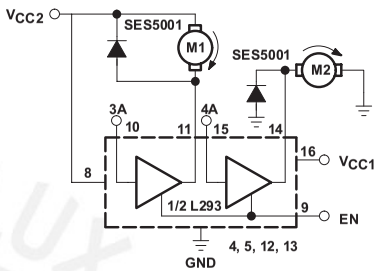
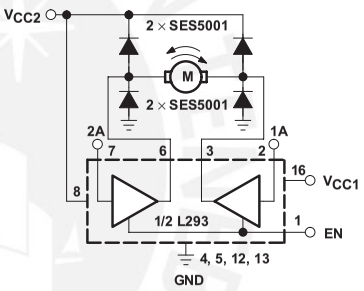
APPLICATION INFORMATION



EN	3A	M1	4A	M2
H	H	Fast motor stop	H	Run
H	L	Run	L	Fast motor stop
L	X	Free-running motor stop	X	Free-running motor stop

L = low, H = high, X = don't care

Figure 4. DC Motor Controls (connections to ground and to supply voltage)



EN	1A	2A	FUNCTION
H	L	H	Turn right
H	H	L	Turn left
H	L	L	Fast motor stop
H	H	H	Fast motor stop
L	X	X	Fast motor stop

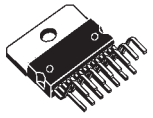
L = low, H = high, X = don't care

Figure 5. Bidirectional DC Motor Control

L298

DUAL FULL-BRIDGE DRIVER

- OPERATING SUPPLY VOLTAGE UP TO 46 V
- TOTAL DC CURRENT UP TO 4 A
- LOW SATURATION VOLTAGE
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)



Multiwatt15

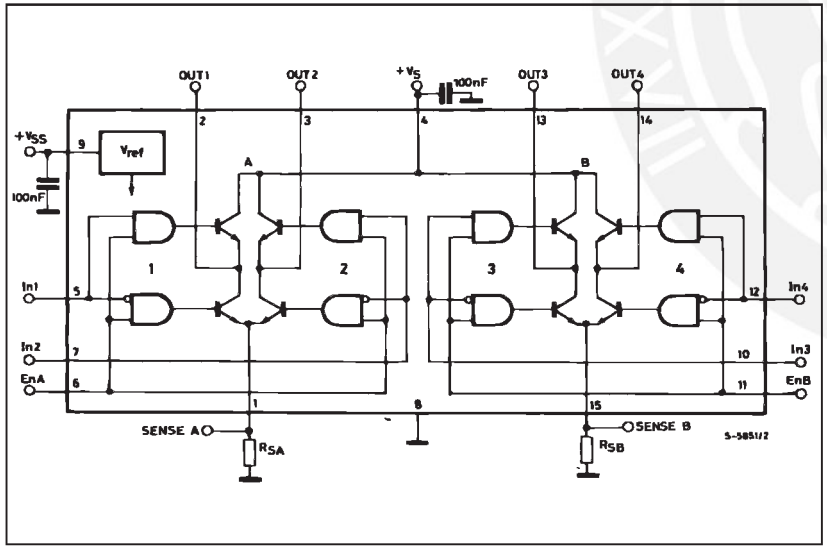
PowerSO20

ORDERING NUMBERS : L298N (Multiwatt Vert.)
L298HN (Multiwatt Horiz.)
L298P (PowerSO20)

DESCRIPTION

The L298 is an integrated monolithic circuit in a 15-lead Multiwatt and PowerSO20 packages. It is a high voltage, high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC and stepping motors. Two enable inputs are provided to enable or disable the device independently of the input signals. The emitters of the lower transistors of each bridge are connected together and the corresponding external terminal can be used for the connection of an external sensing resistor. An additional supply input is provided so that the logic works at a lower voltage.

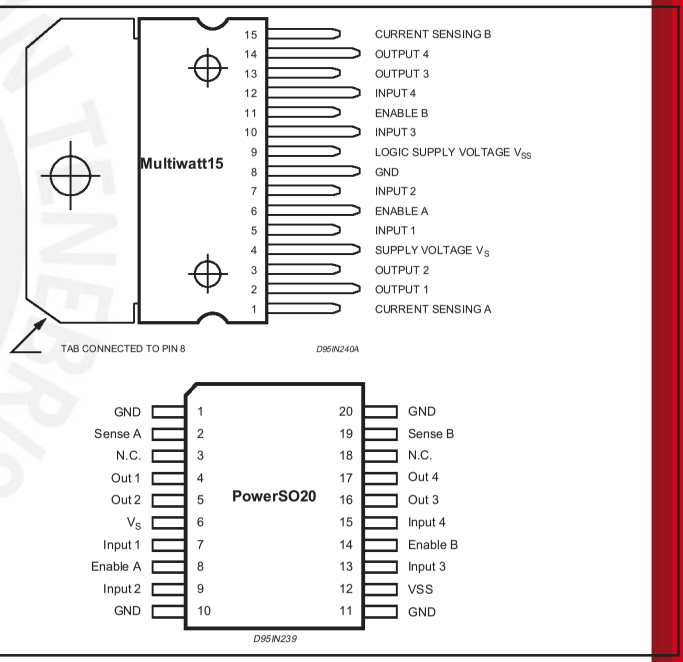
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Power Supply	50	V
V_{SS}	Logic Supply Voltage	7	V
V_i,V_{en}	Input and Enable Voltage	–0.3 to 7	V
I_O	Peak Output Current (each Channel) – Non Repetitive (t = 100µs) –Repetitive (80% on –20% off; t_{on} = 10ms) –DC Operation	 3 2.5 2	 A A A
V_{sens}	Sensing Voltage	–1 to 2.3	V
P_{tot}	Total Power Dissipation (T_{case} = 75°C)	25	W
T_{op}	Junction Operating Temperature	–25 to 130	°C
T_{stg}, T_j	Storage and Junction Temperature	–40 to 150	°C

PIN CONNECTIONS (top view)



THERMAL DATA

Symbol	Parameter		PowerSO20	Multiwatt15	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	–	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	13 (*)	35	°C/W

(*) Mounted on aluminum substrate

PIN FUNCTIONS (refer to the block diagram)

MW.15	PowerSO	Name	Function
1;15	2;19	Sense A; Sense B	Between this pin and ground is connected the sense resistor to control the current of the load.
2;3	4;5	Out 1; Out 2	Outputs of the Bridge A; the current that flows through the load connected between these two pins is monitored at pin 1.
4	6	V_S	Supply Voltage for the Power Output Stages. A non-inductive 100nF capacitor must be connected between this pin and ground.
5;7	7;9	Input 1; Input 2	TTL Compatible Inputs of the Bridge A.
6;11	8;14	Enable A; Enable B	TTL Compatible Enable Input: the L state disables the bridge A (enable A) and/or the bridge B (enable B).
8	1,10,11,20	GND	Ground.
9	12	VSS	Supply Voltage for the Logic Blocks. A100nF capacitor must be connected between this pin and ground.
10; 12	13;15	Input 3; Input 4	TTL Compatible Inputs of the Bridge B.
13; 14	16;17	Out 3; Out 4	Outputs of the Bridge B. The current that flows through the load connected between these two pins is monitored at pin 15.
–	3;18	N.C.	Not Connected

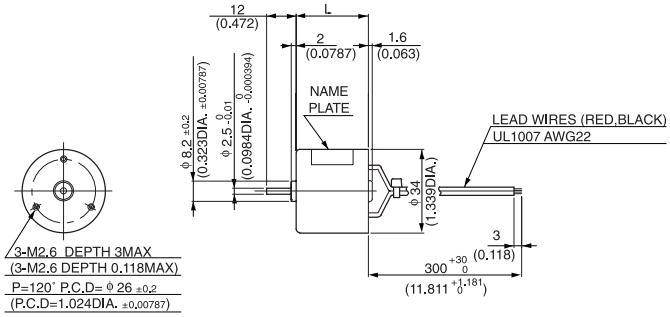
ELECTRICAL CHARACTERISTICS (V_S = 42V; V_{SS} = 5V, T_j = 25°C; unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 4)	Operative Condition	V_{IH} +2.5		46	V
V_{SS}	Logic Supply Voltage (pin 9)		4.5	5	7	V
I_S	Quiescent Supply Current (pin 4)	V_{en} = H; I_L = 0 V_i = L V_i = H		13 50	22 70	mA mA
		V_{en} = L V_i = X			4	mA
I_{SS}	Quiescent Current from V_{SS} (pin 9)	V_{en} = H; I_L = 0 V_i = L V_i = H		24 7	36 12	mA mA
		V_{en} = L V_i = X			6	mA
V_{iL}	Input Low Voltage (pins 5, 7, 10, 12)		–0.3		1.5	V
V_{iH}	Input High Voltage (pins 5, 7, 10, 12)		2.3		VSS	V
I_{iL}	Low Voltage Input Current (pins 5, 7, 10, 12)	V_i = L			–10	µA
I_{iH}	High Voltage Input Current (pins 5, 7, 10, 12)	Vi = H ≤ V_{SS} –0.6V		30	100	µA
V_{en} = L	Enable Low Voltage (pins 6, 11)		–0.3		1.5	V
V_{en} = H	Enable High Voltage (pins 6, 11)		2.3		V_{SS}	V
I_{en} = L	Low Voltage Enable Current (pins 6, 11)	V_{en} = L			–10	µA
I_{en} = H	High Voltage Enable Current (pins 6, 11)	V_{en} = H ≤ V_{SS} –0.6V		30	100	µA
$V_{CEsat(H)}$	Source Saturation Voltage	I_L = 1A I_L = 2A	0.95	1.35 2	1.7 2.7	V V
$V_{CEsat(L)}$	Sink Saturation Voltage	I_L = 1A (5) I_L = 2A (5)	0.85	1.2 1.7	1.6 2.3	V V
V_{CEsat}	Total Drop	I_L = 1A (5) I_L = 2A (5)	1.80		3.2 4.9	V V
V_{sens}	Sensing Voltage (pins 1, 15)		–1 (1)		2	V

DME34

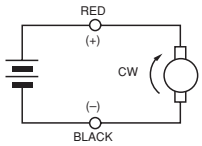
MODEL CODE	VOLTAGE	OUTPUT	CURRENT
SA	12V	1.3W	0.2A
SB	24V	1.3W	0.1A
BA	12V	4.5W	0.65A
BB	24V	4.5W	0.31A
KB	24V	7W	0.41A

●DIMENSIONS Unit mm(inch)



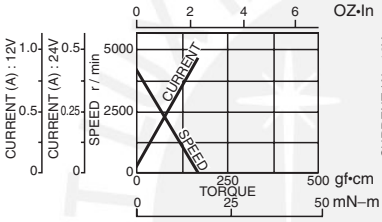
Model	L	Weight	
		g	lb
DME34SA DME34SB	29.5	100	0.22
DME34BA DME34BB	35.0	110	0.24
DME34KB	45	250	0.55

●CONNECTION

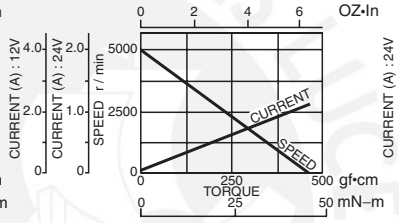


●CURRENT, SPEED-TORQUE CURVE

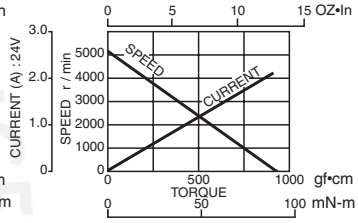
DME34SA, DME34SB



DME34BA, DME34BB



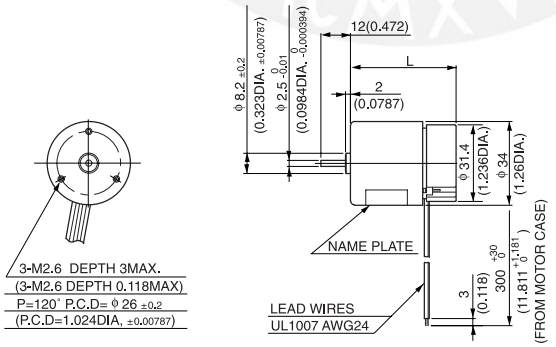
DME34KB



●STANDARD SPECIFICATIONS

Model	Rated						No load		Stall torque	
	Output	Voltage	Torque		Current	Speed	Current	Speed	mN-m	oz·in
	W	V	mN-m	oz·in	A	r/min	A	r/min		
DME34SA	1.3	12	3.9	0.56	0.2	3300	0.04	4300	17	2.36
DME34SB	1.3	24	3.9	0.56	0.1	3300	0.02	4300	17	2.36
DME34BA	4.5	12	11.8	1.67	0.65	3700	0.04	5000	45	6.39
DME34BB	4.5	24	11.8	1.67	0.31	3700	0.04	5000	45	6.39
DME34KB	7	24	14.7	2.08	0.41	4300	0.06	5100	92	13.03

●REVOLUTION SENSOR MAGNET TYPE



Model	L	Weight	
		g	lb
DME34SMA DME34SMB	43.1	110	0.24
DME34BMA DME34BMB	48.6	120	0.26
DME34KMB	58.6	260	0.57

Compact DC Motors

Japan Servo's DC Miniature Motors are widely used in a variety of application fields, from copiers and other office equipment, to remote-controlled equipment, medical equipment, vending machines, and game machines.

These motors may be combined with Japan Servo's full line of gearheads to meet a wide range of torque and output speed specifications.

Japan Servo provides a practical and economic choice as drive actuators. Strict quality control ensure reliable performance as well as prompt delivery at reasonable price. Japan Servo provides a full variation line-up of stock model and customized design motors to best meet your specific application needs.

DC SMALL MOTORS DME Series

The DME Series motor is a feasible and practical DC motor that is used popularly in many applications.

According to user demands, Japan Servo combines the DME motor with a wide variation of high-performance gearboxes to further increase the application possibilities for the DME Series.

Also, in response to demands for a simple, low-cost motor that has a certain amount of controllability, Japan Servo provides DME models that feature pulse generators (magnetic or optical PG).

For certain models of the DME Series, the motor and gearboxes can be ordered separately, allowing for much greater versatility by combining various type motors with a wide range of reduction gears. Please refer to the product line-up chart to select the DME Series motor that is just right for your specific needs.

●DME SERIES MOTOR'S CONSTRUCTION AND CHARACTERISTICS.

MODEL	BRUSH HOLDING	CORE SLOTS	BEARING	MAGNET	LIFE* (hrs)	OUTPUT POWER (W) S	B	K	5	10	15	PAGE
DME 25	Holder	3 slots	Sintered sleeve bearing	Anisotropic	1000		○		◎3			6
DME 33	Spring plate	3 slots	Sintered sleeve bearing	Isotropic Anisotropic	1000	○			◎0.7			9
							○		◎3			
DME 34	Spring plate	3 slots	Sintered sleeve bearing	Isotropic Anisotropic	1000 (500)	○	○	○	◎1.3 ◎4.5 ◎7			15
DME 37	Holder	7 slots	Sintered sleeve bearing	Anisotropic	2000	○			◎4.6			22
							○		◎7.2			
DME 44	Holder	10 slots	Ball bearing	Anisotropic	2000	○			◎9.2			25
							○			◎14.8		
DME 60	Holder	12 slots	Sint. sleeve/Ball bearing	Isotropic Anisotropic	2000	○			◎	13		29
							○				26◎	

FEATURE	BRUSH HOLDER	BEARING	MAGNET
	Holder:Long-life 2000hours (1000 hours only for DME25, due to its high-speed operation)	Ball bearing :Long-life	Anisotropic :High output
	Spring plate:Standard 1000hours	Sintered sleeve bearing :Standard	Isotropic :Standard

*Operated in motor alone, and single direction.

DME

Motors with pulse generators:

There are two types of pulse generators that are featured in DME series motors : the magnetic and optical revolution sensor. (Note, the optical revolution sensor is available only in the DME34 model.) Both are incremental revolution sensor. And all the above generators can output Single Phase pulse signal only. When TWO Phase signal is required, contact our sales agent near you or directly to us. We may quote on case by case basis.

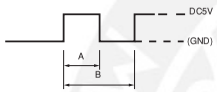
Magnetic Type

Optical Type

Magnetic Revolution Sensor :

Compared to the optical revolution sensor, the magnetic revolution sensor is more resistant to high temperatures, dust contaminations, vibrations and impact shocks. The design of the magnetic revolution sensor type motor is also more simple. In incremental type revolution sensor, pulse output signals are sent to a counter wherein the incremented value is displayed. Signal noise, here, lead to performance errors. Magnetic type revolution sensors are especially vulnerable to signal noise since the signal levels are usually very low (20mA to 30mA). Thus, make sure magnetic revolution sensor type motors are provided proper magnetic shielding, and signal lines are as short as possible (ideally within 5m).

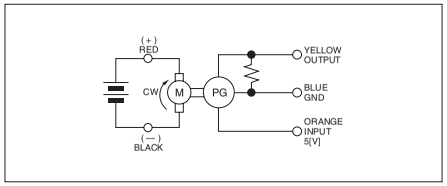
●STANDARD SPECIFICATION OF REVOLUTION SENSOR

REVOLUTION SENSOR TYPE	MAGNETIC	OPTICAL
PULSE PER REVOLUTION	12P/rev.	24P/rev.
INPUT VOLTAGE	DC5V±10%	DC5V±10%
CURRENT CONSUMPTION	5mA nominal	25mA nominal
DUTY (B/A)	50±20%	50±10%
OUTPUT WAVEFORM (COMMON)		

Optical Revolution Sensor:

Long-life LED is used as the light emitter, and a photo-transistor is used as the light detector. When using optical revolution sensor type motors, special considerations are needed to protect against dust and extreme temperatures. The most frequent causes of trouble in optical revolution sensors are : dust build-ups impairing proper optical properties ; and extreme leading to deterioration in light emission performance. Japan Servo can thus ensure full rated performance only in ambient temperatures between 0 to 40 degrees centigrade, and in dust-free conditions.

●CONNECTION



Handling Precautions:

DME Series DC SMALL Motors

Handling Precautions

DME Series DC motors are compact, high-performance and high-output motors that allow for versatile speed control, and that can be operated with battery or other relatively small power supplies. Practical as they are in countless applications, certain basic precautions are necessary in order to avoid abnormal brush wear and hazardous heat damages.

Overloading and locking :

Even when operated at the rated voltage, if the motor is overloaded or locked, excessive torque builds up, increasing the current that flows to the motor and causing burn ups.

Brush wear caused by power supply ripples :

Brush wear is caused either by mechanical abrasion between the brush and the commutator, or by electrical sparks from the commutator. Most of the brush wear is the latter, electrical type, which increases with power supply ripple. It is thus recommended that stable, DC power be used, as possible. However, when using rectified from an AC power supply, make sure that the ripples are minimized with filter or other means.

Ambient condition :

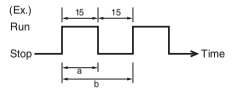
The DC motor's lifetime depends greatly on the condition of the commutator. Dirt, grease or moisture on the commutator surface impairs normal performance, and in turn, increases brush wear.

Operations exceeding rated speeds :

When voltages in excess of the rated value is applied, the motor operates at speed exceeding its rated limit. This can cause : heat damages to the shaft ; direct damages to the brush ; or vibrations causing sparks that damage the commutator surface, which in turn leads to mechanical wear on the brush.

Gear heads for intermittent drive :

This is not suitable for continuous drive. Because the torque is conveyed from fixed shaft to planet gear pieces around the shaft. The duty cycle must be 50% or less. And set ON time at 15 seconds or shorter.



$\frac{a}{b} \times 100 = 50\%$

(This is to apply "36G", "43G", "5C" and "L")

Designed brush position :

When the motor is manufactured, the brush is carefully positioned in relation to the magnet polarity, so that the speed and current are equal in both clockwise and counter-clockwise direction revolutions. Make sure that components such as the brush holder and rear cover are not moved their fixed positions. Changes in the brush magnet position causes electrical performance changes in the forward and reverse direction. Such changes can also impair proper commutations, which in turn lead to unnecessary brush wear.

Motor installation position :

The motor is designed to be installed, used in shaft horizontal position. To use the motor in the vertical position, special considerations are needed in the bearing and washer designs. Contact Japan Servo, our sales agents or our representatives for details.

Supply voltage :

Please make sure that the motor is used within the rated supply voltage, and avoid surge voltages. Upon special order, the motor can also be manufactured with built-in protection circuitry against surges and reverse polarity. Contact Japan Servo, our sales agents or our representatives for details.

JAPAN SERVO CO.,LTD.
International Sales Department
7 Kanda Mitoshiro-cho, Chiyoda-ku, Tokyo
101-0053 JAPAN
Phone : 03-3292-3507
Fax : 03-3292-3509

PC817 Series

High Density Mounting Type Photocoupler

※ Lead forming type (I type) and taping reel type (P type) are also available. (**PC817I/PC817P**)
※※ TÜV (VDE0884) approved type is also available as an option.

■ Features

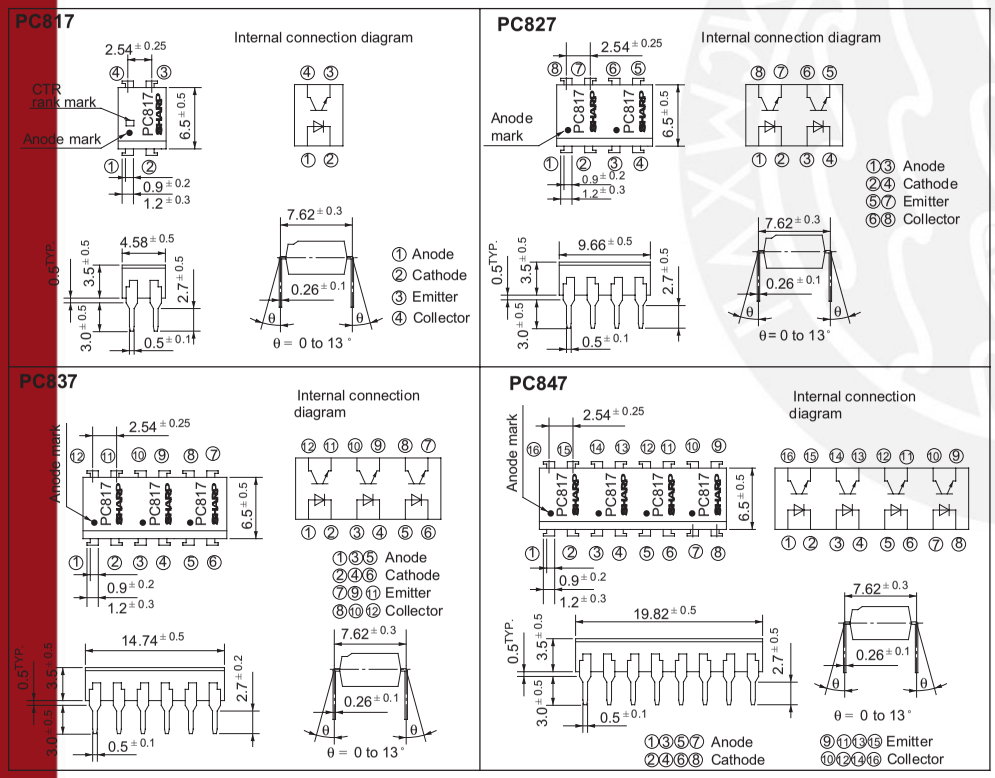
1. Current transfer ratio
   (CTR: MIN. 50% at I_F = 5mA, V_{CE}=5V)
2. High isolation voltage between input and output (V_{iso}: 5 000V_{rms})
3. Compact dual-in-line package
   PC817: 1-channel type
   PC827: 2-channel type
   PC837: 3-channel type
   PC847: 4-channel type
4. Recognized by UL, file No. E64380

■ Applications

1. Computer terminals
2. System appliances, measuring instruments
3. Registers, copiers, automatic vending machines
4. Electric home appliances, such as fan heaters, etc.
5. Signal transmission between circuits of different potentials and impedances

■ Outline Dimensions

(Unit: mm)



■ Absolute Maximum Ratings

(Ta= 25°C)

	Parameter	Symbol	Rating	Unit
Input	Forward current	I_F	50	mA
	*1Peak forward current	I_{FM}	1	A
	Reverse voltage	V_R	6	V
	Power dissipation	P	70	mW
Output	Collector-emitter voltage	V_{CEO}	35	V
	Emitter-collector voltage	V_{ECO}	6	V
	Collector current	I_C	50	mA
	Collector power dissipation	P_C	150	mW
	Total power dissipation	P_{tot}	200	mW
	*2Isolation voltage	V_{iso}	5 000	V_{rms}
	Operating temperature	T_{opr}	- 30 to + 100	°C
	Storage temperature	T_{stg}	- 55 to + 125	°C
	*3Soldering temperature	T_{sol}	260	°C

*1 Pulse width<=100μs, Duty ratio: 0.001
*2 40 to 60% RH, AC for 1 minute
*3 For 10 seconds

■ Electro-optical Characteristics

(Ta= 25°C)

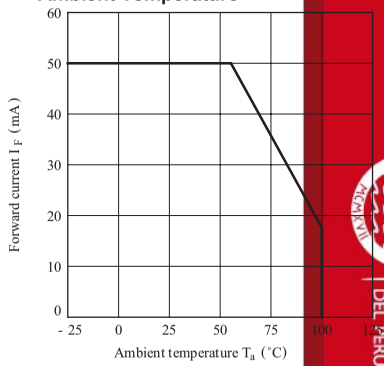
	Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input	Forward voltage		V_F	I_F = 20mA	-	1.2	1.4	V
	Peak forward voltage		V_{FM}	I_{FM} = 0.5A	-	-	3.0	V
	Reverse current		I_R	V_R = 4V	-	-	10	μA
	Terminal capacitance		C_t	V= 0, f= 1kHz	-	30	250	pF
Output	Collector dark current		I_{CEO}	V_{CE} = 20V	-	-	10^{-7}	A
Transfer characteristics	*4Current transfer ratio		CTR	I_F = 5mA, V_{CE} = 5V	50	-	600	%
	Collector-emitter saturation voltage		$V_{CE(sat)}$	I_F = 20mA, I_C = 1mA	-	0.1	0.2	V
	Isolation resistance		R_{ISO}	DC500V, 40 to 60% RH	5×10^{10}	10^{11}	-	Ω
	Floating capacitance		C_f	V= 0, f= 1MHz	-	0.6	1.0	pF
	Cut-off frequency		f_c	V_{CE} = 5V, I_C = 2mA, R_L = 100Ω, - 3dB	-	80	-	kHz
	Response time	Rise time	t_r	V_{CE} = 2V, I_C = 2mA, R_L = 100Ω	-	4	18	μs
		Fall time	t_f		-	3	18	μs

*4 Classification table of current transfer ratio is shown below.

Model No.	Rank mark	CTR (%)
PC817A	A	80 to 160
PC817B	B	130 to 260
PC817C	C	200 to 400
PC817D	D	300 to 600
PC8※7AB	A or B	80 to 260
PC8※7BC	B or C	130 to 400
PC8※7CD	C or D	200 to 600
PC8※7AC	A, B or C	80 to 400
PC8※7BD	B, C or D	130 to 600
PC8※7AD	A, B, C or D	80 to 600
PC8※7	A, B, C, D or No mark	50 to 600

※: 1 or 2 or 3 or 4

Fig. 1 Forward Current vs. Ambient Temperature



FAIRCHILD SEMICONDUCTOR®

www.fairchildsemi.com

KA78XX/KA78XXA

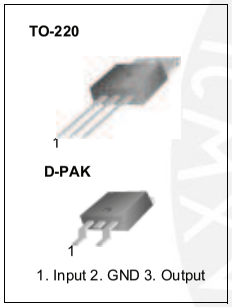
3-Terminal 1A Positive Voltage Regulator

Features

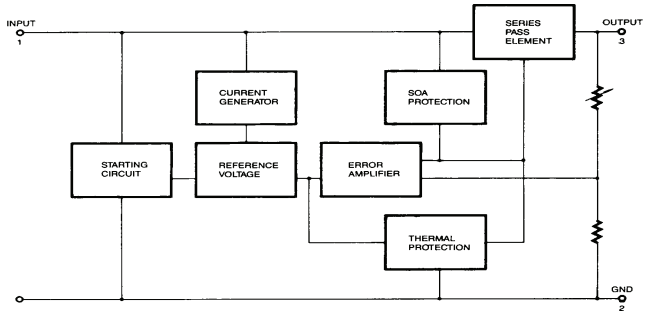
- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

Description

The KA78XX/KA78XXA series of three-terminal positive regulator are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.



Internal Block Digram



Rev. 1.0.0

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Input Voltage (for V_O = 5V to 18V) (for V_O = 24V)	V_I V_I	35 40	V V
Thermal Resistance Junction-Cases (TO-220)	$R_{\theta JC}$	5	°C/W
Thermal Resistance Junction-Air (TO-220)	$R_{\theta JA}$	65	°C/W
Operating Temperature Range (KA78XX/A/R)	T_{OPR}	0 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Electrical Characteristics (KA7805/KA7805R)

(Refer to test circuit ,0°C < T_J < 125°C, I_O = 500mA, V_I =10V, C_I= 0.33µF, C_O=0.1µF, unless otherwise specified)

Parameter	Symbol	Conditions		KA7805 Min.	KA7805 Typ.	KA7805 Max.	Unit
Output Voltage	V_O	T_J =+25 °C		4.8	5.0	5.2	V
		5.0mA ≤ Io ≤ 1.0A, P_O ≤ 15W V_I = 7V to 20V		4.75	5.0	5.25	
Line Regulation (Note1)	Regline	T_J=+25 °C	V_O = 7V to 25V	-	4.0	100	mV
			V_I = 8V to 12V	-	1.6	50	
Load Regulation (Note1)	Regload	T_J=+25 °C	I_O = 5.0mA to1.5A	-	9	100	mV
			I_O =250mA to 750mA	-	4	50	
Quiescent Current	I_Q	T_J =+25 °C		-	5.0	8.0	mA
Quiescent Current Change	ΔI_Q	I_O = 5mA to 1.0A		-	0.03	0.5	mA
		V_I= 7V to 25V		-	0.3	1.3	
Output Voltage Drift	$\Delta V_O/\Delta T$	I_O= 5mA		-	-0.8	-	mV/°C
Output Noise Voltage	V_N	f = 10Hz to 100KHz, T_A=+25 °C		-	42	-	µV/V_O
Ripple Rejection	RR	f = 120Hz V_O = 8V to 18V		62	73	-	dB
Dropout Voltage	V_{Drop}	I_O = 1A, T_J =+25 °C		-	2	-	V
Output Resistance	r_O	f = 1KHz		-	15	-	mΩ
Short Circuit Current	I_{SC}	V_I = 35V, T_A =+25 °C		-	230	-	mA
Peak Current	I_{PK}	T_J =+25 °C		-	2.2	-	A

Note:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

Typical Applications

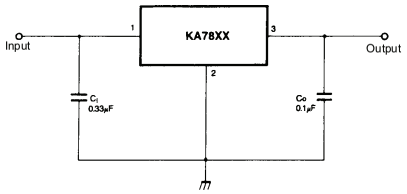


Figure 5. DC Parameters

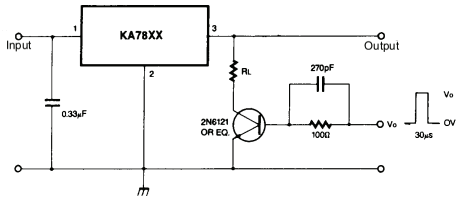


Figure 6. Load Regulation

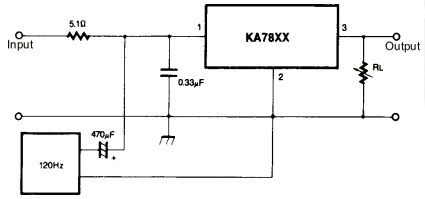


Figure 7. Ripple Rejection

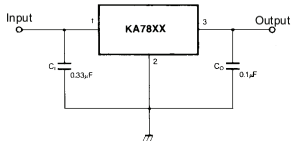


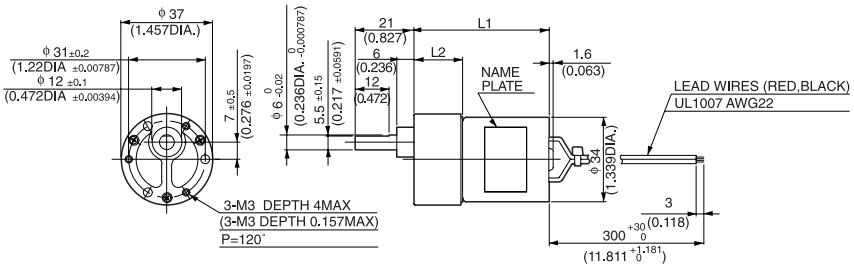
Figure 8. Fixed Output Regulator

WITH GEARBOX

36G

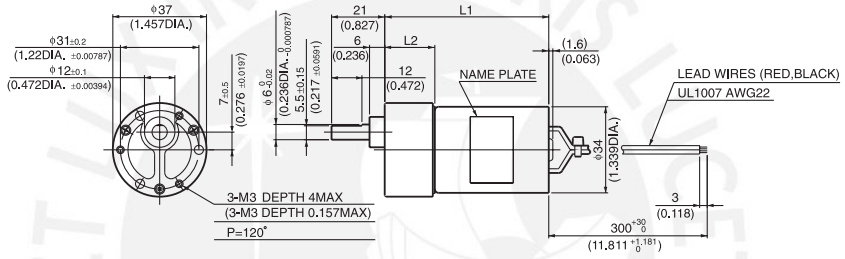
Gear heads for intermittent drive

DME34B36G



GEAR RATIO	L1		L2		WEIGHT	
	(mm)	(inch)	(mm)	(inch)	g	lb
10	54.8	2.157	19.8	0.78	210	0.46
20~30	57.3	2.256	22.3	0.878		
50~100	59.8	2.354	24.8	0.976		
120~300	62.6	2.465	27.3	1.075	230	0.51
400~600	64.8	2.551	29.8	1.173		

DME34K36G



GEAR RATIO	L1		L2		WEIGHT	
	(mm)	(inch)	(mm)	(inch)	g	lb
10	64.8	2.551	19.8	0.78	350	0.77
20~30	67.3	2.669	22.3	0.878		
50~100	69.8	2.748	24.8	0.976		
120~300	72.6	2.858	27.3	1.075	370	0.82
400~600	74.8	2.945	29.8	1.173		

●with 36G TYPE GEARBOX

Model	Gear ratio		10	*18	*20	30	50	60	75	100	*120	*150	*180
	Rated speed	r/min	330	183	165	110	66	55	44	33	27.5	22	18.6
DME34S36G□☆	Rated torque	N·m	0.031	0.052	0.06	0.09	0.12	0.14	0.18	0.25	0.27	0.34	0.39
		oz·in	4.44	7.22	8.33	12.50	18.05	20.83	26.39	36.11	38.88	48.61	55.55
	Rated speed	r/min	370	205	185	123	74	65	54.9	43.4	36.5	30	25.5
DME34B36G□☆	Rated torque	N·m	0.095	0.14	0.16	0.25	0.38	0.39	0.39	0.39	0.39	0.39	0.39
		oz·in	13.47	20.83	23.61	36.11	54.16	55.55	55.55	55.55	55.55	55.55	55.55
	Rated speed	r/min	430	239	215	143	89.0	75.9	62.2	47.7	40.0	32.4	27.2
DME34K36G□B	Rated torque	N·m	0.12	0.19	0.21	0.32	0.39	0.39	0.39	0.39	0.39	0.39	0.39
		oz·in	16.99	26.90	29.73	45.31	55.55	55.55	55.55	55.55	55.55	55.55	55.55

Model	Gear ratio		*200	*250	*300	400	500	600
	Rated speed	r/min	17.2	14.5	12.4	9.5	7.8	6.6
DME34S36G□☆	Rated torque	N·m	0.39	0.39	0.39	0.39	0.39	0.39
		oz·in	55.55	55.55	55.55	55.55	55.55	55.55
	Rated speed	r/min	23.1	18.8	15.8	12	9.6	8.1
DME34B36G□☆	Rated torque	N·m	0.39	0.39	0.39	0.39	0.39	0.39
		oz·in	55.55	55.55	55.55	55.55	55.55	55.55
	Rated speed	r/min	24.6	19.9	16.6	12.5	10.0	8.39
DME34K36G□B	Rated torque	N·m	0.39	0.39	0.39	0.39	0.39	0.39
		oz·in	55.55	55.55	55.55	55.55	55.55	55.55

NOTES 1: On models marked with asterrisks (✻), the direction of the gearbox shaft rotation is in reverse of the motor rorarion direction.
2: In notation model number : fill the reduction ratio denominator in the position marked with the box sign □ ; fill the voltage in the position marked with the star sign ☆.

Features

- High-performance, Low-power AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 130 Powerful Instructions – Most Single-clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
  - On-chip 2-cycle Multiplier
- Nonvolatile Program and Data Memories
  - 8K Bytes of In-System Self-Programmable Flash
    Endurance: 10,000 Write/Erase Cycles
  - Optional Boot Code Section with Independent Lock Bits
    In-System Programming by On-chip Boot Program
    True Read-While-Write Operation
  - 512 Bytes EEPROM
    Endurance: 100,000 Write/Erase Cycles
  - 1K Byte Internal SRAM
  - Programming Lock for Software Security
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescaler, one Compare Mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Three PWM Channels
  - 8-channel ADC in TQFP and QFN/MLF package
    Eight Channels 10-bit Accuracy
  - 6-channel ADC in PDIP package
    Eight Channels 10-bit Accuracy
  - Byte-oriented Two-wire Serial Interface
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Five Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, and Standby
- I/O and Packages
  - 23 Programmable I/O Lines
  - 28-lead PDIP, 32-lead TQFP, and 32-pad QFN/MLF
- Operating Voltages
  - 2.7 - 5.5V (ATmega8L)
  - 4.5 - 5.5V (ATmega8)
- Speed Grades
  - 0 - 8 MHz (ATmega8L)
  - 0 - 16 MHz (ATmega8)
- Power Consumption at 4 Mhz, 3V, 25°C
  - Active: 3.6 mA
  - Idle Mode: 1.0 mA
  - Power-down Mode: 0.5 µA

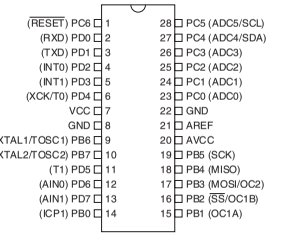
8-bit AVR® with 8K Bytes In-System Programmable Flash

ATmega8
ATmega8L

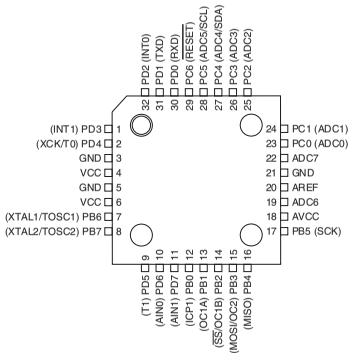
2486P–AVR–02/06

Pin Configurations

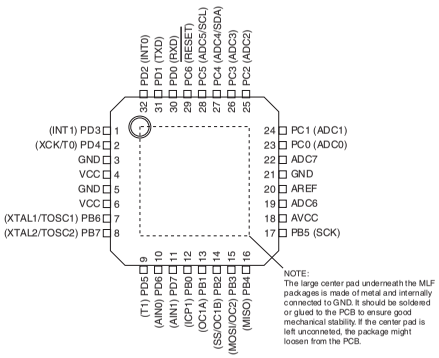
PDIP



TQFP Top View



MLF Top View



NOTE:
The large center pad underneath the MLF packages is made of metal and internally connected to GND. It should be soldered or glued to the PCB to ensure good mechanical stability. If the center pad is left unconnected, the package might loosen from the PCB.

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega8 provides the following features: 8K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes of EEPROM, 1K byte of SRAM, 23 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, a 6-channel ADC (eight channels in TQFP and QFN/MLF packages) with 10-bit accuracy, a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next Interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The Flash Program memory can be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash Section will continue to run while the Application Flash Section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega8 is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many embedded control applications.

The ATmega8 AVR is supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, In-Circuit Emulators, and evaluation kits.

Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

General Purpose Register File

The Zero Flag Z indicates a zero result in an arithmetic or logic operation. See the "Instruction Set Description" for detailed information.

- **Bit 0 – C: Carry Flag**

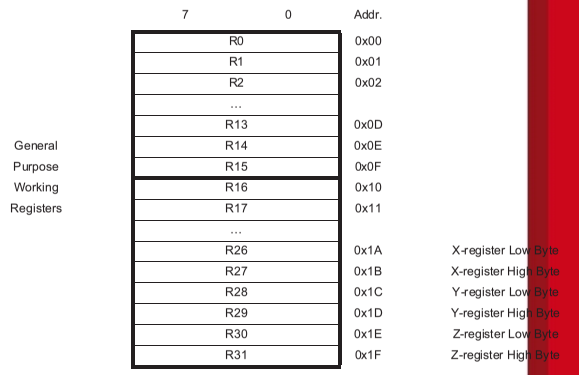
The Carry Flag C indicates a Carry in an arithmetic or logic operation. See the "Instruction Set Description" for detailed information.

The Register File is optimized for the AVR Enhanced RISC instruction set. In order to achieve the required performance and flexibility, the following input/output schemes are supported by the Register File:

- One 8-bit output operand and one 8-bit result input.
- Two 8-bit output operands and one 8-bit result input.
- Two 8-bit output operands and one 16-bit result input.
- One 16-bit output operand and one 16-bit result input.

Figure 3 shows the structure of the 32 general purpose working registers in the CPU.

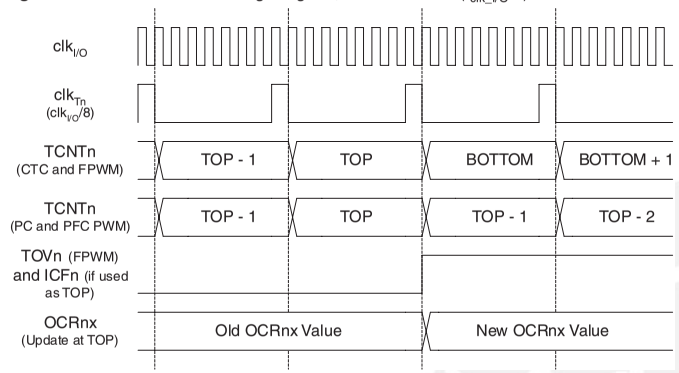
Figure 3. AVR CPU General Purpose Working Registers



Most of the instructions operating on the Register File have direct access to all registers, and most of them are single cycle instructions.

As shown in Figure 3, each register is also assigned a Data memory address, mapping them directly into the first 32 locations of the user Data Space. Although not being physically implemented as SRAM locations, this memory organization provides great flexibility in access of the registers, as the X-, Y-, and Z-pointer Registers can be set to index any register in the file.

Figure 44. Timer/Counter Timing Diagram, with Prescaler ($f_{clk\_I/O}/8$)



16-bit Timer/Counter Register Description

Timer/Counter 1 Control Register A – TCCR1A

Bit	7	6	5	4	3	2	1	0	
	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	TCCR1A
Read/Write	R/W	R/W	R/W	R/W	W	W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7:6 – COM1A1:0: Compare Output Mode for channel A**
- **Bit 5:4 – COM1B1:0: Compare Output Mode for channel B**

The COM1A1:0 and COM1B1:0 control the Output Compare Pins (OC1A and OC1B respectively) behavior. If one or both of the COM1A1:0 bits are written to one, the OC1A output overrides the normal port functionality of the I/O pin it is connected to. If one or both of the COM1B1:0 bit are written to one, the OC1B output overrides the normal port functionality of the I/O pin it is connected to. However, note that the *Data Direction Register* (DDR) bit corresponding to the OC1A or OC1B pin must be set in order to enable the output driver.

When the OC1A or OC1B is connected to the pin, the function of the COM1x1:0 bits is dependent of the WGM13:0 bits setting. Table 36 shows the COM1x1:0 bit functionality when the WGM13:0 bits are set to a normal or a CTC mode (non-PWM).

Table 36. Compare Output Mode, Non-PWM

COM1A1/ COM1B1	COM1A0/ COM1B0	Description
0	0	Normal port operation, OC1A/OC1B disconnected.
0	1	Toggle OC1A/OC1B on Compare Match
1	0	Clear OC1A/OC1B on Compare Match (Set output to low level)
1	1	Set OC1A/OC1B on Compare Match (Set output to high level)

Timer/Counter 1 Control Register B – TCCR1B

Bit	7	6	5	4	3	2	1	0	
	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	TCCR1B
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – ICNC1: Input Capture Noise Canceler**

Setting this bit (to one) activates the Input Capture Noise Canceler. When the noise canceler is activated, the input from the Input Capture Pin (ICP1) is filtered. The filter function requires four successive equal valued samples of the ICP1 pin for changing its output. The Input Capture is therefore delayed by four Oscillator cycles when the noise canceler is enabled.

- **Bit 6 – ICES1: Input Capture Edge Select**

This bit selects which edge on the Input Capture Pin (ICP1) that is used to trigger a capture event. When the ICES1 bit is written to zero, a falling (negative) edge is used as trigger, and when the ICES1 bit is written to one, a rising (positive) edge will trigger the capture.

When a capture is triggered according to the ICES1 setting, the counter value is copied into the Input Capture Register (ICR1). The event will also set the Input Capture Flag (ICF1), and this can be used to cause an Input Capture Interrupt, if this interrupt is enabled.

When the ICR1 is used as TOP value (see description of the WGM13:0 bits located in the TCCR1A and the TCCR1B Register), the ICP1 is disconnected and consequently the Input Capture function is disabled.

- **Bit 5 – Reserved Bit**

This bit is reserved for future use. For ensuring compatibility with future devices, this bit must be written to zero when TCCR1B is written.

- **Bit 4:3 – WGM13:2: Waveform Generation Mode**

See TCCR1A Register description.

- **Bit 2:0 – CS12:0: Clock Select**

The three clock select bits select the clock source to be used by the Timer/Counter, see Figure 41 and Figure 42.

Table 40. Clock Select Bit Description

CS12	CS11	CS10	Description
0	0	0	No clock source. (Timer/Counter stopped)
0	0	1	$clk_{I/O}/1$ (No prescaling)
0	1	0	$clk_{I/O}/8$ (From prescaler)
0	1	1	$clk_{I/O}/64$ (From prescaler)
1	0	0	$clk_{I/O}/256$ (From prescaler)
1	0	1	$clk_{I/O}/1024$ (From prescaler)
1	1	0	External clock source on T1 pin. Clock on falling edge.
1	1	1	External clock source on T1 pin. Clock on rising edge.

8-bit Timer/Counter Register Description

Timer/Counter Control Register – TCCR2

Bit	7	6	5	4	3	2	1	0	
	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	TCCR2
Read/Write	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – FOC2: Force Output Compare**

The FOC2 bit is only active when the WGM bits specify a non-PWM mode. However, for ensuring compatibility with future devices, this bit must be set to zero when TCCR2 is written when operating in PWM mode. When writing a logical one to the FOC2 bit, an immediate Compare Match is forced on the waveform generation unit. The OC2 output is changed according to its COM21:0 bits setting. Note that the FOC2 bit is implemented as a strobe. Therefore it is the value present in the COM21:0 bits that determines the effect of the forced compare.

A FOC2 strobe will not generate any interrupt, nor will it clear the timer in CTC mode using OCR2 as TOP.

The FOC2 bit is always read as zero.

- **Bit 6,3 – WGM21:0: Waveform Generation Mode**

These bits control the counting sequence of the counter, the source for the maximum (TOP) counter value, and what type of waveform generation to be used. Modes of operation supported by the Timer/Counter unit are: Normal mode, Clear Timer on Compare Match (CTC) mode, and two types of Pulse Width Modulation (PWM) modes. See Table 42 and “Modes of Operation” on page 110.

Table 42. Waveform Generation Mode Bit Description

Mode	WGM21 (CTC2)	WGM20 (PWM2)	Timer/Counter Mode of Operation[1]	TOP	Update of OCR2	TOV2 Flag Set
0	0	0	Normal	0xFF	Immediate	MAX
1	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	1	0	CTC	OCR2	Immediate	MAX
3	1	1	Fast PWM	0xFF	TOP	MAX

Note: 1. The CTC2 and PWM2 bit definition names are now obsolete. Use the WGM21:0 definitions. However, the functionality and location of these bits are compatible with previous versions of the timer.

- **Bit 5:4 – COM21:0: Compare Match Output Mode**

These bits control the Output Compare Pin (OC2) behavior. If one or both of the COM21:0 bits are set, the OC2 output overrides the normal port functionality of the I/O pin it is connected to. However, note that the Data Direction Register (DDR) bit corresponding to OC2 pin must be set in order to enable the output driver.

When OC2 is connected to the pin, the function of the COM21:0 bits depends on the WGM21:0 bit setting. Table 43 shows the COM21:0 bit functionality when the WGM21:0 bits are set to a normal or CTC mode (non-PWM).

PD-93991C

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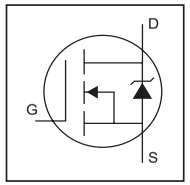
AUTOMOTIVE MOSFET

IRF1405

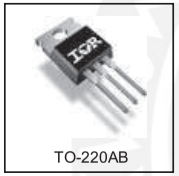
HEXFET® Power MOSFET



V_{DSS} = 55V

$R_{DS(on)}$ = 5.3mΩ

I_D = 169A⑥



TO-220AB

Typical Applications

- Electric Power Steering (EPS)
- Anti-lock Braking System (ABS)
- Wiper Control
- Climate Control
- Power Door

Benefits

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

Description

Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	169⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	118⑥	
I_{DM}	Pulsed Drain Current ①	680	
P_D @T_C = 25°C	Power Dissipation	330	W
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	560	mJ
I_{AR}	Avalanche Current	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy⑦		mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

8/26/03

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.057	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	4.6	5.3	mΩ	V_{GS} = 10V, I_D = 101A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = 10V, I_D = 250µA
g_{fs}	Forward Transconductance	69	—	—	S	V_{DS} = 25V, I_D = 110A
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 55V, V_{GS} = 0V
		—	—	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -20V
Q_g	Total Gate Charge	—	170	260	nC	I_D = 101A
Q_{gs}	Gate-to-Source Charge	—	44	66		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	62	93		V_{GS} = 10V④
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	V_{DD} = 38V
t_r	Rise Time	—	190	—		I_D = 110A
$t_{d(off)}$	Turn-Off Delay Time	—	130	—		R_G = 1.1Ω
t_f	Fall Time	—	110	—		V_{GS} = 10V ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	5480	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	1210	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	280	—		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	—	5210	—		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	—	900	—		V_{GS} = 0V, V_{DS} = 44V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤	—	1500	—		V_{GS} = 0V, V_{DS} = 0V to 44V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	169⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	680		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 101A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	88	130	ns	T_J = 25°C, I_F = 101A
Q_{rr}	Reverse RecoveryCharge	—	250	380	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Starting T_J = 25°C, L = 0.11mH R_G = 25Ω, I_{AS} = 101A. (See Figure 12).

③ I_{SD} ≤ 101A, di/dt ≤ 210A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

⑦ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

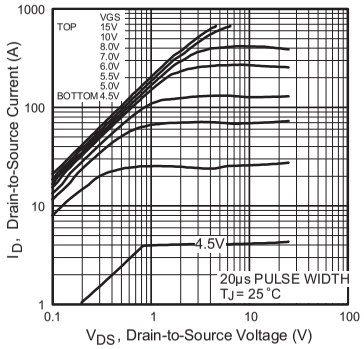

Fig 1. Typical Output Characteristics

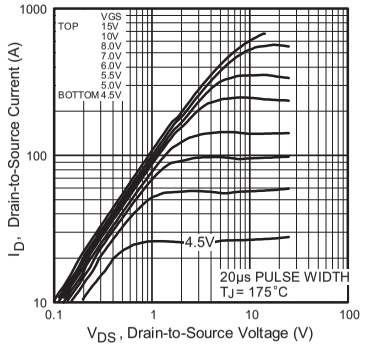

Fig 2. Typical Output Characteristics

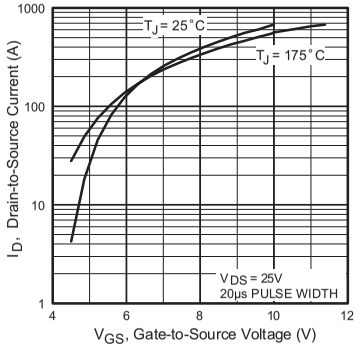

Fig 3. Typical Transfer Characteristics

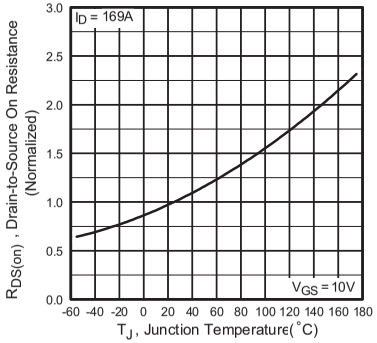

Fig 4. Normalized On-Resistance Vs. Temperature

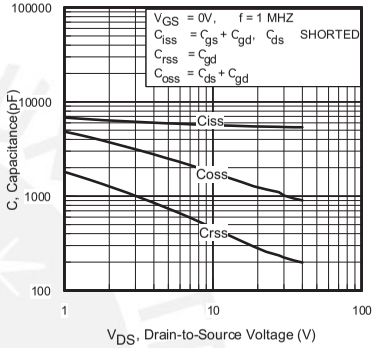

Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

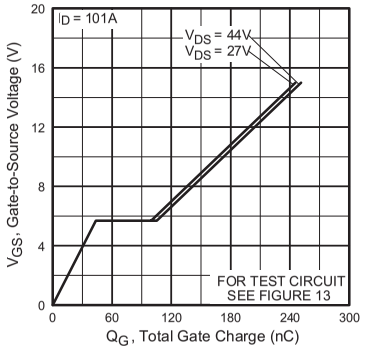

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

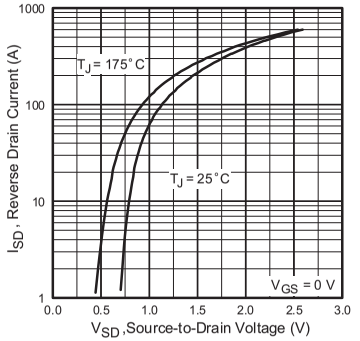

Fig 7. Typical Source-Drain Diode Forward Voltage

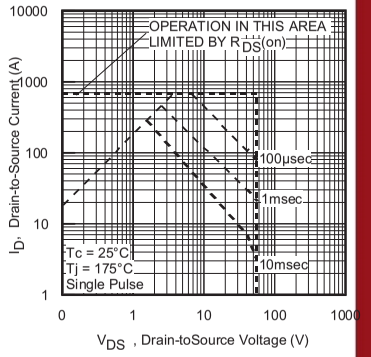

Fig 8. Maximum Safe Operating Area

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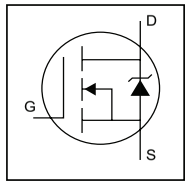
PD-91279E

IRF3205

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 55V

$R_{DS(on)}$ = 8.0mΩ

I_D = 110A⑤

TO-220AB

Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	110 ⑤	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	80	
I_{DM}	Pulsed Drain Current ①	390	
P_D @T_C = 25°C	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current①	62	A
E_{AR}	Repetitive Avalanche Energy①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.75	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.057	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	8.0	mΩ	V_{GS} = 10V, I_D = 62A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	44	——	——	S	V_{DS} = 25V, I_D = 62A④
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	µA	V_{DS} = 55V, V_{GS} = 0V
		——	——	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
Q_g	Total Gate Charge	——	——	146	nC	I_D = 62A
Q_{gs}	Gate-to-Source Charge	——	——	35		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	54		V_{GS} = 10V, See Fig. 6 and 13
$t_{d(on)}$	Turn-On Delay Time	——	14	——	ns	V_{DD} = 28V
t_r	Rise Time	——	101	——		I_D = 62A
$t_{d(off)}$	Turn-Off Delay Time	——	50	——		R_G = 4.5Ω
t_f	Fall Time	——	65	——		V_{GS} = 10V, See Fig. 10 ④
L_D	Internal Drain Inductance	——	4.5	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	——	7.5	——		
C_{iss}	Input Capacitance	——	3247	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	781	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	211	——		ƒ = 1.0MHz, See Fig. 5
E_{AS}	Single Pulse Avalanche Energy②	——	1050⑥	264⑦	mJ	I_{AS} = 62A, L = 138µH

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	110	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)①	——	——	390		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 62A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	69	104	ns	T_J = 25°C, I_F = 62A
Q_{rr}	Reverse Recovery Charge	——	143	215	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 138µH R_G = 25Ω, I_{AS} = 62A. (See Figure 12)

③ I_{SD} ≤ 62A, di/dt ≤ 207A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

⑥ This is a typical value at device destruction and represents operation outside rated limits.

⑦ This is a calculated value limited to T_J = 175°C.

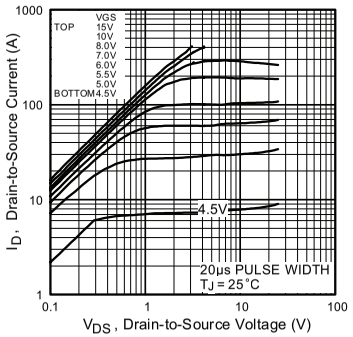


Fig 1. Typical Output Characteristics

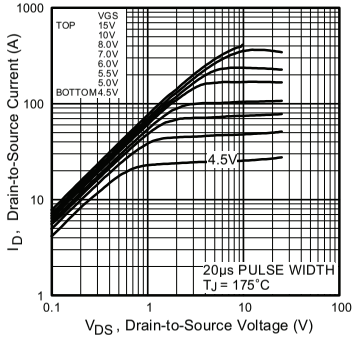


Fig 2. Typical Output Characteristics

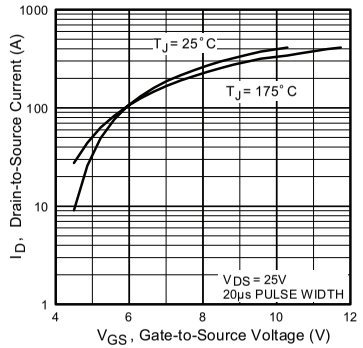


Fig 3. Typical Transfer Characteristics

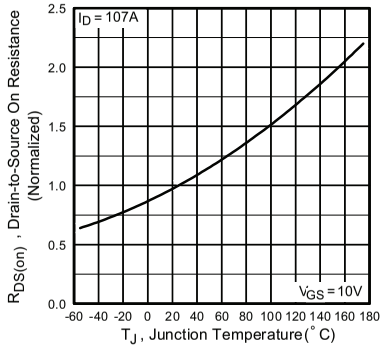


Fig 4. Normalized On-Resistance Vs. Temperature

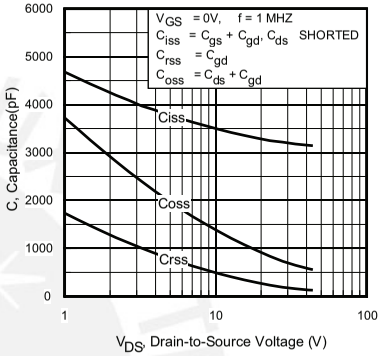


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

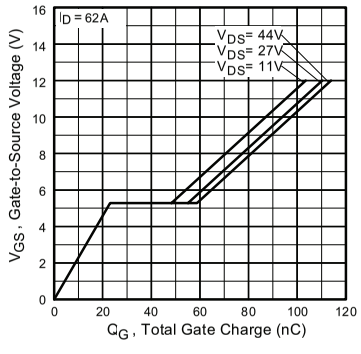


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

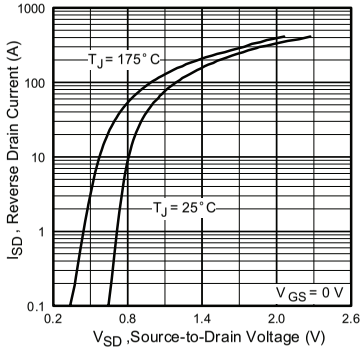


Fig 7. Typical Source-Drain Diode Forward Voltage

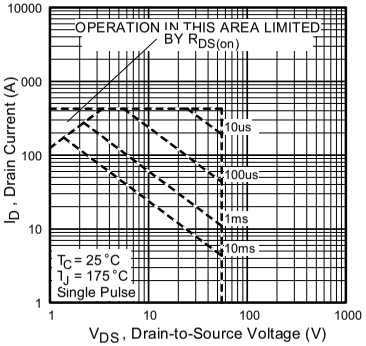


Fig 8. Maximum Safe Operating Area

```
CODIGO DEL TEMA DE TESIS:

; *****************************************************
; BASIC .ASM template file for AVR
; *****************************************************

.include "C:\VMLAB\include\m8def.inc"

; Se define aqui las variable
;
.def  temp  =r16

; Se define el reinicio y los vectores de interrupción,
;
Reinicio:
   rjmp inicio
   rjmp int_INT0      ; Addr $01
        rjmp int_INT1      ; Addr $02
   reti      ; Addr $03
   reti      ; Addr $04
   reti      ; Addr $05
   RJMP INT_OC1A   ;    Usar 'rjmp myVector'
   reti      ; Addr $07        a definir vector de interrupción
   RJMP OVERFLOW; Addr $08
   reti      ; Addr $09
   reti      ; Addr $0A
   reti      ; Addr $0B       Esto es solo un ejemplo
   reti      ; Addr $0C        No todos los MCUs tienen que ser el

mismo
   reti      ; Addr $0D        numero de vectores de interrupción
   reti      ; Addr $0E
   reti      ; Addr $0F
   reti      ; Addr $10

; programa inicia despues del reinicio.
;

INT_OC1A:
     CBI portb,4
     RETI

OVERFLOW:
     SBI portb,4
     RETI
;//////////////////INTERRUPCIÓN UP DOWN

////////////////////////////////////////////
int_INT0:    ; entrada del encoder del motor de ELEVACIÓN
push r17               ;R20, R21, R24, R25, R26
in r17,sreg
push r17
PUSH R16
PUSH R18
PUSH R30
PUSH R31
           cpi r20, $04        ; r20 es el contador inicial cuando

llega a 4 recien entra
           brne cuenta
                ldi r20,$01      ; reinicio el contador r20
                     cpi r25,1        ; r25 =1  up
                 brne down            ;r25 =0 down
                       cpi r21,$b4    ; $b4 =180 grados
                       breq cambio1
                       inc r21         ; sino llego a 180 entonces se

aumenta la cuenta en 1
                       ldi r26,1
                  rjmp endi
```



```
                down:
                       cpi r21,$00
                       breq cambio2
                       dec r21
                       ldi r24,1
                  rjmp endi
          cuenta:
           inc r20
           rjmp endi2
          cambio1:
                 ldi r24,0
                 rjmp endi2      ; llego al maximo 0 grados
          cambio2:
                 ldi r26,0       ; llego al maximo 180 grados
                 rjmp endi2
endi:
convertir:
           ldi r31,0  ;CONTADOR_TXTXTXTXTX
                           ldi r30,$30
                 mov r18, r21
revisar:
                  cpi r18, $0a
          brlo gogo
          subi r18,$0a
          inc r31
          rjmp revisar
    gogo:
                 cpi r31,$0a
                 brlo fin111
                 subi r31,$0a
                 ldi r16,1
                 rjmp finn22
     fin111:
              ldi r16,0
     finn22:
                   add r18,r30
          add r16,r30
          add r31,r30
txbyte:
          sbis    UCSRA, UDRE
          rjmp    txbyte
          out     UDR, r16
tx2:
          sbis    UCSRA, UDRE
          rjmp    tx2
          out     UDR, r31
tx3:
          sbis    UCSRA, UDRE
          rjmp    tx3
          out     UDR, r18
endi2:
POP R31
POP R30
POP R18
POP R16
pop r17
out sreg,r17
pop r17
RETI
;//////////////////INTERRUPCIÓN GIRO

////////////////////////////////////////////
int_INT1:    ; entrada del encoder del motor de giro

push r16                  ;r19, r22, r23, r27, r28, r29
in r16,sreg
push r16
      cpi r19, $04        ; r19 es el contador inicial cuando llega a

4 recien entra
           brne cuenta2
```

```
                ldi r19,$01      ; reinicio el contador r20
                       cpi r30,1        ; r30 =1 derecha
                 brne izquierda                 ;r30 =0 izquierda
                       cpi r22,0    ;
                       breq otro1
                       dec r22         ;
                       ldi r23,1
                   rjmp comparar

                 izquierda:
                       cpi r21,$FE   ; se compara con 254  = $FE es
el maximo
                       breq otro2
                       inc r22
                       ldi r27,1
comparar:
        cpi r22, $7f
        brsh  izq1
             mov r29,r28
             sub r29,r22
             rjmp chau
        izq1:
             cpi r22,$7f
             breq chauj
             mov r29,r22
             sub r29,r28
             rjmp chau

         cuenta2:
          inc r19
          rjmp chau2
         otro1:
                ldi r27,0
                rjmp  chau2     ; llego al maximo 0 grados
         otro2:
                ldi r23,0       ; llego al maximo 180 grados
                rjmp  chau2
chauj:
        mov r29,r22
        sub r29,r28
           chau  :

RCALL CONVERTIR2     ; entrada r29

chau2:
pop r16
out sreg,r16
pop r16

RETI
;CONFIGURACIONES DE LOS PUERTOS DEL

MICROCONTROLADOR////////////////////////////////////
        CONFIG_PUERTOS:     ; configurará puertos de salida y entrada
                    LDI  R16,$FF   ; PUERTO B COMO SALIDA DE LAS PWM
                         OUT DDRB, R16    ; puerto C y D estan como

entradas
                ret
; CONFOGURACIÓN DE LA SENAL

PWM/////////////////////////////////////////////////////
        CONFIG_PWM:   ; configuración PWM rapido 10 bits ......pre-

escalador 1 .......
      ; timer 1=====================
        Ldi r16, (1<<WGM10) ; MODO PUESTA A CERO.......   COM1A1 =0

COM1A0=1
                   OUT  TCCR1A, R16
```



```
                         LDI R16, 0b00001001  ; PRE ESCALADOR 1    PWM
RAPIDO DE 8 BITS
                         OUT TCCR1B, R16
                         LDI R16, 0b00000000
                         OUT TIMSK, R16
                ; timer 2  ========================
                         ldi r17, 0b01001001
        out tccr2,r17

   RET
;CONFIGURACIÓN DE LA INTERRUPCIONES (EXTERNAS

)//////////////////////////////
CONFIG_INTERRUP:
                         ldi r16, 0b00000101  ; configuración de int
externa
                         out MCUCR, R16
                         ldi r16, 0b11000000  ;habilitar interrupciones
externes into int1
                         out GICR, R16
        RET
;CONFIGURACIONES DEL USART

//////////////////////////////////////////////////////////
   CONFIG_USART:
          ldi     r16, high(12)
                  out     UBRRH, r16
                  ldi     r16, low(12)
                  out     UBRRL, r16              ; velocidad: 9600bps
con U2X=1
                  ldi     r16, 1<<U2X
                  out     UCSRA, r16
                  ldi     r16, 1<<TXEN
                  out     UCSRB, r16
        RET


;INICIO//////////////////////////////////////////////////////////////

//////////////
INICIO:
      LDI R16, HIGH (RAMEND); CONFIGURO PILA
           OUT SPH, R16
           LDI R16, LOW (RAMEND)  ; se configura la pila para las
INTERRUPCIONES
           OUT SPL, R16



                RCALL   CONFIG_PUERTOS
                RCALL CONFIG_USART
                RCALL CONFIG_PWM
                RCALL CONFIG_INTERRUP   ;/////////////////usart de l
usart
;       ldi     ZH, high(Mensaje*2)
;       ldi     ZL, low(Mensaje*2)


   ldi r20,1     ; valores iniciales para la interrupción esterna up-
down
   ldi r24,1
   ldi r26,1
   ldi r21,0
```

```
                                ldi r19,1        ; valores iniciales

para a interrupción extena izq-der
                                ldi r22, $7f
                                ldi r23,1
                                ldi r27,1
                                ldi r28,$7f
                                ldi r29,0
                SEI


; SUBRUTINA PARA LA VELOCIDAD

////////////////////////////////////////////////////
VELOCIDAD:
          UNO:
        IN R16,PINC             ; SE COMPARA SI EL SWITCH 1 ESTA EN ON
                ANDI R16, 0b00010000
           CPI  R16, 0b00000000    ;SE ENMASCARA Y SE VERIFICA SI EL

PIN PC4 ESTA EN NIVEL '0'
             BRnE        DOS
      LDI R16,low ($003F)   ; velocidad con ciclo de trabajo al 25%
      OUT OCR1AL, R16
      OUT OCR1BL, R16
      OUT  OCR2,R16
      RJMP PULSADOR_ACCION

    DOS:
      IN R16,PINC             ; SE COMPARA SI EL SWITCH 2 ESTA EN ON
                ANDI R16, 0b00100000
           CPI  R16, 0b00000000    ;SE ENMASCARA Y SE VERIFICA SI EL

PIN PC5 ESTA EN NIVEL '0'
             BRnE V_NORMAL
      LDI R16,low ($00BF)     ; velocidad con ciclo de trabajo al 75%
      OUT OCR1Al, R16
      OUT OCR1BL, R16
      OUT  OCR2,R16
      RJMP PULSADOR_ACCION

    V_NORMAL:
      LDI R16,low ($007F)
      OUT OCR1AL, R16
      OUT OCR1BL, R16
      OUT  OCR2,R16

  PULSADOR_ACCION :

  RCALL MANDO


RJMP VELOCIDAD


MANDO:

uno1:
      in r17, pinc
                andi r17, 0b00000001
                cpi r17,0b00000000
                brne  fin
                                cpi r24,1   ;encoder
                                brne fin          ;encoder
                in r18, TCCR1A
                                ori r18,0b10000000
                           OUT  TCCR1A, R18
                                          ldi r25,1  ;encoder
                rjmp dos2
                fin:
                                in  r16, TCCR1A
```



```
                                andi r16,0b01111111
                                OUT  TCCR1A, R16
                                sbi ddrb,1
                                cbi portb,1
dos2:
                in r17, pinc
                andi r17, 0b00000010
                cpi r17,0b00000000
                brne  finn2
                                cpi r26 ,1   ;encoder
                                brne finn2   ;encoder
                                in r18, TCCR1A
                                ori r18,0b00100000
                                OUT  TCCR1A, R18
                                                        ldi r25,0

;encoder
                RJMP tres3
                finn2:
                          in  r16, TCCR1A
                          andi r16,0b11011111
                     OUT  TCCR1A, R16
                          sbi ddrb,2
             cbi portb,2
tres3:
          in r17, pinc
                andi r17, 0b00000100
                cpi r17,0b00000000
                brne fin3
                     cpi r23,1   ;enoder 2
                     brne fin3     ;encoder 2
                      in r16,tccr2
                      ori r16, 0b00100000
                      out tccr2,r16
                      ldi  r30,0   ;encoder2
           rjmp  cuatro4
           fin3:
          in r16,tccr2
            andi r16, 0b11011111
            out tccr2,r16
           sbi ddrb ,3
         cbi portb,3

cuatro4:
        in r17, pinc
          andi r17, 0b00001000
            cpi r17,0b00000000
            brne fin4
                                cpi  r27,1 ;encoder2
                                brne fin4    ;encoder2
                                 ldi r16, 0b00010100
                                 out timsk,r16
                                 ldi r30,1; encoder 2
        rjmp    finito
        fin4:
                 ldi r16, 0b00000000
                 out timsk,r16
                 sbi ddrb,4
                 cbi portb,4
FINITO:
RET



CONVERTIR2:  ;r19, r22, r23, r27
push r19
push r22
push r27
push r23
```

```
    ldi r19,0  ;CONTADOR TXTXTXTXTX
   ldi r27,$30
     mov r22, r29
        revisarsh:
         cpi r22, $0a
         brlo gogo2
         subi r22,$0a
         inc r19
         rjmp revisarsh
  gogo2:
                cpi r19,$0a
                brlo fincho
                subi r19,$0a
                ldi r23,1
                rjmp finn2cho
  fincho:
         ldi r23,0
 finn2cho:
                  add r19,r27
        add r22,r27
        add r23,r27

tx42:
        sbis    UCSRA, UDRE
        rjmp    tx42
push r16
ldi r16, 13
        out     UDR, r16
        pop r16
txbyte2:
        sbis    UCSRA, UDRE
        rjmp    txbyte2
        out     UDR, r23
tx22:
        sbis    UCSRA, UDRE
        rjmp    tx22
        out     UDR, r19
tx32:
        sbis    UCSRA, UDRE
        rjmp    tx32
        out     UDR, r22


pop r23
pop r27
pop r22
pop r19

RET
```

PRJ DEL PROGRAMA DE TEMA DE TESIS:

```
; ************************************************************
; Proyecto: Tesis de ingenieria electrÓnica
; ************************************************************

; Micro + software running
; ------------------------------------------------------------
.MICRO "ATmega8"
.PROGRAM "lunes14.asm"
.TARGET "lunes14.hex"

.TRACE              ;

; Las siguientes lineas son opcionales;
; ------------------------------------------------------------
.POWER VDD=5 VSS=0  ; Power nodes
.CLOCK 1meg         ; Micro clock
.STORE 250m         ; Trace (micro+signals) storage time

; Micro nodes: RESET, AREF, PB0-PB7, PC0-PC6, PD0-PD7, ACO, TIM1OVF,

ADC6, ADC7
; Se defina aqui el "hardware"
; ------------------------------------------------------------


K0 vss pc0  LATCHED
r1 pc0 vdd 10k
K1 vss pc1     LATCHED
r2 pc1 vdd 10k
K2 vss pc2     LATCHED
r3 pc2 vdd 10k
K3 vss pc3    LATCHED
r4 pc3 vdd 10k

K4 vss pc4                    latched
r5 pc4 vdd 10k
K5 vss pc5        latched
r6 pc5 vdd 10k

K7 vss pd2    LATCHED ; para el int0
r7 pd2 vdd 10k
K8 vss pd3    LATCHED ; para el int1
r8 pd3 vdd 10k

X1  TTY(9600 8 0 0 1 1) PD0 PD1
.plot V(PB1)
.plot V(PB2)
.plot V(PB3)
```