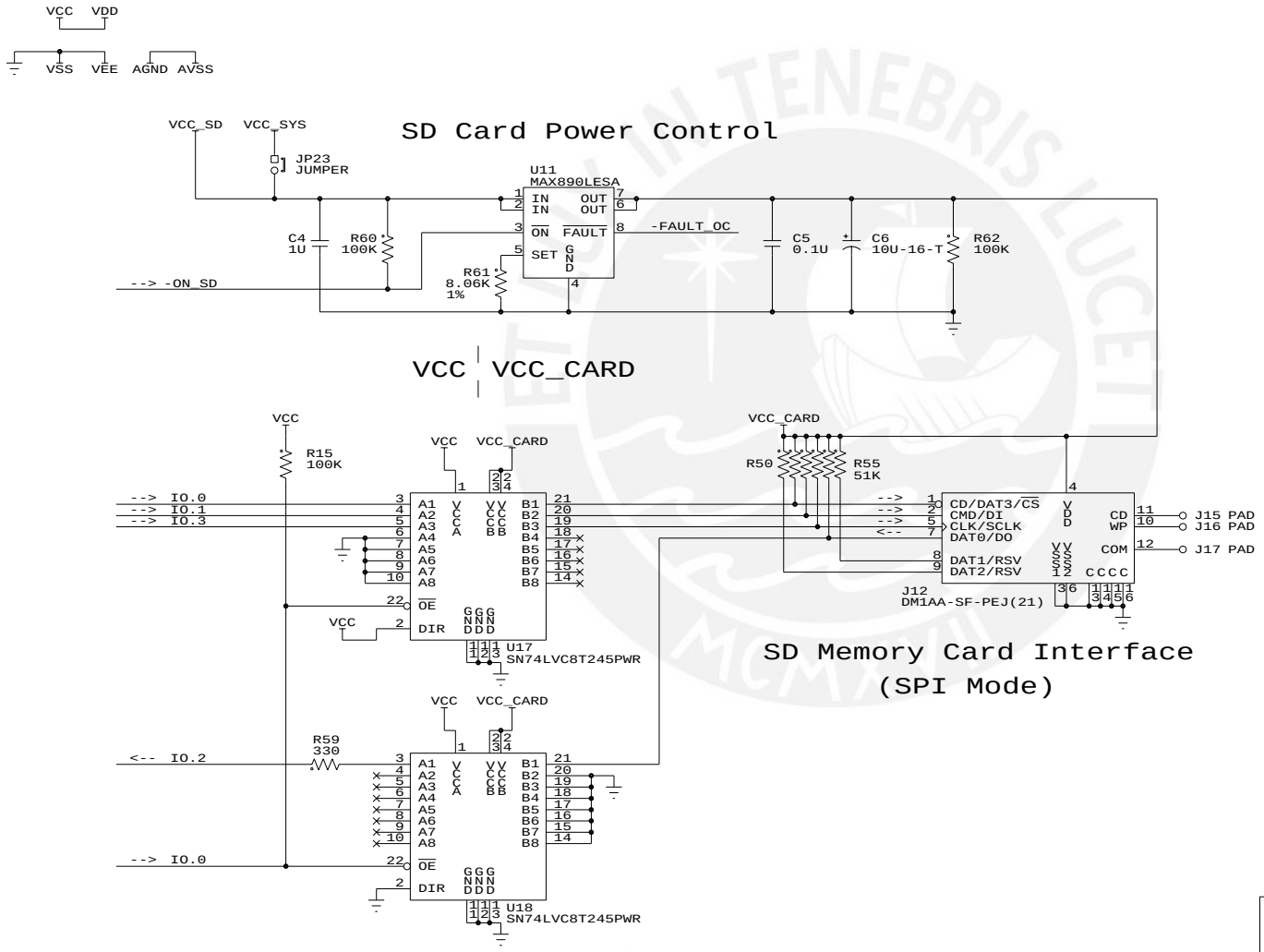
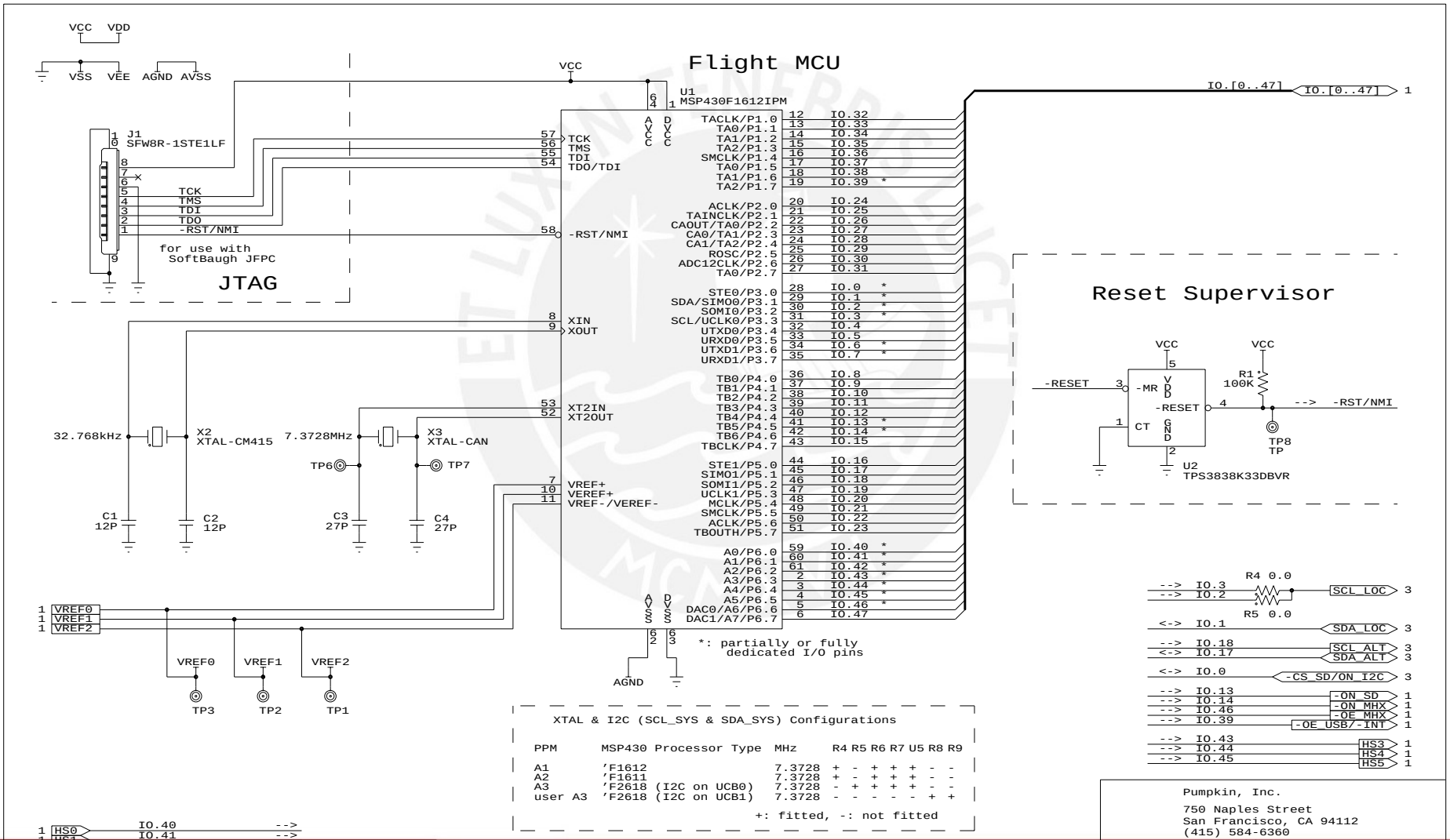


Pumpkin, Inc.
750 Naples Street
San Francisco, CA 94112
(415) 584-6360
www.pumpkininc.com

Title		
CubeSat Kit Development Board		
Size: B	Document Number: 00194D-4.SCH	REV: D
Date: December 27, 2008	Sheet 4 of 10	



XTAL & I2C (SCL_SYS & SDA_SYS) Configurations

PPM	MSP430 Processor Type	MHz	R4	R5	R6	R7	U5	R8	R9
A1	'F1612	7.3728	+	-	+	+	+	-	-
A2	'F1611	7.3728	+	-	+	+	+	-	-
A3	'F2618 (I2C on UCB0)	7.3728	-	+	+	+	+	-	-
user A3	'F2618 (I2C on UCB1)	7.3728	-	-	-	-	-	+	+

+: fitted, -: not fitted

Notes:

1. R4 for USART0 module, R5 for USCI0 module.

Pumpkin, Inc.
750 Naples Street
San Francisco, CA 94112
(415) 584-6360
www.pumpkininc.com

Title		
CubeSat Kit Plugg. Proc. Mod. A (PPM A)		
Size: B	Document Number: 00378B-2.SCH	REV: B
Date: April 6, 2009	Sheet 2 of 4	

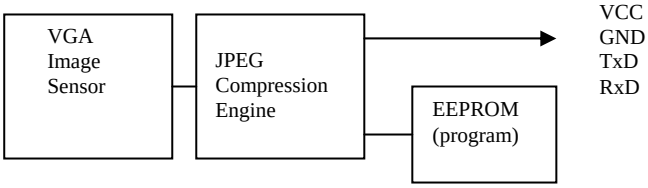
COMedia Ltd.
康大科技有限公司

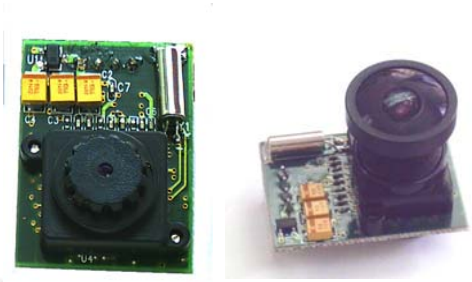
C328-7640
JPEG Camera Module W/ UART Interface

General Description

The C328-7640 is VGA camera module performs as a JPEG compressed still camera and can be attached to a wireless or PDA host. Users can send out a snapshot command from the host in order to capture a full resolution single-frame still picture. The picture is then compressed by the JPEG engine and transferred to the host thru serial port.

Block Diagram





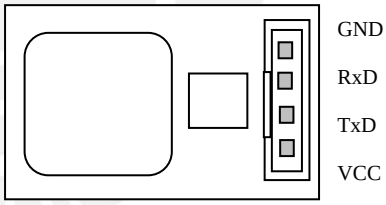
Features

- Small in size, 20x28mm
- VGA resolution, down sample to QVGA or CIF
- 3.3V operation
- Low power consumption 60mA
- User friendly commands to control the module
- UART interface of up to 115.2Kbps
- Auto detect baud rate and make connection to the host
- Power saving mode
- Various lens options

Pin Description

Pin	Description
VCC	Power 3.3VDC
TxD	Data Transmit (3.3V)
RxD	Data Receive (3.3V)
GND	Power Ground

Connector specification: 2mm pitch, 4pin single row
Reference part no: Suyin 190600
Mating connector: Suyin 140600



Bottom View

Command Summary

Detail Command control, please refer to the user's manual

1.	Initial	To configure the image size, color type
2.	Get Picture	Get Picture type
3.	Snapshot	Set snap shot image type
4.	Set Package Size	Set the package size to transmit data from module to Host
5.	Set Baudrate	Change the baud rate
6.	Reset	Reset the whole system or reset the state machine
7.	Power Off	To enter sleep mode
8.	Data	Set the data type and length for transmitting data to host
9.	SYNC	Sync signal to connect between host and module
10.	ACK	Command to indicate the communication success
11.	NAK	Command to indicate the communication fail with error code

Rm 802, Nan Fung Ctr, Castle Peak Rd, Tsuen Wan, NT., Hong Kong. Tel: (852) 2498 6248 Fax: (852) 2414 3050
Email: Sales@comedia.com.hk Web: http://www.comedia.com.hk

Electrical Specification

V_{DD} = 3.3V+10%, TA = 0 to 25°C

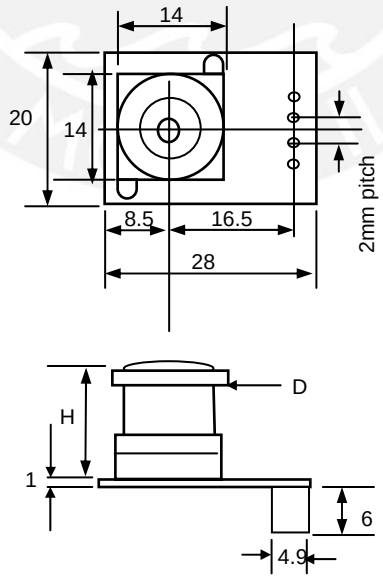
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	DC supply voltage		3.0	3.3	3.6	V
Io	Normal Operation Current	Operating		60		mA
Is	Suspend Current	Suspend		100		uA
V_{IH}	High level input voltage	TTL	2.0			V
V_{IL}	Low level input voltage	TTL			0.8	V

Lens Specification

Description	C328-7640	C328-2225BW	C328-2520BW	C328-3620IR	C328-3620BW	C328-6016BW	C328-6016IR
F/#	2.8	2.5	2.0	2.0	2.0	1.6	1.6
Focal length (mm)	4.63	2.2	2.5	3.6	3.6	6.0	6.0
Field of View Diagonal (deg)	57	118	100	66	66	36	36
Filter Option IR-cut filter	Yes	NA	NA	Yes	NA	NA	Yes
Total height from PCB H (mm)	10	18	24	22	22	20	20
Diameter of lens cap D (mm)	9	18	15	14	14	14	14

Board Measurement

Note: All lens holder are with 14x14, thread of 12mmx0.5, height H will be varied from different lens spec.

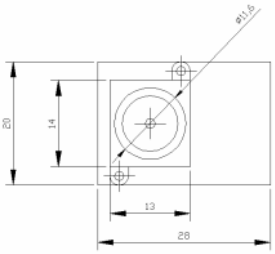
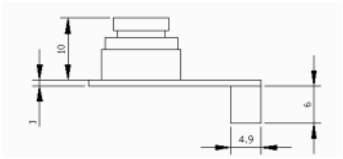
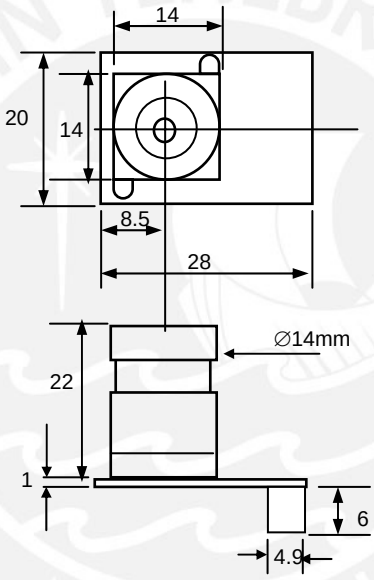


Note: In order to facilitate people for better understanding the communication with the module, we have developed an EV kit, C328-EV232, for user to run under PC Windows environment. However, this module is not designed for PC application. Such PC evaluation is only for better understanding of command control.

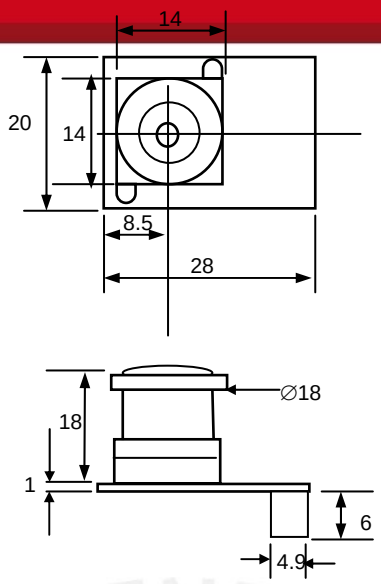
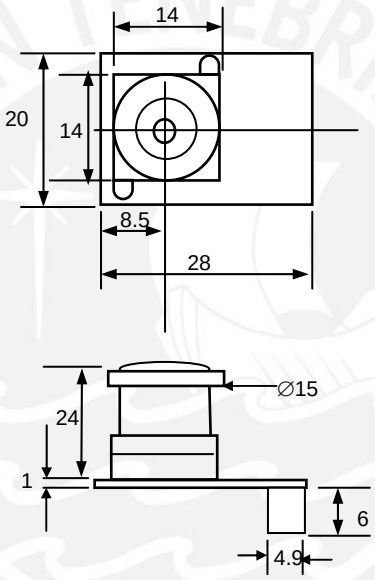
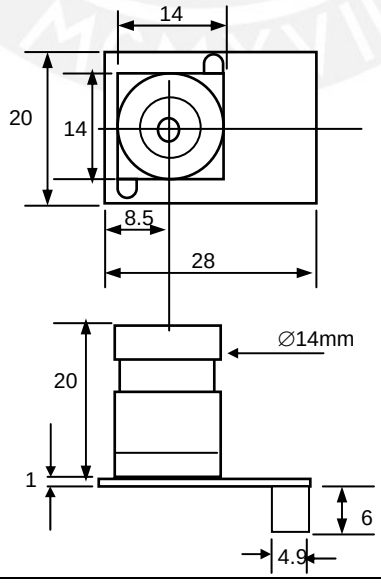
Rm 802, Nan Fung Ctr, Castle Peak Rd, Tsuen Wan, NT., Hong Kong. Tel: (852) 2498 6248 Fax: (852) 2414 3050
Email: Sales@comedia.com.hk Web: http://www.comedia.com.hk

Information of Alternative Lens solution for C328

Note: we suggest to use lens of IR cut filter built-in for outdoor application.

C328-7640 Standard configuration 	 	Detail spec and dimension, pls refer to the spec sheet of C328 F/No 2.8 f= 4.63mm FOV 57° diagonal IR cut filter built-in
C328-3620BW/IR No IR cut filter on the lens 		F/No 2.0 f=3.6mm FOV=66° diagonal

Rm 802, Nan Fung Ctr, Castle Peak Rd, Tsuen Wan, NT., Hong Kong. Tel: (852) 2498 6248 Fax: (852) 2414 3050
Email: Sales@comedia.com.hk Web: http://www.comedia.com.hk

C328-2225BW No IR cut filter on the lens 		F/No 2.5 f=2.2mm FOV=118° diagonal
C328-2520BW No IR cut filter on the lens 		F/No 2.0 f=2.5mm FOV=100° diagonal
C328-6016BW/IR No IR cut filter on the lens 		F/No 1.6 f=6.0mm FOV=36° diagonal

Rm 802, Nan Fung Ctr, Castle Peak Rd, Tsuen Wan, NT., Hong Kong. Tel: (852) 2498 6248 Fax: (852) 2414 3050
Email: Sales@comedia.com.hk Web: http://www.comedia.com.hk

C328-7640 User Manual

Release Note:

1. Jan 28, 2004 – official released v1.0

2. Feb 24, 2004 – official released v1.1

- **Fix the definition of verify code**
- **Fix the bug of unable jump to power save mode**
- **Fix the incorrect connection speed after wake up from power save mode**

3. Apr 24, 2004 – official released v2.0

- **Add auto baud-rate detection**
- **Add support of 9600bps, 19200bps, 38400bps**
- **Disable the 8-bit colour for uncompressed picture**

4. Apr 12, 2005 – official released v2.1

- **Add command to change the light frequency between 50/60 Hz**
- **Add more descriptions of the resolution selection**

5. Aug 19, 2005 – official released v3.0

- **Add description of the auto power mode**
- **Add FAQ section**

COMedia Ltd.
康大科技有限公司

Rm 802, Nan Fung Ctr, Castle Peak Rd, Tsuen Wan NT, Hong Kong
Tel: (852) 2498 6248 Fax (852) 2414 3050
Email: sales@comedia.com.hk
http://www.comedia.com.hk

General Description

The C328 module is a highly integrated serial camera board that can be attached to a wireless or PDA host performing as a video camera or a JPEG compressed still camera. It provides a serial interface (RS-232) and JPEG compression engine to act as a low cost and low powered camera module for high-resolution serial bus security system or PDA accessory applications.

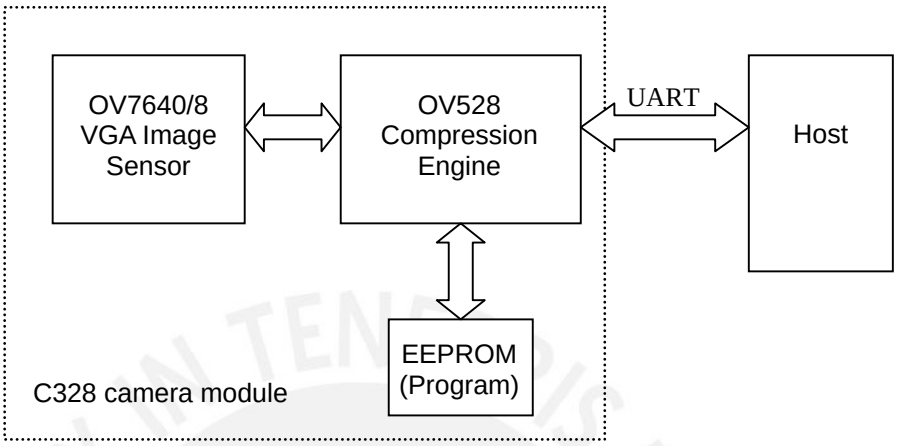


Figure 1 – System block diagram

Features

- Small in size, low cost and low powered (3.3V) camera module for high-resolution serial bus security system or PDA accessory applications.
- On-board EEPROM provides a command-based interface to external host via RS-232.
- UART: 115.2Kbps for transferring JPEG still pictures or 160x128 preview @8bpp with 0.75fps.
- On board OmniVision OV7640/8 VGA color sensor.
- Built-in JPEG CODEC for different resolutions.
- Built-in down sampling, clamping and windowing circuits for VGA, QVGA, 160x120 or 80x60 image resolutions.
- Built-in color conversion circuits for 2-bit gray, 4-bir gray, 8-bit gray, 12-bit RGB, 16-bit RGB or standard JPEG preview images.
- No external DRAM required.

System Configuration

1. Camera Sensor
   The C328-7640 module uses OmniVision OV7640/8 VGA color digital CameraChips with an 8-bit YCbCr interface.

2. OV528 Serial Bridge
   The OV528 Serial Bridge is a JPEG CODEC embedded controller chip that can compress and transfer image data from CameraChips to external device. The OV528 takes 8-bit YCbCr 422 progressive video data from an OV7640/8 CameraChip. The camera interface synchronizes with input video data and performs down sampling, clamping and windowing functions with desired resolution, as well as color conversion that is requested by the user through serial bus host commands.
   The JPEG CODEC can achieve higher compression ratio and better image quality for various image resolutions.

3. Program EEPROM
   A serial type program memory is built-in for C328-7640 to provide a set of user-friendly command interfacing to external host.

Board Layout

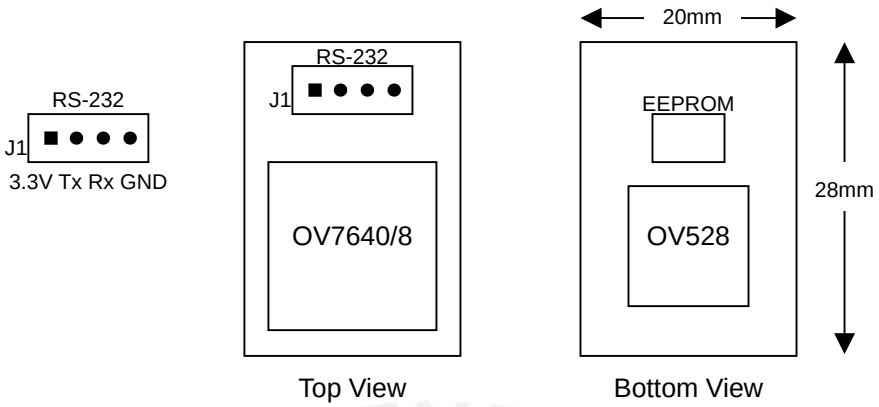


Figure 2 – C328-7640 board layout and serial interface pin

Serial Interface

1. Single Byte Timing Diagram
   A single byte RS-232 transmission consists of the start bit, 8-bit contents and the stop bit. A start bit is always 0, while a stop bit is always 1. LSB is sent out first and is right after the start bit.

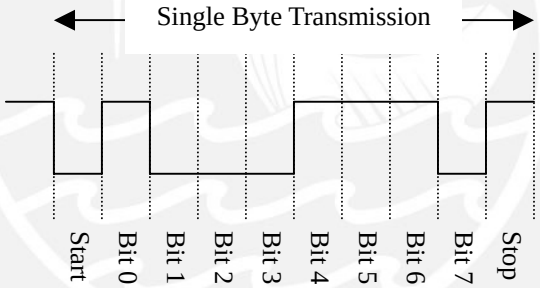


Figure 3 – RS-232 single byte timing diagram

2. Command Timing Diagram
   A single command consists of 6 continuous single byte RS-232 transmissions. The following is an example of SYNC (AA0D00000000h) command.

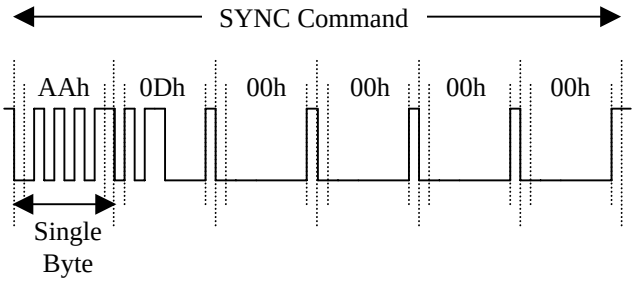


Figure 4 – RS-232 SYNC command timing diagram

Command Set

The C328-7640 module supports total 11 commands for interfacing to host as following:

Command	ID Number	Parameter1	Parameter2	Parameter3	Parameter4
Initial	AA01h	00h	Color Type	RAW Resolution (Still image only)	JPEG Resolution
Get Picture	AA04h	Picture Type	00h	00h	00h
Snapshot	AA05h	Snapshot Type	Skip Frame Low Byte	Skip Frame High Byte	00h
Set Package Size	AA06h	08h	Package Size Low Byte	Package Size High Byte	00h
Set Baudrate	AA07h	1st Divider	2nd Divider	00h	00h
Reset	AA08h	Reset Type	00h	00h	xxh*
Power Off	AA09h	00h	00h	00h	00h
Data	AA0Ah	Data Type	Length Byte 0	Length Byte 1	Length Byte 2
SYNC	AA0Dh	00h	00h	00h	00h
ACK	AA0Eh	Command ID	ACK counter	00h / Package ID Byte 0	00h / Package ID Byte 1
NAK	AA0Fh	00h	NAK counter	Error Number	00h
Light Frequency	AA13h	Frequency Type	00h	00h	00h

* If the parameter is 0xFF, the command is a special Reset command and the firmware responds to it immediately.

1. Initial (AA01h)

The host issues this command to configure the preview image size and color type. After receiving this command, the module will send out an ACK command to the host if the configuration success. Otherwise, an NACK command will be sent out.

1.1 Color Type

C328-7640 can support 7 different color types as follow:

2-bit Gray Scale	01h
4-bit Gray Scale	02h
8-bit Gray Scale	03h
12-bit Color	05h
16-bit Color	06h
JPEG	07h

1.2 Preview Resolution

80x60	01h
160x120	03h

1.3 JPEG Resolution

Since the Embedded JPEG Code can support only multiple of 16, the JPEG preview mode can support following image sizes. It is different from normal preview mode.

80x64	01h
160x128	03h
320x240	05h
640x480	07h

2. Get Picture (AA04h)

The host gets a picture from C328-7640 by sending this command.

2.1 Picture Type

Snapshot Picture	01h
Preview Picture	02h
JPEG Preview Picture	05h

3. Snapshot (AA05h)

C328-7640 keeps a single frame of JPEG still picture data in the buffer after receiving this command.

3.1 Snapshot Type

Compressed Picture	00h
Uncompressed Picture	01h

3.2 Skip Frame Counter

The number of dropped frames can be defined before compression occurs. “0” keeps the current frame, “1” captures the next frame, and so forth.

4. Set Package Size (AA06h)

The host issues this command to change the size of data package which is used to transmit JPEG image data from the C328-7640 to the host. This command should be issued before sending Snapshot command or Get Picture command to C328-7640. It is noted that the size of the last package varies for different image.

4.1 Package Size

The default size is 64 bytes and the maximum size is 512 bytes.

ID	-> Package ID, starts from zero for an image
Data Size	-> Size of image data in the package
Verify Code	-> Error detection code, equals to the lower byte of sum of the whole package data except the verify code field. The higher byte of this code is always zero. i.e. verify code = lowbyte(sum(byte[0] to byte[N-2]))

Note: As the transmission of uncompressed image is not in package mode, it is not necessary to set the package size for uncompressed image.

5. Set Baudrate (AA07h)

Set the C328-7640 baud rate by issuing this command. As the module can auto-detect the baud rate of the incoming command, host can make connection with one of the following baud rate in the table. The module will keep using the detected baud rate until physically power off

5.1 Baudrate Divider

Baudrate = 14.7456MHz / 2 x (2nd Divider + 1) / 2 x (1st Divider + 1)

Baudrate	1st Divider	2nd Divider	Baudrate	1st Divider	2nd Divider
7200 bps	ffh	01h	28800 bps	3fh	01h
9600 bps	bfh	01h	38400 bps	2fh	01h
14400 bps	7fh	01h	57600 bps	1fh	01h
19200 bps	5fh	01h	115200 bps	0fh	01h

6. Reset (AA08h)

The host reset C328-7640 by issuing this command.

6.1 Reset Type

"00h" resets the whole system. C328-7640 will reboot and reset all registers and state machines. "01h" resets state machines only.

7. Power Off (AA09h)

C328-7640 will go into sleep mode after receiving this command. SYNC command (AA0Dh) must be sent to wake up C328-7640 for certain period until receiving ACK command from C328-7640.

8. Data (AA0Ah)

C328-7640 issues this command for telling the host the type and the size of the image data which is ready for transmitting out to the host.

8.1 Data Type

Snapshot Picture	01h
Preview Picture	02h
JPEG Preview Picture	05h

8.2 Length

These three bytes represent the length of data of the Snapshot Picture, Preview Picture or JPEG Preview Picture.

9. SYNC (AA0Dh)

Either the host or the C328-7640 can issue this command to make connection. An ACK command must be sent out after receiving this command.

10. ACK (AA0Eh)

This command indicates the success of last operation. After receiving any valid command, ACK command must be sent out except when getting preview data. The host can issue this command to request image data package with desired package ID after receiving Data command from C328-7640. The host should send this command with package ID F0F0h after receiving a package to end the package transfer. Note that the field "command ID" should be 00h when request image data package.

10.1 Command ID

The command with that ID is acknowledged by this command.

10.2 ACK Counter

No use.

10.3 Package ID

For acknowledging Data command, these two bytes represent the requested package ID. While for acknowledging other commands, these two bytes are set to 00h.

11. NAK (AA0Fh)

This command indicates corrupted transmission or unsupported features.

11.1 NAK Counter

No use.

11.2 Error Number

Picture Type Error	01h	Parameter Error	0bh
Picture Up Scale	02h	Send Register Timeout	0ch
Picture Scale Error	03h	Command ID Error	0dh
Unexpected Reply	04h	Picture Not Ready	0fh
Send Picture Timeout	05h	Transfer Package Number Error	10h
Unexpected Command	06h	Set Transfer Package Size Wrong	11h
SRAM JPEG Type Error	07h	Command Header Error	F0h
SRAM JPEG Size Error	08h	Command Length Error	F1h
Picture Format Error	09h	Send Picture Error	F5h
Picture Size Error	0ah	Send Command Error	ffh

12. Light Frequency (AA13h)

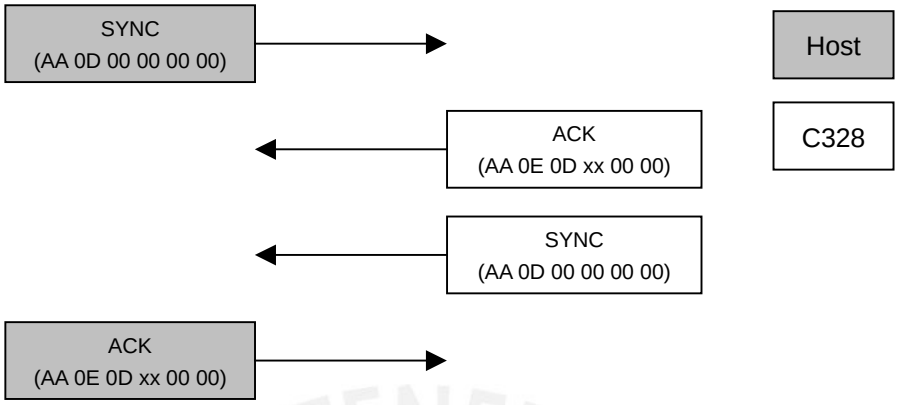
The host issues this command to change the light frequency of the C328-7640.

12.1 Light Frequency Type

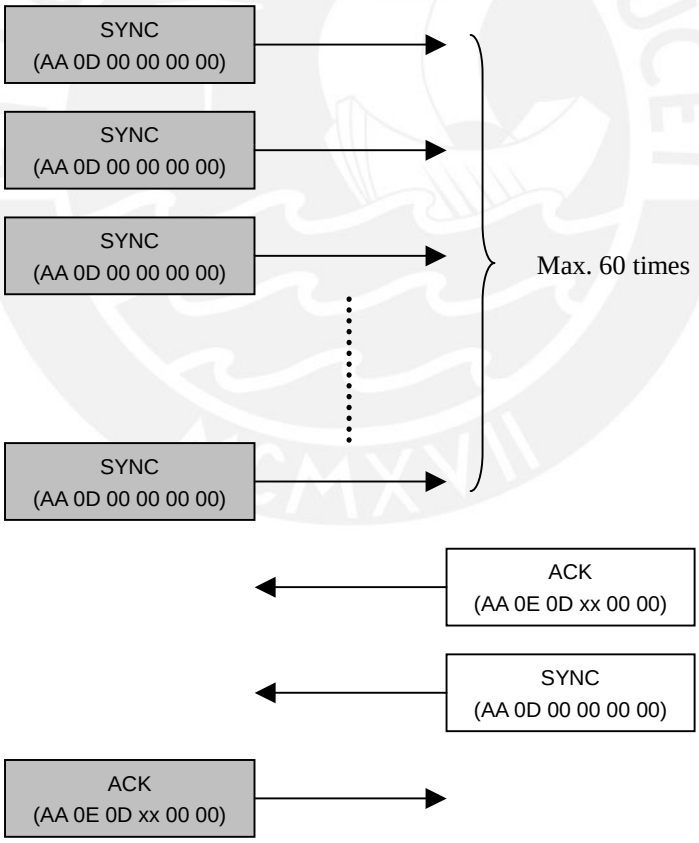
50Hz	00h
60Hz	01h

Command Protocol

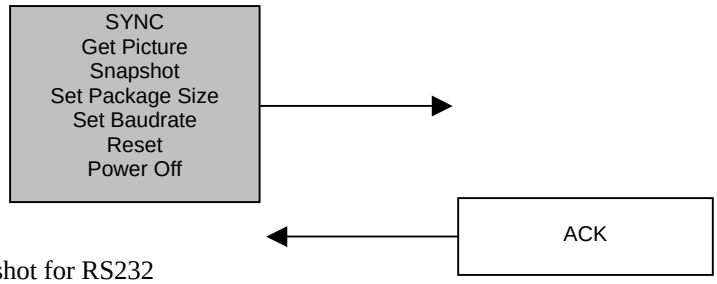
1. SYNC Command



2. Make Connection with C328-7640
   Send the SYNC command (at 14400bps) until receiving ACK command from C328-7640 (usually an ACK command is receive after sending 25 times of SYNC command). This must be done after power up.



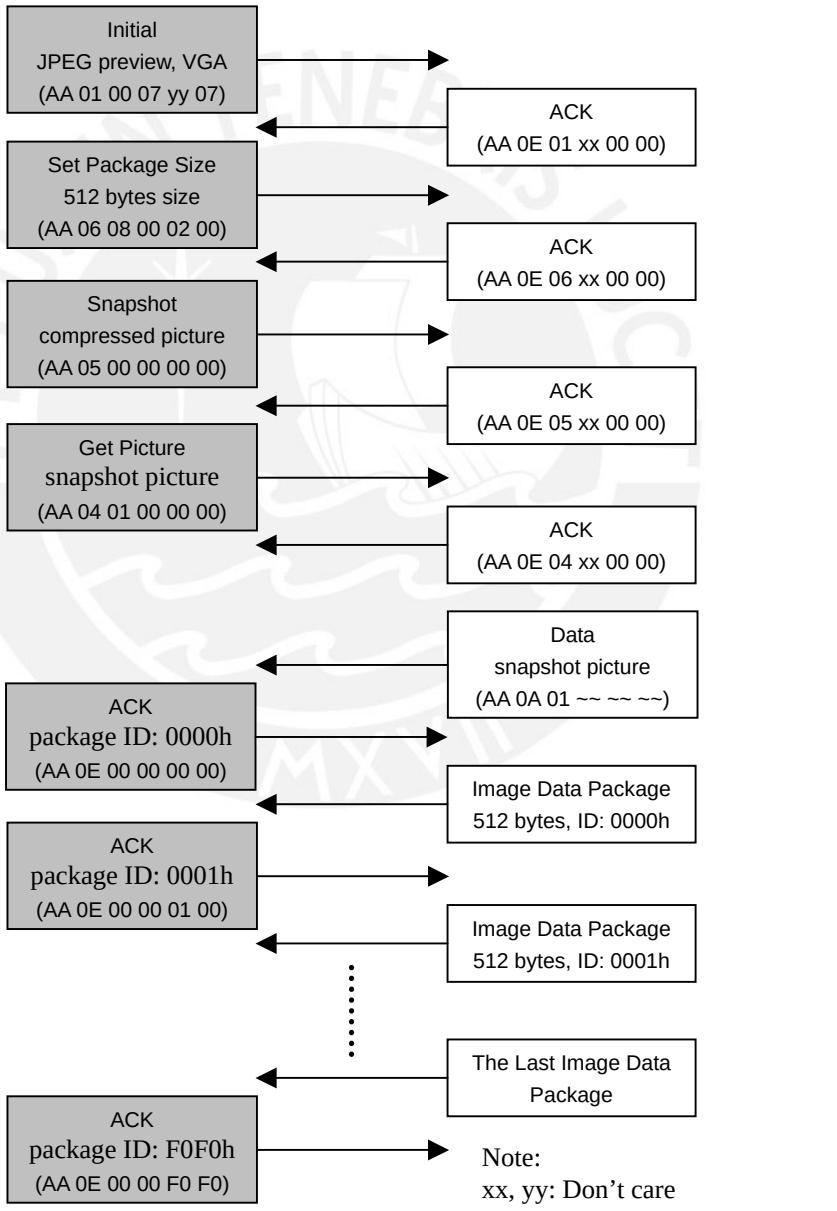
3. Initial, Get Picture, Snapshot, Set Package Size, Set Baudrate, Reset and Power Off Command



4. Getting a Snapshot for RS232

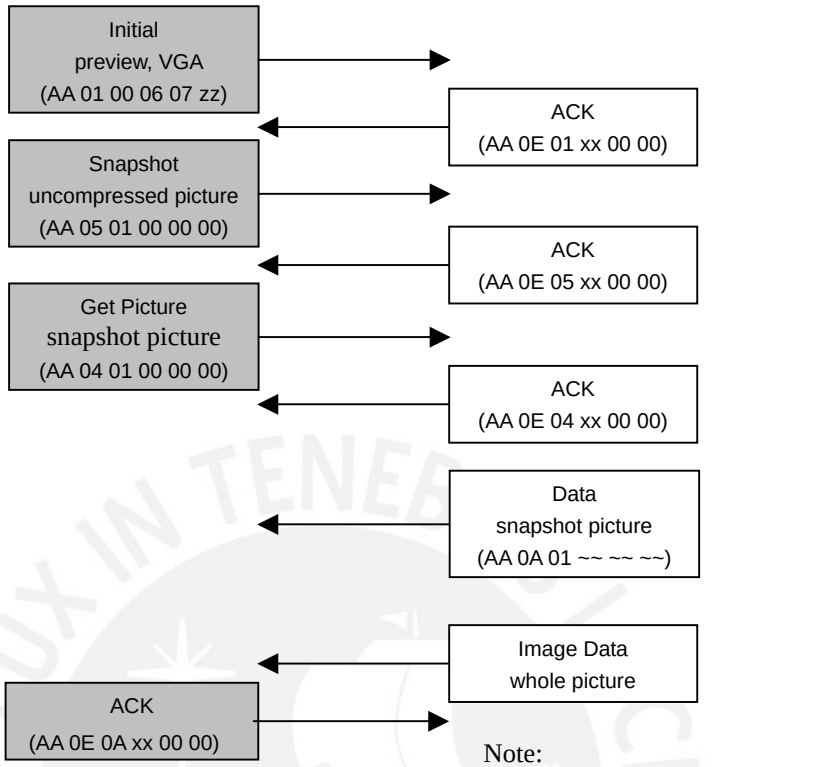
Make sure connection is made before the following communication.

4.1 JPEG Snapshot Picture (eg. 640x480 resolution)



Note:
xx, yy: Don't care
~~: Image size returned by C328

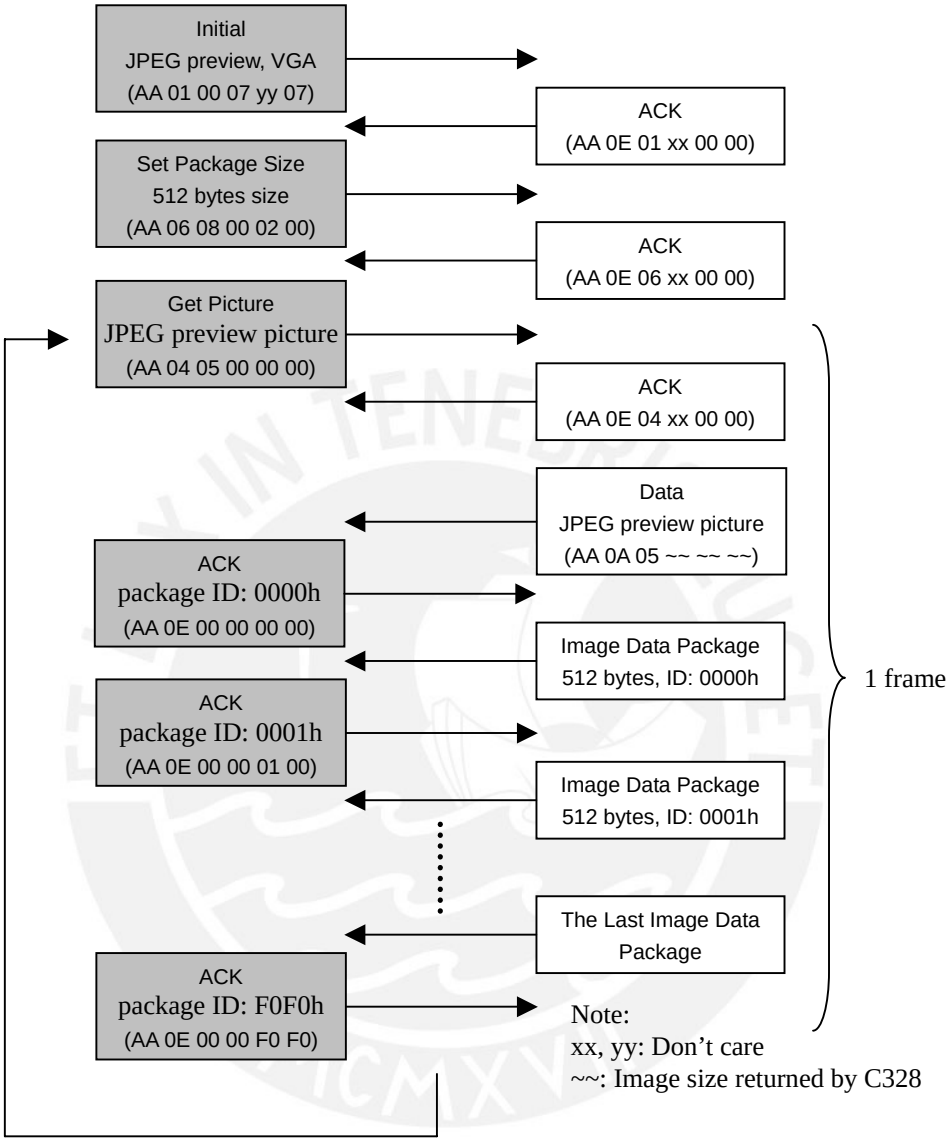
4.2 Snapshot Picture (uncompressed snapshot picture)



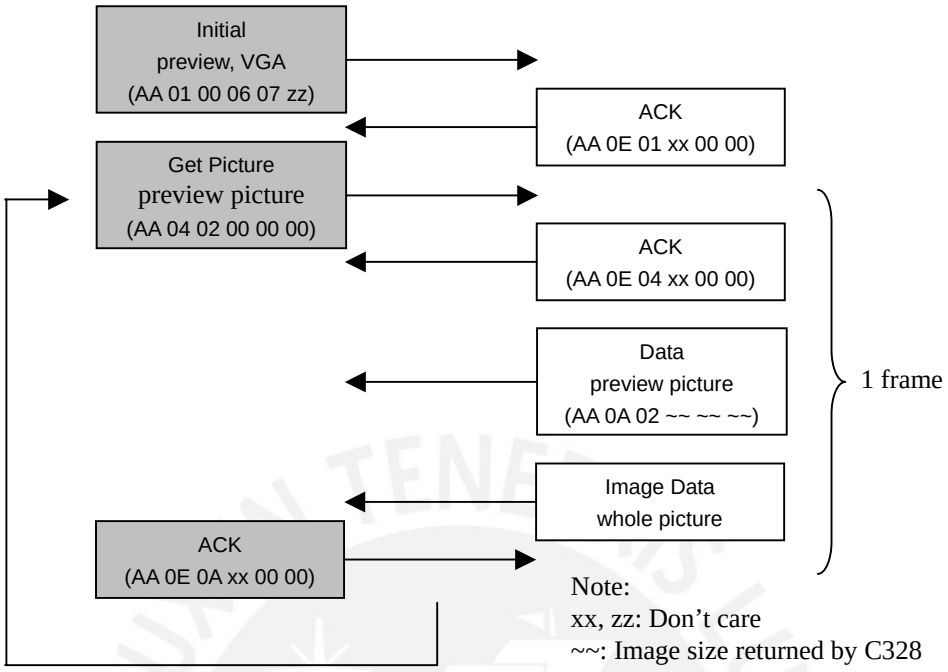
Note:
xx, zz : Don't care
~~: Image size returned by C328

5. Getting JPEG preview pictures (video) for RS232
Make sure connection is made before the following communication.

5.1 JPEG Preview Picture



5.2 Preview Picture (uncompressed preview picture)



Note:
xx, zz: Don't care
~~: Image size returned by C328

FAQ

Q: What is the power range of the camera module?

A: The range is **+3.0V - +3.6V**.

Q: I want to establish the connection between a PC and the camera module. Is there any configuration should be done?

A: To connection with a PC, a **RS-232 transceiver set-up** should be used as a communication interface.

Q: I have sent an SYNC command to camera, but it has no response. How can I synchronize with the module?

A: Users should send the SYNC commands one by one continuously until receiving the ACK and SYNC commands from the module. Normally, **25-60 SYNC** commands are required. After that, users should reply with an ACK command.

Q: What is the baud rate to synchronize with the camera? Will the baud rate change after SYNC?

A: C328 supports **7200, 9600, 14400, 19200, 28800, 38400, 57600 and 115200bps**. Users can synchronize with the camera at one of the baud rate above. Once synchronizing with camera successfully, the baud rate will not be changed until users change it with the “Set Baud rate” command.

Q: When will the baud rate be changed after receiving the “Set Baud rate” command?

A: The baud rate will be changed after the module reply with the ACK command. Users must use the new baud rate after this.

Q: After sending “Getpicture” command to the camera, what will the users receive?

A: After sending "Getpicture" command to the module, users will receive an "ACK", a "Data" command, "AA 0A 01 XX YY ZZ" telling you the image size, and then the first package of image data. .

Q: How to use the image size returned? Also, how many packages must be received to get the captured image?

A: Users can use the image size to calculate the number of packages will be received according to the package size set. The equation is shown in the following:
Number of package = Image size / (Package size – 6)

Q: According to the flow diagram, the ACK command for the first package is AA 0E 00 00 00 00 and that for the second one AA 0E 00 00 01 00. Is the third one AA 0E 00 00 02 00 or AA 0E 00 00 01 01?

A: For the third package, it should be AA 0E 00 00 02 00. Those for the other package are shown in the following:
AA 0E 00 00 L'L H'H.
L'L is the low byte of package ID
H'H is the high byte of package ID
i.e. ID = H'H L'L in hex

Q: After synchronization, I got the first picture with too low to too high luminance. What’s wrong with it?

A: After synchronization, the camera needs a little time for AEC and AGC to be stable. Users should wait for **1-2 seconds** before capturing the first picture.

Q: What are the formats of the uncompressed pictures?

A: The formats are shown in the following:
2-bit Gray Scale: 2-bit for Y only
4-bit Gray Scale: 4-bit for Y only
8-bit Gray Scale: 8-bit for Y only
12-bit Color: 444 (RGB)
16-bit Color: 565 (RGB)

DELKIN DEVICES®

SLC Commercial and Industrial Secure Digital (SD/SDHC) Card

Engineering Specification

Document Number L5ENG00432 Rev. 1.8

Table of Contents

List of Figures

List of Tables

1.0 General Description

The Delkin Devices Secure Digital (SD) memory card is only the size of a postage stamp and the thickness of a credit card. Yet these solid state devices provide high speed performance and large storage capacity for many industrial applications. Delkin SD cards are a versatile storage solution for a wide variety of data. They feature built in write-protection to ensure data security.

Features

- Functionally compliant with SD specification version 1.1 and 2.0 (High Capacity)
- Operating bus modes – SD & SPI
- SD capacities supported: 128MB, 256 MB, 512 MB, 1 GB and 2 GB
- SDHC capacities supported: 4GB and 8GB
- Write Protect Switch
- Solid State Memory
- Supports 2.7 Volt to 3.6 Volt operation
- Error Correction Code (ECC)
- Wear Leveling algorithms for extended card life
- RoHS Compliant (Conforms to European Union Directive 2002/95/EC)

1.1 Recommended Temperature Conditions

Parameter	Temperature Range
Storage Temperature	-50°C ~ 90°C
SLC Commercial Operating Temperature	-0°C ~ 70°C
SLC Industrial Operating Temperature	-40°C ~ 85°C

1.2 Performance

Parameter	Value
Data Transfer Rate*	Up to 25 MB/sec
Sustained Read*	Up to 20 MB/sec
Sustained Write*	Up to 10 MB/sec

1.3 Reliability

Parameter	Value
Endurance Cycle*	2,000,000 cycles minimum
MTBF**	2,000,000 hours
Data Retention	10 Years

* Reference Delkin Reliability Test Report for Compact Flash, Secure Digital, USB and Embedded USB Drives (Document Number L5002).

** Dependent on configuration and testing environment

1.4 Environmental Characteristics

Parameter	Value
Shock	40g's at 11ms
Vibration	15Hz to 2000Hz
Humidity	5% to 95% Non-condensing
Altitude	80,000 feet
Durability	10,000 mating cycles
WP switch Min. moving force	40gf
WP Switch cycles	1000 Cycles min. (@ Slide force 0.4N to 5N)

1.5 Part Numbers

1.5.1 SLC Commercial Grade (0 ~ 70°C) Delkin SD cards

Capacity	Part Number
128MB	SD12xxxyy-C1000-D
256MB	SD25xxxyy-C1000-D
512MB	SD51xxxyy-C1000-D
1GB	SD0Gxxxyy-C1000-D
2GB	SD02xxxyy-C1000-D
4GB	SD04xxxyy-C6000-D
8GB	SD08xxxyy-C6000-D

1.5.2 SLC Industrial Grade (-40 ~ 85°C) Delkin SD cards

Capacity	Part Number
128MB	SE12xxxyy-C1000-D
256MB	SE25xxxyy-C1000-D
512MB	SE51xxxyy-C1000-D
1GB	SE0Gxxxyy-C1000-D
2GB	SE02xxxyy-C1000-D
4GB	SE04xxxyy-C6000-D
8GB	SE08xxxyy-C6000-D
16GB	SE16xxxyy-C6000-D

xxx = place holder for flash designation

yy = place holder for controller/firmware (H8 or HL)

1.6 Card Dimensions

Dimension	Measurement
Length:	32 ± 0.10 mm (1.260 ±.004 in.)
Width:	24 ± 0.10 mm (0.945 ±.004 in.)
Thickness (with label area)	2.1 mm ± 0.15 mm (0.083 ± .006 in.)
Weight:	2.0 g typical

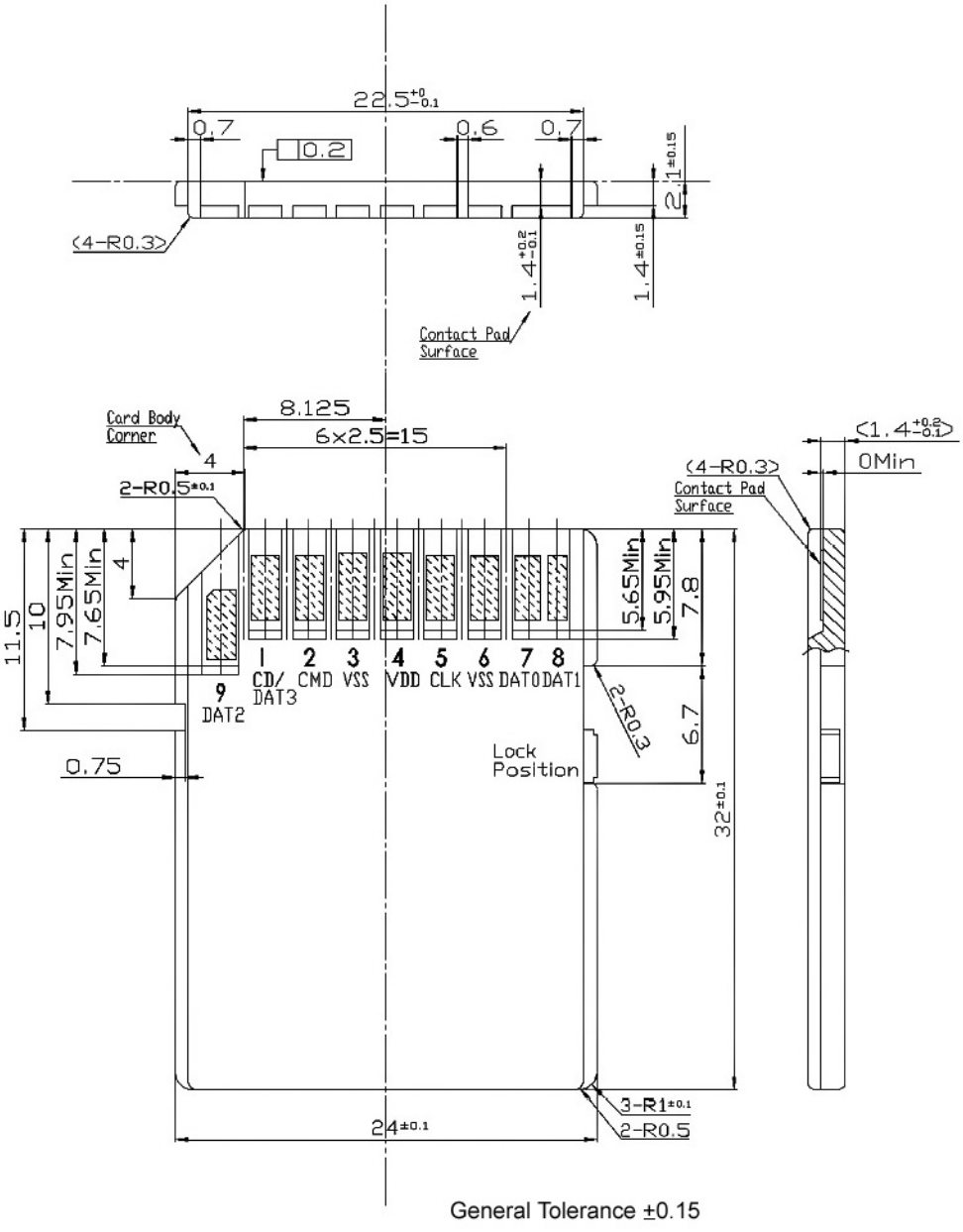


Figure 1. SD card dimensions

2.0 SD Card Interface

2.1 SD Pin Assignment

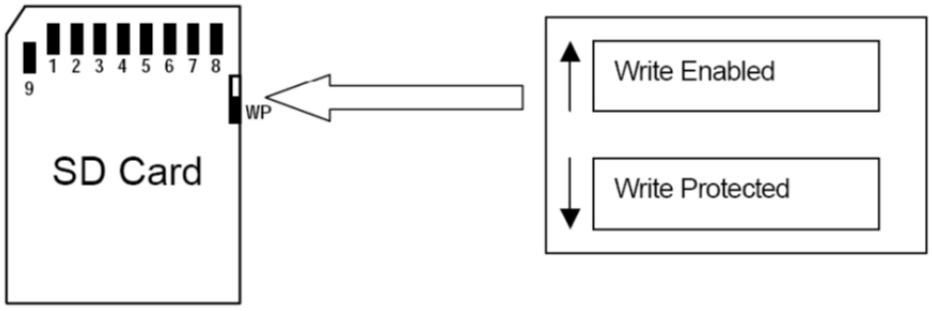


Figure 2. SD card pin designation

Table 1. SD card pin assignment

Pins	SD Mode			SPI Mode		
	Name	IO type [1]	Description	Name	IO Type	Description
1	CD/ DAT3	I/O /PP	Card Detect/ Data Line [Bit3]	CS	I	Chip Select (Negative True)
2	CMD	PP	Command/Response	DI	I	Data In
3	V_{SS1}	S	Ground	V_{SS}	S	Ground
4	V_{dd}	S	Supply Voltage	V_{dd}	S	Supply Voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS2}	S	Ground	V_{SS2}	S	Ground
7	DAT0	I/O /PP	Data Line [Bit0]	DO	O/PP	Data Out
8	DAT1	I/O /PP	Data Line [Bit1]	RSV	-	Reserved [2]
9	DAT2	I/O /PP	Data Line [Bit2]	RSV	-	Reserved [2]

1) S: Power Supply, I: Input, O: Output, I/O: Bi-directionally, 'PP' - IO using push-pull drivers

2) These signals should be pulled up by host side with 10-100k ohm resistance in the SPI Mode.

2.2 SD Bus Topology

The SD Memory Card supports two alternative communication protocols–*SD* and *SPI Bus Mode*. The host system can choose either mode. The same SD Card data can be read and written by both modes. SD mode allows high performance, 4-bit data transfer. The SPI Bus mode provides a simple, common interface for the SPI channel, but exhibits lower performance relative to the SD Mode.

2.3 SD Bus Mode Protocol

The SD bus mode protocol allows the dynamic configuration of 1 to 4 data lines as bidirectional data signals. After power up, by default, the SD card will use only DAT0. After initialization, the host can change the bus width.

Multiple SD card connections are available to the host. Common Vdd, Vss and CLK signal connections are available in multiple connections. However, *Command*, *Respond* and *Data* lines from the host (DAT0-DAT3) are discrete for each. This feature allows for an easy trade-off between hardware cost and system performance. Communication over the SD bus is based on a command and data bit stream initiated by a start bit and terminated by a stop bit.

Command:

Commands are transferred serially on the CMD line. A command is a token to start an operation from host to the card. Commands are sent to an addressed single card (*addressed command*) or to all connected cards (*broadcast command*).

Response:

Responses are transferred serially on the CMD line. A response is a token to answer to a previously received command. Responses are sent from an addressed single card or from all connected cards.

Data:

Data is transferred via the D0-3 data lines. Data can be transferred from the card to the host or vice versa.

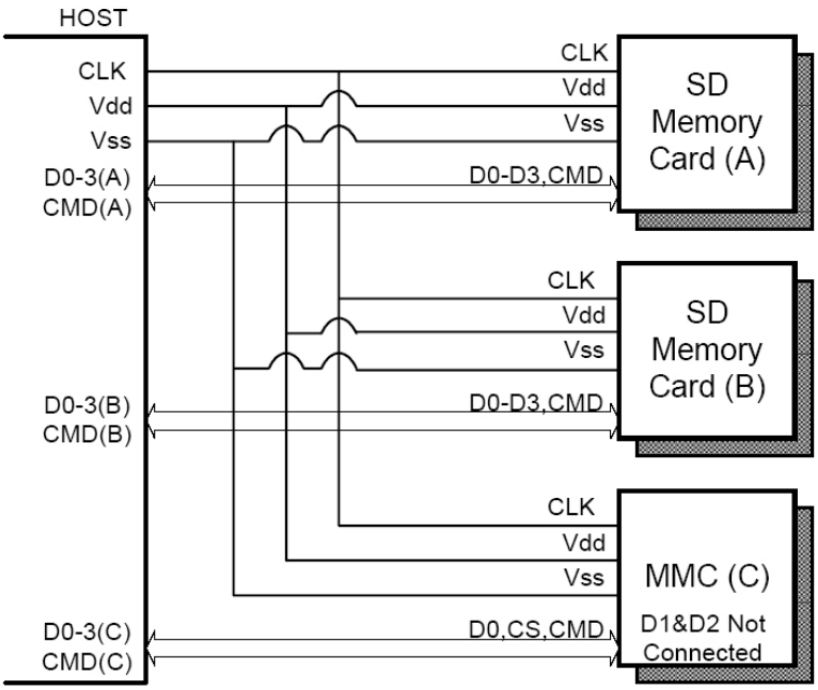


Figure 3. SD card (SD mode) connection diagram

CLK: Host card Clock signal

CMD: Bi-directional Command/ Response Signal

DAT0 - DAT3: 4 Bi-directional data signal

Vdd: Power supply

Vss: GND

2.4 SPI Bus Mode Protocol

The SPI bus allows 1-bit data transfer via two channels (data in/out). The SPI-compatible mode allows *MultiMediaCard* (MMC) host systems to use the SD card with little change. The SPI bus mode protocol utilizes byte transfer. All of the data tokens are multiples of 8-bit bytes and always byte-aligned to the CS signal.

The advantage of the SPI mode is easier host configuration. In particular, an MMC host can be modified with little change. The disadvantage of the SPI mode is reduced performance relative to SD mode.

CAUTION: In host configuration, use ONLY the SD Card Specification. DO NOT use the MMC Specification. Initialization requires the SD-specific ACMD41 synchronization command. Also, take particular care regarding memory registers. Some registers are SD or MMC specific. Even compatible registers can require different definitions, in particular the *CSD* Register.

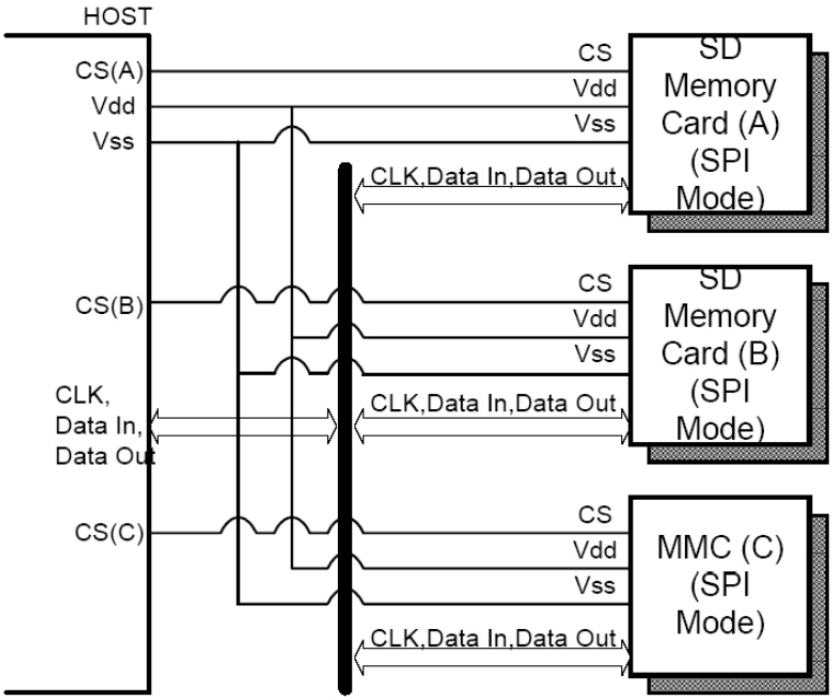


Figure 4. SD card (SPI mode) connection diagram

CS: Card Select Signal

CLK: Host card Clock signal

Data in: Host to card data line

Data out: card to host data line

Vdd: Power supply

Vss: GND

3.0 SD Card Electrical Characteristics

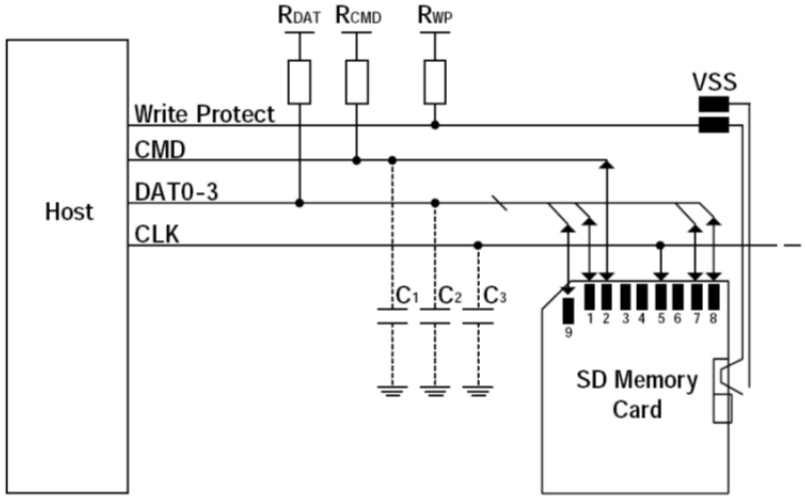


Figure 5. SD card connection diagram

3.1 Absolute Maximum Conditions

Card Type	Parameter	Symbol	Min	Max	Unit
SD	Supply Voltage	V_{DD}	-0.3	+5.0	V
	Input Voltage	V_{IN}	-0.3	V_{DD}+0.3	V
SDHC	Supply Voltage	V_{DD}	-0.3	+4.6	V
	Input Voltage	V_{IN}	-0.3	V_{DD}+0.3	V

3.2 DC Characteristics

This section includes data tables for the following:

- Standard Secure Digital (SD) DC characteristics
- Secure Digital High Capacity (SDHC) DC characteristics
- Signal capacitance

Table 2. Standard Secure Digital (SD) DC characteristics

Item		Symbol	Condition	MIN.	Typ	MAX.	Unit	Note
Supply Voltage 1		VDD	-	2.0	-	3.6	V	For CMD0, 15,55, ACMD41 Only
Supply Voltage 2			-	2.7	-	3.6	V	For All commands
Input Voltage	High Level	VIH	-	VDD*0.625	-	-	V	
	Low Level	VIL	-	-	-	VDD*0.25	V	
Output Voltage	High Level	VOH	VDD = 2V IOH = -100uA	VDD*0.75	-	-	V	
	Low Level	VOL	VDD = 2V IOL = 100uA	-	-	VDD*0.125	V	
Standby Current		ICC1	3.6V Clock 50MHz	-	-	30	mA	
			2.7V Clock Stop	-	-	0.2		
Operation Voltage		ICC2	3.6V/ 50MHz	-	-	80	mA	Write
			2.7V/ 50MHz	-	-	80		Read
Input Voltage Setup Time		Vrs	-	-	-	250	ms	

Table 3. Secure Digital High Capacity (SDHC) DC characteristics

Item		Symbol	Condition	MIN.	Typ.	MAX.	Unit	Note
Supply Voltage		VDD	-	2.7	-	3.6	V	
Input Voltage	High Level	VIH	-	VDD*0.625	-	-	V	

Item		Symbol	Condition	MIN.	Typ.	MAX.	Unit	Note
	Low Level	VIL	-	-	-	VDD*0.25	V	
Output Voltage	High Level	VOH	VDD = 2V IOH = -100uA	VDD*0.75	-	-	V	
	Low Level	VOL	VDD = 2V IOL = 100uA	-	-	VDD*0.125	V	
Standby Current		ICC1	3.6V Clock 25MHz	-	-	30	mA	
			3.0V Clock Stop	-	-	0.55		@25 °C
Operation Current[1]		ICC2	3.6V/ 25MHz, 50MHz	-	-	200	mA	Write
				-	-	200		Read
Input Voltage Setup Time		Vrs	-	-	-	250	ms	

1) Peak Current: RMS value over a 10usec period

Table 4. Signal capacitance

Item	Symbol	Min.	Max.	Unit	Note
Pull up Resistance	RCMD RDAT	10	100	K Ohm	
Bus Signal Line Capacitance	CL	-	100	pF	FPP<20MHz
Single Card Capacitance	CCARD	-	10	pF	
Pull up Resistance inside card(pin1)	RDAT3	10	90	K Ohm	

Note: WP pull-up (R_{wp}) Value is dependent on the Host Interface drive circuit.

3.3 AC Characteristics

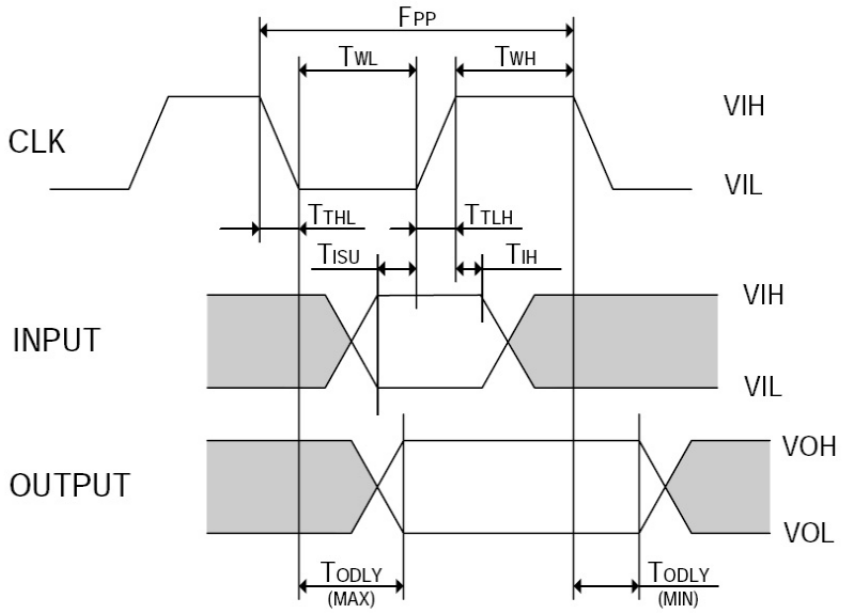


Figure 6. AC timing diagram

Table 5. AC characteristics

Item	Symbol	Min.	Max.	Unit	Note
Clock Frequency (In any State)	F_{sty}	0	50	MHz	C_L<100pF
Clock Frequency (Data Transfer Mode)	F_{PP}	0	50	MHz	C_L<100pF
Clock Frequency (Card Identification Mode)	F_{OD}	$0_{(1)}$/100	400	kHz	C_L<250pF
Clock Low Time	T_{WL}	10	-	ns	C_L<100pF
Clock High Time	T_{WH}	10	-	ns	
Clock Rise Time	T_{TLH}	-	10	ns	
Clock Fall Time	T_{THL}	-	10	ns	
Input Setup Time	T_{ISU}	5	-	ns	C_L< 25pF
Input Hold Time	T_{IH}	5	-	ns	
Output Delay Time	T_{ODLY}	0	14	ns	

4.0 Internal Card Information

4.1 Security Information

Media Key Block (MKB) and *Media ID* are Toshiba copy protection technologies that comply with the CPRM specification. This data security information is NOT development information available for evaluation. The Host System must be compliant with the CPRM specification to use these security functions. This information is kept confidential for security reasons.

4.2 SD Card Registers

The Delkin SD card supports six registers–OCR, CID, CSD, RCA, SCR, and SD Status. The registers OCR, CID, CSD, RCA, and SCR are MMC-compatible. The SD Status register is SD card-specific.

Note: The DSR register IS NOT SUPPORTED in this card.

Table 6. SD card Registers

Resister Name	Bit Width	Description
OCR	32	Operation Condition (VDU Voltage Profile and Busy Status Information)
CID	128	Card Identification information
CSD	128	Card specific information
RCA	16	Relative Card Address
DSR	16	Not Implemented (Programmable Card Driver): Driver Stage Register
SCR	64	SD Memory Cards special features
SD Status	512	Status bits and Card features

DELKIN DEVICES®

SLC Industrial microSD Memory Card

Engineering Specification

Document Number: L5ENG00392

Revision: A

Table of Contents

List of Figures

List of Tables

1 Overview

Delkin microSD cards combine a small form factor with a rugged, reliable package that's manufactured specifically for industrial applications. Unlike ordinary Secure Digital cards, the Delkin microSD encapsulates all internal components to seal out dust, moisture, and electro-static discharge and to enhance shock and vibration performance. Its industrial operating temperature range of -40° to 85°C handles the harshest environments. Combining data-precise Single Level Cell (SLC) components with Error Correction Code and wear leveling algorithms gives the cards an endurance rating of 2,000,000 write/erase cycles. These RoHS-compliant cards are also supported by Delkin's locked-down Bill of Materials that ensures consistent product performance and future compatibility. With outstanding read/write speeds, these cards are ideal for automotive, security, medical, military, aviation, navigation, or any severe-service application where dependability, durability, and data integrity are mission critical.

1.1 Product Features

- **Versatility**
  - Targeted for portable and stationary applications
  - Designed for read-only and read/write cards
  - Card detection (Insertion/Removal)
  - Switch function command supports High-Speed, eCommerce, and future functions
  - Supports both SD and SPI modes
- **Capacity**
  - Standard Capacity microSD Memory Card: Up to and including 2GB
  - High Capacity microSDHC Memory Card: 4GB, 8GB & 16GB (This version of the specification limits capacity up to and including 32GB)
- **Power**
  - Operating voltage range: 2.7-3.6V
- **Current**

  Typical Power Required (Ta=25°@3V)

	Value	Notes
Stand-by	75uA	Max – capacities up to 1GB
	120uA	Max – capacities 2GB and up
Read	47mA	Max (varies by capacity)
Write	59mA	Max (varies by capacity)

- **Durability**
  - Over 2,000,000 Write Cycles
  - Global Wear Leveling
  - Correction of memory field errors
  - Card removal during read operation will never harm the content.

- **Speed**
  - Default mode: Variable clock rate 0-25Mhz, up to 12.5MB/sec interface speed (using 4 parallel data lines)
  - High-Speed mode: Variable clock rate 0-50 MHz, up to 25 MB/sec interface speed (using 4 parallel data lines)
  - Data transfer rate up to 25 MB/sec data transfer rate (using 4 parallel data lines). Maximum data rate with up to 10 cards

- **Security**
  - Contact Protection Mechanism: Complies with highest security of SDMI standard
  - Password Protection of cards
  - Copyright protection mechanism—Complies with highest security of SDMI standard Password Protection of cards (CMD42 -LOCK- UNLOCK)
  - Write Protect feature using mechanical switch
  - Built-in write protection features (permanent and temporary)

- **Ease of Use**
  - Card Detection (Insert/Remove)
  - Application specific commands
  - Comfortable erase mechanism
  - Standard Protocol—attributes of the communication channel:
    - SD Memory Card Communication Channel
    - Six-wire communication channel (clock, command, 4 data lines)
    - Error-protected data transfer
    - Single or multiple block-oriented data transfer
  - Standard Size—microSD Memory Card form factor defined in this specification
  - Standard size microSD Memory Card thickness is defined as 1.0mm nominal (+/- 0.1mm).

1.2 Suggested Applications

- Industrial Computers
- Embedded Systems
- Data Acquisition
- Agriculture
- Gaming
- Telecommunications
- Hundreds of other industries looking for a more robust and rugged digital storage option

1.3 Specifications Summary

The following table provides a summary of the specifications critical to most engineering solutions. For more detailed specifications, refer to the appropriate engineering specification section.

Specification	microSD
Model number	See Table 1
Capacity	128MB – 16GB
Form factor	11mm x 15mm x 1mm
Interface	Dual protocol modes (SD and SPI)
Interface connector	8-pin @ 0-50MHz
Hot swappable	Yes
RoHS compliant	Yes
Performance	
Interface burst speed	25MB/s
Sustained read transfer rate	Up to 23.0 MB/s (varies by capacity)
Sustained write transfer rate	Up to 21.4 MB/s (varies by capacity)
Reliability/Data Integrity	
MTBF (power-on hours)	>2,000,000 hours
Endurance (write/erase cycles)	>2,000,000 cycles
Data Retention	>10 years
Power	
Supply voltage	2.7V -3.6V
Typical power required	Ta=25°@3V
Stand-by	Capacities <2GB: 75uA, ≥2GB: 120uA
Read	Capacities <2GB: 38mA, ≥2GB: 47mA
Write	Capacities <2GB: 47mA, ≥2GB: 59mA
Environmental	
Storage temperature (°C)	-40 ~ 85°C
Operating temperature (°C)	-40 ~ 85°C
Relative humidity (non-condensing)	5 - 95%
Operating shock	40Gs at 11ms
Vibration	15Hz – 2,000Hz
Altitude	80,000 ft.
Durability	10,000 mating cycles

Physical Dimensions	
Length	15.0mm ±0.1mm
Width	11.0mm ±0.1mm
Thickness	1.0mm nominal (+/- 0.1mm See Fig. 2 C1+C3.)
Weight	0.5g typical

1.4 Part Numbers and Availability

microSD Memory Cards and adapters are available from Delkin in the capacities shown in the table below.

Table 1. microSD Card Capacities and Part Numbers

Capacity*	Delkin Part Number	Description
128MB	S212SFQSR-C1000-B	microSD Card with SD Adapter
128MB	S212SFQSR-C1047-B	microSD Card without SD Adapter
256MB	S225SFRTZ-C1001-B	microSD Card with SD Adapter
256MB	S225SFRTZ-C1047-B	microSD Card without SD Adapter
512MB	S251SFRTZ-C1001-B	microSD Card with SD Adapter
512MB	S251SFRTZ-C1047-B	microSD Card without SD Adapter
1GB	S20GMFYTY-C1000-B	microSD Card with SD Adapter
1GB	S20GMFYTY-C1047-B	microSD Card without SD Adapter
2GB	S202MFBSS-C1000-B	microSD Card with SD Adapter
2GB	S202MFBSS-C1047-B	microSD Card without SD Adapter
4GB	S204MFBSS-CX000-B	microSD Card with SD Adapter
4GB	S204MFBSS-CX047-B	microSD Card without SD Adapter
8GB	S208MFBSS-CX000-B	microSD Card with SD Adapter
8GB	S208MFBSS-CX047-B	microSD Card without SD Adapter
16GB	S216MFBSS-CX001-B	microSD Card with SD Adapter
16GB	S216MFBSS-CX047-B	microSD Card without SD Adapter

*Note: Usable capacities are within 10% of the gross capacity figures shown above, which is typical with all NAND flash devices, as a small portion of the total is needed for controller firmware and spare block reserves.

1.5 microSD Memory Card Read/Write Speeds

Read and write speeds vary based on memory capacity and other factors such as the size of data blocks, benchmarking tool utilized, computer speed, etc.

Table 2. microSD Memory Card Read/Write Speeds*

Capacity	Read Speed (MB/s)	Write Speed (MB/s)
128MB	14.3	6.0
256MB	15.9	6.0
512MB	15.9	11.0
1GB	19.0	11.0
2GB	23.0	9.0
4GB	23.0	21.0
8GB	23.0	21.3
16GB	23.0	21.4

*Actual speeds are dependent on host environment, configuration, write size, etc. and may vary.

2 Mechanical Specifications

2.1 External Signal Contacts (ESC)

Table 3. microSD Memory Card Package – External Signal Contacts

Number of ESCs	8 minimum
Distance from front edge	1.1mm
ESC grid	1.1mm
Contact dimensions	0.8mm X 2.9mm
Electrical resistance	30m Ω (worst case : 100m Ω)
Plating Nickel Base Gold	 5um (196.8 microinches) minimum 0.8um (31.5 microinches) minimum

2.2 Design and Format

Table 4. microSD Memory Card package – Dimensions

Dimensions	11mm x 15mm (min. 10.9mm x 14.9mm, max.11.1mm x 15.1mm) Testing according to MIL STD 883, Method 2016
Thickness	Inter Connect Area: 0.7mm ±0.05mm (see Figure 1, C1) Card Thickness: 1.0mm nom. (+/- 0.1mm, see Figure 1, C1/C3) Pull Area: 1.0mm ±0.1mm (see Figure 1, C1)
Printable area	Suggested outside the “Keep Out Area” (see Figure 3)
Surface	Plain (except contacts area)
Edges	Smooth edges
Inverse Insertion	Protection on upper-right corner (top view)
Position of ESC contacts	Along middle of shorter edge

2.3 Reliability and Durability

Table 5. Reliability and Durability

Temperature	Operation: -40°C / 85 °C Storage: -40 °C (168h) / 85 °C (500h) Junction temperature: 95 °C max.
Moisture and Corrosion	Operation: -40°C / 95% relative humidity Storage: -40 °C / 93% relative humidity (500h) Salt water spray: 3% NaCl/35C;24h acc.MIL STD Method 1009
Reliability	2,000,000 write cycles
Durability	10,000 mating cycles
Bending1	10N
Torque1	0.10N*m ± 2.5 °C Max
Drop Test	1.5m free fall
UV light exposure	UV: 254nm, 15Ws/cm2 according to ISO 7816-1
Visual inspection shape and form1	No mold skin; complete form; no cavities Surface smoothness ≤-0.1mm/cm2 within contour; no cracks, No pollution (fat, oil dust, etc.)

Note: SDA's recommended test methods for torque, bending and warpage are defined separately.

2.4 Electrical Static Discharge (ESD) requirements

ESD testing should be conducted according to IEC 61000-4-2. Required ESD parameters are:

- **Human Body Model**: ±4 KV 100pF / 1.5KΩ
- **Machine model**: ±0.25 KV 200pF / 0Ω

2.4.1 Contact Pads Area

- **Human Body Model**: ±4KV, according to IEC 61000-4-2

2.4.2 Non-contact Pads Area

- **Coupling Plane Discharge**: ±8KV
- **Air Discharge**: ±15KV

2.5 Mechanical Form Factor

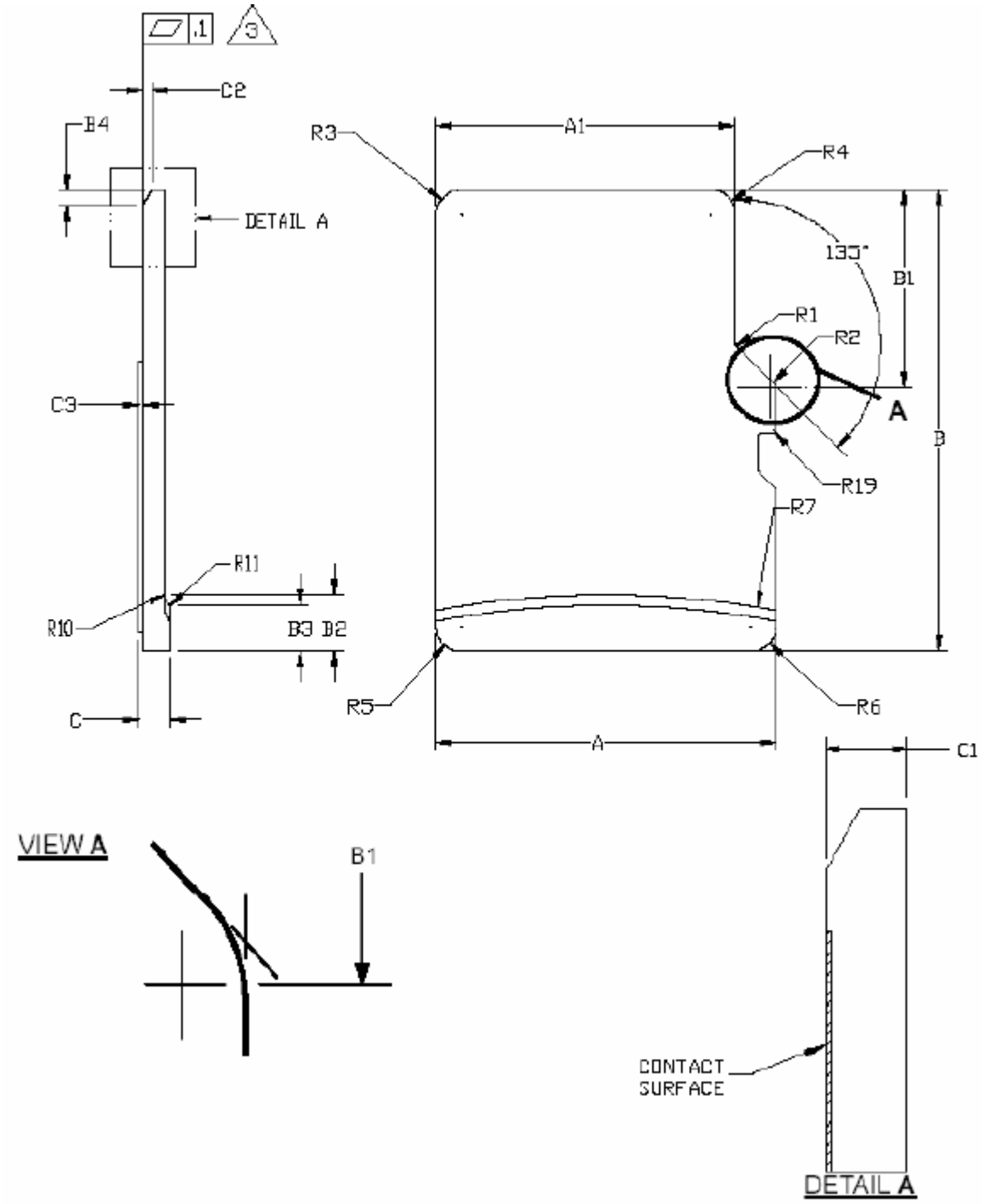


Figure 1. microSD Mechanical Description: Top and Side Views

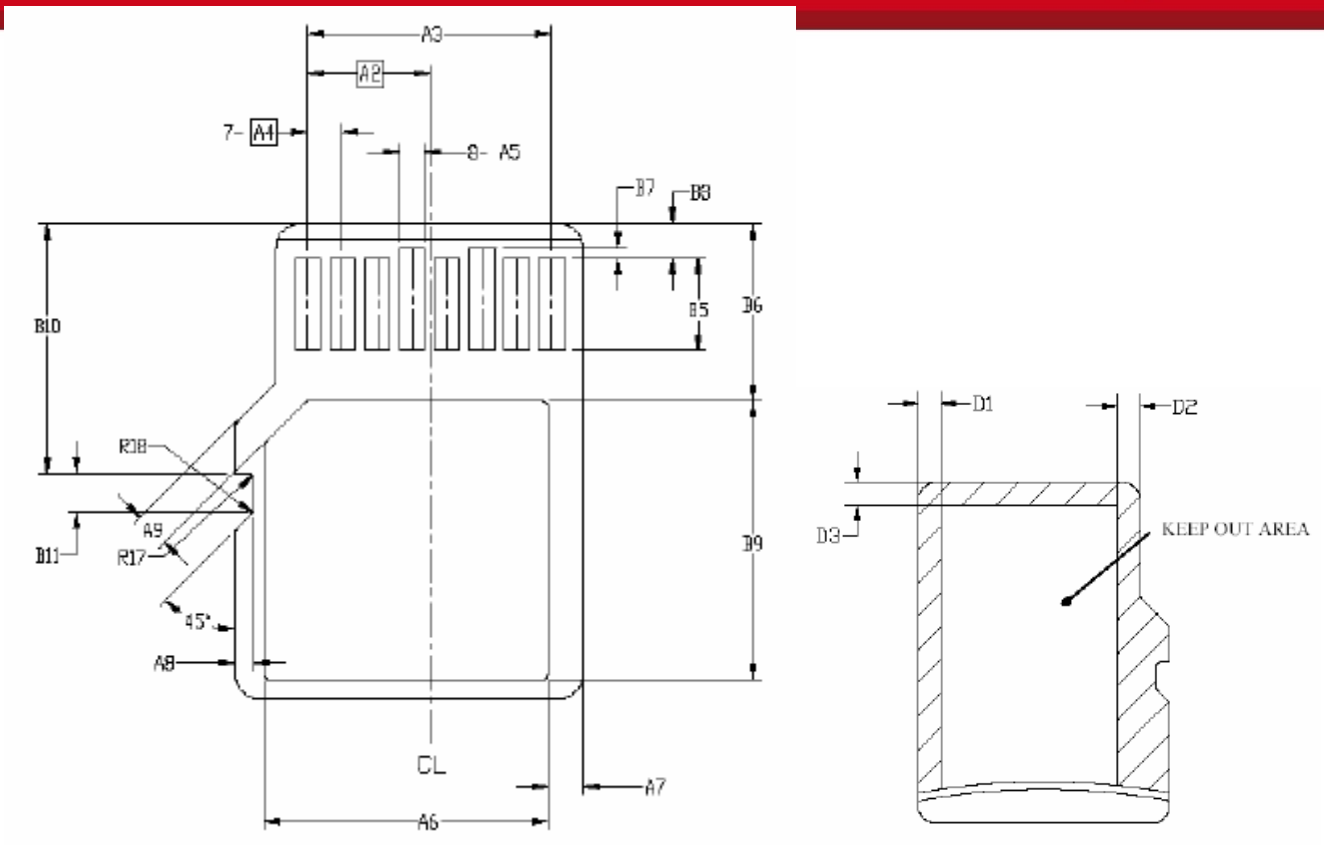


Figure 2. microSD Bottom View and Keep Out Area

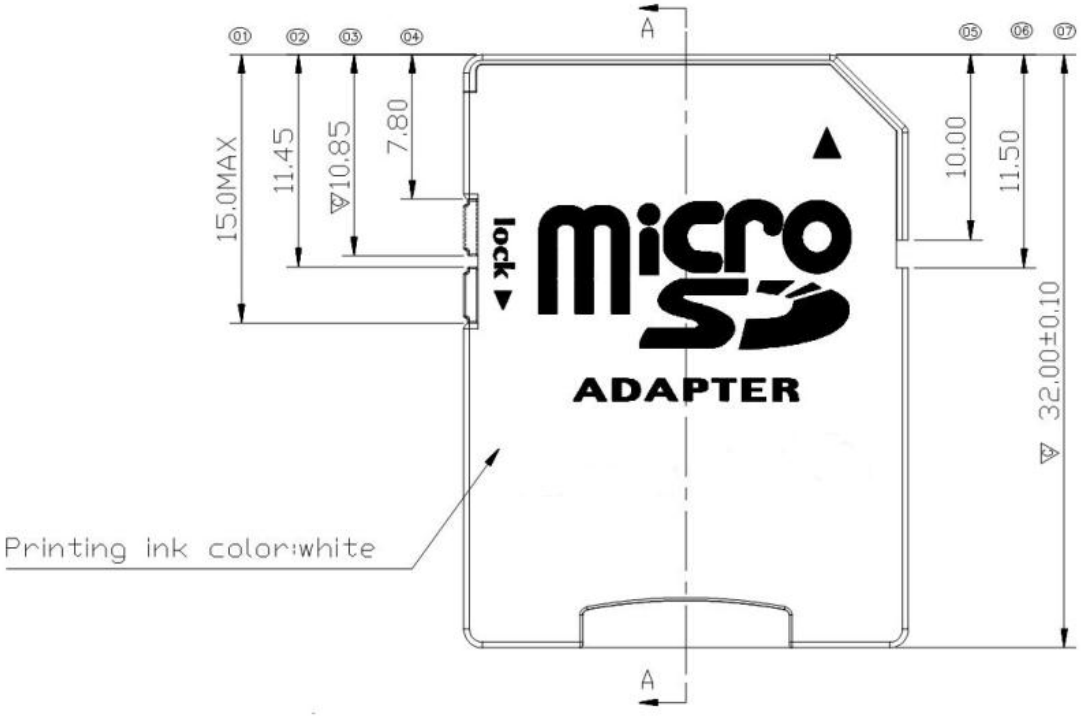


Figure 3. microSD Adapter Top View

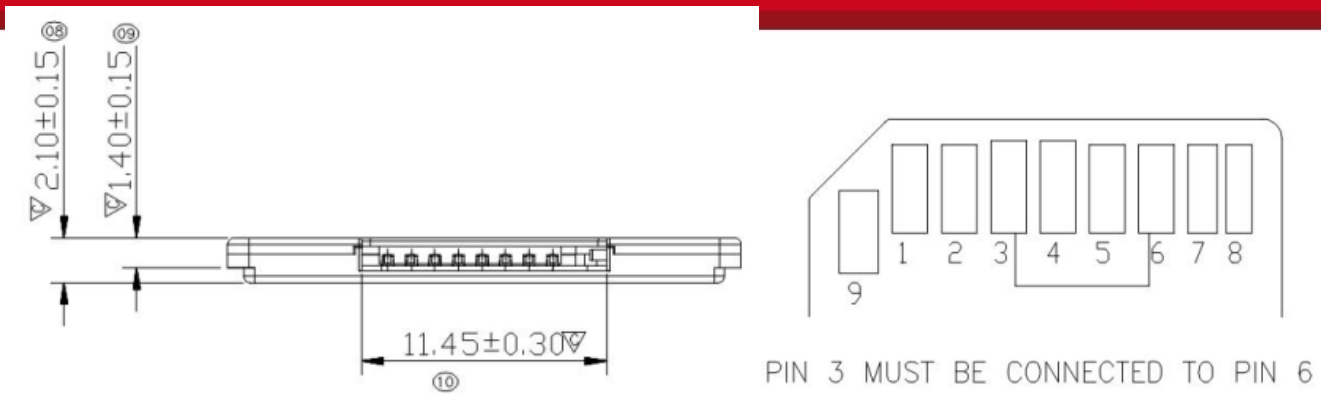


Figure 4. microSD Adapter Contacts

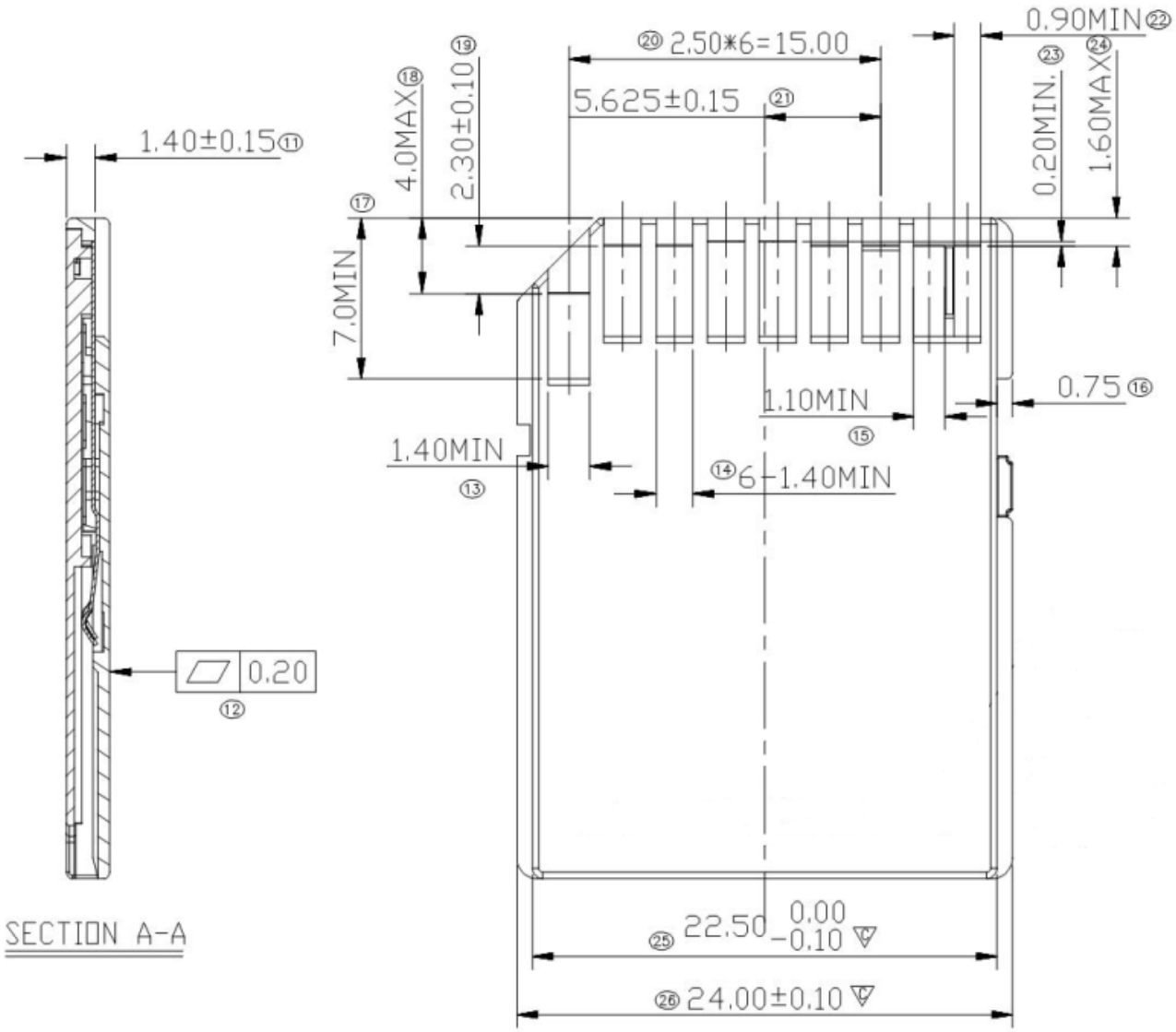


Figure 5. microSD Adapter Bottom and Side Views

Table 6. microSD Memory Card Package - Dimensions

SYMBOL	COMMON DIMENSIONS[1]			NOTE
	MIN[2]	NOM[2]	MAX[2]	
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
C	0.90	1.00	1.10	
C1	0.603	0.703	0.803	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	

SYMBOL	COMMON DIMENSIONS[1] MIN[2]	NOM[2]	MAX[2]	NOTE
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	

Notes:

1. Dimensions are in millimeters.
2. Dimensioning and tolerances per ASME Y14.5M-1994.
3. Coplanarity is additive to C1 max thickness.

3 microSD Card System Concept

The microSD Card provides application designers with a low-cost mass storage device, implemented as a removable card that supports a high security level for content protection, and a compact, easy-to-implement interface. microSD Memory Cards can be grouped into several card classes that differ in the functions they provide (defined by the subset of microSD Memory Card system commands supported by the class).

A microSD Card system includes the microSD Card (or several cards), the bus (SD or SPI), and the Host/Application. Host and Application specifications are beyond the scope of this document. The following sections provide an overview of the card, bus topology, and communication protocols of the microSD Card system. The content protection (security) system description is provided in a separate document.

3.1 Rewritable or Read-only Memory Cards

microSD Memory Cards are available in two formats, as determined by the card manufacturer:

- **Read/Write (RW) card** — (Flash: One Time Programmable – OTP, Multiple Time Programmable – MTP). These cards are typically sold as blank (empty) media and are used for mass data storage, end user video, and audio or digital image recording.
- **Read Only Memory (ROM) card** — ROM cards are manufactured with fixed data content, and are typically used as media for distribution of software, audio, or video content.

3.2 Card Capacity

Two types of microSD Memory Cards are available, differentiated by memory capacity:

- **Standard Capacity** — microSD Memory Card supports capacities up to and including 2GB. All versions of the Physical Specifications define the Standard Capacity microSD Memory Card.
- **High Capacity** — microSDHC Memory Card supports capacities more than 2GB (231 bytes) and this version of the specification limits capacity up to and including 32GB. The High Capacity SDHC Memory Card is recently defined in the “Physical Layer Specification, Version 2.00.”

Only hosts that are compliant to the Physical Layer Specification version 2.00 or higher and the microSD File System Specification Version 2.00 can access High Capacity microSDHC Memory Cards. Other hosts fail to initialize High Capacity microSDHC Memory Cards.

Notes:
1. The Part 1 Physical Layer Specification Version 2.00 and Part 2 File System Specification Version 2.00 allow Standard Capacity microSD Memory Cards to have capacity up to and including 2GB and High Capacity SDHC Memory Cards to have capacity up to and including 32GB. microSDXT Memory Cards with a capacity greater than 32GB will be available with updated versions of Part 1 and Part 2 Specifications.
2. Hosts that can access (read and/or write) SD Memory Cards with a capacity greater than 2GB and up to and including 32GB, shall also be able to access microSD Memory Cards with a capacity of 2GB or less.

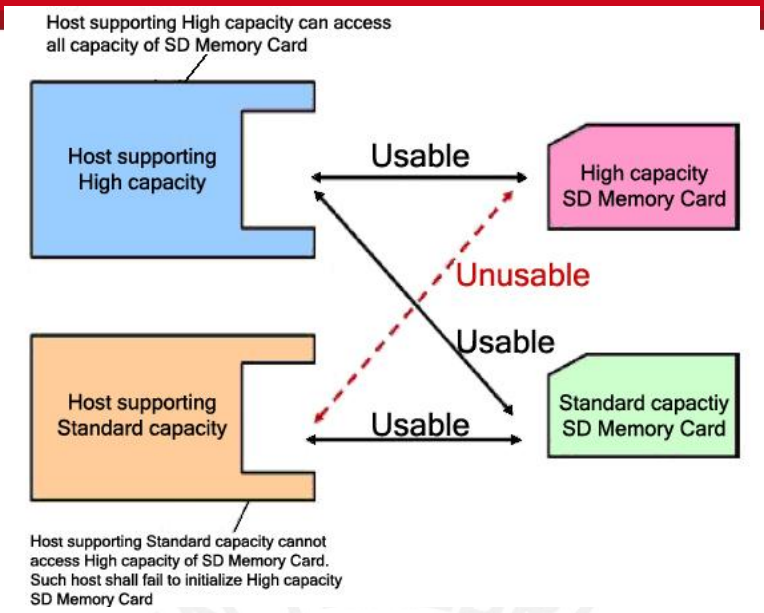


Figure 6. Host/Card Usability

Two types of High Capacity microSDHC Memory Card are specified:

Type A (Single State Card) — This card type has a single High Capacity memory area. Details of Type A are specified in the Physical Layer Specification version 2.00.

Type B (Dual State Card) — This card type has both High Capacity memory areas and Standard Capacity memory areas. In Type B cards, only one memory area can be used at any given time. A mechanical switch is used to select the desired memory area. Details of Type B will be defined in future specifications. It is not necessary for the host to distinguish card types.

3.3 Speed Class

The Secure Digital Association defines a series of *Speed Class Rating* numbers as the official speed measurement for SD cards. The class numbers and their associated performance specifications are shown below:

- **Class 0** — This card class does not specify performance. Class 0 includes all the legacy cards prior to this specification, regardless of performance.
- **Class 2** — equal or greater than 2 MB/s.
- **Class 4** — equal or greater than 4 MB/s.
- **Class 6** — equal or greater than 6 MB/s.
- **Class 10** — equal or greater than 10 MB/s.

Delkin's High Capacity SDHC Memory Cards have a performance rating of Class 6 or higher.

Note: The unit of performance [MB/sec] indicates 1000x1000 [Bytes/sec] while the unit of data size [MB] indicates 1024x1024 [Bytes]. This is because the maximum SD Bus speed is specified by the maximum SD clock frequency (25 [MB/sec] = 25000000 [Bytes/sec] at 50 MHz) and data size is based on memory boundary (power of 2).

3.4 Command System

microSD commands CMD34-37, CMD50, and CMD57 are reserved for microSD command system expansion via the switch command. Switching between the various functions of the command system function group will change the interpretation and associated bus transaction of these commands (i.e., command without data transfer, single block read, and multiple block write). A supporting command system is optional.

- When the "standard command set" (default function 0x0) is selected, these commands will not be recognized by the card and will be considered as illegal commands (as defined in Version 1.01 of the microSD Physical Layer Specification).
- When the “vendor specific” (function 0xE) is selected, the behaviors of these commands are vendor specific. They are not defined by this standard and may change for different card vendors.
- When the “mobile e-commerce” (function 0x1) is selected, the behavior of these commands is governed by the microSD Specifications Part A1: Mobile Commerce Extension Specification.

When either of these extensions is used, special care should be given to proper selection of the command set function. Otherwise, the host command may be interpreted incorrectly.

All other commands of the microSD Memory Card (not reserved for the switch commands) are always available and will be executed as defined in this document regardless of the currently-selected command set.

3.4.1 Send Interface Condition Command (CMD8)

CMD8 (Send Interface Condition Command) is used to initialize SD Memory Cards, compliant to the Physical Specification Version 2.00. CMD8 is valid when the card is in idle state. This command has two functions:

- **Voltage check** — Checks whether the card can operate on the host supply voltage.
- **Enables expansion of existing command and response —** Reviving CMD8 enables expanded functionality to some of the existing commands by redefining previously reserved bits. For example, ACMD41 is expanded to support initialization of High Capacity SDHC Memory Cards.

Table 7. CMD8 Format Description

Bit position	47	46	[45:40]	[39:20]	[19:16]	[15:8]	[7:1]	0
Width (bits)	1	1	6	20	4	8	7	1
Value	‘0’	‘1’	‘001000’	‘00000h’	X	X	X	‘1’
Description	Start bit	Transmission bit	Command index	Reserved bits	Voltage supplied (VHS)	Check pattern	CRC7	End bit

Voltage Supplied	Value Definition
0000b	Not Defined
0001b	2.7-3.6V
0010b	Reserved for Low Voltage Range
0100b	Reserved
1000b	Reserved
Others	Not Defined

When the card is in an Idle state, the host shall issue `CMD8` before `ACMD41`. In the argument, "voltage supplied" is set to the host supply voltage and 'check pattern' is set to any 8-bit pattern. The card checks to determine whether it can operate on the host's supply voltage. The card that accepted the supplied voltage returns an `R7` response. In the response, the card echoes back both the voltage range and check pattern set in the argument. If the card does not support the host supply voltage, it shall not return response and stays in Idle state. Table 8 shows the card operation for `CMD8`.

Table 8. CMD8 Card Operation

Command Argument Check					Response of Card1					
Index	Reserved	VHS	Pattern	CRC	Index	Ver	Reserved	VCA	Pattern	CRC
Don't Care	Don't Care	Don't Care	Don't Care	Error	No Response (CRC Error Indication in the following command)					
Not 8	Don't Care	Don't Care	Don't Care	Correct	Depends on command index					
=8	Don't Care	Mismatch2	Don't Care	Correct	No Response					
=8	Don't Care	Match2	Don't Care	Correct	8	Ver=0	0	Echo Back	Echo Back	Calculate

Notes: 1. Response indicates the actual response the card returns. (Does not include errors during response transfer.)

2. Match means AND for conditions a and b below. Mismatch is other cases.

   a. Only one bit is set to 1 in VHS.

   b. Card supports the host's supply voltage.

3.4.2 Command Functional Difference in High Capacity microSDHC Memory Card

Memory access commands include block read commands (CMD17, CMD18), block write commands (CMD24, CMD25), and block erase commands (CMD32, CMD33). Following are the functional differences between Standard Capacity and High Capacity SDHC Memory Card memory access commands:

- **Command Argument**
  - In High Capacity Cards, the 32-bit argument of memory access commands uses the memory address in block address format. Block length is fixed to 512 bytes.
  - In Standard Capacity Cards; the 32-bit argument of memory access commands uses the memory address in byte address format. Block length is determined by CMD16, for example:
    - Argument 0001h is byte address 0001h in the Standard Capacity Card and 0001h block in the High Capacity Card.
    - Argument 0200h is byte address 0200h in the Standard Capacity Card and 0200h block in the High Capacity Card.
- **Partial Access and Misalign Access**

  Partial access and Misalign access (crossing physical block boundary) are disabled in High Capacity card as the block address is used. Access is only granted based on block addressing.
- **Set Block Length**

  When memory read and write commands are used in block address mode, 512-byte fixed block length is used, regardless of the block length set by CMD16. The setting of the block length does not affect the memory access commands. CMD42 is not classified as a memory access command.

  Data block size shall be specified by CMD16, and the block length can be set up to 512 bytes. Setting block length larger than 512 bytes sets the BLOCK_LEN_ERROR error bit regardless of the card capacity.
- **Write Protected Group**

  The High Capacity SDHC Memory Card does not support write-protected groups. Issuing CMD28, CMD29, and CMD30 generates the ILLEGAL_COMMAND error.

4 microSD Card Interface

The Interface descriptions provided in this section locates the position and orientation of microSD Memory Card contact surfaces (pins) and provides relevant dimensions.

4.1 Pin Assignments

Figure 7 shows the location of the microSD Memory Card pins.

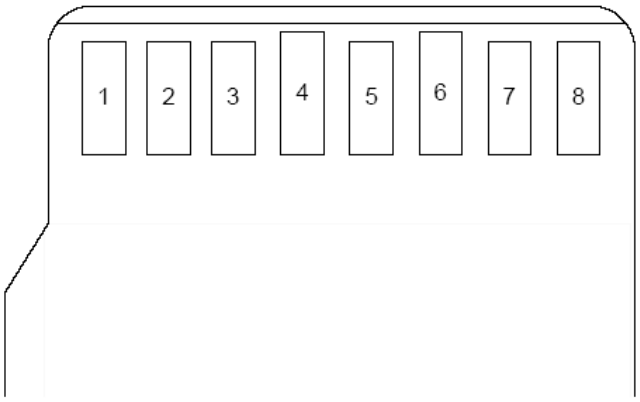


Figure 7. microSD Contacts

4.2 Pin Functions

Table 9 provides the name, type, and function of the microSD Memory Card pins for both the SD and SPI modes.

Table 9. microSD Memory Card Pin Assignments

Pin#	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line[Bit2]	RSV		
2	CD/DAT32	I/O/PP3	Card Detect/Data Line [Bit3]	CS	I	Chip Select (negative true)
3	CMD	PP	Command/Response	DI	I	Data in
4	Vdd	S	Supply voltage	Vdd	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	Vss	S	Supply voltage ground	Vss	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit0]	D0	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [Bit1]	RSV		

Notes: 1. **S** = power supply; **I** = input; **O** = output using push–pull drivers; **PP** = I/O using

push–pull drivers

2. The extended `DAT` line (`DAT1-DAT3`) are input on power up and start to operate as `DAT` lines after the `SET_BUS_WIDTH` command. The Host shall keep its own `DAT1-DAT3` lines in input mode, as well, while they are not used. This is done in order to keep compatibility to Multimedia Cards.
3. After power up, this line is input with 50KΩ pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by the user, during regular data transfer, with the `SET_CLR_CARD_DETECT` (`ACMD42`) command.

4.3 SD Bus Topology

The microSD Card system defines two alternative communication protocols: microSD and SPI. Applications can choose either mode. Mode selection is transparent to the host. The card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. Therefore, applications that use any one communication mode do not have to be aware of the other.

4.3.1 microSD Bus Mode Protocol

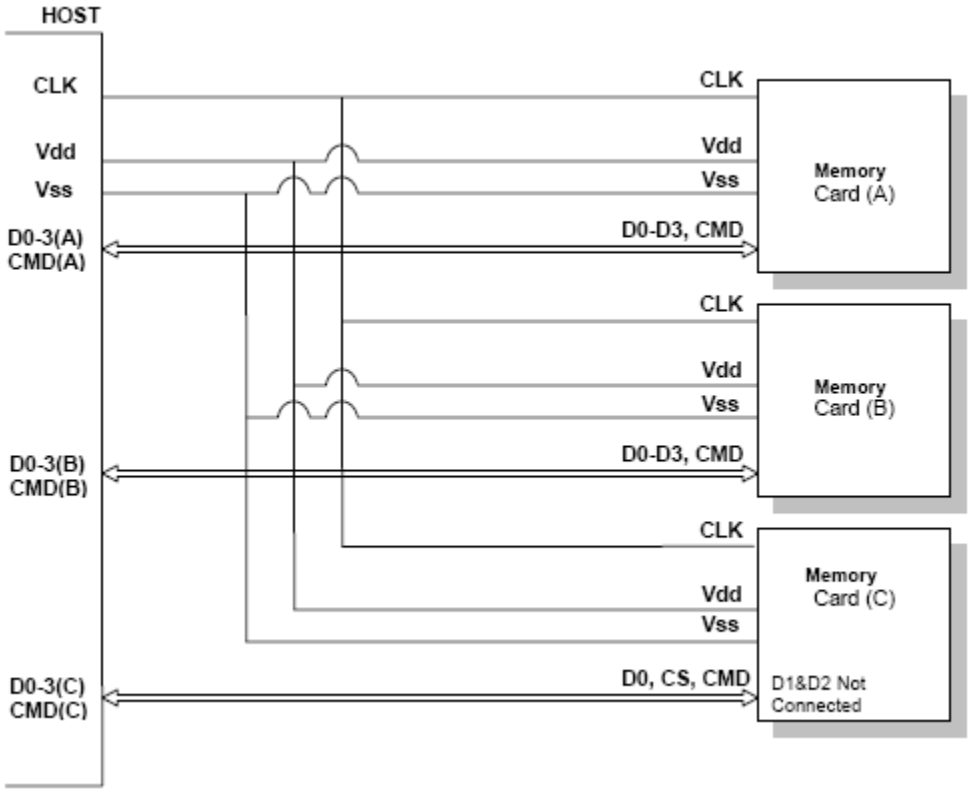


Figure 8. microSD Memory Card System Bus

The microSD bus includes the following signals:

- **CLK** — Host to card clock signal

- **CMD —** Bi-directional Command/Response signals
- **DAT0** - **DAT3 —** Four bi-directional data signals
- **VDD, VSS1, and VSS2 —** Power and ground signals

The microSD Memory Card bus has a signal master (application), multiple slaves (cards), synchronous star topology (see Figure 5). Clock, power, and ground signals are common to all cards. Command (CMD) and data (DAT0 – DAT3) signals are dedicated to each card providing continuous point to point connection to all the cards.

During initialization, process commands are sent to each card individually, allowing the application to detect the cards and assign logical address to the physical slots. Data is always sent (received) to (form) each card individually. However, in order to simplify the handing of the card stack, after the initialization process, all commands may be sent concurrently to all cards. Addressing information is provided in the command packet.

microSD bus allows dynamic configuration of the number of data lines. After power up, by default, the microSD Memory Card will use only DAT0 for data transfer. After initialization the host can change the bus width (number of active data line). This feature allows easy tradeoff between HW cost and system performance.

Note: While DAT1-DAT3 are not in use, the related Host's DAT lines should be in tri-state (input mode).

4.3.2 SPI Bus Mode Protocol

The SPI compatible communication mode of the SD Memory Card is designed for communication with a SPI channel, commonly found in various microcontrollers in the market. The interface is selected during the first reset command after power up and cannot be changed as long as the part is powered on.

The SPI standard defines the physical link only, and not the complete data transfer protocol. The SD Memory Card SPI implementation uses the same command set of the SD mode. From the application point of view, the advantage of the SPI mode is the capability of using an off-the-self host, hence reducing the design-in effort to a minimum. The disadvantage is the loss of performance, relative to the SD mode which enables the wide bus option. The SD Memory Card SPI interface is compatible with SPI hosts available on the market.

As any other SPI device, the SD Memory Card SPI channel consists of the following four signals:

- **CS —** Host to card Chip Select signal
- **CLK —** Host to card clock signal
- **DataIn —** Host to card data signal
- **DataOut —** Card to host data signal

Another SPI common characteristic is byte transfer, which is implemented in the card as well. All data tokens are multiples of byte (8-bit) and are always byte-aligned to the CS signal.

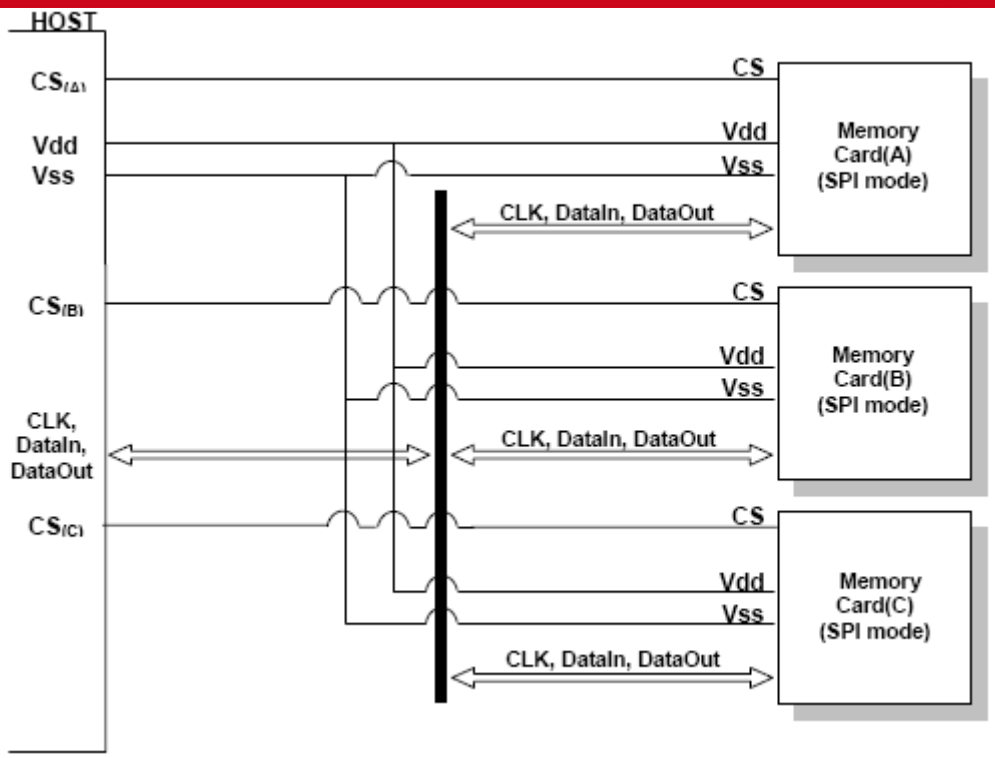


Figure 9. microSD Memory Card SPI System Bus

Card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal (see Figure 8).

The SPI interface uses 6 of the 8 SD bus signals (DAT1 and DAT2 are not used, DAT3 is the CS signal.) of the SD bus.

5 Read and Write Operations

5.1 microSD Bus Protocol

5.1.1 Command

A command is a token which starts an operation. Commands are sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). Commands are transferred serially on the CMD line.

5.1.2 Response

A response is a token, which is sent from an addressed card, or (synchronously) from all connected cards to the host as an answer to a received command. Responses are transferred serially on the CMD line.

5.1.3 Data

Data can be transferred from the card to the host or vice versa. Data is transferred via the DAT line.

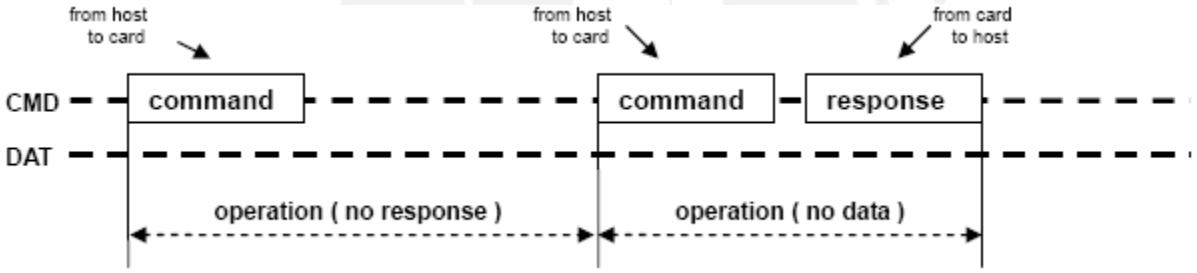


Figure 10. “no response” and “no data” Operations

The basic transaction transfers information directly within the command or response structure. In addition, some operations have a data token.

Data transfer to/from the SD memory card is done in blocks, always succeeded by CRC bits. Single and multiple block operations are defined. Note that the Multiple Block operation mode is better for faster write operation. A multiple block transmission is terminated when a STOP command follows on the CMD line. Data transfer can be configured by the host to use single or multiple data lines.

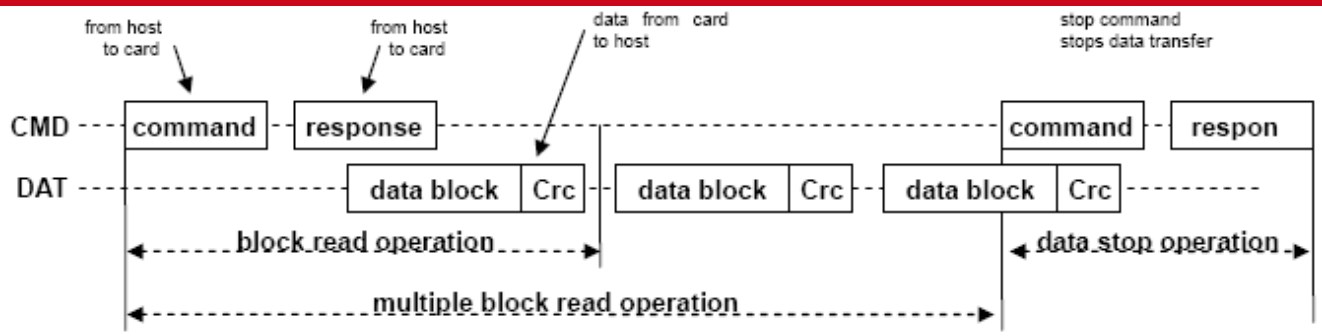


Figure 11. Multiple Block Read Operation

The block write operation uses a simple busy signaling of the write operation duration on the DAT0 data line (see Figure 12), regardless of the number of data lines used for transferring the data.

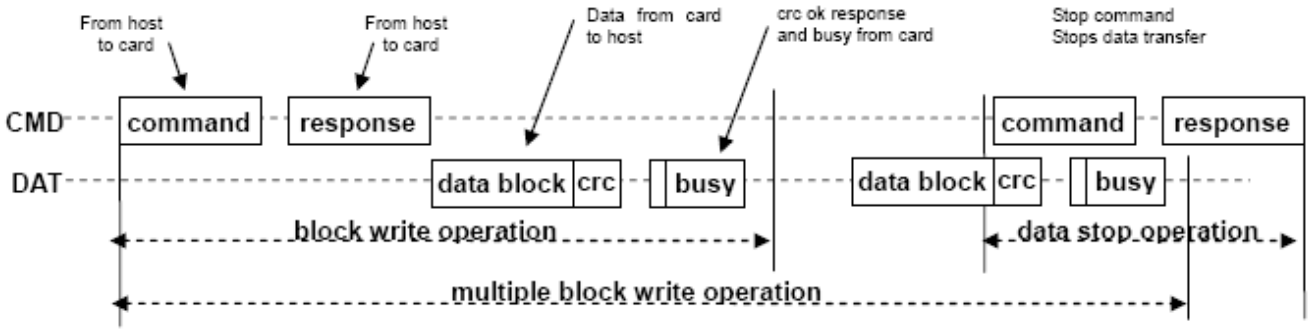


Figure 12. Multiple Block Write Operation

Command tokens use the coding scheme shown below:

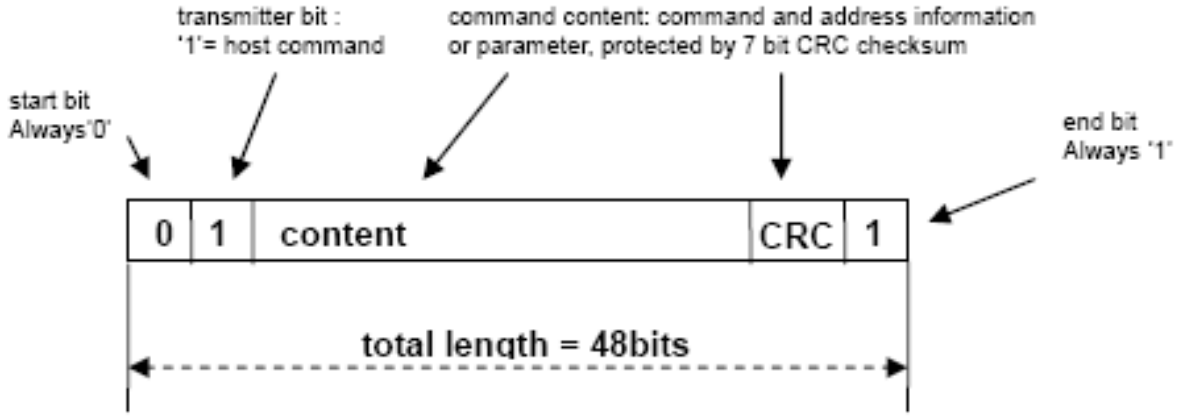


Figure 13. Command Token Format

Each command token is preceded by a start bit and succeeded by an end bit. The total length is 48 bits.

Each token is protected by CRC bits so that transmission errors can be detected and operation may be repeated. Response tokens have four coding schemes, depending on their content. The token length is either 48 or 136 bits.

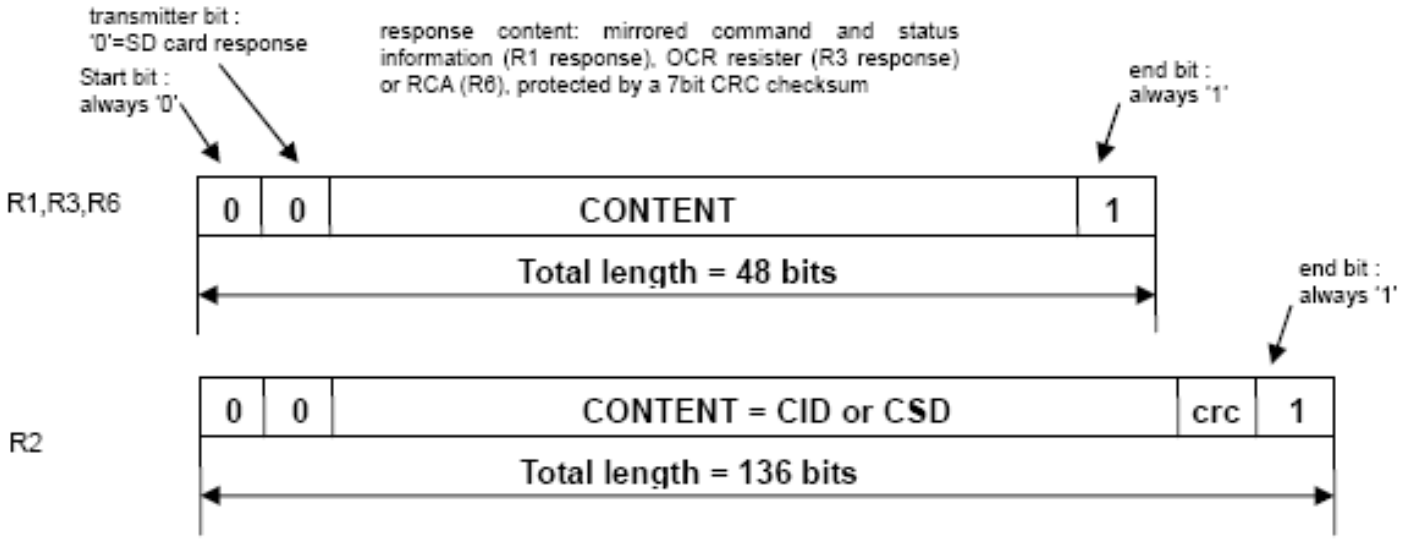


Figure 14. Response Token Format

In the CMD line, the MSB bit is transmitted first and the LSB bit is the last.

When the Wide Bus option is used, the data is transferred 4 bits at a time (see Figure 15). Start when the end bits, as well as the CRC bits are transmitted for every one of the DAT lines. CRC bits are calculated and checked for every DAT line individually. The CRC status response and busy indication will be sent by the card to the host on DAT0 only. (DAT1-DAT3 during that period are “don’t care.”)

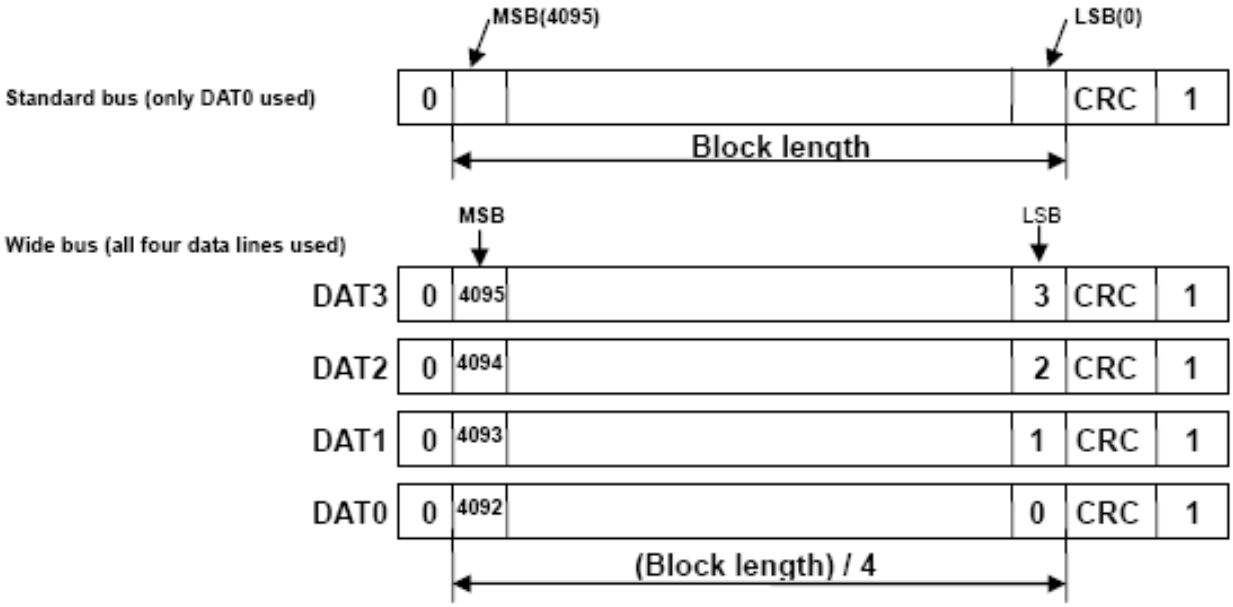


Figure 15. Data Packet Format

5.2 SPI Bus Protocol

While the microSD Channel is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented.

5.2.1 Command

Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal (i.e., the length is a multiple of 8 clock cycles).

5.2.2 Response

The response behavior in the SPI mode differs from the SD mode in the following three aspects:

* The selected card always responds to the command.
* Two new (8- and 16-bit) response structures are used.
* When the card encounters a data retrieval problem, it will respond with an error (which replaces the expected data block) rather than returning a time-out, as in the SD mode.

In addition to the command response, every data block sent to the card during write operations will be acknowledged with a special data response token.

5.2.3 Data Read

Single and multiple blocks read commands are supported in SPI mode. However, in order to comply with the SPI industry standard, only two (unidirectional) signals are used. Upon reception of a valid read command the card will respond with a response token followed by a data token of the length defined in a previous `SET_BLOCKLEN` (`CMD16`) command. A multiple block read operation is terminated, similar to the SD protocol, with the `STOP_TRANSMISSION` command.

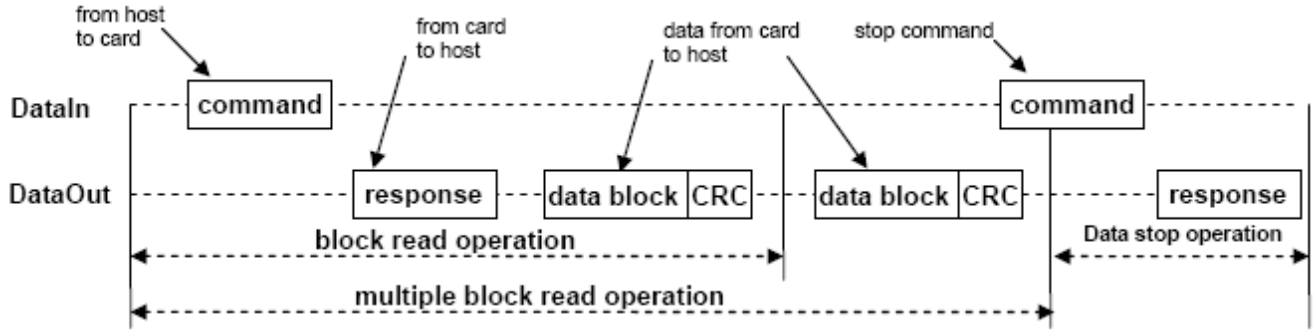


Figure 16. Read Operation

A valid data block suffixed with a 16 CRC generated by the standard CCITT polynomial $X^{16}+X^{12}+X^{5}+1$. In the case of data retrieval error, the card will not transmit any data. Instead, a special data error token will be sent to the host. Figure 17 shows a data read operation which terminated with an error token.

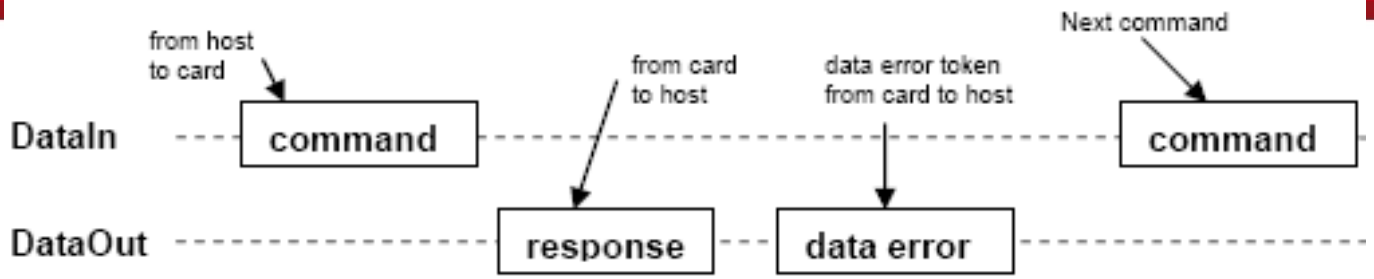


Figure 17. Read Operation – Data Error

Single and multiple block write operations are supported in SPI mode. Upon receipt of a valid write command, the card replies with a response token, and then waits for a data block to be sent from the host. CRC suffix, block length, and start address restrictions are identical to the read operation. (See Figure 17.)

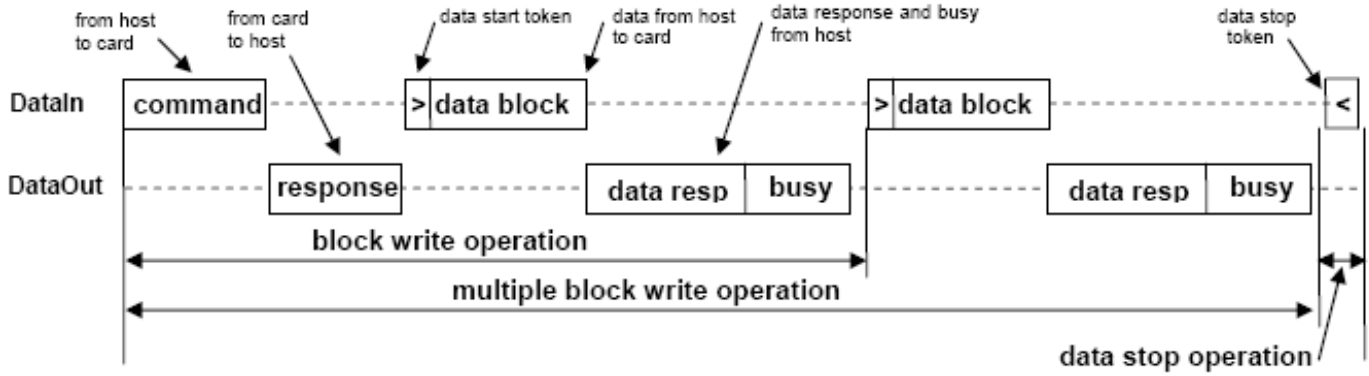


Figure 18. Write Operation

After a data block has been received, the card will respond with a data-response token. If the data block has been received without errors, it will be programmed. As long as the card is busy programming, a continuous stream of busy tokens will be sent to the host (effectively holding the `Data Out` line low).

5.3 Card Registers

Six registers are defined within the card interface: OCR, CID, CSD, RCA, DSR and SCR. These can be accessed only by corresponding commands. The OCR, CID, CSD and SCR registers carry the card- and content-specific information, while the RCA and DSR registers are configuration registers, storing actual configuration parameters.

In order to enable future extension, the card shall return `0` in the reserved register bits.

5.3.1 OCR Register

The 32-bit operation conditions register stores the voltage profile of the card. Additionally, this register includes status information bits. One status bit is set if the card power up procedure has been finished. This register includes another status bit indicating the card capacity status after set power up status bit. The OCR register shall be implemented by the cards.

The 32-bit operation conditions register stores the voltage profile of the card. Bit 7 of OCR is newly defined for Dual Voltage Card and set to 0 in default. If a Dual Voltage Card does not receive CMD8, OCR bit 7 in the response indicates 0, and the Dual Voltage Card which received CMD8, sets this bit to 1.

Additionally, this register includes two more status information bits.

* **Bit 31** — Card power up status bit. This status bit is set if the card power up procedure has completed.
* **Bit 30** — Card capacity status bit. This status bit is set to 1 if the card is High Capacity SDHC Memory Card. 0 Indicates that the card is Standard Capacity SD Memory Card. The Card Capacity status bit is valid after the card power up procedure is completed and the card power up status bit is set to 1. The Host shall read this status bit to identify a Standard or High Capacity SDHC Memory Card. The OCR register shall be implemented by the cards.

Table 10. OCR Register Definition

OCR bit position	OCR Fields Definition
0-3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved for Low Voltage Range
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	2.7-2.8
16	2.8-2.9
17	2.9-3.0
18	3.0-3.1
19	3.1-3.2
20	3.2-3.3
21	3.3-3.4
22	3.4-3.5
23	3.5-3.6
24-29	Reserved
30	Card Capacity Status (CCS)1
31	Card power up status bit (busy)2

VDD Voltage Window

Notes: 1. This bit is valid only when the card power up status bit is set.
2. This bit is set to LOW if the card has not finished the power up routine.

The supported voltage range is coded as shown in Table 10. A voltage range is not supported if the corresponding bit value is set to LOW. As long as the card is busy, the corresponding bit (31) is set to LOW.

5.3.2 CID Register

The Card Identification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual Read/Write (RW) card shall have a unique identification number.

Table 11. CID Register Definition

Name	Field	Width	CID-slice
Manufacturer ID	MID	8	[127:120]
OEM/Application ID	OID	16	[119:104]
Product name	PNM	40	[103:64]
Product revision	PRV	8	[63:56]
Product serial number	PSN	32	[55:24]
Reserved	--	4	[23:20]
Manufacturing date	MDT	12	[19:8]
CRC7 checksum	CRC	7	[7:1]
Not used (always 1)	--	1	[0:0]

The structure of the CID register is defined as follows:

* **MID**

  An 8-bit binary number that identifies the card manufacturer. The MID number is controlled, defined, and allocated to a SD Memory Card manufacturer by the SD-3C, LLC. This procedure is established to ensure uniqueness of the CID register.

* **OID**

  A two-character ASCII string that identifies the card OEM and/or the card contents (when used as a distribution media either on ROM or FLASH cards). The OID number is controlled, defined, and allocated to an SD Memory Card manufacturer by the SD-3C, LLC. This procedure is established to ensure uniqueness of the CID register.

  Note: SD-3C, LLC licenses companies that wish to manufacture and/or sell SD Memory Cards, including but not limited to flash memory, ROM, OTP, RAM, and SDIO Combo Cards. The SD-3C, LLC is a limited liability company established by Matsushita Electric Industrial Co. Ltd., SanDisk Corporation and Toshiba Corporation.

* **PNM**

  The product name is a string, five-character ASCII string.

* **PRV**

  The product revision is composed of two Binary Coded Decimal (BCD) digits, four bits each, representing an “n.m” revision number. The “n” is the most significant nibble and “m”

is the least significant nibble. For example, the PRV binary value field for product revision "6.2" will be 0110 0010b.

5.3.3 CSD Register

The Card-Specific Data register provides information regarding access to card contents. The CSD defines the data format, error correction type, maximum data access time, whether the DSR register can be used, etc. The programmable part of the register (indicated by R, W or W1, see Table 12 below) can be changed by CMD27.

5.3.4 CSD_STRUCTURE

Field structures of the CSD register differ, depending on the Physical Specification Version and Card Capacity. The CSD_STRUCTURE field in the CSD register indicates its structure version.

5.3.5 CSD Register (CSD Version 2.0)

Table 12 shows Definition of the CSD for the High Capacity SDHC Memory Card (CSD Version 2.0). This section describes the CSD fields and the relevant data types for the High Capacity SDHC Memory Card.

CSD Version 2.0 is applied to only the High Capacity SDHC Memory Card. The field name in parenthesis is set to fixed value and indicates that the host is not necessary to refer these fields. The fixed values enables host, which refers to these fields, to keep compatibility to CSD Version 1.0. The Cell Type field is coded as follows:

* **R** — Readable
* **W(1)** — Writable once
* **W** — Writable multiple times

Table 12. CSD Register Fields (Version 2.0)

Name	Field	Width	Value	Cell Type	CSD-slice
CSD structure Reserved	CSD_STRUCTURE -	2 6	01b 00 0000b	R	[127:126] [125:120]
Data read access-time	(TAAC)	8	0Eh	R	[119:112]
Data read access-time in CLK Cycles (NSAC*100)	(NSAC)	8	00h	R	[111:104]
Max. data transfer rate	(TRAN_SPEED)	8	32h or 5Ah	R	[103:96]
Card command classes	CCC	12	01x11011010 1b	R	[95:84]
Max. read data block length	(READ_BL_LEN)	4	9	R	[83:80]
Partial blocks for read allowed	(READ_BL_PARTIAL)	1	0	R	[79:79]
Write block misalignment	(WRITE BLK MISALIGN)	1	0	R	[78:78]
Read block misalignment	(READ_BLK_MISALIGN)	1	0	R	[77:77]

Name	Field	Width	Value	Cell Type	CSD-slice
DSR implemented	DSR_IMP	1	x	R	[76:76]
Reserved	-	6	00 0000b	R	[75:70]
Device size	C SIZE	22	00 xxxxh	R	[69:48]
Reserved	-	1	0	R	[47:47]
Erase single block enable	(ERASE_BLK_EN)	1	1	R	[46:46]
Erase sector size	(SECTOR_SIZE)	7	7Fh	R	[45:39]
Write protect group size	(WP_GRP_SIZE)	7	0000000b	R	[38:32]
Write protect group enable Reserved	WP_GRP_ENABLE)	1 2	0 00b	R	[31:31] [30:29]
Write speed factor	(R2W_FACTOR)	3	010b	R	[28:26]
Max. write data block length	(WRITE_BL_LEN)	4	9	R	[25:22]
Partial blocks for write allowed Reserved	(WRITE_BL_PARTIAL -	1 5	0 00000b	R	[21:21] [20:16]
File format group	(FILE _FORMAT_GRP)	1	0	R	[15:15]
Copy flag (OTP)	COPY	1	x	R/W(1)	[14:14]
Permanent write protection	PERM_WRITE_PROTECT	1	x	R/W(1)	[13:13]
Temporary write protection	TMP_WRITE_PROTECT	1	x	R/W	[12:12]
File format	(FILE_FORMAT)	2	00b	R	[11:10]
Reserved	-	2	00b	R	[9:8]
CRC	CRC	7	xxxxxxxb	R/W	[7:1]
Not used, value is always 1	-	1	1	-	[0:0]

CSD register fields are defined as follows:

* **TAAC**

  This field is fixed on 0Eh, which indicates 1 ms. The host should not use TAAC, NSAC, and R2W_FACTOR to calculate timeout, and should use fixed timeout values for read and write operations.

* **NSAC**

  This field is fixed to 00h. NSAC should not be used to calculate time-out values.

* **TRAN_SPEED**

  Definition of this field is same as in CSD Version1.0.

* **CCC**

  Definition of this field is same as in CSD Version1.0.

* **READ_BL_LEN**

  This field is fixed to 9h, which indicates READ_BL_LEN=512 Byte.

* **READ_BL_PARTIAL**

  This field is fixed to 0, which indicates partial block read is inhibited and only unit of block access is allowed.

* **WRITE _BLK_MISALIGN**

  This field is fixed to 0, which indicates write access crossing physical block boundaries is always disabled in High Capacity SDHC Memory Cards.

* **READ_BLK_MISALIGN**

  This field is fixed to 0, which indicates read access crossing physical block boundaries is always disabled in High Capacity SDHC Memory Cards.

* **DSR_IMP**

  Definition of this field is same as in CSD Version 1.0.

* **C_SIZE**

  This field is expanded to 22 bits and can indicate up to 2TB. This is the same as the maximum memory space specified by a 32-bit block address.

  This parameter is used to calculate the user data area capacity in the SD Memory Card (not include the protected area). The user data area capacity is calculated from `C_SIZE` as follows:

  Memory capacity = `(C_SIZE+1) x 512K bytes`.

  As the maximum capacity of the Physical Layer Specification, Version 2.00 is 32GB; the upper six bits of this field shall be set to `0`.

* **ERASE_BLK_EN**

  This field is fixed to 1, which means the host can erase one or multiple units of 512 bytes.

* **SECTOR_SIZE**

  This field is fixed to 7Fh, which indicates 64K bytes. This value does not relate to the erase operation. Version 2.00 cards indicate memory boundaries by AU size and this field should not be used.

* **WP_GRP_SIZE**

  This field is fixed to 00h. The High Capacity SDHC Memory Card does not support write protected groups.

* **WP_GRP_ENABLE**

  This field is fixed to 0. The High Capacity SDHC Memory Card does not support write protected groups.

* **R2W_FACTOR**

  This field is fixed to 2h, which indicates 4 multiples. Write timeout can be calculated by multiplying the read access time and R2W_FACTOR. However, the host should not use this factor and should use 250 ms for write timeout.

* **WRITE_BL_LEN**

  This field is fixed to 9h, which indicates `WRITE_BL_LEN=512` bytes.

* **WRITE_BL_PARTIAL**

  This field is fixed to 0, which indicates partial block read is inhibited and only unit of block access is allowed.

* **FILE_FORMAT_GRP**

  This field is set to 0. Host should not use this field.

* **COPY**

  Definition of this field is same as in CSD Version 1.0.

* **PERM_WRITE_PROTECT**

  Definition of this field is same as in CSD Version 1.0.

* **TMP_WRITE_PROTECT**

  Definition of this field is same as in CSD Version 1.0.

* **FILE_FORMAT**

  This field is set to 0. Host should not use this field.

* **CRC**

  Definition of this field is same as in CSD Version1.0.

* **RCA Register**

  The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is `0x0000`. The value `0x0000` is reserved to set all cards into the Stand-by State with `CMD7`.

* **DSR Register (Optional)**

  The 16-bit Driver Stage Register can be used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate, or number of cards). The CSD register carries the information about the DSR register usage. The default value of the DSR register is `0x404`.

* **SCR Register**

  In addition to the CSD register, there is another configuration register named SD CARD Configuration Register (SCR). SCR provides information on the SD Memory Card's special features that were configured into the given card. The size of SCR register is 64 bits. This register shall be set in the factory by the SD Memory Card manufacturer.

  Table 13 describes the SCR register content.

Table 13. SCR Fields

Description	Field	Width	Cell Type	SCR Slice
SCR Structure	SCR_STRUCTURE	4	R	[63:60]
SD Memory Card – Spec. Version	SD_SPEC	4	R	[59:56]
Data_status_after erases	DATA_STAT_AFTER_ERASE	1	R	[55:55]
SD Security Support	SD_SECURITY	3	R	[54:52]
DAT Bus widths supported	SD_BUS_WIDTHS	4	R	[51:48]
Reserved	-	16	R	[47:32]
Reserved for manufacturer usage	-	32	R	[31:0]

Table 14. SCR Register Structure Versions

SCR_STRUCTURE	SCR Structure Version	SD Physical Layer Spec Version
D	SCR Version 1.0	Version 1.01 - 2.00
1-15	Reserved	

* **SD_SPEC**

  Describes the Physical Layer Specification Version supported by the card.

Table 15. Physical Layer Specification Version

SD_SPEC	Physical Layer Specification Version Number
0	Version 1.0-1.01
1	Version 1.10
2	Version 2.00
3-15	Reserved

* **DATA_STAT_AFTER_ERASE**

  Defines the data status after erase, whether it is 0 or 1, the status is card vendor dependent.

* **SD_SECURITY**

  Describes the Security Specification Version supported by the card.

Table 16. SD-supported Security Algorithm

SD_SECURITY	Security Specification Version
0	No security
1	Not used
2	Version 1.01
3	Version 2.00
4-7	Reserved

Note that it is mandatory for a writable SD Memory Card to support Security Protocol. For ROM and OTP types of the SD Memory Card, this security feature is optional. In the case of the Standard Capacity SD Memory Card Version 1.01, this field shall be set to 2. For the High Capacity SDHC Memory Card, this field shall be set to 3.

* **SD_BUS_WIDTHS**

The following table describes all of the DAT bus widths that are supported by this card.

Table 17. SD Memory Card Supported Bus Widths

SD_BUS_WIDTHS	Supported Bus Widths
Bit 0	1 bit (DAT0)
Bit 1	Reserved
Bit 2	4 bit (DAT0-3)
Bit 3	Reserved

Since the SD Memory Card supports at least the two bus modes 1-bit or 4-bit width, then any SD card shall set at least bits 0 and 2 (`SD_BUS_WIDTH=0101`).

File Systems

HCC has been developing embedded file systems for more than a decade and has a highly optimized range of file systems designed to meet the performance requirements of any application. Using HCC file systems will make your application more reliable and will help to protect your customer's data. HCC file systems can be seamlessly dropped into any environment to support any storage media, RTOS, compiler or microcontroller.

File Systems

Five highly optimized file systems: Each file system is finely tuned to provide the best performance for its intended environment. With full support for traditional FAT and Flash systems, developers can choose a system optimized for flexibility, performance or resource-limited environments.

Extensive target media drivers: HCC collaborate closely with the industry's leading storage suppliers and can provide support for almost any flash device or storage medium. We routinely supply drivers for everything from simple USB pen drives and SD cards, to the most advanced NAND and NOR flash.

No-compromise fail-safety: HCC has developed truly fail-safe file systems that guarantee the highest possible data integrity.

With abstractions for more than 15 real-time operating systems, and our broad range of products, our one-size-doesn't-fit-all approach is sure to provide an optimal solution for most applications. Why not get a file system that is designed to meet your particular needs and ensure that your data is securely, efficiently and reliably cared for?

FAT File Systems

All of HCC's FAT-compatible file systems can be used with NAND and NOR memories in conjunction with our fail-safe Flash Translation Layer, SafeFTL, which acts as the driver and provides wear-leveling, bad block management and error correction.

FAT: High Performance 12/16/32 FAT File System. Full featured FAT file system optimized for high-performance with FAT12/16/32-compliant media. There's extensive support for external media, including SD/MMC and Compact flash cards, or any device arranged as an array of logical sectors.

THIN: File System for Resource-Limited Applications. Full-featured FAT file system for MCUs with limited resources. THIN is compatible with media such as SD/MMC and Compact flash cards. The code has been designed to provide a balance of speed vs. memory, with options that allow the developer to make performance trade-offs using available resources. This permits a full file system to be run on a low-cost microcontroller with limited resources.

SafeFAT: Fail-safe File System. Robust, full featured fail-safe FAT file system that provides the same features as a standard FAT file system. It implements a system of journaling/transaction operations that provide the strongest possible assurance that all memory operations will be performed correctly, and that the system can recover coherently from unexpected events such as reset or power loss.

Flash File Systems

SafeFLASH: Fail-safe File System. Designed for high performance and 100% fail-safety. It can be used with all NOR and NAND flash as well as any media that can simulate a block-structured array. SafeFLASH supports dynamic and static wear-leveling and provides a highly efficient solution in which data integrity is critical.

TINY: Fail-safe Limited Resource File System. A full-featured, fail-safe flash file system for use in resource-constrained applications. TINY is designed for use with NOR Flash with erasable sectors <4kB. Typical devices include Atmel DataFlash AT45, MSP430 internal flash, and many serial flash devices including ST and Microchip SST Serial Flash. It eliminates many fragmentation and flash management problems and results in a compact and reliable file system that provides a full set of features, even on a low-cost controller.

Advanced Fail-safety

Conventional FAT file systems are not fail-safe and often experience difficulties when common problems such as power loss or unexpected resets occur. Corrupt files can sometimes be corrected using 'check-disk' but this requires manual intervention and often valuable data is lost.

Product quality and performance can be seriously undermined by this kind of problem, but the threat can be eliminated by using a robust fail-safe file system from HCC. When used in a correctly designed system, it will guarantee that data will always be consistent. Our file systems are transaction-based but permit single file operation without reference to the rest of the system. In order to ensure the maximum integrity, our media drivers are also designed to provide fail-safe behavior. We have some of the industry's leading experience in this area, why not talk to us about how to implement your application in the most robust way possible?

Supported Flash & Media Devices

HCC supports a huge array of storage media from the most basic USB pen-drive to the most complex Solid State Drive (SSD). The number and variety of available flash devices changes at an incredible rate. Nonetheless, HCC supports hundreds of flash devices from manufacturers including Atmel, Intel, Micron, Toshiba, Hynix, Samsung, Spansion, Numonyx, Macronix, Winbond and many others. We support hundreds of flash parts as well as numerous specialty devices including Solid State Drives (SSD), MLC flash and ClearNAND. All HCC file systems conform to a standard API and are fully interchangeable.
Our fail-safe Flash Translation Layer, SafeFTL, can be used in conjunction with our file systems to provide wear-leveling, bad block management and error correction for almost any known device.

	FAT	THIN	SafeFAT	SafeFLASH	TINY
NAND Flash	Y*	Y*	Y*	Y	N
NOR Flash	Y*	Y*	Y*	Y	Y*
Small Sector NOR	Y*	Y*	Y*	Y	Y
MMC/SD/SDHC/SDXC	Y	Y	Y	N	N
Compact Flash	Y	Y	Y	N	N
SSD Flash	Y	Y	Y	N	N
USB Mass Storage	Y	Y	Y	N	N
RAM	Y	Y	Y	Y	Y

* Requires SafeFTL flash translation layer.

Broad Range of Target Processors & Tools

HCC usually delivers file systems with tested drivers that are fully abstracted for a particular real-time operating system, micro-controller and compiler. In most cases there is little or no integration effort required by developers.

RTOS Abstractions

RTOS abstractions are available for the following systems: CMX RTX, eCOS, emBOS, EUROS, FreeRTOS, Keil RTX, Nucleus, Quadros RTXC, ThreadX, µ-velOSity, µC/OS-II, and many others. Importantly, for custom schedulers and super loops, HCC offers an abstraction for 'No RTOS'. We also offer our own eTaskSync, a small cooperative scheduler, which is designed to handle all processing and interface requirements of HCC middleware. This means that developers can choose our robust quality and outstanding performance irrespective of their legacy software.

Extensive Compiler Support

Eclipse/GCC, IAR Embedded Workbench, Keil ARM Compiler, Freescale CodeWarrior, Atmel AVR Studio, Green Hills Multi, Microchip MPLAB, Renesas HEW, TI Code Composer Studio, Mentor CodeSourcery, Atollic True Studio and many more.

Microcontrollers

Atmel AVR32, SAM3/7/9; ARM Cortex-M0/M3/M4, ARM7/9/11; Freescale ColdFire, Kinetis, PowerPC, i.MX; Infineon C164; Microchip PIC24, PIC32; NXP LPC1300/1700/1800/2000/3000/4000; Renesas SH-2A, RX600; STMicroelectronics STM32; Texas Instruments MSP430, Stellaris, C2000, Hercules, DaVinci, Sitara.

Licensing & Purchasing

All HCC reusable software components are royalty-free and distributed in source form with support and maintenance included for one year with all purchases. We deliver sample projects tailored to an environment agreed with customers to ensure the quickest possible start. Visit HCC's website to find a sample license and to obtain the contact details of your local sales representative. Or, simply send an email to info@hcc-embedded.com and we will send all the details you require.

HCC embedded

US sales office: 444 East 82nd Street New York NY 10028 • **Tel:** +1 212 734 1345
European sales offices: 24a Melville St, Edinburgh EH3 7NS Scotland, UK • **Tel.:** +44 7918 787 571
1133 Budapest, Váci út 76., Hungary • **Tel.:** +36 1 450 1302
info@hcc-embedded.com • sales@hcc-embedded.com • **www.hcc-embedded.com**

CMOS Image Sensor
with Image Signal Processing

HV7131GP

V2.4

Revision History

Revision	Script Date	Comments
V1.0	2001/11/08/Thu – 2001/11/14/Thu	- HV7131GP Preliminary is released
V1.1	2001/12/21/Fri	- Gamma slope table of Knee/De-Knee is added, and some misprints are corrected
V1.2	2002/03/25/Mon	- Knee/De-Knee function is abandoned, instead 10bit ADC is implemented. - Register descriptions are revised - Frame timing is revised.
V1.3	2002/04/25/Thu	- register information is updated
V1.4	2002/05/06/Mon	- Data output timing & interface is added
V1.5	2002/05/13/Tue	- Chip layout information is revised, and miscellaneous typo errors are corrected
V1.6	2002/05/28/Tue	- chip layout information is omitted for confidentiality, and power consumption information is added.
V1.7	2002/06/14/Fri	- CLCC 40 Pin Diagram added
V1.8	2002/12/26/Thu.	- PKG Drawing Added
V1.9	2003/01/17/Fri.	- Register Description Revision
V2.0	2003/06/04/Wed.	- 40 pin diagram revision
V2.1	2003/07/10/Thu..	- ENB Setting guide information is added
V2.2	2003/12/11/Thu..	- C[7:0] PAD information is added.
V2.3	2004/06/26/Sat	-I2C Data Hold Time Revision - External pull-up/ pull-down resistance is added
V2.4	2004/10/29/Fri	- Value of SNR, Dynamic Range, Sensitivity is added at Features.

Disclaimer

This document is a general product description and is subject to change without notice. MagnaChip Semiconductor Ltd., assumes no responsibility or liability arising from use of circuit described, and no patent licenses are implied.

CONTENTS

General Description

HV7131GP is a highly integrated single chip CMOS color image sensor implemented by proprietary MagnaChip 0.35um CMOS sensor process realizing high sensitivity and wide dynamic range. Total pixel array size is 652x492, and 652x488 pixels are active. Each active pixel composed of 4 transistors has a micro-lens to enhance sensitivity, and converts photon energy to analog pixel voltage. On-chip 10bit Analog to Digital Converter (ADC) digitizes analog pixel voltage, and on-chip Correlated Double Sampling (CDS) scheme reduces Fixed Pattern Noise (FPN) dramatically. General image processing functions such as gamma correction, color interpolation, color correction, color space conversion, auto exposure, and auto white balance are implemented to diversify its applications, and various output formats are supported for the sensor to easily interface with different video codec chips. The integration of sensor function and image processing functions make HV7131GP especially very suitable for mobile imaging systems such as IMT-2000 phone's video part that requires very low power and system compactness.

Features

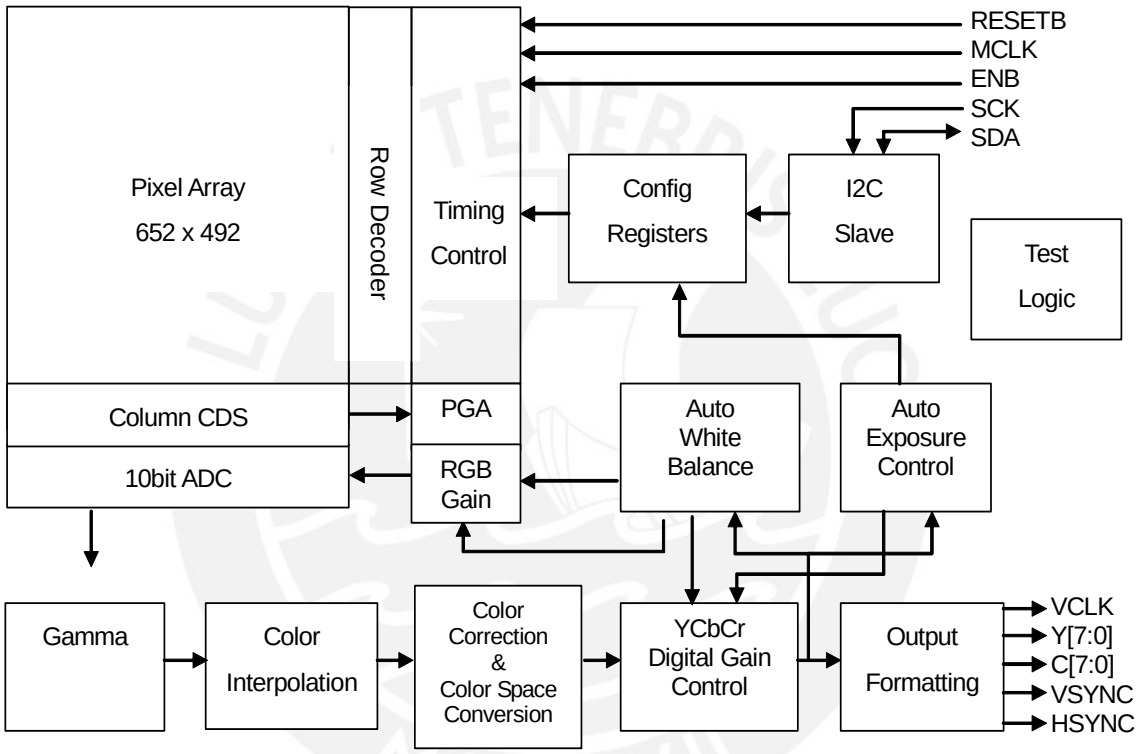
- 1/4 inch optical format
- Total pixel : 652 x 492 / Active pixel : 652x488
- 5.6um x 5.6um active square pixel
- Micro-lens for high sensitivity
- RGB mosaic color filter array
- On-chip 10 bit ADC
- Correlated double sampling for reduction of Fixed Pattern Noise
- Black Level Compensation
- Gamma correction by programmable piecewise linear approximation
- 3x3 Color interpolation
- Color correction by programmable 3x3 matrix operation
- Color space conversion from RGB to YCbCr
- Sub-sampling Modes : 1/4, 1/16
- Various output formats : YCbCr 4:2:2, YCbCr 4:4:4, RGB 4:4:4, Bayer
- 8bit / 16bit Data Bus Mode
- Automatic Exposure Control
- Automatic White Balance Control
- Frame Rate : 30 f/s at 25Mhz, HBLANK = 208, VBLANK = 8
- Power Consumption: 86mW @ 30f/s and 2.8V, 68mW @ 15f/s and 2.8V, 336uW @ power down
- Operation Voltage Range : 2.6V ~ 3.0V, Operation Temperature : -10 ~ +50 degrees Celsius

- Package Types : CLCC 40 PIN, COB(Chip-on-Board), COF(Chip-on-Flex)

  * To the matter concerning package, Wafer business companies are unrelated contents.

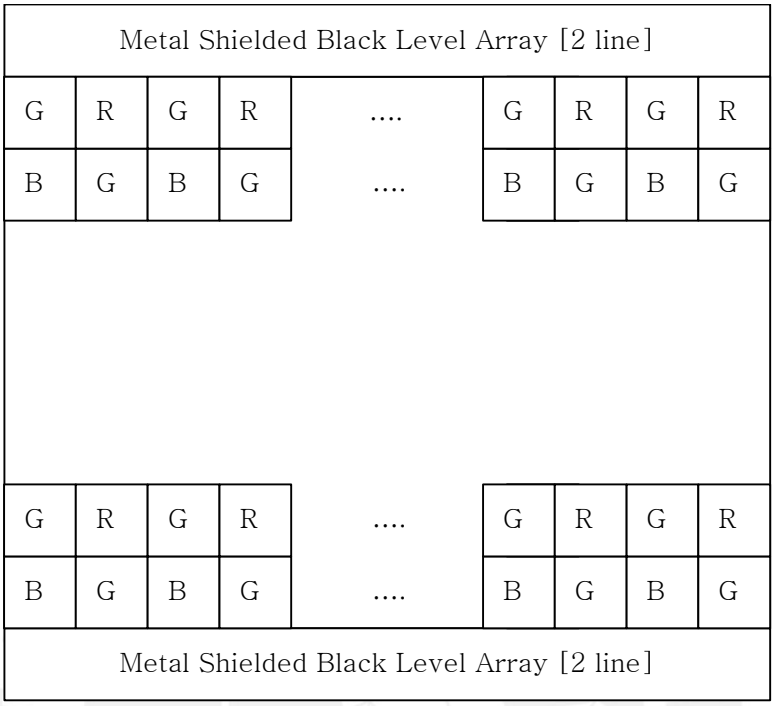
- Dynamic Range : 52 dB
- SNR_{MAX} : 42 dB
- Sensitivity : 3000 mV / lux·sec (Green Pixel)

Block Diagram



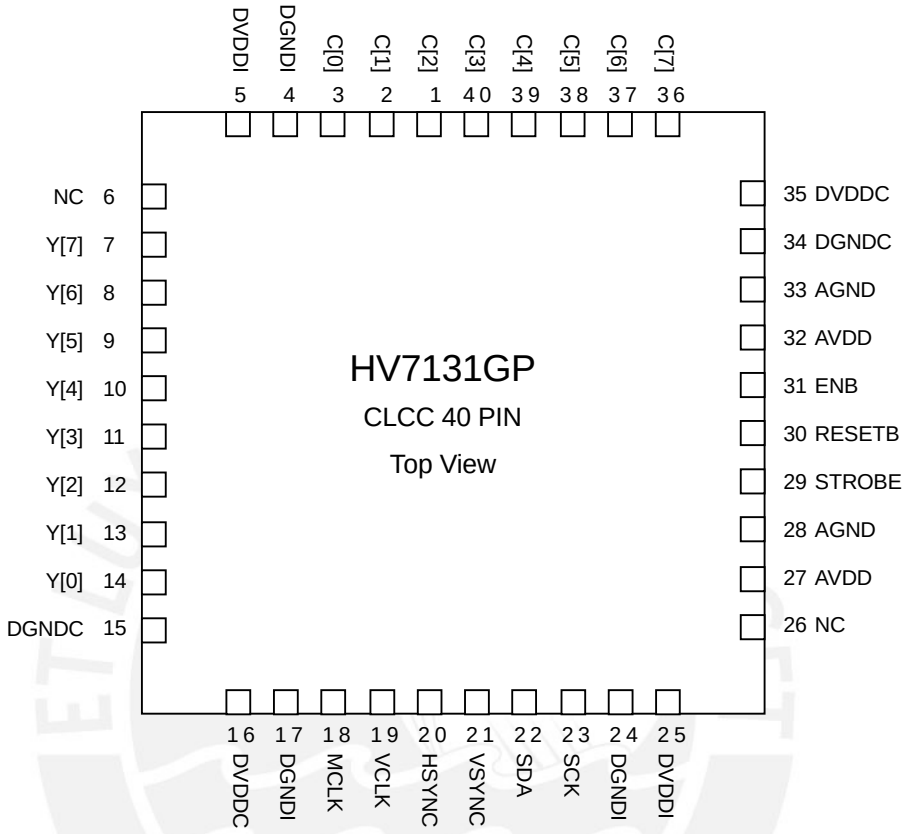
1. PGA : Programmable Gain Amplifier
2. Color Correction and Color Space Conversion are merged into one matrix operation for hardware simplification

Pixel Array Structure



Note: If black level data output is enabled(SCTRC[1] set to high) with Bayer mode set(SCTRA[1:0] == 2'b00), data output in the areas of Metal Shielded Black Level Array can be monitored during 4 line period of HSYNC right after VSYNC goes from high state to low state.

Pin Diagram



* To the matter concerning package, Wafer business companies are unrelated contents.

Pin Description

The input mode of HSYNC/VSYNC/Y[7:0]/C[7:0] is used to test internal image processing function in mass production so that it should be not assumed about slave mode operation. The device does not support slave mode operation. When 8bit output mode is used, we recommend that C[7:0] be set up as pull-up or pull-down according to I2C regulation. Although there is no pull-up or pull-down, it is no influence on function operation and leakage current does not become a problem after stabilization of chip. In case of application with C[7:0] without pull-up or pull-down, any problems were not generated.

Pin	Type	Symbol	Description
1-3	B	C[2:0]	Video Chrominance Data[2:0]
4	G	DGNDI	Digital Ground for I/O Buffer
5	P	DVDDI	Digital Power for I/O Buffer
6	N	NC	No Connection
7-14	O	Y[7:0]	Video Luminance Data[7:0]
15	G	DGNDC	Ground for Internal Digital Block
16	P	DVDDC	Power for Internal Digital Block
17	G	DGNDI	Digital Ground for I/O Buffer
18	I	MCLK	Master Input Clock
19	O	VCLK	Video Output Clock
20	O	HSYNC	Video Horizontal Line Synchronization signal. Image data is valid, when HSYNC is high.
21	O	VSYNC	Video Frame Synchronization signal. VSYNC is active at start of image data frame.
22	B	SDA	I2C Standard data I/O port
23	I	SCK	I2C Clock Input
24	G	DGNDI	Digital Ground for I/O Buffer
25	P	DVDDI	Digital Power for I/O Buffer
26	N	NC	No Connection
27	P	AVDD	Power for Analog Block
28	G	AGND	Ground for Analog Block
29	O	STROBE	Strobe Signal Output
30	I	RESETB	Sensor Reset, Low Active
31	I	ENB	Sensor sleep mode is controlled externally by this pin when sleep mode register bit SCTRB[4] is low. ENB low : sleep mode, ENB high : normal mode
32	P	AVDD	Power for Analog Block
33	G	AGND	Ground for Analog Block
34	G	DGNDC	Ground for Internal Digital Block
35	P	DVDDC	Power for Internal Digital Block
36-40	B	C[7:3]	Video Chrominance Data[7:3]

* To the matter concerning package, Wafer business companies are unrelated contents.

Note) B: bi-direction pin, P: power pin, G: ground pin, O: output pin, I: Input pin

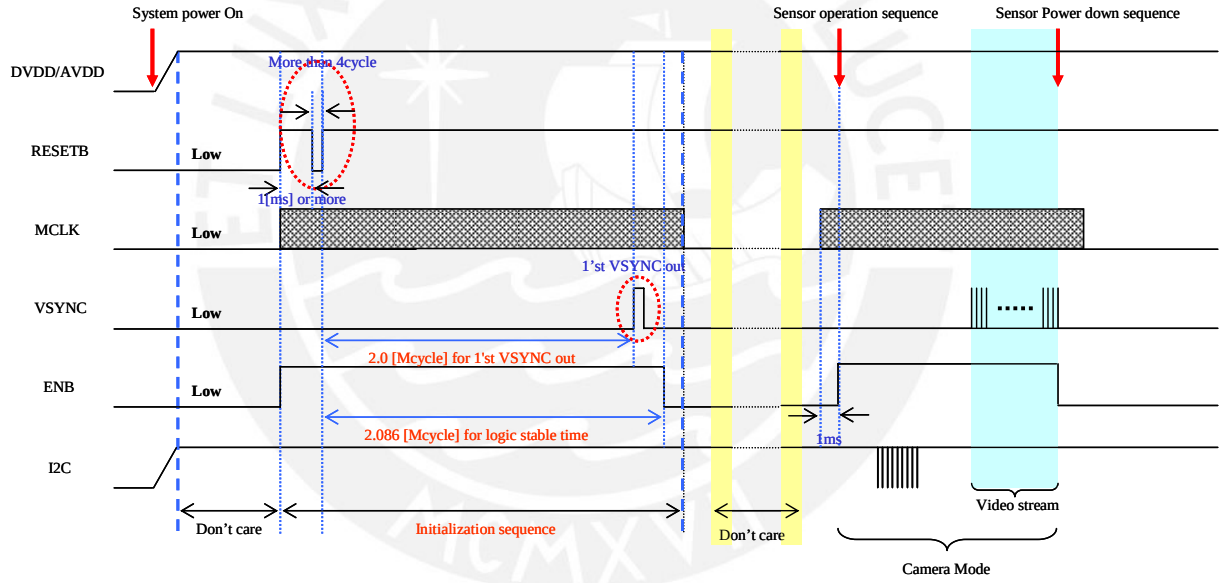
Functional Description

Pixel Architecture

Pixel architecture is a 4 transistor NMOS pixel design. The additional use of a dedicated transfer transistor in the architecture reduces most of reset level noise so that fixed pattern noise is not visible. Furthermore, micro-lens is placed upon each pixel in order to increase fill factor so that high pixel sensitivity is achieved.

ENB Setting guide information for normal stand-by mode

It is necessary that this kind of initialization sequence for the normal stand-by mode of HV7131GP after system power on



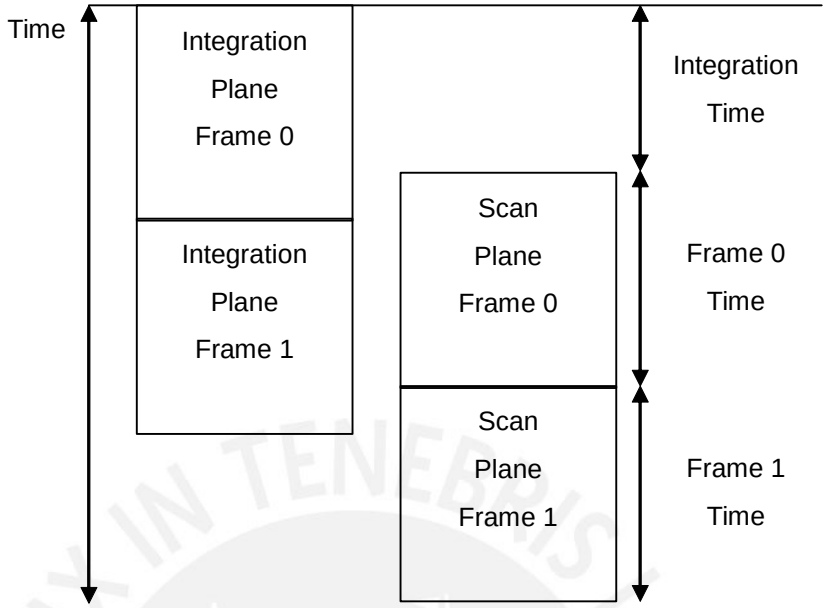
ex) If MCLK = 25[Mhz]

=> 2.086[Mcycle] / 25[MHz] = 83.44 ms

The time period of ENB high value have to keep for 83.44[ms] or more

Sensor Imaging Operation

Imaging operation is implemented by the offset mechanism of integration domain and scan domain(rolling shutter scheme). First integration plane is initiated, and after the programmed integration time is elapsed, scan plane is initiated, then image data start being produced.



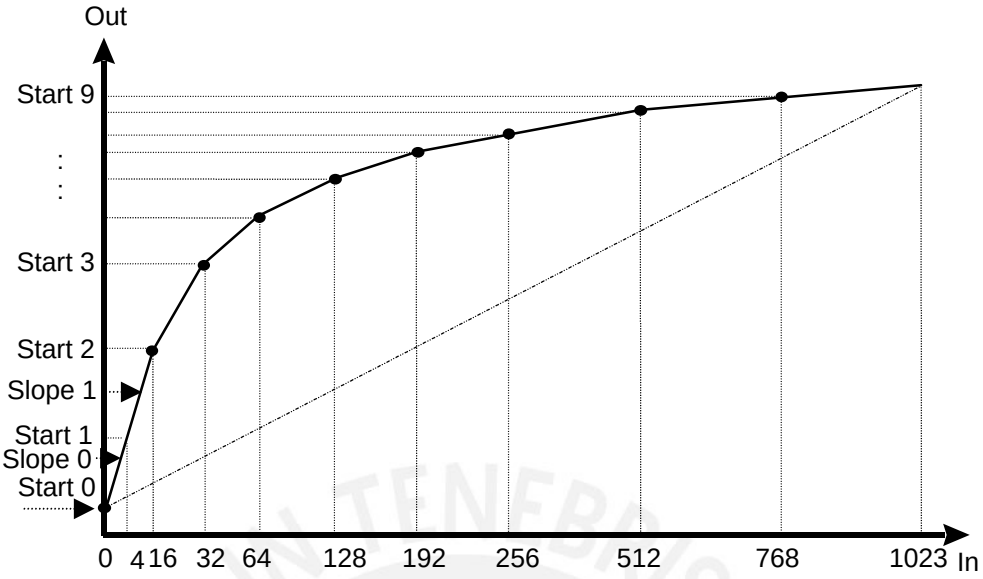
10bit on-chip ADC

On-chip ADC converts analog pixel voltage to 10bit digital data.

Gamma Correction

Piecewise linear gamma approximation method is implemented. Ten piece linear segments are supported and user-programmable.

Gamma Slope Registers are programmed as the integer value of real slope value that is multiplied by 64.



Gamma Transfer Function

Color Interpolation

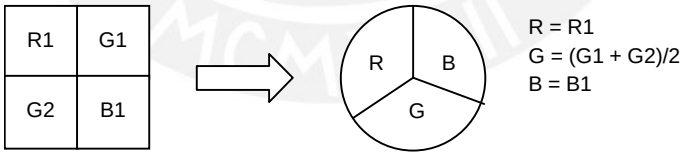
Three methods are supported to interpolate missing R, G, or B for mosaic image data from pixel array as follows.

a) 3x3 linear color interpolation

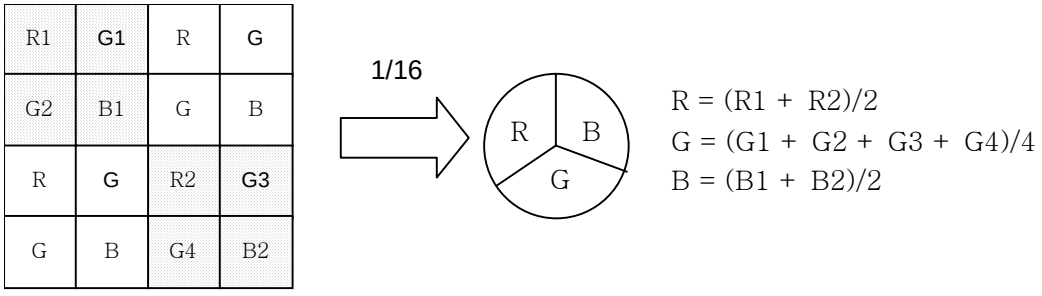
Interpolation is done by moving 3x3 interpolation window by one pixel horizontally and vertically

b) 1/4 subsampling color interpolation

Interpolation is done by moving 2x2 interpolation window by two pixels each time horizontally and vertically. The equation for color interpolation in each 2x2 window is simple as follows.



c) 1/16 subsampling color interpolation



Color Correction & Color Space Conversion

Both of Color Correction and Color Space conversion are implemented by 3x3 matrix operation, so that two stages may be merged into one matrix stage.

Color correction matrix may be resolved by measuring sensor's color spread characteristics for primary color source and calculating the inverse matrix of color spread matrix. For color space conversion matrix, the equation from CCIR-601 standard is normally used. Therefore, the intended single matrix for color correction and color space conversion may be resolved as below.

*Intended single matrix = Color Space Conversion Matrix * Color Correction Matrix*

Intended single matrix coefficients are programmable from –127/64 to 127/64. Programming register value for intended single matrix coefficients should be resolved by the following equations.

For positive values, CMAxx = Integer (Real Coefficient Value x 64);

For negative values, CMAxx = Two Complement(Integer (Real Coefficient Value x 64));

Real Coefficient Value values from –127/64 to 127/64 can be programmed.

CCIR-601 YCbCr color space conversion equation

< Conversion Equation >
Y = (77R + 150G + 29B)/256 Range: 16 ~ 235
Cb = (-44R –87G + 131B)/256 + 128 Range: 16 ~ 240
Cr = (131R – 110G – 21B)/256 + 128 Range: 16 ~ 240

< Reverse Conversion >
R = Y + 1.371(Cr – 128)
G = Y – 0.698(Cr – 128) – 0.336(Cb – 128)
B = Y + 1.732(Cb – 128)

In the above equations, R, G, and B are gamma-corrected values.

Digital Gain Control

Y, Cb, and Cr digital channels are scaled by this block that receives scaling values from Auto Exposure and Auto White Balance blocks. Scaling resolution is 1/128 and value range is 1.9 ~ 0.1.

Output Formatting

The output formats such as Bayer Raw Data, RGB 4:4:4, YCbCr 4:4:4, and YCbCr 4:2:2 are supported. Possible output bus widths are 8 bits and 16bits, and the sequence of Cb and Cr are programmable.

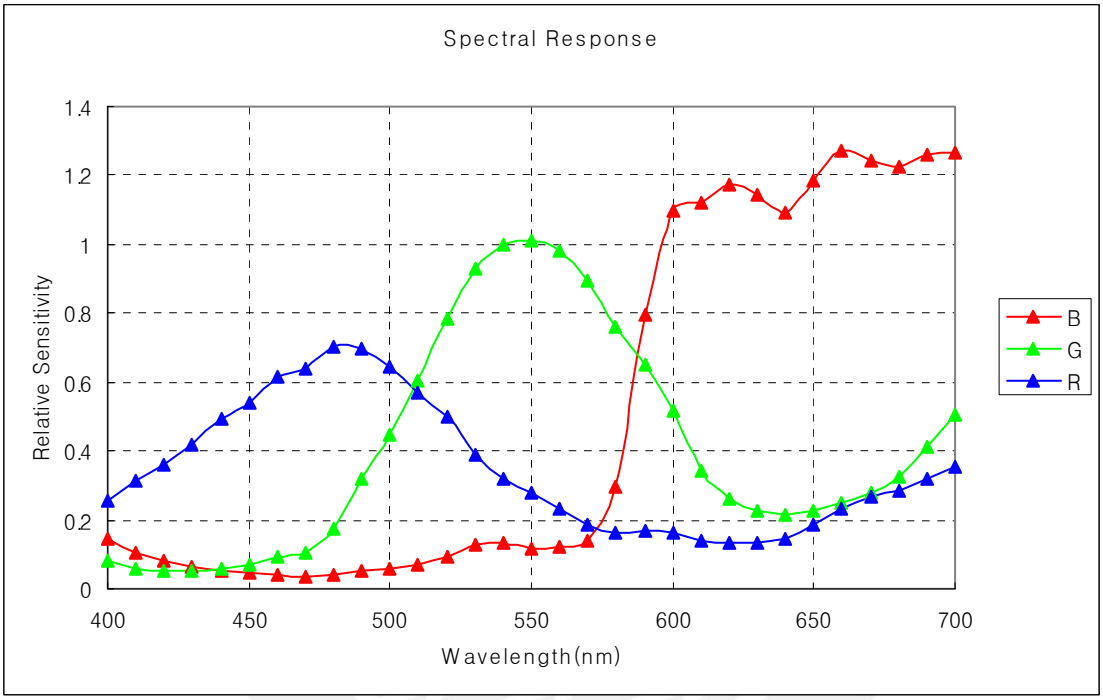
Auto Exposure Control

Y mean value is continuously calculated every frame, and the integration time value is increased or decreased according to difference between target Y mean value and current frame Y mean value.

Auto White Balance

Cb/Cr frame mean value is calculated every frame and according to Cb/Cr frame mean values' displacement from Cb/Cr white target point, R/B scaling values for R/B data are resolved.

Spectral Characteristics



Register Description

Register	Symbol	Address (Hex)	Default (Hex)	Description
Device ID	DEVID	00	40	Product ID, Revision No.
Sensor Control A	SCTRA	01	0b	Operation mode, X/Y flip, Image size
Sensor Control B	SCTRB	02	00	Power down, Clock division
Sensor Control C	SCTRC	03	01	Sensor Internal control Register
Row Start Address High	RSAH	08	00	Row Start Address[8]
Row Start Address Low	RSAL	09	02	Row Start Address[7:0]
Column Start Address High	CSAH	0a	00	Column Start Address[9:8]
Column Start Address Low	CSAL	0b	02	Column Start Address[7:0]
Window Height High	WIHH	0c	01	Window Height Address[8]
Window Height Low	WIHL	0d	e0	Window Height Address[7:0]

Window Width High	WIWH	0e	02	Window Width Address[9:8]
Window Width Low	WIWL	0f	80	Window Width Address[7:0]
HBLANK Time High	HBLANKH	10	00	HBLANK Time [15:8]
HBLANK Time Low	HBLANKL	11	d0	HBLANK Time [7:0]
VBLANK Time High	VBLANKH	12	00	VBLANK Time [15:8]
VBLANK Time Low	VBLANKL	13	08	VBLANK Time [7:0]
Red Color Gain	RCG	14	10	Gain for Red Pixel Output
Green Color Gain	GCG	15	10	Gain for Green Pixel Output
Blue Color Gain	BCG	16	10	Gain for Blue Pixel Output
Preamp Gain	PREAMP	17	10	Preamp Gain for Pixel Output
Preamp Gain Min	PREMIN	18	00	Preamp Gain Min Value for AE
Preamp Gain Max	PREMAX	19	3f	Preamp Gain Max Value for AE
Preamp Gain Nominal	PRENOM	1a	10	Preamp Gain Normal Value for AE
ASP Bias	ASPBIAS	1b	13	Amp Bias, Pixel Bias
Reset Clamp	RSTCLMP	1c	07	Reset Level Clamping Value
ADC Bias	ADCBIAS	20	0f	ADC Bias
Red Pixel Black Offset	OREDI	21	7f	ADC Offset Value for Light-shielded Red Pixel
Green Pixel Black Offset	OGRNI	22	7f	ADC Offset Value for Light-shielded Green Pixel
Blue Pixel Black Offset	OBLUI	23	7f	ADC Offset Value for Light-shielded Blue Pixel
Red Pixel Active Offset	OREDU	24	RO	ADC Offset Value for Active Red Pixel
Green Pixel Active Offset	OGRNU	25	RO	ADC Offset Value for Active Green Pixel
Blue Pixel Active Offset	OBLUU	26	RO	ADC Offset Value for Active Blue Pixel
Black Level Threshold	BLCTH	27	ff	Black Level Threshold Value
ISP Function Enable	ISPFEN	30	0f	Image processing functions enable
ISP Output Format	OUTFMT	31	39	Image data output format control
ISP Output Polarity	OUTINV	32	00	Output signal polarity control
Green Edge Threshold	EDGETH	33	00	Green pixel edge threshold for 3x3 color interpolation
Color Matrix Coefficient 11	CMA11	34	2e	Color matrix coefficient 11
Color Matrix Coefficient 12	CMA12	35	c5	Color matrix coefficient 12
Color Matrix Coefficient 13	CMA13	36	0c	Color matrix coefficient 13
Color Matrix Coefficient 21	CMA21	37	0d	Color matrix coefficient 21

Color Matrix Coefficient 22	CMA22	38	3c	Color matrix coefficient 22
Color Matrix Coefficient 23	CMA23	39	f7	Color matrix coefficient 23
Color Matrix Coefficient 31	CMA31	3a	f8	Color matrix coefficient 31
Color Matrix Coefficient 32	CMA32	3b	cf	Color matrix coefficient 32
Color Matrix Coefficient 33	CMA33	3c	39	Color matrix coefficient 33
Gamma Segment Point 0	GMAP0	40	00	Start point for gamma line segment 0
Gamma Segment Point 1	GMAP1	41	04	Start point for gamma line segment 1
Gamma Segment Point 2	GMAP2	42	1c	Start point for gamma line segment 2
Gamma Segment Point 3	GMAP3	43	34	Start point for gamma line segment 3
Gamma Segment Point 4	GMAP4	44	54	Start point for gamma line segment 4
Gamma Segment Point 5	GMAP5	45	78	Start point for gamma line segment 5
Gamma Segment Point 6	GMAP6	46	90	Start point for gamma line segment 6
Gamma Segment Point 7	GMAP7	47	a4	Start point for gamma line segment 7
Gamma Segment Point 8	GMAP8	48	e0	Start point for gamma line segment 8
Gamma Segment Point 9	GMAP9	49	f4	Start point for gamma line segment 9
Gamma Segment Slope 0	GMAS0	50	40	Slope value for gamma line segment 0
Gamma Segment Slope 1	GMAS1	51	80	Slope value for gamma line segment 1
Gamma Segment Slope 2	GMAS2	52	60	Slope value for gamma line segment 2
Gamma Segment Slope 3	GMAS3	53	40	Slope value for gamma line segment 3
Gamma Segment Slope 4	GMAS4	54	24	Slope value for gamma line segment 4
Gamma Segment Slope 5	GMAS5	55	18	Slope value for gamma line segment 5
Gamma Segment Slope 6	GMAS6	56	14	Slope value for gamma line segment 6
Gamma Segment Slope 7	GMAS7	57	0f	Slope value for gamma line segment 7
Gamma Segment Slope 8	GMAS8	58	05	Slope value for gamma line segment 8
Gamma Segment Slope 9	GMAS9	59	02	Slope value for gamma line segment 9
AE Mode 1	AEM1	60	39	Auto exposure mode selection 1
AE Mode 2	AEM2	61	ba	Auto exposure mode selection 2
Integration Time High	INTH	63	07	Integration Time [23:16]
Integration Time Middle	INTM	64	a1	Integration Time [15:8]
Integration Time Low	INTL	65	20	Integration Time [7:0]
AE Target	AETGT	66	70	Frame Luminance Target Value
AE Lock & Fine Tune Boundary	AELBND	67	a2	Y frame mean value displacement boundary from AE target where AE goes into Lock state. Fine tuning boundary is also specified.

AE Unlock Boundary	AEUNLCK	68	2a	Y frame mean value displacement from AE target where AE update speed transits from 2x integration unit speed to 1x integration unit speed
AE Integration Step High	AEINCH	6a	1	Integration Increment Step Unit [17:16]
AE Integration Step Middle	AEINCM	6b	e8	Integration Increment Step Unit [15:8]
AE Integration Step Low	AEINCL	6c	48	Integration Increment Step Unit [7:0]
AE Integration Limit High	AELMH	6d	17	Integration Time Limit [23:16]
AE Integration Limit Middle	AELMM	6e	d7	Integration Time Limit [15:8]
AE Integration Limit Low	AELML	6f	84	Integration Time Limit [7:0]]
AWB Mode 1	AWBM1	70	41	AWB mode selection 1
AWB Mode 2	AWBM2	71	2	AWB mode selection 2
Cb Target	CBTGT	73	80	Cb Plane Target Frame Mean Value. Normal white point is 80h.
Cr Target	CRTGT	74	80	Cr Plane Target Frame Mean Value. Normal white point is 80h.
AWB Lock Boundary	AWBLB	75	2	Cb/Cr Frame Mean Displacement from Cb Target and Cr Target where AWB goes into LOCK state
AWB Unlock Boundary	AWBULB	76	06	Displacement from ideal white pixel where AWB release from LOCK state
AWB White Pixel Boundary	AWBWPB	77	30	Displacement from ideal white pixel where AWB recognizes a pixel as a white pixel affected by light source
Y Digital Gain	YGAIN	78	40	Y digital gain for Auto Exposure Control
Cb Digital Gain	CBGAIN	79	40	Cb digital gain for Auto White Balance control
Cr Digital Gain	CRGAIN	7a	40	Cr digital gain for Auto White Balance control
AE Status	AEST	7b	RO	AE operation status
AWB Status	AWBST	7c	RO	AWB operation status
Y Frame Mean	YFMEAN	7d	RO	Y Frame Mean Value

Cb Frame Mean	CBFMEAN	7e	RO	Cb Frame Mean Value
Cr Frame Mean	CRFMEAN	7f	RO	Cr Frame Mean Value
Minimum Anti-Banding Gain	BNDGMIN	80	08	Minimum gain value with Anti-Banding enabled
Maximum Anti-Banding Gain	BNDGMAX	81	18	Maximum gain value with Anti-Banding enabled
Integration-Scan Plane Offset High	ISOFSH	82	RO	Integration-Scan Plane Offset[23:16]
Integration-Scan Plane Offset Middle	ISOFSM	83	RO	Integration-Scan Plane Offset[16:8]
Integration-Scan Plane Offset Low	ISOFSL	84	RO	Integration-Scan Plane Offset[7:0]
AWB Luminance High Boundary	AWBLUHI	8a	C8	During CbCr frame mean value calculation, AWB discards pixel of which luminance is larger than this register value.
AWB Luminance Low Boundary	AWBLULO	8b	0a	During CbCr frame mean value calculation, AWB discards pixel of which luminance is smaller than this register value.
AWB Valid Number	AWBNO	8c	02	AWB update when the number of valid color pixel is larger than (this minimum value x 64)
Dark Bad Pixel Concealment Mode	DPCMODE	90	0	Dark Bad Pixel Concealment Mode selection
Dark Bad Integration Time High	DPCINTH	91	13	Integration Time Value High Byte where filtering operation gets active when dark bad pixel filtering mode is enabled.
Dark Bad Integration Time Middle	DPCINTM	92	12	Integration Time Value Middle Byte where filtering operation gets active when dark bad pixel filtering mode is enabled.
Dark Bad Integration Time Low	DPCINTL	93	D0	Integration Time Value Low Byte where filtering operation gets active when dark bad pixel filtering mode is enabled.
Dark Bad G Threshold	DPCGTH	94	0c	Neighbor-differential threshold value that specify G dark bad pixel
Dark Bad R/B Threshold	DPCCTH	95	0c	Neighbor-differential threshold value that specify R/B dark bad pixel

Device ID [DEVID : 00h : 40h]

7	6	5	4	3	2	1	0
Product ID				Revision Number			
0	1	0	0	0	0	0	0

High nibble represents Sensor Array Resolution, Low Nibble represents Revision Number.

Sensor Control A [SCTRA : 01h : 0bh]

7	6	5	4	3	2	1	0
Operation Mode				X-Flip	Y-Flip	Video Mode	
0	0	0	0	1	0	1	1

Category	Operation Mode	Note
TestC	1111	At CDS operation, reset and image bit-lines are all written to high. This mode is just for monitoring purpose.
	1110	At CDS operation, image bit-line is written to high. In this mode, all Bayer data output are 8'h00.
	1101	At CDS operation, reset bit-line is written to high. In this mode, all Bayer data output are 8'hff.
	1100	Reserved
TestA	10x1	ADC overflow test with CDS output disconnected. In this mode, all Bayer data output are 8'hff.
	10x0	ADC underflow test with CDS output disconnected. In this mode, all Bayer data output are 8'h00.
TestI	011x	Image processing function test
TestB	0101	I2C state machine test
	0100	Sensor operation state machine test
Normal	0000	Normal imaging operation

X-Flip	Image is horizontally flipped
Y-Flip	Image is vertically flipped
Video Mode	11 3x3 color interpolation 10 1/4 subsampling mode 01 1/16 subsampling mode 00 Bayer output mode

Sensor Control B [SCTRB : 02h : 00h]

7	6	5	4	3	2	1	0
AE/AWB Block Sleep	Datapath Block Sleep	Analog Block Sleep	Sleep Mode	Strobe Enable	Clock Division		
0	0	0	0	0	0	0	0

< Clock Acronym Definition >

MCF : Master Clock Frequency	DCF : Divided Clock Frequency
SCF : Sensor Clock Frequency	ICF : Image Processing Clock Frequency
VCF : Video Clock Frequency	LCF : Line Clock Frequency

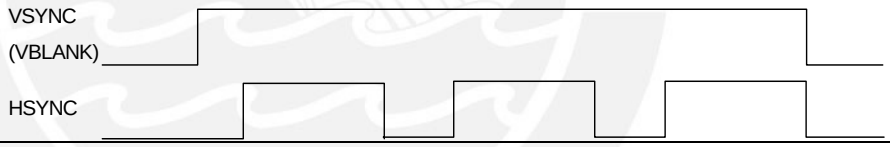
< Clock Frequency Relation >

MCF : MCF	DCF : MCF/Clock Division	
SCF : DCF/2	ICF	SCF for 3x3 interpolation, SCF/2 for 1/4 subsampling mode SCF/4 for 1/16 subsampling mode
VCF : ICF for 16bit output, ICF*2 for 8bit output	LCF : 1/(HBLANK Period + HSYNC Period)	

AE/AWB Block Sleep	AE/AWB block goes into sleep mode with this bit set to high.
Datapath Block Sleep	Image processing datapath block goes into sleep mode with this bit set to high.
Analog Block Sleep	all internal analog block goes into sleep mode with this bit set to high. With All Digital Block Sleep active, sensor goes into power down mode.
Sleep Mode	all internal digital and analog block goes into sleep with this bit set to high.
Strobe Enable	When strobe signal is enabled by this bit, STROBE pin will indicates when strobe light should be splashed in the dark environment to get adequate lighted image.
Clock Division	divides input master clock(IMC) for internal use. Internal divided clock frequency(DCF) is defined as master clock frequency(MCF) divided by specified clock divisor. Internal divided clock frequency(DCF) is as follows. 000 : MCF, 001 : MCF/2, 010 : MCF/4, 011 : MCF/8 100 : MCF/16, 101 : MCF/32, 110 : MCF/64, 111 : MCF/128

Sensor Control C [SCTRC : 03h : 01h]

7	6	5	4	3	2	1	0
Black Level Average Output	Y[7:0] Pad Output with HSYNC high	C[7:0] Pad Output with 8bit mode	HSYNC in VBLANK	reserved	Unified Gain	Black Level Data Enable	Black Level Compens-ation
0	0	0	0	0	0	0	1

Black Level Average Output	This bit enable R/G/B Active Offset registers[24h-26h] to represent black level average value, instead of updated active offset values
Y[7:0] Pad Output with HSYNC high	With this bit set to high, Y[7:0] pads go into tri-state when HSYNC is inactive.
C[7:0] Pad Output with 8bit mode	With this bit set to high, C[7:0] pads go into zero driving state with 8bit output mode enabled. Otherwise, these pads go into tri-state.
HSYNC in VBLANK	VBLANK is equivalent to VSYNC, and HSYNC is the inversion of HBLANK, and this bit control whether HSYNC is active or not when VBLANK unit is LCF. 
Unified Gain	G gain is used for R, G, and B analog gain
Black Level Data Enable	HSYNC is generated for light-shielded pixels in 4 lines.
Black Level Compensation	Black level average values of light-shielded pixels are compensated when active image data is produced.

Row Start Address High [RSAH : 08h : 0h]

7	6	5	4	3	2	1	0
reserved							Row Start Address High
0	0	0	0	0	0	0	0

Row Start Address Low [RSAL : 09h : 02h]

7	6	5	4	3	2	1	0
Row Start Address Low							
0	0	0	0	0	0	1	0

Row Start Address register defines the row start address of image read out operation.

Column Start Address High [CSAH : 0ah : 0h]

7	6	5	4	3	2	1	0
reserved						Column Start Address High	
0	0	0	0	0	0	0	0

Column Start Address Low [CSAL : 0bh : 02h]

7	6	5	4	3	2	1	0
Column Start Address Low							
0	0	0	0	0	0	1	0

Column Start Address register defines the column start address of image read out operation.

Window Height High [WIHH : 0ch : 1h]

7	6	5	4	3	2	1	0
reserved							Window Height High
0	0	0	0	0	0	0	1

Window Height Low [WIHL : 0dh : e0h]

7	6	5	4	3	2	1	0
Window Height Low							
1	1	1	0	0	0	0	0

Window Height register defines the height of image to be read out.

Window Width High [WIWH : 0eh : 2h]

7	6	5	4	3	2	1	0
reserved						Window Width High	
0	0	0	0	0	0	1	0

Window Width Low [WIWL : 0fh : 80h]

7	6	5	4	3	2	1	0
Window Width Low							
1	0	0	0	0	0	0	0

Window Width Address register defines the width of image to be read out.

HBLANK Time High [HBLANKH : 10h : 00h]

7	6	5	4	3	2	1	0
HBLANK Time High							
0	0	0	0	0	0	0	0

HBLANK Time Low [HBLANKL : 11h : d0h]

7	6	5	4	3	2	1	0
HBLANK Time Low							
1	1	0	1	0	0	0	0

HBLANK Time register defines data blank time between current line and next line by using Sensor Clock Period unit (1/SCF), and should be larger than 208(d0h).

VBLANK Time High[VBLANK : 12h : 00h]

7	6	5	4	3	2	1	0
VBLANK Time High							
0	0	0	0	0	0	0	0

VBLANK Time Low[VBLANK : 13h : 08h]

7	6	5	4	3	2	1	0
VBLANK Time Low							
0	0	0	0	1	0	0	0

VBLANK Time register defines active high duration of VSYNC output. Active high VSYNC indicates frame boundary between continuous frames. For VSYNC-HSYNC timing relation in the frame transition, please refer to Frame Timing section.

Each sensor has a little different photo-diode characteristics so that the sensor provides internal adjustment registers that calibrate internal sensing circuit in order to get optimal performance. Sensor characteristics adjustment registers are as below.

R Color Gain [RCG : 14h : 10h]

7	6	5	4	3	2	1	0
reserved		R Color Gain					
0	0	0	1	0	0	0	0

G Color Gain [GCG : 15h : 10h]

7	6	5	4	3	2	1	0
reserved		G Color Gain					
0	0	0	1	0	0	0	0

B Color Gain [BCG : 16h : 10h]

7	6	5	4	3	2	1	0
reserved		B Color Gain					
0	0	0	1	0	0	0	0

There are three color gain registers for R, G, B pixels, respectively. Programmable range is from 0.5X ~ 2.5X. Effective Gain = 0.5 + B<5:0>/32. These registers may be used for white balance and color effect with independent R,G,B color control. Default gain is 1X.

Preamp Gain [PREAMP : 17h : 10h]

7	6	5	4	3	2	1	0
Preamp Gain							
0	0	0	1	0	0	0	0

Preamp Gain is common gain for R, G, B channel and used for auto exposure control. Programmable range is from 0.5X ~ 16.5X. Default gain is 1.5X.
Gain = 0.5 + B<7:0>/16

Preamp Gain Min [PREMIN : 18h : 00h]

7	6	5	4	3	2	1	0
Preamp Gain Min							
0	0	0	0	0	0	0	0

Preamp Gain Min is minimum value of preamp gain when sensor adjusts pre-amplifier gain for auto exposure control. Programmable range is same as preamp gain. Recommended value is 0.5X.

Preamp Gain Max [PREMAX : 19h : 3fh]

7	6	5	4	3	2	1	0
Preamp Gain Max							
0	0	1	1	1	1	1	1

Preamp Gain Max is maximum value of preamp gain when sensor adjusts preamp gain for auto

exposure control. Programmable range is same as preamp gain. Recommended value is 16.5X.

Preamp Gain Normal [PRENOR : 1ah : 10h]

7	6	5	4	3	2	1	0
Preamp Gain Normal							
0	0	0	1	0	0	0	0

Preamp Gain Normal is reference value of preamp gain when sensor adjusts preamp gain for auto exposure control. First, sensor controls integration time before adjusting preamp gain for auto exposure control. After integration time is changed to the minimum or maximum value, sensor adjusts preamp gain from this register value. Refer to figure of AE mode1 register(60H).
Programmable range is same as preamp gain. Recommended value is 1.5X.

ASP Bias [ASPBIAS : 1bh : 13h]

7	6	5	4	3	2	1	0
reserved	Pixel Bias			Amp Bias			
0	0	0	1	0	0	1	1

Pixel Bias	controls the amount of current in internal pixel bias circuit to amplify pixel output effectively. The larger register value increases the amount of current.
Amplifier Bias	controls the amount of current in internal amplifier bias circuit to amplify pixel output effectively. The larger register value increases the amount of current.

Reset Level Clamp [RSTCLMP : 1ch : 07h]

7	6	5	4	3	2	1	0
Reserved				Reset Level Clamp			
0	0	0	0	0	1	1	1

Because extremely bright image like sun affects reset data voltage of pixel to lower, bright image is captured as black image in image sensor regardless of correlated double sampling. To solve this extraordinary phenomenon, we adopt the method to clamp reset data voltage. Reset Level Clamp controls the reset data voltage to prevent inversion of extremely bright image. The larger register value clamps the reset data level at highest voltage level. Default value is 7 to clamp the reset data level at appropriate voltage level.

ADC Bias [ADCBIAS : 20h : 0fh]

7	6	5	4	3	2	1	0
Reserved				ADC Bias			
0	0	0	0	1	1	1	1

ADC Bias controls the amount of current in ADC bias circuit to operate ADC effectively. The larger register value increases the amount of current.

Red Pixel Black Offset [OREDI : 21h : 7fh]

7	6	5	4	3	2	1	0
Red Pixel Black Offset							
0	1	1	1	1	1	1	1

Green Pixel Black Offset [OGRNI : 22h : 7fh]

7	6	5	4	3	2	1	0
Green Pixel Black Offset							
0	1	1	1	1	1	1	1

Blue Pixel Black Offset [OBLUI : 23h : 7fh]

7	6	5	4	3	2	1	0
Blue Pixel Black Offset							
0	1	1	1	1	1	1	1

These registers control the offset voltage of ADC that changes the black level value for light-shielded pixels, red, green and blue pixel respectively. Register bit functions are composed as follows.

Pixel Black Offset[7]	The bit specifies whether to subtract or add offset voltage in ADC input for light-shielded pixels.
Pixel Black Offset[6:0]	This value specifies the amount of offset voltage for light-shielded pixels.

Red Pixel Active Offset [OREDU : 24h : RO]

7	6	5	4	3	2	1	0
Red Pixel Active Offset							
RO	RO	RO	RO	RO	RO	RO	RO

Green Pixel Active Offset [OGRNU : 25h : RO]

7	6	5	4	3	2	1	0

Green Pixel Active Offset							
RO	RO	RO	RO	RO	RO	RO	RO

Blue Pixel Active Offset [OBLUU : 26h : RO]

7	6	5	4	3	2	1	0
Blue Pixel Active Offset							
RO	RO	RO	RO	RO	RO	RO	RO

These registers control the offset voltage of ADC that changes the black level value for active pixels, red, green and blue pixel respectively. The registers are internally updated by black level compensation logic, and are read-only registers. Register bit functions are composed as follows.

Pixel Active Offset[7]	The bit specifies whether to subtract or add offset voltage in ADC input for active pixels.
Pixel Active Offset[6:0]	This value specifies the amount of offset voltage for active pixels.

Black Level Threshold [BLCTH : 27h : ffh]

7	6	5	4	3	2	1	0
Black Level Threshold							
1	1	1	1	1	1	1	1

The register specifies the maximum value which determines whether light-shielded pixel output is valid. When light-shielded pixel output exceeds this limit, the pixel is not accounted for black level calculation.

ISP Function Enable [ISPFEN : 30h : 0fh]

7	6	5	4	3	2	1	0
Reserved				Matrix Operation	Color Interpolation	Gamma Correction	reserved
0	0	0	0	1	1	1	1

Matrix Conversion	In HV7131GP, two matrix operations of color correction & color space conversion are merged into one matrix operation. With this bit set to high, the matrix operation is enabled, and otherwise R/G/B data is output through output formatter.
Color Interpolation	With SCTRA[1:0] set to 3x3 color interpolation, this bit control the final channel between color interpolated R/G/B and Bayer data. With this bit set

	to low, R/G/B channels for one pixel are fed with the same one Bayer value so that image similar to black & white is produced.
Gamma Correction	With this bit set to high, 10 segments piecewise approximate gamma is enabled.

Output Format [OUTFMT : 31h : 39h]

7	6	5	4	3	2	1	0
Gamma-corrected Bayer	Bayer 8bit output	Cb First	Y First	8 Bit Output	reserved	YCbCr 4:4:4	YCbCr 4:2:2
0	0	1	1	1	0	0	1

Gamma-corrected Bayer	Bayer data that are gamma corrected is output when Bayer mode is set in SCTRA register.
Bayer 8bit output	Bayer data is output with 8bit mode. two LSB of 10 bit Bayer data is stripped out.
Cb First	Cb pixel in front of Cr pixel in 16bit or 8bit video data output modes
Y First	Y pixel in front of Cb and Cr pixels in 8bit video output mode. This option is meaningful only with 8bit output mode.
8 Bit Output	Image Data is produced only in Y[7:0]. C[7:0] should be discarded
YCbCr 4:4:4	YCbCr 24bit data for a pixel is produced with 16bit output mode. With color space conversion disabled, RGB 24bit data for a pixel is produced in this mode. This mode is meaningful only with 16bit output mode.
YCbCr 4:2:2	YCbCr data for a pixel is produced with 8/16 output mode

Output Inversion[OUTINV : 32h : 0h]

7	6	5	4	3	2	1	0
reserved				Clocked HSYNC	VSYNC inversion	HSYNC inversion	VCLK inversion
0	0	0	0	0	0	0	0

Clocked HSYNC	In HSYNC, VCLK is embedded, that is, HSYNC is toggling at VCLK rate during normal HSYNC time
VSYNC inversion	VSYNC output polarity is inverted
HSYNC inversion	HSYNC output polarity is inverted

VCLK inversion	VCLK output polarity is inverted

Green Edge Threshold[EDGETH : 33h : 00h]

7	6	5	4	3	2	1	0
Green Edge Threshold							
0	0	0	0	0	0	0	0

In 3x3 color interpolation mode, missing G pixel is interpolated with edge detection considering neighbor G pixels, and this register controls edge threshold to select edge direction. The smaller value means that the more patterns are recognized as edge, and image may get sharper, but not always.

Color Matrix Coefficients

Both of Color Correction and Color Space conversion are implemented by 3x3 matrix operation, so that two stages may be merged into one matrix stage.

Color correction matrix may be resolved by measuring sensor's color spread characteristics for primary color source and calculating the inverse matrix of color spread matrix. For color space conversion matrix, the equation from CCIR-601 standard is normally used. Therefore, the intended single matrix for color correction and color space conversion may be resolved as below.

*Intended single matrix = Color Space Conversion Matrix * Color Correction Matrix*

Intended single matrix coefficients are programmable from –127/64 to 127/64. Programming register value for intended single matrix coefficients should be resolved by the following equations.

For positive values, CMAxx = Integer(RealCoefficientValue x 64);

For negative values, CMAxx = TwoComplement(Integer(RealCoefficientValue x 64));

RealCoefficientValue values from –127/64 to 127/64 can be programmed.

CCIR-601 YCbCr color space conversion equation

< Conversion Equation >
Y = (77R + 150G + 29B)/256 Range: 16 ~ 235
Cb = (-44R –87G + 131B)/256 + 128 Range: 16 ~ 240
Cr = (131R – 110G – 21B)/256 + 128 Range: 16 ~ 240

< Reverse Conversion >
R = Y + 1.371(Cr – 128)
G = Y – 0.698(Cr – 128) – 0.336(Cb – 128)
B = Y + 1.732(Cb – 128)

In the above equations, R, G, and B are gamma-corrected values

Color Matrix Coefficient 11 [CMA11 : 34h : 2eh]

7	6	5	4	3	2	1	0

Color Matrix Coefficient 11							
0	0	1	0	1	1	1	0

Color Matrix Coefficient 12 [CMA12 : 35h : c5h]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 12							
1	1	0	0	0	1	0	1

Color Matrix Coefficient 13 [CMA13 : 36h : 0ch]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 13							
0	0	0	0	1	1	0	0

Color Matrix Coefficient 21 [CMA21 : 37h : 0dh]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 21							
0	0	0	0	1	1	0	1

Color Matrix Coefficient 22 [CMA22 : 38h : 3ch]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 22							
0	0	1	1	1	1	0	0

Color Matrix Coefficient 23 [CMA23 : 39h : f7h]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 23							
1	1	1	1	0	1	1	1

Color Matrix Coefficient 31 [CMA31 : 3ah : f8h]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 31							
1	1	1	1	1	0	0	0

Color Matrix Coefficient 32 [CMA32 : 3bh : cfh]

7	6	5	4	3	2	1	0

Color Matrix Coefficient 32							
1	1	0	0	1	1	1	1

Color Matrix Coefficient 33 [CMA33 : 3ch : 39h]

7	6	5	4	3	2	1	0
Color Matrix Coefficient 33							
0	0	1	1	1	0	0	1

Gamma Segment Start Points

Gamma Segment Start Points specify the start points of nine line segments for piecewise gamma approximation. Current default gamma curve is very selected for optimum gray gradation.

Gamma Point 0 [GAMP0 : 40h : 00h]

7	6	5	4	3	2	1	0
Gamma Point 0							
0	0	0	0	0	0	0	0

Gamma Point 1 [GMAP1 : 41h : 04h]

7	6	5	4	3	2	1	0
Gamma Point 1							
0	0	0	0	0	1	0	0

Gamma Point 2 [GMAP2 : 42h : 1ch]

7	6	5	4	3	2	1	0
Gamma Point 2							
0	0	0	1	1	1	0	0

Gamma Point 3 [GMAP3 : 43h : 34h]

7	6	5	4	3	2	1	0
Gamma Point 3							
0	0	1	1	0	1	0	0

Gamma Point 4 [GMAP4 : 44h : 54h]

7	6	5	4	3	2	1	0
Gamma Point 4							

0	1	0	1	0	1	0	0

Gamma Point 5 [GMAP5 : 45h : 78h]

7	6	5	4	3	2	1	0
Gamma Point 5							
0	1	1	1	1	0	0	0

Gamma Point 6 [GMAP6 : 46h : 90h]

7	6	5	4	3	2	1	0
Gamma Point 6							
1	0	0	1	0	0	0	0

Gamma Point 7 [GMAP7 : 47h : a4h]

7	6	5	4	3	2	1	0
Gamma Point 7							
1	0-	1	0	0	1	0	0

Gamma Point 8 [GMAP8 : 48h : e0h]

7	6	5	4	3	2	1	0
Gamma Point 8							
1	1	1	0	0	0	0	0

Gamma Point 9 [GMAP9 : 49h : f4h]

7	6	5	4	3	2	1	0
Gamma Point 9							
1	1	1	1	0	1	0	0

Gamma Slope Values

Gamma Slope Registers are programmed as the integer value of real slope value that is multiplied by 64.

Gamma Slope 0 [GMAS0 : 50h : 40h]

7	6	5	4	3	2	1	0
Gamma Slope 0							
0	1	0	0	0	0	0	0

Gamma Slope 1 [GMAS1 : 51h : 80h]

7	6	5	4	3	2	1	0
Gamma Slope 1							
1	0	0	0	0	0	0	0

Gamma Slope 2 [GMAS2 : 52h : 60h]

7	6	5	4	3	2	1	0
Gamma Slope 1							
0	1	1	0	0	0	0	0

Gamma Slope 3 [GMAS3 : 53h : 40h]

7	6	5	4	3	2	1	0
Gamma Slope 3							
0	1	0	0	0	0	0	0

Gamma Slope 4 [GMAS4 : 54h : 24h]

7	6	5	4	3	2	1	0
Gamma Slope 4							
0	0	1	0	0	1	0	0

Gamma Slope 5 [GMAS5 : 55h : 18h]

7	6	5	4	3	2	1	0
Gamma Slope 5							
0	0	0	1	1	0	0	0

Gamma Slope 6 [GMAS6 : 56h : 14h]

7	6	5	4	3	2	1	0
Gamma Slope 6							
0	0	0	1	0	1	0	0

Gamma Slope 7 [GMAS7 : 57h : 0fh]

7	6	5	4	3	2	1	0
Gamma Slope 7							
0	0	0	0	1	1	1	1

Gamma Slope 8 [GMAS8 : 58h : 05h]

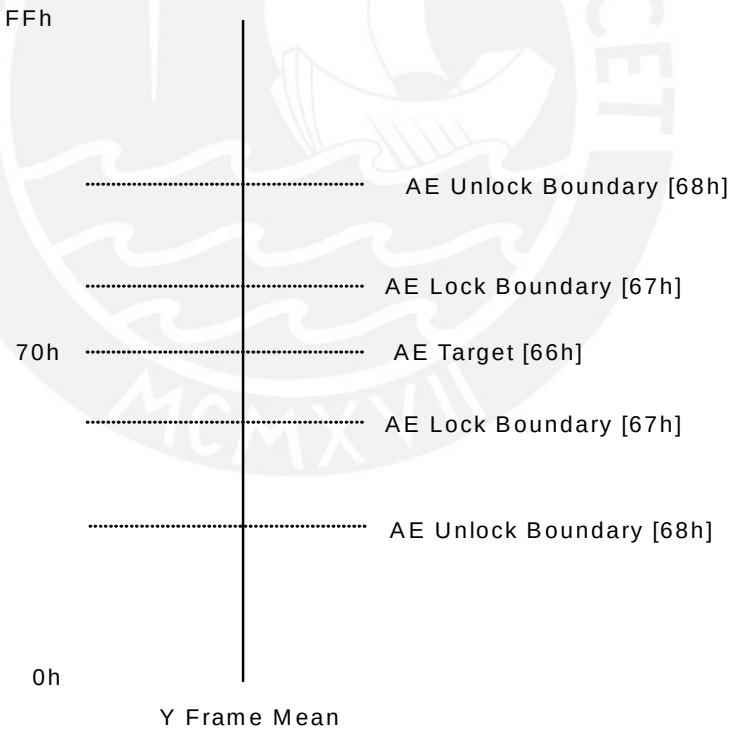
7	6	5	4	3	2	1	0
Gamma Slope 8							
0	0	0	0	0	1	0	1

Gamma Slope 9 [GMAS9 : 59h : 02h]

7	6	5	4	3	2	1	0
Gamma Slope 9							
0	0	0	0	0	0	1	0

Auto Exposure

Y mean value is continuously calculated every frame, and the integration time value is increased or decreased according to the displacement between current frame Y mean value and target Y mean value.



AE Mode Control 1 [AEM1 : 60h : 39h]

7	6	5	4	3	2	1	0
Anti – Banding Enable	Full Window	Window Mode		AE speed		AE Mode	

0	0	1	1	1	0	0	1

Anti-Banding Enable	When Anti-Banding is enabled, AE initializes Integration Time registers[63h-65h] to 4 x Anti-Banding Step value[6ah-6ch], and integration increment/decrement amount is set to Anti-Banding Step value in order to remove banding noise caused by intrinsic energy waveform of light sources. Banding noise is inherent in CMOS image sensor that adopts rolling shutter scheme for image acquisition. In this mode, AE operates with very large unit, typically a reciprocal of (2 x power line frequency), so that minute integration time tuning is not liable. Therefore, this mode is recommended for only indoor use.	
Full Window	With this bit set to high, window mode is discarded and full image data is accounted for AE Y frame mean evaluation	
Window Mode	11	1/8 center weighted window mode. Weighting ratio is 8:1 for inside area vs. outside area
	10	1/8 center only window mode.
	01	1/4 center weighted window mode. Weighting ratio is 4:1 for inside area vs. outside area
	00	1/4 center only window mode.
AE Speed	(fast)11 - 10 - 01 - 00(slow)	
AE Mode	11	Gain-Only control mode. Only preamp gain is controlled to get optimum exposure state.
	10	Time-Only control mode. Only integration time is controlled to get optimum exposure state.
	01	Time-Gain control mode. integration time and preamp gain are controlled to get optimum exposure state.
	00	AE function is disabled

AE Mode Control 2 [AEM2 : 61h : bah]

7	6	5	4	3	2	1	0
Gain Speed		Integration Time Fine Tune	Preamp Gain Fine Tune	Anti-Banding Minimum Break	AE Subsampli-ng mode	AE Analog Gain Control	AE Digital Gain control
1	0	1	1	1	0	1	0

Gain Speed	Gain update speed is specified as follows. (fast)11 - 10 - 01 - 00(slow)
Integration Time Fine Tune	Integration time fine tuning is performed when AE arrive around AE Fine Tune Boundary to settle into AE lock state smoothly.
Preamp Gain Fine Tune	Preamp gain fine tuning is performed when AE arrive around AE Fine Tune Boundary to settle into AE lock state smoothly.
Anti-Banding Minimum Break	When AE is still of out lock state despite that AE preamp analog gain update value exceeds preamp minimum gain value(18h) and integration time(63h-65h) is reached to AE Anti-Banding Step(6ah-6ch), integration time(63h-65h) is broken to less than AE Anti-Banding Step(6ah-6ch).
AE Subsampling Mode	AE statistics is executed on 1/4 of original image data to save power consumption
AE Analog Gain Control	AE updates preamp gain register(17h) in order to reach optimum exposure state
AE Digital Gain Control	AE updates Y digital gain register(78h) in order to reach optimum exposure state

Integration Time High [INTH: 63h : 07h]

7	6	5	4	3	2	1	0
Integration Time High [23:16]							
0	0	0	0	0	1	1	1

Integration Time Middle [INTM: 64h: a1h]

7	6	5	4	3	2	1	0
Integration Time Middle[15:8]							
1	0	1	0	0	0	0	1

Integration Time Low [INTL: 65h: 20h]

7	6	5	4	3	2	1	0
Integration Time Low[7:0]							
0	0	1	0	0	0	0	0

Integration time value register defines the time during which active pixel element evaluates photon energy that is converted to digital data output by internal ADC processing. Integration time is equivalent to exposure time of general camera so that integration time need to be increased in dark environment

and decreased according to lighting condition. Maximum integration time is register maximum value(2^{24}-1) x sensor clock period(80ns, SCF 12.5Mhz @ DCF 25Mhz) = 1.34sec.

AE Target [AETGT : 66h : 70h]

7	6	5	4	3	2	1	0
AE Target							
0	1	1	1	0	0	0	0

This register defines the target luminance value for AE operation.

AE Lock Boundary [AELBND : 67h : a2h]

7	6	5	4	3	2	1	0
AE Fine Boundary				AE Lock Boundary			
1	0	1	0	0	0	1	0

AE Lock Boundary specifies the displacement of Y Frame Mean value(7dh) from AE Target in which AE goes into LOCK state. With Anti-Banding is enabled, this displacement condition is discarded, and instead AE Unlock Boundary is used as Lock boundary.

AE Fine Boundary specifies the displacement of Y Frame Mean value(7dh) from AE Target in which AE start to tune fine integration time or preamp gain in order to goes into lock state smoothly.

AE Unlock Boundary [AEUNLCK : 68h : 2ah]

7	6	5	4	3	2	1	0
AE Unlock Boundary							
0	0	1	0	1	0	1	0

AE Unlock Boundary 0 specifies Y Frame Mean displacement from AE Target where integration time increment/decrement speed changes from 2x (integration unit step) to 1x (integration unit step). In anti-banding mode, this boundary is used as lock boundary for exposure control.

AE Anti-Banding Step High [AEANTH : 6ah : 1h]

7	6	5	4	3	2	1	0
reserved						AE Anti-Banding Step High	
0	0	0	0	0	0	0	1

AE Anti-Banding Step Middle [AEANTM : 6bh : e8h]

7	6	5	4	3	2	1	0

AE Anti-Banding Step High							
1	1	1	0	1	0	0	0

AE Anti-Banding Step Low [AEANTL : 6ch : 48h]

7	6	5	4	3	2	1	0
AE Anti-Banding Step Low							
0	1	0	0	1	0	0	0

AE Anti-Banding Step specifies integration time unit value that AE uses when Anti-Banding is enabled. Anti-Banding Step value is resolved by the following equation.

Anti-Banding Step Value = Sensor Operation Frequency (SCF) / (2x power line frequency)

The default value is set with SCF 12.5Mhz, 50Hz power line, that is,

Anti-Banding Step Value = 12.5Mhz / (2 x 50) = 125000d = 1e848h

AE Integration Time Limit High [AELMH : 6dh : 17h]

7	6	5	4	3	2	1	0
AE Integration Time Limit High							
0	0	0	1	0	1	1	1

AE Integration Time Limit Middle [AELMM : 6eh : d7h]

7	6	5	4	3	2	1	0
AE Integration Time Limit Middle							
1	1	0	1	0	1	1	1

AE Integration Time Limit Low [AELML : 6fh : 84h]

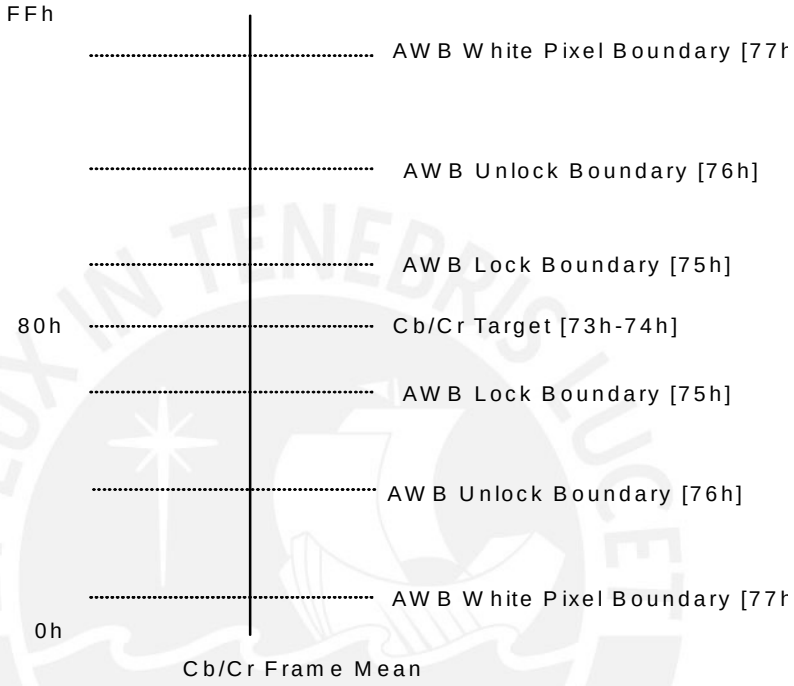
7	6	5	4	3	2	1	0
AE Integration Time Limit Low							
1	0	0	0	0	1	0	0

These three registers define the maximum integration time value that is allowed to sensor operation. It is desirable to set the value to multiples of AE Anti-Banding Step to easily operate with Anti-banding mode enabled. The default value is set to 1/8sec with SCF set to 25Mhz

12.5Mhz / 8 = 1,562,500 = 17d784

Auto White Balance

Cb/Cr frame mean value is calculated every frame and according to Cb/Cr frame mean values' displacement from Cb/Cr white target point, R/B scaling values for R/B data are resolved.



AWB Mode Control 1 [AWBM : 70h : 41h]

7	6	5	4	3	2	1	0
reserved	Full Window	Window Mode		AWB speed		reserved	AWB On
0	1	0	0	0	0	0	1

Full Window	With this bit set to high, window mode is discarded and full image data is accounted for AE Y frame mean evaluation	
Window Mode	11	1/8 center weighted window mode. Weighting ratio is 8:1 for inside area vs. outside area
	10	1/8 center only window mode.
	01	1/4 center weighted window mode. Weighting ratio is 4:1 for inside area vs. outside area
	00	1/4 center only window mode.

AWB Speed	(Fast)11 - 10 - 01 - 00(slow)
AWB On	Auto White Balance Control Enabled

AWB Mode Control 2 [AEM2 : 71h : 02h]

7	6	5	4	3	2	1	0
Reserved				AWB Low Speed	AWB Subsampli-ng mode	AWB Analog Gain Control	AWB Digital Gain control
0	0	0	0	0	0	1	0

AWB Low Speed	With this bit set to high, analog gain speed is decreased to 1/4 of the normal speed.
AWB Subsampling Mode	AWB statistics is executed on 1/4 of original image data to save power consumption
AWB Analog Gain Control	AWB updates R/B gain registers(14h,16h) in order to reach optimum white balance state
AWB Digital Gain Control	AWB updates Cb/Cr digital gain registers(79h,7ah) in order to reach optimum white balance state

Cb Target [CBTGT : 73h : 80h]

7	6	5	4	3	2	1	0
Cb Target							
1	0	0	0	0	0	0	0

This register defines Cb target frame mean value for AWB operation.

Cr Target [CRTGT : 74h : 80h]

7	6	5	4	3	2	1	0
Cr Target							
1	0	0	0	0	0	0	0

This register defines Cr target frame mean value for AWB operation.

AWB Lock Boundary [AWBLB : 75h : 2h]

7	6	5	4	3	2	1	0
Reserved				AWB Lock Boundary			

0	0	0	0	0	0	1	0

It specifies Cb/Cr frame mean values' displacement from Cb/Cr Target (73h-74h) value where AWB goes into LOCK state.

AWB Unlock Boundary [AWBUB : 76h : 06h]

7	6	5	4	3	2	1	0
AWB Unlock Boundary							
0	0	0	0	0	1	1	0

It specifies Cb/Cr frame mean values' displacement from Cb/Cr Target (73h-74h) where AWB is released from LOCK state. AWB operation retains LOCK state unless Cb/Cr frame mean values' displacement value exceeds this boundary. The value should be larger AWB Lock Boundary.

AWB White Pixel Boundary [AWBWPB : 77h : 30h]

7	6	5	4	3	2	1	0
AWB White Pixel Boundary							
0	0	1	1	0	0	0	0

When Cb/Cr frame mean values' displacement from Cb/Cr Target exceeds AWB White Pixel Boundary value, AWB accept frame color as it is and does not try to correct white balance deviation.

Y Digital Gain [YGAIN : 78h : 40h]

7	6	5	4	3	2	1	0
Y Digital Gain							
0	1	0	0	0	0	0	0

The register represents the current Y digital gain value (1/64 resolution) in Digital Gain block, and is updated every frame by AE logic when AE digital gain update mode is active.

Cb Digital Gain [CBGAIN : 79h : 40]

7	6	5	4	3	2	1	0
Cb Digital Gain							
0	1	0	0	0	0	0	0

The register represents the current Cb digital gain value (1/64 resolution) in Digital Gain block, and is updated every frame by AWB logic when AWB digital gain update mode is active.

Cr Digital Gain [AWBSCLB : 7ah : 40h]

7	6	5	4	3	2	1	0
Cr Digital Gain							

0	1	0	0	0	0	0	0

The register represents the current Cr scaling value(1/64 resolution) in Digital Gain block, and is updated every frame by AWB logic when AWB digital gain update mode is active.

AE Status [AEST : 7bh : RO]

7	6	5	4	3	2	1	0
AE Mode State				AE Lock state			
RO	RO	RO	RO	RO	RO	RO	RO

AE Mode State	This nibble represents the mode where internal Y plane FSM is currently placed among time-gain control, time-only control, or gain-only control modes.
AE Lock State	Y channel FSM status, “0000” means that AE Y plane is in lock state

AWB Status [AWBST : 7ch : RO]

7	6	5	4	3	2	1	0
Reserved			AE/AWB Lock	Cb Lock State		Cr Lock State	
RO	RO	RO	RO	RO	RO	RO	RO

AE/AWB Lock	This single status bit indicates that AE and AWB are in lock state for optimum still image capture.
Cb Lock State	Cb channel FSM status. “00” means that AWB Cb plane is in lock state
Cr Lock State	Cr channel FSM status. “00” means that AWB Cr plane is in lock state

Y Frame Mean [YFMEAN : 7dh : RO]

7	6	5	4	3	2	1	0
Y Frame Mean							
RO	RO	RO	RO	RO	RO	RO	RO

The register reports current Y plane frame mean value.

Cb Frame Mean [CBFMEAN : 7eh : RO]

7	6	5	4	3	2	1	0
Cb Frame Mean							
RO	RO	RO	RO	RO	RO	RO	RO

The register reports current Cb plane frame mean value.

Cr Frame Mean [CRFMEAN : 7fh : RO]

7	6	5	4	3	2	1	0
Cr Frame Mean							
RO	RO	RO	RO	RO	RO	RO	RO

The register reports current Cr plane frame mean value.

Minimum Anti-Banding Gain [BNDGMIN : 80h : 08h]

7	6	5	4	3	2	1	0
Minimum Anti-Banding Gain							
0	0	0	0	1	0	0	0

The register specifies the minimum limit to which AE may decrease preamp gain or Y digital gain in order to get optimum exposure value while Anti-Banding Mode is enabled and the following condition is met.

AE Lock Boundary < (Y Frame Mean - AE Target) < AE Unlock Boundary.

Maximum Anti-Banding Gain [BNDGMAX : 81h : 18h]

7	6	5	4	3	2	1	0
Maximum Anti-Banding Gain							
0	0	0	1	1	0	0	0

The register specifies the maximum limit to which AE may increase preamp gain or Y digital gain in order to get optimum exposure value while Anti-Banding Mode is enabled and the following condition is met.

AE Lock Boundary < (AE Target - Y Frame Mean) < AE Unlock Boundary.

Integration-Scan Offset High [ISOFSH : 82h : RO]

7	6	5	4	3	2	1	0
Integration-Scan Offset High							
RO	RO	RO	RO	RO	RO	RO	RO

Integration-Scan Offset Middle [ISOFSM : 83h : RO]

7	6	5	4	3	2	1	0
Integration-Scan Offset Middle							
RO	RO	RO	RO	RO	RO	RO	RO

Integration-Scan Offset Low [ISOFSH : 84h : RO]

7	6	5	4	3	2	1	0
Integration-Scan Offset Low							
RO	RO	RO	RO	RO	RO	RO	RO

The register represents time offset between integration plane and scan plane. The value should be the same as the value specified by integration time register(63h – 65h).

AWB Luminance High Boundary [AWBLUHI : 8ah : c8h]

7	6	5	4	3	2	1	0
AWB Luminance High Boundary							
1	1	0	0	1	0	0	0

During Cb/Cr frame mean value calculation, AWB discards pixel of which luminance value is larger than this register value.

AWB Luminance Low Boundary [AWBLULO : 8bh : 0ah]

7	6	5	4	3	2	1	0
AWB Luminance Low Boundary							
0	0	0	0	1	0	1	0

During Cb/Cr frame mean value calculation, AWB discards pixel of which luminance value is smaller than this register value.

AWB Valid Number [AWBNO : 8ch : 02h]

7	6	5	4	3	2	1	0
AWB Valid Number							
0	0	0	0	0	0	1	0

AWB update when the number of valid color pixel is larger than (this valid value x 64).

Dark Bad Pixel Concealment Mode [DPCMODE : 90h : 0h]

7	6	5	4	3	2	1	0
Reserved						Dark Bad Pixel Concealment Mode	
0	0	0	0	0	0	0	0

Dark Bad Pixel Concealment	10	Dark Bad Pixel Concealment is always performed.

Mode	01	Dark Bad Pixel Concealment is performed when Integration Time (63h-65h) exceeds Dark Bad Integration Time(91h-93h)
	11, 00	Dark Bad Pixel Concealment is turned off

Dark Bad Integration Time High [DPCINTH : 91h : 13h]

7	6	5	4	3	2	1	0
Dark Bad Integration Time High							
0	0	0	1	0	0	1	1

Dark Bad Integration Time Middle [DPCINTM : 92h : 12h]

7	6	5	4	3	2	1	0
Dark Bad Integration Time Middle							
0	0	0	1	0	0	1	0

Dark Bad Integration Time Low [DPCINTL : 93h : d0h]

7	6	5	4	3	2	1	0
Dark Bad Integration Time Low							
1	1	0	1	0	0	0	0

Dark Bad Integration Time registers(91h-93h) specify minimum integration time value(63h-65h) where dark bad concealment operation is performed when dark bad pixel concealment mode is “01 (binary)”.

Dark Bad G Threshold [DPCGTH : 94h : 0ch]

7	6	5	4	3	2	1	0
Dark Bad G Threshold							
0	0	0	0	1	1	0	0

The register value specify the current G pixel’s differential value with neighboring G pixels, and is used to check whether current G pixel is dark bad pixel or not.

Dark Bad C Threshold [DPCGTH : 95h : 0ch]

7	6	5	4	3	2	1	0
Dark Bad C Threshold							
0	0	0	0	1	1	0	0

The register value specify the current R or B pixel's differential value with neighboring G pixels, and is used to check whether current R or B pixel is dark bad pixel or not.

Frame Timing

For clear description of frame timing, clocks' acronym and relation are reminded in here again.

< Clock Acronym Definition >

MCF : Master Clock Frequency	DCF : Divided Clock Frequency
SCF : Sensor Clock Frequency	ICF : Image Processing Clock Frequency
VCF : Video Clock Frequency	LCF : Line Clock Frequency

< Clock Frequency Relation >

MCF : MCF	DCF : MCF/Clock Division	
SCF : DCF/2	ICF	SCF for 3x3 interpolation, SCF/2 for 1/4 subsampling mode SCF/4 for 1/16 subsampling mode
VCF : ICF for 16bit output, ICF*2 for 8bit output	LCF : 1/(HBLANK Period + HSYNC Period)	

HBLANK Period : HBLANK Time register value * (1/SCF)

HSYNC Period : HSYNC Active Time

< Frame Time Calculation >

Core Frame Time is

(IDLE SLOT + Video Height * LCP)

and Real Frame Time is resolved as follows.

When Integration Time > Core Frame Time, Real Frame Time is (Integration Time + VBLANK * LCP), otherwise is (Core Frame Time + VBLANK * LCP).

1. 3x3 Color Interpolation Timing

3x3 Color Interpolation Frame Timing Related Parameters			
Master Clock Frequency(MCF)	20Mhz	Divided Clock Frequency(DCF)	MCF/1 = 20Mhz
Sensor Clock Frequency(SCF)	DCF/2 = 10Mhz	Sensor Clock Period(SCP)	1/10Mhz = 100ns
Window Width	640	Window Height	480
HBLANK Value	208	VBLANK Value	8
VSYNC Mode	Line Mode	Line Clock Period(LCP)	848 SCPs
Output Bus Width	8bit	VGA Video Output Frequency	SCF * 2 = 20Mhz

Final Video Output Size	640x480	.	.

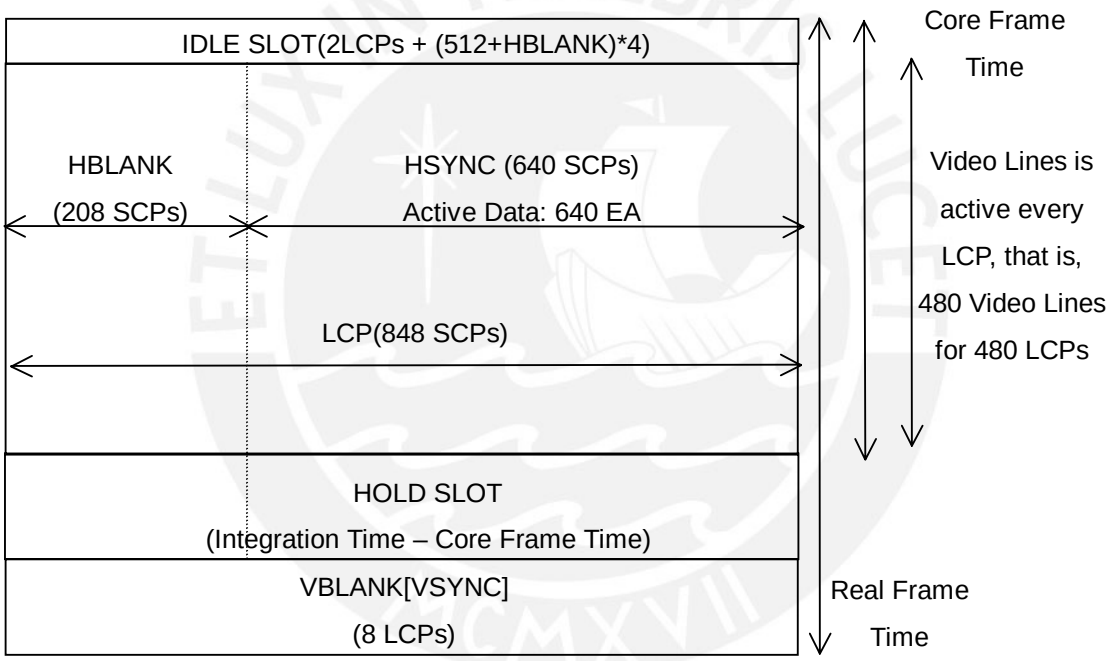
If Integration Time < Core Frame Time, Real Frame Time is

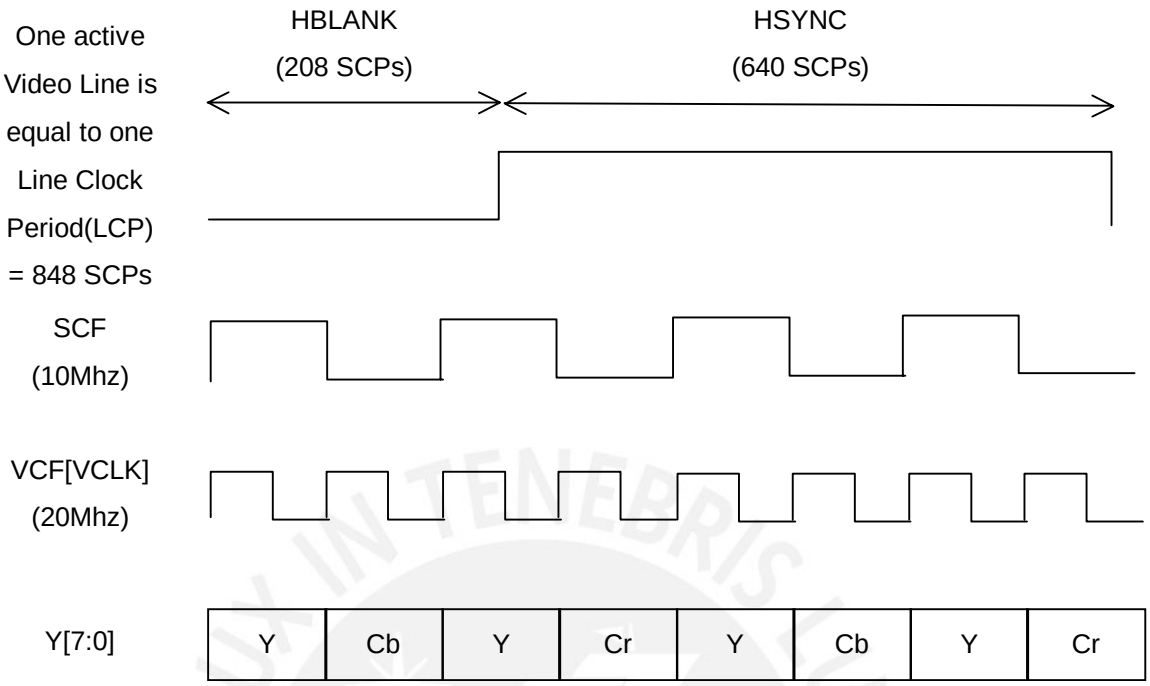
2 * (208 + 640) SCPs + 480 * (208 + 640) SCPs + 8 * (208 + 640) SCPs = 415520 SCPs = 0.041552sec

else Real Frame Time is

Integration Time * SCPs + 8 * (208 + 640) SCPs.

HOLD SLOT in frame timing appears only if integration time is larger than core frame time.

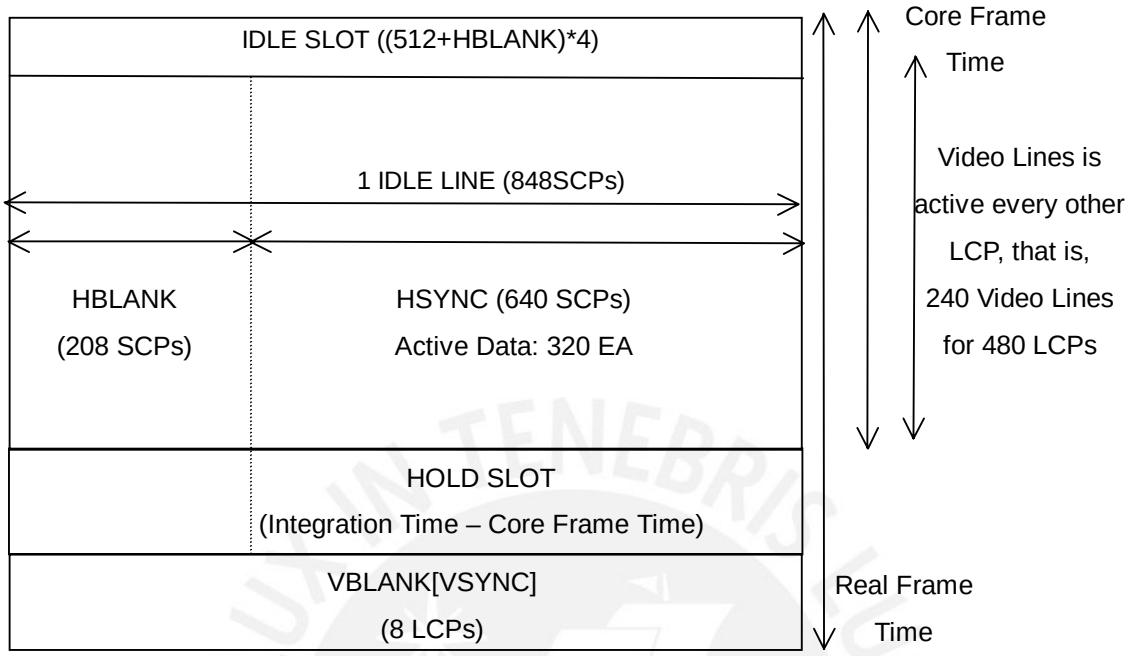


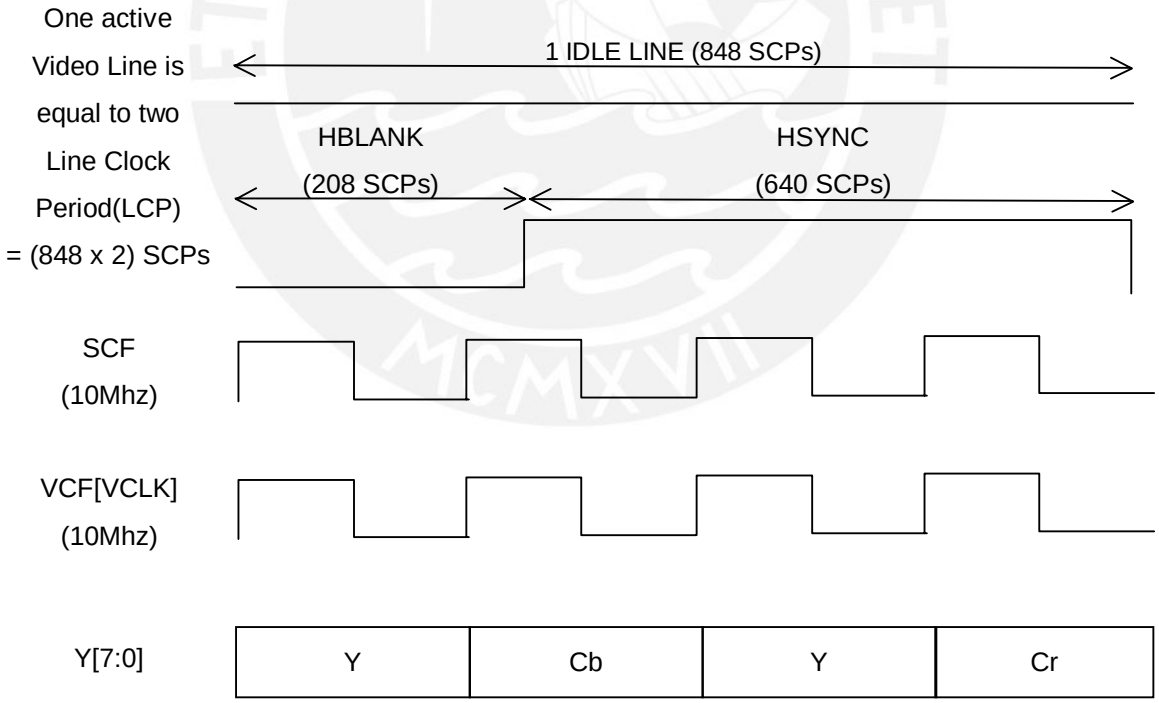


2. 1/4 Subsampling Timing

1/4 Subsampling Frame Timing Related Parameters			
Master Clock Frequency(MCF)	20Mhz	Divided Clock Frequency(DCF)	MCF/1 = 20Mhz
Sensor Clock Frequency(SCF)	DCF/2 = 10Mhz	Sensor Clock Period(SCP)	1/10Mhz = 100ns
Window Width	640	Window Height	480
HBLANK Value	208	VBLANK Value	8
VSYNC Mode	Line Mode	Line Clock Period(LCP)	848 * 2 SCPs
Output Bus Width	8bit	SIF Video Output Frequency	SCF * 1 = 10Mhz
Final Video Output Size	320x240		

In 1/4 subsampling mode, valid video data is produced every other line, i.e. for 480 LCPs, active video lines are 240. HSYNC active time is equal to HSYNC active time of 3x3 color interpolation mode, but video clock frequency is half of 3x3 color interpolation mode's to produce half size output in horizontal direction.



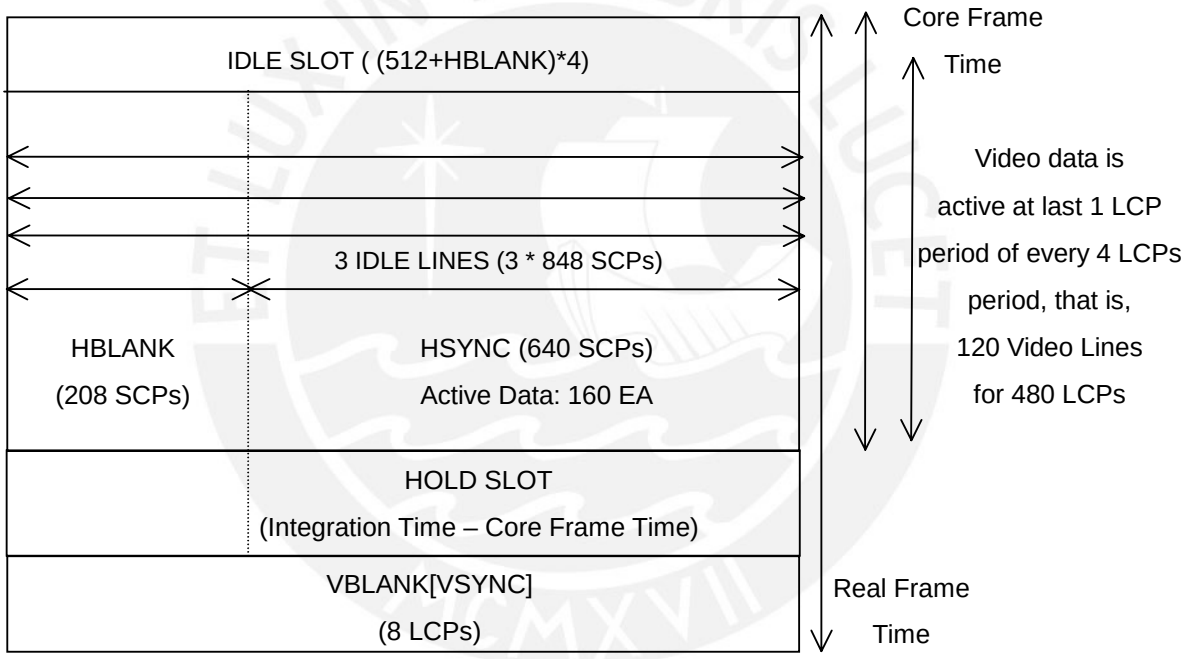


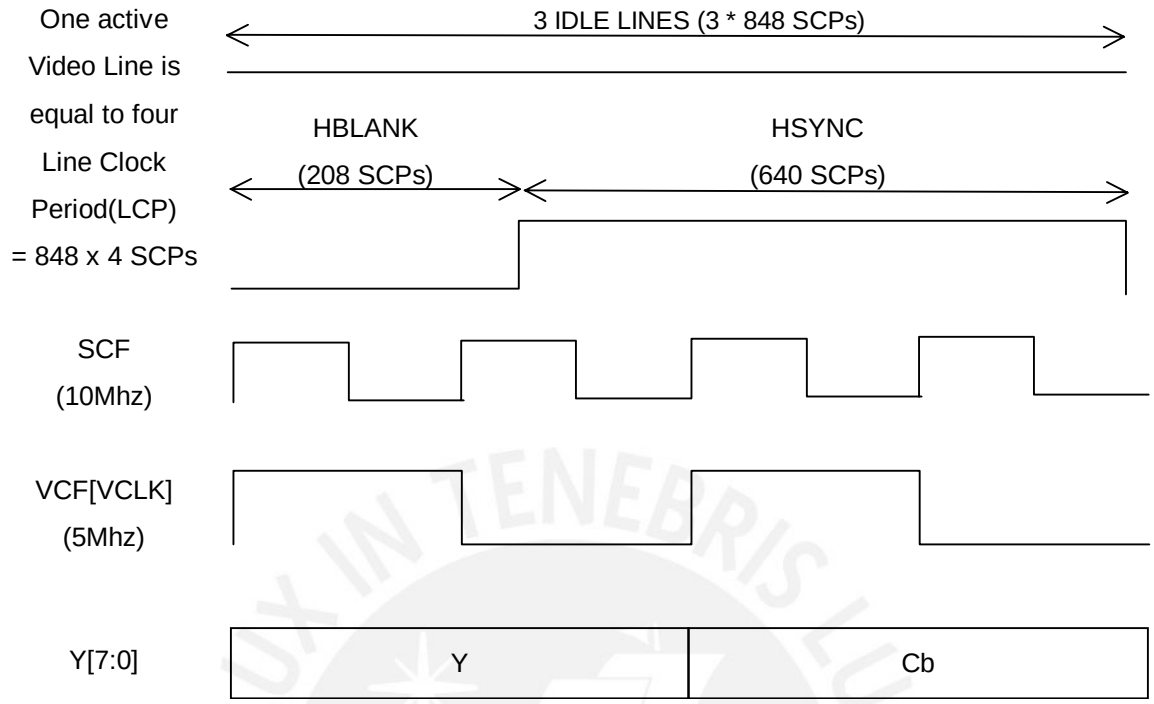
3. 1/16 Subsampling Timing

1/16 Subsampling Frame Timing Related Parameters			
Master Clock Frequency(MCF)	20Mhz	Divided Clock Frequency(DCF)	MCF/1 = 20Mhz
Sensor Clock Frequency(SCF)	DCF/2 = 10Mhz	Sensor Clock Period(SCP)	1/10Mhz = 100ns

Window Width	640	Window Height	480
HBLANK Value	208	VBLANK Value	8
VSYNC Mode	Line Mode	Line Clock Period(LCP)	848 * 4 SCPs
Output Bus Width	8bit	QSIF Video Output Frequency	SCF / 2 = 5Mhz
Final Video Output Size	160x120		

In 1/16 subsampling mode, valid video data is produced every four line, i.e. for 480 LCPs, active video lines are 120. HSYNC active time is equal to HSYNC active time of 3x3 color interpolation mode, but video clock frequency is a quarter of 3x3 color interpolation mode's to produce a quarter size output in horizontal direction.





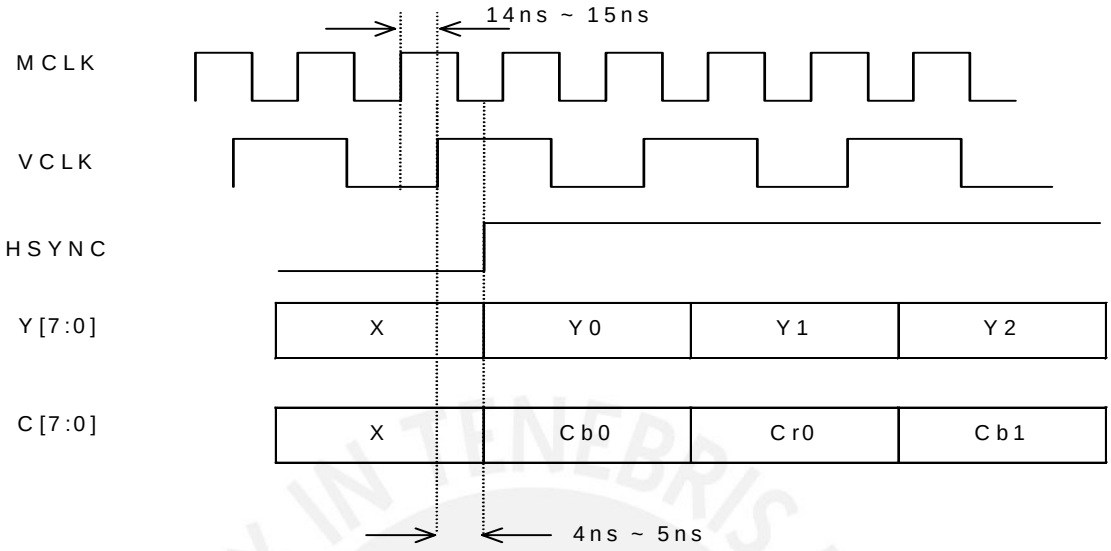
Anti-Banding Configuration

For Anti-Banding mode to work correctly, the following registers should be configured to the appropriate values.

AE Mode	60h	Anti-Banding Enable[7]
AE Anti-Banding Step	6a-6ch	SCF / (2 x power line frequency)
AE Integration Time Limit	6d-6fh	The value should be multiples of AE Anti-Banding Step

When Anti-Banding is enabled, AE initializes Integration Time registers[63-65h] to 4 x Anti-Banding Step value[6a-6ch], and integration increment/decrement amount is set to Anti-Banding Step value in order to remove anti-banding noise caused by intrinsic energy waveform of light sources. Banding noise is inherent in CMOS image sensor that adopts rolling shutter scheme for image acquisition.

Data Output Timing and Interface



As specified in the above data output timing diagram, the timing margin between video clock pin (VCLK) and data pins (Y[7:0] or C[7:0]) is about 4ns ~ 5ns. This margin may be sufficient or not according to how much video clock and data pins are delayed internally in the backend chip, respectively. To safely latch the data output in the backend chip, it is recommended that data be latched at negative edge of VCLK. The above timing margin diagram represents 16bit output interface, but is also valid for 8bit output interface.

Output Data Format

Output Format is controlled by configuring Output Format register[31h]. Configurable options are specified again for your reference.

Output Format [OUTFMT : 31h : 39h]

7	6	5	4	3	2	1	0
reserved	reserved	Cb First	Y First	8 Bit Output	reserved	YCbCr 4:4:4	YCbCr 4:2:2
0	0	1	1	1	0	0	1

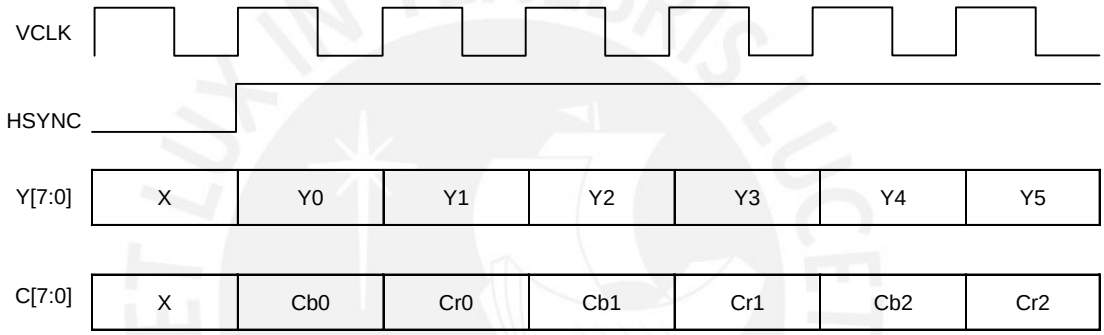
Cb First	Cb pixel in front of Cr pixel in 16bit or 8bit video data output modes
Y First	Y pixel in front of Cb and Cr pixels in 8bit video output mode. This option is meaningful only with 8bit output mode.
8 Bit Output	Image Data is produced only in Y[7:0]. C[7:0] should be discarded

YCbCr 4:4:4	YCbCr 24bit data for a pixel is produced with 16bit output mode. With color space conversion disabled, RGB 24bit data for a pixel is produced in this mode. This mode is meaningful only with 16bit output mode.
YCbCr 4:2:2	YCbCr data for a pixel is produced with 8/16 output mode

Output timings for general configurations are described below. Slot named as “X” means that it is has no meaningful value and should be discarded.

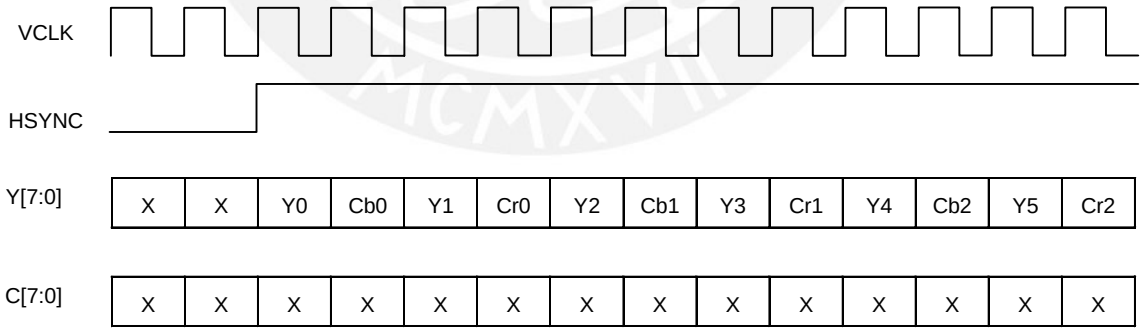
1. YCbCr 4:2:2 with 16bit output

Register bit configurations: 16bit output, Cb First, YCbCr 4:2:2



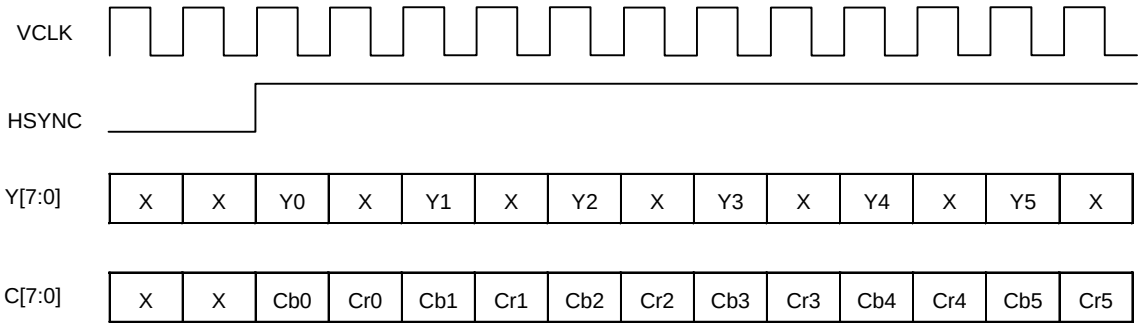
2. YCbCr 4:2:2 with 8bit output

Register bit configurations: 8bit output, Y First, Cb First, YCbCr 4:2:2



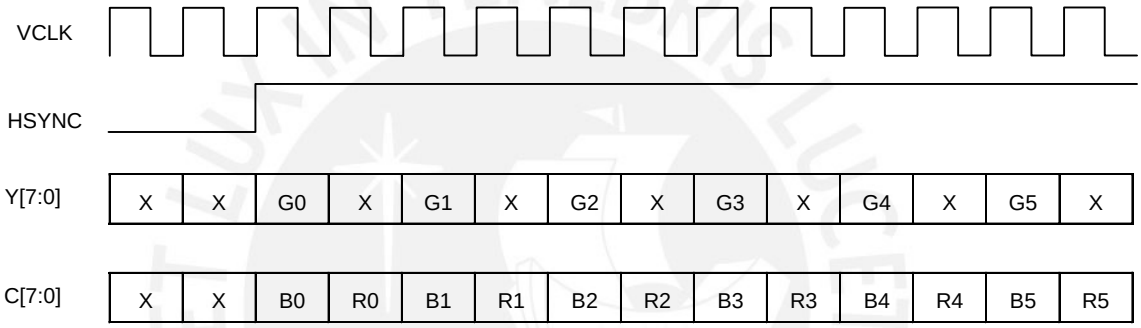
3. 24bit YCbCr 4:4:4 output

Register bit configurations : 8bit output, Y First, Cb First, YCbCr 4:4:4, and color space conversion enabled



4. 24bit RGB 4:4:4 output

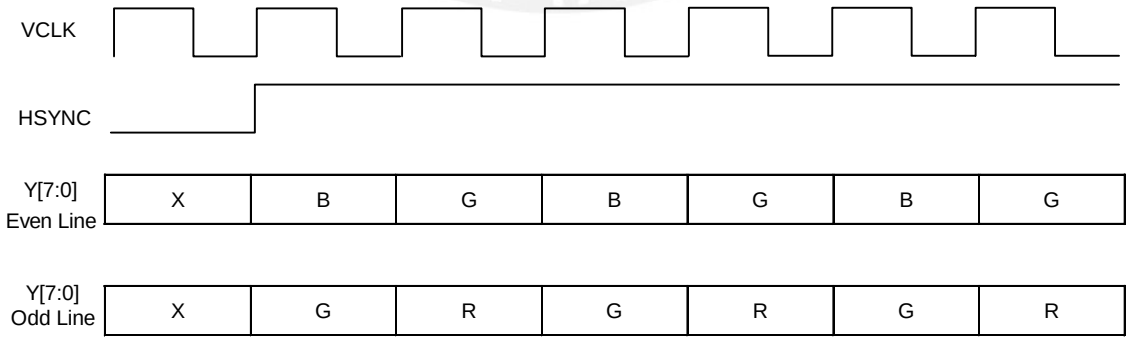
Register bit configurations : 8bit output, Y First, Cb First, YCbCr 4:4:4, and color space conversion disabled



Bayer Data Format

SCTRA[1:0] is set to Bayer mode

- When Bayer output mode is selected, Window Width x Window Height raw image data are produced with the following sequence. After VSYNC goes low state, the first HSYNC line of a frame is activated with B pixel data appearing first when both of Column Start Address and Row Start Address are even.



I2C Chip Interface

Register Write Sequences

One Byte Write

S	22H	A	01H	A	03H	A	P
*1	*2	*3	*4	*5	*6	*7	*8

Set "Sensor Control A" register into Window mode

*1. Drive: I2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit]

*3. Read: acknowledge from sensor

*4. Drive: 01H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: 03H [Video Mode : CIF

*7. Read: acknowledge from sensor

*8. Drive: I2C stop condition

Multiple Byte Write using Auto Address Increment

S	22H	A	6aH	A	51H	A	61H	A	P
*1	*2	*3	*4	*5	*6	*7	*8	*9	*10

Set "AE Integration Step High/Low" register as 5161H with auto address increment

*1. Drive: I2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit]

*3. Read: acknowledge from sensor

*4. Drive: 6aH [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: 51H [AE Integration Step High]

*7. Read: acknowledge from sensor

*8. Drive: 61H [AE Integration Step Low]

*9. Read: acknowledge from sensor

*10. Drive: I2C stop condition

Register Read Sequence

S	22H	A	50H	A	S	23H	A	Data of 50H	A	P
*1	*2	*3	*4	*5	*6	*7	*8	*9	*10	*11

Read "Reset Level Control" register from HV7131GP

*1. Drive: I2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit(be careful. R/W=0)]

*3. Read: acknowledge from sensor

*4. Drive: 50H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: I^2C start condition

*7. Drive: 23H(001_0001 + 1) [device address + R/W bit(be careful. R/W=1)]

*8. Read: acknowledge from sensor

*9. Read: Read “Reset Level Control Value” from sensor

*10. Drive: acknowledge to sensor. If there is more data bytes to read, SDA should be driven to low and data read states(*9, *10) is repeated. Otherwise SDA should be driven to high to prepare for the read transaction end.

*11. Drive: I2C stop condition

AC/DC Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Units	Min.	Max.
Vdpp	Digital supply voltage	Volts	-0.3	7.0
Vapp	Analog supply voltage	Volts	-0.3	7.0
Vipp	Input signal voltage	Volts	-0.3	7.0
Top	Operating Temperature	°C	-30	70
Tst	Storage Temperature	°C	-40	85

Caution: Stresses exceeding the absolute maximum ratings may induce failure.

DC Characteristic

Symbol	Parameter	Units	Min.	Typical.	Max.	Conditions&Note
V_{dd}	Internal operation supply voltage	Volt	2.6	-	3.0	-
I_{dd}	Operating current consumption	mA		-	40	At 15fps(12.5Mhz)
HsI_{dd}	Hard Sleep Static current consumption	uA		-	48	At 15fps(12.5Mhz)
SsI_{dd}	Soft Sleep Static current consumption	uA	-	-	276	At 15fps(12.5Mhz)
V_{ih}	Input voltage logic "1"	Volt	2.0	-	3.0	-
V_{il}	Input voltage logic "0"	Volt	0	-	0.8	-
V_{oh}	Output voltage logic "1"	Volt	2	-	-	at Ioh = -4mA
V_{ol}	Output voltage logic "0"	Volt	-	-	0.4	at Iol = 4mA
Iih	Input High Current	uA	-10	-	10	-
Iil	Input Low Current	uA	-10	-	10	-
T_a	Ambient operating temperature	Celsius	-10	-	50	-
Cin	Input capacitance	pF	5	-	-	-
Cout	Output capacitance	pF	-	-	30	-
Cbid	Bi-directional buffer capacitance	pF	-	-	30	-
R_{Epud}	External pull-up / pull-down resistance	Ohm	-	-	20k	1)

Note.1) R Epud is just applied to SDA and SCK pin. And If R Epud is less than 20K Ohm, power consumption is increased.

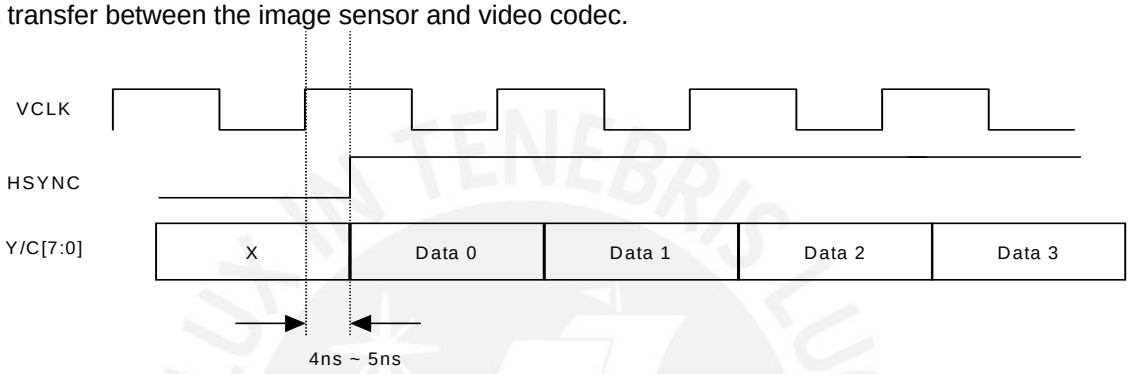
AC Operating Conditions

Symbol	Parameter	Max Operation Frequency	Units	Notes
MCLK	Main clock frequency	25	MHz	1,2
SCK	I^2C clock frequency	400	KHz	3

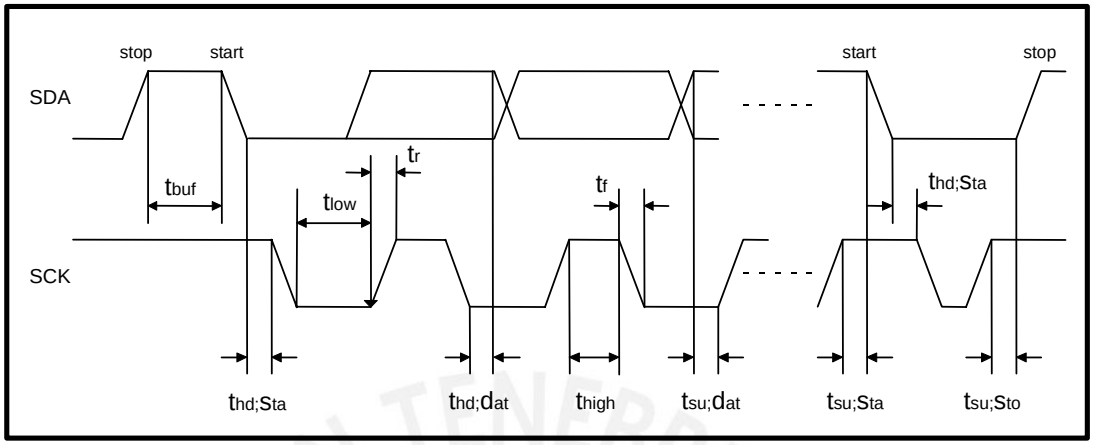
1. MCLK may be divided by internal clock division logic for easy integration with high speed video codec system.
2. Frame Rate : 30 frames/sec at 25Mhz, HBLANK = 208, VBLANK = 8
3. SCK is driven by host processor. For the detail serial bus timing, refer to I2C chip interface section

Output AC Characteristics

All output timing delays are measured with output load 60[pF]. Output delay includes the internal clock path delay and output driving delay that changes in respect to the output load, the operating environment, and a board design. Due to the variable valid time delay of the output, video output signals Y[7:0], C[7:0], HSYNC, and VSYNC may be latched in the negative edge of VCLK for the stable data transfer between the image sensor and video codec.



I2C Bus Timing



Parameter	Symbol	Min.	Max.	Unit
SCK clock frequency	f_{sck}	0	400	KHz
Time that I^2C bus must be free before a new transmission can start	t_{buf}	1.2	-	us
Hold time for a START	$t_{hd;sta}$	1.0	-	us
LOW period of SCK	t_{low}	1.2	-	us
HIGH period of SCK	t_{high}	1.0	-	us
Setup time for START	$t_{su;sta}$	1.05	-	us
Data hold time	$t_{hd;dat}$	0.1	-	us
Data setup time	$t_{su;dat}$	250	-	ns
Rise time of both SDA and SCK	t_r	-	250	ns
Fall time of both SDA and SCK	t_f	-	300	ns
Setup time for STOP	$t_{su;sto}$	1.05	-	us
Capacitive load of SCK/SDA	C_b	-	30	pf

Electro-Optical Characteristics

Parameter	Units	Min.	Typical	Max.	Note
Sensitivity	mV / lux·sec		3000		Green Pixel
Dark Signal	mV		12		1/10" , 60℃
Output Saturation Signal	mV		1000		

- Color temperature of light source: 3200K / IR cut-off filter (CM-500S, 1mm thickness) is used.

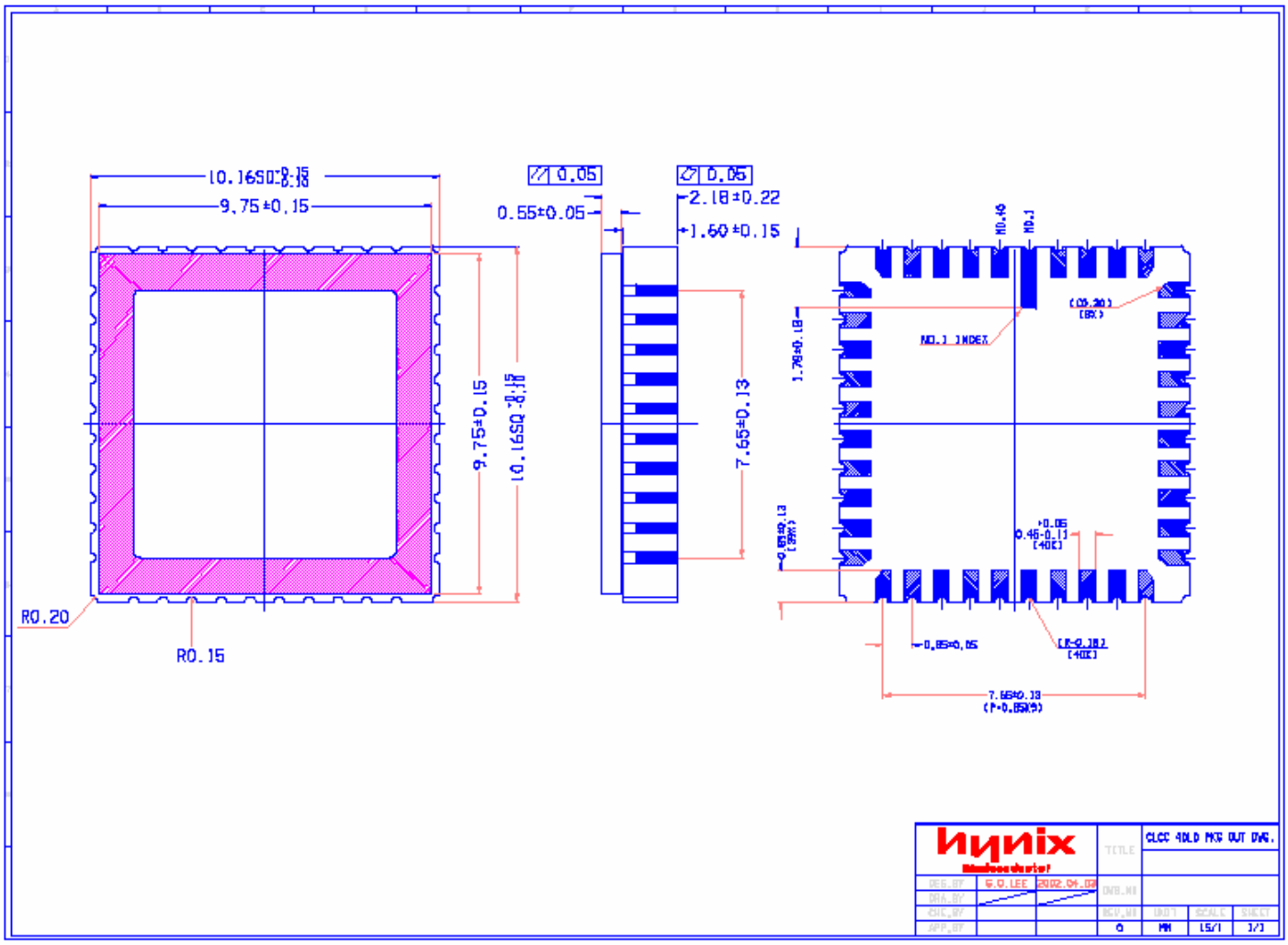
Soldering

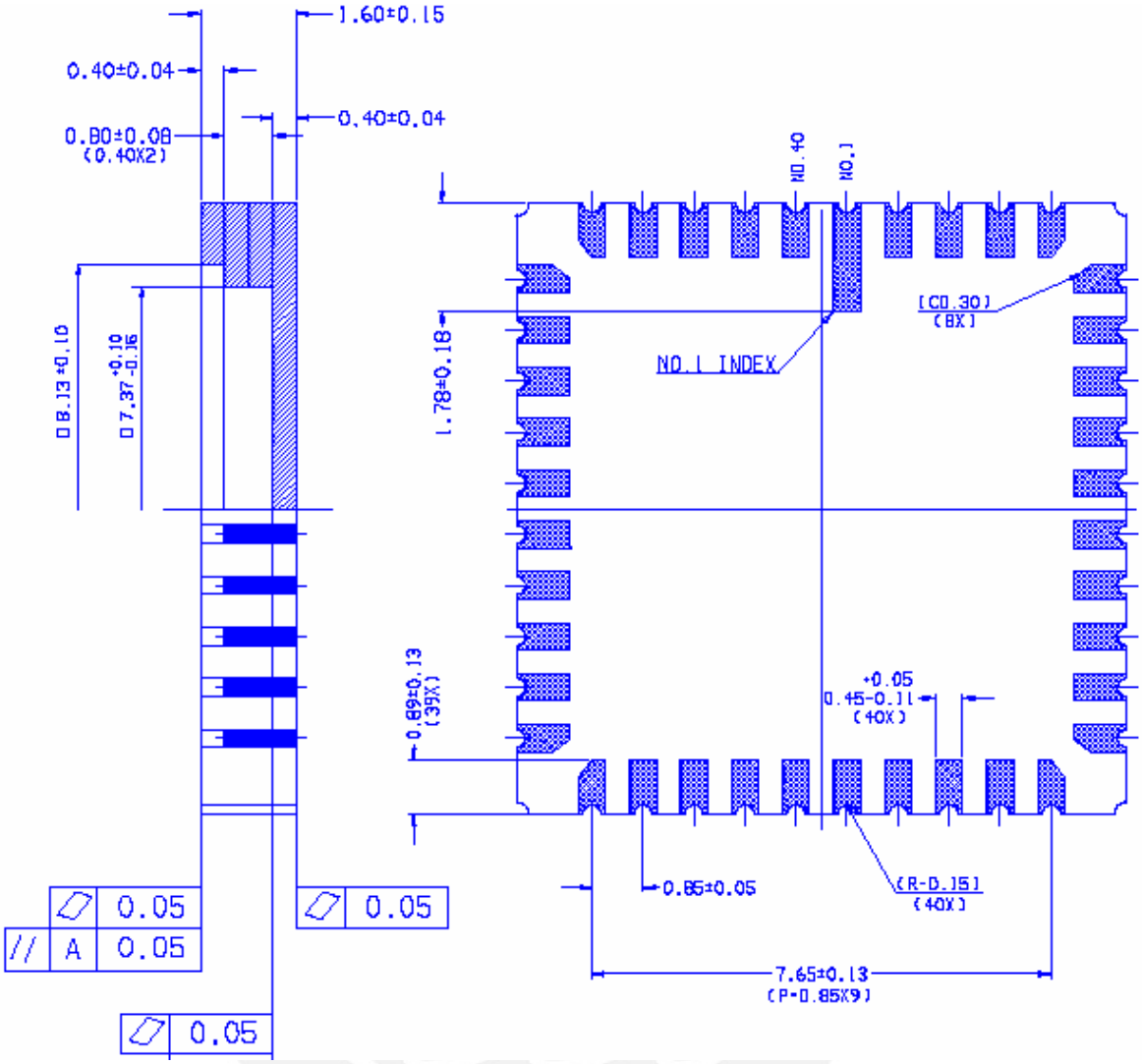
Infrared(IR) / Convection solder reflow condition

Parameter	Units	Min.	Typical	Max.	Note
Peak Temperature Range	Celsius	-	230	240	1)

Note: 1) Time within 5 Celsius of actual peak temperature, 10sec

CLCC Package Specification





* To the matter concerning package, Wafer business companies are unrelated contents.

MagnaChip Semiconductor Ltd.

* Contact Point *

CIS Marketing Team

891 Daechi-dong Kangnam-Gu Seoul 135-738 Korea

Tel: 82-2-3459-5577

Fax: 82-2-3459-5580

E-mail : hanho1.lee@magnachip.com

ATP Industrial Grade SD Card Specification

AF512SDI-5ACXX

AF1GSDI-5ACXX

AF2GSDI-5ADXX

AF4GSDI-5ACXX

AF8GSDI-5ACXX

Revision 3.7

Disclaimer:

ATP Electronics Inc. shall not be liable for any errors or omissions that may appear in this document, and disclaims responsibility for any consequences resulting from the use of the information set forth herein.

The information in this manual is subject to change without notice.

ATP general policy does not recommend the use of its products in life support applications where in a failure or malfunction of the product may directly threaten life or injury.

The information set forth in this document is considered to be "Proprietary" and "Confidential" property owned by ATP.

Revision History

Date	Version	Changes compared to previous issue
April 15th, 2008	1.0	- Base version
August 13th, 2008	1.1	- Add 8GB item
Sep. 19th, 2010	1.2	- Combine SDHC product spec with SD product spec - Update the product performance - Add Bend,Torque, Salt Spray, Solar Radiation certification - Add ESD, Water, Dust proof certification - Update MTBF
Mar. 4th, 2011	2.0	- Update P/N - Update MTBF
May. 24th, 2011	2.1	- Revise 8GB P/N - Revise performance
May. 31st, 2011	2.2	- Add density 16GB - Update performance
Jul. 6th, 2011	2.3	- Revise P/N - Update performance
Jul. 20th, 2011	2.4	- Revise
Jul. 27th, 2011	3.0	- Revise
Nov. 1st, 2011	3.1	- Add 4GB/8GB density - Add ATP SD life monitor tool
Nov. 17th, 2011	3.2	- Update Performance
Mar. 13th, 2012	3.3	- Add new features: StaticDataRefresh and SD Life Monitoring Tool - Add TBW (Total Bytes Written) information - Add 1GB density and performance
Mar. 29th, 2012	3.4	- Add SPI mode information in Chapter 7
Jun. 21st, 2012	3.5	- Separate specification by models - Revise endurance information

Aug. 6th, 2012	3.6	- Update AF512SDI-5ACXX
Sep. 19th, 2012	3.7	- Product line up AF512SDI-5ACXX, AF1GSDI-5ACXX, AF2GSDI-5ADXX, AF4GSDI-5ACXX, AF8GSDI-5ACXX - Update Data Retention information

Table of Contents

1 ATP Industrial Grade SD/SDHC Card Overview

1.1 ATP Product Availability

Figure 1-1: Product Pictures

ATP P/N	CAPACITY
AF512SDI-5ACXX	512MB
AF1GSDI-5ACXX	1GB
*AF2GSDI-5ADXX	2GB
*AF4GSDI-5ACXX	4GB
*AF8GSDI-5ACXX	8GB

Table 1-1: Capacities

*Note: Support by project, please contact ATP for more information.

1.2 Main Features

- Compatible with SD Specifications Version 2.00
- Support SD mode, SPI mode
- High reliability, operating at -40°C to 85°C
- SLC (Single-Level-Cell) NAND Flash
- Water proof, Dust proof and ESD proof
- SIP (System-In-Package) process
- Resistance to Shock and Vibration
- Enhanced endurance by Global Wear Leveling algorithm
- SaticDataRefresh technology to ensure data integrity in read operations
- Available Life Monitor Tool to check the remaining life of ATP SD/SDHC card
- Enhanced power cycling support
- Support BCH ECC up to 40bits/1KByte
- Supports CPRM
- Form factor: 32 x 24 x 2.1mm
- RoHS compliant
- CE & FCC certification
- Controlled BOM
- Customized service: adjustable CID registers, firmware & setting and label by projects

1.3 Application

ATP Industrial Grade SD/SDHC cards are designed for demanding industrial applications, such as handheld computing, military/aerospace, automotive, marine navigation, embedded systems, communication equipment or networking, medical equipment, and automation, where mission-critical data requires the highest level of reliability, durability, and data integrity.

2 Product Specifications

2.1 Environment Specifications

TYPE		MEASUREMENT
Temperature	Operation	-40°C to 85°C
	Non-Operation	-40°C to 85°C
Humidity	Operation	25°C, 10% ~ 95% RH, non-condensing
	Non-Operation	40°C, 10% ~ 93% RH, non-condensing
Bend Test	Non-Operation	10N to the center of the card, 250 cycles, 30 cycles/minute
Torque Test	Non-Operation	0.15N-m or +/-2.5°, 30 cycles/minute, 1000 cycles
Salt Spray Test (MIL-STD-883G Method1009.8)	Non-Operation	35℃,Over 85% RH,5% Salt Concentration, 24 hours
Solar Radiation Test	Non-Operation	40℃ ,Irradiation 1000W/m², 24 hours
UV Light Exposure Test (ISO 7816-1)	Non-Operation	254nm, 15Ws/cm2
Drop Test	Non-Operation	150cm/Free fall, total 6 drops

Table 2-1: Environment

2.2 Reliability

TYPE	MEASUREMENT	
Number of insertions	10,000 minimum	
Endurance Technology	SLC NAND Flash block endurance: 512MB / 2GB / 4GB / 8GB: 60,000 P/E cycles 1GB: 100,000 P/E cycles	
	Global Wear Leveling algorithm	
TBW (Total Bytes Written)	512MB	6.1 Terabytes random write
		12.3 Terabytes sequential write
	1GB	20 Terabytes random write
		40 Terabytes sequential write
	2GB	24 Terabytes random write
		48 Terabytes sequential write
	4GB	48 Terabytes random write
		96 Terabytes sequential write
	8GB	96 Terabytes random write
		192 Terabytes sequential write
MTBF(@ 25°C)	>2,000,000 hours	

Table 2-2: Reliability

Note: Endurance for flash cards can be predicted based on the usage conditions applied to the device, the internal NAND flash cycles, the write amplification factor, and the wear leveling efficiency of the flash devices.

2.3 Data Retention

512MB/2GB/4GB/8GB SD card

Endurance Used	Number of P/E Cycles Used (block level)	Corresponding Data Retention at 25C use condition
10% P/E cycles	6,000 Cycles	10 years
100% P/E cycles	60,000 Cycles	1 year

1GB SD card

Endurance Used	Number of P/E Cycles Used (block level)	Corresponding Data Retention at 25C use condition
10% P/E cycles	10,000 Cycles	10 years
100% P/E cycles	100,000 Cycles	1 year

Table 2-3: Data Retention

Note 1: Data retention refers to the ability of a memory bit to retain its data state over a period of time after the data is written in NAND Flash regardless of whether the part is powered on or powered off.
A data retention failure is when there is at least 1 bit of data that cannot be read or is read incorrectly.

Note 2: NAND Flash suppliers refer to JEDEC JESD47 & JESD22 for Data Retention testing.
Based on the information provided by NAND Flash suppliers, ATP targets Data Retention as above table for reference.

2.4 Performance

Model P/N	Seq. Read (KB/s)	Seq. Write (KB/s)	Random Read (KB/s)	Random Write (KB/s)
AF512SDI-5ACXX	19579	14998	17855	5078
AF1GSDI-5ACXX	18989	17009	17123	5371
AF2GSDI-5ADXX	20634	11296	18980	4154
AF4GSDI-5ACXX	20469	18720	18196	6081
AF8GSDI-5ACXX	20317	16377	18196	5577

Table 2-4: Performance

Note: Tested by HDBench 3.40 beta6 with 40MB file size. The performance may vary depending on the configuration, firmware, setting, application and testing environment.

2.5 Electrical Characteristics

TYPE	MEASUREMENT
Card supported Voltage	2.7~3.6V
Card supported Frequency	0~50 MHz
Data Bus Width Supported	1 or 4 bits

Table 2-5: Electrical Characteristics

2.6 Extra Features

TYPE	MEASUREMENT
Water Proof	IEC 60529 Edition 2.1: 2001-02—IPX7, below 1000mm water, 30min
Dust Proof	IEC 60529 Edition 2.1: 2001-02—IP6X
ESD Proof	IEC 61000-4-2: contact pad +/- 4KV, non-contact pad (Coupling plane discharge) +/- 8KV, non-contact pad (Air discharge) +/- 15KV
RoHS Compliant	Yes

Table 2-6: Extra Features

2.7 Global Wear Leveling- Longer Life Expectancy

The program / erase cycle of each sector/page/block is finite. Writing constantly on the same spot will cause the flash to wear out quickly. Furthermore, bit errors are not proportioned to P/E cycles; sudden death may occur when the block is close to its P/E cycle limit. Then unrecoverable bit errors will cause fatal data loss (especially for system data or FAT).

Global wear leveling algorithm evenly distributes the P/E cycles of each block to minimize the possibility of one block exceeding its max P/E cycles before the rest. In return, the life expectancy of memory storage device is prolonged and the chance/occurrence of unrecoverable bit errors could be reduced.

2.8 StaticDataRefresh Technology – Ensure Data Integrity

Over time the error bits accumulate to the threshold in the flash memory cell and eventually become uncorrectable despite using the ECC engine. In the traditional handling method, the data is moved to a different location in the flash memory; despite the corrupted data is beyond repaired before the transition.

To prevent data corruption, the SD card monitors the error bit levels in every operation; when it reaches the preset threshold value, StaticDataRefresh is achieved by erasing and re-programming the data into the same block or into another block. After the re-programming operation is completed, the controller reads the data and compares the data/parity to ensure data integrity.

2.9 SD Life Monitoring Tool – Lifespan check

ATP provides SD Life Monitoring Tool, which can automatically identify ATP memory cards and check the remaining life of ATP microSD / SD cards under Windows 2000/XP/Vista/7. Users can thus evaluate ATP memory card's health status at run time and receive an early warning before its life ends.

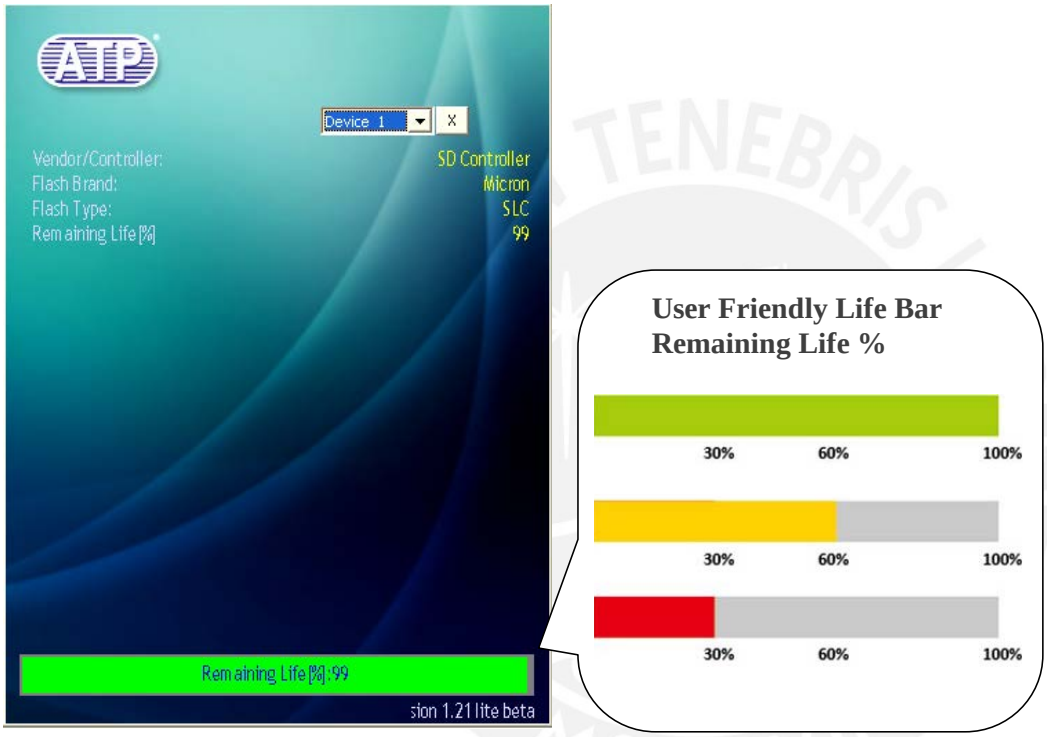


Figure 2-9: SD Life Monitoring

Note: The SD card will be busy while SD Life Monitoring Tool is retrieving the information from the SD card. Due to this reason, the user cant' execute this software from the same SD card that is being monitored.

2.10 Physical Dimension (Units in MM)

TYPE	MEASUREMENT
Length	32mm +/- 0.1mm
Width	24mm +/- 0.1mm
Thickness	2.1mm +/- 0.15mm
Weight	2.0 gram Max.

Table 2-10 Physical Dimension

2.11 Mechanical Form Factor (Units in MM)

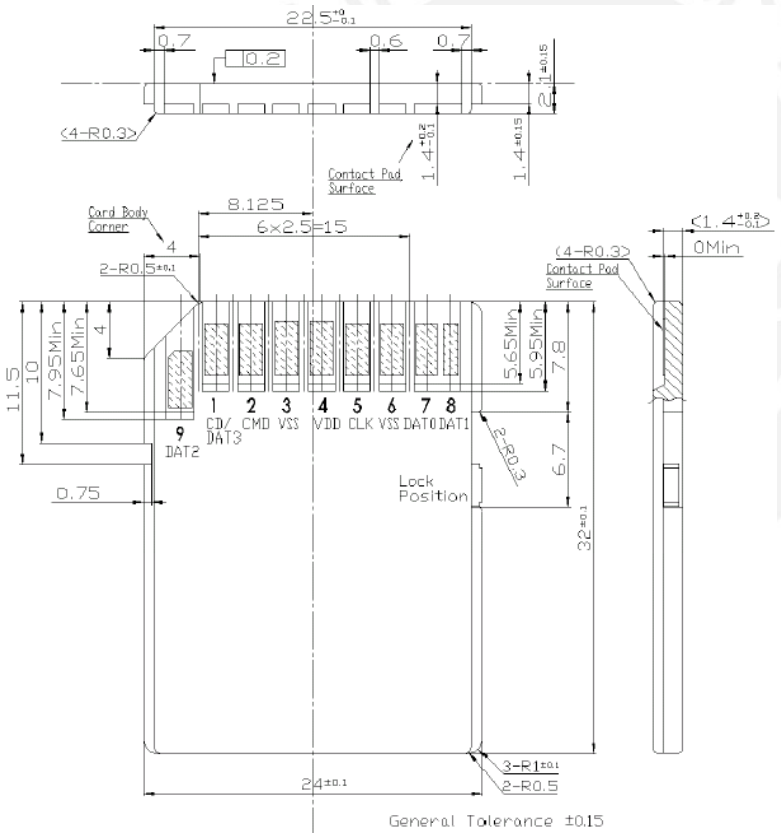


Figure 2-11: Physical Dimension

3 Electrical Characteristics

3.1 DC Characteristics

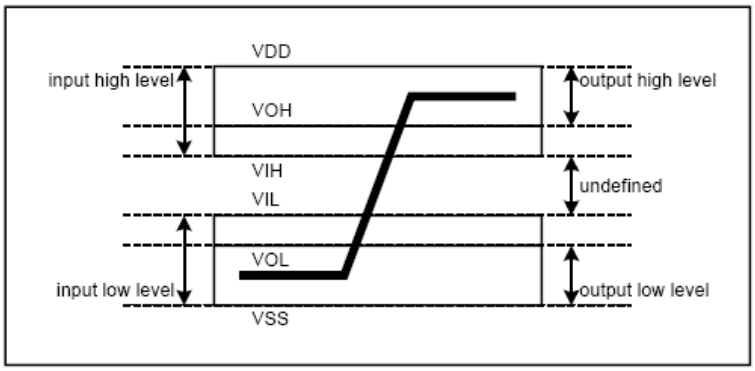


Figure 3-1: Bus Signal Level

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNIT	REMARK
Supply Voltage	V_{DD}	2.7	3.3	3.6	V	
Operating Current	I_{CC1}	-	50		mA	
Standby Current	I_{SB}	-	-	200	µA	
Input Leakage Current	I_{LI}	-10	-	10	µA	
Output Leakage Current	I_{LO}	-10	-	10	µA	
Input High Voltage	V_{IH}	0.625 x V_{DD}	-	V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	Vss -0.3	-	0.25 x V_{DD}	V	
Output High Voltage	V_{OH}	0.75x V_{DD}	-	-	V	
Output Low Voltage	V_{OL}	-	-	0.125 x V_{DD}	V	

Table 3-1: DC Characteristics

3.2 AC Characteristics

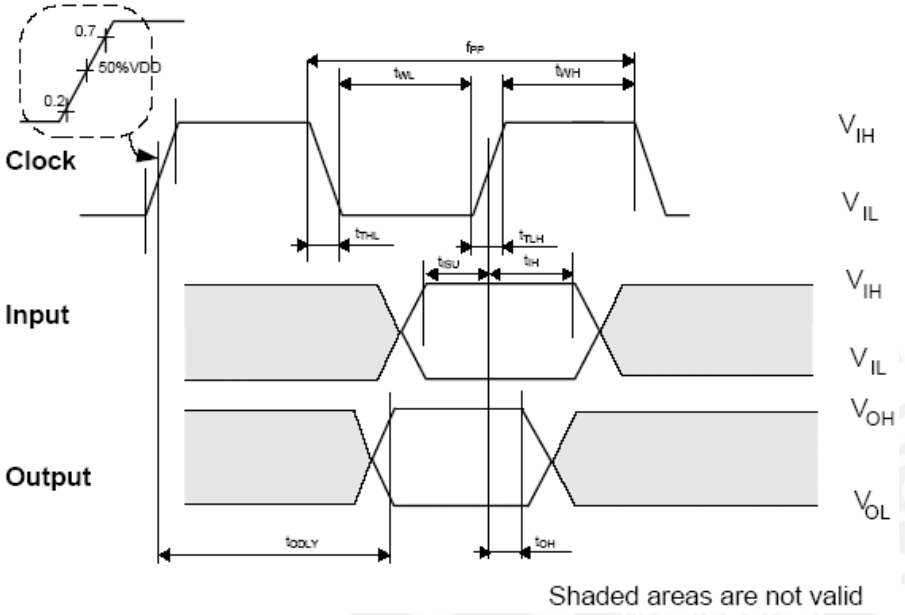


Figure 3-2: Timing diagram data input/output referenced to clock (Default)

High Speed Mode Bus Timing:

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{card} <= 10 pF(1 card)
Clock low time	t_{WL}	7	-	ns	C_{card} <= 10 pF(1 card)
Clock high time	t_{WH}	7	-	ns	C_{card} <= 10 pF(1 card)
Clock rise time	t_{TLH}	-	3	ns	C_{card} <= 10 pF(1 card)
Clock fall time	t_{THL}	-	3	ns	C_{card} <= 10 pF(1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6	-	ns	C_{card} <= 10 pF(1 card)
Input hold time	t_{IH}	2	-	ns	C_{card} <= 10 pF(1 card)

Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	14	ns	C_L <= 40 pF(1 card)

Table 3-2: Bus Timing - Parameters Values (High Speed Mode)

Default Bus Timing(Backward Compatible):

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{card} <= 10 pF(1 card)
Clock frequency Identification Mode	f_{OD}	0	400	KHz	C_{card} <= 10 pF(1 card)
Clock low time	t_{WL}	10	-	ns	C_{card} <= 10 pF(1 card)
Clock high time	t_{WH}	10	-	ns	C_{card} <= 10 pF(1 card)
Clock rise time	t_{TLH}	-	10	ns	C_{card} <= 10 pF(1 card)
Clock fall time	t_{THL}	-	10	ns	C_{card} <= 10 pF(1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5	-	ns	C_{card} <= 10 pF(1 card)
Input hold time	t_{IH}	5	-	ns	C_{card} <= 10 pF(1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	14	ns	C_L <= 40 pF(1 card)

Comment [Leo1]: 100K 最低是否要求

Table 3-3: Bus Timing - Parameters Values (Default)

(1) 0Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

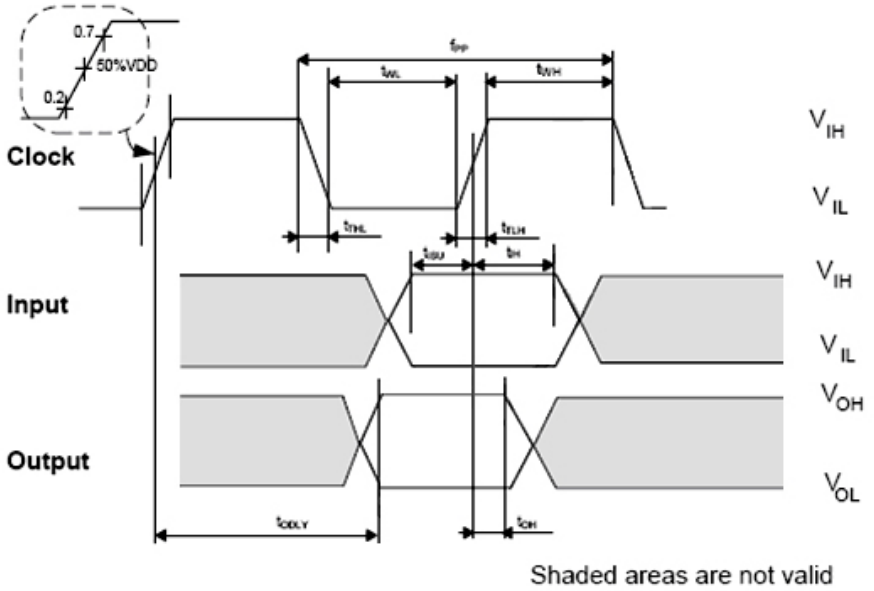


Figure 3-3: Timing diagram data input/output referenced to clock (High-Speed)

PARAMETER	SYMBOL	MIN	MAX	UNIT	REMARK
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL}),					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	
Clock low time	t_{WL}	7		ns	
Clock high time	t_{WH}	7		ns	
Clock rise time	t_{TLH}		3	ns	
Clock fall time	t_{THL}		3	ns	
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	
Input hold time	t_{IH}	2		ns	
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	
Output Hold time	t_{OH}	2.5		ns	
Total System capacitance for each line	C_L		40	pF	

Comment [Leo2]: 是否要求 100K 最低?

Table 3-3: Bus Timing - Parameters Values (High-Speed)

4 SD Card Hardware System

4.1 SD Card Description

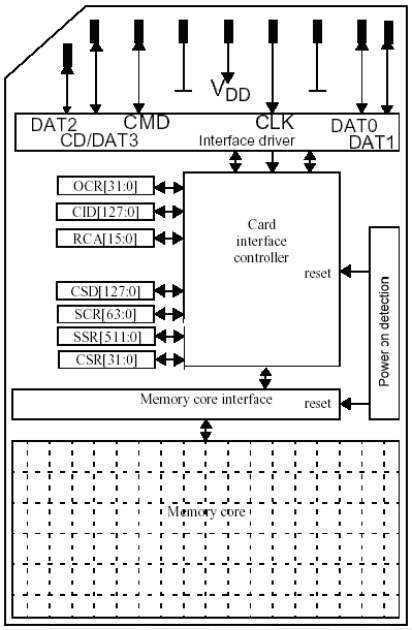


Figure 4-1: SD Card Function Block Diagram

PIN #	SD INTERFACE			SPI INTERFACE		
	NAME	TYPE	DESCRIPTION	NAME	TYPE	DESCRIPTION
1	CD/ DAT3[2]	I/O/PP	Card Detect /Data Line (Bit 3)	CS	I	Chip Select (Active Low)
2	CMD	PP	Command/ Response	DI	I/PP	Data In
3	VSS[1]	S	Supply Voltage Ground	VSS	S	Supply Voltage Ground
4	VDD	S	Supply Voltage	VDD	S	Supply Voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS[2]	S	Supply Voltage Ground	VSS[2]	S	Supply Voltage Ground
7	DAT0	I/O/PP	Data Line (Bit 0)	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line (Bit 1)	RSV		
9	DAT2	I/O/PP	Data Line (Bit 2)	RSV		

Table 4-1: Pad Assignment

1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;
2) The extended DAT Lines (Dat1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
3) After power up this line is input with 50Kohm pull-up (can be used for card detection or SPD mode selection). The pull-up should be disconnected by user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command

Each card has a set of information registers. Please refer to chapter 5 for the details of registers.

NAME	WIDT	DESCRIPTION
CID	128	Card identification number; card individual number for identification.
RCA	16	Relative card address; local system address of a card, dynamically suggested by the card and approved by the host during initialization.
CSD	128	Card Specific Data; information about the card operation conditions.
SCR	64	SD Configuration Register; information about the SD Card's Special Features capabilities.
OCR	32	Operation conditions register.
SSR	512	SD Status; information about the card proprietary features.
CSR	32	Card Status; information about the card status.

Table 4-2: SD Card registers

4.2 SD BUS Topology

The SD Card bus has a single master (application), multiple slaves (cards), synchronous star topology. Clock, power and ground signals are common to all cards. Command (CMD) and data (DAT0 - DAT3) signals are dedicated to each card providing continues point to point connection to all the cards.
During initialization process commands are sent to each card individually, allowing the application to detect the cards and assign logical addresses to the physical slots. Data is always sent (received) to (from) each card individually. However, in order to simply the handling of the card stack, after the initialization process, all commands may be sent concurrently to all cards. Addressing information is provided in the command packet.
SD bus allows dynamic configuration of the number of data lines. After power up, by default, the SD Card will use only DAT0 for data transfer. After initialization the host can change the bus width (number of active data lines). This feature allows easy trade off between HW cost and system performance.
Note that while DAT1-DAT3 are not in use, the related Host's DAT lines should be in tri-state (input mode).

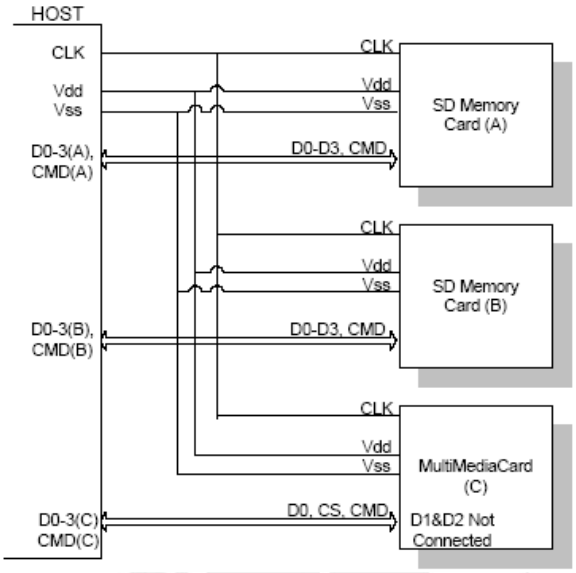


Figure 4-2: SD Card system bus Topology

4.3 SD Card Hardware Interface

The SD Card has six communication lines and three supply lines:

- CMD: Command is a bidirectional signal. The host and card drivers are operating in push pull mode.
- DAT0-3: Data lines are bidirectional signals. Host and card drivers are operating in push pull mode
- CLK: Clock is a host to card signal. CLK operates in push pull mode
- VDD: VDD is the power supply line for all cards.
- VSS1, VSS2 are two ground lines.

In addition to those lines that are connected to the internal card circuitry there are two contacts of the Write Protect/Card Detect switch that are part of the socket. Those contacts are not mandatory but if they exist they should be connected as given in the following figure. When DAT3 is used for card detection, R_{DAT} for DAT3 should be unconnected and another resistor should be connected to the ground.

R_{DAT} and R_{CMD} are pull-up resistors protecting the CMD and the DAT lines against bus floating when no card is inserted or when all card drivers are in a high-impedance mode. The host shall pull-up all DAT0-3 lines by RDAT, even if the host uses SD Card as 1 bit mode- only in SD mode. Also, the host shall pull-up all "RSV" lines in SPI mode, even though they are not used. R_{WP} is used for the Write Protect/Card Detection switch.

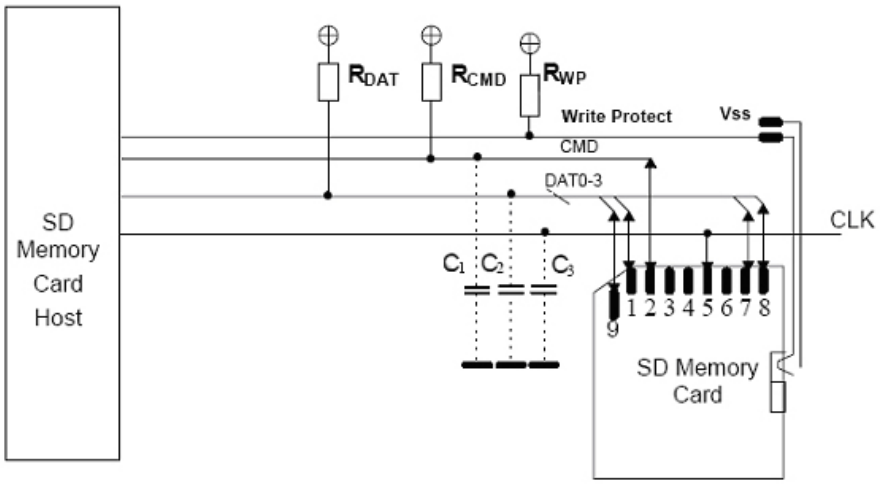


Figure 4-3: Bus circuitry diagram

4.4 Bus Signal Line Load

The total capacitance CL of each line of the SD bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance CBUS itself and the capacitance C_{CARD} of each card connected to this line:
$C_L = C_{HOST} + C_{BUS} + N*C_{CARD}$
N is the number of connected cards.

PARAMETER	SYMBOL	MIN	MAX.	UNIT	REMARK
Pull-up resistance for CMD	R_{CMD}	10	100	Kohm	to prevent bus floating
Pull-up resistance for DAT	R_{DAT}	10	100	Kohm	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card CHOST+CBUS shall not exceed 30 pF
Single card capacitance	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	f_{PP} <= 20 MHz
Pull-up resistance inside card (pin1)	RDAT3	10	90	Kohm	May be used for card detection

Table 4-3: Bus Signal Line Load

4.5 Hot Insertion and Removal

To guarantee the proper sequence of card pin connection during hot insertion, the use of either a special hot-insertion capable card connector or an auto-detect loop on the host side (or some similar mechanism) is mandatory. No card shall be damaged by inserting or removing a card into the SD Card bus even when the power (VDD) is up. Data transfer operations are protected by CRC codes, therefore any bit changes induced by card insertion and removal can be detected by the SD Card bus master. The inserted card must be properly reset also when CLK carries a clock frequency f_{PP}. Each card shall have power protection to prevent card (and host) damage. Data transfer failures induced by removal/insertion are detected by the bus master. They must be corrected by the application, which may repeat the issued command.

4.6 Power up

The power up of the SD Card bus is handled locally in each SD Card and in the bus master.

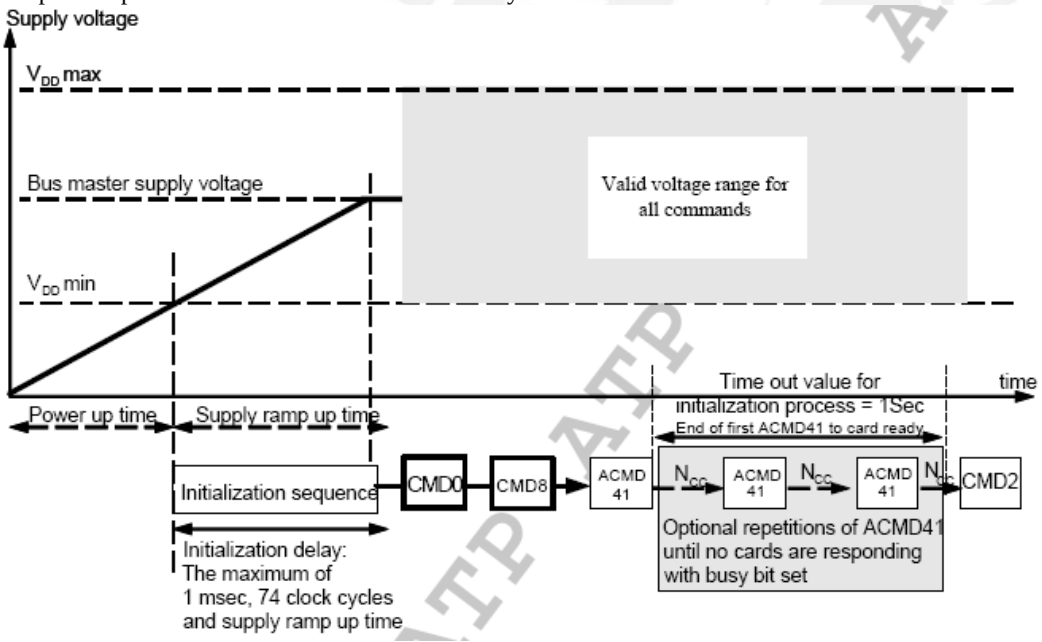


Figure 4-4: Power-up diagram

• 'Power up time' is defined as voltage rising time from 0 volt to VDD min and depends on application parameters such as the maximum number of SD Cards, the bus length and the characteristic of the

power supply unit.

• 'Supply ramp up time' provides the time that the power is built up to the operating level (the bus master supply voltage) and the time to wait until the SD card can accept the first command.

• The host shall supply power to the card so that the voltage is reached to Vdd_min within 250ms and start to supply at least 74 SD clocks to the SD card with keeping CMD line to high. In case of SPI mode, CS shall be held to high during 74 clock cycles.

• After power up (including hot insertion, i.e. inserting a card when the bus is operating) the SD Card enters the *idle state*. In case of SD host, CMD0 is not necessary. In case of SPI host, CMD0 shall be the first command to send the card to SPI mode.

• CMD8 is newly added in the Physical Layer Specification Version 2.00 to support multiple voltage ranges and used to check whether the card supports supplied voltage. The version 2.00 host shall issue CMD8 and verify voltage before card initialization. The host that does not support CMD8 shall supply high voltage range.

• ACMD41 is a synchronization command used to negotiate the operation voltage range and to poll the cards until they are out of their power-up sequence. In case the host system connects multiple cards, the host shall check that all cards satisfy the supplied voltage. Otherwise, the host should select one of the cards and initialize.

4.7 Compatibility to Multi Media Card

The SD Card protocol is designed to be a super-set of the Multi Media Card Version 2.11 protocol. For complete details refer to Multi Media Card specification.

4.8 Card Capacity

• Standard Capacity SD Memory Cards supports capacity up to and including 2 G bytes (231 bytes). All versions of the Physical Specifications define the Standard Capacity SD Memory Card.
• High Capacity SD Memory Cards supports capacity more than 2 G bytes (231 bytes) and this version of specification limits capacity up to and including 32 GB. High Capacity SD Memory Card is newly defined from the Physical Layer Specification Version 2.00. Only hosts that are compliant to the Physical Layer Specification version 2.00 or higher and the SD File System Specification Ver2.00 can access High Capacity SD Memory Cards. Other hosts fail to initialize High Capacity SD Memory Cards.

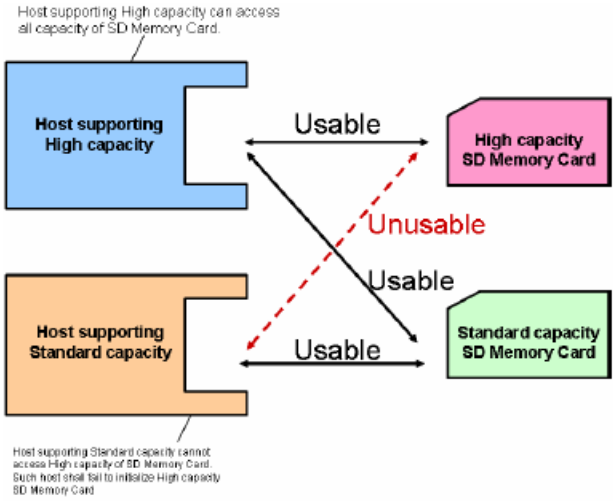


Figure 4-5: Hosts-Cards Usability

5 Card Registers

Within the card interface seven registers are defined: OCR, CID, CSD, RCA, SCR, SSR and CSR. These can be accessed only by corresponding commands. The OCR, CID, CSD and SCR registers carry the card/content specific information, while the RCA register is configuration register storing actual configuration parameters and SSR and CSR are two status fields.

5.1 OCR Register

The 32-bit operation conditions register stores the VDD voltage profile of the card. In addition, this register includes a status information bit. This status bit is set if the card power up procedure has been finished.

OCR BIT POSITION	VDD VOLTAGE WINDOW
0-6	reserved
7	1.7-1.95
8-14	2.0-2.6
15	2.7-2.8
16	2.8-2.9
17	2.9-3.0
18	3.0-3.1
19	3.1-3.2
20	3.2-3.3
21	3.3-3.4
22	3.4-3.5
23	3.5-3.6
24-29	reserved
30	Card Capacity Status [1]
31	card power up status bit [2]

1) This bit is valid only when the card power up status bit is set.
2) This bit is set to LOW if the card has not finished the power up routine

Table 5-1: OCR register definition

The supported voltage range is coded as shown in Table 5-1. A voltage range is not supported if the corresponding bit value is set to LOW. As long as the card is busy, the corresponding bit (31) is set to LOW.

5.2 CID Register

The Card IDentification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification

number. The structure of the CID register is defined in the following paragraphs:

NAME	FIELD	WIDTH	CID-SLICE
Manufacturer ID	MID	8	[127:120]
OEM/Application ID	OID	16	[119:104]
Product name	PNM	40	[103:64]
Product revision	PRV	8	[63:56]
Product serial number	PSN	32	[55:24]
reserved	--	4	[23:20]
Manufacturing date	MDT	12	[19:8]
CRC7 checksum	CRC	7	[7:1]
not used, always '1'	-	1	[0:0]

Table 5-2: The CID fields

Comment [Leo3]: 是否要介绍 ATP 的 CID 设置

• MID

An 8 bit binary number identifies the card manufacturer. The MID number is controlled, defined and allocated to a SD Card manufacturer by the SD Group. This procedure is established to ensure uniqueness of the CID register.

• OID

A 2 ASCII string characters that identifies the card OEM and/or the card contents (when used as a distribution media either on ROM or FLASH cards). The OID number is controlled, defined and allocated to a SD Card manufacturer by the SD Group. This procedure is established to ensure uniqueness of the CID register.

• PNM

The product name is a string, 5 ASCII characters long.

• PRV

The product revision is composed of two Binary Coded Decimal (BCD) digits, four bits each, representing an "n.m" revision number. The "n" is the most significant nibble and "m" is the least significant nibble. As an example, the PRV binary value field for product revision "6.2" will be: 0110 0010

• PSN

The Serial Number is 32 bits of binary number.

• MDT

The manufacturing date composed of two hexadecimal digits, one is 8 bit representing the year(y) and the other is four bits representing the month(m). The "m" field [11:8] is the month code. 1 = January.

The "y" field [19:12] is the year code. 0 = 2000. As an example, the binary value of the Date field for

production date “April 2001” will be: 00000001 0100.

• CRC

CRC7 checksum (7 bits). This is the checksum of the CID contents.

5.3 CSD Register

The Card-Specific Data register provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be hanged by CMD27. The type of the entries in the table below is coded as follows: R = readable, W(1) = writable once, W = multiple writable.

NAME	FIELD	WIDTH	CELL TYPE	CSD-SLICE
CSD structure	CSD_STRUCTURE	2	R	[127:126]
reserved	-	6	R	[125:120]
data read access-time-1	TAAC	8	R	[119:112]
data read access-time-2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]
max. data transfer rate	TRAN_SPEED	8	R	[103:96]
card command classes	CCC	12	R	[95:84]
max. read data block length	READ_BL_LEN	4	R	[83:80]
partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]
write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]
read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]
DSR implemented	DSR_IMP	1	R	[76:76]
reserved	-	6	R	[75:70]
device size	C_SIZE	22	R	[69:48]
reserved	-	1	R	[47:47]
erase single block enable	ERASE_BLK_EN	1	R	[46:46]
erase sector size	SECTOR_SIZE	7	R	[45:39]
write protect group size	WP_GRP_SIZE	7	R	[38:32]
write protect group enable	WP_GRP_ENABLE	1	R	[31:31]
reserved		2	R	[30:29]
write speed factor	R2W_FACTOR	3	R	[28:26]
max. write data block length	WRITE_BL_LEN	4	R	[25:22]
partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]
reserved	-	5	R	[20:16]

File format group	FILE_FORMAT_GRP	1	R	[15:15]
copy flag (OTP)	COPY	1	R/W(1)	[14:14]
permanent write protection	PERM_WRITE_PROTECT	1	R/W(1)	[13:13]
temporary write protection	TMP_WRITE_PROTECT	1	R/W	[12:12]
File format	FILE_FORMAT	2	R	[11:10]
reserved	-	2	R	[9:8]
CRC	CRC	7	R/W	[7:1]
not used, always'1'	-	1	-	[0:0]

Table 5-3: The CSD Register fields

The following sections describe the CSD fields and the relevant data types. If not explicitly defined otherwise, all bit strings are interpreted as binary coded numbers starting with the left bit first.

• CSD_STRUCTURE

Version number of the related CSD structure

CSD_STRUCTURE	CSD STRUCTURE VERSION	VALID FOR SD CARD PHYSICAL SPECIFICATION VERSION
0	CSD version 1.0	Version 1.0-1.10 Version 2.00/Standard Capacity
1	CSD version 2.0	Version 2.00 /High Capacity
2-3	reserved	

Table 5-4: CSD register structure

• TAAC

Defines the asynchronous part of the data access time.

TAAC BIT POSITION	CODE
2:0	time unit
	0=1ns, 1=10ns, 2=100ns, 3=1µs, 4=10µs, 5=100µs, 6=1ms, 7=10ms
6:3	time value
	0=reserved, 1=1.0, 2=1.2, 3=1.3, 4=1.5, 5=2.0, 6=2.5, 7=3.0, 8=3.5, 9=4.0, A=4.5, B=5.0, C=5.5, D=6.0, E=7.0, F=8.0

7	reserved

Table 5-5: TAAC access time definition

• NSAC

Defines the worst case for the clock dependent factor of the data access time. The unit for NSAC is 100 clock cycles. Therefore, the maximal value for the clock dependent part of the data access time is 25.5k clock cycles. The total access time NAC is the sum of TAAC and NSAC. It has to be computed by the host for the actual clock rate. The read access time should be interpreted as a typical delay for the first data bit of a data block or stream.

• TRAN_SPEED

The following table defines the maximum data transfer rate per one data line - TRAN_SPEED:

TRAN_SPEED BIT	CODE
2:0	transfer rate unit
	0=100kbit/s, 1=1Mbit/s, 2=10Mbit/s,
	3=100Mbit/s, 4... 7=reserved
6:3	time value
	0=reserved, 1=1.0, 2=1.2, 3=1.3, 4=1.5, 5=2.0, 6=2.5, 7=3.0, 8=3.5, 9=4.0, A=4.5, B=5.0, C=5.5, D=6.0, E=7.0, F=8.0
7	reserved

Table 5-6: Maximum data transfer rate definition

Note that for current SD Cards that field is always 0_0110_010b (032h) which is equal to 25MHz - the mandatory maximum operating frequency of SD Card. In High-Speed mode, that field is always 0_1011_010b (05Ah) which is equal to 50MHz. And when the timing mode returns to the default by CMD6 or CMD0 command, its value will be 032h.

• CCC

The SD Card command set is divided into subsets (command classes). The card command class register CCC defines which command classes are supported by this card. A value of '1' in a CCC bit means that the corresponding command class is supported.

CCC BIT	SUPPORTED CARD COMMAND CLASS
0	class 0
1	class 1
.....	
11	class 11

Table 5-7: Supported card command classes

• READ_BL_LEN

The maximum read data block length is computed as $2^{READ\_BL\_LEN}$. The maximum block length might therefore be in the range 512...2048 bytes. Note that in SD Card the WRITE_BL_LEN is always equal to READ_BL_LEN

READ_BL_LEN	BLOCK LENGTH	REMARK
0-8	reserved	
9	2^9 = 512 Bytes	
.....		
11	2^{11} = 2048 Bytes	
12-15	reserved	

Table 5-8: Data block length

• READ_BL_PARTIAL (always = 1 in SD Card)

Partial Block Read is always allowed in SD Card. It means that smaller blocks can be used as well. The minimum block size will be one byte.

• WRITE_BLK_MISALIGN

Defines if the data block to be written by one command can be spread over more than one physical block of the memory device. The size of the memory block is defined in WRITE_BL_LEN.

WRITE_BLK_MISALIGN=0 signals that crossing physical block boundaries is invalid.

WRITE_BLK_MISALIGN=1 signals that crossing physical block boundaries is allowed.

• READ_BLK_MISALIGN

Defines if the data block to be read by one command can be spread over more than one physical

block of the memory device. The size of the memory block is defined in READ_BL_LEN.

READ_BLK_MISALIGN=0 signals that crossing physical block boundaries is invalid.

READ_BLK_MISALIGN=1 signals that crossing physical block boundaries is allowed.

• DSR_IMP

Defines if the configurable driver stage is integrated on the card. If set, a driver stage register (DSR)

must be implemented also.

• C_SIZE

This field is expanded to 22 bits and can indicate up to 2 TBytes (It is the same as the maximum memory space specified by a 32-bit block address.)

This parameter is used to calculate the user data area capacity in the SD memory card (not include the protected area). The user data area capacity is calculated from C_SIZE as follows:

memory capacity = (C_SIZE+1) * 512K byte

As the maximum capacity of the Physical Layer Specification Version 2.00 is 32 GB, the upper 6 bits of his field shall be set to 0.

• ERASE_BLK_EN

This field is fixed to 1, which means the host can erase one or multiple units of 512 bytes.

• SECTOR_SIZE

This field is fixed to 7Fh, which indicates 64 KBytes. This value does not relate to erase operation. Version 2.00 cards indicates memory boundary by AU size and this field should not be used.

• WP_GRP_SIZE

This field is fixed to 00h. The High Capacity SD Memory Card does not support write protected groups.

• WP_GRP_ENABLE

This field is fixed to 00h. The High Capacity SD Memory Card does not support write protected groups.

• R2W_FACTOR

This field is fixed to 2h, which indicates 4 multiples. Write timeout can be calculated by multiplying the read access time and R2W_FACTOR. However, the host should not use this factor and should use 250 ms for write timeout.

• WRITE_BL_LEN

This field is fixed to 9h, which indicates WRITE_BL_LEN=512 Byte.

• WRITE_BL_PARTIAL

This field is fixed to 0, which indicates partial block read is inhibited and only unit of block access is allowed.

• FILE_FORMAT_GRP

This field is set to 0. Host should not use this field.

.

• COPY
Defines if the contents is original (= ‘0’) or has been copied (=’1’). The COPY bit for OTP and MTP devices, sold to end consumers, is set to ‘1’ which identifies the card contents as a copy. The COPY bit is an one time programmable bit.

• PERM_WRITE_PROTECT
Permanently protects the whole card content against overwriting or erasing (all write and erase commands for this card are permanently disabled). The default value is ‘0’, i.e. not permanently write protected.

• TMP_WRITE_PROTECT

Temporarily protects the whole card content from being overwritten or erased (all write and erase commands for this card are temporarily disabled). This bit can be set and reset. The default value is ‘0’, i.e. not write protected.

• FILE_FORMAT
This field is set to 0.

• CRC

The CRC field carries the check sum for the CSD contents. The checksum has to be recalculated by the host for any CSD modification. The default corresponds to the initial CSD contents.

5.4 RCA Register

The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0000. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7.

5.5 SCR Register

In addition to the CSD register there is another configuration register that named - SD CARD Configuration Register (SCR). SCR provides information on SD Card's special features that were configured into the given card. The size of SCR register is 64 bit. This register is set in the factory by ATP.

The following table describes the SCR register content.

DESCRIPTION	FIELD	WIDTH	CELL TYP	SCR SLICE
SCR Structure	SCR_STRUCTURE	4	R	[63:60]
SD Card - Spec. Version	SD_SPEC	4	R	[59:56]
data_status_after erases	DATA_STAT_AFTER_ERASE	1	R	[55:55]
SD Security Support	SD_SECURITY	3	R	[54:52]
DAT Bus widths supported	SD_BUS_WIDTHS	4	R	[51:48]
reserved	-	16	R	[47:32]
reserved for manufacturer usage	-	32	R	[31:0]

Table 5-16: The SCR Fields

• SCR_STRUCTURE

Version number of the related SCR structure in the SD Card Physical Layer Specification.

SCR_STRUCTURE	SCR STRUCTURE VERSION	VALID FOR SD PHYSICAL LAYER SPECIFICATION VERSION
0	SCR version No. 1.0	Version 1.01-2.00
1-15	reserved	

Table 5-9: SCR register structure version

• SD_SPEC

Describes the SD Card Physical Layer Specification version supported by this card.

SD_SPEC	PHYSICAL LAYER SPECIFICATION VERSION NUMBER
0	Version 1.0-1.01
1	Version 1.10
2	Version 2.00
3-15	reserved

Table 5-10: SD Card Physical Layer Specification Version

• DATA_STAT_AFTER_ERASE

Defines the data status after erase, whether it is '0' or '1'.

• SD_SECURITY

Describes the security algorithm supported by the card.

SD_SECURITY	SUPPORTED ALGORITHM
0	no security
1	Not used
2	Version 1.01
3	Version 2.0
4-7	reserved

Table 5-11: SD Supported security algorithm

• SD_BUS_WIDTHS

Describes all the DAT bus widths that are supported by this card.

SD_BUS_WIDTHS	SUPPORTED BUS WIDTHS
Bit 0	1 bit (DAT0)
Bit 1	reserved
Bit 2	4 bit (DAT0-3)
Bit 3 [MSB]	reserved

Table 5-12: SD Card Supported Bus Widths

5.6 SSR Register

SD Status; information about the card proprietary features (See 6.5)

5.7 CSR Register

Card Status; information about the card status (See 6.5).

6 SD Card Functional Description

6.1 SD BUS Protocol

Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

• **Command**: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.

• **Response**: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.

• **Data**: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

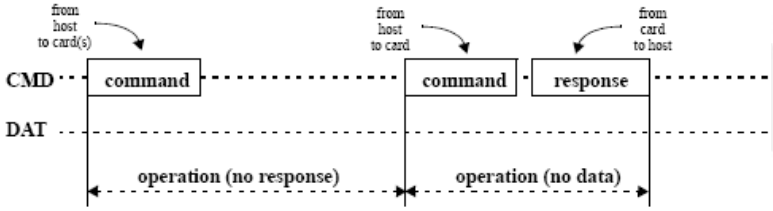


Figure 6-1: “no response” And “no data” Operations

Card addressing is implemented using a session address, assigned to the card during the initialization phase. The basic transaction on the SD bus is the command/response transaction. This type of bus transactions transfers their information directly within the command or response structure. In addition, some operations have a data token.

Data transfers to/from the SD Card are done in blocks. Data blocks always were succeeded by CRC bits. Single and multiple block operations are defined. Note that the Multiple Block operation mode is better for faster write operation. A multiple block transmission is terminated when a stop command follows on the CMD line. Data transfer can be configured by the host to use single or multiple data lines.

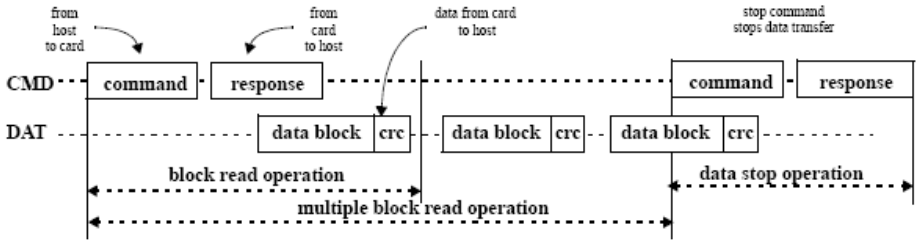


Figure 6-2: (Multiple) Block Read Operation

The block write operation uses a simple busy signaling of the write operation duration on the DAT0 data line regardless of the number of data lines used for transferring the data

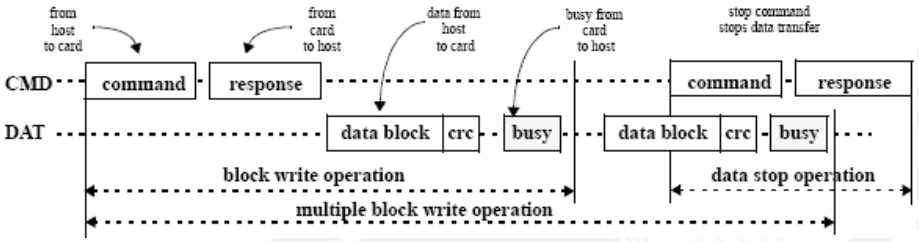


Figure 6-3: (Multiple) Block Write Operation

Command tokens have the following coding scheme:

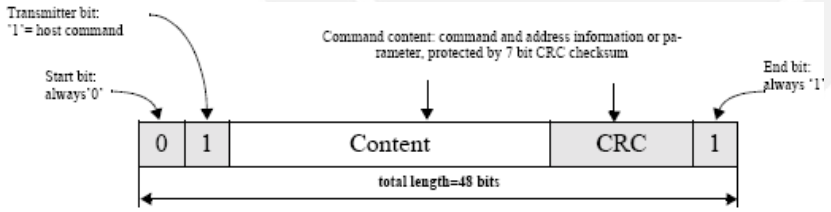


Figure 6-4: Command Token Format

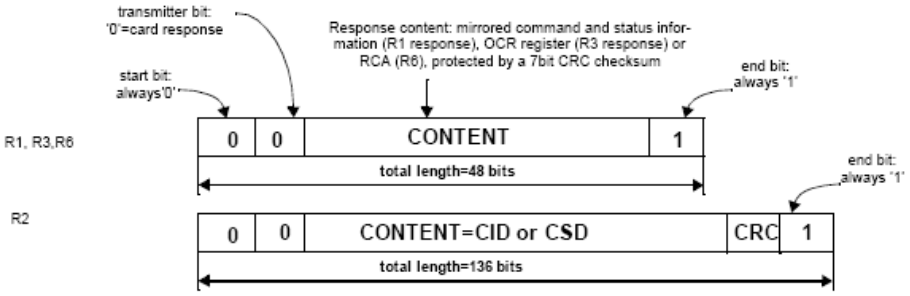


Figure 6-5: Response Token Format

In the CMD line the MSB bit is transmitted first the LSB bit is the last. When the wide bus option is used, the data is transferred 4 bits at a time. Start and end bits, as well as the CRC bits, are transmitted for every one of the DAT lines. CRC bits are calculated and checked for every DAT line individually. The CRC status response and Busy indication will be sent by the card to the host on DAT0 only (DAT1-DAT3 during that period are don't care).
There are two types of Data packet format for the SD card.
(1) Usual data (8 bit width) The usual data (8 bit width) are sent in LSB (Least Significant Byte) first, MSB (Most Significant Byte) last manner. But in the individual byte it is MSB (Most Significant Bit) first, LSB (Least Significant Bit) last.

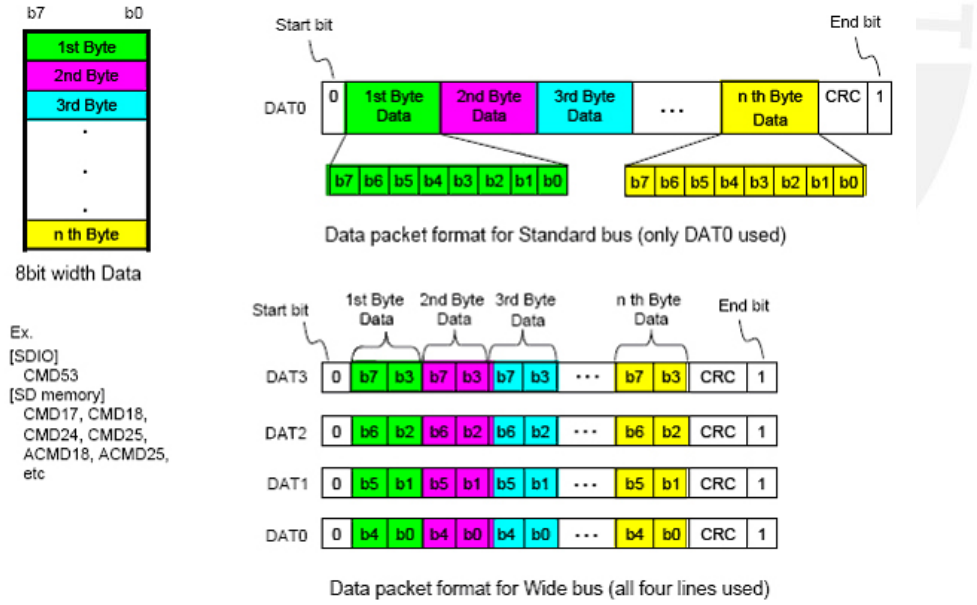


Figure 6-6: Data packet format - Usual data

(2) Wide width data (SD Memory Register) The wide width data is shifted from MSB bit.

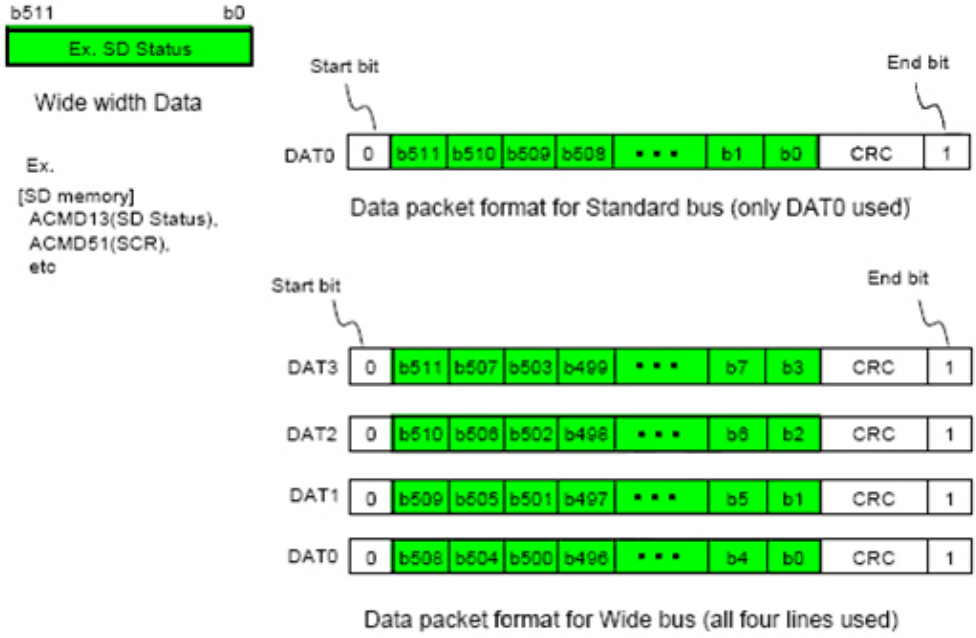


Figure 6-7: Data packet format - Wide width data

6.2 Command

6.2.1 Command Types and Format

All communication between host and cards is controlled by the host (master). The host sends commands of two types: broadcast and addressed (point-to-point) commands.

• Broadcast commands

Broadcast commands are intended for all cards. Some of these commands require a response.

• Addressed (point-to-point) commands

The addressed commands are sent to the addressed card and cause a response from this card.

• Command Format

All commands have a fixed code length of 48 bits, needing a transmission time of 2.4 μs @ 20 MHz

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'1'	x	x	x	'1'
Description	start bit	transmission bit	command index	argument	CRC7	end bit

Table 6-1: Command Format

A command always starts with a start bit (always '0'), followed by the bit indicating the direction of transmission (host = '1'). The next 6 bits indicate the index of the command, this value being interpreted as a binary coded number (between 0 and 63). Some commands need an argument (e.g. an address), which is coded by 32 bits. A value denoted by 'x' in the table above indicates this variable is dependent on the command. All commands are protected by a CRC. Every command codeword is terminated by the end bit (always '1'). All commands and their arguments are listed in Table 6-3-Table 6-11.

6.2.2 Command Classes

The command set of the SD Card system is divided into several classes (See Table 6-2). Each class supports a set of card functionalities.

Class 0, 2, 4, 5 and 8 are mandatory supported by ATP SD Cards. The other classes are optional. The supported Card Command Classes (CCC) are coded as a parameter in the card specific data (CSD) register of each card, providing the host with information on how to access the card.

Comment [Leo4]: ATP 支持?

	CARD COMMAND CLASS	0	1	2	3	4	5	6	7	8	9	10	11
SUPPORTED COMMANDS	class description	basic	reserved	block read	Reserved	block write	erase	write protection	lock card	application specific	I/O mode	switch	reserved
CMD0	Mandatory	+											
CMD2	Mandatory	+											
CMD3	Mandatory	+											
CMD4	Mandatory	+											
CMD5	Optional										+		
CMD6	Mandatory											+	
CMD7	Mandatory	+											
CMD8	Mandatory	+											

CMD9	Mandatory	+											
CMD10	Mandatory	+											
CMD12	Mandatory	+											
CMD13	Mandatory	+											
CMD15	Mandatory	+											
CMD16	Mandatory			+		+			+				
CMD17	Mandatory			+									
CMD18	Mandatory			+									
CMD24	Mandatory					+							
CMD25	Mandatory					+							
CMD27	Mandatory					+							
CMD28	Optional							+					
CMD29	Optional							+					
CMD30	Optional							+					
CMD32	Mandatory						+						
CMD33	Mandatory						+						
CMD34-37	Optional											+	
CMD38	Mandatory						+						
CMD42	Optional								+				
CMD50	Optional											+	
CMD52	Optional										+		
CMD53	Optional										+		
CMD55	Mandatory									+			
CMD56	Mandatory									+			
CMD57	Optional											+	
ACMD6	Mandatory									+			
ACMD13	Mandatory									+			
ACMD22	Mandatory									+			
ACMD23	Mandatory									+			
ACMD41	Mandatory									+			
ACMD42	Mandatory									+			
ACMD51	Mandatory									+			

Table 6-2: Card Command Classes (CCCs)

6.2.3 • Detailed Command Description

The following tables define in detail all SD Card bus commands.

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION
CMD0	bc	[31:0] stuff bits	-	GO_IDLE_STATE	resets all cards to idle state
CMD1	reserved				
CMD2	bcr	[31:0] stuff bits	R2	ALL_SEND_CID	asks any card to send the CID numbers on the CMD line (any card that is connected to the host will respond)
CMD3	bcr	[31:0] stuff bits	R6	SEND_RELATIVE_ ADDR	ask the card to publish a new relative address (RCA)
CMD5	reserved for I/O cards (refer to "SDIO Card Specification")				
CMD7	ac	[31:16] RCA [15:0] stuff bits	R1b (only from the selected card)	SELECT/DESELECT_ CARD	command toggles a card between the stand-by and transfer states or between the programming and disconnect states. In both cases the card is selected by its own relative address and gets deselected by any other address; address 0 deselects all. In case that the RCA equal 0 then the host may do one of the following: - Use other RCA number to perform card deselection. - Re-send CMD3 to change its RCA number to other than 0 and then use CMD7with RCA=0 for card de-selection.
CMD8	bcr	[31:12]reserve d bits [11:8]supply voltage(VHS) [7:0]check pattern	R7	SEND_IF_COND	Sends SD Memory Card interface condition, which includes host supply voltage information and asks the card whether card supports voltage. Reserved bits shall be set to '0'.
CMD9	ac	[31:16] RCA [15:0] stuff bits	R2	SEND_CSD	addressed card sends its card-specific data (CSD) on the CMD line.
CMD10	ac	[31:16] RCA [15:0] stuff bits	R2	SEND_CID	addressed card sends its card identification (CID) on CMD the line.
CMD11	reserved				
CMD12	ac	[31:0] stuff bits	R1b	STOP_ TRANSMISSION	forces the card to stop transmission
CMD13	ac	[31:16] RCA [15:0] stuff bits	R1	SEND_STATUS	addressed card sends its status register.
CMD14	reserved				
CMD15	ac	[31:16] RCA [15:0] stuff bits	-	GO_INACTIVE_ STATE	sets the card to inactive state in order to protect the card stack against communication breakdowns.

Table 6-3: Basic commands (class 0)

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION
CMD16	ac	[31:0] block length	R1	SET_BLOCKLEN	In the case of a Standard Capacity SD Memory Card, this command sets the block length (in bytes) for all following block commands (read, write, lock). Default block length is fixed to 512 Bytes. Set length is valid for memory access commands only if partial block read operation are allowed in CSD. In the case of a High Capacity SD Memory Card, block length set by CMD16 command does not affect the memory read and write commands. Always 512 Bytes fixed block length is used. This command is effective for LOCK_UNLOCK command. In both cases, if block length is set larger than 512Bytes, the card sets the BLOCK_LEN_ERROR bit.
CMD17	adtc	[31:0] data address	R1	READ_SINGLE_ BLOCK	In the case of a Standard Capacity SD Memory Card, this command, this command reads a block of the size selected by the SET_BLOCKLEN command[1]. In the case of a High Capacity Card, block length is fixed 512 Bytes regardless of the SET_BLOCKLEN command.
CMD18	adtc	[31:0] data address	R1	READ_MULTIPLE_BLOCK	continuously transfers data blocks from card to host until interrupted by a STOP_TRANSMISSION command.
CMD19	reserved				
...					
CMD23					

1) The data transferred must not cross a physical block boundary unless READ_BLK_MISALIGN is set in the CSD.

Table 6-2: Block oriented read commands (class 2)

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION
CMD16	ac	[31:0] block length	R1	SET_BLOCKLEN	In the case of a Standard Capacity SD Memory Card, this command sets the block length (in bytes) for all following block commands (read, write, lock). Default block length is fixed to 512 Bytes. Set length is valid for memory access commands only if partial block read operation are allowed in CSD. In the case of a High Capacity SD Memory Card, block length set by CMD16 command does not affect the memory read and write commands. Always 512 Bytes fixed block length is used. This command is effective for LOCK_UNLOCK command. In both cases, if block length is set larger than 512Bytes, the card sets the BLOCK_LEN_ERROR bit.
CMD24	adtc	[31:0] data address	R1	WRITE_BLOCK	In the case of a Standard Capacity SD Memory Card, this command writes a block of the size selected by the SET_BLOCKLEN command[1]. In the case of a High Capacity Card, block length is fixed 512 Bytes regardless of the SET_BLOCKLEN command.
CMD25	adtc	[31:0] data address	R1	WRITE_MULTIPLE_BLOCK	continuously writes blocks of data until a STOP_TRANSMISSION follows.
CMD26	Reserved For Manufacturer				
CMD27	adtc	[31:0] stuff bits	R1	PROGRAM_CSD	programming of the programmable bits of the CSD.

1) The data transferred must not cross a physical block boundary unless WRITE_BLK_MISALIGN is set in the CSD. In case that write partial blocks is not supported then the block length=default block length (given in CSD).

Table 6-4: Block oriented write commands (class 4)

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION
CMD28	ac	[31:0] data address	R1b	SET_WRITE_PROT	if the card has write protection fea-tures, this command sets the write protection bit of the addressed group. The properties of write protection are coded in the card specific data (WP_GRP_SIZE).
CMD29	ac	[31:0] data address	R1b	CLR_WRITE_PROT	if the card provides write protection features, this command clears the write protection bit of the addressed group.
CMD30	adtc	[31:0] write protect data address	R1	SEND_WRITE_PROT	if the card provides write protection features, this command asks the card to send the status of the write protection bits.[1]
CMD31	reserved				

1)32 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits are transferred in a payload format via the data line. The last (least significant) bit of the protection bits corresponds to the first addressed group. If the addresses of the last groups are outside the valid range, then the corresponding write protection bits shall be set to zero

Table 6-5: Block oriented write protection commands (class 6)

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION
CMD32	ac	[31:0] data address	R1	ERASE_WR_BLK_START	sets the address of the first write-block to be erased.
CMD33	ac	[31:0] data address	R1	ERASE_WR_BLK_END	sets the address of the last write block of the continuous range to be erased.
CMD38	ac	[31:0] stuff bits	R1b	ERASE	erases all previously selected write blocks.
CMD39	reserved				
CMD40					Non Valid in SD Card - Reserved for MultiMediaCard I/O mode
CMD41	reserved				

Table 6-6: Erase commands (class 5)

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION
CMD16	ac	[31:0] block length	R1	SET_BLOCKLEN	In the case of a Standard Capacity SD Memory Card, this command sets the block length (in bytes) for all following block commands (read, write, lock). Default block length is fixed to 512 Bytes. Set length is valid for memory access commands only if partial block read operation are allowed in CSD. In the case of a High Capacity SD Memory Card, block length set by CMD16 command does not affect the memory read and write commands. Always 512 Bytes fixed block length is used. This command is effective for LOCK_UNLOCK command. In both cases, if block length is set larger than 512Bytes, the card sets the BLOCK_LEN_ERROR bit.
CMD42	adtc	[31:0] stuff bits.	R1	LOCK_UNLOCK	Used to set/reset the password or lock/unlock the card. The size of the data block is set by the SET_BLOCK_LEN command.
CMD43-49	reserved				
CMD51	reserved				

Table 6-7: Lock card (class 7)

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION
CMD55	ac	[31:16] RCA [15:0] stuff bits	R1	APP_CMD	Indicates to the card that the next command is an application specific command rather than a standard command
CMD56	adtc	[31:1] stuff bits. [0]: RD/WR1	R1	GEN_CMD	Used either to transfer a data block to the card or to get a data block from the card for general purpose/application specific commands. In the case of a Standard Capacity SD Memory Cards, the size of the data block shall be set by the SET_BLOCK_LEN command. In the case of a High Capacity SD Memory Cards, the size of the data block is fixed to 512 byte. The host sets RD/WR=1 for reading data from the card and sets to 0 for writing data to the card.
CMD58-59	reserved				
CMD60-63	reserved for manufacturer				

1) RD/WR: “1” the host gets a block of data from the card. “0” the host sends block of data to the card. All the application specific commands (given in Table 21) are supported if Class 8 is allowed (mandatory in SD Card).

Table 6-8: Application specific commands (class 8)

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION
CMD52. CMD54	reserved for I/O mode (refer to "SDIO Card Specification")				

Table 6-9: I/O mode commands (class 9)

The following table describes all the application specific commands supported/reserved by the SD Card. All the following ACMDs shall be preceded with APP_CMD command (CMD55).

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION

ACMD6	ac	[31:2] stuff bits [1:0]bus width	R1	SET_BUS_WIDTH	Defines the data bus width ('00'=1bit or '10'=4 bits bus) to be used for data transfer. The allowed data bus widths are given in SCR register.
ACMD13	adtc	[31:0] stuff bits	R1	SD_STATUS	Send the SD Card status.
ACMD17	reserved				
ACMD18	--	--	--	--	Reserved for SD security applications1
ACMD19 to ACMD21	reserved				
ACMD22	adtc	[31:0] stuff bits	R1	SEND_NUM_WR_BLOCKS	Send the number of the written (without errors) write blocks. Responds with 32bit+CRC data block. If WRITE_BL_PARTIAL='0', the unit of ACMD22 is always 512byte.If WRITE_BL_PARTIAL='1', the unit of ACMD22 is a block length which was used when the write command was executed.
ACMD23	ac	[31:23] stuff bits [22:0]Number of blocks	R1	SET_WR_BLK_ERASE_COUNT	Set the number of write blocks to be pre-erased before writing (to be used for faster Multiple Block WR command). "1"=default (one wr block)(2).
ACMD24	reserved				
ACMD25	--	--	--	--	Reserved for SD security applications1
ACMD26	--	--	--	--	Reserved for SD security applications1
ACMD38	--	--	--	--	Reserved for SD security applications1
ACMD39 to ACMD40	reserved				
ACMD41	bcr	[31]reserved bit [30]HCS(OCR[30]) [29:24]reserved bits [23:0] VDD Voltage Window(OCR[23:0])	R3	SD_SEND_OP_COND	Asks the accessed card to send its operating condition register (OCR) content in the response on the CMD line.
ACMD42	ac	[31:1] stuff bits [0]set_cd	R1	SET_CLR_CARD_DETECT	Connect[1]/Disconnect[0] the 50KOhm pull-up resistor on CD/DAT3 (pin 1) of the card.
ACMD43	--	--	--	--	Reserved for SD security applications1

ACMD49					
ACMD51	adtc	[31:0] stuff bits	R1	SEND_SCR	Reads the SD Configuration Register (SCR).

(1) Refer to "SD Memory Card Security Specification" for detailed explanation about the SD Security Features
(2) Command STOP_TRAN (CMD12) shall be used to stop the transmission in Write Multiple Block whether the pre-erase (ACMD23) feature is used or not.

Table 6-10: Application Specific Commands used/reserved by SD Card

CMD INDEX	TYPE	ARGUMENT	RESP	ABBREVIATION	COMMAND DESCRIPTION
CMD6	adtc	[31] Mode 0:Check function 1:Switch function [30:24] reserved (All '0') [23:20] reserved for function group 6 (All '0' or 0xF) [19:16] reserved for function group 5 (All '0' or 0xF) [15:12] reserved for function group 4 (All '0' or 0xF) [11:8] reserved for function group 3 (All '0' or 0xF) [7:4] function group 2 for command system [3:0] function group 1 for access mode	R1	SWITCH_ FUNC	Checks switchable function (mode 0) and switch card function (mode 1).
CMD34 CMD35 CMD36 CMD37 CMD50 CMD57	Reserved for each command system set by switch function command (CMD6).				

Table 6-11: Switch function commands (class 10)

6.3 Card State Transition Table

Table 6-12 defines the card state transitions in dependency of the received command.

	CURRENT STATE									
	idle	**ready**	**iden**	**stby**	**tran**	**data**	**rcv**	**prg**	**dis**	**ina**
TRIGGER OF STATE CHANGE	**changes to**									
CLASS INDEPENDENT										
"Operation Complete"	-	-	-	-	-	-	-	tran	stby	-
class 0										
CMD0	idle	idle	idle	idle	idle	idle	idle	idle	idle	-
CMD2	-	ident	-	-	-	-	-	-	-	-
CMD3	-	-	stby	stby	-	-	-	-	-	-

CMD4	-	-	-	stby	-	-	-	-	-	-
CMD7, card is addressed	-	-	-	tran	-	-	-	-	prg	-
CMD7, card is not addressed	-	-	-	stby	stby	stby	-	dis	-	-
CMD8	idle	-	-	-	-	-	-	-	-	-
CMD9	-	-	-	stby	-	-	-	-	-	-
CMD10	-	-	-	stby	-	-	-	-	-	-
CMD12	-	-	-	-	-	tran	prg	-	-	-
CMD13	-	-	-	stby	tran	data	rcv	prg	dis	-
CMD15	-	-	-	ina	ina	ina	ina	ina	ina	-
class 2										
CMD16	-	-	-	-	tran	-	-	-	-	-
CMD17	-	-	-	-	data	-	-	-	-	-
CMD18	-	-	-	-	data	-	-	-	-	-
class 4										
CMD16	see class 2									
CMD24	-	-	-	-	rcv	-	-	-	-	-
CMD25	-	-	-	-	rcv	-	-	-	-	-
CMD27	-	-	-	-	rcv	-	-	-	-	-
class 6										
CMD28	-	-	-	-	prg	-	-	-	-	-
CMD29	-	-	-	-	prg	-	-	-	-	-
CMD30	-	-	-	-	data	-	-	-	-	-
class 5										
CMD32	-	-	-	-	tran	-	-	-	-	-
CMD33	-	-	-	-	tran	-	-	-	-	-
CMD38	-	-	-	-	prg	-	-	-	-	-
class 7										
CMD42	-	-	-	-	rcv	-	-	-	-	-
class 8										
CMD55	idle	-	-	stby	tran	data	rcv	prg	dis	-
CMD56; RD/WR = 0	-	-	-	-	rcv	-	-	-	-	-
CMD56; RD/WR = 1	-	-	-	-	data	-	-	-	-	-
ACMD6	-	-	-	-	tran	-	-	-	-	-
ACMD13	-	-	-	-	data	-	-	-	-	-

	CURRENT STATE									
	idle	**ready**	**ident**	**stby**	**tran**	**dat**	**rcv**	**prg**	**dis**	**ina**
ACMD22	-	-	-	-	data	-	-	-	-	-
ACMD23	-	-	-	-	tran	-	-	-	-	-
ACMD18,25,26,38, 43,44,45,46,47,48,49	Refer to “SD Card Security Specification” for explanation about the SD Security Features									
ACMD41, card VDD range compatible	ready	-	-	-	-	-	-	-	-	-
ACMD41, card is busy	idle	-	-	-	-	-	-	-	-	-
ACMD41, card VDD range not compatible	ina	-	-	-	-	-	-	-	-	-
ACMD42	-	-	-	-	tran	-	-	-	-	-
ACMD51	-	-	-	-	data	-	-	-	-	-
class 9										
CMD52-CMD54	refer to "SDIO Card Specification"									
class 10										
CMD6	-	-	-	-	data	-	-	-	-	-
CMD34-37,50,57	-	-	-	-	tran	-	-	-	-	-
class 11										
CMD41; CMD43...CMD49, CMD58-CMD59	reserved									
CMD60...CMD63	reserved for manufacturer									

Table 6-12: Card state transition table

Responses

All responses are sent via the command line CMD. The response transmission always starts with the left bit of the bit string corresponding to the response codeword. The code length depends on the response type.

A response always starts with a start bit (always '0'), followed by the bit indicating the direction of transmission (card = '0'). A value denoted by 'x' in the tables below indicates a variable entry. All responses except for the type R3 (see below) are protected by a CRC. Every command codeword is terminated by the end bit (always '1'). There are five types of responses for SD Card. Their formats are defined as follows:

• **R1** (normal response command): code length 48 bit. The bits 45:40 indicate the index of the command to be responded to, this value being interpreted as a binary coded number (between 0 and 63). The status of the card is coded in 32 bits. Note that in case that data transfer to the card is involved then a busy signal may appear on the data line after the transmission of each block of data. The host shell check for busy after data block transmission.

Bit position	47	46	[45:40]	[39:8]	[7:1]
Width (bits)	1	1	6	32	7
Value	'0'	'0'	x	x	x
Description	start bit	transmission bit	command index	card status	CRC7

Table 6-13: Response R1

• **R1b** is identical to R1 with an optional busy signal transmitted on the data line. The card may become busy after receiving these commands based on its state prior to the command reception. The Host shell check for busy at the response. Refer to Chapter 4.12.3 for detailed description and timing diagrams.

• **R2** (CID, CSD register): code length 136 bits. The contents of the CID register are sent as a response to the commands CMD2 and CMD10. The contents of the CSD register are sent as a response to CMD9. Only the bits [127...1] of the CID and CSD are transferred, the reserved bit [0] of these registers is replaced by the end bit of the response.

Bit position	135	134	[133:128]	[127:1]	0
Width (bits)	1	1	6	127	1
Value	'0'	'0'	'111111'	x	'1'
Description	start bit	transmission bit	reserved	CID or CSD register incl. internal CRC7	end bit

Table 6-14: Response R2

• **R3** (OCR register): code length 48 bits. The contents of the OCR register is sent as a response to ACMD41.

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	'111111'	x	'1111111'	'1'
Description	start bit	transmission bit	reserved	OCR register	reserved	end bit

Table 6-15: Response R3

• **R6** (Published RCA response): code length 48 bit. The bits 45:40 indicate the index of the

Bit position	47	46	[45:40]	[39:8] Argument field		[7:1]	0
Width (bits)	1	1	6	16	16	7	1
Value	'0'	'0'	x	x	x	x	'1'
Description	start bit	transmission bit	command index ('000011')	New published RCA [31:16] of the card	[15:0] card status bits: 23,22,19,12:0 (see Table 30)	CRC 7	end bit

Table 6-16: Response R6

command to be responded to - in that case it will be '000011' (together with bit 5 in the status bits it means = CMD3). The 16 MSB bits of the argument field are used for the Published RCA number.

• **R7**(Card interface condition): Code length is 48 bits. The card support voltage information is sent by the response of CMD8. Bits 19-16 indicate the voltage range that the card supports. The card that accepted the supplied voltage returns R7 response. In the response, the card echoes back both the voltage range and check pattern set in the argument.

Bit position	47	46	[45:40]	[39:20]	[19:16]	[15:8]	[7:1]	0
Width (bits)	1	1	6	20	4	8	7	1
Value	'0'	'0'	'001000'	'00000h'	x	x	x	'1'

Description	start bit	transmission bit	command index	reserved bits	voltage accepted	echo-back of check pattern	CRC 7	end bit

Table 6-17: Response R7

Table 6-18 shows the format of 'voltage accepted' in R7.

voltage accepted	Value Definition
0000b	Not Defined
0001b	2.7-3.6V
0010b	Reserved for Low Voltage Range
0100b	Reserved
1000b	Reserved
Others	Not Defined

Table 6-18: Voltage Accepted in R7

6.4 SD Card Status

SD Card supports two card status field as follows:

- '*Card Status*': compatible to the MultiMediaCard protocol.

- '*SD_Status*': Extended status field of 512bits that supports special features of the SD Card and future Application Specific features.

6.4.1 Card Status

The response format R1 contains a 32-bit field named *card status*. This field is intended to transmit the card's status information (which may be stored in a local status register) to the host. If not specified otherwise, the status entries are always related to the previous issued command. The semantics of this register is according to the CSD entry SPEC_VERS, indicating the version of the response formats (possibly used for later extensions). Table 6-19 defines the different entries of the status. The type and clear condition fields in the table are abbreviated as follows:

• Type:

E: Error bit.
S: Status bit.
R: Detected and set for the actual command response.
X: Detected and set during command execution. The host must poll the card by issuing the status command in order to read these bits.

• Clear Condition:

A: According to the card current state.
B: Always related to the previous command. Reception of a valid command will clear it (with a delay of one command).
C: Clear by read.

Bits	Identifier	Type	Value	Description	Clear Condition
31	OUT_OF_RANGE	E R X	'0'= no error '1'= error	The command's argument was out of the allowed range for this card.	C
30	ADDRESS_ERROR	E R X	'0'= no error '1'= error	A misaligned address which did not match the block length was used in the command.	C
29	BLOCK_LEN_ERROR	E R X	'0'= no error '1'= error	The transferred block length is not allowed for this card, or the number of transferred bytes does not match the block length.	C
28	ERASE_SEQ_ERROR	E R	'0'= no error '1'= error	An error in the sequence of erase commands occurred.	C
27	ERASE_PARAM	E R X	'0'= no error '1'= error	An invalid selection of write-blocks for erase occurred.	C
26	WP_VIOLATION	E R X	'0'= not protected '1'= protected	Attempt to program a write protected block.	C
25	CARD_IS_LOCKED	S X	'0' = card unlocked '1' = card locked	When set, signals that the card is locked by the host	A

Bits	Identifier	Type	Value	Description	Clear Condition
24	LOCK_UNLOCK_ FAILED	E R X	'0' = no error '1' = error	Set when a sequence or password error has been detected in lock/unlock card command.	C
23	COM_CRC_ERROR	E R	'0'= no error '1'= error	The CRC check of the previous command failed.	B
22	ILLEGAL_COMMAND	E R	'0'= no error '1'= error	Command not legal for the card state	B
21	CARD_ECC_FAILED	E R X	'0'= success '1'= failure	Card internal ECC was applied but failed to correct the data.	C
20	CC_ERROR	E R X	'0'= no error '1'= error	Internal card controller error	C
19	ERROR	E R X	'0'= no error '1'= error	A general or an unknown error occurred during the operation.	C

17, 18	reserved				
16	CSD_OVERWRITE	E R X	’0’= no error ’1’= error	can be either one of the following errors: - The read only section of the CSD does not match the card content. - An attempt to reverse the copy (set as original) or permanent WP (unprotected) bits was made.	C
15	WP_ERASE_SKIP	S X	’0’= not protected ’1’= protected	Only partial address space was erased due to existing write pro tected blocks.	C
14	CARD_ECC_DISABLED	S X	’0’= enabled 1’= disabled	The command has been executed without using the internal ECC.	A
13	ERASE_RESET	S R	’0’= cleared ’1’= set	An erase sequence was cleared before executing because an out of erase sequence command was received	C
12:9	CURRENT_STATE	S X	0 = idle 1 = ready 2 = ident 3 = stby 4 = tran 5 = data; 6 = rcv; 7 = prg 8 = dis 9-14 = reserved 15 = reserved	The state of the card when receiving the command. If the command execution causes a state change, it will be visible to the host in the response to the next command. The four bits are interpreted as a binary coded number between 0 and 15.	B
8	READY_FOR_DATA	S X	’0’= not ready ’1’= ready	corresponds to buffer empty signaling on the bus	A
7,6	reserved				
5	APP_CMD	S R	‘0’ = Disabled ‘1’ = Enabled	The card will expect ACMD, or indication that the command has been interpreted as ACMD	C
4	reserved				
3	AKE_SEQ_ERROR	E R	‘0’ = no error ‘1’ = error	Error in the sequence of authenti cation process	
2,1, 0	reserved				

Table 6-19: Card status

The following table defines for each command responded by a R1 response the affected bits in the status field. An 'x' means the error/status bit may be set in the response to the respective command.

CMD#	Response Format 1 Status bit #																					
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12 :9	8	5
3									x	x			x							x		
6	x						x		x	x	x	x	x	x	x					x		
7					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
12	x	x				x	x		x	x	x	x	x	x	x			x		x		
13	x	x			x	x	x	x	x	x	x	x	x	x	x	x	x	x		x	x	
16			x		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
17	x	x			x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
18	x	x			x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
24	x	x	x		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
25	x	x	x		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
26					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
27					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
28	x				x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
29	x				x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
30	x				x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
32	x			x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
33	x			x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
38				x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
42					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		
55					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x
56					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
ACMD 6	x				x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x
ACMD 13					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x
ACMD 22					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x
ACMD 23					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x
ACMD 42					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x
ACMD 51					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x

Table 6-18: Card status field / command - cross reference

6.4.2 SD Status

The SD Status contains status bits that are related to the SD Card proprietary features and may be used for future application specific usage. The size of the SD Status is one data block of 512bit. The content of this register is transmitted to the Host over the DAT bus along with 16 bit CRC. The SD Status is sent to the host over the DAT bus if ACMD13 is sent (CMD55 followed with CMD13). ACMD13 can be sent to a card only in '*tran_state'* (card is selected). SD Status structure is described in bellow. The same abbreviation for 'type' and 'clear condition' were used as for the Card Status above.

Bits	Identifier	Type	Value	Description	Clear Condi-tion
511: 510	DAT_BUS_WIDTH	S R	'00'= 1 (default) '01'= reserved '10'= 4 bit width '11'= reserved	Shows the currently defined data bus width that was defined by SET_BUS_WIDTH command	A
509	SECURED_MODE	S R	'0'= Not in the mode '1'= In Secured Mode	Card is in Secured Mode of operation	A
508: 496	reserved				
495: 480	SD_CARD_TYPE	SR	' 00xxh'= SD Memory Cards as defined in Physical Spec Ver1.01-2.00 ('x'=don't care). The following cards are currently defined: ' 0000'= Regular SD RD/WR Card. ' 0001'= SD ROM Card	In the future, the 8 LSBs will be used to define different variations of an SD Memory Card (Each bit will define different SD Types). The 8 MSBs will be used to define SD Cards that do not comply with current	A
479: 448	SIZE_OF_PROTECTED_AREA	SR	in units of MULT*BLOCK_LEN refer to CSD register	The actual area = (SIZE_OF_PROTECTED_AREA) * MULT * BLOCK_LEN.	A
447: 440	SPEED_CLASS	SR	Speed Class of the card (See below)	(See below)	A
439: 432	PERFORMANCE_MOVE	SR	Performance of move indicated by 1 [MB/s] step. (See below)	(See below)	A
431: 428	AU_SIZE	SR	Size of AU (See below)	(See below)	A
427:	reserved				
424					
423: 408	ERASE_SIZE	SR	Number of AUs to be erased at a time	(See below)	A
407: 402	ERASE_TIMEOUT	SR	Timeout value for erasing areas specified by UNIT_OF_ERASE_AU	(See below)	A
401: 400	ERASE_OFFSET	SR	Fixed offset value added to erase time.	(See below)	A
399:312	reserved				
311:0	reserved				

Table 6-19: SD Card Status

• SIZE_OF_PROTECTED_AREA

Setting this field differs between Standard and High Capacity Cards.
In the case of a Standard Capacity Card, the capacity of protected area is calculated as follows:
Protected Area = SIZE_OF_PROTECTED_AREA_* MULT * BLOCK_LEN.
SIZE_OF_PROTECTED_AREA is specified by the unit in MULT*BLOCK_LEN.
In the case of a High Capacity Card, the capacity of protected area is specified in this field:
Protected Area = SIZE_OF_PROTECTED_AREA
SIZE_OF_PROTECTED_AREA is specified by the unit in byte.

• SPEED_CLASS

This 8-bit field indicates the Speed Class and the value can be calculated by Pw/2.

SPEED_CLASS	Value Definition
00h	Class 0
01h	Class 2
02h	Class 4
03h	Class 6
04h – FFh	Reserved

Table 6-20: Speed Class Code Field

• PERFORMANCE_MOVE

This 8-bit field indicates Pm and the value can be set by 1 [MB/sec] step. If the card does not move used RUs, Pm should be considered as infinity. Setting to FFh means infinity. The minimum value of Pm
is defined by in Table 6-21.

PERFORMANCE_MOVE	Value Definition
00h	Not Defined
01h	1 [MB/sec]
02h	2 [MB/sec]
.....	.....
FEh	254 [MB/sec]
FFh	Infinity

Table 6-21: Performance Move Field

• AU_SIZE

This 4-bit field indicates AU Size and the value can be selected in power of 2 from 16 KB.

AU_SIZE	Value Definition
0h	Not Defined
1h	16 KB
2h	32 KB
3h	64 KB
4h	128 KB
5h	256 KB
6h	512 KB
7h	1 MB
8h	2 MB
9h	4 MB
Ah – Fh	Reserved

Table 6-22: AU_SIZE Field

The maximum AU size, depends on the card capacity, is defined in Table 6-23. The card can set any AU size between RU size and maximum AU size.

Capacity	16 MB – 64 MB	128 MB-256 MB	512 MB	1 GB – 32 GB
Maximum AU Size	512 KB	1 MB	2 MB	4 MB

Table 6-23: Maximum AU size

• ERASE_SIZE

This 16-bit field indicates NERASE. When NERASE numbers of AUs are erased, the timeout value is specified by ERASE_TIMEOUT (Refer to ERASE_TIMEOUT). The host should determine proper number of AUs to be erased in one operation so that the host can indicate progress of erase operation. If this field is set to 0, the erase timeout calculation is not supported.

ERASE_SIZE	Value Definition
0000h	Erase Time-out Calculation is not supported.
0001h	1 AU
0002	2 AU
0003	3 AU
.....	.....
FFFFh	65535 AU

Table 6-24: Erase Size Field

• ERASE_TIMEOUT

This 6-bit field indicates the TERASE and the value indicates erase timeout from offset when multiple AUs are erased as specified by ERASE_SIZE. The range of ERASE_TIMEOUT can be defined as up to 63 seconds and the card manufacturer can choose any combination of ERASE_SIZE and ERASE_TIMEOUT depending on the implementation. Once ERASE_TIMEOUT is determined, it determines the ERASE_SIZE. The host can determine timeout for any number of AU erase by the Equation (6). Refer to 4.14 for the concept of calculating erase timeout. If ERASE_SIZE field is set to 0, this field shall be set to 0.

ERASE_TIMEOUT	Value Definition
00	Erase Time-out Calculation is not supported.
01	1 [sec]
02	2 [sec]
03	3 [sec]
.....	.....
63	63 [sec]

Table 6-24: Erase Timeout Field

• ERASE_OFFSET

This 2-bit field indicates the TOFFSET and one of four values can be selected. The erase offset adjusts the line by moving in parallel on the upper side. Refer to Figure 4-33 and Equation (6) in 4.14. This field is meaningless if ERASE_SIZE and ERASE_TIMEOUT fields are set to 0.

ERASE_OFFSET	Value Definition
0h	0 [sec]
1h	1 [sec]
2h	2 [sec]
3h	3 [sec]

Table 6-25: Erase Offset Field

6.5 Card Identification Mode and Data Transfer Mode

Two operation modes are defined for the SD Card system:

• Card identification mode

The host will be in card identification mode after reset and while it is looking for new cards on the bus. Cards will be in this mode after reset until the SEND_RCA command (CMD3) is received.

• Data transfer mode

Cards will enter data transfer mode once their RCA is first published. The host will enter data transfer mode after identifying all the cards on the bus. The following table shows the dependencies between operation modes and card states. Each state in the SD Card state diagram (see Figure 6-8) is associated with one operation mode:

CARD STATE	OPERATION MODE
Inactive State	inactive
Idle State	card identification mode
Ready State	
Identification State	
Stand-by State	data transfer mode
Transfer State	
Sending-data State	
Receive-data State	
Programming State	
Disconnect State	

Table 6-26: Overview of Card States vs. Operation modes

While in card identification mode the host resets all the cards that are in card identification mode, validates operation voltage range, identifies cards and asks them to publish Relative Card Address (RCA). This operation is done to each card separately on its own CMD line. All data communication in the Card Identification Mode uses the command line (CMD) only.

6.5.1 Card Identification Mode

While in card identification mode the host resets all the cards that are in card identification mode, validates operation voltage range, identifies cards and asks them to publish Relative Card Address (RCA). This operation is done to each card separately on its own CMD line. All data communication in the Card Identification Mode uses the command line (CMD) only. During the card identification process, the card shall operate in the SD clock frequency of the identification clock rate fOD .

The command GO_IDLE_STATE (CMD0) is the software reset command and sets each card into Idle State regardless of the current card state. Cards in Inactive State are not affected by this command. After power-on by the host, all cards are in Idle State, including the cards that have been in Inactive State before. After power-on or CMD0, all cards' CMD lines are in input mode, waiting for start bit of the next command. The cards are initialized with a default relative card address (RCA=0x0000) and with a default driver stage register setting (lowest speed, highest driving current capability).

At the start of communication between the host and the card, the host may not know the card supported voltage and the card may not know whether it supports the current supplied voltage. The host issues a reset command (CMD0) with a specified voltage while assuming it may be supported by the card. To verify the voltage, a following new command (CMD8) is defined in the Physical Layer Specification Version 2.00. SEND_IF_COND (CMD8) is used to verify SD Memory Card interface operating condition. The card checks the validity of operating condition by analyzing the argument of CMD8 and the host checks the validity by analyzing the response of CMD8. The supplied voltage is indicated by VHS filed in the argument. The card assumes the voltage specified in VHS as the current supplied voltage. Only 1-bit of VHS shall be set to 1 at any given time. Both CRC and check pattern are used for the host to check validity of communication between the host and the card. If the card can operate on the supplied voltage, the response echoes back the supply voltage and the check pattern that were set in the command argument. If the card cannot operate on the supplied voltage, it returns no response and stays in idle state. It is mandatory to issue CMD8 prior to first ACMD41 for initialization of High Capacity SD Memory Card (See Figure 6-27). Receipt of CMD8 makes the cards realize that the host supports the Physical Layer Version 2.00 and the card can enable new functions. It is also mandatory for low-voltage host to send CMD8 before ACMD41. In case that a Dual Voltage Card is not receiving CMD8 the card will work as a high-voltage only card, and in this case that a low voltage host didn't send CMD8 the card will go to inactive at ACMD41. SD_SEND_OP_COND (ACMD41) is designed to provide SD Memory Card hosts with a mechanism to identify and reject cards which do not match the VDD range desired by the host. This is accomplished by the host sending the required VDD voltage window as the operand of this command. Cards which cannot perform data transfer in the specified range shall discard themselves from further bus operations and go into Inactive State. The levels in the OCR register shall be defined accordingly. Note that ACMD41 is application specific command, therefore APP_CMD (CMD55) shall always precede ACMD41. The RCA to be used for CMD55 in idle_state shall be the card's default RCA = 0x0000. After the host issues a reset command (CMD0) to reset the card, the host shall issue CMD8 prior to ACMD41 to re-initialize the SD Memory card.

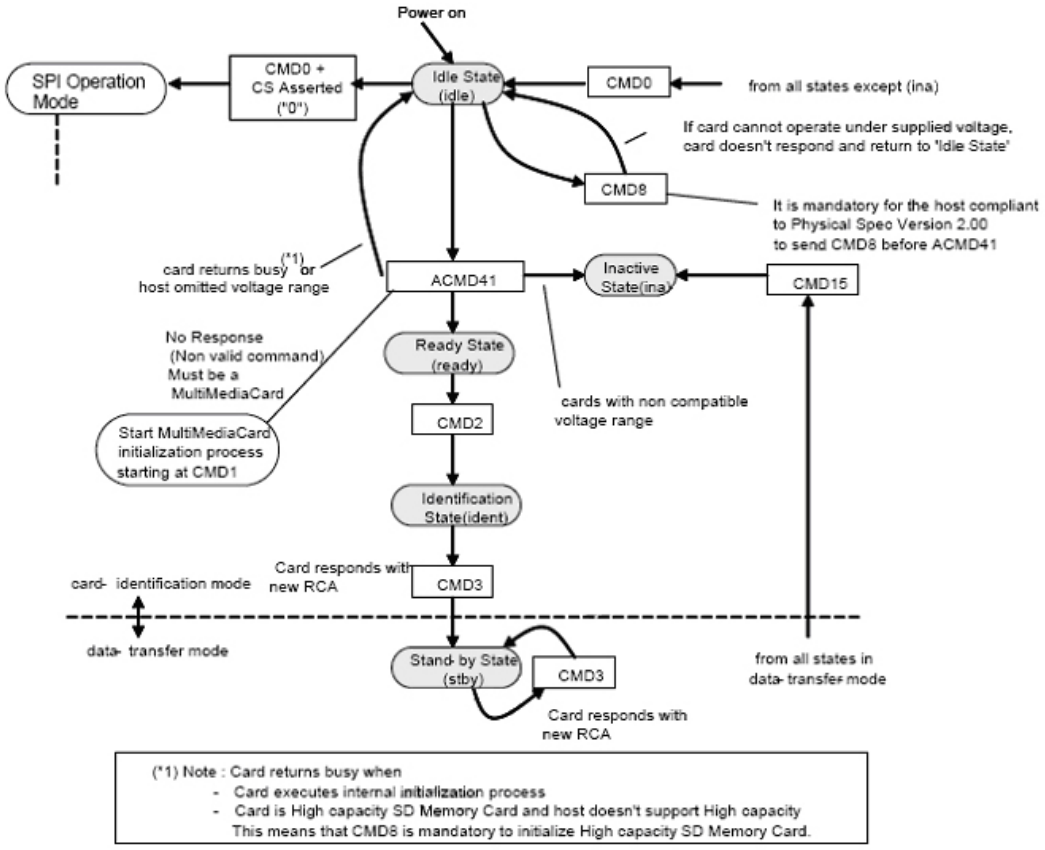


Figure 6-27: SD Card state diagram (card identification mode)

By setting the OCR to zero in the argument of ACMD41, the host can query each card and determine the common voltage range before sending out-of-range cards into the Inactive State (query mode). This query should be used if the host is able to select a common voltage range or if a notification to the application of non usable cards in the stack is desired. The card does not start initialization if ACMD41 is issued as a query. Afterwards, the host may choose a voltage for operation and reissue ACMD41 with this condition, sending incompatible cards into the Inactive State. During the initialization procedure, the host is not allowed to change the operating voltage range.

After the bus is activated the host starts card initialization and identification process (See Figure 6-28). The initialization process starts with SD_SEND_OP_COND (ACMD41) by setting its operational conditions and the HCS bit in the OCR. The HCS (Host Capacity Support) bit set to 1 indicates that the host supports High Capacity SD Memory card. The HCS (Host Capacity Support) bit set to 0 indicates that the host does not support High Capacity SD Memory card.
Receiving of CMD8 expands the ACMD41 function; HCS in the argument and CCS (Card Capacity

Status) in the response. HCS is ignored by cards, which didn't respond to CMD8. However the host should set HCS to 0 if the card returns no response to CMD8. Standard Capacity SD Memory Card ignores HCS. If HCS is set to 0, High Capacity SD Memory Card never return ready statue (keep busy bit to 0). The busy bit in the OCR is used by the card to inform the host that initialization of ACMD41 is
completed. Setting the busy bit to 0 indicates that the card is still initializing. Setting the busy bit to 1 indicates completion of initialization. The host repeatedly issues ACMD41 until the busy bit is set to 1. The card checks the operational conditions and the HCS bit in the OCR only at the first ACMD41. While
repeating ACMD41, the host shall not issue another command except CMD0.
If the card responds to CMD8, the response of ACMD41 includes the CCS field information. CCS is valid when the card returns ready (the busy bit is set to 1). CCS=1 means that the card is a High Capacity SD Memory Card.
CCS=0 means that the card is a Standard Capacity SD Memory Card.
The host performs the same initialization sequence to all of the new cards in the system. Incompatible cards are sent into Inactive State. The host then issues the command ALL_SEND_CID (CMD2), to each
card to get its unique card identification (CID) number. Card that is unidentified (i.e. which is in Ready State) sends its CID number as the response (on the CMD line). After the CID was sent by the card it goes into Identification State. Thereafter, the host issues CMD3 (SEND_RELATIVE_ADDR) asks the card to publish a new relative card address (RCA), which is shorter than CID and which is used to address the card in the future data transfer mode. Once the RCA is received the card state changes to the Stand-by State. At this point, if the host wants to assign another RCA number, it can ask the card to publish a new number by sending another CMD3 command to the card. The last published RCA is the actual RCA number of the card.
The host repeats the identification process, i.e. the cycles with CMD2 and CMD3 for each card in the system.

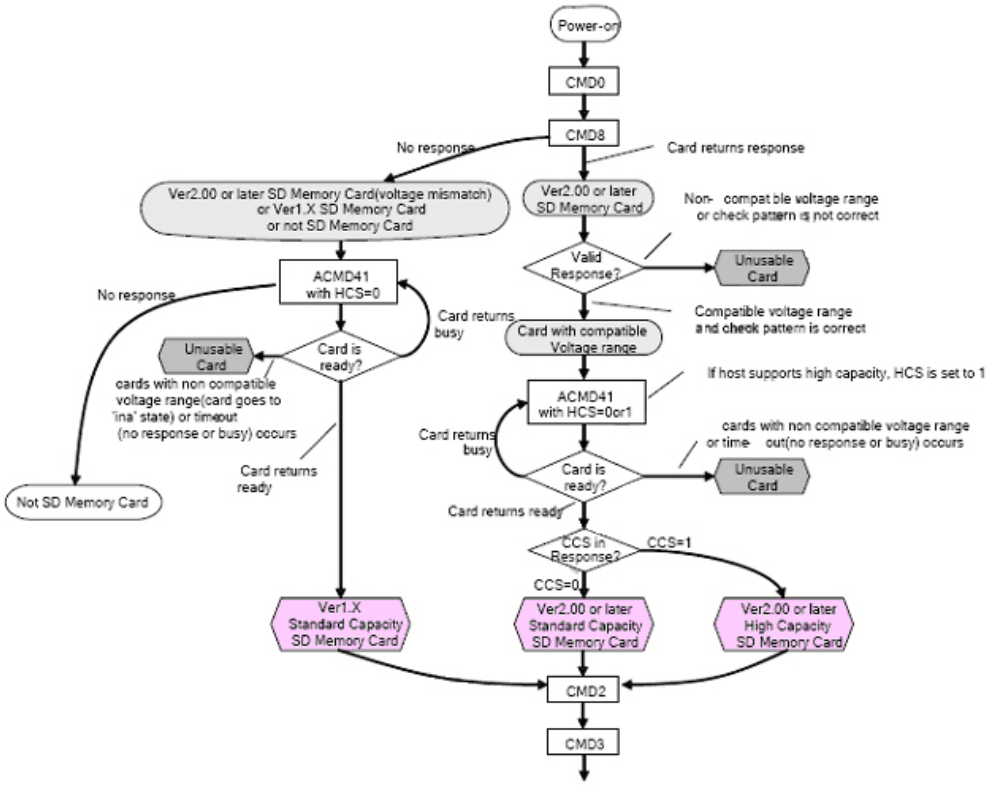


Figure 6-28: Card Initialization and Identification Flow (SD mode)

6.5.2 Data Transfer Mode

Until the end of Card Identification Mode the host must remain at f_{OD} frequency because some cards may have operating frequency restrictions during the card identification mode. In Data Transfer Mode the host may operate the card in f_{PP} frequency range. The host issues SEND_CSD (CMD9) to obtain the Card Specific Data (CSD register), e.g. block length, card storage capacity, etc.

CMD7 is used to select one card and put it into the *Transfer State*. When CMD7 is issued with the reserved relative card address "0x0000", all cards are put back to *Stand-by State* (Note that it is the responsibility of the Host to reserve the RCA=0 for card de-selection).

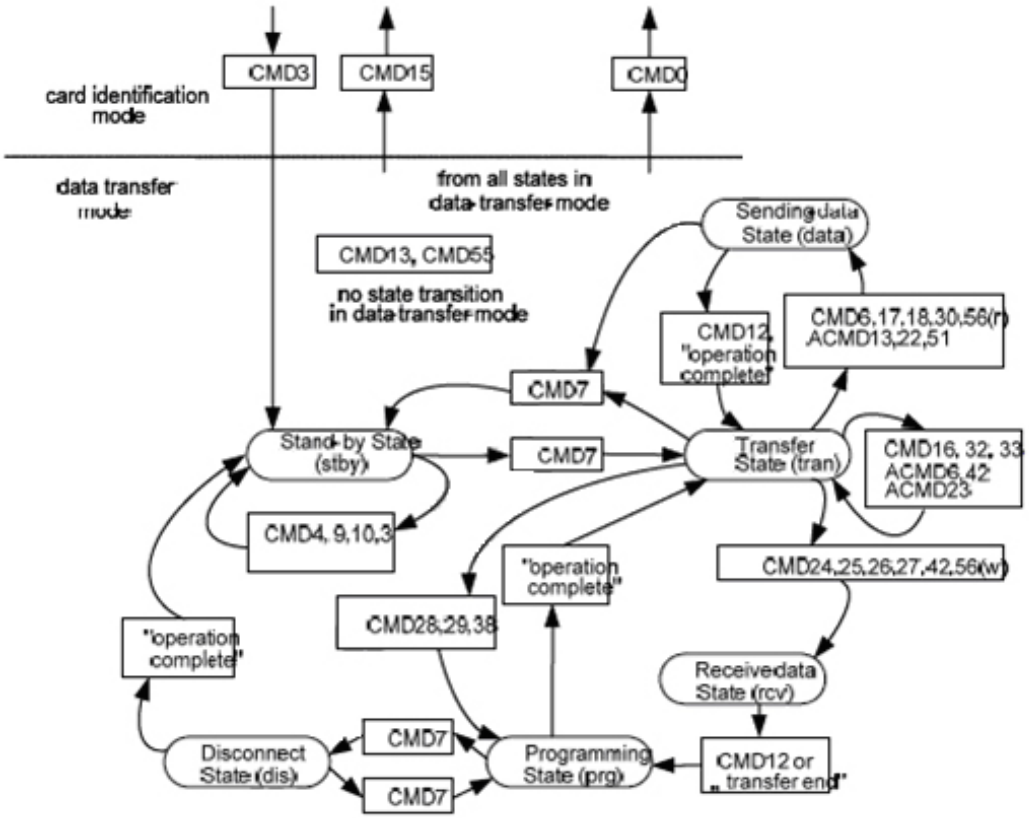


Figure 6-29: SD Card state diagram (data transfer mode)

6.6 Error Handling

To correct defects in the memory field inside card the card include error correction codes in the payload data (ECC). This correction is intended to correct static errors. Additionally two methods of detecting errors generated during the data transfer (dynamic errors) via a cyclic redundancy check (CRC) are implemented

6.6.1 Error Correction Code (ECC)

The ATP SD Card is free of static errors. All errors are covered inside the card, even errors occurring during the lifetime of the card are covered for the user. The only effect which may be notified by the end user is, that the overall memory capacity may be reduced by small number of blocks. All flash handling is done on card, so that no external error correction is needed.

6.6.2 Cyclic Redundancy Check (CRC)

The CRC is intended for protecting SD Card commands, responses and data transfer against transmission errors on the SD Card bus. One CRC is generated for every command and checked for every response on the CMD line. For data blocks one CRC per transferred block is generated. The CRC is generated and checked as described in the following.

• CRC7

The CRC7 check is used for all commands, for all responses except type R3, and for the CSD and CID registers. The CRC7 is a 7-bit value and is computed as follows:

generator polynomial: $G(x) = x^7 + x^3 + 1$.
$M(x) = (\text{first bit}) * x^n + (\text{second bit}) * x^{n-1} + ... + (\text{last bit}) * x^0$
$CRC[6...0] = \text{Remainder } [(M(x) * x^7) / G(x)]$

The first bit is the most left bit of the corresponding bitstring (of the command, response, CID or CSD). The degree n of the polynomial is the number of CRC protected bits decreased by one. The number of bits to be protected is 40 for commands and responses (n = 39), and 120 for the CSD and CID (n = 119).

• CRC16

In case of one DAT line usage (as in MultiMediaCard) than the CRC16 is used for payload protection in block transfer mode. The CRC check sum is a 16-bit value and is computed as follows:

generator polynomial $G(x) = x^{16} + x^{12} + x^5 + 1$

$M(x) = (\text{first bit}) * x^n + (\text{second bit}) * x^{n-1} + ... + (\text{last bit}) * x^0$
$CRC[15...0] = \text{Remainder } [(M(x) * x^{16}) / G(x)]$

The first bit is the first data bit of the corresponding block. The degree *n* of the polynomial denotes the number of bits of the data block decreased by one (e.g. n = 4095 for a block length of 512 bytes). The generator polynomial G(x) is a standard CCITT polynomial. The code has a minimal distance d=4 and is used for a payload length of up to 2048 Bytes (n <= 16383). The same CRC16 method is used in single DAT line mode and in wide bus mode. In wide bus mode, the CRC16 is done on each line separately.

6.6.3 CRC and Illegal Command

All commands are protected by CRC (cyclic redundancy check) bits. If the addressed card's CRC check fails, the card does not respond and the command is not executed. The card does not change its state, and COM_CRC_ERROR bit is set in the status register. Similarly, if an illegal command has been received, the card will not change its state, will not response and will set the ILLEGAL_COMMAND error bit in the status register. Only the non-errodata neous state branches are shown in the state diagrams contains a complete state transition description.

There are different kinds of illegal commands:

• Commands which belong to classes not supported by the card (e.g. write commands in read only cards).
• Commands not allowed in the current state (e.g. CMD2 in Transfer State).
• Commands which are not defined (e.g. CMD5).

6.6.4 Read, Write and Erase Time-out

The times after which a time-out condition for read operations occurs are (card independent) **either 100 times longer** than the typical access times for these operations given below **or 100ms (the lower of them)**. The times after which a time-out condition for Write/Erase operations occurs are (card independent) **either 100 times longer** than the typical program times for these operations given below **or 250ms (the lower of them).** A card shall complete the command within this time period, or give up and return an error message. If the host does not get any response with the given time out it should assume the card is not going to respond anymore and try to recover (e.g. reset the card, power cycle, reject, etc.). The typical access and program times are defined as follows:

• Read

The read access time is defined as the sum of the two times given by the CSD parameters TAAC and NSAC . These card parameters define the typical delay between the end bit of the read command and

the start bit of the data block. This number is card dependent and should be used by the host to calculate throughput and the maximal frequency for stream read.

• Write

The R2W_FACTOR field in the CSD is used to calculate the typical block program time obtained by multiplying the read access time by this factor. It applies to all write/erase commands (e.g. SET(CLR)_WRITE_PROTECT, PROGRAM_CSD and the block write commands).

• Erase

The duration of an erase command will be (order of magnitude) the number of write blocks (WRITE_BL) to be erased multiplied by the block write delay.

7 SPI Mode

7.1 Introduction

The SPI mode consists of a secondary communication protocol which is offered by SD Cards. This mode is a subset of the SD Card protocol, designed to communicate with a SPI channel, The interface is selected during the first reset command after power up (CMD0) and cannot be changed once the part is powered on.

7.2 SPI BUS Topology

The ATP SD Card SPI interface is compatible with SPI hosts available on the market. As any other SPI device the ATP SD Card SPI channel consists of the following four signals:

CS: Host to card Chip Select signal.

CLK: Host to card clock signal

DataIn: Host to card data signal.

DataOut: Card to host data signal.

Another SPI common characteristic are byte transfers, which is implemented in the card as well. All data tokens are multiples of bytes (8 bit) and always byte aligned to the CS signal.

The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal (see Figure 7-1).

The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can deassert the CS signal without affecting the programming process.

The SPI interface uses the 7 out of the SD 9 signals (DAT1 and DAT 2 are not used, DAT3 is the CS signal) of the SD bus.

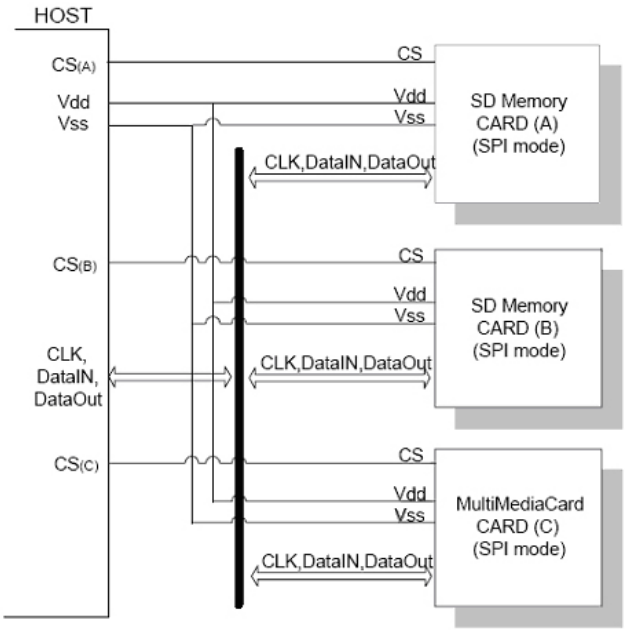


Figure 7-1: SD Card system (SPI mode) bus topology

7.3 SPI Bus Protocol

While the SD Memory Card channel is based on command and data bit streams that are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal (i.e. the length is a multiple of 8 clock cycles). The card starts to count SPI bus clock cycle at the assertion of the CS signal. Every command or data token shall be aligned to 8-clock cycle boundary. Similar to the SD Memory Card protocol, the SPI messages consist of command, response and datablock tokens. All communication between host and cards is controlled by the host (master). The host starts every bus transaction by asserting the CS signal low. The selected card always responds to the command as opposed to the SD mode. When the card encounters a data retrieval problem in a read operation, it will respond with an error response (which replaces the expected data block) rather than by a timeout as in the SD mode. Additionally, every data block sent to the card during write operations will be responded with a data response token.

In the case of a Standard Capacity Memory Card, a data block can be as big as one card write block and as small as a single byte. Partial block read/write operations are enabled by card options specified in the CSD register. In the case of a High Capacity SD Memory Card, the size of data block is fixed to 512 bytes. The block length set by CMD16 is only used for CMD42 and not used for memory data transfer. So, partial block read/write operations are also disabled. Furthermore, Write Protected commands

(CMD28, CMD29 and CMD30) are not supported.

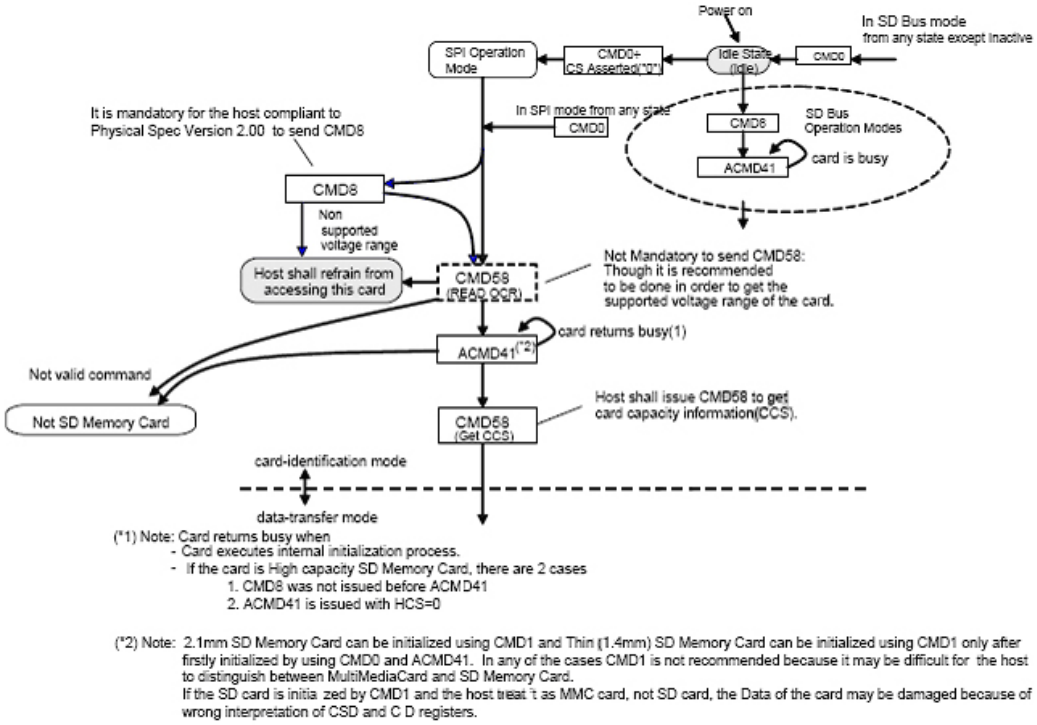


Figure 7-2: SPI Mode Initialization Flow

7.3.1 Mode Selection and Initialization

The SD Card is powered up in the SD mode. It will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0). If the card recognizes that the SD mode is required it will not respond to the command and remain in the SD mode. If SPI mode is required, the card will switch to SPI and respond with the SPI mode R1 response. The only way to return to the SD mode is by entering the power cycle. In SPI mode, the SD Card protocol state machine in SD mode is not observed. All the SD Card commands supported in SPI mode are always available. Figure 7-3 shows the initialization sequence of SPI mode. SEND_IF_COND (CMD8) is used to verify SD Memory Card interface operating condition. The argument format of CMD8 is the same as defined in SD mode and the response format of CMD8 is defined in Section 7.3.2.6. The card checks the validity of operating condition by analyzing the argument of CMD8 and the host checks the validity by analyzing the response of CMD8. The supplied voltage is indicated by VHS filed in the argument. The card assumes the voltage specified in VHS as the current supplied voltage. Only 1-bit of VHS shall be

set to 1 at any given time. Check pattern is used for the host to check validity of communication between the host and the card. If the card indicates an illegal command, the card is legacy and does not support CMD8. If the card supports CMD8 and can operate on the supplied voltage, the response echoes back the supply voltage and the check pattern that were set in the command argument. If VCA in the response is set to 0, the card cannot operate on the supplied voltage. If check pattern is not matched, CMD8 communication is not valid. In this case, it is recommended to retry CMD8 sequence.

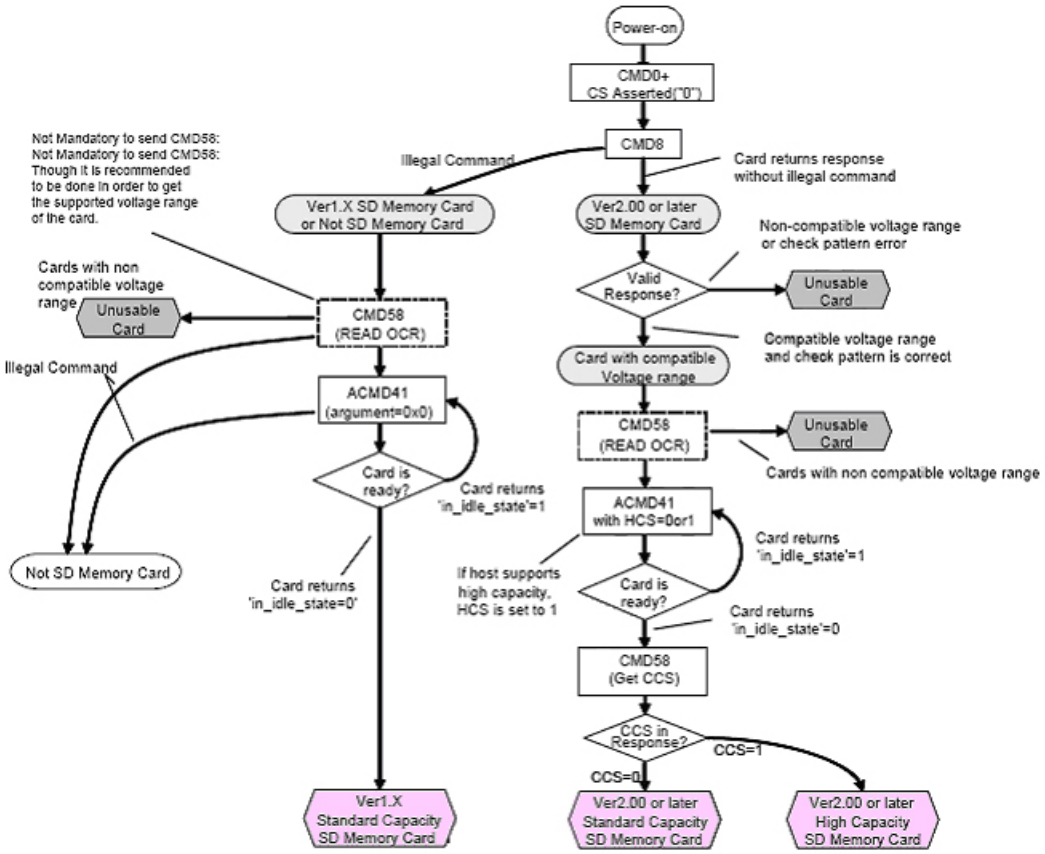


Figure 7-3: SPI Mode Initialization Flow

READ_OCR (CMD58) is designed to provide SD Memory Card hosts with a mechanism to identify cards that do not match the VDD range desired by the host. If the host does not accept voltage range, it shall not proceed further initialization sequence. The levels in the OCR register shall be defined accordingly. SD_SEND_OP_COND (ACMD41) is used to start initialization and to check if the card has completed initialization. It is mandatory to issue CMD8 prior to the first ACMD41. Receiving of CMD8 expands the CMD58 and ACMD41 function; HCS (High Capacity Support) in the argument of ACMD41 and CCS (Card Capacity Status) in the response of CMD58. HCS is ignored by the card, which didn't accept CMD8. Standard Capacity SD Memory Card ignores HCS. The "in idle state" bit

in the R1 response of ACMD41 is used by the card to inform the host if initialization of ACMD41 is completed. Setting this bit to "1" indicates that the card is still initializing. Setting this bit to "0" indicates completion of initialization. The host repeatedly issues ACMD41 until this bit is set to "0". The card checks the HCS bit in the OCR only at the first ACMD41. While repeating ACMD41, the host shall not issue another command except CMD0. After initialization is completed, the host should get CCS information in the response of CMD58. CCS is valid when the card accepted CMD8 and after the completion of initialization. CCS=1 means that the card is a High Capacity SD Memory Card. CCS=0 means that the card is a Standard Capacity SD.

7.3.2 Bus Transfer Protection

Every SD Card token transferred on the bus is protected by CRC bits. In SPI mode, the SD Card offers a non protected mode which enables systems built with reliable data links to exclude the hardware or firmware required for implementing the CRC generation and verification functions. In the non-protected mode the CRC bits of the command, response and data tokens are still required in the tokens. However, they are defined as 'don't care' for the transmitter and ignored by the receiver.

The SPI interface is initialized in the non-protected mode. However, the RESET command (CMD0) which is used to switch the card to SPI mode, is received by the card while in SD mode and, therefore, must have a valid CRC field.
Since CMD0 has no arguments, the content of all the fields, including the CRC field, are constants and need not be calculated in run time. A valid reset command is:

0x40, 0x0, 0x0, 0x0, 0x0, 0x95

The host can turn the CRC option on and off using the CRC_ON_OFF command (CMD59).

7.3.3 Data Read

The SPI mode supports single block read and Multiple Block read operations (CMD17 or CMD18 in the SD Card protocol). Upon reception of a valid read command the card will respond with a response token followed by a data token of the length defined in a previous SET_BLOCKLEN (CMD16) command (refer to Figure 7-3).

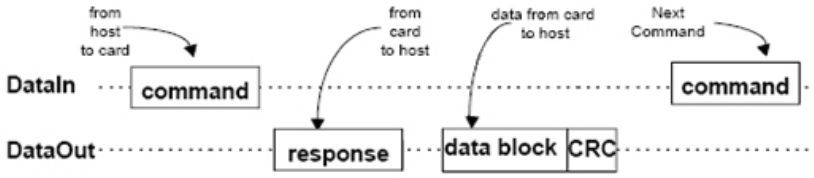


Figure 7-3: Single Block Read operation

In case of a data retrieval error, the card will not transmit any data. Instead, a special data error token will be sent to the host. Figure 7-4 shows a data read operation which terminated with an error token rather than a data block.

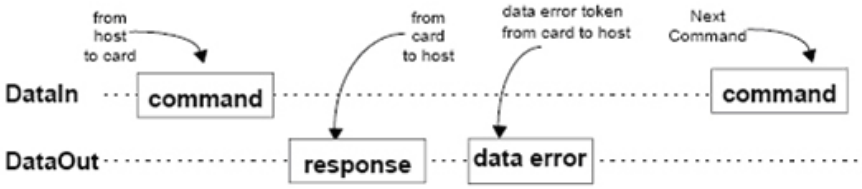


Figure 7-4: Read operation - data error

In case of Multiple block read operation every transferred block has its suffixed of 16 bit CRC. Stop transmission command (CMD12) will actually stop the data transfer operation (the same as in SD Card operation mode).

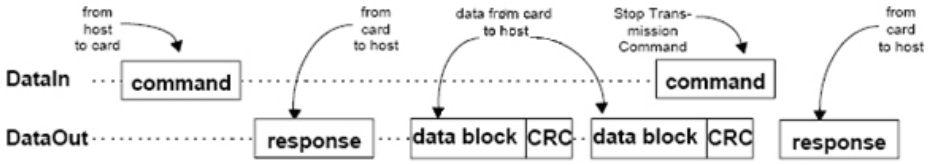


Figure 7-5: Multiple Block Read operation

7.3.4 Data Write

In SPI mode the SD Card supports single block and Multiple block write commands. Upon reception of a valid write command (CMD24 or CMD25 in the SD Card protocol), the card will respond with a response token and will wait for a data block to be sent from the host. CRC suffix, block length and start address restrictions are (with the exception of the CSD parameter WRITE_BL_PARTIAL controlling the partial block write option) identical to the read operation.

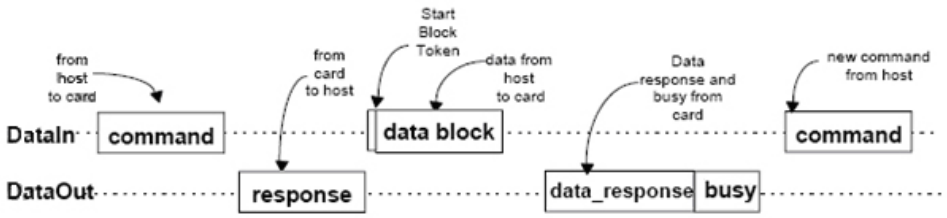


Figure 7-6: Single Block Write operation

Every data block has a prefix of 'Start Block' token (one byte).

After a data block has been received, the card will respond with a data-response token. If the data block has been received without errors, it will be programmed. As long as the card is busy programming, a continuous stream of busy tokens will be sent to the host (effectively holding the DataOut line low).

In Multiple Block write operation the stop transmission will be done by sending 'Stop Tran' token instead of 'Start Block' token at the beginning of the next block. In case of Write Error indication (on the data response) the host shall use SEND_NUM_WR_BLOCKS (ACMD22) in order to get the number of well written write blocks.

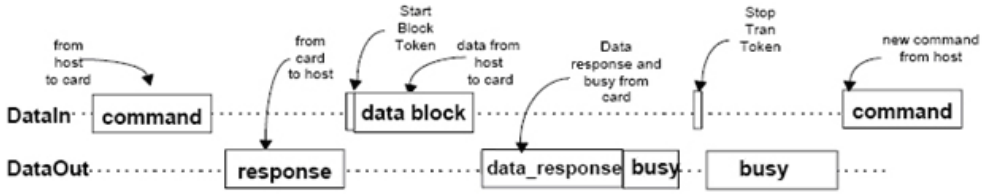


Figure 7-7: Multiple Block Write operation

While the card is busy, resetting the CS signal will not terminate the programming process. The card will release the DataOut line (tri-state) and continue with programming. If the card is reselected before the programming is finished, the DataOut line will be forced back to low and all commands will be rejected. Resetting a card (using CMD0) will terminate any pending or active programming operation. This may destroy the data formats on the card. It is in the responsibility of the host to prevent it.

7.3.5 Erase & Write Protect Management

The erase and write protect management procedures in the SPI mode are identical to those of the SD mode. While the card is erasing or changing the write protection bits of the predefined sector list, it will

be in a busy state and hold the DataOut line low. Figure 7-8 illustrates a 'no data' bus transaction with and without busy signaling.

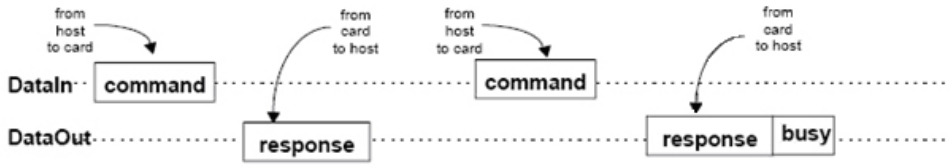


Figure 7-8: 'No data' operations

7.3.6 Read CID/CSD Registers

Unlike the SD Card protocol (where the register contents is sent as a command response), reading the contents of the CSD and CID registers in SPI mode is a simple read-block transaction. The card will respond with a standard response token followed by a data block of 16 bytes suffixed with a 16 bit CRC. The data time out for the CSD command cannot be set to the cards TAAC since this value is stored in the card's CSD. Therefore the standard response time-out value (NCR) is used for read latency of the CSD register.

7.3.7 Reset Sequence

The SD Card requires a defined reset sequence. After power on reset or CMD0 (software reset) the card enters an idle state. At this state the only valid host commands are ACMD41 (SD_SEND_OP_COND), CMD58 (READ_OCR) and CMD59 (CRC_ON_OFF). CMD1 (SEND_OP_COND) is also valid - that means that in SPI mode CMD1 and ACMD41 have the same behavior. After Power On, once the card accepted valid ACMD41, it will be able to accept also CMD1 even if used after re-initializing (CMD0) the card.

The host must poll the card (by repeatedly sending CMD1 or ACMD41) until the 'in-idle-state' bit in the card response indicates (by being set to 0) that the card completed its initialization processes and is ready for the next command.

In SPI mode, as opposed to SD mode, ACMD41 (or CMD1 as well) has no operands and does not return the contents of the OCR register. Instead, the host may use CMD58 (available in SPI mode only) to read the OCR register. Furthermore, it is in the responsibility of the host to refrain from accessing cards that do not support its voltage range. The usage of CMD58 is not restricted to the initializing phase only, but can be issued at any time.

ATP Electronics Inc.
TEL: +1-408-732-5000
FAX: +1-408-732-5055
sales@atpinc.com
750 North Mary Ave. Sunnyvale,
CA 94085 USA

ATP Electronics Europe B.V.
TEL: +31-88-287-0000
FAX: +31-88-287-0099
sales-europe@atpinc.com
Corkstraat 46, Rotterdam 3047 AC,
The Netherlands

ATP Electronics Tokyo Office
TEL: +81-03-6206-8097
FAX: +81-03-6206-8098
sales-japan@atpinc.com
www.atpinc.co.jp
#1007, 10F, 1-8-4 Kandasakuma-cho,
Chiyoda-ku, Tokyo

ATP Electronics (Shanghai), Inc.
TEL: +86-21-5080-2220
FAX: +86-21-5080-2219
sales@cn.atpinc.com
www.atpinc.com.cn
Room 102, No.500 BiBo road,
Zhangjiang High-tech park, Shanghai,
China, 201203

www.atpinc.com

Your Ultimate Memory Solution!

MIXED SIGNAL MICROCONTROLLER

FEATURES

- Low Supply Voltage Range 1.8 V to 3.6 V
- Ultra-Low Power Consumption
  - Active Mode: 365 µA at 1 MHz, 2.2 V
  - Standby Mode (VLO): 0.5 µA
  - Off Mode (RAM Retention): 0.1 µA
- Wake-Up From Standby Mode in Less Than 1 µs
- 16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time
- Three-Channel Internal DMA
- 12-Bit Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, and Autoscan Feature
- Dual 12-Bit Digital-to-Analog (D/A) Converters With Synchronization
- 16-Bit Timer_A With Three Capture/Compare Registers
- 16-Bit Timer_B With Seven Capture/Compare-With-Shadow Registers
- On-Chip Comparator
- Four Universal Serial Communication Interfaces (USCIs)
  - USCI_A0 and USCI_A1
    - Enhanced UART Supporting Auto-Baudrate Detection
    - IrDA Encoder and Decoder
    - Synchronous SPI
  - USCI_B0 and USCI_B1
    - I^2C™
    - Synchronous SPI
- Supply Voltage Supervisor/Monitor With Programmable Level Detection
- Brownout Detector
- Bootstrap Loader
- Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse
- Family Members:
  - MSP430F2416
    - 92KB + 256B Flash Memory
    - 4KB RAM
  - MSP430F2417
    - 92KB + 256B Flash Memory
    - 8KB RAM
  - MSP430F2418
    - 116KB + 256B Flash Memory
    - 8KB RAM
  - MSP430F2419
    - 120KB + 256B Flash Memory
    - 4KB RAM
  - MSP430F2616
    - 92KB + 256B Flash Memory
    - 4KB RAM
  - MSP430F2617
    - 92KB + 256B Flash Memory
    - 8KB RAM
  - MSP430F2618
    - 116KB + 256B Flash Memory
    - 8KB RAM
  - MSP430F2619
    - 120KB + 256B Flash Memory
    - 4KB RAM
- Available in 80-Pin Quad Flat Pack (LQFP), 64-Pin LQFP, and 113-Pin Ball Grid Array (BGA) (See Table 1)
- For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide* (SLAU144)

DESCRIPTION

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The calibrated digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 µs.

The MSP430F261x and MSP430F241x series are microcontroller configurations with two built-in 16-bit timers, a fast 12-bit A/D converter, a comparator, dual 12-bit D/A converters, four universal serial communication interface (USCI) modules, DMA, and up to 64 I/O pins. The MSP430F241x devices are identical to the MSP430F261x devices, with the exception that the DAC12 and the DMA modules are not implemented.

Typical applications include sensor systems, industrial control applications, and hand-held meters. The 12mmx12mm LQFP-64 package is also available as a non-magnetic package for medical imaging applications.

Table 1. Available Options(1)

T_A	PACKAGED DEVICES(2)		
	PLASTIC 113-PIN BGA (ZQW)	PLASTIC 80-PIN LQFP (PN)	PLASTIC 64-PIN LQFP (PM)
-40°C to 105°C	MSP430F2416TZQW MSP430F2417TZQW MSP430F2418TZQW MSP430F2419TZQW MSP430F2616TZQW MSP430F2617TZQW MSP430F2618TZQW MSP430F2619TZQW	MSP430F2416TPN MSP430F2417TPN MSP430F2418TPN MSP430F2419TPN MSP430F2616TPN MSP430F2617TPN MSP430F2618TPN MSP430F2619TPN	MSP430F2416TPM MSP430F2417TPM MSP430F2418TPM MSP430F2419TPM MSP430F2616TPM MSP430F2617TPM MSP430F2618TPM MSP430F2619TPM MSP430F2618TPMR-NM

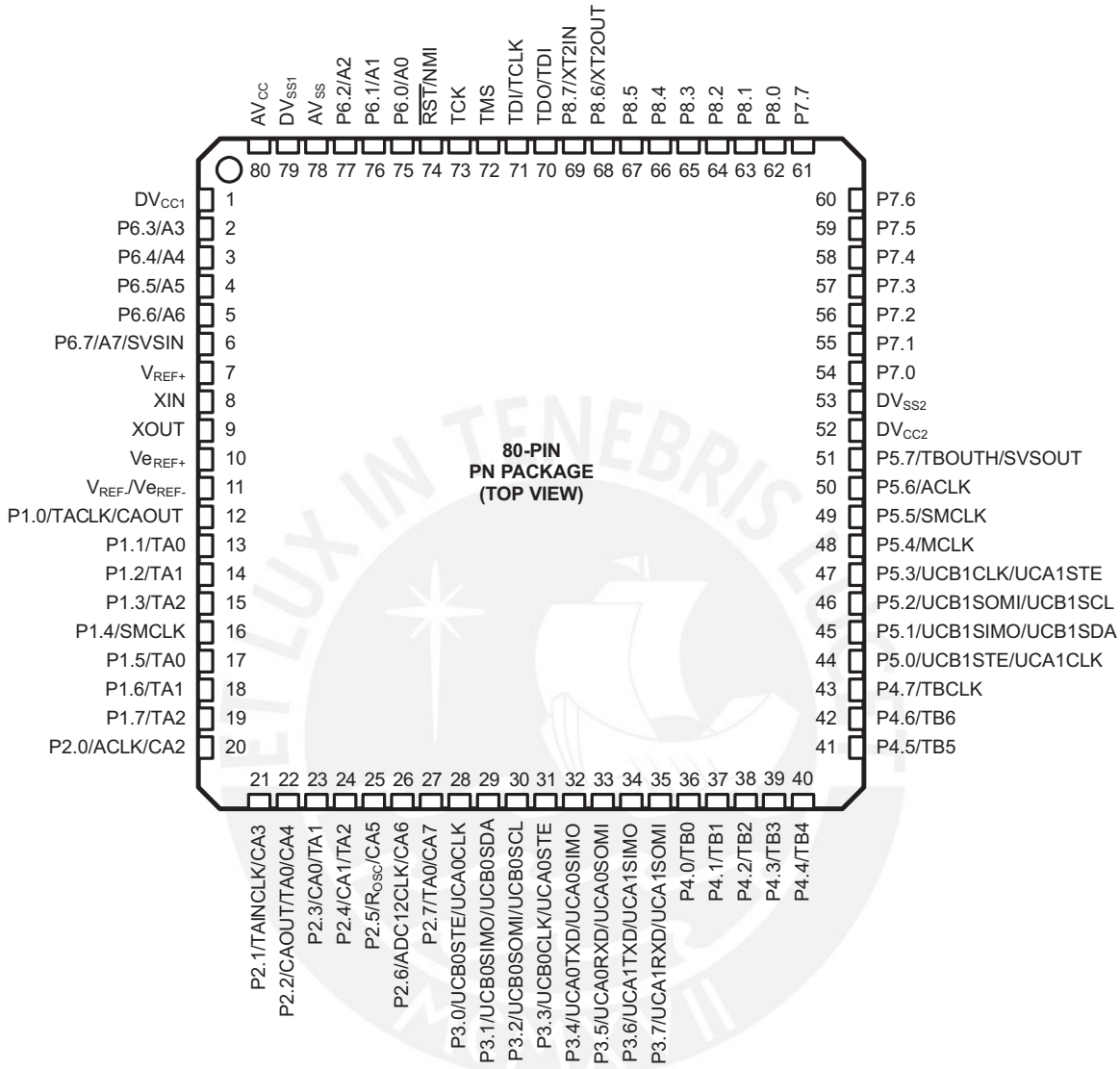
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Development Tool Support

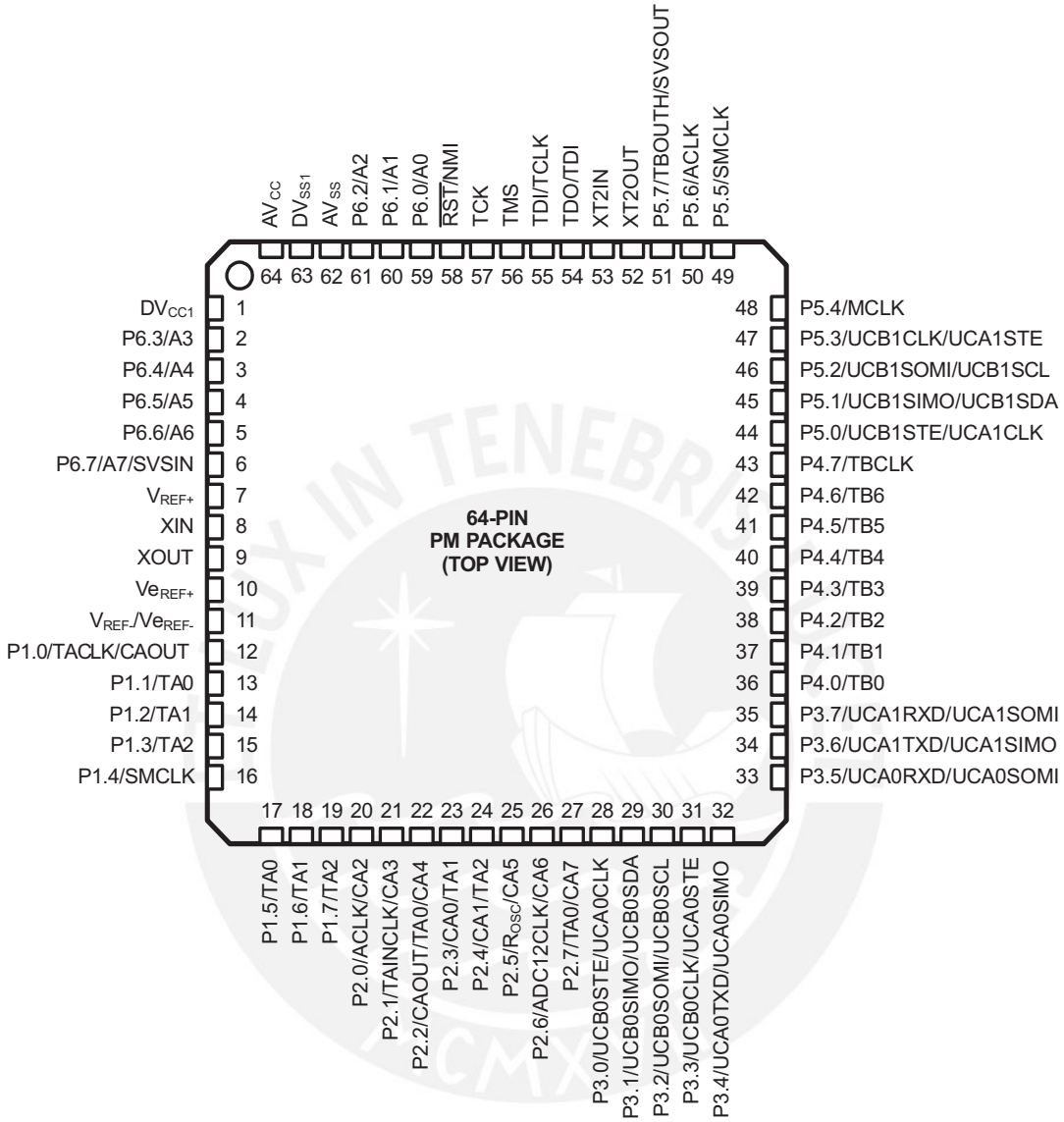
All MSP430 microcontrollers include an Embedded Emulation Module (EEM) allowing advanced debugging and programming through easy-to-use development tools. Recommended hardware options include:

- Debugging and Programming Interface
  - MSP-FET430UIF (USB)
  - MSP-FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
  - MSP-FET430U64 (PM Package)
  - MSP-FET430U80 (PN Package)
- Standalone Target Board
  - MSP-TS430PM64
- Production Programmer
  - MSP-GANG430

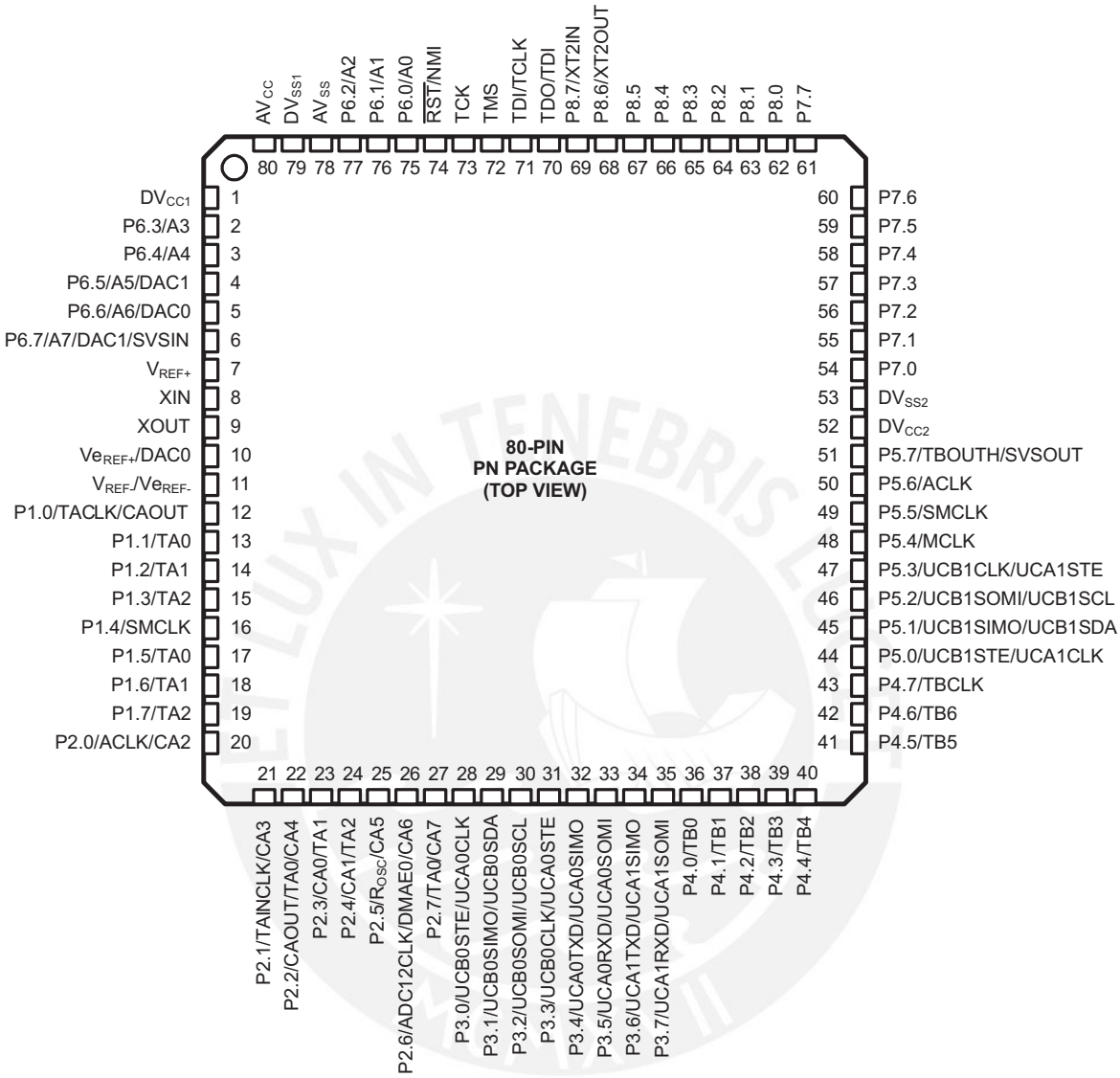
Device Pinout, MSP430F241x, 80-Pin PN Package



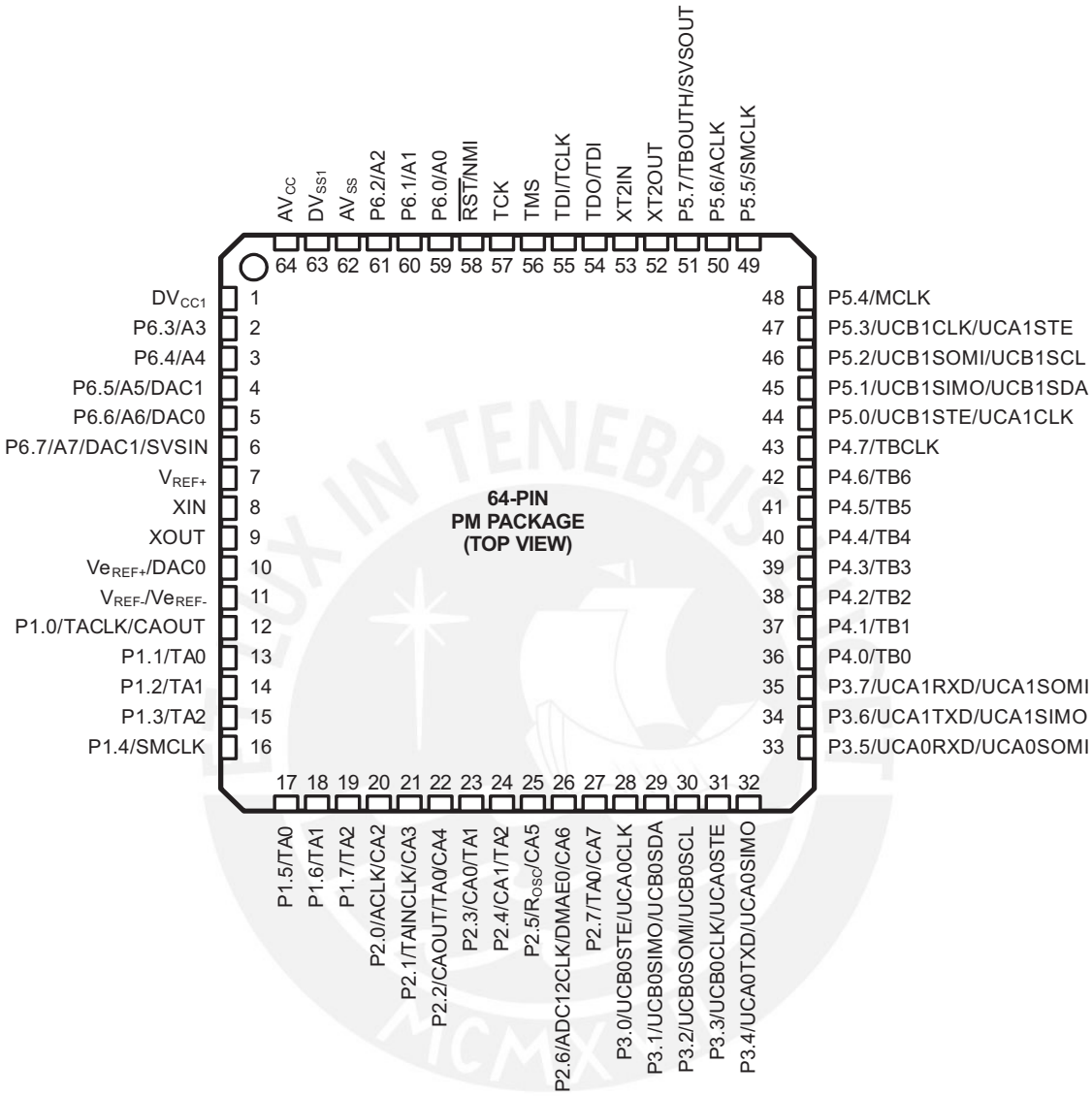
Device Pinout, MSP430F241x, 64-Pin PM Package



Device Pinout, MSP430F261x, 80-Pin PN Package



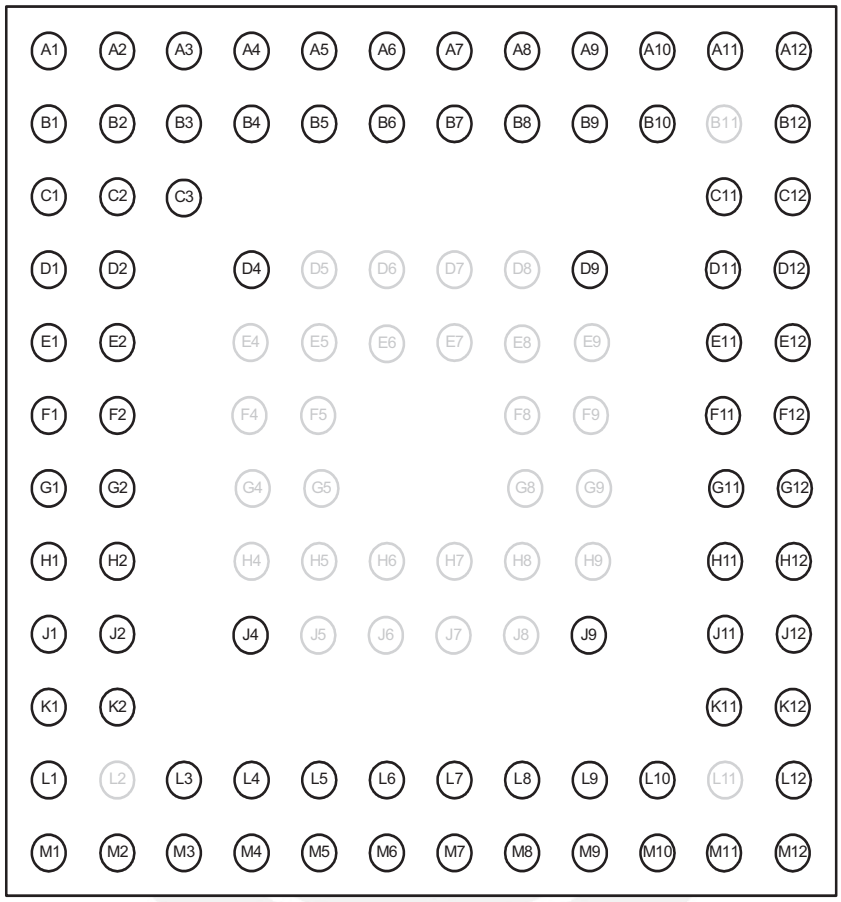
Device Pinout, MSP430F261x, 64-Pin PM Package



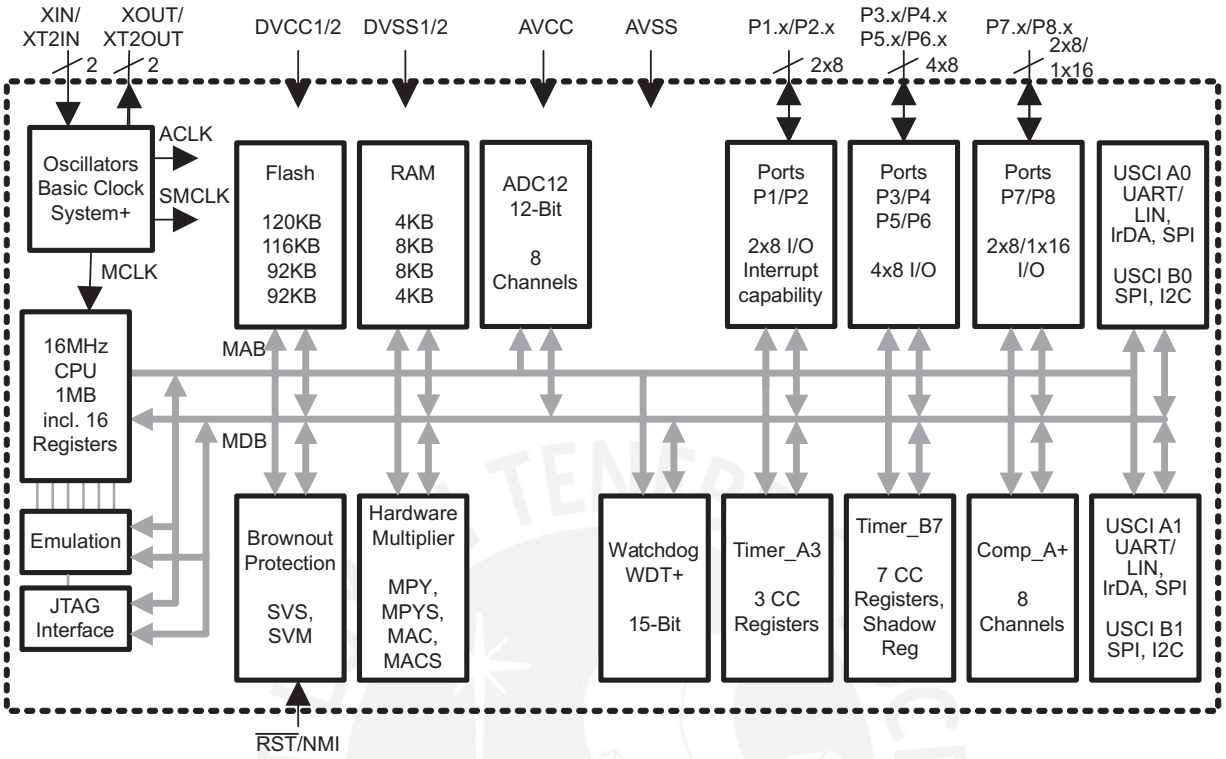
Device Pinout, 113-Pin ZQW Package

NOTE

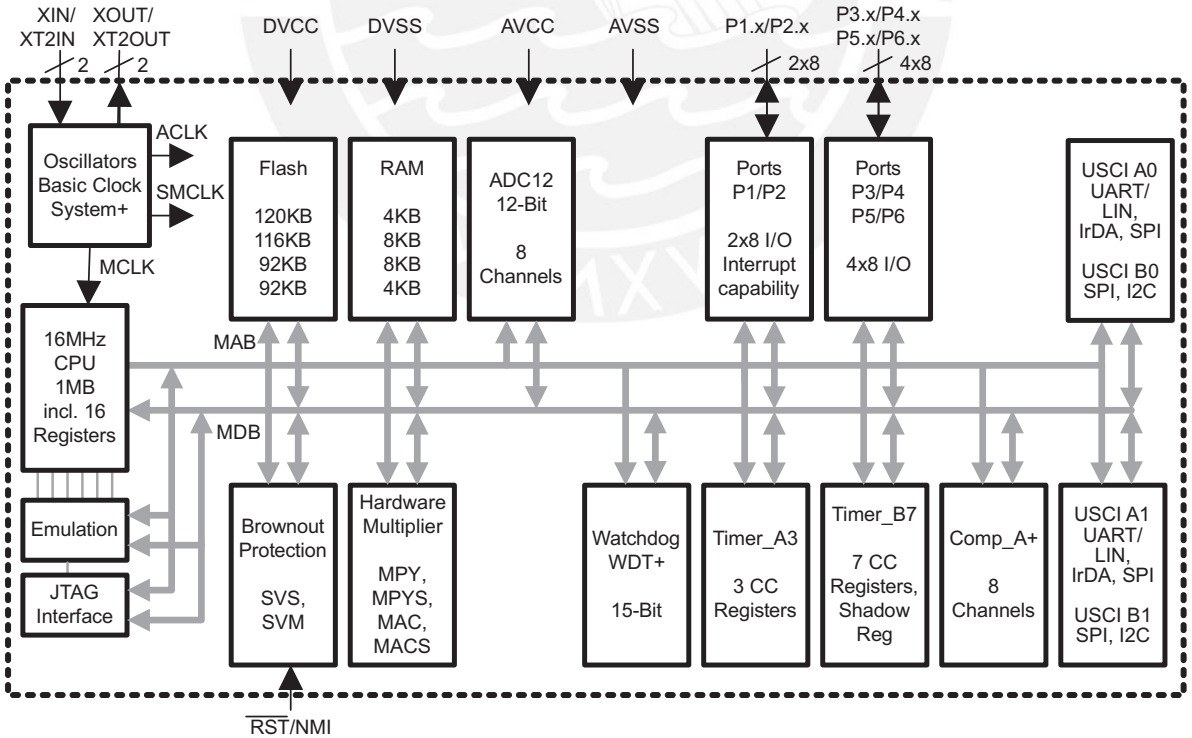
For terminal assignments, see Table 2.



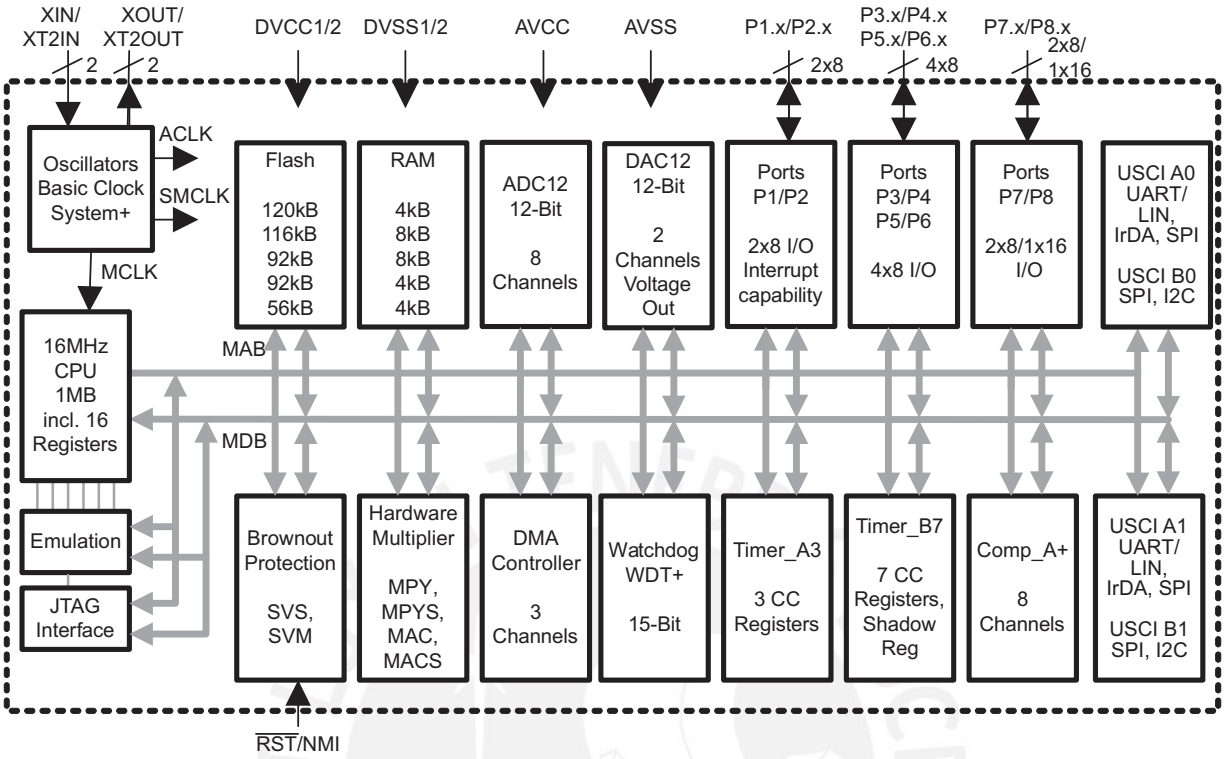
Functional Block Diagram, MSP430F241x, 80-Pin PN Package



Functional Block Diagram, MSP430F241x, 64-Pin PM Package



Functional Block Diagram, MSP430F261x, 80-Pin PN Package



Functional Block Diagram, MSP430F261x, 64-Pin PM Package

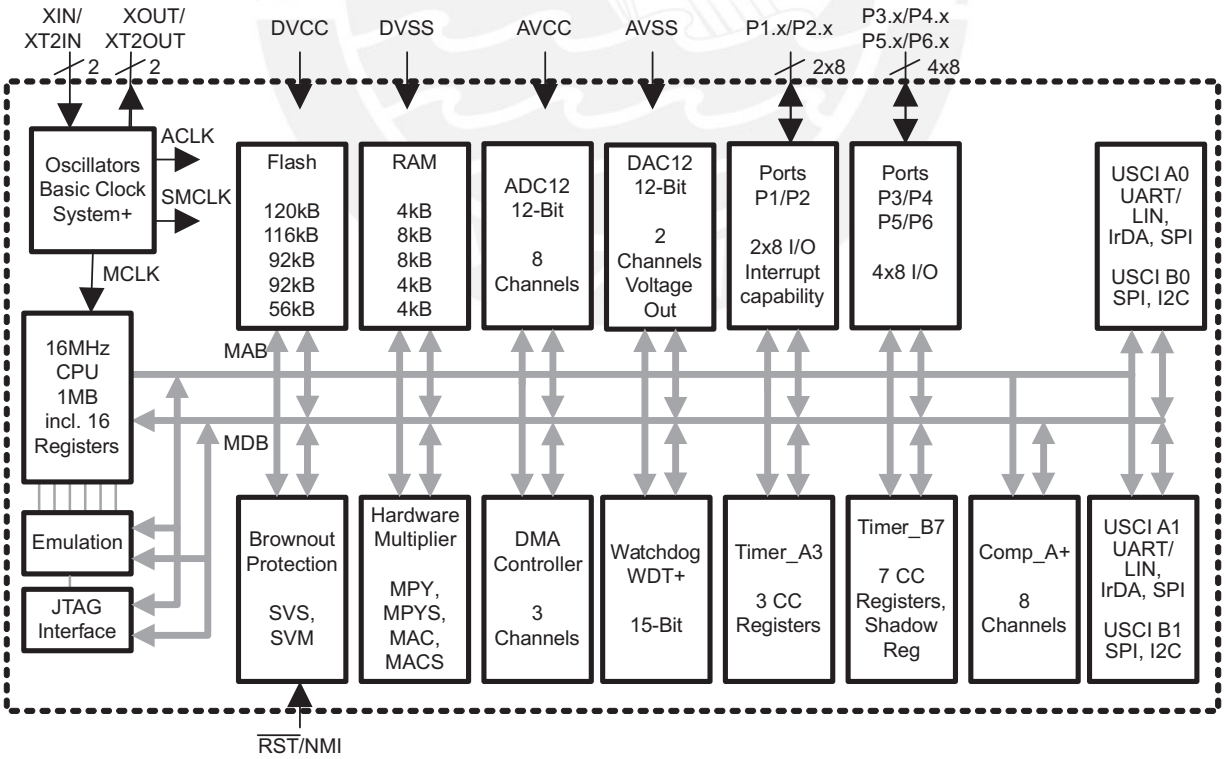


Table 2. Terminal Functions

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	64 PIN	80 PIN	113 PIN		
AV_{CC}	64	80	A2		Analog supply voltage, positive terminal. Supplies only the analog portion of ADC12 and DAC12.
AV_{SS}	62	78	B2, B3		Analog supply voltage, negative terminal. Supplies only the analog portion of ADC12 and DAC12.
DV_{CC1}	1	1	A1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS1}	63	79	A3		Digital supply voltage, negative terminal. Supplies all digital parts.
DV_{CC2}		52	F12		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS2}		53	E12		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TACLK/CAOUT	12	12	G2	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input Comparator_A output
P1.1/TA0	13	13	H1	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output BSL transmit
P1.2/TA1	14	14	H2	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	15	J1	I/O	General-purpose digital I/O pin Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	16	J2	I/O	General-purpose digital I/O pin SMCLK signal output
P1.5/TA0	17	17	K1	I/O	General-purpose digital I/O pin Timer_A, compare: Out0 output
P1.6/TA1	18	18	K2	I/O	General-purpose digital I/O pin Timer_A, compare: Out1 output
P1.7/TA2	19	19	L1	I/O	General-purpose digital I/O pin Timer_A, compare: Out2 output
P2.0/ACLK/CA2	20	20	M1	I/O	General-purpose digital I/O pin ACLK output/Comparator_A input
P2.1/TAINCLK/CA3	21	21	M2	I/O	General-purpose digital I/O pin Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0/CA4	22	22	M3	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0B input Comparator_A output BSL receive Comparator_A input
P2.3/CA0/TA1	23	23	L3	I/O	General-purpose digital I/O pin Timer_A, compare: Out1 output Comparator_A input
P2.4/CA1/TA2	24	24	L4	I/O	General-purpose digital I/O pin Timer_A, compare: Out2 output Comparator_A input
$P2.5/R_{OSC}$/CA5	25	25	M4	I/O	General-purpose digital I/O pin Input for external resistor defining the DCO nominal frequency Comparator_A input

Table 2. Terminal Functions (continued)

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	64 PIN	80 PIN	113 PIN		
P2.6/ADC12CLK/ DMAE0(1)/CA6	26	26	J4	I/O	General-purpose digital I/O pin Conversion clock - 12-bit ADC DMA channel 0 external trigger Comparator_A input
P2.7/TA0/CA7	27	27	L5	I/O	General-purpose digital I/O pin Timer_A, compare: Out0 output Comparator_A input
P3.0/UCB0STE/ UCA0CLK	28	28	M5	I/O	General-purpose digital I/O pin USCI_B0 slave transmit enable/USCI_A0 clock input/output
P3.1/UCB0SIMO/ UCB0SDA	29	29	L6	I/O	General-purpose digital I/O pin USCI_B0 slave-in master-out in SPI mode, SDA I2C data in I2C mode
P3.2/UCB0SOMI/ UCB0SCL	30	30	M6	I/O	General-purpose digital I/O pin USCI_B0 slave-out master-in in SPI mode, SCL I2C clock in I2C mode
P3.3/UCB0CLK/ UCA0STE	31	31	L7	I/O	General-purpose digital I/O USCI_B0 clock input/output, USCI_A0 slave transmit enable
P3.4/UCA0TXD/ UCA0SIMO	32	32	M7	I/O	General-purpose digital I/O pin USCI_A transmit data output in UART mode, slave data in/master out in SPI mode
P3.5/UCA0RXD/ UCA0SOMI	33	33	L8	I/O	General-purpose digital I/O pin USCI_A0 receive data input in UART mode, slave data out/master in in SPI mode
P3.6/UCA1TXD/ UCA1SIMO	34	34	M8	I/O	General-purpose digital I/O pin USCI_A1 transmit data output in UART mode, slave data in/master out in SPI mode
P3.7/UCA1RXD/ UCA1SOMI	35	35	L9	I/O	General-purpose digital I/O pin USCI_A1 receive data input in UART mode, slave data out/master in in SPI mode
P4.0/TB0	36	36	M9	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0A/B input, compare: Out0 output
P4.1/TB1	37	37	J9	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1A/B input, compare: Out1 output
P4.2/TB2	38	38	M10	I/O	General-purpose digital I/O pin Timer_B, capture: CCI2A/B input, compare: Out2 output
P4.3/TB3	39	39	L10	I/O	General-purpose digital I/O pin Timer_B, capture: CCI3A/B input, compare: Out3 output
P4.4/TB4	40	40	M11	I/O	General-purpose digital I/O pin Timer_B, capture: CCI4A/B input, compare: Out4 output
P4.5/TB5	41	41	M12	I/O	General-purpose digital I/O pin Timer_B, capture: CCI5A/B input, compare: Out5 output
P4.6/TB6	42	42	L12	I/O	General-purpose digital I/O pin Timer_B, capture: CCI6A input, compare: Out6 output
P4.7/TBCLK	43	43	K11	I/O	General-purpose digital I/O pin Timer_B, clock signal TBCLK input

(1) MSP430F261x devices only

Table 2. Terminal Functions (continued)

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	64 PIN	80 PIN	113 PIN		
P5.0/UCB1STE/ UCA1CLK	44	44	K12	I/O	General-purpose digital I/O pin USCI_B1 slave transmit enable/USCI_A1 clock input/output
P5.1/UCB1SIMO/ UCB1SDA	45	45	J11	I/O	General-purpose digital I/O pin USCI_B1 slave-in master-out in SPI mode, SDA I2C data in I2C mode
P5.2/UCB1SOMI/ UCB1SCL	46	46	J12	I/O	General-purpose digital I/O pin USCI_B1 slave-out master-in in SPI mode, SCL I2C clock in I2C mode
P5.3/UCB1CLK/ UCA1STE	47	47	H11	I/O	General-purpose digital I/O USCI_B1 clock input/output, USCI_A1 slave transmit enable
P5.4/MCLK	48	48	H12	I/O	General-purpose digital I/O pin Main system clock MCLK output
P5.5/SMCLK	49	49	G11	I/O	General-purpose digital I/O pin Submain system clock SMCLK output
P5.6/ACLK	50	50	G12	I/O	General-purpose digital I/O pin Auxiliary clock ACLK output
P5.7/TBOUTH/SVSOUT	51	51	F11	I/O	General-purpose digital I/O pin Switch all PWM digital output ports to high impedance - Timer_B TB0 to TB6 SVS comparator output
P6.0/A0	59	75	D4	I/O	General-purpose digital I/O pin Analog input A0 - 12-bit ADC
P6.1/A1	60	76	A4	I/O	General-purpose digital I/O pin Analog input A1 - 12-bit ADC
P6.2/A2	61	77	B4	I/O	General-purpose digital I/O pin Analog input A2 - 12-bit ADC
P6.3/A3	2	2	B1	I/O	General-purpose digital I/O pin Analog input A3 - 12-bit ADC
P6.4/A4	3	3	C1	I/O	General-purpose digital I/O pin Analog input A4 - 12-bit ADC
P6.5/A5/DAC1(2)	4	4	C2, C3	I/O	General-purpose digital I/O pin Analog input A5 - 12-bit ADC DAC12.1 output
P6.6/A6/DAC0(2)	5	5	D1	I/O	General-purpose digital I/O pin Analog input A6 - 12-bit ADC DAC12.0 output
P6.7/A7/DAC1(2)/SVSIN	6	6	D2	I/O	General-purpose digital I/O pin Analog input A7 - 12-bit ADC DAC12.1 output SVS input
P7.0		54	E11	I/O	General-purpose digital I/O pin
P7.1		55	D12	I/O	General-purpose digital I/O pin
P7.2		56	D11	I/O	General-purpose digital I/O pin
P7.3		57	C12	I/O	General-purpose digital I/O pin
P7.4		58	C11	I/O	General-purpose digital I/O pin

(2) MSP430F261x devices only

Table 2. Terminal Functions (continued)

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	64 PIN	80 PIN	113 PIN		
P7.5		59	B12	I/O	General-purpose digital I/O pin
P7.6		60	A12	I/O	General-purpose digital I/O pin
P7.7		61	A11	I/O	General-purpose digital I/O pin
P8.0		62	B10	I/O	General-purpose digital I/O pin
P8.1		63	A10	I/O	General-purpose digital I/O pin
P8.2		64	D9	I/O	General-purpose digital I/O pin
P8.3		65	A9	I/O	General-purpose digital I/O pin
P8.4		66	B9	I/O	General-purpose digital I/O pin
P8.5		67	B8	I/O	General-purpose digital I/O pin
P8.6/XT2OUT		68	A8	I/O	General-purpose digital I/O pin Output terminal of crystal oscillator XT2
P8.7/XT2IN		69	A7	I/O	General-purpose digital I/O pin Input port for crystal oscillator XT2. Only standard crystals can be connected.
XT2OUT	52			O	Output terminal of crystal oscillator XT2
XT2IN	53			I	Input port for crystal oscillator XT2
RST/NMI	58	74	B5	I	Reset input, nonmaskable interrupt input port, or bootstrap loader start (in flash devices)
TCK	57	73	A5	I	Test clock (JTAG). TCK is the clock input port for device programming test and bootstrap loader start
TDI/TCLK	55	71	A6	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	54	70	B7	I/O	Test data output port. TDO/TDI data output or programming data input terminal.
TMS	56	72	B6	I	Test mode select. TMS is used as an input port for device programming and test.
V_{eREF+}/DAC0(3)	10	10	F2	I	Input for an external reference voltage/DAC12.0 output
V_{REF+}	7	7	E2	O	Output of positive terminal of the reference voltage in the ADC12
V_{REF-}/V_{eREF-}	11	11	G1	I	Negative terminal for the reference voltage for both sources, the internal reference voltage or an external applied reference voltage
XIN	8	8	E1	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	9	F1	O	Output port for crystal oscillator XT1. Standard or watch crystals can be connected.
Reserved	-	-	(4)	NA	Reserved pins. Connection to DV_{SS}, AV_{SS} recommended.

(3) MSP430F261x devices only
(4) Reserved pins are L2, E4, F4, G4, H4, D5, E5, F5, G5, H5, J5, D6, E6, H6, J6, D7, E7, H7, J7, D8, E8, F8, G8, H8, J8, E9, F9, G9, H9, B11, L11.

SHORT-FORM DESCRIPTION

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 3 shows examples of the three types of instruction formats; Table 4 shows the address modes.

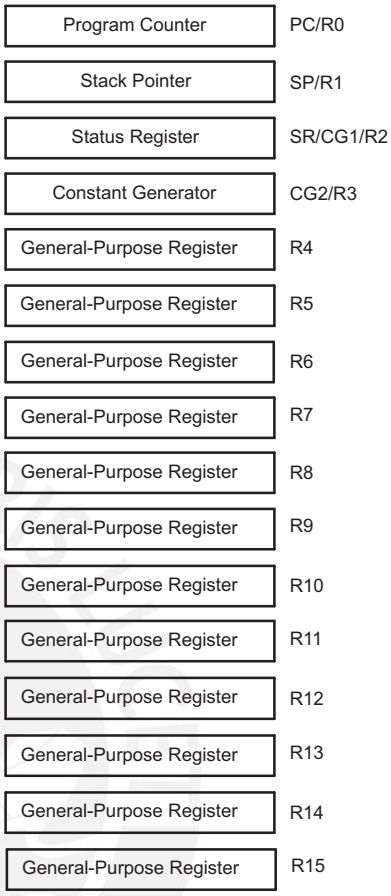


Table 3. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 -> R5
Single operands, destination only	CALL R8	PC ->(TOS), R8-> PC
Relative jump, un/conditional	JNE	Jump-on-equal bit = 0

Table 4. Address Mode Descriptions

ADDRESS MODE	S(1)	D(1)	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 -> R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)-> M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) -> M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) -> M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) -> M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) -> R11 R10 + 2-> R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 -> M(TONI)

(1) S = source, D = destination

Operating Modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active. MCLK is disabled
  - DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc-generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc-generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc-generator is disabled
  - Crystal oscillator is stopped

Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, flash is not programmed) the CPU enters LPM4 immediately after power-up.

Table 5. Interrupt Sources

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog Timer+ Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV See (2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(Non)maskable, (Non)maskable, (Non)maskable	0FFFCh	30
Timer_B7	TBCCR0 CCIFG(4)	Maskable	0FFFAh	29
Timer_B7	TBCCR1 to TBCCR6 CCIFGs, TBIFG(2)(4)	Maskable	0FFF8h	28
Comparator_A+	CAIFG	Maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	Maskable	0FFF4h	26
Timer_A3	TACCR0 CCIFG(4)	Maskable	0FFF2h	25
Timer_A3	TACCR1 CCIFG TACCR2 CCIFG(2)(4)	Maskable	0FFF0h	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG(2)(5)	Maskable	0FFEEh	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive or transmit	UCA0TXIFG, UCB0TXIFG(2)(6)	Maskable	0FFECh	22
ADC12	ADC12IFG(2)(4)	Maskable	0FFEAh	21
			0FFE8h	20
I/O port P2 (eight flags)	P2IFG.0 to P2IFG.7(2)(4)	Maskable	0FFE6h	19
I/O port P1 (eight flags)	P1IFG.0 to P1IFG.7(2)(4)	Maskable	0FFE4h	18
USCI_A1/USCI_B1 receive USCI_B1 I2C status	UCA1RXIFG, UCB1RXIFG(2)(5)	Maskable	0FFE2h	17
USCI_A1/USCI_B1 transmit USCI_B1 I2C receive or transmit	UCA1TXIFG, UCB1TXIFG(2)(6)	Maskable	0FFE0h	16
DMA	DMA0IFG, DMA1IFG, DMA2IFG(2)(4)	Maskable	0FFDEh	15
DAC12	DAC12_0IFG, DAC12_1IFG(2)(4)	Maskable	0FFDCh	14
See (7)(8)			0FFDAh to 0FFC0h	15 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
(2) Multiple source flags
(3) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are located in the module.
(5) In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.
(6) In UART/SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.
(7) The address 0FFBEh is used as bootstrap loader security key (BSLSKEY).
A 0AA55h at this location disables the BSL completely.
A zero disables the erasure of the flash if an invalid password is supplied.
(8) The interrupt vectors at addresses 0FFDAh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

Special Function Registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Legend		
	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is reset or set by PUC.
	rw-(0,1):	Bit can be read and written. It is reset or set by POR.
		SFR bit is not present in device.

Table 6. Interrupt Enable Register 1 and 2

Address	7	6	5	4	3	2	1	0
00h			**ACCVIE**	**NMIIE**			**OFIE**	**WDTIE**
			rw-0	rw-0			rw-0	rw-0

WDTIE Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.
OFIE Oscillator fault interrupt enable
NMIIE (Non)maskable interrupt enable
ACCVIE Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h					**UCB0TXIE**	**UCB0RXIE**	**UCA0TXIE**	**UCA0RXIE**
					rw-0	rw-0	rw-0	rw-0

UCA0RXIE USCI_A0 receive interrupt enable
UCA0TXIE USCI_A0 transmit interrupt enable
UCB0RXIE USCI_B0 receive interrupt enable
UCB0TXIE USCI_B0 transmit interrupt enable

Table 7. Interrupt Flag Register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				**NMIIFG**	**RSTIFG**	**PORIFG**	**OFIFG**	**WDTIFG**
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG Set on watchdog timer overflow (in watchdog mode) or security key violation.
Reset on V_{CC} power-on or a reset condition at the $\overline{RST}$/NMI pin in reset mode.
OFIFG Flag set on oscillator fault.
PORIFG Power-On Reset interrupt flag. Set on V_{CC} power-up.
RSTIFG External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power-up.
NMIIFG Set via $\overline{RST}$/NMI pin

Address	7	6	5	4	3	2	1	0
03h					**UCB0TXIFG**	**UCB0RXIFG**	**UCA0TXIFG**	**UCA0RXIFG**
					rw-1	rw-0	rw-1	rw-0

UCA0RXIFG USCI_A0 receive interrupt flag
UCA0TXIFG USCI_A0 transmit interrupt flag
UCB0RXIFG USCI_B0 receive interrupt flag
UCB0TXIFG USCI_B0 transmit interrupt flag

Memory Organization

Table 8. Memory Organization

		MSP430F2416 MSP430F2616	MSP430F2417 MSP430F2617	MSP430F2418 MSP430F2618	MSP430F2419 MSP430F2619
Memory	Size	92KB	92KB	116KB	120KB
Main: interrupt vector	Flash	0x0FFFF-0x0FFC0	0x0FFFF-0x0FFC0	0x0FFFF-0x0FFC0	0x0FFFF-0x0FFC0
Main: code memory	Flash	0x18FFF-0x02100	0x19FFF-0x03100	0x1FFFF-0x03100	0x1FFFF-0x02100
RAM (total)	Size	4KB 0x020FF-0x01100	8KB 0x030FF-0x01100	8KB 0x030FF-0x01100	4KB 0x020FF-0x01100
Extended	Size	2KB 0x020FF-0x01900	6KB 0x030FF-0x01900	6KB 0x030FF-0x01900	2KB 0x020FF-0x01900
Mirrored	Size	2KB 0x018FF-0x01100	2KB 0x018FF-0x01100	2KB 0x018FF-0x01100	2KB 0x018FF-0x01100
Information memory	Size	256 Byte	256 Byte	256 Byte	256 Byte
	Flash	0x010FF-0x01000	0x010FF-0x01000	0x010FF-0x01000	0x010FF-0x01000
Boot memory	Size	1KB	1KB	1KB	1KB
	ROM	0x00FFF-0x00C00	0x00FFF-0x00C00	0x00FFF-0x00C00	0x00FFF-0x00C00
RAM (mirrored at 0x18FF to 0x01100)	Size	2KB 0x009FF-0x00200	2KB 0x009FF-0x00200	2KB 0x009FF-0x00200	2KB 0x009FF-0x00200
Peripherals	16-bit	0x001FF-0x00100	0x001FF-0x00100	0x001FF-0x00100	0x001FF-0x00100
	8-bit	0x000FF-0x00010	0x000FF-0x00010	0x000FF-0x00010	0x000FF-0x00010
	8-bit SFR	0x0000F-0x00000	0x0000F-0x00000	0x0000F-0x00000	0x0000F-0x00000

Bootstrap Loader (BSL)

The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by a user-defined password. For complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader (BSL) User's Guide* (SLAU319).

Table 9. BSL Pin Functions

BSL FUNCTION	PM, PN PACKAGE PINS	ZQW PACKAGE PINS
Data Transmit	13 - P1.1	H1 - P1.1
Data Receive	22 - P2.2	M3 - P2.2

Flash Memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory.*
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.
- Flash content integrity check with marginal read modes

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide* (SLAU144).

DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12 conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode without having to awaken to move data to or from a peripheral.

Oscillator and System Clock

The clock system in the MSP430F241x and MSP430F261x family of devices is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very low-power low-frequency oscillator, an internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

The DCO settings to calibrate the DCO output frequency are stored in the information memory segment A.

Calibration Data Stored in Information Memory Segment A

Calibration data is stored for the DCO and for the ADC12. It is organized in a tag-length-value (TLV) structure.

Table 10. Tags Used by the TLV Structure

NAME	ADDRESS	VALUE	DESCRIPTION
TAG_DCO_30	0x10F6	0x01	DCO frequency calibration at V_{CC} = 3 V and T_A = 25°C at calibration
TAG_ADC12_1	0x10DA	0x08	ADC12_1 calibration tag
TAG_EMPTY	-	0xFE	Identifier for empty memory areas

Table 11. Labels Used by the ADC Calibration Structure

LABEL	CONDITION AT CALIBRATION	SIZE	ADDRESS OFFSET
CAL_ADC_25T85	INCHx = 0x1010, REF2_5 = 1, T_A = 85°C	word	0x000E
CAL_ADC_25T30	INCHx = 0x1010, REF2_5 = 1, T_A = 30°C	word	0x000C
CAL_ADC_25VREF_FACTOR	REF2_5 = 1, T_A = 30°C	word	0x000A
CAL_ADC_15T85	INCHx = 0x1010, REF2_5 = 0, T_A = 85°C	word	0x0008
CAL_ADC_15T30	INCHx = 0x1010, REF2_5 = 0, T_A = 30°C	word	0x0006
CAL_ADC_15VREF_FACTOR	REF2_5 = 0, T_A = 30°C	word	0x0004
CAL_ADC_OFFSET	External V_{REF} = 1.5 V, $f_{ADC12CLK}$ = 5 MHz	word	0x0002
CAL_ADC_GAIN_FACTOR	External V_{REF} = 1.5 V, $f_{ADC12CLK}$ = 5 MHz	word	0x0000
CAL_BC1_1MHZ	-	byte	0x0007
CAL_DCO_1MHZ	-	byte	0x0006
CAL_BC1_8MHZ	-	byte	0x0005
CAL_DCO_8MHZ	-	byte	0x0004
CAL_BC1_12MHZ	-	byte	0x0003
CAL_DCO_12MHZ	-	byte	0x0002
CAL_BC1_16MHZ	-	byte	0x0001
CAL_DCO_16MHZ	-	byte	0x0000

Brownout, Supply Voltage Supervisor (SVS)

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM) (the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must ensure that the default DCO settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

Digital I/O

There are up to eight 8-bit I/O ports implemented—ports P1 through P8:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and port P2.
- Read and write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup or pulldown resistor.
- Ports P7 and P8 can be accessed word-wise.

Watchdog Timer (WDT+)

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs 16x16, 16x8, 8x16, and 8x8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 pin or 4 pin) or I^2C, and asynchronous combination protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

The USCI_A module provides support for SPI (3 pin or 4 pin), UART, enhanced UART, and IrDA.

The USCI_B module provides support for SPI (3 pin or 4 pin) and I^2C

Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 12. Timer_A3 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
ZQW	PM, PN					PM, PN	ZQW
G2 - P1.0	12 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
M2 - P2.1	21 - P2.1	TAINCLK	INCLK				
H1 - P1.1	13 - P1.1	TA0	CCI0A	CCR0	TA0	13 - P1.1	H1 - P1.1
M3 - P2.2	22 - P2.2	TA0	CCI0B			17 - P1.5	K1 - P1.5
		DV_{SS}	GND			27 - P2.7	L5 - P2.7
		DV_{CC}	V_{CC}				
H2 - P1.2	14 - P1.2	TA1	CCI1A	CCR1	TA1	14 - P1.2	H2 - P1.2
		CAOUT (internal)	CCI1B			18 - P1.6	K2 - P1.6
		DV_{SS}	GND			23 - P2.3	L3 - P2.3
		DV_{CC}	V_{CC}			ADC12 (internal)	
						DAC12_0 (internal)	
						DAC12_1 (internal)	
J1 - P1.3	15 - P1.3	TA2	CCI2A	CCR2	TA2	15 - P1.3	J1 - P1.3
		ACLK (internal)	CCI2B			19 - P1.7	L1 - P1.7
		DV_{SS}	GND			24 - P2.4	L4 - P2.4
		DV_{CC}	V_{CC}				

Timer_B7

Timer_B7 is a 16-bit timer/counter with seven capture/compare registers. Timer_B7 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 13. Timer_B3, Timer_B7 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
ZQW	PM, PN					PM, PN	ZQW
K11 - P4.7	43 - P4.7	TBCLK	TBCLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
K11 - P4.7	43 - P4.7	TBCLK	INCLK				
M9 - P4.0	36 - P4.0	TB0	CCI0A	CCR0	TB0	36 - P4.0	M9 - P4.0
M9- P4.0	36 - P4.0	TB0	CCI0B			ADC12 (internal)	
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
J9 - P4.1	37 - P4.1	TB1	CCI1A	CCR1	TB1	37 - P4.1	J9 - P4.1
J9 - P4.1	37 - P4.1	TB1	CCI1B			ADC12 (internal)	
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
M10 - P4.2	38 - P4.2	TB2	CCI2A	CCR2	TB2	38 - P4.2	M10 - P4.2
M10 - P4.2	38 - P4.2	TB2	CCI2B			DAC_0 (internal)	
		DV_{SS}	GND			DAC_1 (internal)	
		DV_{CC}	V_{CC}				
L10 - P4.3	39 - P4.3	TB3	CCI3A	CCR3	TB3	39 - P4.3	L10 - P4.3
L10 - P4.3	39 - P4.3	TB3	CCI3B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
M11 - P4.4	40 - P4.4	TB4	CCI4A	CCR4	TB4	40 - P4.4	M11 - P4.4
M11 - P4.4	40 - P4.4	TB4	CCI4B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
M12 - P4.5	41 - P4.5	TB5	CCI5A	CCR5	TB5	41 - P4.5	M12 - P4.5
M12 - P4.5	41 - P4.5	TB5	CCI5B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
L12 - P4.6	42 - P4.6	TB6	CCI6A	CCR6	TB6	42 - P4.6	L12 - P4.6
		ACLK (internal)	CCI6B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				

Comparator_A+

The primary function of the Comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

ADC12

The ADC12 module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator, and a 16-word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

DAC12

The DAC12 module is a 12-bit R-ladder voltage-output digital-to-analog converter (DAC). The DAC12 may be used in 8-bit or 12-bit mode and may be used in conjunction with the DMA controller. When multiple DAC12 modules are present, they may be grouped together for synchronous operation.

Peripheral File Map

Table 14. Peripherals File Map

MODULE	REGISTER	SHORT FORM	ADDRESS
DMA(1)	DMA channel 2 transfer size	DMA2SZ	0x01F2
	DMA channel 2 destination address	DMA2DA	0x01EE
	DMA channel 2 source address	DMA2SA	0x01EA
	DMA channel 2 control	DMA2CTL	0x01E8
	DMA channel 1 transfer size	DMA1SZ	0x01E6
	DMA channel 1 destination address	DMA1DA	0x01E2
	DMA channel 1 source address	DMA1SA	0x01DE
	DMA channel 1 control	DMA1CTL	0x01DC
	DMA channel 0 transfer size	DMA0SZ	0x01DA
	DMA channel 0 destination address	DMA0DA	0x01D6
	DMA channel 0 source address	DMA0SA	0x01D2
	DMA channel 0 control	DMA0CTL	0x01D0
	DMA module interrupt vector word	DMAIV	0x0126
	DMA module control 1	DMACTL1	0x0124
	DMA module control 0	DMACTL0	0x0122
DAC12(1)	DAC12_1 data	DAC12_1DAT	0x01CA
	DAC12_1 control	DAC12_1CTL	0x01C2
	DAC12_0 data	DAC12_0DAT	0x01C8
	DAC12_0 control	DAC12_0CTL	0x01C0

(1) MSP430F261x devices only

Table 14. Peripherals File Map (continued)

MODULE	REGISTER	SHORT FORM	ADDRESS
ADC12	Interrupt vector word register	ADC12IV	0x01A8
	Interrupt enable register	ADC12IE	0x01A6
	Interrupt flag register	ADC12IFG	0x01A4
	Control register 1	ADC12CTL1	0x01A2
	Control register 0	ADC12CTL0	0x01A0
	Conversion memory 15	ADC12MEM15	0x015E
	Conversion memory 14	ADC12MEM14	0x015C
	Conversion memory 13	ADC12MEM13	0x015A
	Conversion memory 12	ADC12MEM12	0x0158
	Conversion memory 11	ADC12MEM11	0x0156
	Conversion memory 10	ADC12MEM10	0x0154
	Conversion memory 9	ADC12MEM9	0x0152
	Conversion memory 8	ADC12MEM8	0x0150
	Conversion memory 7	ADC12MEM7	0x014E
	Conversion memory 6	ADC12MEM6	0x014C
	Conversion memory 5	ADC12MEM5	0x014A
	Conversion memory 4	ADC12MEM4	0x0148
	Conversion memory 3	ADC12MEM3	0x0146
	Conversion memory 2	ADC12MEM2	0x0144
	Conversion memory 1	ADC12MEM1	0x0142
	Conversion memory 0	ADC12MEM0	0x0140
	ADC memory-control register15	ADC12MCTL15	0x008F
	ADC memory-control register14	ADC12MCTL14	0x008E
	ADC memory-control register13	ADC12MCTL13	0x008D
	ADC memory-control register12	ADC12MCTL12	0x008C
	ADC memory-control register11	ADC12MCTL11	0x008B
	ADC memory-control register10	ADC12MCTL10	0x008A
	ADC memory-control register9	ADC12MCTL9	0x0089
	ADC memory-control register8	ADC12MCTL8	0x0088
	ADC memory-control register7	ADC12MCTL7	0x0087
	ADC memory-control register6	ADC12MCTL6	0x0086
	ADC memory-control register5	ADC12MCTL5	0x0085
	ADC memory-control register4	ADC12MCTL4	0x0084
	ADC memory-control register3	ADC12MCTL3	0x0083
	ADC memory-control register2	ADC12MCTL2	0x0082
	ADC memory-control register1	ADC12MCTL1	0x0081
	ADC memory-control register0	ADC12MCTL0	0x0080

Table 14. Peripherals File Map (continued)

MODULE	REGISTER	SHORT FORM	ADDRESS
Timer_B7	Capture/compare register 6	TBCCR6	0x019E
	Capture/compare register 5	TBCCR5	0x019C
	Capture/compare register 4	TBCCR4	0x019A
	Capture/compare register 3	TBCCR3	0x0198
	Capture/compare register 2	TBCCR2	0x0196
	Capture/compare register 1	TBCCR1	0x0194
	Capture/compare register 0	TBCCR0	0x0192
	Timer_B register	TBR	0x0190
	Capture/compare control 6	TBCCTL6	0x018E
	Capture/compare control 5	TBCCTL5	0x018C
	Capture/compare control 4	TBCCTL4	0x018A
	Capture/compare control 3	TBCCTL3	0x0188
	Capture/compare control 2	TBCCTL2	0x0186
	Capture/compare control 1	TBCCTL1	0x0184
	Capture/compare control 0	TBCCTL0	0x0182
	Timer_B control	TBCTL	0x0180
	Timer_B interrupt vector	TBIV	0x011E
Timer_A3	Capture/compare register 2	TACCR2	0x0176
	Capture/compare register 1	TACCR1	0x0174
	Capture/compare register 0	TACCR0	0x0172
	Timer_A register	TAR	0x0170
	Reserved		0x016E
	Reserved		0x016C
	Reserved		0x016A
	Reserved		0x0168
	Capture/compare control 2	TACCTL2	0x0166
	Capture/compare control 1	TACCTL1	0x0164
	Capture/compare control 0	TACCTL0	0x0162
	Timer_A control	TACTL	0x0160
	Timer_A interrupt vector	TAIV	0x012E
Hardware Multiplier	Sum extend	SUMEXT	0x013E
	Result high word	RESHI	0x013C
	Result low word	RESLO	0x013A
	Second operand	OP2	0x0138
	Multiply signed +accumulate/operand 1	MACS	0x0136
	Multiply+accumulate/operand 1	MAC	0x0134
	Multiply signed/operand 1	MPYS	0x0132
	Multiply unsigned/operand 1	MPY	0x0130
Flash	Flash control 4	FCTL4	0x01BE
	Flash control 3	FCTL3	0x012C
	Flash control 2	FCTL2	0x012A
	Flash control 1	FCTL1	0x0128
Watchdog	Watchdog Timer control	WDTCTL	0x0120

Table 14. Peripherals File Map (continued)

MODULE	REGISTER	SHORT FORM	ADDRESS
USCI_A0/B0	USCI_A0 auto baud rate control	UCA0ABCTL	0x005D
	USCI_A0 transmit buffer	UCA0TXBUF	0x0067
	USCI_A0 receive buffer	UCA0RXBUF	0x0066
	USCI_A0 status	UCA0STAT	0x0065
	USCI_A0 modulation control	UCA0MCTL	0x0064
	USCI_A0 baud rate control 1	UCA0BR1	0x0063
	USCI_A0 baud rate control 0	UCA0BR0	0x0062
	USCI_A0 control 1	UCA0CTL1	0x0061
	USCI_A0 control 0	UCA0CTL0	0x0060
	USCI_A0 IrDA receive control	UCA0IRRCTL	0x005F
	USCI_A0 IrDA transmit control	UCA0IRTCLT	0x005E
	USCI_B0 transmit buffer	UCB0TXBUF	0x006F
	USCI_B0 receive buffer	UCB0RXBUF	0x006E
	USCI_B0 status	UCB0STAT	0x006D
	USCI_B0 I2C Interrupt enable	UCB0CIE	0x006C
	USCI_B0 baud rate control 1	UCB0BR1	0x006B
	USCI_B0 baud rate control 0	UCB0BR0	0x006A
	USCI_B0 control 1	UCB0CTL1	0x0069
	USCI_B0 control 0	UCB0CTL0	0x0068
	USCI_B0 I2C slave address	UCB0SA	0x011A
	USCI_B0 I2C own address	UCB0OA	0x0118
USCI_A1/B1	USCI_A1 auto baud rate control	UCA1ABCTL	0x00CD
	USCI_A1 transmit buffer	UCA1TXBUF	0x00D7
	USCI_A1 receive buffer	UCA1RXBUF	0x00D6
	USCI_A1 status	UCA1STAT	0x00D5
	USCI_A1 modulation control	UCA1MCTL	0x00D4
	USCI_A1 baud rate control 1	UCA1BR1	0x00D3
	USCI_A1 baud rate control 0	UCA1BR0	0x00D2
	USCI_A1 control 1	UCA1CTL1	0x00D1
	USCI_A1 control 0	UCA1CTL0	0x00D0
	USCI_A1 IrDA receive control	UCA1IRRCTL	0x00CF
	USCI_A1 IrDA transmit control	UCA1IRTCLT	0x00CE
	USCI_B1 transmit buffer	UCB1TXBUF	0x00DF
	USCI_B1 receive buffer	UCB1RXBUF	0x00DE
	USCI_B1 status	UCB1STAT	0x00DD
	USCI_B1 I2C Interrupt enable	UCB1CIE	0x00DC
	USCI_B1 baud rate control 1	UCB1BR1	0x00DB
	USCI_B1 baud rate control 0	UCB1BR0	0x00DA
	USCI_B1 control 1	UCB1CTL1	0x00D9
	USCI_B1 control 0	UCB1CTL0	0x00D8
	USCI_B1 I2C slave address	UCB1SA	0x017E
	USCI_B1 I2C own address	UCB1OA	0x017C
	USCI_A1/B1 interrupt enable	UC1IE	0x0006
	USCI_A1/B1 interrupt flag	UC1IFG	0x0007
Comparator_A+	Comparator_A port disable	CAPD	0x005B
	Comparator_A control2	CACTL2	0x005A
	Comparator_A control1	CACTL1	0x0059

Table 14. Peripherals File Map (continued)

MODULE	REGISTER	SHORT FORM	ADDRESS
Basic Clock	Basic clock system control 3	BCSCTL3	0x0053
	Basic clock system control 2	BCSCTL2	0x0058
	Basic clock system control 1	BCSCTL1	0x0057
	DCO clock frequency control	DCOCTL	0x0056
Brownout, SVS	SVS control register (reset by brownout signal)	SVSCTL	0x0055
Port PA(2)	Port PA resistor enable	PAREN	0x0014
	Port PA selection	PASEL	0x003E
	Port PA direction	PADIR	0x003C
	Port PA output	PAOUT	0x003A
	Port PA input	PAIN	0x0038
Port P8(2)	Port P8 resistor enable	P8REN	0x0015
	Port P8 selection	P8SEL	0x003F
	Port P8 direction	P8DIR	0x003D
	Port P8 output	P8OUT	0x003B
	Port P8 input	P8IN	0x0039
Port P7(3)	Port P7 resistor enable	P7REN	0x0014
	Port P7 selection	P7SEL	0x003E
	Port P7 direction	P7DIR	0x003C
	Port P7 output	P7OUT	0x003A
	Port P7 input	P7IN	0x0038
Port P6	Port P6 resistor enable	P6REN	0x0013
	Port P6 selection	P6SEL	0x0037
	Port P6 direction	P6DIR	0x0036
	Port P6 output	P6OUT	0x0035
	Port P6 input	P6IN	0x0034
Port P5	Port P5 resistor enable	P5REN	0x0012
	Port P5 selection	P5SEL	0x0033
	Port P5 direction	P5DIR	0x0032
	Port P5 output	P5OUT	0x0031
	Port P5 input	P5IN	0x0030
Port P4	Port P4 selection	P4SEL	0x001F
	Port P4 resistor enable	P4REN	0x0011
	Port P4 direction	P4DIR	0x001E
	Port P4 output	P4OUT	0x001D
	Port P4 input	P4IN	0x001C
Port P3	Port P3 resistor enable	P3REN	0x0010
	Port P3 selection	P3SEL	0x001B
	Port P3 direction	P3DIR	0x001A
	Port P3 output	P3OUT	0x0019
	Port P3 input	P3IN	0x0018

(2) 80-pin PN and 113-pin ZQW devices only
(3) 80-pin PN and 113-pin ZQW devices only

Table 14. Peripherals File Map (continued)

MODULE	REGISTER	SHORT FORM	ADDRESS
Port P2	Port P2 resistor enable	P2REN	0x002F
	Port P2 selection	P2SEL	0x002E
	Port P2 interrupt enable	P2IE	0x002D
	Port P2 interrupt-edge select	P2IES	0x002C
	Port P2 interrupt flag	P2IFG	0x002B
	Port P2 direction	P2DIR	0x002A
	Port P2 output	P2OUT	0x0029
	Port P2 input	P2IN	0x0028
Port P1	Port P1 resistor enable	P1REN	0x0027
	Port P1 selection	P1SEL	0x0026
	Port P1 interrupt enable	P1IE	0x0025
	Port P1 interrupt-edge select	P1IES	0x0024
	Port P1 interrupt flag	P1IFG	0x0023
	Port P1 direction	P1DIR	0x0022
	Port P1 output	P1OUT	0x0021
	Port P1 input	P1IN	0x0020
Special Functions	SFR interrupt flag 2	IFG2	0x0003
	SFR interrupt flag 1	IFG1	0x0002
	SFR interrupt enable 2	IE2	0x0001
	SFR interrupt enable 1	IE1	0x0000

Absolute Maximum Ratings(1)

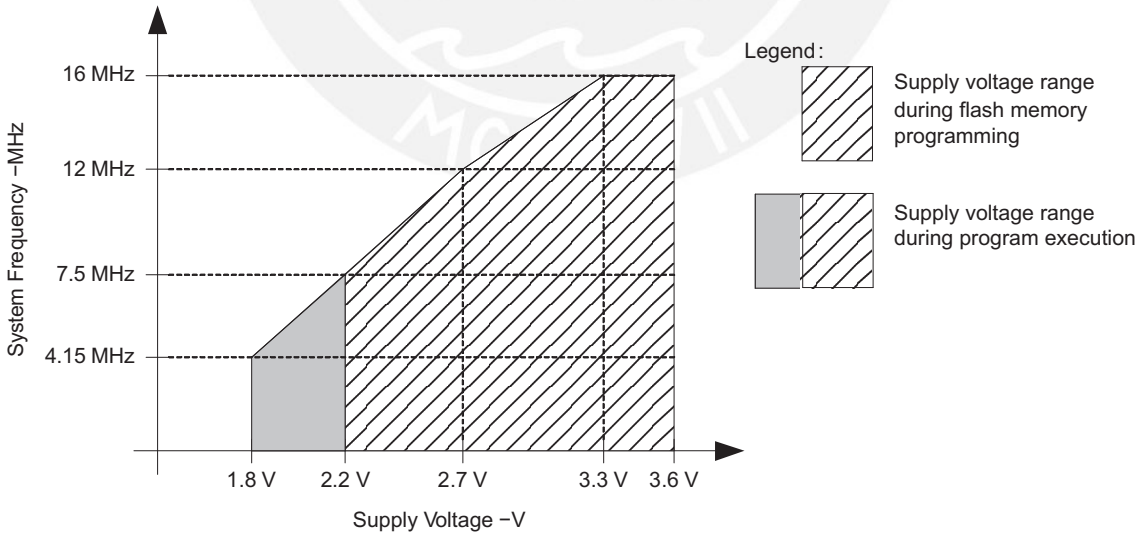
	Voltage applied at V_{CC} to V_{SS}		-0.3 V to 4.1 V
	Voltage applied to any pin(2)		-0.3 V to V_{CC} + 0.3 V
	Diode current at any device terminal		±2 mA
T_{stg}	Storage temperature(3)	Unprogrammed device	-55°C to 150°C
		Programmed device	-55°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage (AV_{CC} = DV_{CC} = V_{CC}(1))	During program execution	1.8	3.6	V
		During flash program/erase	2.2	3.6	
V_{SS}	Supply voltage (AV_{SS} = DV_{SS} = V_{SS})		0	0	V
T_A	Operating free-air temperature	I version	-40	85	°C
		T version	-40	105	
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(2)(3)	V_{CC} = 1.8 V, Duty cycle = 50% ± 10%	dc	4.15	MHz
		V_{CC} = 2.7 V, Duty cycle = 50% ± 10%	dc	12	
		V_{CC} ≥ 3.3 V, Duty cycle = 50% ± 10%	dc	16	

(1) It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power-up.
(2) The MSP430 CPU is clocked directly with MCLK. Both the high and low phases of MCLK must not exceed the pulse duration of the specified maximum frequency.
(3) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



Note: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Operating Area

Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,1MHz}$	Active mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32768 Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		365	395	µA
			105°C			375	420	
			-40°C to 85°C	3 V		515	560	
			105°C			525	595	
$I_{AM,1MHz}$	Active mode (AM) current (1 MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 32768 Hz, Program executes in RAM, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		330	370	µA
			105°C			340	390	
			-40°C to 85°C	3 V		460	495	
			105°C			470	520	
$I_{AM,4kHz}$	Active mode (AM) current (4 kHz)	$f_{MCLK} = f_{SMCLK} = f_{ACLK}$ = 32768 Hz/8 = 4096 Hz, f_{DCO} = 0 Hz, Program executes in flash, SELMx = 11, SELS = 1, DIVMx = DIVSx = DIVAx = 11, CPUOFF = 0, SCG0 = 1, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		2.1	9	µA
			105°C	2.2 V		15	31	
			-40°C to 85°C	3 V		3	11	
			105°C	3 V		19	32	
$I_{AM,100kHz}$	Active mode (AM) current (100 kHz)	$f_{MCLK} = f_{SMCLK} = f_{DCO(0, 0)} \approx$ 100 kHz, f_{ACLK} = 0 Hz, Program executes in flash, RSELx = 0, DCOx = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 1	-40°C to 85°C	2.2 V		67	86	µA
			105°C	2.2 V		80	99	
			-40°C to 85°C	3 V		84	107	
			105°C	3 V		99	128	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

Typical Characteristics - Active Mode Supply Current (Into V_{CC})

ACTIVE MODE CURRENT vs SUPPLY VOLTAGE (T_A = 25°C)

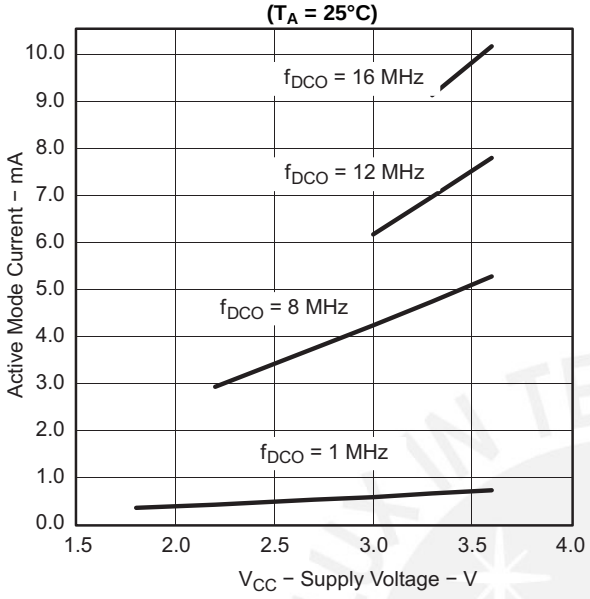


Figure 2.

ACTIVE MODE CURRENT vs DCO FREQUENCY

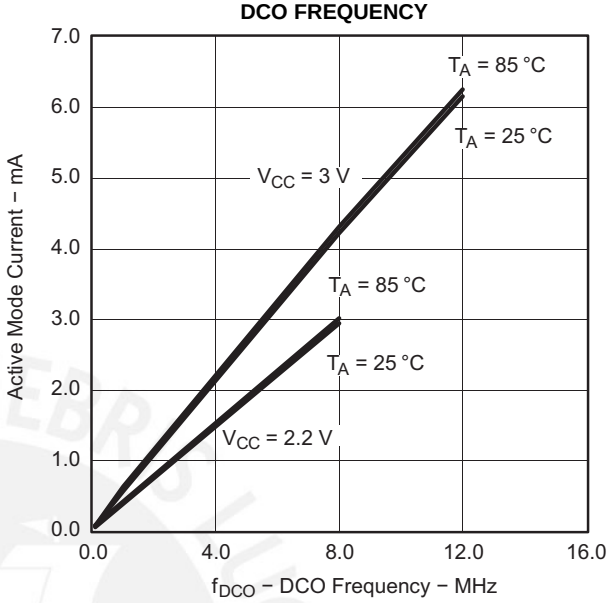


Figure 3.

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{LPM0,1MHz}$	Low-power mode 0 (LPM0) current(3)	f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	-40°C to 85°C	2.2 V		68	63	µA
			105°C			83	98	
			-40°C to 85°C	3 V		87	105	
			105°C			100	125	
$I_{LPM0,100kHz}$	Low-power mode 0 (LPM0) current(3)	f_{MCLK} = 0 MHz, f_{SMCLK} = $f_{DCO(0, 0)}$ ≈ 100 kHz, f_{ACLK} = 0 Hz, RSELx = 0, DCOx = 0, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 1	-40°C to 85°C	2.2 V		37	49	µA
			105°C			50	62	
			-40°C to 85°C	3 V		40	55	
			105°C			57	73	
I_{LPM2}	Low-power mode 2 (LPM2) current(4)	f_{MCLK} = f_{SMCLK} = 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	-40°C to 85°C	2.2 V		23	33	µA
			105°C			35	46	
			-40°C to 85°C	3 V		25	36	
			105°C			40	55	
$I_{LPM3,LFXT1}$	Low-power mode 3 (LPM3) current(3)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32,768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C	2.2 V		0.8	1.2	µA
			25°C			1	1.3	
			85°C			4.6	7	
			105°C			14	24	
			-40°C	3 V		0.9	1.3	
			25°C			1.1	1.5	
			85°C			5.5	8	
			105°C			17	30	
$I_{LPM3,VLO}$	Low-power mode 3 (LPM3) current(4)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	-40°C	2.2 V		0.4	1	µA
			25°C			0.5	1	
			85°C			4.3	6.5	
			105°C			14	24	
			-40°C	3 V		0.6	1.2	
			25°C			0.6	1.2	
			85°C			5	7.5	
			105°C			16.5	29.5	
I_{LPM4}	Low-power mode 4 (LPM4) current(5)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	-40°C	2.2 V		0.1	0.5	µA
			25°C			0.1	0.5	
			85°C			4	6	
			105°C			13	23	
			-40°C	3 V		0.2	0.5	
			25°C			0.2	0.5	
			85°C			4.7	7	
			105°C			14	24	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF.
(3) Current for brownout and WDT clocked by SMCLK included.
(4) Current for brownout and WDT clocked by ACLK included.
(5) Current for brownout included.

Typical Characteristics - LPM4 Current

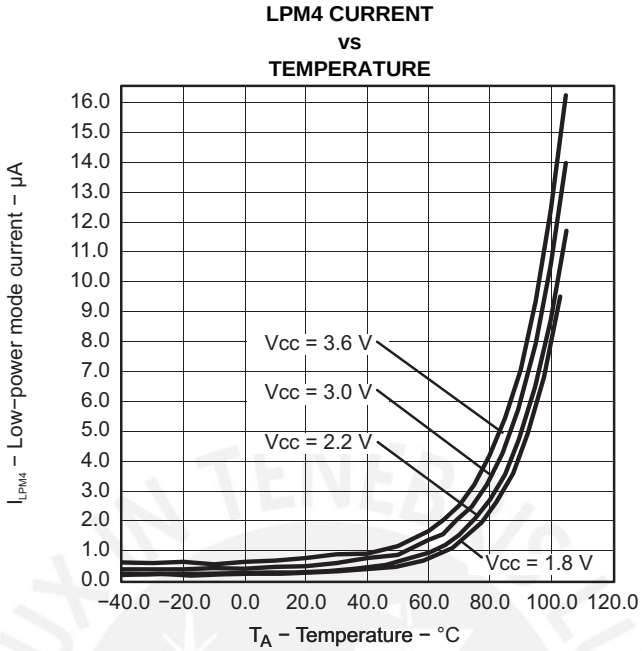


Figure 4.

Schmitt-Trigger Inputs (Ports P1 Through P8, $\overline{RST}$/NMI, JTAG, XIN, and XT2IN)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45 V_{CC}		0.75 V_{CC}	V
			2.2 V	1.00		1.65	
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage			0.25 V_{CC}		0.55 V_{CC}	V
			2.2 V	0.55		1.20	
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis (V_{IT+} - V_{IT-})		2.2 V	0.2		1	V
			3 V	0.3		1	
R_{Pull}	Pullup/pulldown resistor	For pullup: $V_{IN} = V_{SS}$, For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

(1) XIN and XT2IN in bypass mode only

Inputs (Ports P1 and P2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag(1)	2.2 V, 3 V	20		ns

(1) An external signal sets the interrupt flag every time the minimum interrupt pulse width $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$.

Leakage Current (Ports P1 Through P8)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.y)}$	High-impedance leakage current	(1) (2)	2.2 V, 3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

Standard Inputs ($\overline{RST}$/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{IL}	Low-level input voltage		2.2 V, 3 V	V_{SS}	V_{SS} + 0.6	V
V_{IH}	High-level input voltage		2.2 V, 3 V	0.8 V_{CC}	V_{CC}	V

Outputs (Ports P1 Through P8)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = -1.5 mA (1)	2.2 V	V_{CC} - 0.25		V_{CC}	V
		$I_{(OHmax)}$ = -6 mA (2)	2.2 V	V_{CC} - 0.6		V_{CC}	
		$I_{(OHmax)}$ = -1.5 mA (1)	3 V	V_{CC} - 0.25		V_{CC}	
		$I_{(OHmax)}$ = -6 mA (2)	3 V	V_{CC} - 0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1.5 mA (1)	2.2 V	V_{SS}		V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 6 mA (2)	2.2 V	V_{SS}		V_{SS} + 0.6	
		$I_{(OLmax)}$ = 1.5 mA (1)	3 V	V_{SS}		V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA (2)	3 V	V_{SS}		V_{SS} + 0.6	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±12 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

Output Frequency (Ports P1 Through P8)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	P1.4/SMCLK, C_L = 20 pF, R_L = 1 kΩ (1) (2)	2.2 V	dc		10	MHz
			3 V	dc		12	
$f_{Port°CLK}$	Clock output frequency	P2.0/ACLK/CA2, P1.4/SMCLK, C_L = 20 pF (2)	2.2 V	dc		12	MHz
			3 V	dc		16	
$t_{(Xdc)}$	Duty cycle of output frequency	P5.6/ACLK, C_L = 20 pF, LF mode		30	50	70	%
		P5.6/ACLK, C_L = 20 pF, XT1 mode		40	50	60	
		P5.4/MCLK, C_L = 20 pF, XT1 mode		40		60	
		P5.4/MCLK, C_L = 20 pF, DCO		50% - 15 ns		50% + 15 ns	
		P1.4/SMCLK, C_L = 20 pF, XT2 mode		40		60	
		P1.4/SMCLK, C_L = 20 pF, DCO		50% - 15 ns		50% + 15 ns	

(1) A resistive divider with two 0.5-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics - Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

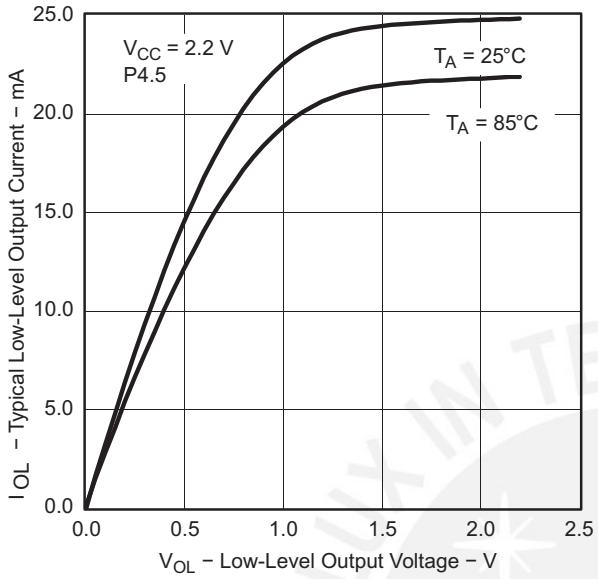


Figure 5.

LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

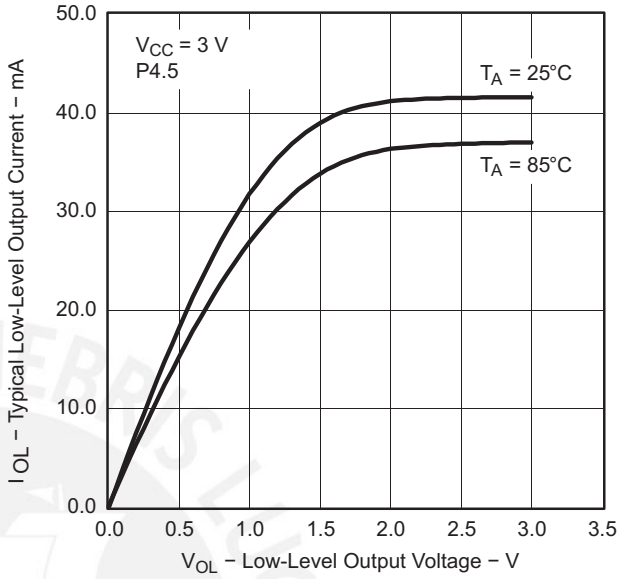


Figure 6.

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

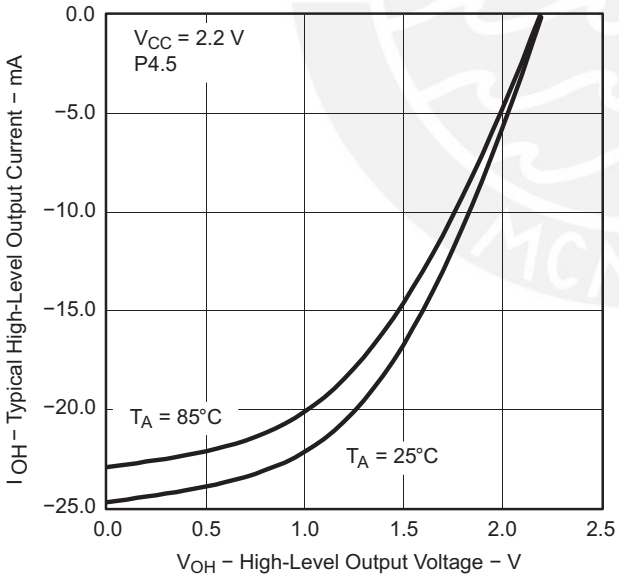


Figure 7.

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

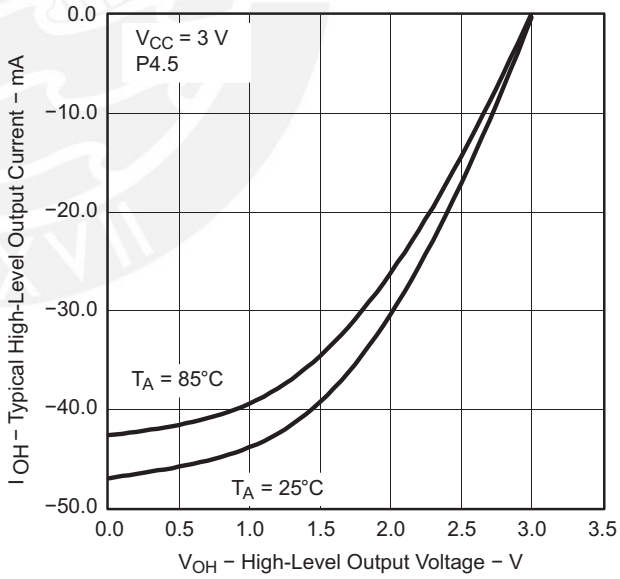


Figure 8.

POR and Brownout Reset (BOR)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	See Figure 9	$dV_{CC}/dt \le 3$ V/s			0.7 × $V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$	See Figure 9 through Figure 11	$dV_{CC}/dt \le 3$ V/s				1.71	V
$V_{hys(B\_IT-)}$	See Figure 9	$dV_{CC}/dt \le 3$ V/s		70	130	210	mV
$t_{d(BOR)}$	See Figure 9					2000	µs
$t_{(reset)}$	Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally		2.2 V, 3 V	2			µs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)}$ + $V_{hys(B_IT-)}$is ≤ 1.8 V.

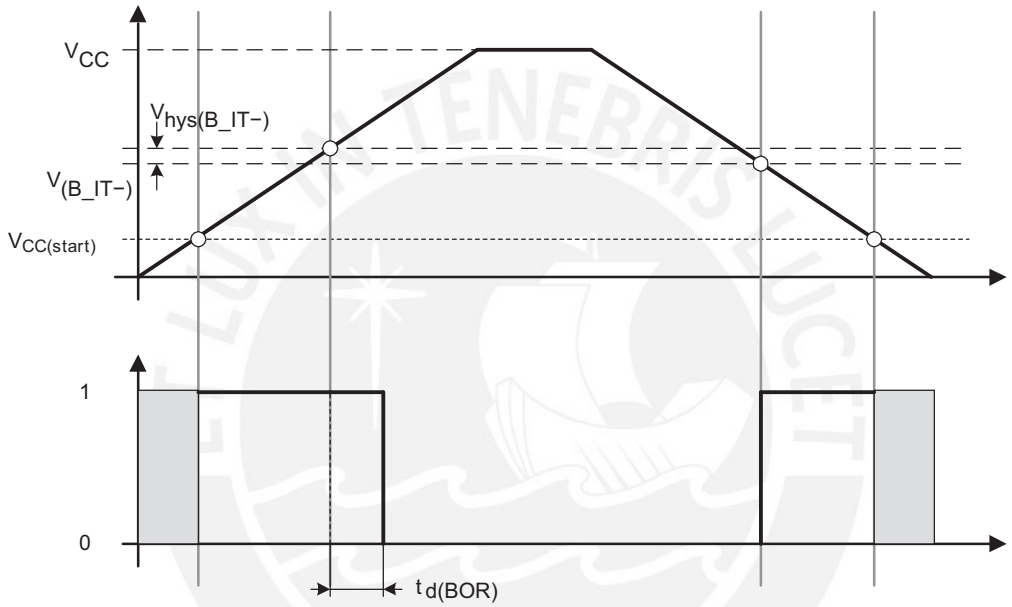


Figure 9. POR and BOR vs Supply Voltage

Typical Characteristics - POR and BOR

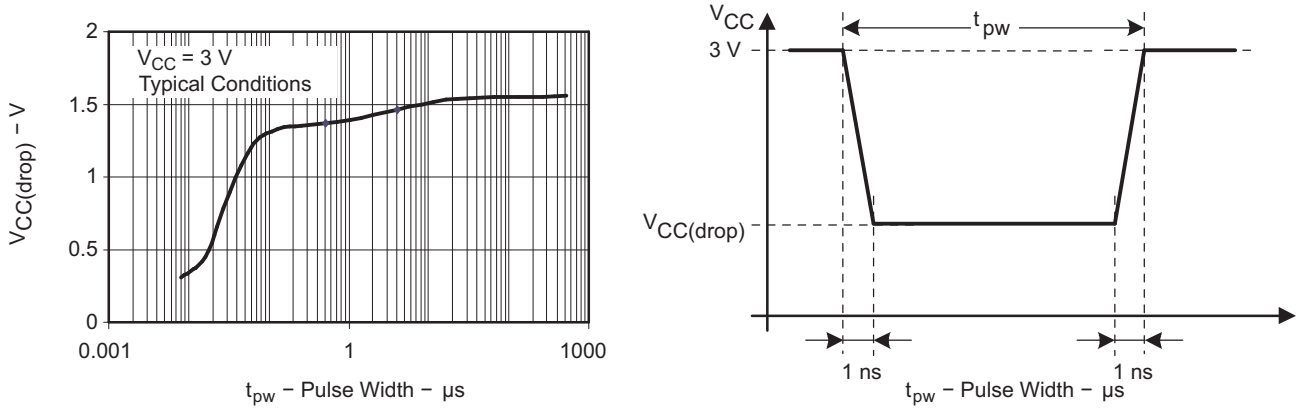


Figure 10. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR jor BOR Signal

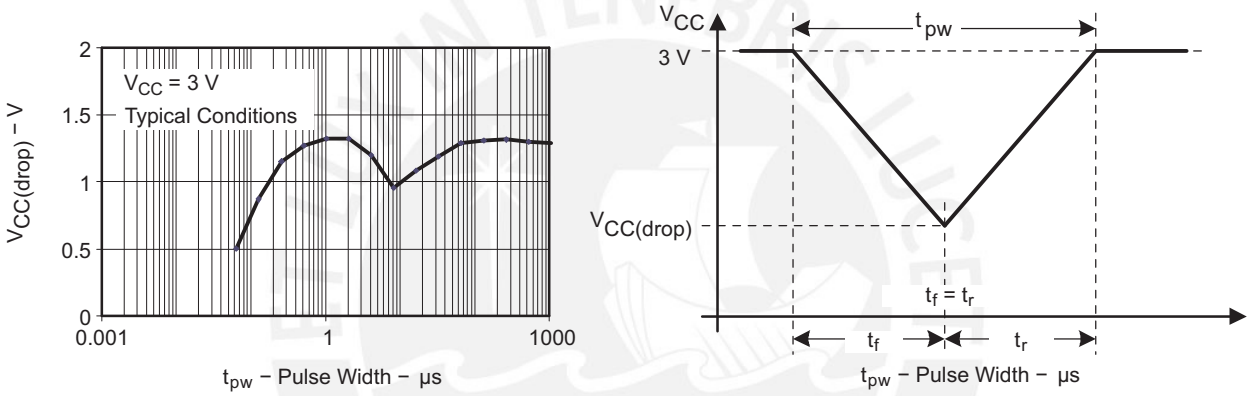


Figure 11. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR or BOR Signal

Supply Voltage Supervisor (SVS), Supply Voltage Monitor (SVM)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(SVSR)}$	dV_{CC}/dt > 30 V/ms (see Figure 12)		5		150	µs
	dV_{CC}/dt ≤ 30 V/ms				2000	
$t_{d(SVSon)}$	SVSon, switch from VLD = 0 to VLD ≠ 0, V_{CC} = 3 V			150	300	µs
t_{settle}	VLD ≠ 0 (1)				12	µs
$V_{(SVSstart)}$	VLD ≠ 0, V_{CC}/dt ≤ 3 V/s (see Figure 12)			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	V_{CC}/dt ≤ 3 V/s (see Figure 12)	VLD = 1	70	120	155	mV
		VLD = 2 to 14	0.004 × $V_{(SVS\_IT-)}$		0.016 × $V_{(SVS\_IT-)}$	V
	V_{CC}/dt ≤ 3 V/s (see Figure 12), external voltage applied on A7	VLD = 15	4.4		20	mV
$V_{(SVS\_IT-)}$	V_{CC}/dt ≤ 3V/s (see Figure 12 and Figure 13)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.25	
		VLD = 3	2.05	2.2	2.37	
		VLD = 4	2.14	2.3	2.48	
		VLD = 5	2.24	2.4	2.60	
		VLD = 6	2.33	2.5	2.71	
		VLD = 7	2.46	2.65	2.86	
		VLD = 8	2.58	2.8	3	
		VLD = 9	2.69	2.9	3.13	
		VLD = 10	2.83	3.05	3.29	
		VLD = 11	2.94	3.2	3.42	
		VLD = 12	3.11	3.35	3.61 (2)	
		VLD = 13	3.24	3.5	3.76 (2)	
		VLD = 14	3.43	3.7 (2)	3.99 (2)	
	V_{CC}/dt ≤ 3 V/s (see Figure 12 and Figure 13), external voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (3)	VLD ≠ 0, V_{CC} = 2.2 V, 3 V			10	15	µA

(1) t_{settle} is the settling time that the comparator output needs to have a stable level after VLD is switched from VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be >50 mV.
(2) The recommended operating voltage range is limited to 3.6 V.
(3) The current consumption of the SVS module is not included in the I_{CC} current consumption data.

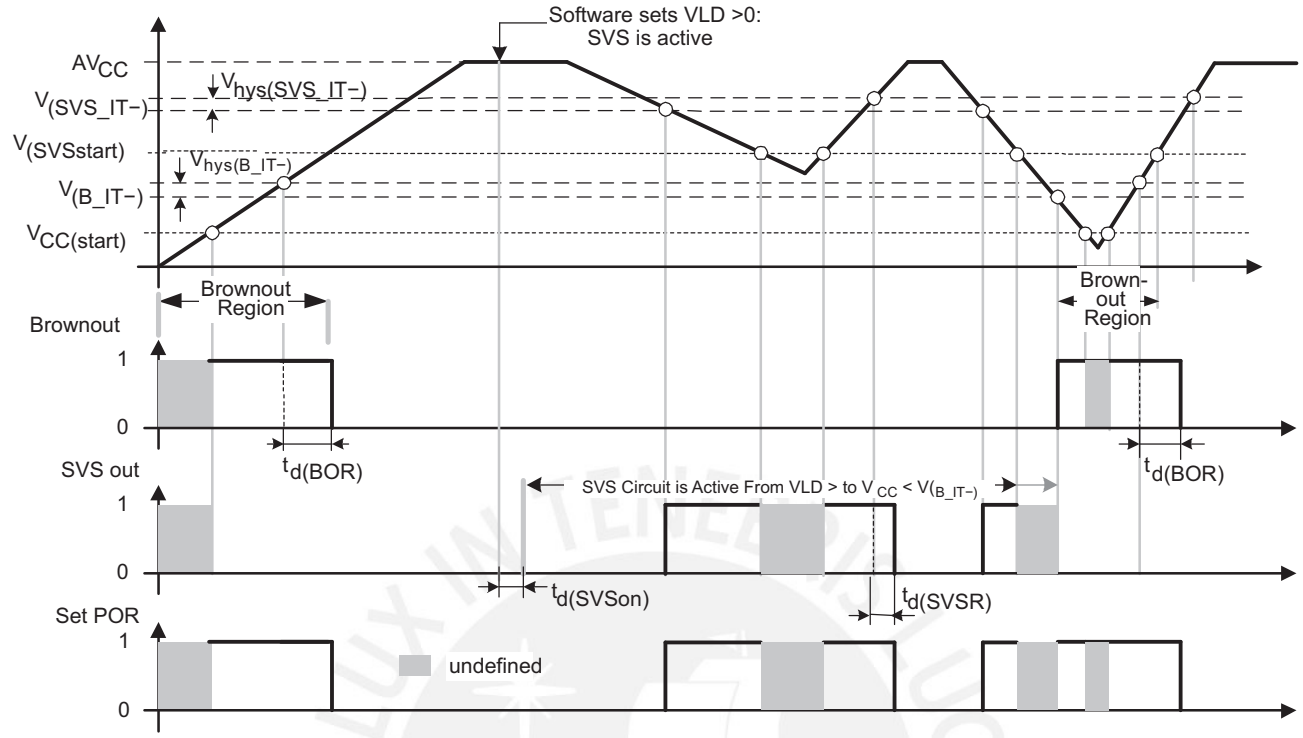


Figure 12. SVS Reset (SVSR) vs Supply Voltage

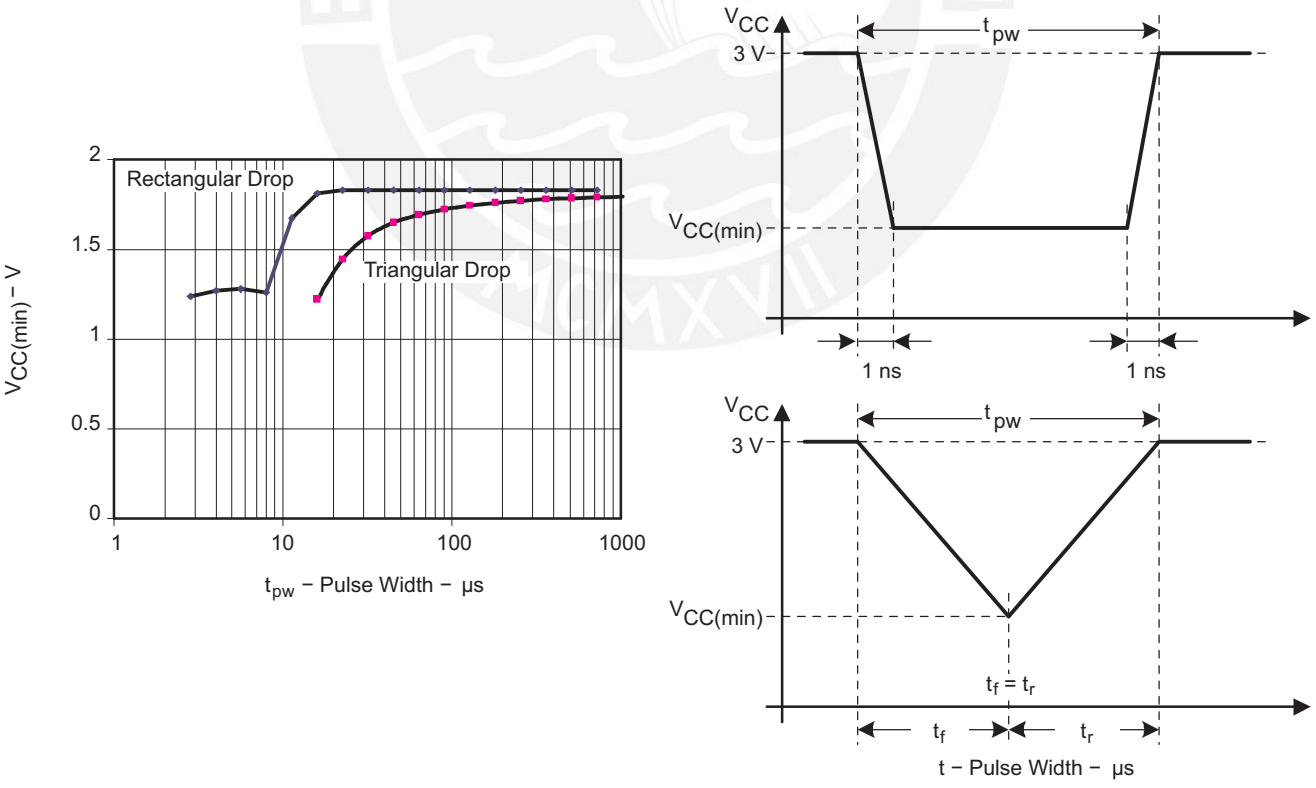


Figure 13. $V_{CC(min)}$: Square Voltage Drop and Triangle Voltage Drop to Generate an SVS Signal (VLD = 1)

Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	
		RSELx = 15		3.0		3.6	
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	2.2 V, 3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	2.2 V, 3 V	0.07		0.17	MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	2.2 V, 3 V	0.10		0.20	MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	2.2 V, 3 V	0.14		0.28	MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	2.2 V, 3 V	0.20		0.40	MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	2.2 V, 3 V	0.28		0.54	MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	2.2 V, 3 V	0.39		0.77	MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	2.2 V, 3 V	0.54		1.06	MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	2.2 V, 3 V	0.80		1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	2.2 V, 3 V	1.10		2.10	MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	2.2 V, 3 V	1.60		3.00	MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	2.2 V, 3 V	2.50		4.30	MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	2.2 V, 3 V	3.00		5.50	MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	2.2 V, 3 V	4.30		7.30	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	2.2 V, 3 V	6.00		9.60	MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	2.2 V, 3 V	8.60		13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V	12.0		18.5	MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V	16.0		26.0	MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$	2.2 V, 3 V			1.55	ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$	2.2 V, 3 V	1.05	1.08	1.12	ratio
	Duty cycle	Measured at P1.4/SMCLK	2.2 V, 3 V	40	50	60	%

Calibrated DCO Frequencies - Tolerance at Calibration

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	Frequency tolerance at calibration		25°C	3 V	-1	±0.2	+1	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	3 V	0.990	1	1.010	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	3 V	7.920	8	8.080	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	3 V	11.88	12	12.12	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V	15.84	16	16.16	MHz

Calibrated DCO Frequencies - Tolerance Over Temperature 0°C to 85°C

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	1-MHz tolerance over temperature		0°C to 85°C	3 V	-2.5	±0.5	+2.5	%
	8-MHz tolerance over temperature		0°C to 85°C	3 V	-2.5	±1.0	+2.5	%
	12-MHz tolerance over temperature		0°C to 85°C	3 V	-2.5	±1.0	+2.5	%
	16-MHz tolerance over temperature		0°C to 85°C	3 V	-3	±2.0	+3	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	0.970	1	1.030	MHz
				3 V	0.975	1	1.025	
				3.6 V	0.970	1	1.030	
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	7.760	8	8.40	MHz
				3 V	7.800	8	8.20	
				3.6 V	7.600	8	8.24	
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	0°C to 85°C	2.2 V	11.64	12	12.36	MHz
				3 V	11.64	12	12.36	
				3.6 V	11.64	12	12.36	
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	0°C to 85°C	3 V	15.52	16	16.48	MHz
				3.6 V	15.00	16	16.48	

Calibrated DCO Frequencies - Tolerance Over Supply Voltage V_{CC}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over V_{CC}			25°C	1.8 V to 3.6 V	-3	±2	+3	%
8-MHz tolerance over V_{CC}			25°C	1.8 V to 3.6 V	-3	±2	+3	%
12-MHz tolerance over V_{CC}			25°C	2.2 V to 3.6 V	-3	±2	+3	%
16-MHz tolerance over V_{CC}			25°C	3 V to 3.6 V	-6	±2	+3	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	0.97	1	1.03	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	25°C	1.8 V to 3.6 V	7.76	8	8.24	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	25°C	2.2 V to 3.6 V	11.64	12	12.36	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	25°C	3 V to 3.6 V	15	16	16.48	MHz

Calibrated DCO Frequencies - Overall Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
	1-MHz tolerance overall		-40°C to 105°C	1.8 V to 3.6 V	-5	±2	+5	%
	8-MHz tolerance overall		-40°C to 105°C	1.8 V to 3.6 V	-5	±2	+5	%
	12-MHz tolerance overall		-40°C to 105°C	2.2 V to 3.6 V	-5	±2	+5	%
	16-MHz tolerance overall		-40°C to 105°C	3 V to 3.6 V	-6	±3	+6	%
$f_{CAL(1MHz)}$	1-MHz calibration value	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, Gating time: 5 ms	-40°C to 105°C	1.8 V to 3.6 V	0.95	1	1.05	MHz
$f_{CAL(8MHz)}$	8-MHz calibration value	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, Gating time: 5 ms	-40°C to 105°C	1.8 V to 3.6 V	7.6	8	8.4	MHz
$f_{CAL(12MHz)}$	12-MHz calibration value	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, Gating time: 5 ms	-40°C to 105°C	2.2 V to 3.6 V	11.4	12	12.6	MHz
$f_{CAL(16MHz)}$	16-MHz calibration value	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, Gating time: 2 ms	-40°C to 105°C	3 V to 3.6 V	15	16	17	MHz

Typical Characteristics - Calibrated DCO Frequency

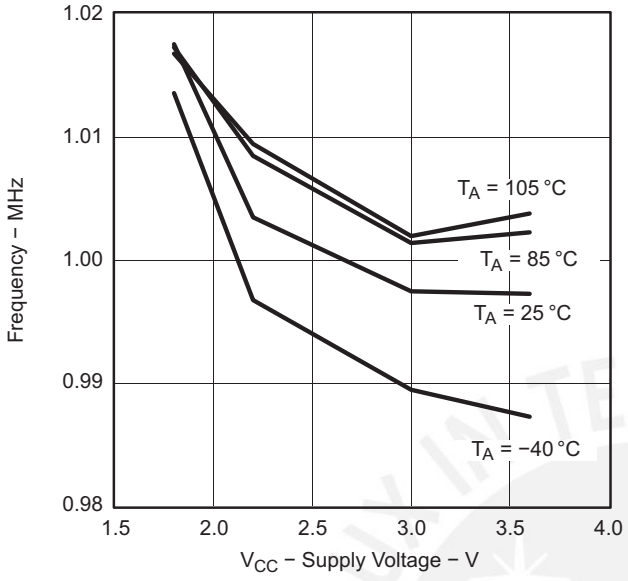


Figure 14.

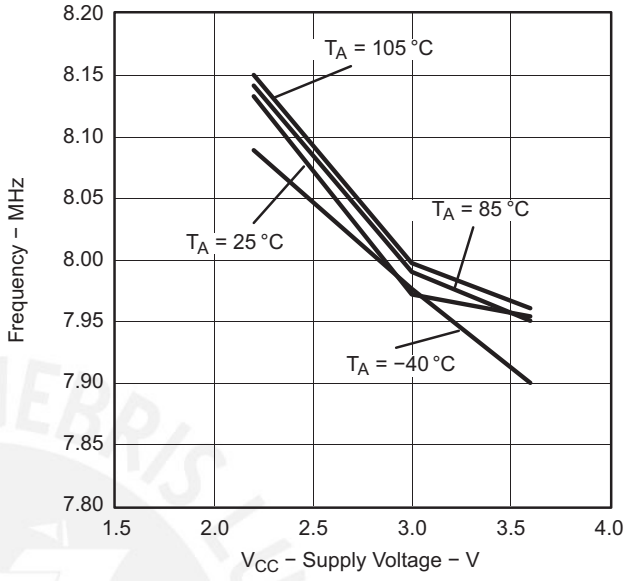


Figure 15.

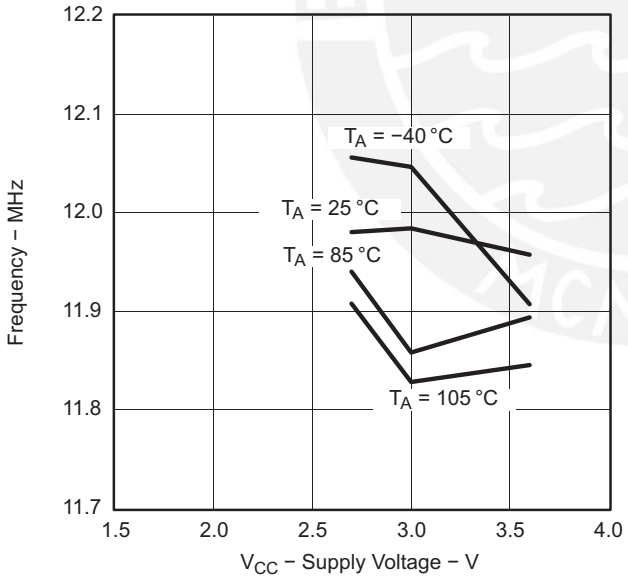


Figure 16.

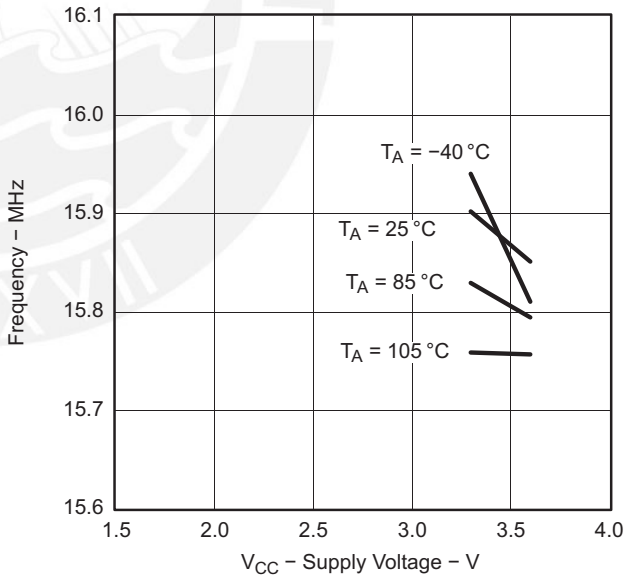


Figure 17.

Wake-Up From Lower-Power Modes (LPM3, LPM4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3 or LPM4 (1)	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ	2.2 V, 3 V			2	µs
		BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ				1.5	
		BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ				1	
		BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ	3 V			1	
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3 or LPM4 (2)				$1 / f_{MCLK}$ + $t_{Clock,LPM3/4}$		

(1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
(2) Parameter applicable only if DCOCLK is used for MCLK.

Typical Characteristics - DCO Clock Wake-Up Time From LPM3 or LPM4

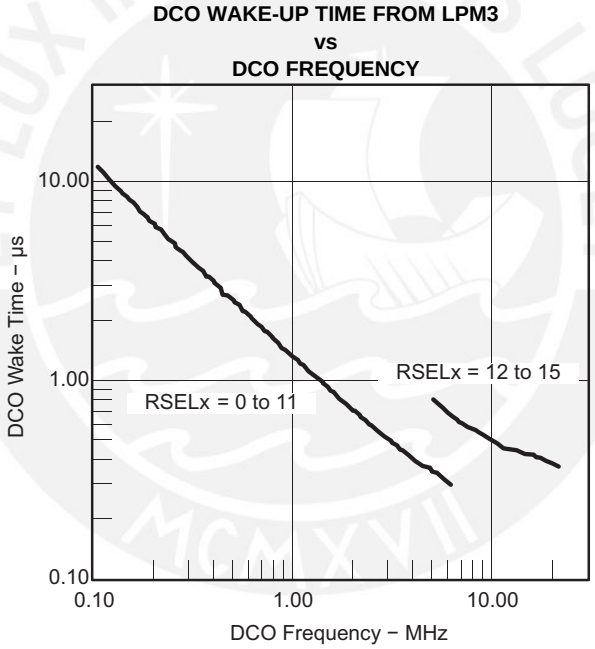


Figure 18.

DCO With External Resistor R_{OSC} (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
$f_{DCO,ROSC}$	DCO output frequency with R_{OSC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0, T_A = 25°C	2.2 V	1.8	MHz
			3 V	1.95	
D_T	Temperature drift	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V, 3 V	±0.1	%/°C
D_V	Drift with V_{CC}	DCOR = 1, RSELx = 4, DCOx = 3, MODx = 0	2.2 V, 3 V	10	%/V

(1) R_{OSC} = 100 kΩ. Metal film resistor, type 0257, 0.6 W with 1% tolerance and T_K = ±50 ppm/°C.

Typical Characteristics - DCO With External Resistor R_{OSC}

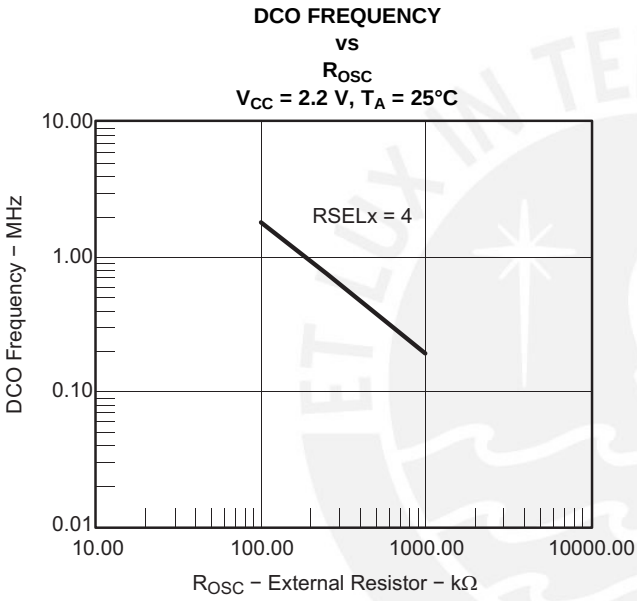


Figure 19.

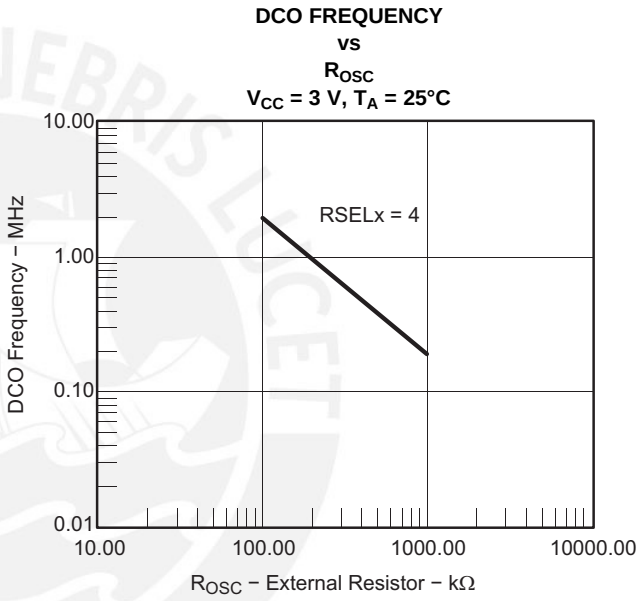


Figure 20.

Typical Characteristics - DCO With External Resistor R_{OSC} (continued)

DCO FREQUENCY vs TEMPERATURE
V_{CC} = 3 V

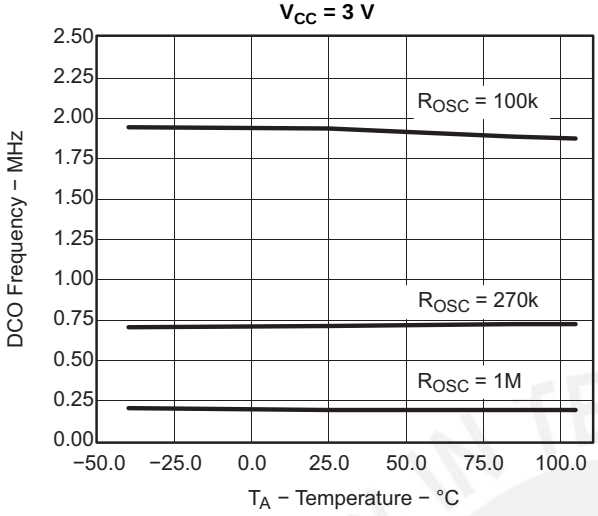


Figure 21.

DCO FREQUENCY vs SUPPLY VOLTAGE
T_A = 25°C

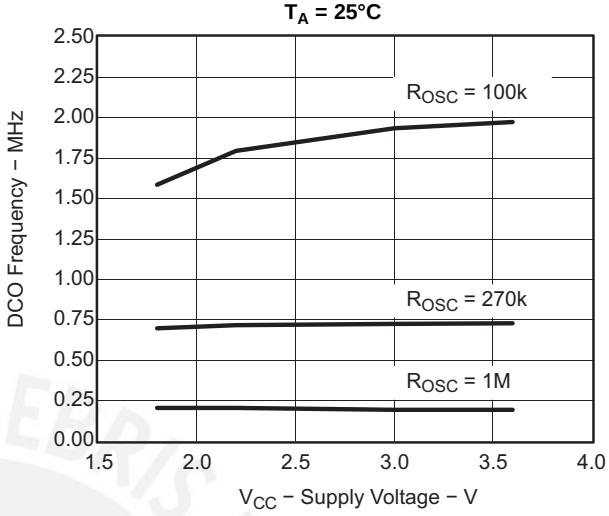


Figure 22.

Crystal Oscillator LFXT1, Low-Frequency Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, LFXT1Sx = 3, XCAPx = 0	1.8 V to 3.6 V	10000	32768	50000	Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			200		
$C_{L,eff}$	Integrated effective load capacitance, LF mode(2)	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			11		
	Duty cycle, LF mode	XTS = 0, Measured at P2.0/ACLK, $f_{LFXT1,LF}$ = 32768 Hz	2.2 V, 3 V	30	50	70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode(3)	XTS = 0, LFXT1Sx = 3, XCAPx = 0(4)	2.2 V, 3 V	10		10000	Hz

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
(a) Keep the trace between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
(g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the crystal that is used.

(3) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(4) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T_A	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	-40°C to 85°C	2.2 V, 3 V	4	12	20	kHz
		105°C				22	
df_{VLO}/dT	VLO frequency temperature drift(1)		2.2 V, 3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift(2)	25°C	1.8 V to 3.6 V		4		%/V

(1) Calculated using the box method:
I: (MAX(-40 to 85°C) - MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C - (-40°C))
T: (MAX(-40 to 105°C) - MIN(-40 to 105°C)) / MIN(-40 to 105°C) / (105°C - (-40°C))

(2) Calculated using the box method: (MAX(1.8 to 3.6 V) - MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V - 1.8 V)

Crystal Oscillator LFXT1, High-Frequency Mode(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,HF0}$	LFXT1 oscillator crystal frequency, HF mode 0	XTS = 1, LFXT1Sx = 0, XCAPx = 0	1.8 V to 3.6 V	0.4		1	MHz
$f_{LFXT1,HF1}$	LFXT1 oscillator crystal frequency, HF mode 1	XTS = 1, LFXT1Sx = 1, XCAPx = 0	1.8 V to 3.6 V	1		4	MHz
$f_{LFXT1,HF2}$	LFXT1 oscillator crystal frequency, HF mode 2	XTS = 1, LFXT1Sx = 2, XCAPx = 0	1.8 V to 3.6 V	2		10	MHz
			2.2 V to 3.6 V	2		12	
			3 V to 3.6 V	2		16	
$f_{LFXT1,HF,logic}$	LFXT1 oscillator logic-level square-wave input frequency, HF mode	XTS = 1, LFXT1Sx = 3, XCAPx = 0	1.8 V to 3.6 V	0.4		10	MHz
			2.2 V to 3.6 V	0.4		12	
			3 V to 3.6 V	0.4		16	
OA_{HF}	Oscillation allowance for HF crystals (see Figure 23 and Figure 24)	XTS = 1, XCAPx = 0, LFXT1Sx = 0, $f_{LFXT1,HF}$ = 1 MHz, $C_{L,eff}$ = 15 pF			2700		Ω
		XTS = 1, XCAPx = 0, LFXT1Sx = 1, $f_{LFXT1,HF}$ = 4 MHz, $C_{L,eff}$ = 15 pF			800		
		XTS = 1, XCAPx = 0, LFXT1Sx = 2, $f_{LFXT1,HF}$ = 16 MHz, $C_{L,eff}$ = 15 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, HF mode(2)	XTS = 1, XCAPx = 0(3)			1		pF
	Duty cycle, HF mode	XTS = 1, XCAPx = 0, Measured at P2.0/ACLK, $f_{LFXT1,HF}$ = 10 MHz	2.2 V, 3 V	40	50	60	%
		XTS = 1, XCAPx = 0, Measured at P2.0/ACLK, $f_{LFXT1,HF}$ = 16 MHz		40	50	60	
$f_{Fault,HF}$	Oscillator fault frequency(4)	XTS = 1, LFXT1Sx = 3, XCAPx = 0(5)	2.2 V, 3 V	30		300	kHz

(1) To improve EMI on the XT2 oscillator the following guidelines should be observed:
(a) Keep the trace between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
(g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(3) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(4) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.

(5) Measured with logic-level input frequency, but also applies to operation with crystals.

Typical Characteristics - LFXT1 Oscillator in HF Mode (XTS = 1)

OSCILLATION ALLOWANCE vs CRYSTAL FREQUENCY $C_{L,eff}$ = 15 pF, T_A = 25°C

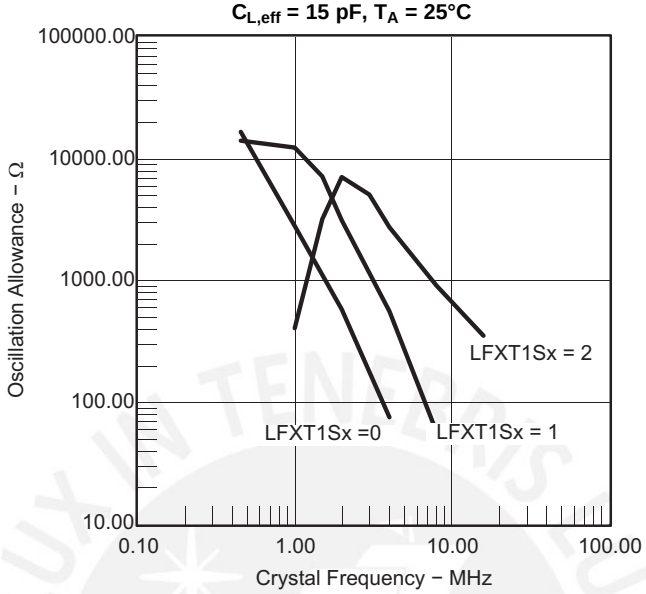


Figure 23.

OSCILLATOR SUPPLY CURRENT vs CRYSTAL FREQUENCY $C_{L,eff}$ = 15 pF, T_A = 25°C

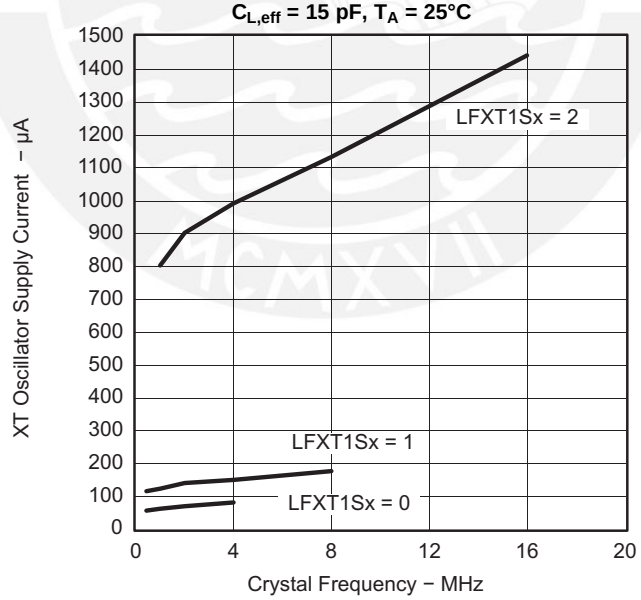


Figure 24.

Crystal Oscillator XT2[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{XT2}	XT2 oscillator crystal frequency, mode 0	XT2Sx = 0	1.8 V to 3.6 V	0.4		1	MHz
f_{XT2}	XT2 oscillator crystal frequency, mode 1	XT2Sx = 1	1.8 V to 3.6 V	1		4	MHz
f_{XT2}	XT2 oscillator crystal frequency, mode 2	XT2Sx = 2	1.8 V to 2.2 V	2		10	MHz
			2.2 V to 3.6 V	2		12	
			3 V to 3.6 V	2		16	
f_{XT2}	XT2 oscillator logic-level square-wave input frequency	XT2Sx = 3	1.8 V to 2.2 V	0.4		10	MHz
			2.2 V to 3.6 V	0.4		12	
			3 V to 3.6 V	0.4		16	
OA	Oscillation allowance (see Figure 25 and Figure 26)	XT2Sx = 0, f_{XT2} = 1 MHz, $C_{L,eff}$ = 15 pF			2700		Ω
		XT2Sx = 1, f_{XT2} = 4 MHz, $C_{L,eff}$ = 15 pF			800		
		XT2Sx = 2, f_{XT2} = 16 MHz, $C_{L,eff}$ = 15 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, HF mode[2]	See [3]			1		pF
	Duty cycle	Measured at P1.4/SMCLK, f_{XT2} = 10 MHz	2.2 V, 3 V	40	50	60	%
		Measured at P1.4/SMCLK, f_{XT2} = 16 MHz		40	50	60	
f_{Fault}	Oscillator fault frequency, HF mode[4]	XT2Sx = 3[5]	2.2 V, 3 V	30		300	kHz

(1) To improve EMI on the XT2 oscillator the following guidelines should be observed:
(a) Keep the trace between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
(d) Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(3) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(4) Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.

(5) Measured with logic-level input frequency, but also applies to operation with crystals.

Typical Characteristics - XT2 Oscillator

OSCILLATION ALLOWANCE vs CRYSTAL FREQUENCY
$C_{L,eff}$ = 15 pF, T_A = 25°C

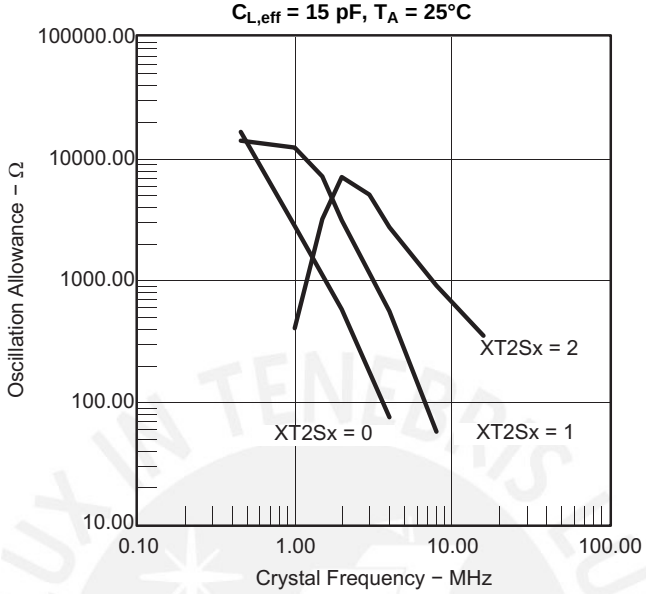


Figure 25.

OSCILLATOR SUPPLY CURRENT vs CRYSTAL FREQUENCY
$C_{L,eff}$ = 15 pF, T_A = 25°C

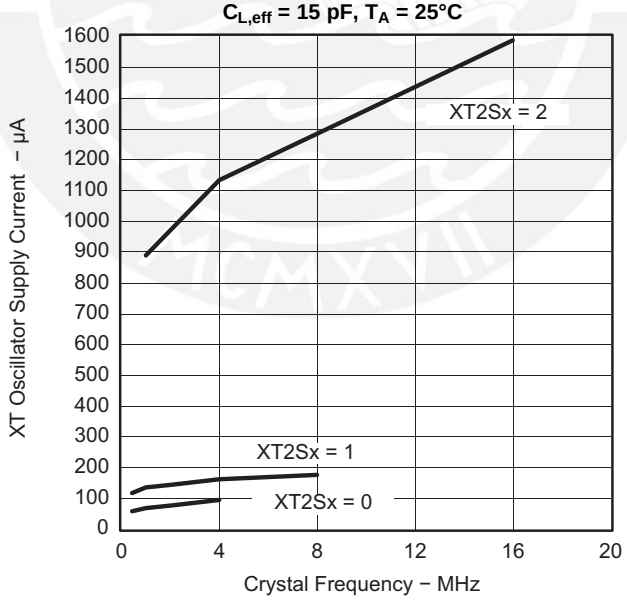


Figure 26.

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK, ACLK External: TACLK, INCLK Duty cycle = 50% ± 10%	2.2 V			10	MHz
			3 V			16	
$t_{TA,cap}$	Timer_A capture timing	TA0, TA1, TA2	2.2 V, 3 V	20			ns

Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TB}	Timer_B clock frequency	Internal: SMCLK, ACLK External: TACLK, INCLK Duty cycle = 50% ± 10%	2.2 V			10	MHz
			3 V			16	
$t_{TB,cap}$	Timer_B capture timing	TB0, TB1, TB2	2.2 V, 3 V	20			ns

USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)(1)		2.2 V, 3 V			1	MHz
t_τ	UART receive deglitch time(2)		2.2 V	50	150	600	ns
			3 V	50	100	600	

(1) The DCO wake-up time must be considered in LPM3 or LPM4 for baud rates above 1 MHz.
(2) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed.

USCI (SPI Master Mode)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see Figure 27 and Figure 28)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK Duty cycle = 50% ± 10%			f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time		2.2 V	110		ns
			3 V	75		
$t_{HD,MI}$	SOMI input data hold time		2.2 V	0		ns
			3 V	0		
$t_{VALID,MO}$	SIMO output data valid time	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V		30	ns
			3 V		20	

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

USCI (SPI Slave Mode)(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see Figure 29 and Figure 30)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock		2.2 V, 3 V		50		ns
$t_{STE,LAG}$	STE lag time, Last clock to STE high		2.2 V, 3 V	10			ns
$t_{STE,ACC}$	STE access time, STE low to SOMI data out		2.2 V, 3 V		50		ns
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance		2.2 V, 3 V		50		ns
$t_{SU,SI}$	SIMO input data setup time		2.2 V	20			ns
			3 V	15			
$t_{HD,SI}$	SIMO input data hold time		2.2 V	10			ns
			3 V	10			
$t_{VALID,SO}$	SOMI output data valid time	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V		75	110	ns
			3 V		50	75	

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.
For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ see the SPI parameters of the attached slave.

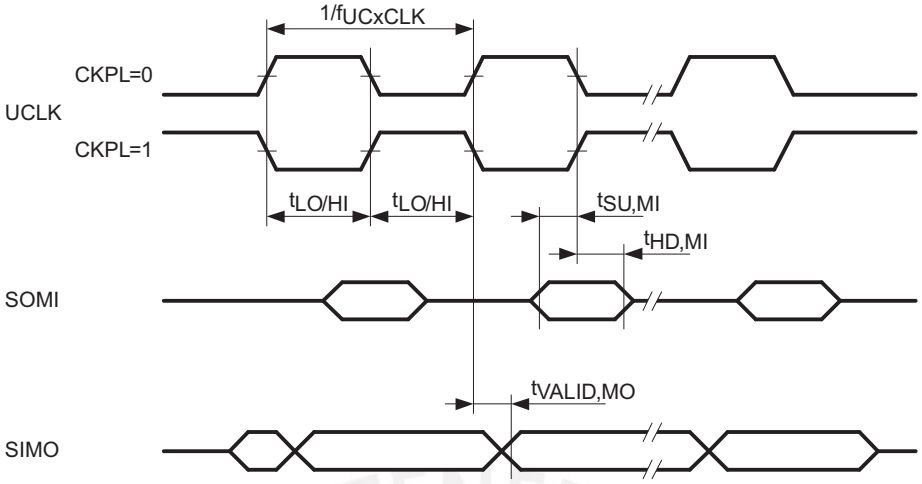


Figure 27. SPI Master Mode, CKPH = 0

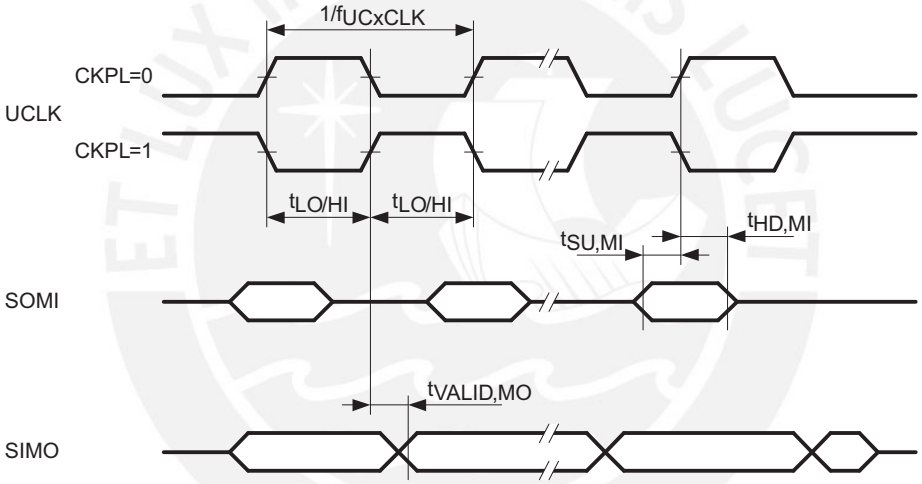


Figure 28. SPI Master Mode, CKPH = 1

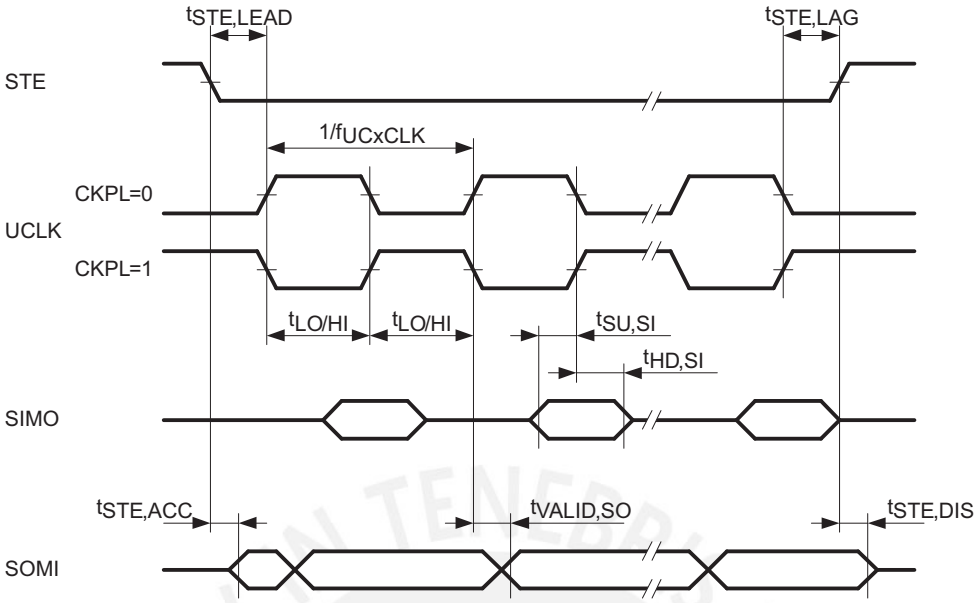


Figure 29. SPI Slave Mode, CKPH = 0

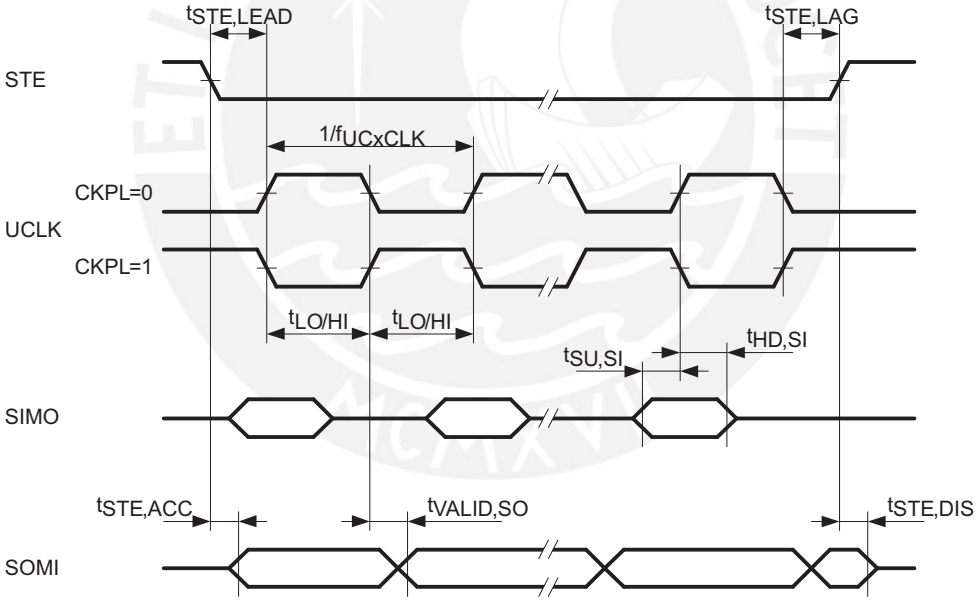


Figure 30. SPI Slave Mode, CKPH = 1

USCI (I^2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 31)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V, 3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		2.2 V, 3 V	0			ns
$t_{SU,DAT}$	Data setup time		2.2 V, 3 V	250			ns
$t_{SU,STO}$	Setup time for STOP		2.2 V, 3 V	4			µs
t_{SP}	Pulse duration of spikes suppressed by input filter		2.2 V	50	150	600	ns
			3 V	50	100	600	

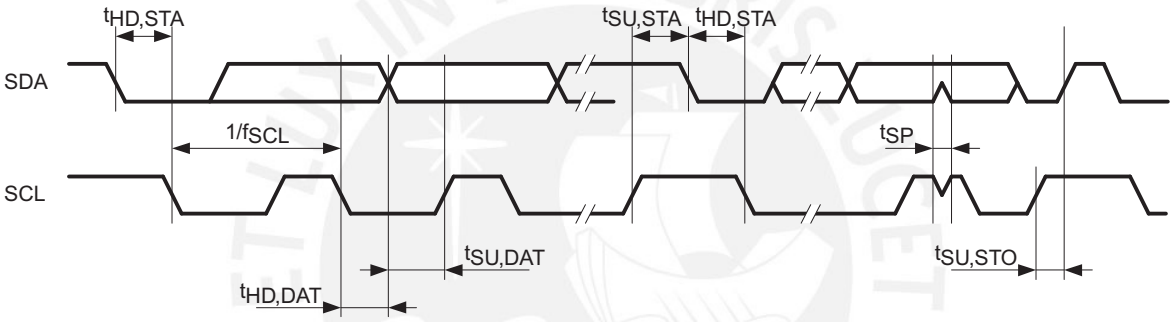


Figure 31. I^2C Mode Timing

Comparator_A+ (1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON = 1, CARSEL = 0, CAREF = 0	2.2 V		25	40	µA
			3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON = 1, CARSEL = 0, CAREF = 1/2/3, No load at P2 3/CA0/TA1 and P2.4/CA1/TA2	2.2 V		30	50	µA
			3 V		45	71	
V_{IC}	Common-mode input voltage range	CAON = 1	2.2 V, 3 V	0		V_{CC} - 1	V
$V_{(Ref025)}$	(Voltage at 0.25 V_{CC} node) ÷ V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P2 3/CA0/TA1 and P2.4/CA1/TA2	2.2 V, 3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	(Voltage at 0.5 V_{CC} node) ÷ V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P2 3/CA0/TA1 and P2.4/CA1/TA2	2.2 V, 3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	See Figure 35 and Figure 36	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P2 3/CA0/TA1 and P2.4/CA1/TA2, T_A = 85°C	2.2 V	390	480	540	mV
			3 V	400	490	550	
$V_{(offset)}$	Offset voltage (2)		2.2 V, 3 V	-30		30	mV
V_{hys}	Input hysteresis	CAON = 1	2.2 V, 3 V	0	0.7	1.4	mV
$t_{(response)}$	Response time, low to high and high to low (3) (see Figure 32 and Figure 33)	T_A = 25°C, Overdrive 10 mV, Without filter: CAF = 0	2.2 V	80	165	300	ns
			3 V	70	120	240	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF = 1	2.2 V	1.4	1.9	2.8	µs
			3 V	0.9	1.5	2.2	

(1) The leakage current for the Comparator_A+ terminals is identical to $I_{lkg(Px.y)}$ specification.
(2) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.
(3) The response time is measured at P2.2/CAOUT/TA0/CA4 with an input voltage step and with Comparator_A+ already enabled (CAON = 1). If CAON is set at the same time, a settling time of up to 300 ns is added to the response time.

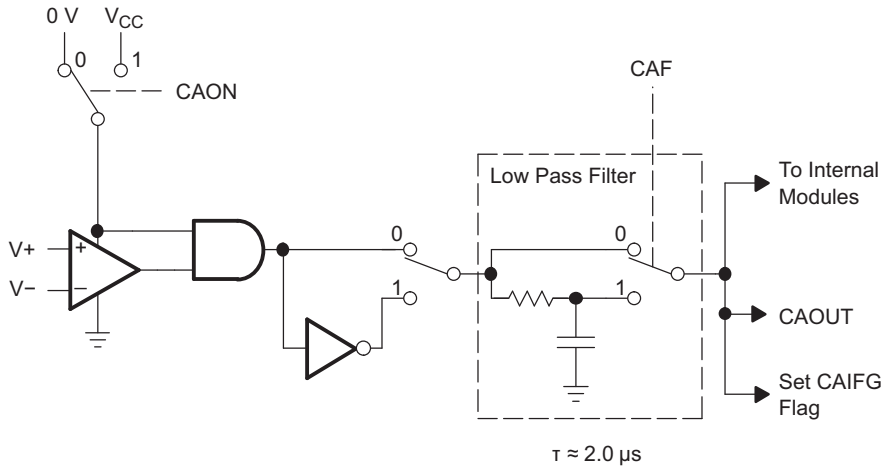


Figure 32. Comparator_A+ Module Block Diagram

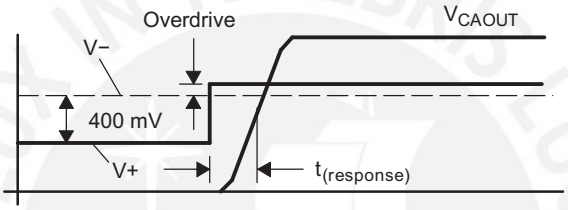


Figure 33. Overdrive Definition

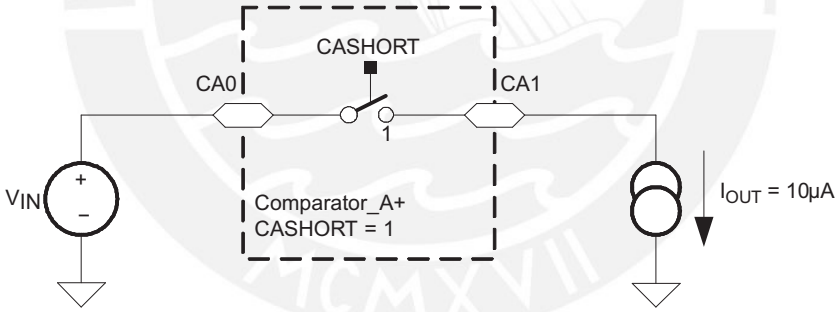


Figure 34. Comparator_A+ Short Resistance Test Condition

Typical Characteristics, Comparator_A+

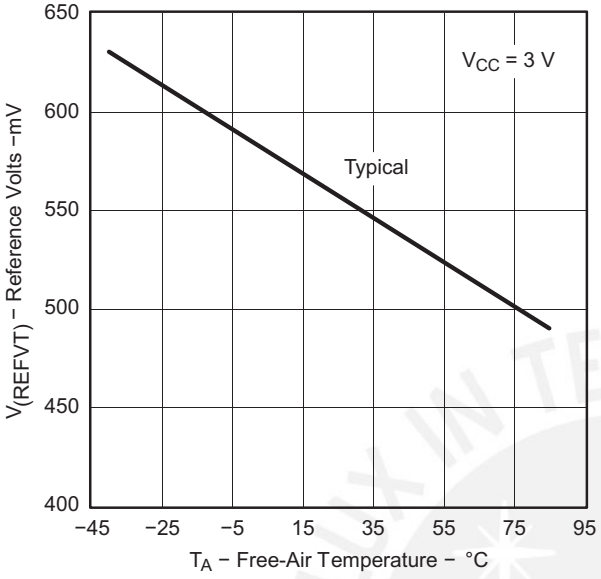


Figure 35.

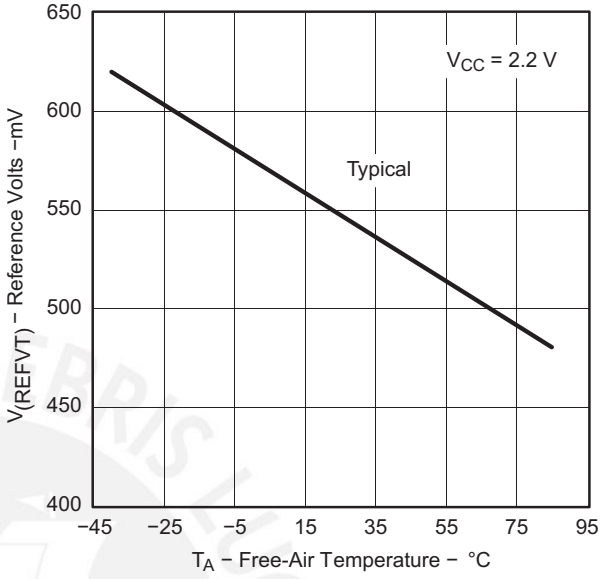


Figure 36.

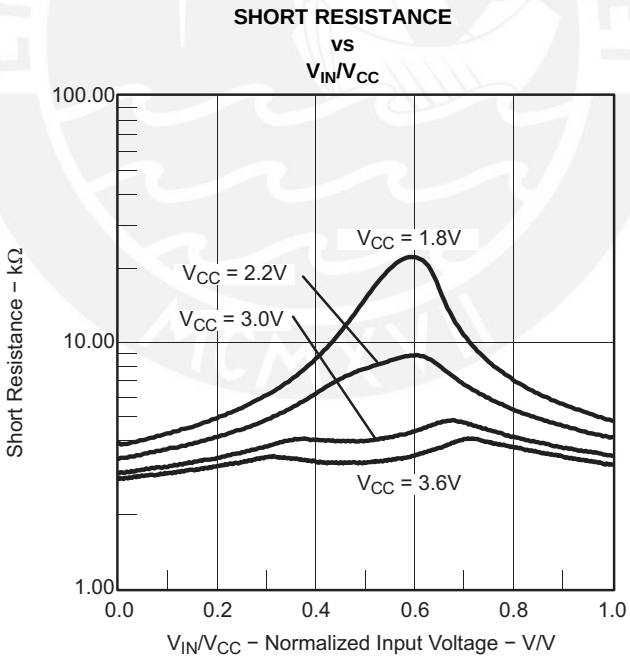


Figure 37.

12-Bit ADC Power Supply and Input Range Conditions (1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together, AV_{SS} and DV_{SS} are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(P6.x/Ax)}$	Analog input voltage range(2)	All P6.0/A0 to P6.7/A7 terminals, Analog inputs selected in ADC12MCTLx register, P6Sel.x = 1, 0 ≤ × ≤ 7, $V_{(AVSS)} \le V_{P6.x/Ax} \le V_{(AVCC)}$		0		V_{AVCC}	V
I_{ADC12}	Operating supply current into AV_{CC} terminal(3)	$f_{ADC12CLK}$ = 5 MHz, ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0	2.2 V		0.65	0.8	mA
			3 V		0.8	1	
I_{REF+}	Operating supply current into AV_{CC} terminal(4)	$f_{ADC12CLK}$ = 5 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 1	3 V		0.5	0.7	mA
		$f_{ADC12CLK}$ = 5 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 0	2.2 V		0.5	0.7	mA
			3 V		0.5	0.7	
C_I	Input capacitance(5)	Only one terminal can be selected at one time, P6.x/Ax	2.2 V			40	pF
R_I	Input MUX ON resistance(5)	0 V ≤ V_{Ax} ≤ V_{AVCC}	3 V			2000	Ω

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC12}.
(4) The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables settling of the built-in reference before starting an A/D conversion.
(5) Not production tested, limits verified by design.

12-Bit ADC External Reference(1)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (2)		1.4	V_{AVCC}	V
V_{REF-}/V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (3)		0	1.2	V
(V_{eREF+} - V_{REF-} /V_{eREF-})	Differential external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (4)		1.4	V_{AVCC}	V
I_{VeREF+}	Static leakage current	0 V ≤ V_{eREF+} ≤ V_{AVCC}	2.2 V, 3 V		±1	µA
$I_{VREF-/VeREF-}$	Static leakage current	0 V ≤ V_{eREF-} ≤ V_{AVCC}	2.2 V, 3 V		±1	µA

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

12-Bit ADC Built-In Reference

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	NOM	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REF2_5V = 1 for 2.5 V, I_{VREF+}max ≤ I_{VREF+} ≤ I_{VREF+}min	-40°C to 85°C	3 V	2.4	2.5	2.6	V
			105°C		2.37	2.5	2.64	
		REF2_5V = 0 for 1.5 V, I_{VREF+}max ≤ I_{VREF+} ≤ I_{VREF+}min	-40°C to 85°C	2.2 V, 3 V	1.44	1.5	1.56	
			105°C		1.42	1.5	1.57	
$AV_{CC(min)}$	AV_{CC} minimum voltage, positive built-in reference active	REF2_5V = 0, I_{VREF+}max ≤ I_{VREF+} ≤ I_{VREF+}min			2.2			V
		REF2_5V = 1, -0.5 mA ≤ I_{VREF+} ≤ I_{VREF+}min			2.8			
		REF2_5V = 1, -1 mA ≤ I_{VREF+} ≤ I_{VREF+}min			2.9			
I_{VREF+}	Load current out of V_{REF+}terminal			2.2 V	0.01		-0.5	mA
				3 V	0.01		-1	
$I_{L(VREF)+}$	Load-current regulation, V_{REF+} terminal (1)	I_{VREF+} = 500 µA ± 100 µA, Analog input voltage ≈ 0.75 V, REF2_5V = 0		2.2 V			±2	LSB
				3 V			±2	
		I_{VREF+} = 500 µA ± 100 µA, Analog input voltage ≈ 1.25 V, REF2_5V = 1		3 V			±2	LSB
$I_{DL(VREF)+}$	Load current regulation, V_{REF+} terminal (2)	I_{VREF+} = 100 µA → 900 µA, C_{VREF+} = 5 µF, ax ≈ 0.5 × V_{REF+}, Error of conversion result ≤ 1 LSB		3 V			20	ns
C_{VREF+}	Capacitance at pin V_{REF+} (3)	REFON = 1, 0 mA ≤ I_{VREF+} ≤ I_{VREF+}max		2.2 V, 3 V	5	10		µF
T_{REF+}	Temperature coefficient of built-in reference (2)	I_{VREF+} is a constant in the range of 0 mA ≤ I_{VREF+} ≤ 1 mA		2.2 V, 3 V			±100	ppm/°C
t_{REFON}	Settle time of internal reference voltage (see Figure 38) (4) (2)	I_{VREF+} = 0.5 mA, C_{VREF+} = 10 µF, V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V		2.2 V			17	ms

(1) Not production tested, limits characterized.
(2) Not production tested, limits verified by design.
(3) The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests uses two capacitors between pins V_{REF+} and AV_{SS} and V_{REF-}/V_{eREF-} and AV_{SS}: 10 µF tantalum and 100 nF ceramic.
(4) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load.

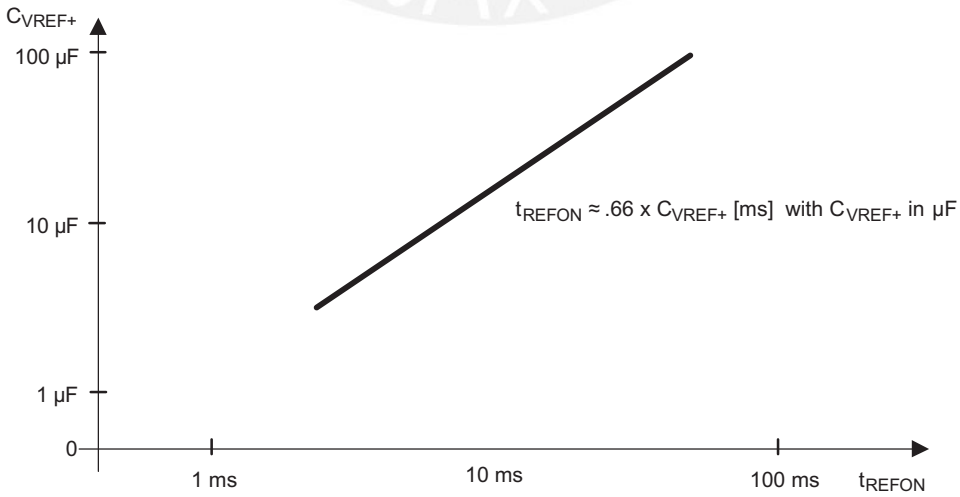


Figure 38. Typical Settling Time of Internal Reference t_{REFON} vs External Capacitor on V_{REF+}

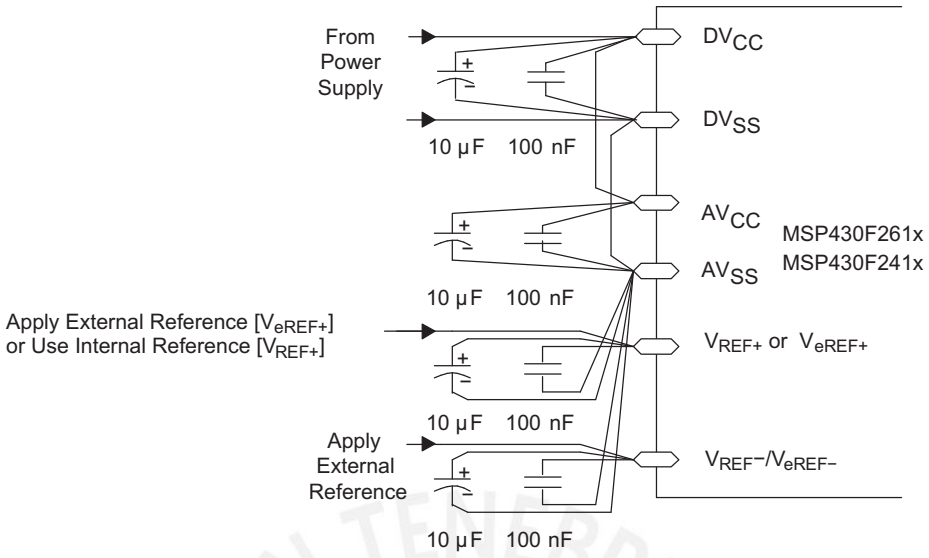


Figure 39. Supply Voltage and Reference Voltage Design V_{REF-}/V_{eREF-} External Supply

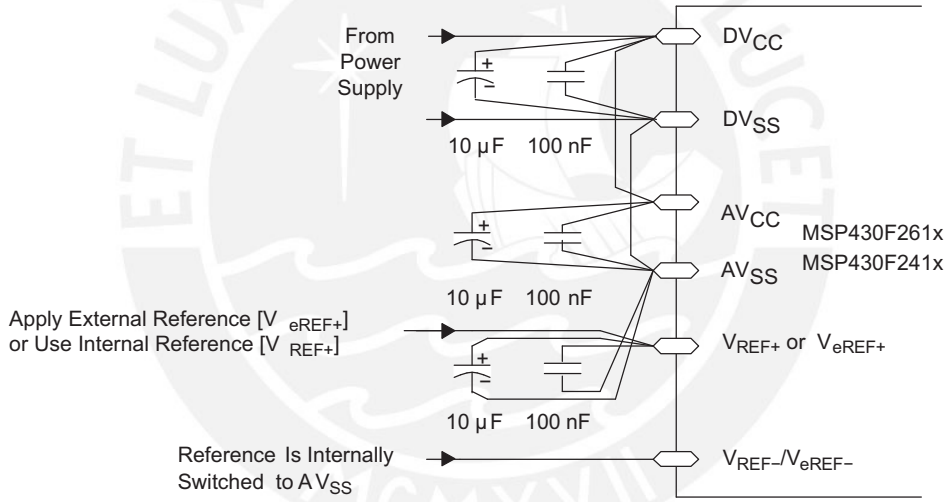


Figure 40. Supply Voltage and Reference Voltage Design V_{REF-}/V_{eREF-}= AV_{SS}, Internally Connected

12-Bit ADC Timing Parameters

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$		For specified performance of ADC12 linearity parameters	2.2 V, 3 V	0.45	5	6.3	MHz
$f_{ADC12OSC}$	Internal ADC12 oscillator	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$	2.2 V, 3 V	3.7	5	6.3	MHz
$t_{CONVERT}$	Conversion time	$C_{VREF+} \geq 5$ µF, Internal oscillator, $f_{ADC12OSC}$ = 3.7 MHz to 6.3 MHz	2.2 V, 3 V	2.06		3.51	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0			13 × ADC12DIV × $1/f_{ADC12CLK}$		µs
$t_{ADC12ON}$	Turn-on settling time of the ADC (1)	See (2)				100	ns
t_{Sample}	Sampling time (1)	R_S = 400 Ω, R_I = 1000 Ω, C_I = 30 pF, $\tau = [R_S + R_I] \times C_I$ (3)	3 V	1220			ns
			2.2 V	1400			

(1) Limits verified by design
(2) The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(3) Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns, where n = ADC resolution = 12, R_S = external source resistance

12-Bit ADC Linearity Parameters

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error	1.4 V ≤ (V_{eREF+} - V_{REF-}/V_{eREF-}) min ≤ 1.6 V	2.2 V, 3 V			±2	LSB
		1.6 V < (V_{eREF+} - V_{REF-}/V_{eREF-}) min ≤ V_{AVCC}				±1.7	
E_D	Differential linearity error	(V_{eREF+} - V_{REF-}/V_{eREF-}) min ≤ (V_{eREF+} - V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V			±1	LSB
E_O	Offset error	(V_{eREF+} - V_{REF-}/V_{eREF-}) min ≤ (V_{eREF+} - V_{REF-}/V_{eREF-}), Internal impedance of source RS < 100 Ω, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V		±2	±4	LSB
E_G	Gain error	(V_{eREF+} - V_{REF-}/V_{eREF-}) min ≤ (V_{eREF+} - V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V		±1.1	±2	LSB
E_T	Total unadjusted error	(V_{eREF+} - V_{REF-}/V_{eREF-}) min ≤ (V_{eREF+} -V_{REF-}/V_{eREF-}), C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V		±2	±5	LSB

12-Bit ADC Temperature Sensor and Built-In V_{MID}

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal (1)	REFON = 0, INCH = 0Ah, ADC12ON = 1, T_A = 25°C	2.2 V		40	120	µA
			3V		60	160	
V_{SENSOR} (2) (3)		ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		986		mV
			3V		986		
TC_{SENSOR} (3)		ADC12ON = 1, INCH = 0Ah	2.2 V		3.55		mV/°C
			3V		3.55		
$t_{SENSOR(sample)}$ (3)	Sample time required if channel 10 is selected (4)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30			µs
			3V	30			
I_{VMID}	Current into divider at channel 11 (5)	ADC12ON = 1, INCH = 0Bh	2.2 V			NA (5)	µA
			3V			NA (5)	
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, V_{MID} is approximately 0.5 × V_{AVCC}	2.2 V		1.1	1.1 ± 0.04	V
			3V		1.5	1.5 ± 0.04	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (6)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			

(1) The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON = 1), or (ADC12ON = 1 AND INCH = 0Ah and sample signal is high). Therefore it includes the constant current through the sensor and the reference.
(2) The temperature sensor offset can be as much as ±20°C. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor.
(3) Limits characterized
(4) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$
(5) No additional current is needed. The V_{MID} is used during sampling.
(6) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$, no additional on time is needed.

12-Bit DAC Supply Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} = DV_{CC}, AV_{SS} = DV_{SS} = 0 V			2.2		3.6	V
I_{DD}	Supply current, single DAC channel (1) (2)	DAC12AMPx = 2, DAC12IR = 0, DAC12_xDAT = 0x0800	2.2 V, 3 V	-40°C to 85°C		50	110	µA
				105°C		69	150	
		DAC12AMPx = 2, DAC12IR = 1, DAC12_xDAT = 0x0800, V_{eREF+} = V_{REF+} = AV_{CC}	2.2 V, 3 V			50	130	
		DAC12AMPx = 5, DAC12IR = 1, DAC12_xDAT = 0x0800, V_{eREF+} = V_{REF+}= AV_{CC}	2.2 V, 3 V			200	440	
		DAC12AMPx = 7, DAC12IR = 1, DAC12_xDAT = 0x0800, V_{eREF+} = V_{REF+} = AV_{CC}	2.2 V, 3 V			700	1500	
PSRR	Power-supply rejection ratio (3) (4)	DAC12_xDAT = 800h, V_{REF} = 1.5 V, ΔAV_{CC} = 100 mV	2.2 V			70		dB
		DAC12_xDAT = 800h, V_{REF} = 1.5 V or 2.5 V, ΔAV_{CC} = 100 mV	3 V			70		

(1) No load at the output pin, DAC12_0 or DAC12_1, assuming that the control bits for the shared pins are set properly.
(2) Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications.
(3) PSRR = 20 × log(ΔAV_{CC}/ΔV_{DAC12_xOUT})
(4) V_{REF} is applied externally. The internal reference is not used.

12-Bit DAC Linearity Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
	Resolution	12-bit monotonic		12			bits
INL	Integral nonlinearity(1)	V_{REF} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V		±2.0	±8.0	LSB
		V_{REF} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V				
DNL	Differential nonlinearity(1)	V_{REF} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V		±0.4	±1.0	LSB
		V_{REF} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V				
E_O	Offset voltage without calibration(1)(2)	V_{REF} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V			±21	mV
		V_{REF} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V				
	Offset voltage with calibration(1)(2)	V_{REF} = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V			±2.5	
		V_{REF} = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V				
$d_{E(O)}/d_T$	Offset error temperature coefficient(3)		2.2 V, 3 V		30		µV/C
E_G	Gain error(3)	V_{REF} = 1.5 V	2.2 V			±3.50	% FSR
		V_{REF} = 2.5 V	3 V				
$d_{E(G)}/d_T$	Gain temperature coefficient(3)		2.2 V, 3 V		10		ppm of FSR/°C
t_{Offset_Cal}	Time for offset calibration(4)	DAC12AMPx = 2	2.2 V, 3 V			100	ms
		DAC12AMPx = 3, 5				32	
		DAC12AMPx = 4, 6, 7				6	

(1) Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients "a" and "b" of the first-order equation: y = a + b × x. VDAC12_xOUT = E_O + (1 + E_G) × (V_{eREF+}/4095) × DAC12_xDAT, DAC12IR = 1.
(2) The offset calibration works on the output operational amplifier. Offset calibration is triggered setting bit DAC12CALON.
(3) Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients "a" and "b" of the first-order equation: y = a + b × x. VDAC12_xOUT = E_O + (1 + E_G) × (V_{eREF+}/4095) × DAC12_xDAT, DAC12IR = 1.
(4) The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx= {0, 1}. The DAC12 module should be configured prior to initiating calibration. Port activity during calibration may affect accuracy and is not recommended.

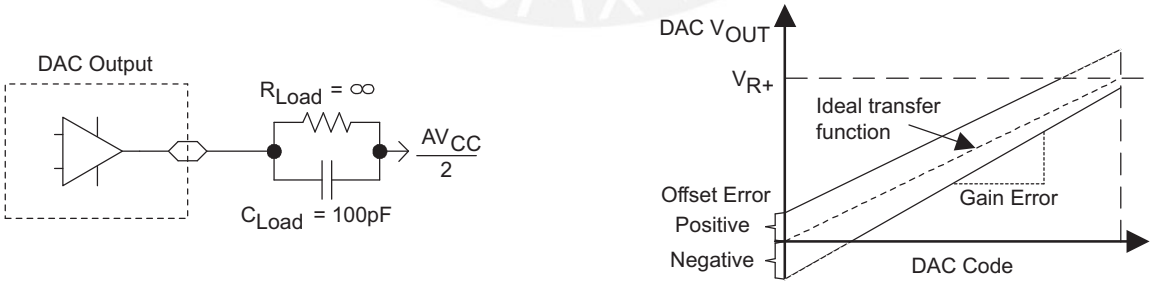


Figure 41. Linearity Test Load Conditions and Gain/Offset Definition

Typical Characteristics - 12-Bit DAC, Linearity Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TYPICAL INL ERROR vs DIGITAL INPUT DATA

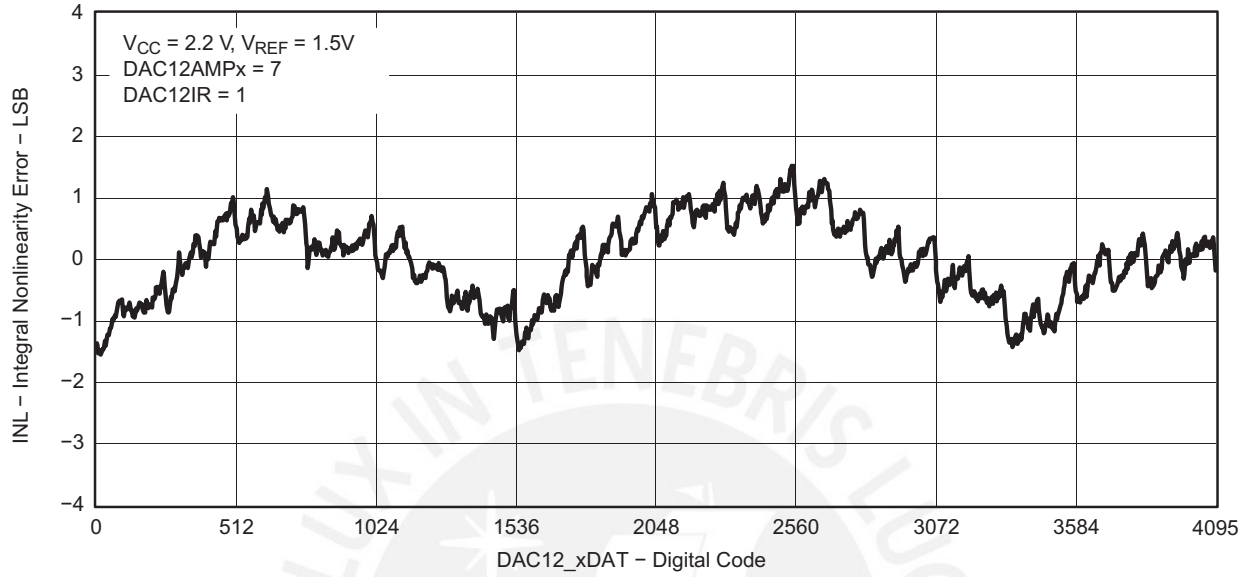


Figure 42.

TYPICAL DNL ERROR vs DIGITAL INPUT DATA

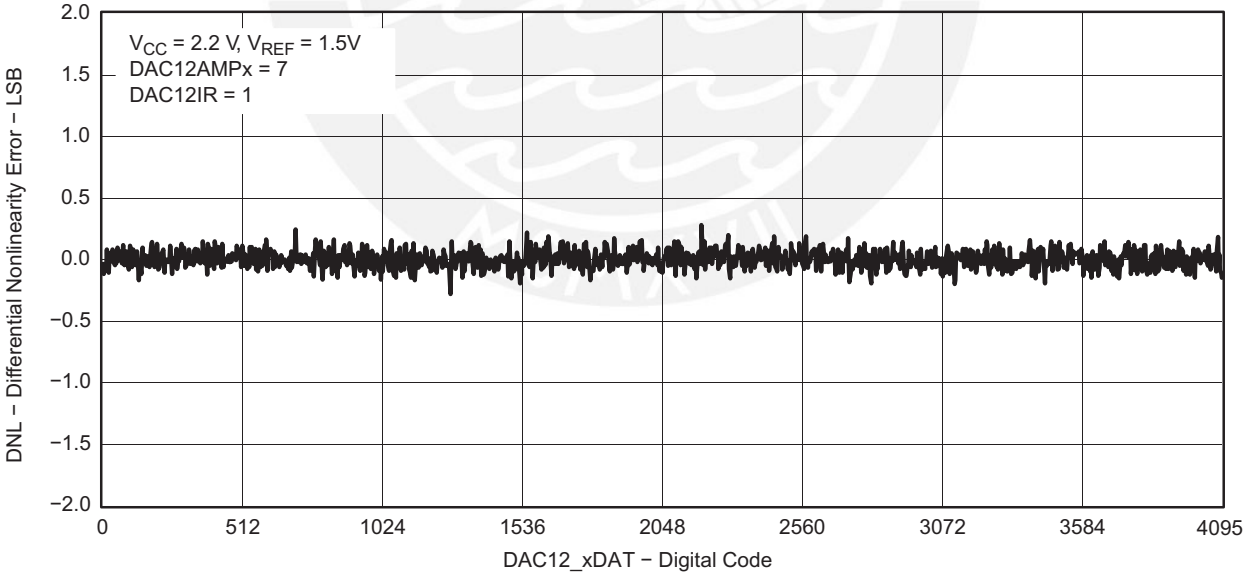


Figure 43.

12-Bit DAC Output Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_O	Output voltage range(1) (see Figure 44)	No Load, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2 V, 3 V	0		0.005	V
		No Load, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC} - 0.05		AV_{CC}	
		R_{Load} = 3 kΩ, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7		0		0.1	
		R_{Load} = 3 kΩ, $V_{eREF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC} - 0.13		AV_{CC}	
$C_{L(DAC12)}$	Maximum DAC12 load capacitance		2.2 V, 3 V			100	pF
$I_{L(DAC12)}$	Maximum DAC12 load current		2.2 V	-0.5		0.5	mA
			3 V	-1		1	
$R_{O/P(DAC12)}$	Output resistance (see Figure 44)	R_{Load} = 3 kΩ, $V_{O/P(DAC12)}$ = 0 V, DAC12AMPx = 7, DAC12_xDAT = 0h	2.2 V, 3 V		150	250	Ω
		R_{Load} = 3 kΩ, $V_{O/P(DAC12)} = AV_{CC}$, DAC12AMPx = 7, DAC12_xDAT = 0FFFh			150	250	
		R_{Load} = 3 kΩ, 0.3 V < $V_{O/P(DAC12)}$ < AV_{CC} - 0.3 V, DAC12AMPx = 7			1	4	

(1) Data is valid after the offset calibration of the output amplifier.

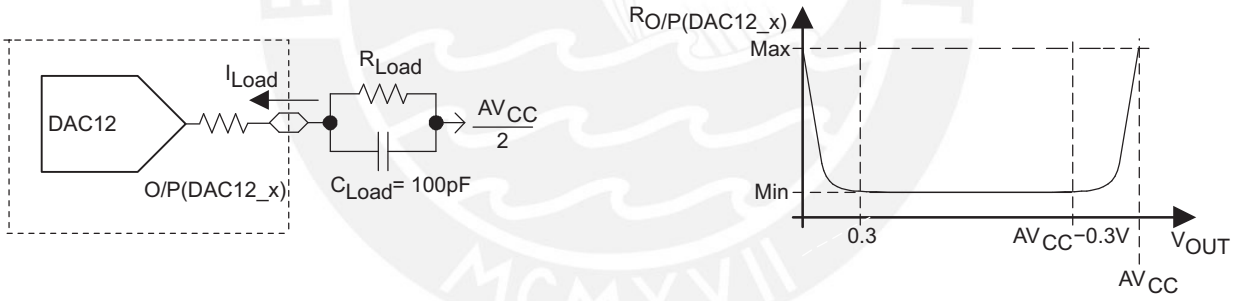


Figure 44. DAC12_x Output Resistance Tests

12-Bit DAC Reference Input Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{eREF+}	Reference input voltage range	DAC12IR = 0(1)(2)	2.2 V, 3 V		AV_{CC} / 3	AV_{CC} + 0.2	V
		DAC12IR = 1(3)(4)			AV_{CC}	AV_{CC} + 0.2	
$R_{i(VREF+)}$, $R_{i(VeREF+)}$	Reference input resistance	DAC12_0 IR = DAC12_1 IR = 0	2.2 V, 3 V	20			MΩ
		DAC12_0 IR = 1, DAC12_1 IR = 0		40	48	56	kΩ
		DAC12_0 IR = 0, DAC12_1 IR = 1					
		DAC12_0 IR = DAC12_1 IR = 1, DAC12_0 SREFx = DAC12_1 SREFx(5)		20	24	28	

(1) For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV_{CC}).
(2) The maximum voltage applied at reference input voltage terminal $V_{eREF+} = [AV_{CC} - VE(O)] / [3 \times (1 + E_G)]$.
(3) For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV_{CC}).
(4) The maximum voltage applied at reference input voltage terminal $V_{eREF+} = [AV_{CC} - V_{E(O)}] / (1 + E_G)$.
(5) When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive dividers for each DAC are in parallel reducing the reference input resistance.

12-Bit DAC Dynamic Specifications

$V_{REF} = V_{CC}$, DAC12IR = 1 (see Figure 45 and Figure 46), over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
t_{ON}	DAC12 on-time	DAC12_xDAT = 800h, $Error_{V(O)}$ < ±0.5 LSB(1) (see Figure 45)	DAC12AMPx = 0 → {2, 3, 4}	2.2 V, 3 V		60	120	µs
			DAC12AMPx = 0 → {5, 6}			15	30	
			DAC12AMPx = 0 → 7			6	12	
$t_{S(FS)}$	Settling time, full scale	DAC12_xDAT = 80h → F7Fh → 80h	DAC12AMPx = 2	2.2 V, 3 V		100	200	µs
			DAC12AMPx = 3, 5			40	80	
			DAC12AMPx = 4, 6, 7			15	30	
$t_{S(C-C)}$	Settling time, code to code	DAC12_xDAT = 3F8h → 408h → 3F8h BF8h → C08h → BF8h	DAC12AMPx = 2	2.2 V, 3 V		5		µs
			DAC12AMPx = 3, 5			2		
			DAC12AMPx = 4, 6, 7			1		
SR	Slew rate(2)	DAC12_xDAT = 80h → F7Fh → 80h	DAC12AMPx = 2	2.2 V, 3 V	0.05	0.12		V/µs
			DAC12AMPx = 3, 5		0.35	0.7		
			DAC12AMPx = 4, 6, 7		1.5	2.7		
	Glitch energy, full scale	DAC12_xDAT = 80h → F7Fh → 80h	DAC12AMPx = 2	2.2 V, 3 V		600		nV-s
			DAC12AMPx = 3, 5			150		
			DAC12AMPx = 4, 6, 7			30		
BW_{-3dB}	3-dB bandwidth, V_{DC} = 1.5 V, V_{AC} = 0.1 V_{PP} (see Figure 47)	DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h		2.2 V, 3 V	40			kHz
		DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h			180			
		DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h			550			
	Channel-to-channel crosstalk(1) (see Figure 48)	DAC12_0DAT = 800h, No load, DAC12_1DAT = 80h ↔ F7Fh, R_{Load} = 3 kΩ, f_{DAC12_1OUT} = 10 kHz, Duty cycle = 50%		2.2 V, 3 V		-80		dB
		DAC12_0DAT = 80h ↔ F7Fh, R_{Load} = 3 kΩ, DAC12_1DAT = 800h, No load, f_{DAC12_0OUT} = 10 kHz, Duty cycle = 50%				-80		

(1) R_{Load} and C_{Load} are connected to AV_{SS} (not $AV_{CC}/2$) in Figure 45.
(2) Slew rate applies to output voltage steps ≥ 200 mV.

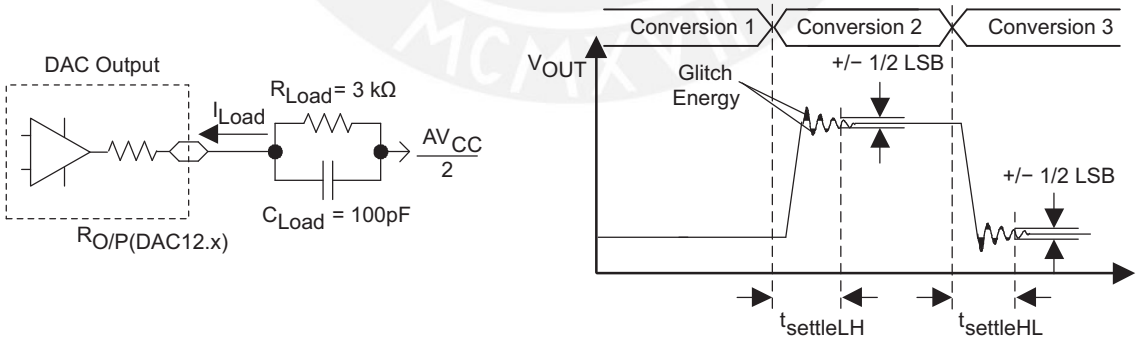


Figure 45. Settling Time and Glitch Energy Testing

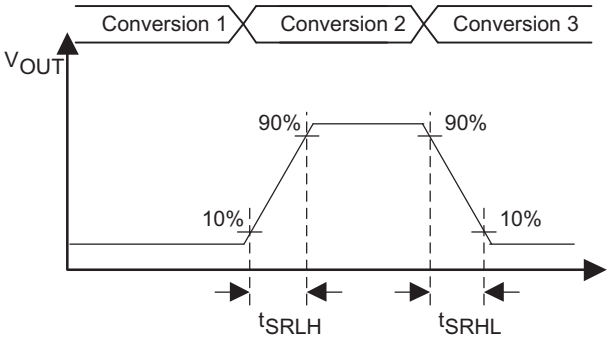


Figure 46. Slew Rate Testing

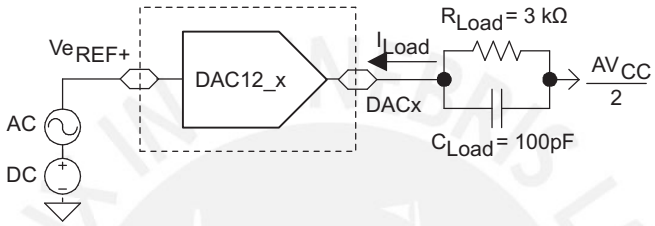


Figure 47. Test Conditions for 3-dB Bandwidth Specification

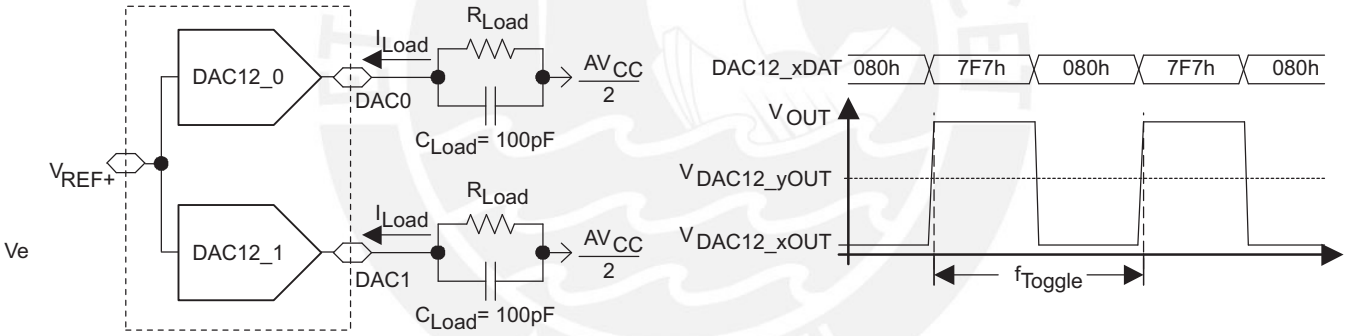


Figure 48. Crosstalk Test Conditions

Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V/3.6 V		1	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V/3.6 V		1	7	mA
t_{CPT}	Cumulative program time (1)		2.2 V/3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.2 V/3.6 V	20			ms
	Program and erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	(2)			30		t_{FTG}
$t_{Block, 0}$	Block program time for first byte or word	(2)			25		t_{FTG}
$t_{Block, 1-63}$	Block program time for each additional byte or word	(2)			18		t_{FTG}
$t_{Block, End}$	Block program end-sequence wait time	(2)			6		t_{FTG}
$t_{Mass\ Erase}$	Mass erase time	(2)			10593		t_{FTG}
$t_{Seg\ Erase}$	Segment erase time	(2)			4819		t_{FTG}

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(2) These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage (1)	CPU halted	1.6		V

(1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

JTAG Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency (1)	2.2 V	0		5	MHz
		3 V	0		10	
$R_{Internal}$	Internal pullup resistance on TMS, TCK, and TDI/TCLK (2)	2.2 V, 3 V	25	60	90	kΩ

(1) f_{TCK} may be restricted to meet the timing requirements of the module selected.
(2) TMS, TCK, and TDI/TCLK pullup resistors are implemented in all versions.

JTAG Fuse (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C	2.5		V
V_{FB}	Voltage level on TEST for fuse blow		6	7	V
I_{FB}	Supply current into TEST during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

(1) Once the fuse is blown, no further access to the JTAG/Test and emulation feature is possible, and JTAG is switched to bypass mode.

APPLICATION INFORMATION

Port P1 (P1.0 to P1.7), Input/Output With Schmitt Trigger

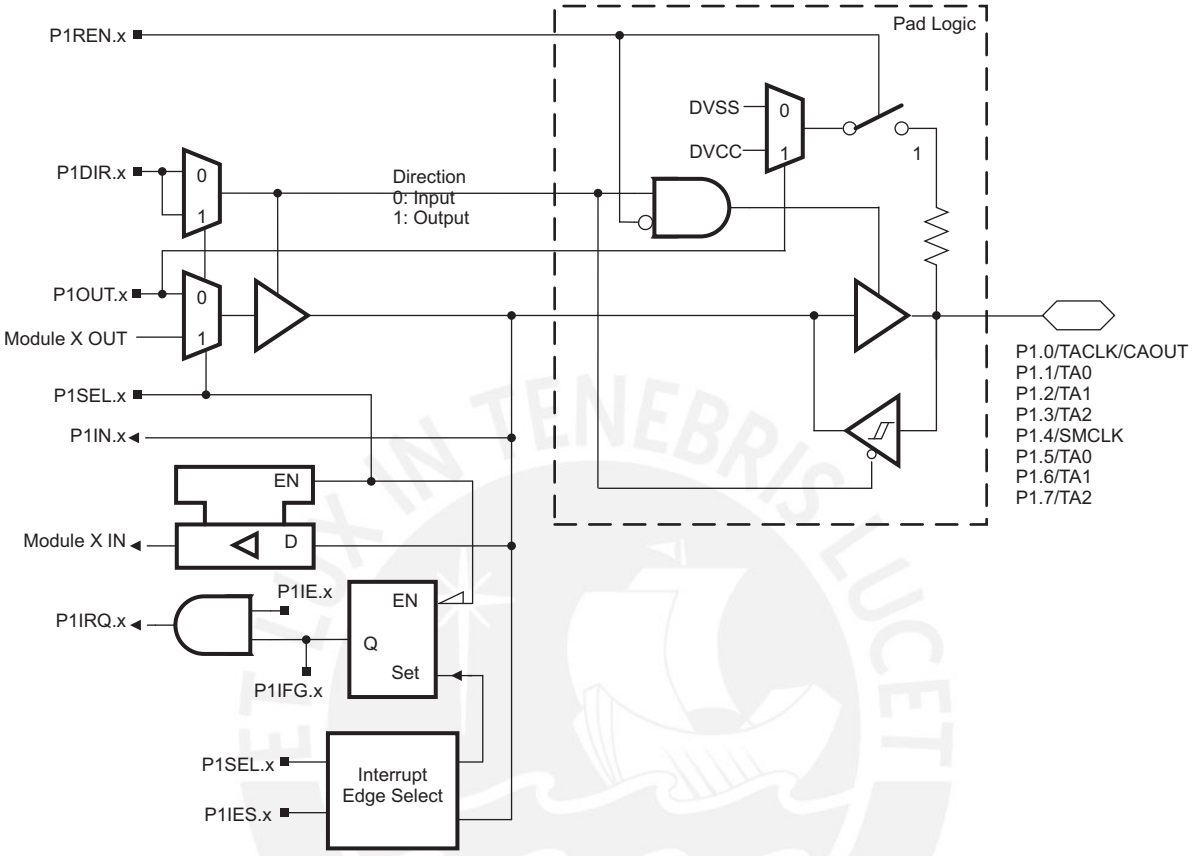


Table 15. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS / SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TACLK/CAOUT	0	P1.0 (I/O)	I: 0; O: 1	0
		Timer_A3.TACLK	0	1
		CAOUT	1	1
P1.1/TA0	1	P1.1 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.2/TA1	2	P1.2 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI1A	0	1
		Timer_A3.TA1	1	1
P1.3/TA2	3	P1.3 (I/O)	I: 0; O: 1	0
		Timer_A3.CCI2A	0	1
		Timer_A3.TA2	1	1
P1.4/SMCLK	4	P1.4 (I/O)	I: 0; O: 1	0
		SMCLK	1	1
P1.5/TA0	5	P1.5 (I/O)	I: 0; O: 1	0
		Timer_A3.TA0	1	1
P1.6/TA1	6	P1.6 (I/O)	I: 0; O: 1	0
		Timer_A3.TA1	1	1
P1.7/TA2	7	P1.7 (I/O)	I: 0; O: 1	0
		Timer_A3.TA2	1	1

Port P2 (P2.0 to P2.4, P2.6, and P2.7), Input/Output With Schmitt Trigger

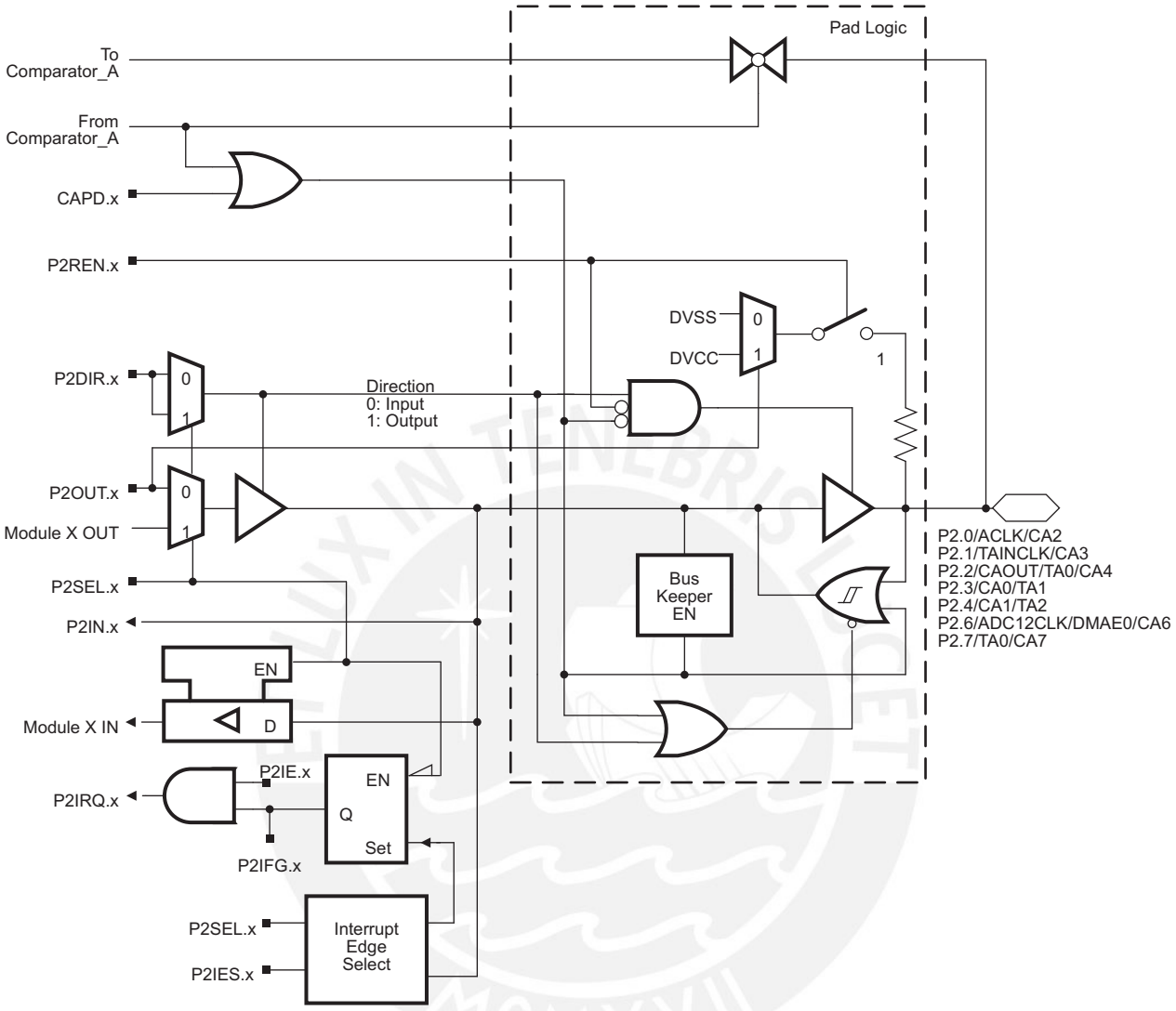


Table 16. Port P2 (P2.0 to P2.4, P2.6, and P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS / SIGNALS(1)		
			CAPD.x	P2DIR.x	P2SEL.x
P2.0/ACLK/CA2	0	P2.0 (I/O)	0	I: 0; O: 1	0
		ACLK	0	1	1
		CA2	1	X	X
P2.1/TAINCLK/CA3	1	P2.1 (I/O)	0	I: 0; O: 1	0
		Timer_A3.INCLK	0	0	1
		DV_{SS}	0	1	1
		CA3	1	X	X
P2.2/CAOUT/TA0/CA4	2	P2.2 (I/O)	0	I: 0; O: 1	0
		CAOUT	0	1	1
		Timer_A3.CCI0B	0	0	1
		CA4	1	X	X
P2.3/CA0/TA1	3	P2.3 (I/O)	0	I: 0; O: 1	0
		Timer_A3.TA1	0	1	1
		CA0	1	X	X
P2.4/CA1/TA2	4	P2.4 (I/O)	0	I: 0; O: 1	0
		Timer_A3.TA2	0	1	X
		CA1	1	X	1
P2.6/ADC12CLK/ DMAE0(2)/CA6	6	P2.6 (I/O)	0	I: 0; O: 1	0
		ADC12CLK	0	1	1
		DMAE0	0	0	1
		CA6	1	X	X
P2.7/TA0/CA7	7	P2.7 (I/O)	0	I: 0; O: 1	0
		Timer_A3.TA0	0	1	1
		CA7	1	X	X

(1) X = Don't care
(2) MSP430F261x devices only

Port P2 (P2.5), Input/Output With Schmitt Trigger

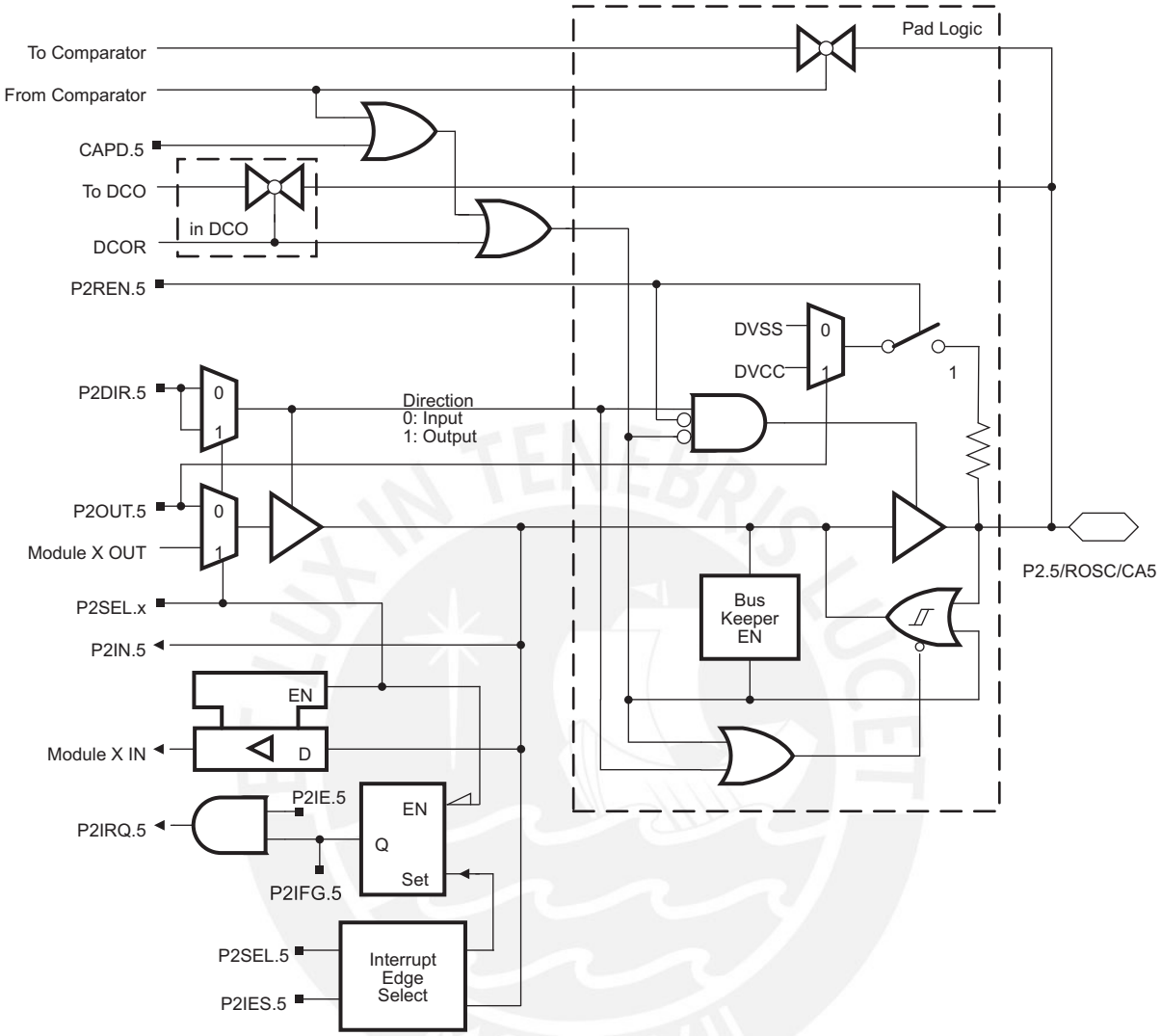


Table 17. Port P2 (P2.5) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]			
			CAPD	DCOR	P2DIR.5	P2SEL.5
P2.5/R_{OSC}/CA5	5	P2.5 (I/O)	0	0	I: 0; O: 1	0
		R_{OSC}[2]	0	1	X	X
		DV_{SS}	0	0	1	1
		CA5	1 or selected	0	X	X

(1) X = Don't care
(2) If R_{OSC} is used, it is connected to an external resistor.

Port P3 (P3.0 to P3.7), Input/Output With Schmitt Trigger

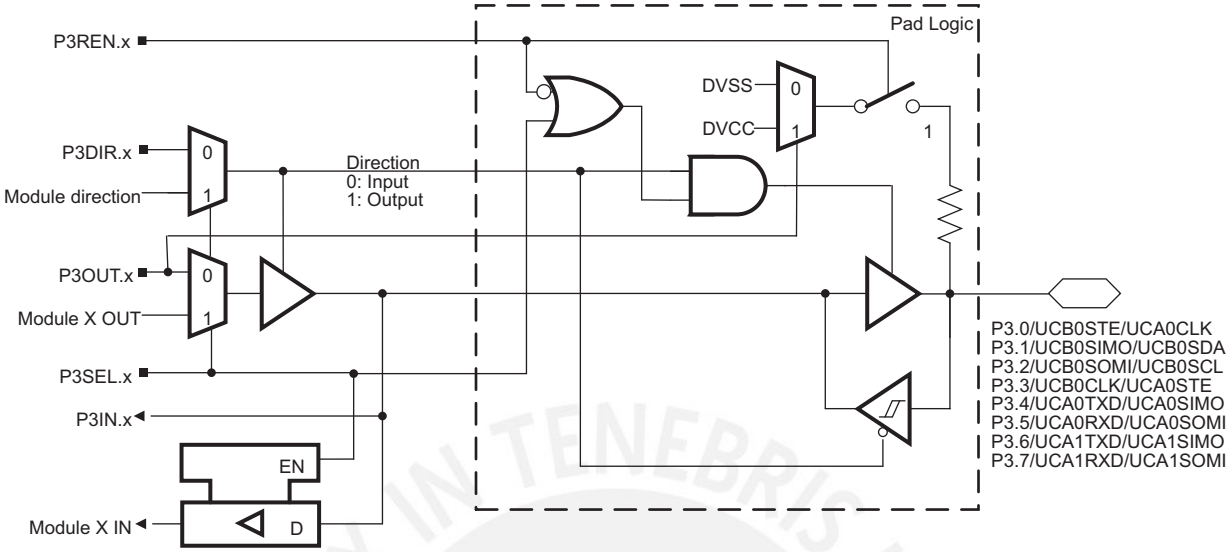


Table 18. Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS / SIGNALS(1)	
			P3DIR.x	P3SEL.x
P3.0/UCB0STE/ UCA0CLK	0	P3.0 (I/O)	I: 0; O: 1	0
		UCB0STE/UCA0CLK(2)(3)	X	1
P3.1/UCB0SIMO/ UCB0SDA	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA(4)(5)	X	1
P3.2/UCB0SOMI/ UCB0SCL	2	P3.2 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL(4)(5)	X	1
P3.3/UCB0CLK/ UCA0STE	3	P3.3 (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE(4)	X	1
P3.4/UCA0TXD/ UCA0SIMO	4	P3.4 (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO(4)	X	1
P3.5/UCA0RXD/ UCA0SOMI	5	P3.5 (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI(4)	X	1
P3.6/UCA1TXD/ UCA1SIMO	6	P3.6 (I/O)	I: 0; O: 1	0
		UCA1TXD/UCA1SIMO(4)	X	1
P3.7/UCA1RXD/ UCA1SOMI	7	P3.7 (I/O)	I: 0; O: 1	0
		UCA1RXD/UCA1SOMI(4)	X	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI_A0/B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(4) The pin direction is controlled by the USCI module.
(5) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.

Port P4 (P4.0 to P4.7), Input/Output With Schmitt Trigger

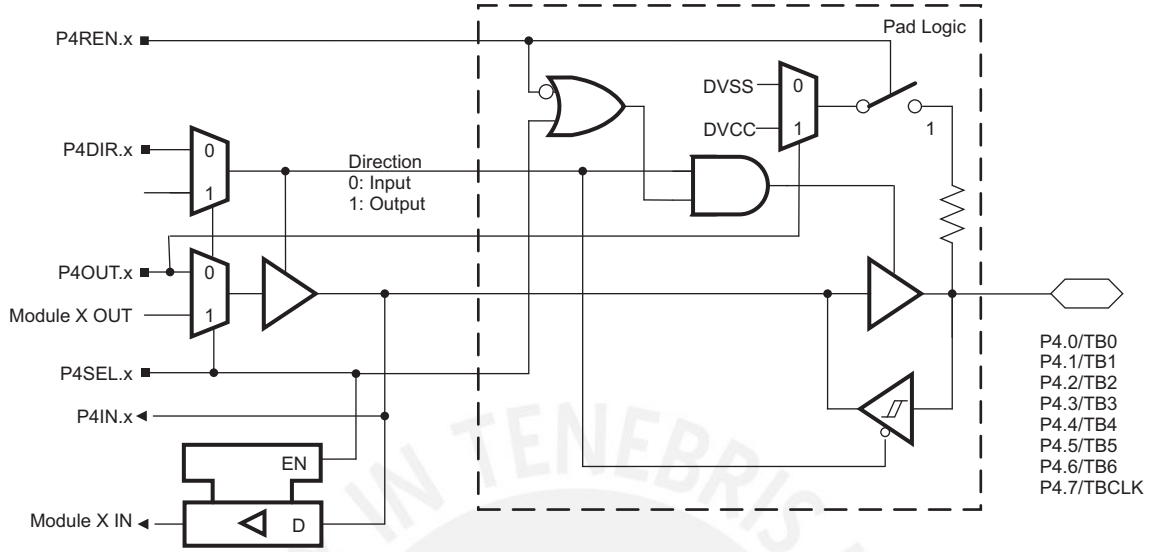


Table 19. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS / SIGNALS(1)	
			P4DIR.x	P4SEL.x
P4.0/TB0	0	P4.0 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI0A and Timer_B7.CCI0B	0	1
		Timer_B7.TB0	1	1
P4.1/TB1	1	P4.1 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI1A and Timer_B7.CCI1B	0	1
		Timer_B7.TB1	1	1
P4.2/TB2	2	P4.2 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI2A and Timer_B7.CCI2B	0	1
		Timer_B7.TB2	1	1
P4.3/TB3	3	P4.3 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI3A and Timer_B7.CCI3B	0	1
		Timer_B7.TB3	1	1
P4.4/TB4	4	P4.4 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI4A and Timer_B7.CCI4B	0	1
		Timer_B7.TB4	1	1
P4.5/TB5	5	P4.5 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI5A and Timer_B7.CCI5B	0	1
		Timer_B7.TB5	1	1
P4.6/TB6	6	P4.6 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI6A and Timer_B7.CCI6B	0	1
		Timer_B7.TB6	1	1
P4.7/TBCLK	7	P4.7 (I/O)	I: 0; O: 1	0
		Timer_B7.TBCLK	1	1

(1) X = Don't care

Port P5 (P5.0 to P5.7), Input/Output With Schmitt Trigger

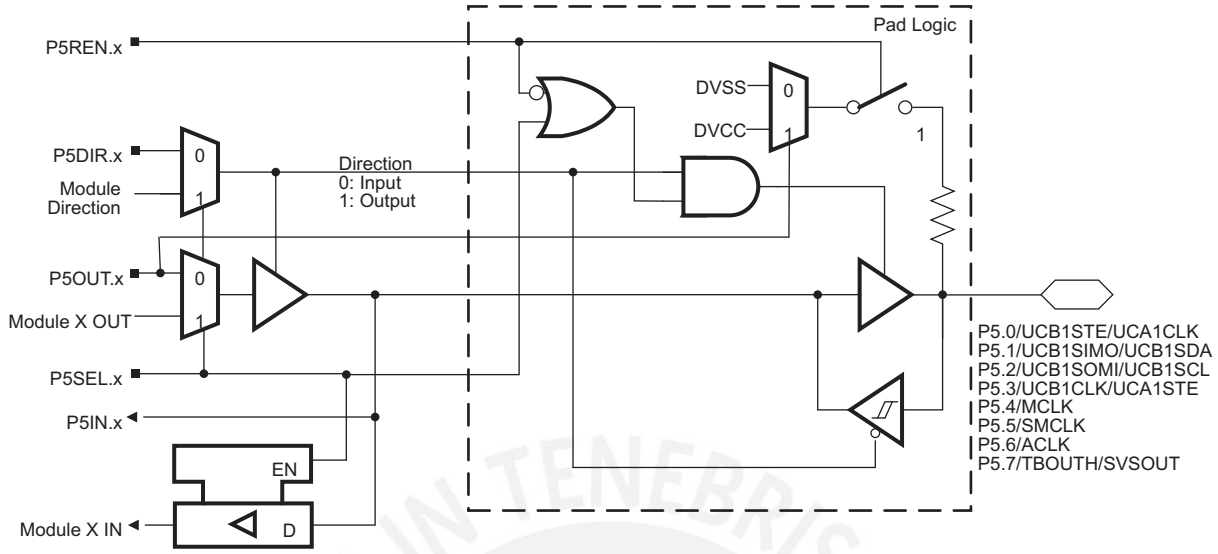


Table 20. Port P5 (P5.0 to P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS / SIGNALS(1)	
			P5DIR.x	P5SEL.x
P5.0/UCB1STE/ UCA1CLK	0	P5.0 (I/O)	I: 0; O: 1	0
		UCB1STE/UCA1CLK(2)(3)	X	1
P5.1/UCB1SIMO/ UCB1SDA	1	P5.1 (I/O)	I: 0; O: 1	0
		UCB1SIMO/UCB1SDA(2)(4)	X	1
P5.2/UCB1SOMI/ UCB1SCL	2	P5.2 (I/O)	I: 0; O: 1	0
		UCB1SOMI/UCB1SCL(2)(4)	X	1
P5.3/UCB1CLK/ UCA1STE	3	P5.3 (I/O)	I: 0; O: 1	0
		UCB1CLK/UCA1STE(2)	X	1
P5.4/MCLK	4	P5.0 (I/O)	I: 0; O: 1	0
		MCLK	1	1
P5.5/SMCLK	5	P5.1 (I/O)	I: 0; O: 1	0
		SMCLK	1	1
P5.6/ACLK	6	P5.2 (I/O)	I: 0; O: 1	0
		ACLK	1	1
P5.7/TBOUTH/SVSOUT	7	P5.7 (I/O)	I: 0; O: 1	0
		TBOUTH	0	1
		SVSOUT	1	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA1CLK function takes precedence over UCB1STE function. If the pin is required as UCA1CLK input or output USCI_A1/B1 will be forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(4) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.

Port P6 (P6.0 to P6.4), Input/Output With Schmitt Trigger

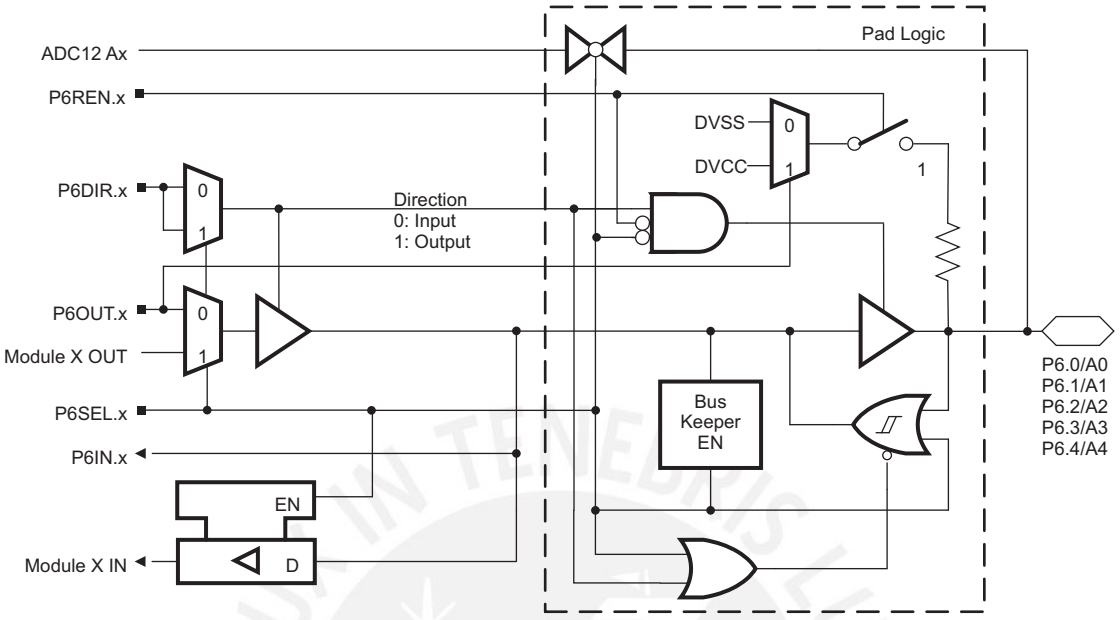


Table 21. Port P6 (P6.0 to P6.4) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS / SIGNALS (1)		
			P6DIR.x	P6SEL.x	INCH.x
P6.0/A0	0	P6.0 (I/O)	I: 0; O: 1	0	0
		A0 (2)	X	1	1 (y = 0)
P6.1/A1	1	P6.1 (I/O)	I: 0; O: 1	0	0
		A1 (2)	X	1	1 (y = 1)
P6.2/A2	2	P6.2 (I/O)	I: 0; O: 1	0	0
		A2 (2)	X	1	1 (y = 2)
P6.3/A3	3	P6.3 (I/O)	I: 0; O: 1	0	0
		A3 (2)	X	1	1 (y = 3)
P6.4/A4	4	P6.4 (I/O)	I: 0; O: 1	0	0
		A4 (2)	X	1	1 (y = 4)

(1) X = Don't care
(2) The ADC12 channel Ax is connected to AV_{SS} internally if not selected.

Port P6 (P6.5 and P6.6), Input/Output With Schmitt Trigger

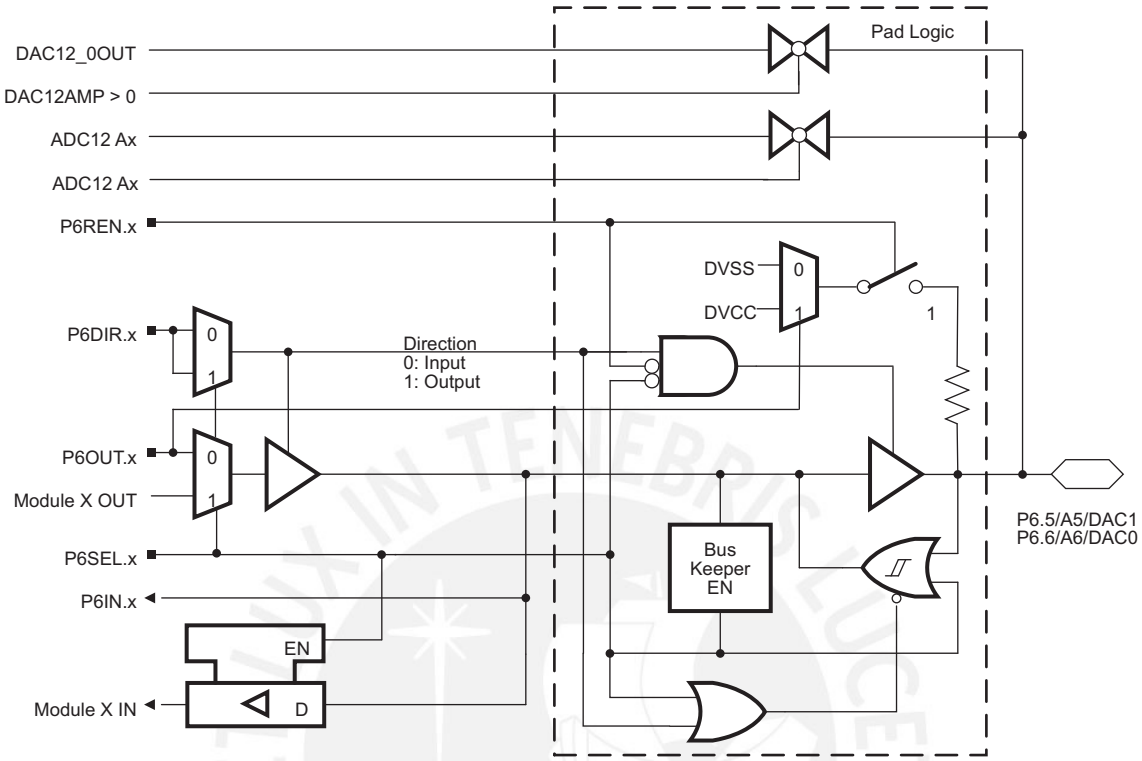


Table 22. Port P6 (P6.5 and P6.6) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]			
			P6DIR.x	P6SEL.x	DAC12AMP > 0	INCH.y
P6.5/A5/DAC1[2]	5	P6.5 (I/O)	I: 0; O: 1	0	0	0
		DV_{SS}	1	1	0	0
		A5[3]	X	X	0	1 (y = 5)
		DAC1 (DAC12OPS = 1)[4]	X	X	1	0
P6.6/A6/DAC0[5]	6	P6.6 (I/O)	I: 0; O: 1	0	0	0
		DV_{SS}	1	1	0	0
		A6[6]	X	X	0	1 (y = 6)
		DAC0 (DAC12OPS = 0)[7]	X	X	1	0

(1) X = Don't care
(2) MSP430F261x devices only
(3) The ADC12 channel Ax is connected to AV_{SS} internally if not selected.
(4) The DAC outputs are floating if not selected.
(5) MSP430F261x devices only
(6) The ADC12 channel Ax is connected to AV_{SS} internally if not selected.
(7) The DAC outputs are floating if not selected.

Port P6 (P6.7), Input/Output With Schmitt Trigger

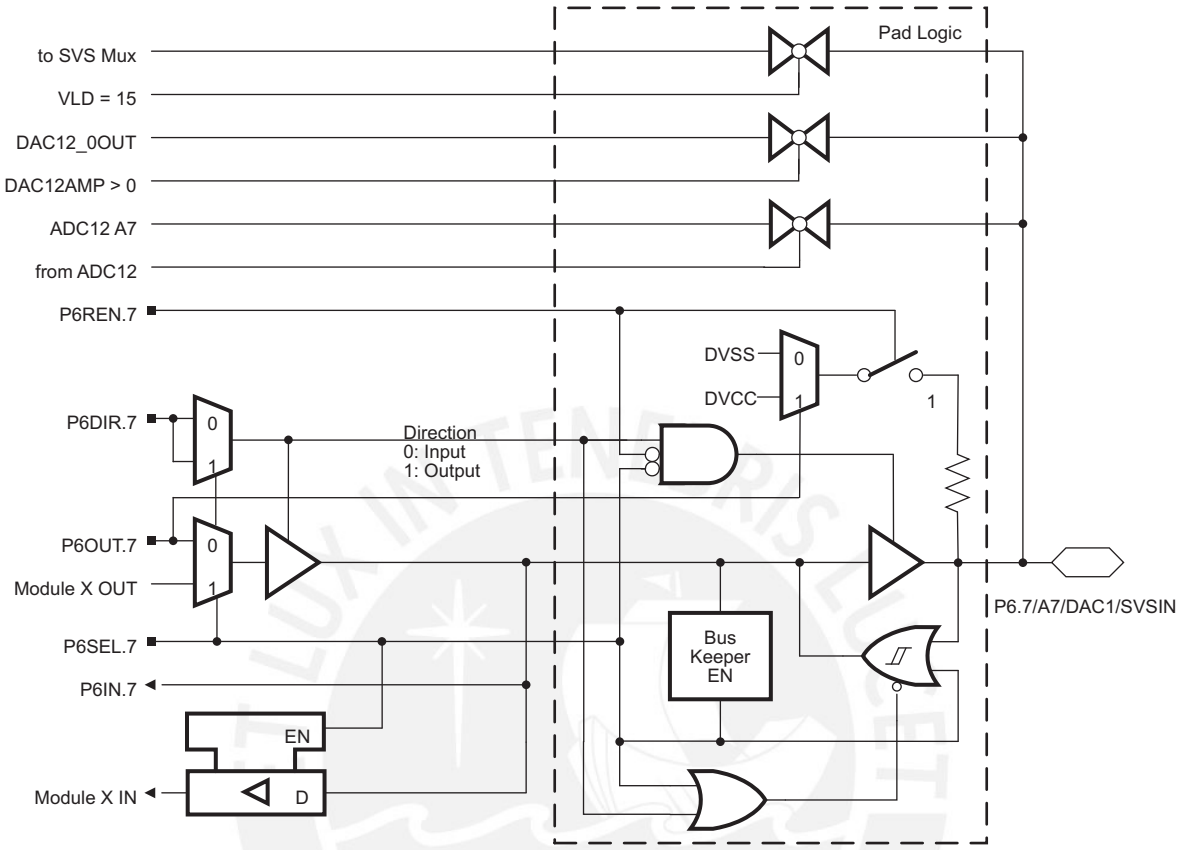


Table 23. Port P6 (P6.7) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS / SIGNALS[1]			
			P6DIR.x	P6SEL.x	INCH.y	DAC12AMP>0
P6.7/A7/DAC1[2]/ SVSIN[2]	7	P6.7 (I/O)	I: 0; O: 1	0	0	0
		DV_{SS}	1	1	0	0
		A7[3]	X	1	1 (y = 7)	0
		DAC1 (DAC12OPS = 0)[4]	X	1	0	1
		SVSIN (VLD = 15)	X	1	0	0

(1) X = Don't care
(2) MSP430F261x devices only
(3) The ADC12 channel Ax is connected to AV_{SS} internally if not selected.
(4) The DAC outputs are floating if not selected.

Port P7 (P7.0 to P7.7), Input/Output With Schmitt Trigger(5)

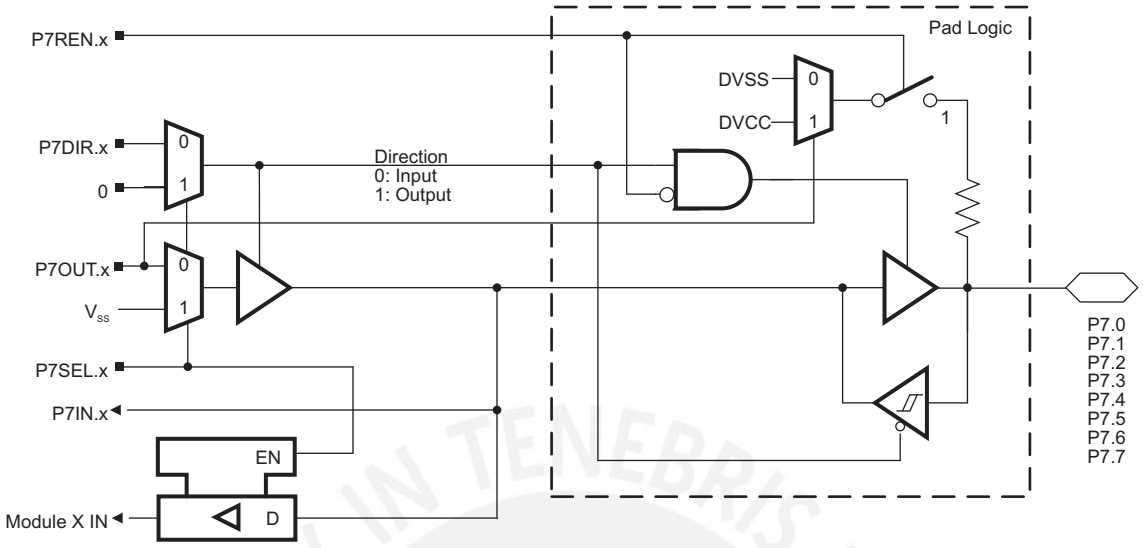


Table 24. Port P7 (P7.0 to P7.7) Pin Functions(1)

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS / SIGNALS(2)	
			P7DIR.x	P7SEL.x
P7.0	0	P7.0 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.1	1	P7.1 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.2	2	P7.2 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.3	3	P7.3 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.4	4	P7.4 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.5	5	P7.5 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.6	6	P7.6 (I/O)	I: 0; O: 1	0
		Input	X	1
P7.7	7	P7.7 (I/O)	I: 0; O: 1	0
		Input	X	1

(5) 80-pin devices only
(1) 80-pin devices only
(2) X = Don't care

Port P8 (P8.0 to P8.5), Input/Output With Schmitt Trigger(3)

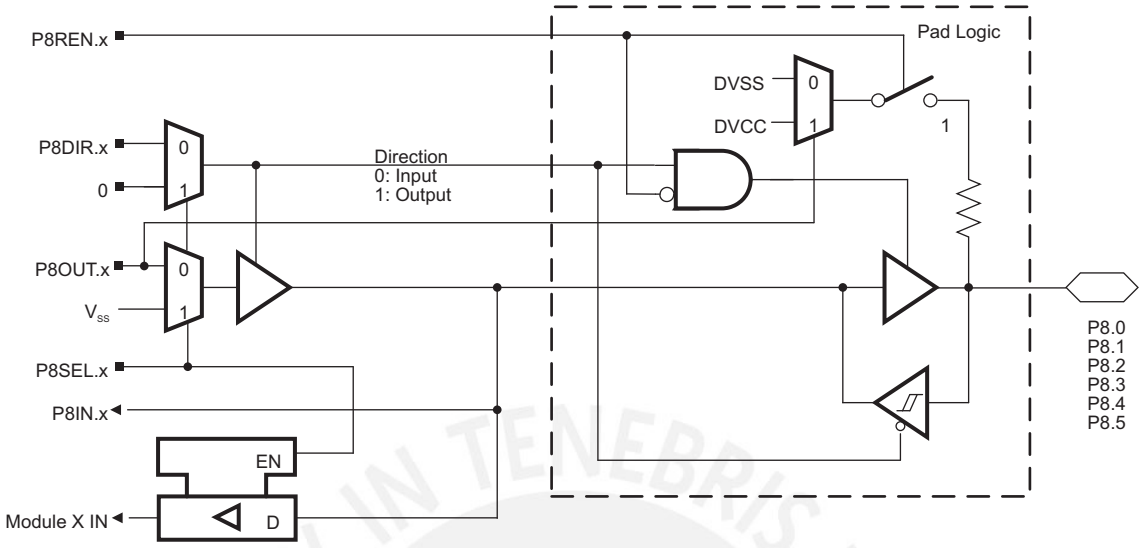


Table 25. Port P8 (P8.0 to P8.5) Pin Functions(1)

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS / SIGNALS(2)	
			P8DIR.x	P8SEL.x
P8.0	0	P8.0 (I/O)	I: 0; O: 1	0
		Input	X	1
P8.1	1	P8.1 (I/O)	I: 0; O: 1	0
		Input	X	1
P8.2	2	P8.2 (I/O)	I: 0; O: 1	0
		Input	X	1
P8.3	3	P8.3 (I/O)	I: 0; O: 1	0
		Input	X	1
P8.4	4	P8.4 (I/O)	I: 0; O: 1	0
		Input	X	1
P8.5	5	P8.5 (I/O)	I: 0; O: 1	0
		Input	X	1

(3) 80-pin devices only
(1) 80-pin devices only
(2) X = Don't care

Port P8 (P8.6), Input/Output With Schmitt Trigger(3)

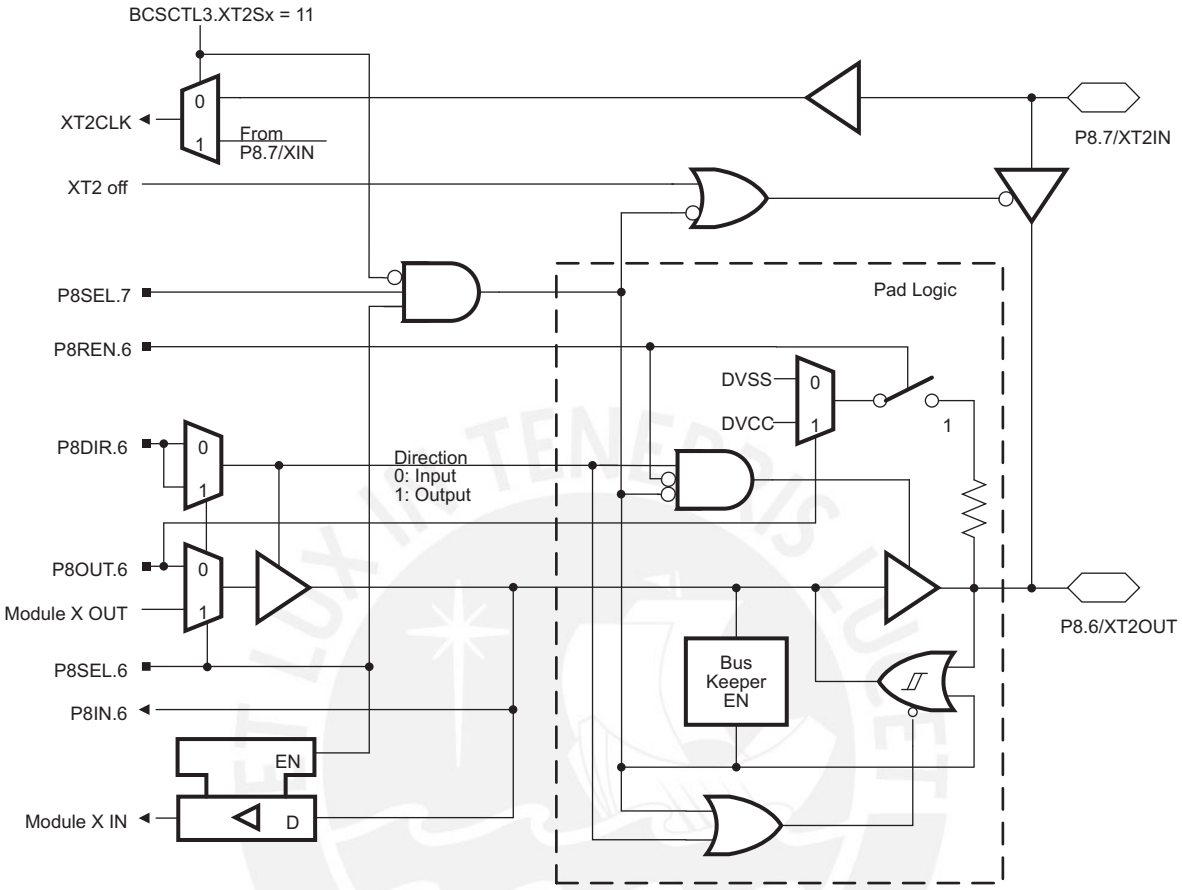


Table 26. Port P8 (P8.6) Pin Functions(1)

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS / SIGNALS	
			P8DIR.x	P8SEL.x
P8.6/XT2OUT	6	P8.6 (I/O)	I: 0; O: 1	0
		XT2OUT (default)	0	1
		DV_{SS}	1	1

(3) 80-pin devices only
(1) 80-pin devices only

Port P8 (P8.7), Input/Output With Schmitt Trigger(2)

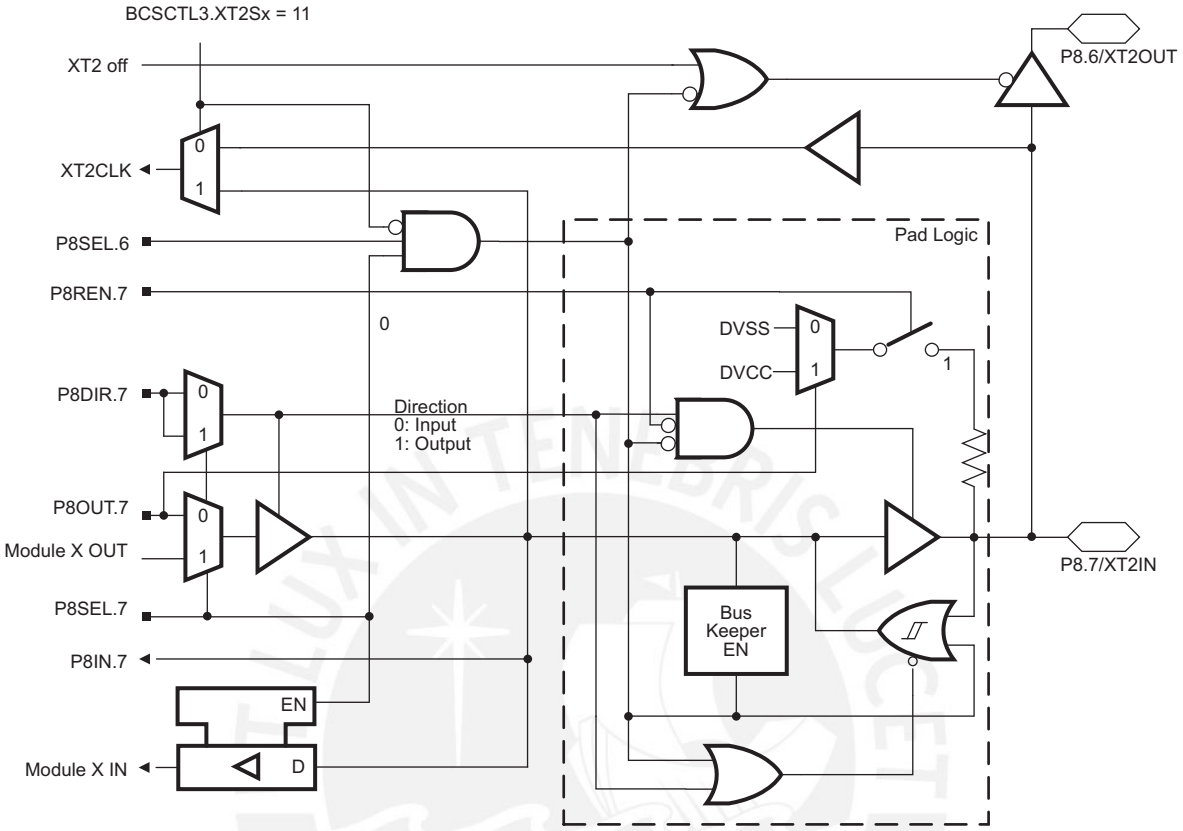
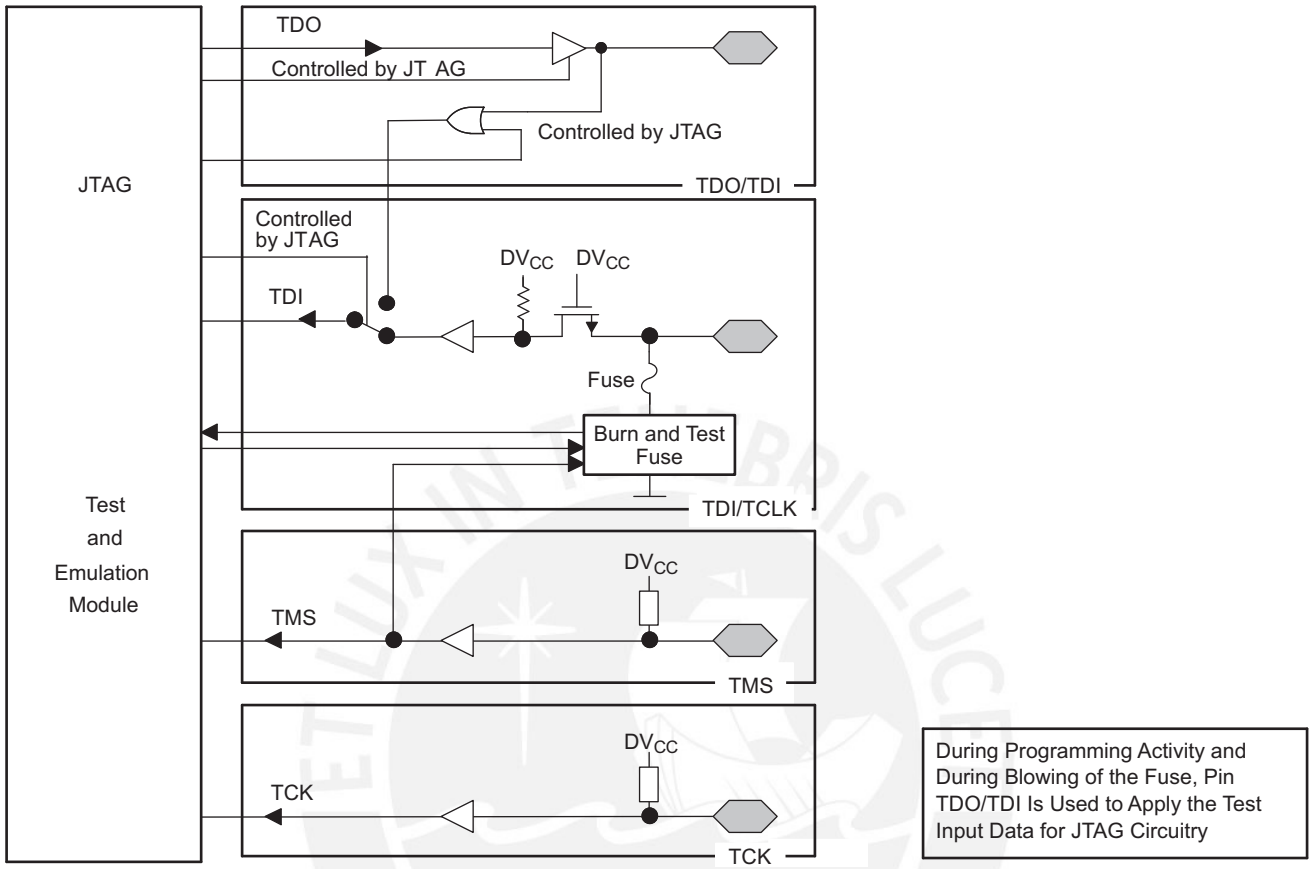


Table 27. Port P8 (P8.7) Pin Functions(1)

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS / SIGNALS	
			P8DIR.x	P8SEL.x
P8.7/XT2IN	7	P8.7 (I/O)	I: 0; O: 1	0
		XT2IN (default)	0	1
		V_{SS}	1	1

(2) 80-pin devices only
(1) 80-pin devices only

JTAG Pins: TMS, TCK, TDI/TCLK, TDO/TDI, Input/Output With Schmitt Trigger



JTAG Fuse Check Mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF} , of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is again taken low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current flows only when the fuse check mode is active and the TMS pin is in a low state (see Figure 49). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

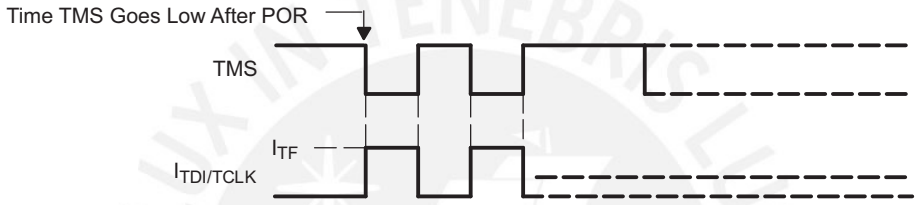


Figure 49. Fuse Check Mode Current

REVISION HISTORY

LITERATURE NUMBER	DESCRIPTION
SLAS541	Product Preview release
SLAS541A	Production Data release Corrected the format and the content shown on the first page. Corrected pin number of P3.6 and P3.7 in 64-pin package in the terminal function list. Corrected the port schematics. Corrected "calibration data" section (page 20). Typos and formatting corrected. Added the figure "typical characteristics - LPM4 current" (Page 33).
SLAS541B	Added preview of MSP430F261x BGA devices.
SLAS541C	Release to market of MSP430F261x BGA devices
SLAS541D	Added the ESD disclaimer (page 1). Added reserved BGA pins to the terminal function list (pages 10 and following). Corrected the references in the output port parameters (page 36). Corrected the cumulative program time of the flash (page 75).
SLAS541E	Corrected LFXT1Sx values in Figures 23 and 24 (page 52). Corrected XT2Sx values in Figures 25 and 26 (page 54). Corrected $t_{CMErase}$ MIN value from 200 ms to 20 ms and removed two notes in the flash memory table (page 75).
SLAS541F	Renamed Tags Used by the ADC Calibration Tags table to Tags used by the TLV Structure (page 20). Changed value of TAG_ADC12_1 from 0x10 to 0x08 in Tags used by the TLV Structure (page 20). Added CAOUT to P1.0/TACLK, Changed Timer_A3.CCI0A to Timer_A3.CCI1A and Timer_A3.TA0 to Timer_A3.TA1 in P1.2/TA1 row, Changed Timer_A3.CCI0A to Timer_A3.CCI2A and Timer_A3.TA0 to Timer_A3.TA2 in P1.3/TA2 row in Port P1 (P1.0 to P1.7) pin functions table (page 78). Changed TA0 to Timer_A3.CCI0B in P2.2/CAOUT/TA0/CA4 row of Port P2.0, P2.3, P2.4, P2.6 and P2.7 pin functions table (page 80).
SLAS541G	Changed limits on $t_{d(SVSon)}$ parameter (page 40)
SLAS541H	Changed Control Bits/Signals in Table 21, Table 22, and Table 23. Changed crystal signal names in Table 26 and Table 27.
SLAS541I	Changed T_{stg}, Programmed device, to -55°C to 150°C in Absolute Maximum Ratings.
SLAS541J	Added nonmagnetic package option to Description and Table 1.
SLAS541K	Changed P8.6/XT2OUT and P8.7/XT2IN to I/O in Table 2.

TEXAS INSTRUMENTS

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
MSP430F2416TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2416T	Samples
MSP430F2416TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2416T	Samples
MSP430F2416TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2416T	Samples
MSP430F2416TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2416T	Samples
MSP430F2416TZQW	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	M430F2416T	Samples
MSP430F2416TZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	M430F2416T	Samples
MSP430F2417TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2417T	Samples
MSP430F2417TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2417T	Samples
MSP430F2417TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2417T	Samples
MSP430F2417TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2417T	Samples
MSP430F2417TZQW	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	M430F2417T	Samples
MSP430F2417TZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	M430F2417T	Samples
MSP430F2418TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2418T	Samples
MSP430F2418TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2418T	Samples
MSP430F2418TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2418T	Samples

TEXAS INSTRUMENTS

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
MSP430F2418TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2418T	Samples
MSP430F2418TZQW	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	M430F2418T	Samples
MSP430F2418TZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	M430F2418T	Samples
MSP430F2419TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2419T	Samples
MSP430F2419TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2419T	Samples
MSP430F2419TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2419T	Samples
MSP430F2419TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2419T	Samples
MSP430F2419TZQW	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	M430F2419T	Samples
MSP430F2419TZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	M430F2419T	Samples
MSP430F2616TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2616T	Samples
MSP430F2616TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2616T	Samples
MSP430F2616TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2616T	Samples
MSP430F2616TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2616T	Samples
MSP430F2616TZQW	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	M430F2616T	Samples
MSP430F2616TZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	M430F2616T	Samples

TEXAS INSTRUMENTS

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
MSP430F2617TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2617T	Samples
MSP430F2617TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2617T	Samples
MSP430F2617TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2617T	Samples
MSP430F2617TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2617T	Samples
MSP430F2617TZQW	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	M430F2617T	Samples
MSP430F2617TZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	M430F2617T	Samples
MSP430F2618TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2618T	Samples
MSP430F2618TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2618T	Samples
MSP430F2618TPMR-NM	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 105	430F2618NM	Samples
MSP430F2618TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2618T	Samples
MSP430F2618TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2618T	Samples
MSP430F2618TZQW	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	M430F2618T	Samples
MSP430F2618TZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	M430F2618T	Samples
MSP430F2619TPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2619T REV #	Samples
MSP430F2619TPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2619T REV #	Samples
MSP430F2619TPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2619T	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
MSP430F2619TPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	M430F2619T	Samples
MSP430F2619TZQW	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	M430F2619T	Samples
MSP430F2619TZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 105	M430F2619T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF MSP430F2618 :

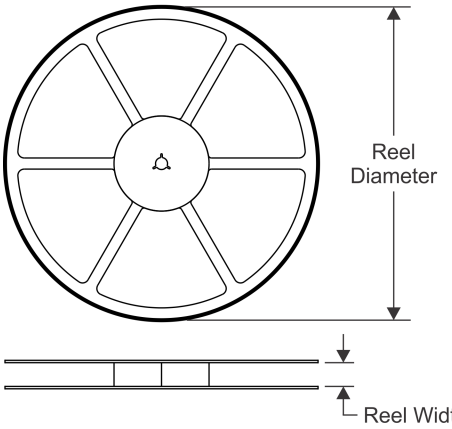
- Enhanced Product: MSP430F2618-EP

NOTE: Qualified Version Definitions:

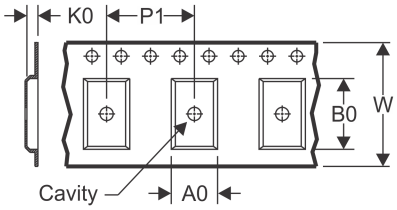
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

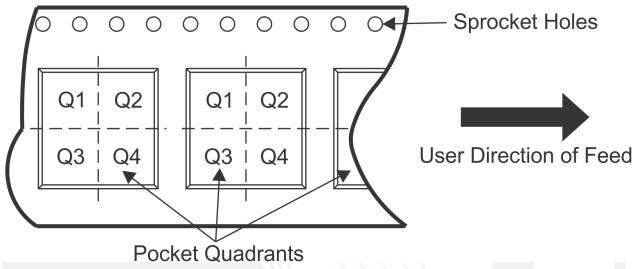


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

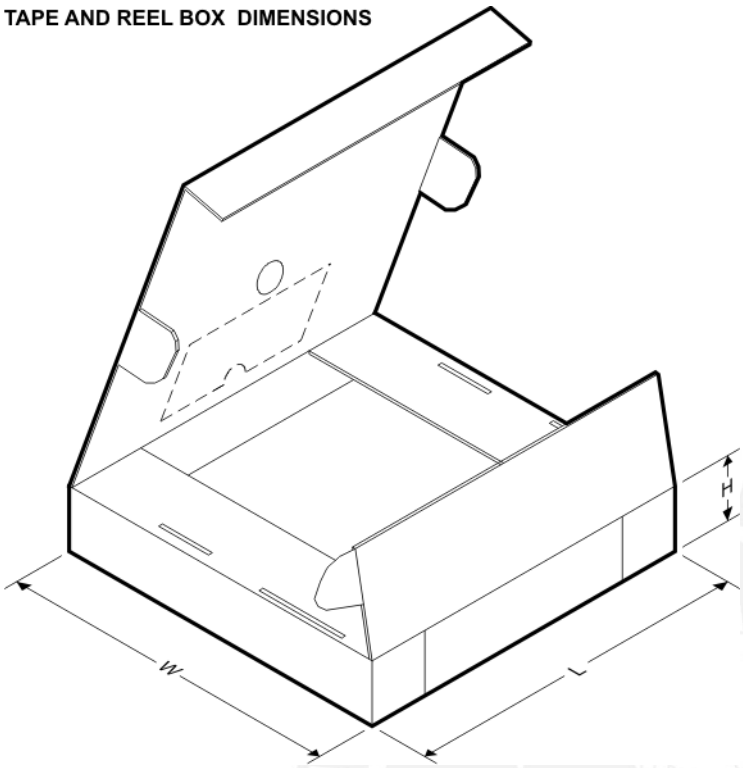


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F2416TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2416TPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F2416TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2417TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2417TPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F2417TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2418TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2418TPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F2418TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2419TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2419TPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F2419TZQWR	BGA MI	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	CROSTAR JUNIOR											
MSP430F2616TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2616TPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F2616TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2617TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2617TPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F2617TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2618TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2618TPMR-NM	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2618TPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F2618TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F2619TPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F2619TPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F2619TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

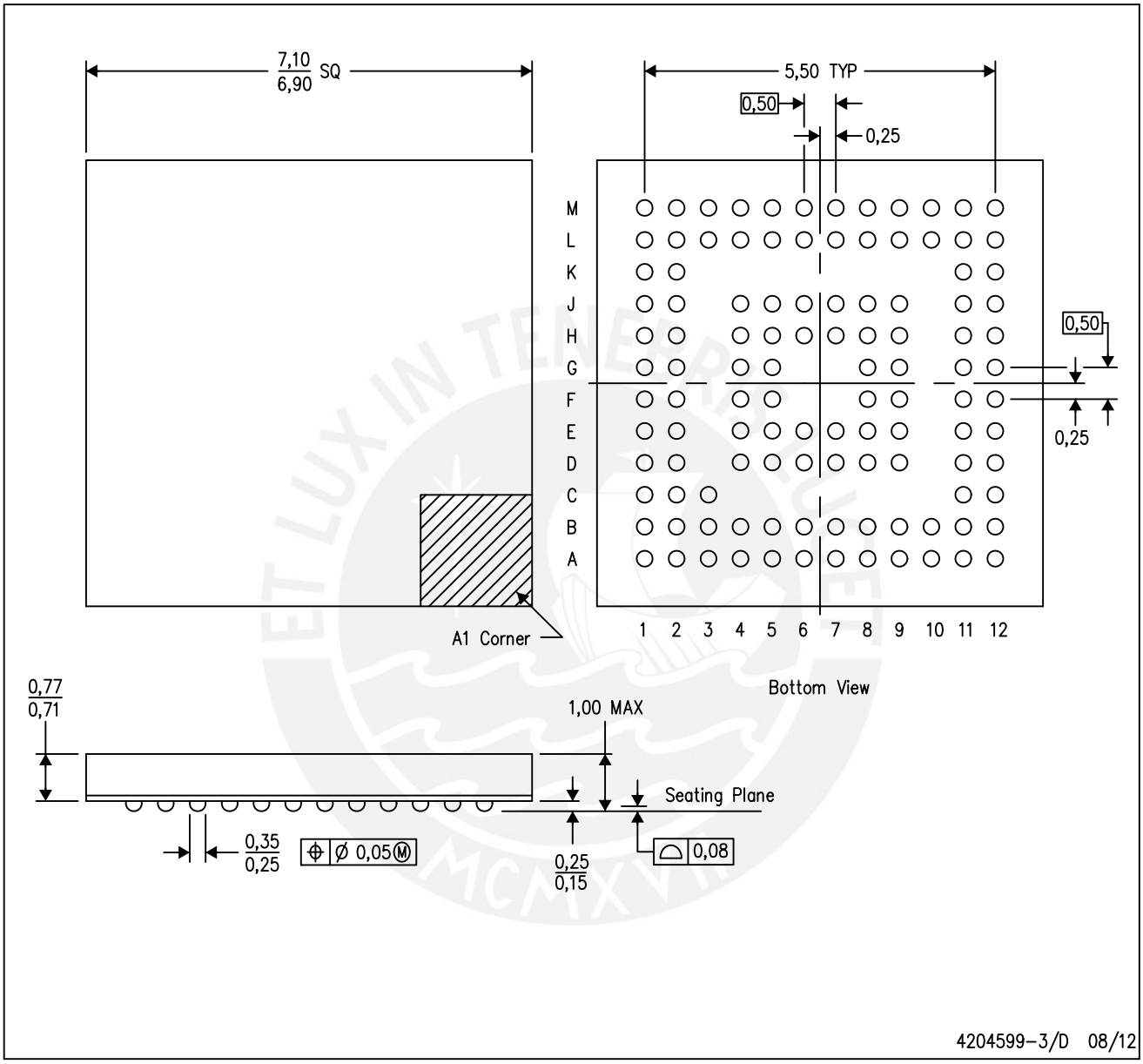


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F2416TPMR	LQFP	PM	64	1000	367.0	367.0	45.0
MSP430F2416TPNR	LQFP	PN	80	1000	367.0	367.0	45.0
MSP430F2416TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430F2417TPMR	LQFP	PM	64	1000	367.0	367.0	45.0
MSP430F2417TPNR	LQFP	PN	80	1000	367.0	367.0	45.0
MSP430F2417TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430F2418TPMR	LQFP	PM	64	1000	367.0	367.0	45.0
MSP430F2418TPNR	LQFP	PN	80	1000	367.0	367.0	45.0
MSP430F2418TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430F2419TPMR	LQFP	PM	64	1000	367.0	367.0	45.0
MSP430F2419TPNR	LQFP	PN	80	1000	367.0	367.0	45.0
MSP430F2419TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430F2616TPMR	LQFP	PM	64	1000	367.0	367.0	45.0
MSP430F2616TPNR	LQFP	PN	80	1000	367.0	367.0	45.0
MSP430F2616TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430F2617TPMR	LQFP	PM	64	1000	367.0	367.0	45.0
MSP430F2617TPNR	LQFP	PN	80	1000	367.0	367.0	45.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F2617TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430F2618TPMR	LQFP	PM	64	1000	367.0	367.0	45.0
MSP430F2618TPMR-NM	LQFP	PM	64	1000	367.0	367.0	45.0
MSP430F2618TPNR	LQFP	PN	80	1000	367.0	367.0	45.0
MSP430F2618TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430F2619TPMR	LQFP	PM	64	1000	367.0	367.0	45.0
MSP430F2619TPNR	LQFP	PN	80	1000	367.0	367.0	45.0
MSP430F2619TZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6

ZQW (S–PBGA–N113) PLASTIC BALL GRID ARRAY

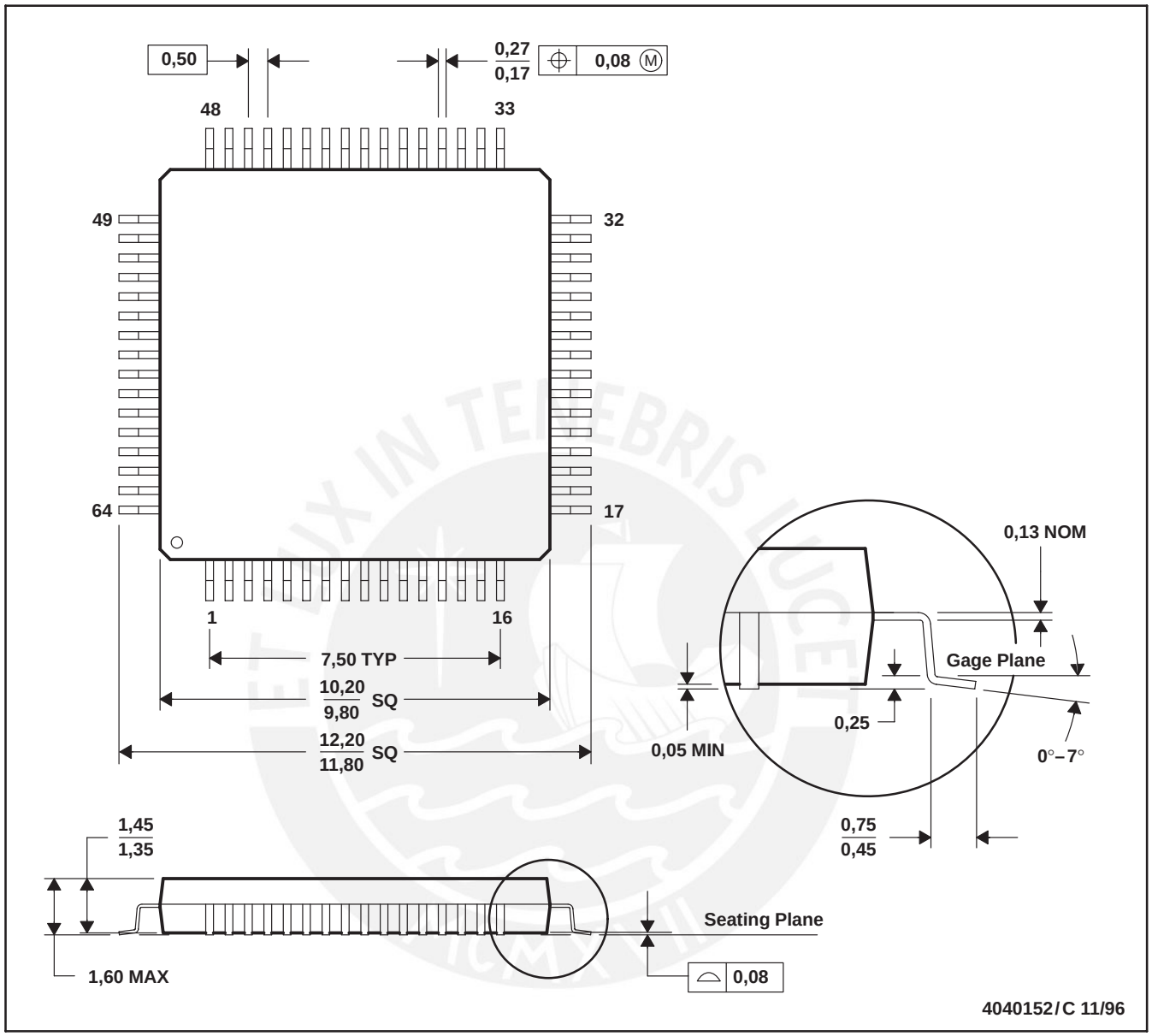


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a Pb–free solder ball design.

MicroStar Junior is a trademark of Texas Instruments.

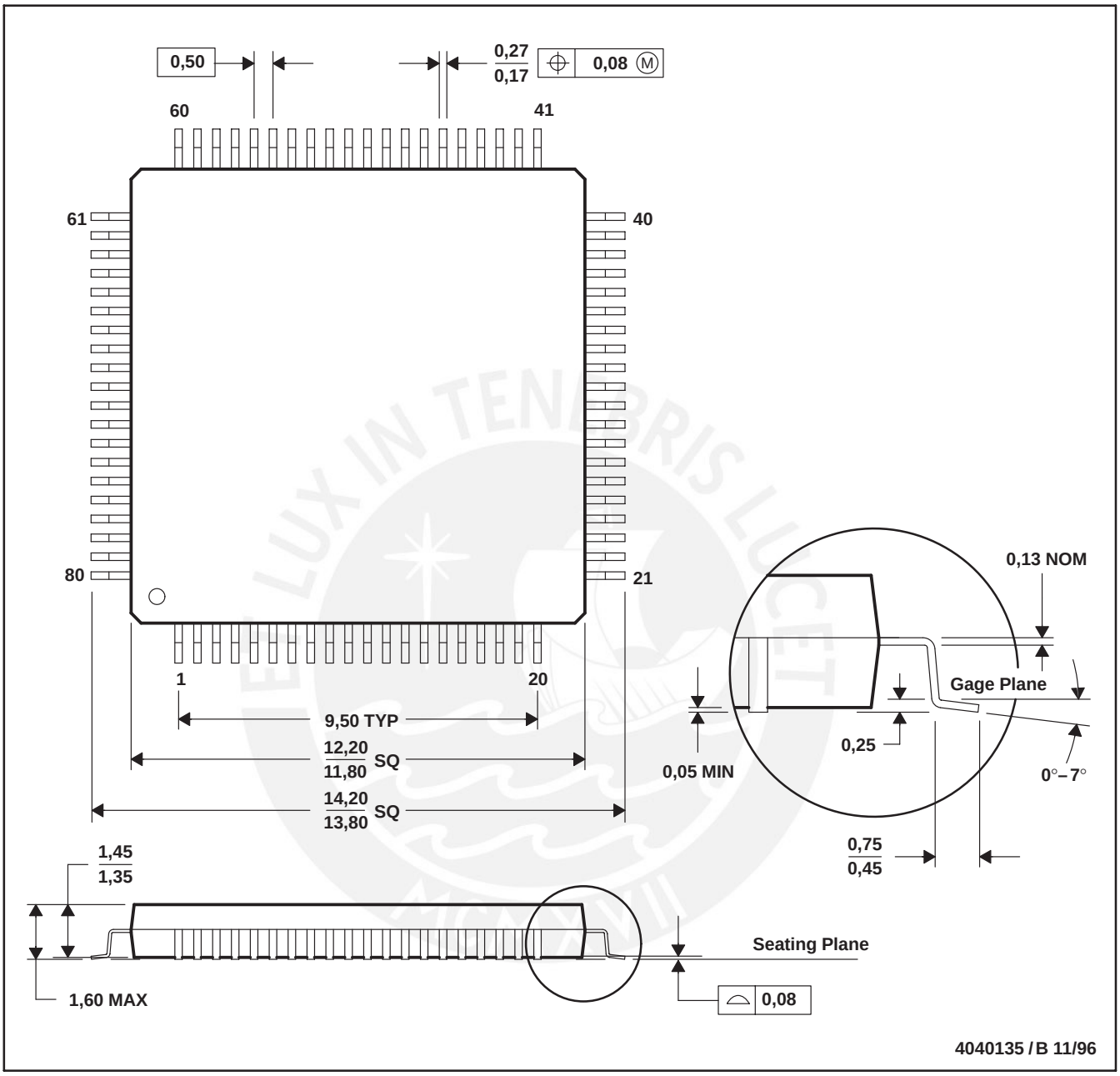
MTQF008A – JANUARY 1995 – REVISED DECEMBER 1996

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

OVT OV528

Single Chip Camera-to-Serial Bridge

Last Modified: October 10, 2002
Document Version: 1.3

Contents

Figures

Tables

Features

General Features

- Low-cost, single-chip & low-powered solution for high resolution serial bus PDA/cellular phone camera accessory applications
- 3.3V I/O, 2.5V core, 64-pin/100-pin TQFP, 64-pin BGA
- No external DRAM required

Camera Interfaces

- OV76x0 VGA color digital cameras
- OV66x0 CIF color digital cameras
- 8-bit camera input interface
- Built-in down-sampling, clamping and windowing circuits for VGA/CIF/SIF/QCIF/160x128/80x64 image resolutions
- Built-in color conversion circuits for 4 gray/16 gray/256 gray/12-bit RGB/16-bit RGB/Pallet 256 RGB preview images

Serial Interfaces

- RS-232: 115.2K bps ~ 920K bps for transferring JPEG still pictures or 160x128 preview @8 bpp with 0.75~6 fps
- 4-wire serial bus: 1~2M bps for transferring JPEG still pictures or SIF (320x240) preview @4 bpp with 6~8 fps

The Compression Engine

- JPEG CODEC with variable quality settings for different resolutions

Miscellaneous

- Serial camera control bus
- General purpose I/O pins
- Built-in Micro Controller (MC)
- Built-in PLL

OV528-64 vs. OV528-100

Table 1. OV528-64 vs. OV528-100

		OV528-64	OV528-100
Physical Difference	Pin	64-pin	100-pin
	MC Pins	Less MC Interface - Port: P2[0] - No Interrupt Pins - No Control Pins	More MC Interface - Port: P0[7:0], P2[7:0] - Interrupt: Int[1:0] - Control: WR_, RD_, ALE and PSEN_
		Fewer IO VDD & VSS(Total 7-pairs)	More IO VDD & VSS (Total 9-pairs)
		No Parallel I/F with program memory - No P_S	Parallel I/F with program memory - P_S
	GPIO Pins	Fewer GPIO(Total 8) - GPIO0[1], GPIO0[3], GPIO0[7:6] - GPIO1[3:0]	More GPIO(Total 15) - GPIO0[7:1] - GPIO1[7:0]
	ID Pins	Fewer ID pins (Total 4) - ID[3:0]	More ID pins(Total 7) - ID[6:0]
Functional Difference	Program Memory Interface	- Cannot support parallel interface with program memory - Cannot support optional program memory	- Supports parallel interface with program memory - Supports optional program memory for large program size (up to 64k)
	GPIO	- Total of 8 dedicated GPIO pins that can be used for general purpose I/O	- Total of 15 dedicated GPIO pins that can be used for general purpose I/O - P0[7:0] and P2[7:0] can be used for general purpose
	Serial ID	- Maximum 16 different IDs	- Maximum 128 different IDs

Architecture

General Description

The OV528 Serial Bus Camera System performs as a video camera or a JPEG compressed still camera and can be attached to a wireless or PDA host. When it performs as a video camera, the TFT-LCD panel of the host operates as a viewfinder. Users can send out a snapshot command from the host in order to capture a full resolution single-frame still picture. The picture is then compressed by the JPEG engine and transferred to the host.

Functional Description

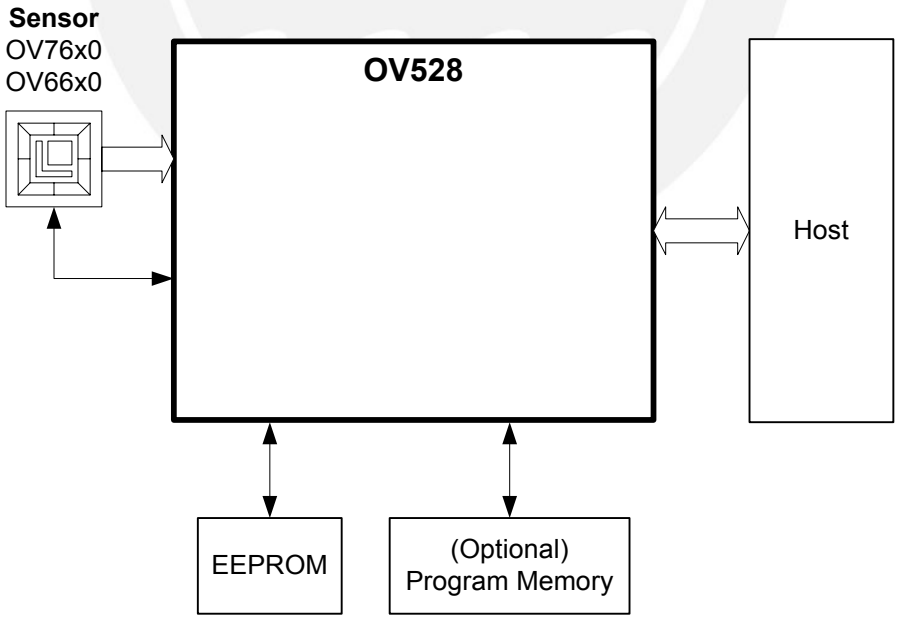
OV528, the Single Chip Camera-to-Serial Bridge, is a low-cost, single-chip & low-powered solution for high-resolution serial bus PDA/cellular phone camera accessory applications. Along with OV76x0/OV66x0 CMOS VGA/CIF color digital CameraChips, OV528 comprises a low-cost, highly integrated serial camera system. There is no additional DRAM required.

The OV528 system, as shown in Figure 1, consists of a CameraChip, Program Memory and OV528 Serial Bridge.

Camera Sensors

The OV528 supports OmniVision OV76x0/ and OV66x0 CameraChips with an 8-bit YC_bC_r interface.

Figure 1. System Block Diagram



Program Memory

A program memory is required for the embedded MC to respond to host commands correctly, as well as to store all necessary parameters for adjusting image/compression qualities. A serial type program memory is required for OV528, while both serial and parallel types of program memory can be adapted to OV528-100.

The contents of the program memory can be updated on the fly.

OV528 Serial Bridge

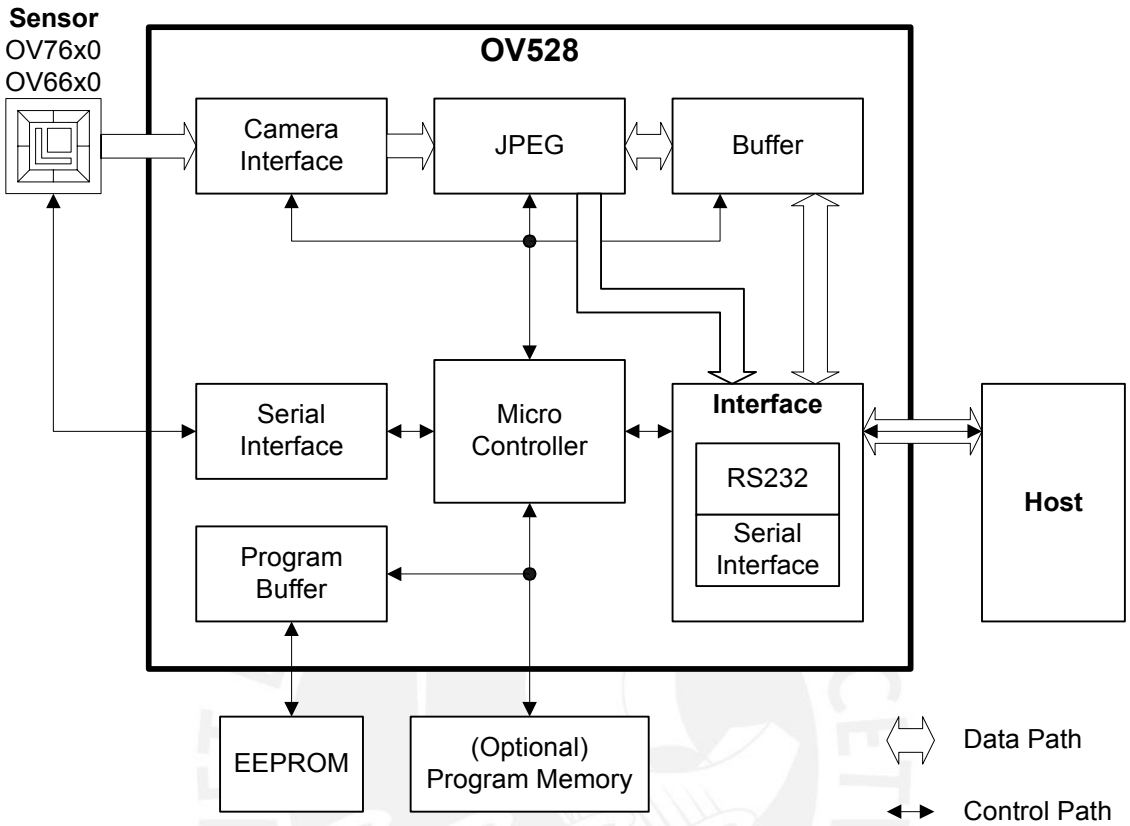
The OV528 Serial Bridge is a controller chip that can transfer image data from CameraChips to wireless/PDA hosts.

The OV528 takes 8-bit YC_bC_r 422 progressive video data from an OV76x0/OV66x0 CameraChip. The camera interface synchronizes with input video data and performs down-sampling, clamping and windowing functions with desired resolution, as well as color conversion that is requested by the user through serial bus host commands.

The JPEG CODEC with variable quality settings can achieve higher compression ratio & better image quality for various image resolutions.

The Serial Camera Control Bus is used to achieve greater flexibility in camera interface.

Figure 2. Functional Block Diagram



Pin Definitions

Pin Assignments

Figure 3. OV528-T64 Pin Assignment

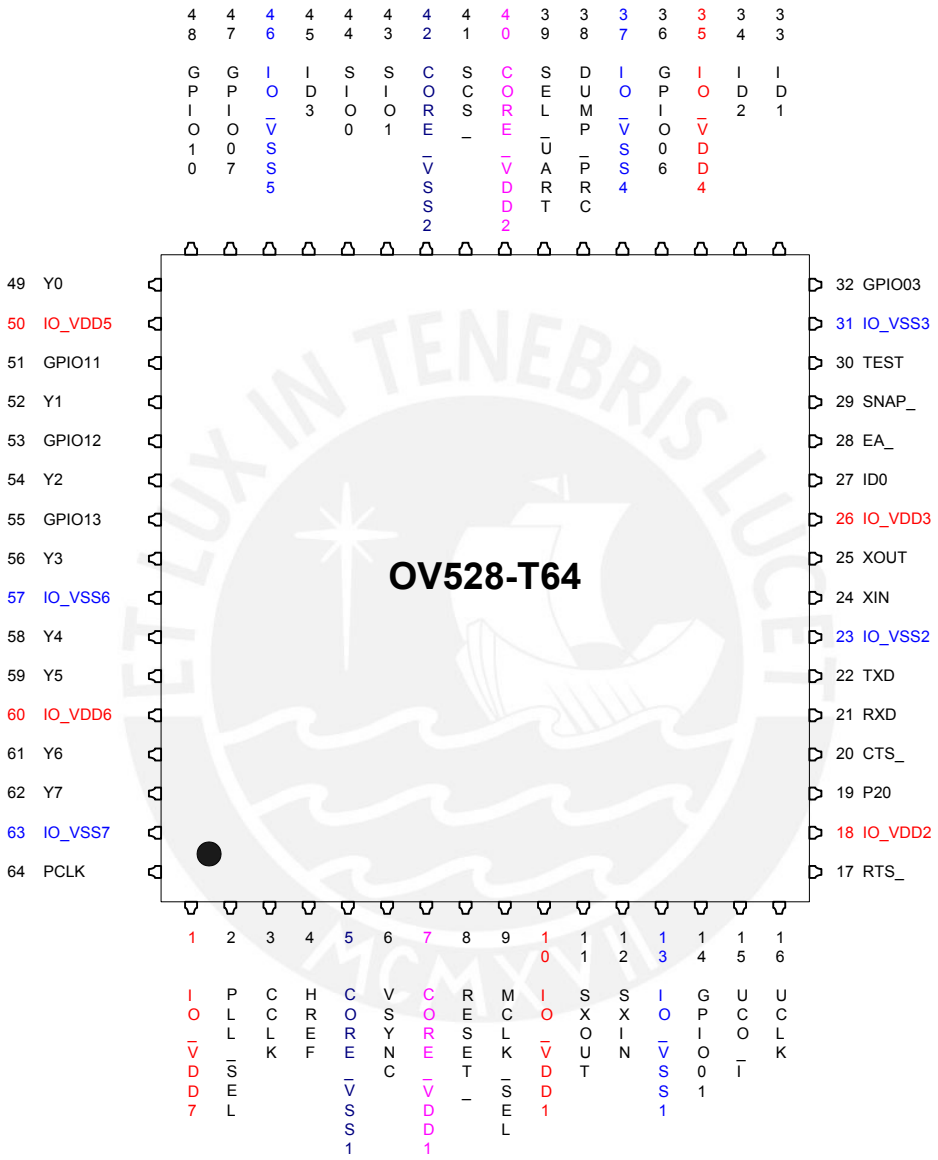
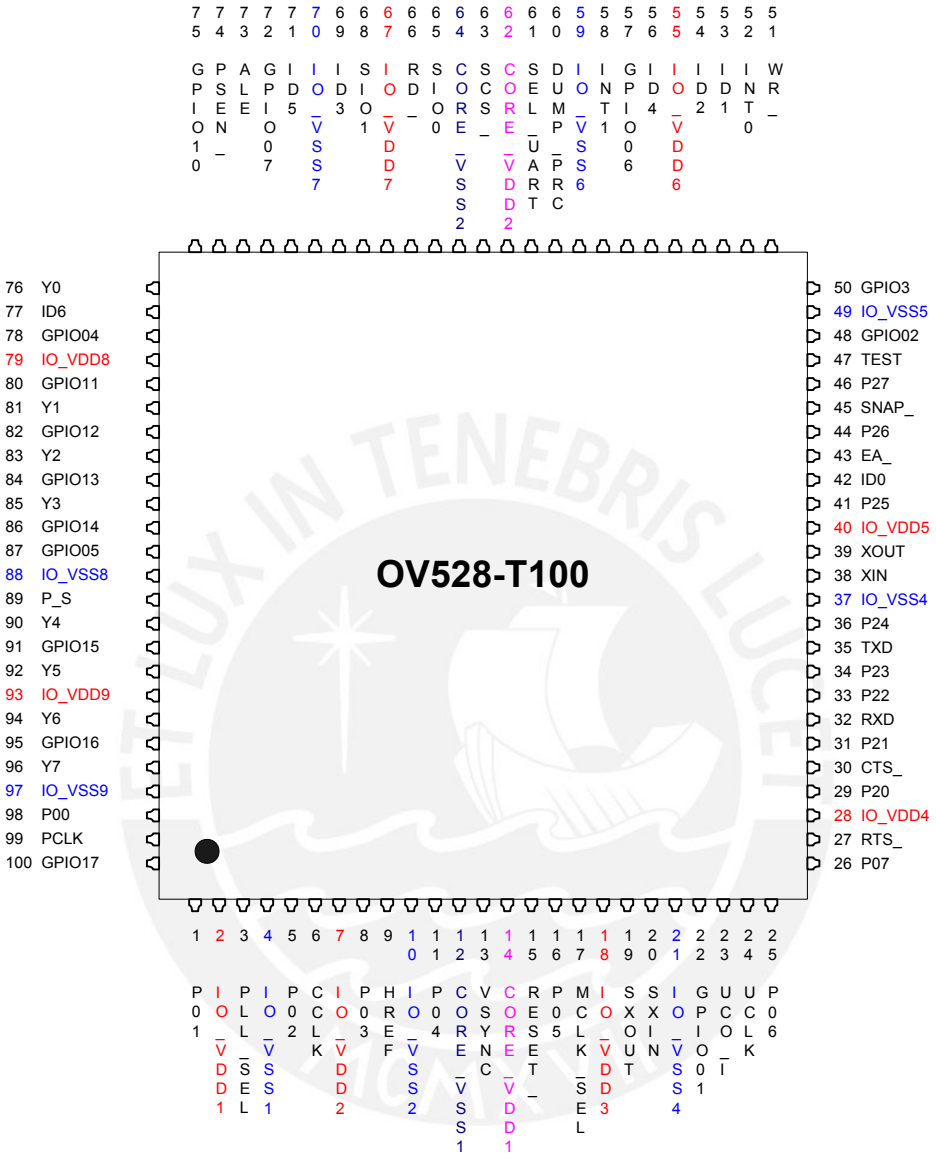


Figure 4. OV528-T100 Pin Assignment



OV528-T64 Pin Descriptions

Table 2. OV528-T64 Pin Descriptions – All Pins in Numeric Order

Pin #	Name	I/O	Function
1	DVDD		Digital 3.3V power
2	PLL_SEL	I	PLL select
3	CCLK	O	Camera clock output
4	HREF	I	Camera horizontal window reference input
5	CVSS		Digital ground
6	VSYNC	I	Camera vertical sync input
7	CVDD		Digital 2.5V power
8	RESET_	I	Power-on reset input. Low-active
9	MCLK_SEL	I	Master clock select. 1 from internal PLL. 0 from 48MHz crystal
10	DVDD		Digital 3.3V power
11	SXOUT	O	Serial bus crystal output
12	SXIN	I	Serial bus crystal input
13	DVSS		Digital ground
14	GPIO0[1]	I/O	General purpose I/O port 0 bit 1
15	UCO_I	I	External/internal MC select. 0 for internal MC. Must select internal MC for OV528
16	UCLK	O	RS-232 master clock output
17	RTS_	I/O	RS-232 RTS_
18	DVDD		Digital 3.3V power
19	P2[0]	I/O	Internal MC port 2 bit 0
20	CTS_	I	RS-232 CTS_
21	RXD	I	RS-232 RXD
22	TXD	O	RS-232 TXD
23	DVSS		Digital ground
24	XIN	I	System crystal input
25	XOUT	O	System crystal output
26	DVDD		Digital 3.3V power
27	ID[0]	I/O	Serial program memory ID bit 0
28	EA_	I/O	Internal MC EA_
29	SNAP_	I	Snapshot button input. Low-active
30	TEST	I	Test mode enabled/disabled. 1 for enabled
31	DVSS		Digital ground
32	GPIO0[3]	I/O	General purpose I/O port 0 bit 3
33	ID[1]	I/O	Serial program memory ID bit 1
34	ID[2]	I/O	Serial program memory ID bit 2
35	DVDD		Digital 3.3V power
36	GPIO0[6]	I/O	General purpose I/O port 0 bit 6
37	DVSS		Digital ground
38	DUMP_PRC	I	Host programming enabled/disabled. 1 for enabled
39	SEL_UART_	I	Serial bus select. 0 for RS-232
40	CVDD		Digital 2.5V power
41	SCS_	O	Serial camera chip select output
42	CVSS		Digital ground
43	SIO1	O	Serial camera control signal 1

Pin #	Name	I/O	Function
44	SIO0	I/O	Serial camera control signal 0
45	ID[3]	I/O	Serial program memory ID bit 3
46	DVSS		Digital ground
47	GPIO0[7]	I/O	General purpose I/O port 0 bit 7
48	GPIO1[0]	I/O	General purpose I/O port 0 bit 0
49	Y[0]	I	Camera $Y/C_b/C_r$ input bit 0
50	DVDD		Digital 3.3V power
51	GPIO1[1]	I/O	General purpose I/O port 0 bit 1
52	Y[1]	I	Camera $Y/C_b/C_r$ input bit 0
53	GPIO1[2]	I/O	General purpose I/O port 0 bit 2
54	Y[2]	I	Camera $Y/C_b/C_r$ input bit 0
55	GPIO1[3]	I/O	General purpose I/O port 0 bit 3
56	Y[3]	I	Camera $Y/C_b/C_r$ input bit 0
57	DVSS		Digital ground
58	Y[4]	I	Camera $Y/C_b/C_r$ input bit 0
59	Y[5]	I	Camera $Y/C_b/C_r$ input bit 0
60	DVDD		Digital 3.3V power
61	Y[6]	I	Camera $Y/C_b/C_r$ input bit 0
62	Y[7]	I	Camera $Y/C_b/C_r$ input bit 0
63	DVSS		Digital ground
64	PCLK	I	Camera pixel clock input

Table 3. OV528-T64 Pin Descriptions – Camera Interface (12 pins)

Pin #	Name	I/O	Function
3	CCLK	O	Camera clock output
4	HREF	I	Camera horizontal window reference input
6	VSYNC	I	Camera vertical sync input
49, 52, 54, 56, 58, 59, 61, 62	Y[0:7]	I	Camera $Y/C_b/C_r$ inputs
64	PCLK	I	Camera pixel clock input

Table 4. OV528-T64 Pin Descriptions – Serial Camera Control Bus (3 pins)

Pin #	Name	I/O	Function
41	SCS_	O	Serial camera chip select output
43	SIO1	O	Serial camera control signal 1
44	SIO0	I/O	Serial camera control signal 0

Table 5. OV528-T64 Pin Descriptions – Serial Interface (4 pins)

Pin #	Name	I/O	Function
17	RTS_	I/O	RS-232 RTS_
20	CTS_	I	RS-232 CTS_
21	RXD	I	RS-232 RXD
22	TXD	O	RS-232 TXD

Table 6. OV528-T64 Pin Descriptions – Clock & Reset (7 pins)

Pin #	Name	I/O	Function
2	PLL_SEL	I	PLL select
8	RESET_	I	Power-on reset input. Low-active
11	SXOUT	O	Serial bus crystal output
12	SXIN	I	Serial bus crystal input
16	UCLK	O	RS-232 master clock output
24	XIN	I	System crystal input
25	XOUT	O	System crystal output

Table 7. OV528-T64 Pin Descriptions – Serial Program ID (4 pins)

Pin #	Name	I/O	Function
27, 33, 34, 45	ID[0:3]	I/O	Serial program memory ID bit 0~3

Table 8. OV528-T64 Pin Descriptions – GPIO (9 pins)

Pin #	Name	I/O	Function
14	GPIO0[1]	I/O	General purpose I/O port 0 bit 1
32	GPIO0[3]	I/O	General purpose I/O port 0 bit 3
36, 47	GPIO0[6:7]	I/O	General purpose I/O port 0 bit 6~7
48, 51, 53, 55	GPIO1[0:3]	I/O	General purpose I/O port 0 bit 0~3

Table 9. OV528-T64 Pin Descriptions – Misc. (6 pins)

Pin #	Name	I/O	Function
9	MCLK_SEL	I	Master clock select. 1 from internal PLL. 0 from 48MHz crystal
15	UCO_I	I	External/internal MC select. 0 for internal MC. Must select internal MC for OV528
29	SNAP_	I	Snapshot button input. Low-active
30	TEST	I	Test mode enabled/disabled. 1 for enabled
38	DUMP_PRC	I	Host programming enabled/disabled. 1 for enabled
39	SEL_UART_	I	Serial bus select. 0 for RS-232

Table 10. OV528-T64 Pin Descriptions – Internal MC I/O Ports (1 pin)

Pin #	Name	I/O	Function
19	P2[0]	I/O	Internal MC port 2 bit 0
28	EA_	I/O	Internal MC EA_

Table 11. OV528-T64 Pin Descriptions – Power & Ground (18 pins)

Pin #	Name	I/O	Function
1, 10, 18, 26, 35, 50, 60	DVDD		Digital 3.3V power
7, 40	CVDD		Digital 2.5V power
13, 23, 31, 37, 46, 57, 63	DVSS		Digital ground
5, 42	CVSS		Digital ground

OV528-T100 Pin Descriptions

Table 12. OV528-T100 Pin Descriptions – All Pins in Numeric Order

Pin #	Name	I/O	Function
1	P0[1]	I/O	Internal MC port 0 bit 1
2	DVDD		Digital 3.3V power
3	PLL_SEL	I	PLL select
4	DVSS		Digital ground
5	P0[2]	I/O	Internal MC port 0 bit 2
6	CCLK	O	Camera clock output
7	DVDD		Digital 3.3V power
8	P0[3]	I/O	Internal MC port 0 bit 3
9	HREF	I	Camera horizontal window reference input
10	DVSS		Digital ground
11	P0[4]	I/O	Internal MC port 0 bit 4
12	CVSS		Digital ground
13	VSYNC	I	Camera vertical sync input
14	CVDD		Digital 2.5V power
15	RESET_	I	Power-on reset input. Low-active
16	P0[5]	I/O	Internal MC port 0 bit 5
17	MCLK_SEL	I	Master clock select. 1 from internal PLL. 0 from 48MHz crystal
18	DVDD		Digital 3.3V power
19	SXOUT	O	Serial bus crystal output
20	SXIN	I	Serial bus crystal input
21	DVSS		Digital ground
22	GPIO0[1]	I/O	General purpose I/O port 0 bit 1
23	UCO_I	I	External/internal MC select. 0 for internal MC
24	UCLK	O	RS-232 master clock output
25	P0[6]	I/O	Internal MC port 0 bit 6
26	P0[7]	I/O	Internal MC port 0 bit 7
27	RTS_	I/O	RS-232 RTS_
28	DVDD		Digital 3.3V power
29	P2[0]	I/O	Internal MC port 2 bit 0
30	CTS_	I	RS-232 CTS_
31	P2[1]	I/O	Internal MC port 2 bit 1
32	RXD	I	RS-232 RXD
33	P2[2]	I/O	Internal MC port 2 bit 2
34	P2[3]	I/O	Internal MC port 2 bit 3
35	TXD	O	RS-232 TXD
36	P2[4]	I/O	Internal MC port 2 bit 4
37	DVSS		Digital ground
38	XIN	I	System crystal input
39	XOUT	O	System crystal output
40	DVDD		Digital 3.3V power
41	P2[5]	I/O	Internal MC port 2 bit 5
42	ID[0]	I/O	Serial program memory ID bit 0
43	EA_	I	Internal MC EA_
44	P2[6]	I/O	Internal MC port 2 bit 6

Pin #	Name	I/O	Function
45	SNAP_	I	Snapshot button input. Low-active
46	P2[7]	I/O	Internal MC port 2 bit 7
47	TEST	I	Test mode enabled/disabled. 1 for enabled
48	GPIO0[2]	I/O	General purpose I/O port 0 bit 2
49	DVSS		Digital ground
50	GPIO0[3]	I/O	General purpose I/O port 0 bit 3
51	WR_	I/O	Internal MC WR_
52	INT0_	O	Internal MC INT0_
53	ID[1]	I/O	Serial program memory ID bit 1
54	ID[2]	I/O	Serial program memory ID bit 2
55	DVDD		Digital 3.3V power
56	ID[4]	I/O	Serial program memory ID bit 4
57	GPIO0[6]	I/O	General purpose I/O port 0 bit 6
58	INT1_	O	Internal MC INT1_
59	DVSS		Digital ground
60	DUMP_PRC	I	Host programming enabled/disabled. 1 for enabled
61	SEL_UART_	I	Serial bus select. 0 for RS-232
62	CVDD		Digital 2.5V power
63	SCS_	O	Serial camera chip select output
64	CVSS		Digital ground
65	SIO1	O	Serial camera control signal 1
66	RD_	I/O	Internal MC RD_
67	DVDD		Digital 3.3V power
68	SIO0	I/O	Serial camera control signal 0
69	ID[3]	I/O	Serial program memory ID bit 3
70	DVSS		Digital ground
71	ID[5]	I/O	Serial program memory ID bit 5
72	GPIO0[7]	I/O	General purpose I/O port 0 bit 7
73	ALE	I/O	Internal MC ALE
74	PSEN_	O	Internal MC PSEN_
75	GPIO1[0]	I/O	General purpose I/O port 0 bit 0
76	Y[0]	I	Camera Y/C_b/C_r input bit 0
77	ID[6]	I/O	Serial program memory ID bit 6
78	GPIO0[4]	I/O	General purpose I/O port 0 bit 4
79	DVDD		Digital 3.3V power
80	GPIO1[1]	I/O	General purpose I/O port 0 bit 1
81	Y[1]	I	Camera Y/C_b/C_r input bit 1
82	GPIO1[2]	I/O	General purpose I/O port 0 bit 2
83	Y[2]	I	Camera Y/C_b/C_r input bit 2
84	GPIO1[3]	I/O	General purpose I/O port 0 bit 3
85	Y[3]	I	Camera Y/C_b/C_r input bit 3
86	GPIO1[4]	I/O	General purpose I/O port 0 bit 4
87	GPIO0[5]	I/O	General purpose I/O port 0 bit 5
88	DVSS		Digital ground
89	P_S	I	Serial/parallel program memory select. 1 for parallel. 0 for serial
90	Y[4]	I	Camera Y/C_b/C_r input bit 4
91	GPIO1[5]	I/O	General purpose I/O port 0 bit 5

Pin #	Name	I/O	Function
92	Y[5]	I	Camera Y/C_b/C_r input bit 5
93	DVDD		Digital 3.3V power
94	Y[6]	I	Camera Y/C_b/C_r input bit 6
95	GPIO1[6]	I/O	General purpose I/O port 0 bit 6
96	Y[7]	I	Camera Y/C_b/C_r input bit 7
97	DVSS		Digital ground
98	P0[0]	I/O	Internal MC port 0 bit 0
99	PCLK	I	Camera pixel clock input
100	GPIO1[7]	I/O	General purpose I/O port 0 bit 7

Table 13. OV528-T100 Pin Descriptions – Camera Interface (12 pins)

Pin #	Name	I/O	Function
6	CCLK	O	Camera clock output
9	HREF	I	Camera horizontal window reference input
13	VSYNC	I	Camera vertical sync input
76, 81, 83, 85, 90, 92, 94, 96	Y[0:7]	I	Camera Y/C_b/C_r inputs
99	PCLK	I	Camera pixel clock input

Table 14. OV528-T100 Pin Descriptions – Serial Camera Control Bus (3 pins)

Pin #	Name	I/O	Function
63	SCS_	O	Serial camera chip select output
65	SIO1	O	Serial camera control signal 1
68	SIO0	I/O	Serial camera control signal 0

Table 15. OV528-T100 Pin Descriptions – Serial Interface (4 pins)

Pin #	Name	I/O	Function
27	RTS_	I/O	RS-232 RTS_
30	CTS_	I	RS-232 CTS_
32	RXD	I	RS-232 RXD
35	TXD	O	RS-232 TXD

Table 16. OV528-T100 Pin Descriptions – Clock & Reset (7 pins)

Pin #	Name	I/O	Function
3	PLL_SEL	I	PLL select
15	RESET_	I	Power-on reset input. Low-active
19	SXOUT	O	Serial bus crystal output
20	SXIN	I	Serial bus crystal input
24	UCLK	O	RS-232 master clock output
38	XIN	I	System crystal input
39	XOUT	O	System crystal output

Table 17. OV528-T100 Pin Descriptions – Serial Program ID (7 pins)

Pin #	Name	I/O	Function
42, 53, 54, 69, 56, 71, 77	ID[0:6]	I/O	Serial program memory ID bit 0~6

Table 18. OV528-T100 Pin Descriptions – GPIO (15 pins)

Pin #	Name	I/O	Function
22, 48, 50, 78, 87, 57, 72	GPIO0[1:7]	I/O	General purpose I/O port 0 bit 1~7
75, 80, 82, 84, 86, 91, 95, 100	GPIO1[0:7]	I/O	General purpose I/O port 0 bit 0~7

Table 19. OV528-T100 Pin Descriptions – Misc. (7 pins)

Pin #	Name	I/O	Function
17	MCLK_SEL	I	Master clock select. 1 from internal PLL. 0 from 48MHz crystal
23	UCO_I	I	External/internal MC select. 0 for internal MC
45	SNAP_	I	Snapshot button input. Low-active
47	TEST	I	Test mode enabled/disabled. 1 for enabled
60	DUMP_PRC	I	Host programming enabled/disabled. 1 for enabled
61	SEL_UART_	I	Serial bus select. 0 for RS-232
89	P_S	I	Serial/parallel program memory select. 1 for parallel. 0 for serial

Table 20. OV528-T100 Pin Descriptions –Internal MC I/O Ports (23 pins)

Pin #	Name	I/O	Function
98, 1, 5, 8, 11, 16, 25, 26	P0[0:7]	I/O	Internal MC port 0 bit 0~7
29, 31, 33, 34, 36, 41, 44, 46	P2[0:7]	I/O	Internal MC port 2 bit 0~7
43	EA_	I	Internal MC EA_
51	WR_	I/O	Internal MC WR_
52	INT0_	O	Internal MC INT0_
58	INT1_	O	Internal MC INT1_
66	RD_	I/O	Internal MC RD_
73	ALE	I/O	Internal MC ALE
74	PSEN_	O	Internal MC PSEN_

Table 21. OV528-T100 Pin Descriptions – Power & Ground (22 pins)

Pin #	Name	I/O	Function
2, 7, 18, 28, 40, 55, 67, 79, 93	DVDD		Digital 3.3V power
14, 62	CVDD		Digital 2.5V power
4, 10, 21, 37, 49, 59, 70, 88, 97	DVSS		Digital ground
12, 64	CVSS		Digital ground

OV528-B64 Pin Descriptions

Table 22. OV528-B64 Pin Descriptions – All Pins in Numeric Order

Pin #	Name	I/O	Function
A1	GPIO1[0]	I/O	General purpose I/O port 0 bit 0
A2	GPIO0[7]	I/O	General purpose I/O port 0 bit 7
A3	ID[3]	I/O	Serial program memory ID bit 3
A4	CVSS	GND	Digital ground
A5	DUMP_PRC	I	Host programming enabled/disabled. 1 for enabled
A6	DVDD	PWR	Digital 3.3V power
A7	ID[1]	I/O	Serial program memory ID bit 1
A8	GPIO0[3]	I/O	General purpose I/O port 0 bit 3
B1	DVDD	PWR	Digital 3.3V power
B2	Y[0]	I	Camera Y/C_b/C_r input bit 0
B3	SIO1	O	Serial camera control signal 1
B4	SCS_	O	Serial camera chip select output
B5	SEL_UART_	I	Serial bus select. 0 for RS-232
B6	GPIO0[6]	I/O	General purpose I/O port 0 bit 6
B7	ID[2]	I/O	Serial program memory ID bit 2
B8	TEST	I	Test mode enabled/disabled. 1 for enabled
C1	Y[1]	I	Camera Y/C_b/C_r input bit 1
C2	GPIO1[1]	I/O	General purpose I/O port 0 bit 1
C3	SIO0	I/O	Serial camera control signal 0
C4	CVDD	PWR	Digital 2.5V power
C5	DVSS	GND	Digital ground
C6	ID[0]	I/O	Serial program memory ID bit 0
C7	EA_	I/O	Internal MC EA_
C8	SNAP_	I	Snapshot button input. Low-active
D1	GPIO1[3]	I/O	General purpose I/O port 0 bit 3
D2	Y[2]	I	Camera Y/C_b/C_r input bit 2
D3	GPIO1[2]	I/O	General purpose I/O port 0 bit 2
D4	DVSS	GND	Digital ground
D5	DVSS	GND	Digital ground
D6	XIN	I	System crystal input
D7	XOUT	O	System crystal output
D8	DVDD	PWR	Digital 3.3V power
E1	Y[5]	I	Camera Y/C_b/C_r input bit 3
E2	Y[3]	I	Camera Y/C_b/C_r input bit 4
E3	DVSS	GND	Digital ground
E4	DVSS	GND	Digital ground
E5	DVSS	GND	Digital ground
E6	TXD	O	RS-232 TXD
E7	CTS_	I	RS-232 CTS_
E8	RXD	I	RS-232 RXD
F1	Y[6]	I	Camera Y/C_b/C_r input bit 6
F2	DVDD	PWR	Digital 3.3V power
F3	Y[4]	I	Camera Y/C_b/C_r input bit 4
F4	CVDD	PWR	Digital 2.5V power

Pin #	Name	I/O	Function
F5	DVDD	PWR	Digital 3.3V power
F6,	DVSS	GND	Digital ground
F7	DVDD	PWR	Digital 3.3V power
F8	P2[0]	I/O	Internal MC port 2 bit 0
G1	Y[7]	I	Camera Y/C_b/C_r input bit 7
G2	PLL_SEL	I	PLL select
G3	HREF	I	Camera horizontal window reference input
G4	CVSS	GND	Digital ground
G5	RESET_	I	Power-on reset input. Low-active
G6	SXOUT	O	Serial bus crystal output
G7	UCO_I	I	External/internal MC select. 0 for internal MC. Must select internal MC for OV528
G8	RTS_	I/O	RS-232 RTS_
H1	PCLK	I	Camera pixel clock input
H2	DVDD	PWR	Digital 3.3V power
H3	CCLK	O	Camera clock output
H4	VSYNC	I	Camera vertical sync input
H5	MCLK_SEL	I	Master clock select. 1 from internal PLL. 0 from 48MHz crystal
H6	SXIN	I	Serial bus crystal input
H7	GPIO0[1]	I/O	General purpose I/O port 0 bit 1
H8	UCLK	O	RS-232 master clock output

Table 23. OV528-B64 Pin Descriptions – Camera Interface (12 pins)

Pin #	Name	I/O	Function
H3	CCLK	O	Camera clock output
G3	HREF	I	Camera horizontal window reference input
H4	VSYNC	I	Camera vertical sync input
B2, C1, D2, E2, F3, E1, F1, G1	Y[0:7]	I	Camera Y/C_b/C_r inputs
H1	PCLK	I	Camera pixel clock input

Table 24. OV528-B64 Pin Descriptions – Serial Camera Control Bus (3 pins)

Pin #	Name	I/O	Function
B4	SCS_	O	Serial camera chip select output
B3	SIO1	O	Serial camera control signal 1
C3	SIO0	I/O	Serial camera control signal 0

Table 25. OV528-B64 Pin Descriptions – Serial Interface (4 pins)

Pin #	Name	I/O	Function
G8	RTS_	I/O	RS-232 RTS_
E7	CTS_	I	RS-232 CTS_
E8	RXD	I	RS-232 RXD
E6	TXD	O	RS-232 TXD

Table 26. OV528-B64 Pin Descriptions – Clock & Reset (7 pins)

Pin #	Name	I/O	Function
G2	PLL_SEL	I	PLL select
G5	RESET_	I	Power-on reset input. Low-active
G6	SXOUT	O	Serial bus crystal output
H6	SXIN	I	Serial bus crystal input
H8	UCLK	O	RS-232 master clock output
D6	XIN	I	System crystal input
D7	XOUT	O	System crystal output

Table 27. OV528-B64 Pin Descriptions – Serial Program ID (4 pins)

Pin #	Name	I/O	Function
C6, A7, B7, A3	ID[0:3]	I/O	Serial program memory ID bit 0~3

Table 28. OV528-B64 Pin Descriptions – GPIO (9 pins)

Pin #	Name	I/O	Function
H7	GPIO0[1]	I/O	General purpose I/O port 0 bit 1
A8	GPIO0[3]	I/O	General purpose I/O port 0 bit 3
B6, A2	GPIO0[6:7]	I/O	General purpose I/O port 0 bit 6~7
A1, C2, D3, D1	GPIO1[0:3]	I/O	General purpose I/O port 0 bit 0~3

Table 29. OV528-B64 Pin Descriptions – Misc. (6 pins)

Pin #	Name	I/O	Function
H5	MCLK_SEL	I	Master clock select. 1 from internal PLL. 0 from 48MHz crystal
G7	UCO_I	I	External/internal MC select. 0 for internal MC. Must select internal MC for OV528
C8	SNAP_	I	Snapshot button input. Low-active
B8	TEST	I	Test mode enabled/disabled. 1 for enabled
A5	DUMP_PRC	I	Host programming enabled/disabled. 1 for enabled
B5	SEL_UART_	I	Serial bus select. 0 for RS-232

Table 30. OV528-B64 Pin Descriptions – Internal MC I/O Ports (2 pins)

Pin #	Name	I/O	Function
F8	P2[0]	I/O	Internal MC port 2 bit 0
C7	EA_	I/O	Internal MC EA_

Table 31. OV528-B64 Pin Descriptions – Power & Ground (18 pins)

Pin #	Name	I/O	Function
H2, F5, F7, D8, A6, B1, F2	DVDD		Digital 3.3V power
F4, C4	CVDD		Digital 2.5V power
C5, D4, D5, E3, E4, E5, F6,	DVSS		Digital ground
G4, A4	CVSS		Digital ground

Electrical Characteristics

Table 32. DC Electrical Characteristics
V_{DD} = 3.3V±10%, TA = 0 to 125°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage	CMOS	0.7xV_{DD}			V
V_{IH}	High level input voltage	TTL	2.0			V
V_{IL}	Low level input voltage	CMOS			0.3xV_{DD}	V
V_{IL}	Low level input voltage	TTL			0.8	V
V_{OH}	High level output voltage		2.4		V_{DD}	V
V_{OL}	Low level output voltage			0.2	0.4	V
Is	Suspend Current	Suspend		90		uA
Io	Normal Operation Current	Operating		55		mA

Table 33. Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{DD}	DC supply voltage 3.3V (I/O)	3.0 to 3.6	V
V_{CC}	DC supply voltage 2.5V (core)	2.25 to 2.75	V
T_A	Commercial temperature	0 to 125	°C

Register Table & Command Set

Register Table

Table 34. Register List

Register Address	Register Name	R/W	Function	Default Value
00h	CID	RW	Chip ID Default ID is for OV528. Users can use this register for sensor ID.	28h
01h	HSB	RW	Horizontal start byte of image windowing	01h
02h	VSB	RW	Vertical start byte of image windowing	01h
03h	HPL	RW	Horizontal pixel length. The pixel length = HPL*4. The default horizontal pixel length is 640	A0h
04h	VPL	RW	Vertical pixel length. The pixel length = VPL*4. The default vertical pixel length is 480	78h
05h	PLC	RW	Polarity control Bit 7~3: Reserved Bit 2: PCLK Bit 1: HREF Bit 0: VSYNC 0: inverted 1: normal	03h
06h	IDC	RW	Bit 7: Enable Bit 6~0: Image disable counter. After sensor starting, users can decide how many frames to discard before capturing.	81h
07h	RSVD	RW	Reserved	00h
08h	JPC	RW	JPEG control Bit 7: global JPEG enable Bit 6: JPEG decoder enable Bit 5~1: JPEG control setting Bit 0: JPEG encoder enable Please use only those value below 00h: update quantization table 9Fh: encoding BEh: stop encoding C2h: decoding 82h: stop decoding	00h
09h	PVC	RW	Preview control Bit 7: Snapshot button status. Read only 3Fh: start 00h: stop	00h
0Ah	HBB	RW	Buffer transfer size – high byte (Real_Size/2)	28h
0Bh	LBB	RW	Buffer transfer size – low byte (Real_Size/2)	15h

Register Address	Register Name	R/W	Function	Default Value
0Ch	SBC	RW	Serial bus control Bit 7: RTS_ polarity control 0: inverted 1: normal Bit 6: Phase control Bit 5: Bit ordering 0: low bit first 1: high bit first Bit 4: TXD/RXD polarity control 0: inverted 1: normal Bit 3: MC program control 0: normal 1: download via serial bus Bit 2~0: serial bus control enabled/disabled 7h: enabled others: disabled	1Fh
0Dh	UBR	RW	RS-232 baud rate control Baud rate = SXIN / 2 / (UBR+1)	7Fh
0Eh	UDIV	RW	UCLK divider 80h: UCLK = XIN others: UCLK = XIN / 2 / (UDIV+1)	01h
0Fh	CDIV	RW	CCLK divider 80h: CCLK = XIN others: CCLK = XIN*2 / (CDIV+1)	01h
10h	CCC	RW	Color conversion control Bit 7: Reserved Bit 6~5: Down-sampling 0: normal 1: %2 2: %4 3: %8 Bit 4: Gray/Color select 0: gray 1: color Bit 3~2: Color select 0: 8-bit color 1: 12-bit color 2: 16-bit color 3: reserved Bit 1~0: Gray select 0: 4 gray 1: 16 gray 2: 256 gray 3: reserved	00h

Register Address	Register Name	R/W	Function	Default Value
11h	BFC	RW	Buffer control Bit 7: Reserved Bit 6: Write buffer failure table 0: enabled 1: disabled Bit 5~3: Buffer access mode 0: JPEG encoder access 3: MC access 4: JPEG decoder access others: forbidden Bit 2: Buffer failure table 0: disabled 1: enabled Bit 1: Address auto increment 0: disabled 1: enabled Bit 0: Write/read buffer 0: write 1: read	00h
12h	BWA	RW	Buffer failure table write address	00h
13h	HBWA	RW	High byte address for MC to access buffer	00h
14h	LBWA	RW	Low byte address for MC to access buffer	00h
15h	HBWD	RW	Highest byte of write data for buffer failure table	00h
16h	MBWD	RW	Middle byte of write data for buffer failure table	00h
17h	LBWD	RW	Lowest byte of write data for buffer failure table	00h
18h	HBRD	R	Highest byte of read data for buffer failure table	~
19h	MBRD	R	Middle byte of read data for buffer failure table	~
1Ah	LBRD	R	Lowest byte of read data for buffer failure table	~
1Bh	BAC	RW	Buffer access control 0: MC access 1: JPEG encoder access 2: JPEG decoder access others: forbidden	01h
1Ch	HBJPB	RW	High byte address of JPEG buffer for MC access	00h
1Dh	LBJPB	RW	Low byte address of JPEG buffer for MC access	00h
1Eh	HBJPWD	RW	High byte write data of JPEG buffer for MC access	00h
1Fh	LBJPWD	RW	Low byte write data of JPEG buffer for MC access	00h
20h	HBJPRD	R	High byte read data of JPEG buffer for MC access	~
21h	LBJPWD	R	Low byte read data of JPEG buffer for MC access	~
22h	HBBWD	RW	High byte write data of buffer for MC access	00h
23h	LBBWD	RW	Low byte write data of buffer for MC access	00h
24h	HBBRD	R	High byte read data of buffer for MC access	~
25h	LBBRD	R	Low byte read data of buffer for MC access	~
26H	HBSRD	R	High byte read data of serial bus for MC access	~
27h	LBSRD	R	Low byte read data of serial bus for MC access	~

Register Address	Register Name	R/W	Function	Default Value
28h	CHC	RW	Chip control Bit 7~6: Reserved Bit 5: JPEG decoding 0: disabled 1: enabled Bit 4: Serial bus IN control 0: Read MC commands from the host 1: Read data from the host to buffer Bit 3~2: Serial bus OUT control 0: Write preview image to the host 1: Write JPEG still picture to the host 2: Write MC commands to the host Bit 1~0: JPEG encoding/Buffer transfer 0: Transfer data from the host to buffer 3: JPEG encoding	00h
29h	HBSWD	RW	High byte write data of serial bus for MC access	00h
2Ah	LBSWD	RW	Low byte write data of serial bus for MC access	00h
2Bh	CSD	R	Current data byte received from serial bus	~
2Ch	RSTC	W	Reset control Bit 2: Logic reset 0: reset 1: normal Bit 1: System reset 0: reset 1: normal Bit 0: Suspend 0: normal 1: suspend	06h
2Dh	RUST	RW	Resume start time	00h
2Eh	RUET	RW	Resume end time	00h
2Fh ~ 47h	RSVD	~	Reserved	~
48h	C0	RW	R matrix Y coefficient. R=C0*Y+C1* C_r+C2* C_b+ROF	40h
49h	C1	RW	R matrix C_r coefficient	00h
4Ah	C2	RW	R matrix C_b coefficient	58h
4Bh	ROF	RW	R matrix offset	00h
4Ch	C3	RW	G matrix Y coefficient. G=C3*Y+C4* C_r+C5* C_b+GOF	40h
4Dh	C4	RW	G matrix C_r coefficient	96h
4Eh	C5	RW	G matrix C_b coefficient	Adh
4Fh	GOF	RW	G matrix offset	00h
50h	C6	RW	B matrix Y coefficient. B=C6*Y+C7* C_r+C8* C_b+BOF	40h
51h	C7	RW	B matrix C_r coefficient	6Fh
52h	C8	RW	B matrix C_b coefficient	00h
53h	BOF	RW	B matrix offset	00h
54h	RSTP0	RW	R step conversion 0	24h
55h	RSTP1	RW	R step conversion 1	49h
56h	RSTP2	RW	R step conversion 2	6Dh
57h	RSTP3	RW	R step conversion 3	92h
58h	RSTP4	RW	R step conversion 4	B6h
59h	RSTP5	RW	R step conversion 5	DBh
5Ah	RSTP6	RW	R step conversion 6	FFh
5Bh	GSTP0	RW	G step conversion 0	24h
5Ch	GSTP1	RW	G step conversion 1	49h
5Dh	GSTP2	RW	G step conversion 2	6Dh
5Eh	GSTP3	RW	G step conversion 3	92h
5Fh	GSTP4	RW	G step conversion 4	B6h

Register Address	Register Name	R/W	Function	Default Value
60h	GSTP5	RW	G step conversion 5	DBh
61h	GSTP6	RW	G step conversion 6	FFh
62h	BSTP0	RW	B step conversion 0	55h
63h	BSTP1	RW	B step conversion 1	AAh
64h	BSTP2	RW	B step conversion 2	FFh
65h	CSS	RW	Chip select & status Bit 7: Serial bus received FIFO empty status. Read only Bit 6: Serial bus received FIFO full status. Read only Bit 5: Serial bus transmitted FIFO empty status. Read only Bit 4: Serial bus transmitted FIFO full status. Read only Bit 3: Reserved Bit 2: Chip select of program memory Bit 1: Chip select of buffer Bit 0: Chip select of JPEG buffer	08h
66h	HBSRC	R	Highest byte of serial bus received counter	~
67h	MBSRC	R	Middle byte of serial bus received counter	~
68h	LBSRC	R	Lowest byte of serial bus received counter	~
69h	HBSRI	RW	Highest byte of serial bus received interrupt counter	00h
6Ah	MBSRI	RW	Middle byte of serial bus received interrupt counter	00h
6Bh	LBSRI	RW	Lowest byte of serial bus received interrupt counter	08h
6Ch	HBSBTC	R	Highest byte of serial bus transmitted counter	~
6Dh	MBSBTC	R	Middle byte of serial bus transmitted counter	~
6Eh	LBSBTC	R	Lowest byte of serial bus transmitted counter	~
6Fh	HBSBTI	RW	Highest byte of serial bus transmitted interrupt counter	00h
70h	MBSBTI	RW	Middle byte of serial bus transmitted interrupt counter	00h
71h	LBSBTI	RW	Lowest byte of serial bus transmitted interrupt counter	08h
72h	QZC	RW	Quantization control Bit 7: Chroma quantization select 0: w/o rounding 1: w rounding Bit 6~4: Chroma quantization bias Bit 3: Luma quantization select 0: w/o rounding 1: w rounding Bit 2~0: Luma quantization bias	CCh
73h	SBD	RW	Snapshot de-bounce delay	10h
74h	INT0M	RW	MC external interrupt 0 mask Bit 7: Buffer overflow interrupt Bit 6: Serial bus receiving done interrupt Bit 5: Serial bus transmitting done interrupt Bit 4: JPEG decoding done interrupt Bit 3: JPEG encoding done interrupt Bit 2: Reserved Bit 1: Image start interrupt Bit 0: Snapshot interrupt	FFh
75h	INT0S	R	MC external interrupt 0 status	~
76h	HBPA	RW	High byte of MC program memory address	00h
77h	LBPA	RW	Low byte of MC program memory address	00h
78h	PWD	RW	MC program memory write data	00h
79h	PRD	R	MC program memory read data	~
7Ah	RSVD	RW	Reserved	00h
7Bh	SCCS	RW	SCCB speed control SCCB Clock = XIN/2/(SCCS+1)	13h

Register Address	Register Name	R/W	Function	Default Value
7Ch	SCCC	RW	SCCB command 0: Start, Perform SCCB start condition 1: Write Byte, Ship out SCCW from SIO0 by MSB first 2: Write Bit, Ship out SCCW[7] from SIO0 3: Read Byte, Store the data on SIO0 in SCCR by MSB first 4: Read Bit, Store the data on SIO0 in SCCR[0] 5: Stop, Perform SCCB stop condition 6: Toggle “scs_”, Reverse the current “scs_” signal 7: Idle	07h
7Dh	SCCW	RW	SCCB write data	00h
7Eh	SCCR	R	SCCB read data	~
7Fh	SCCB	R	SCCB busy Bit 7: busy 0: normal 1: busy	~
80h	INT1M	RW	MC external interrupt 1 mask Bit 7~2: Reserved Bit 1: SCCB ready Bit 0: JPEG decoder header done	FFh
81h	INT1S	R	MC external interrupt 1 status	~
82h	GPIO0R	R	GPIO0 read data	~
83h	GPIO0D	RW	GPIO0 direction control 0: output 1: input	FFh
84h	GPIO0W	RW	GPIO0 write data	0Fh
85h	GPIO1R	R	GPIO1 read data	~
86h	GPIO1D	RW	GPIO1 direction control 0: output 1: input	00h
87h	GPIO1W	RW	GPIO1 write data	AAh
88h	JPHS	RW	JPEG header size	14h
89h	HJPES	R	High byte of JPEG encoding size (Real_Size/4)	~
8Ah	LJPES	R	Low byte of JPEG encoding size (Real_Size/4)	~
8Bh	JPQTA	RW	JPEG quantization table address	00h
8Ch	JPQTW	RW	JPEG quantization table write data	00h

Register Address	Register Name	R/W	Function	Default Value
8Dh	JPSR	RW	JPEG status register Bit 7: Byte stuff 0: disabled 1: enabled Bit 6: Encoder table 0: disabled 1: enabled Bit 5: Quantization table 0: disabled 1: enabled Bit 4: Header 0: disabled 1: enabled Bit 3: Decoder one shot 0: disabled 1: enabled Bit 2: Encoder one shot 0: disabled 1: enabled Bit 1: Operation modes 0: encoding 1: decoding Bit 0: CODEC 0: enabled 1: disabled	04h
8Eh	HBJEBC	RW	High byte of JPEG encoder block count	1Ch
8Fh	LBJEBC	RW	Low byte of JPEG encoder block count	20h
90h	STCS	R	Serial bus transmitting checksum	~
91h	SRCS	R	Serial bus receiving checksum	~
92h	JQTRD	R	JPEG quantization table read data	~
93h	HBBRA	R	High byte of buffer read address	~
94h	LBBRA	R	Low byte of buffer read address	~
95h	SPC0	RW	Special Control Register 0 40h(160x128), 20h(80x64 for VGA), 3ah(80x64 for CIF), 80h(Other)	80h
96h	SPC1	RW	Special Control Register 1 00h(160x128), 00h(80x64 for VGA), 2eh(80x64 for CIF), 00h(Other)	00h
97h	SPC2	RW	Special Control Register 2 44h(160x128), 22h(80x64 for VGA), 38h(80x64 for CIF), 80h(Other)	80h
98h	SPC3	RW	Special Control Register 3 44h(160x128), 22h(80x64 for VGA), e3h(80x64 for CIF), 00h(Other)	00h
99h	SPC4	RW	Special Control Register 4 13h(160x128), 13h(80x64 for VGA), 13h(80x64 for CIF), 00h(Other)	00h
9Ah	SPC5	RW	Special Control Register 5 13h(160x128), 13h(80x64 for VGA), 13h(80x64 for CIF), 00h(Other)	00h

Example of Command Set

Users can define their own command sets by changing firmware and the host driver. This is a sample command set? This is the default command set?

Table 35. Command List

Command	ID Number	Parameter1	Parameter2	Parameter3	Parameter4
INITIAL	FFFFFF01h	Interface Speed	Preview Type	Preview Resolution	JPEG Resolution
DUMP	FFFFFF02h	00h	00h	00h	00h
SET REGISTER	FFFFFF03h	Address Low Byte	Address High Byte	Data Low Byte	Data High Byte
GET PICTURE	FFFFFF04h	Picture Type	Picture ID	00h	00h
SNAPSHOT	FFFFFF05h	Snapshot Type	Skip Frame Low Byte	Skip Frame High Byte	00h
SAVE DATA	FFFFFF06h	Destination	Length Byte 0	Length Byte 1	Picture ID/ Length Byte 2
Reserved	FFFFFF07h	~	~	~	~
RESET	FFFFFF08h	Reset Type	00h	00h	xxh*
POWER OFF	FFFFFF09h	00h	00h	00h	00h
DATA	FFFFFF0Ah	Data Type	Length Byte 0	Length Byte 1	Picture ID/ Length Byte 2
GET REGISTER	FFFFFF0Bh	Address Low Byte	Address High Byte	00h	00h
DOWNLOAD PROGRAM	FFFFFF0Ch	Destination	Length Byte 0	Length Byte 1	Length Byte 2
SYNC	FFFFFF0Dh	00h	00h	00h	00h
ACK	FFFFFF0Eh	Command ID	ACK counter	00h	00h
NAK	FFFFFF0Fh	00h	NAK counter	Error Number	00h

* If the parameter is FFh, the command is a special Reset command and the firmware performs it immediately.

INITIAL (FFFFFF01h)

The host issues this command to configure the OV528. After receiving this command, the OV528 programs its internal settings based on the MC firmware.

Interface Speed

Serial Interface Speed = System Clock Frequency / (2 * Interface Speed)

Table 36. RS-232 Baud Rate

Y12 (kHz)	Y13 (kHz)	Baud Rate Parameter	Baud Rate (Hz)	Description
12,000	SXIN=3,686.4	8	7,200	$3,686,400 / 2^{8+1}$
12,000	SXIN=3,686.4	7	14,400	$3,686,400 / 2^{7+1}$
12,000	SXIN=3,686.4	6	28,800	$3,686,400 / 2^{6+1}$
12,000	SXIN=3,686.4	5	57,600	$3,686,400 / 2^{5+1}$
12,000	SXIN=3,686.4	4	115,200	$3,686,400 / 2^{4+1}$
		…		
12,000	SXIN=4,915.2	8	9,600	$4,915,200 / 2^{8+1}$
12,000	SXIN=4,915.2	7	19,200	$4,915,200 / 2^{7+1}$
12,000	SXIN=4,915.2	6	38,400	$4,915,200 / 2^{6+1}$
12,000	SXIN=4,915.2	5	76,800	$4,915,200 / 2^{5+1}$
12,000	SXIN=4,915.2	4	153,600	$4,915,200 / 2^{4+1}$
		…		
14,745.6	SXIN=UCLK	8	7,200	$3,686,400 / 2^{8+1}$
14,745.6	SXIN=UCLK	7	14,400	$3,686,400 / 2^{7+1}$
14,745.6	SXIN=UCLK	6	28,800	$3,686,400 / 2^{6+1}$
14,745.6	SXIN=UCLK	5	57,600	$3,686,400 / 2^{5+1}$
14,745.6	SXIN=UCLK	4	115,200	$3,686,400 / 2^{4+1}$
		…		

Preview Type

4 gray scale	01h
16 gray scale	02h
256 gray scale	03h
8-bit color	04h
12-bit color	05h
16-bit color	06h
JPEG	07h

Preview Resolution for VGA Sensor

80 X 60	01h
160 X 120	03h
320 X 240	05h
640 X 480	07h

Preview Resolution for CIF Sensor

88 X 72	02h
176 X 144	04h
352 X 288	06h

JPEG Preview Resolution for VGA Sensor

80 X 64	01h
160 X 128	03h
320 X 240	05h
640 X 480	07h

JPEG Preview Resolution for CIF Sensor

80 X 64	02h
176 X 144	04h
352 X 288	06h

DUMP (FFFFFF02h)

OV528 resets all registers to default values after receiving this command.

SET REGISTER (FFFFFF03h)

The host can program OV528 internal registers by sending this command.

GET PICTURE (FFFFFF04h)

The host can get a picture from the OV528 by sending this command.

Picture Type

Snapshot Picture	01h
Preview Picture	02h
Serial Flash Picture	03h
Parallel Flash Picture	04h
JPEG Preview Picture	05h
Display Picture	06h

Picture ID

This parameter determines which picture is going to be sent out from external flash memory. The picture ID starts from 1.

SNAPSHOT (FFFFFF05h)

OV528 keeps a single frame of JPEG still picture data in the buffer after receiving this command.

Snapshot Type

Compressed Picture	00h
Uncompressed Picture	01h

Skip Frame Counter

The host can define the number of dropped frames before compression occurs. “0” keeps the current frame, “1” captures the next frame, and so forth.

SAVE DATA (FFFFFF06h)

The host can save data to the OV528 by sending this command.

Destination

Serial Bus to Data Memory	01h
Serial Bus to FIFO Memory	02h
Serial Bus to Serial Flash	03h
Serial Bus to Parallel Flash	04h
Data Memory to Serial Flash	05h
Data Memory to Parallel Flash	06h

Length Byte 1 and Length Byte 0

If data is saved from Data Memory to Serial/Parallel Flash memory and the picture ID starts from 1, those two bytes are 0000h. Alternatively, these two bytes represent the lower two bytes of saved data length.

Picture ID/Length Byte 2

If data is saved from Data Memory to Serial/Parallel Flash memory and the picture ID starts from 1, this byte represents the picture number. Or, this byte represents the highest byte of the saved data length.

RESET (FFFFFF08h)

The host can reset OV528 by issuing this command.

Reset Type

"00h" resets the whole system. OV528 will reboot and reset all registers and state machines. "01h" resets state machines only.

POWER OFF (FFFFFF09h)

The host can suspend OV528 by sending this command. OV528 will go into sleep mode after receiving this command. The host must send SYNC command (FFFFFF0Dh) to wake up OV528 for certain period until receiving ACK command from OV528.

DATA (FFFFFF0Ah)

The host receives data from OV528 by sending this command. The unit of length is bytes and doesn't include the command length.

Data Type

Register Data	00h
JPEG Picture	01h
Preview Picture	02h
Serial Flash Picture	03h
Parallel Flash Picture	04h
JPEG Preview Picture	05h
Display Picture	06h

Length Byte 1 and Length Byte 0

If the host received JPEG Picture, Preview Picture, Register or Flash Picture data along with the Picture ID 0, these two bytes represent the length of received data. Or(Otherwise?), these two bytes are 0000h.

Picture ID/Length Byte 2

If the host received Flash Picture data and the Picture ID starts from 1, this byte represents the Picture Number. Or, this byte is the highest byte of the length. Pls verifiy correct wording

GET REGISTER (FFFFFF0Bh)

The host can read the OV528 internal registers by sending this command. The OV528 will respond and send back the register value by using the DATA command (FFFFFF0Ah).

DOWNLOAD PROGRAM (FFFFFF0Ch)

The host can download a program to OV528 by sending this command. After downloading the program into the program memory of OV528, the host must send SYNC command for certain period and wait until it responses and sends ACK command to the host.

Destination

Program Memory: 05h

Length

These three bytes represent the lower two bytes of download length.

SYNC (FFFFFF0Dh)

Either the host or the OV528 can issue this command. ACK command (FFFFFF0Eh) must be sent out after receiving this command.

ACK (FFFFFF0Eh)

This command indicates a correct transmission. After receiving any valid command, ACK command must be sent out except when downloading program or getting preview data.

Command ID

The received command ID

ACK Count

A sequence-counter for ACK

NAK (FFFFFF0Fh)

This command indicates corrupted transmission or unsupported features.

NAK Count

A sequence-counter for NAK

Error Number

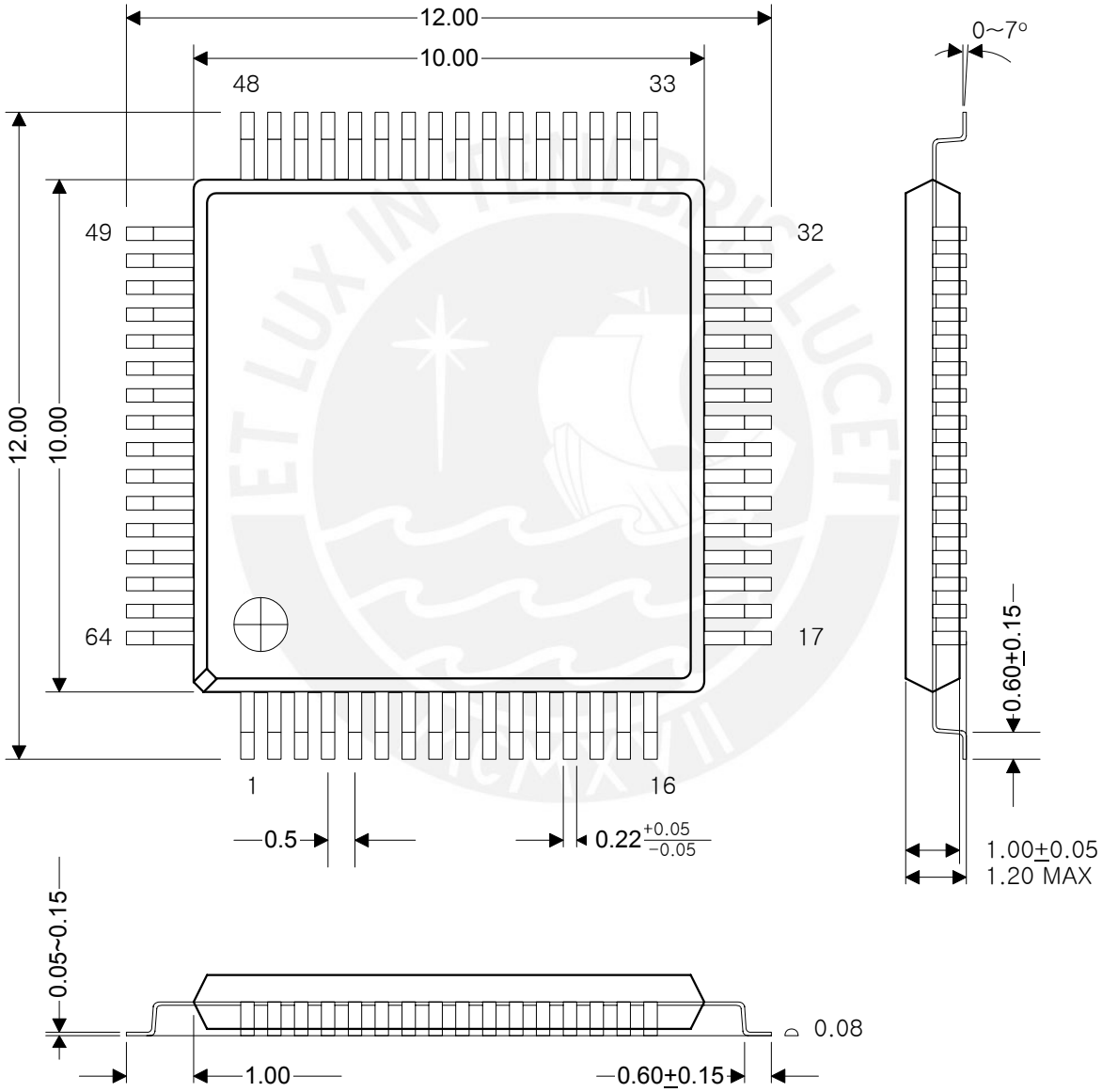
Error condition number

Mechanical Information

OV528-T64 Package

Figure 5. OV528-T64 Package

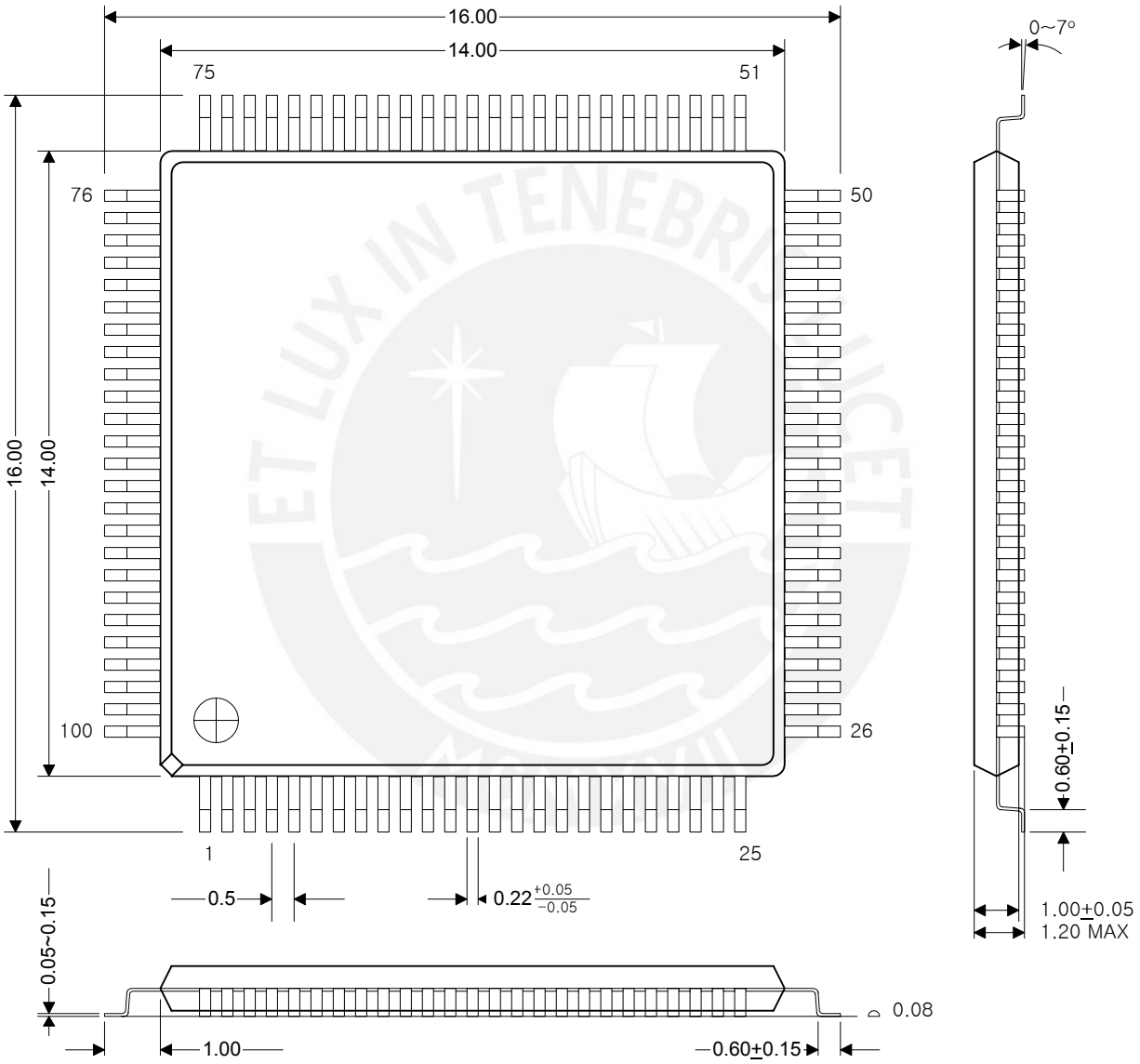
Dimension: mm



OV528-T100 Package

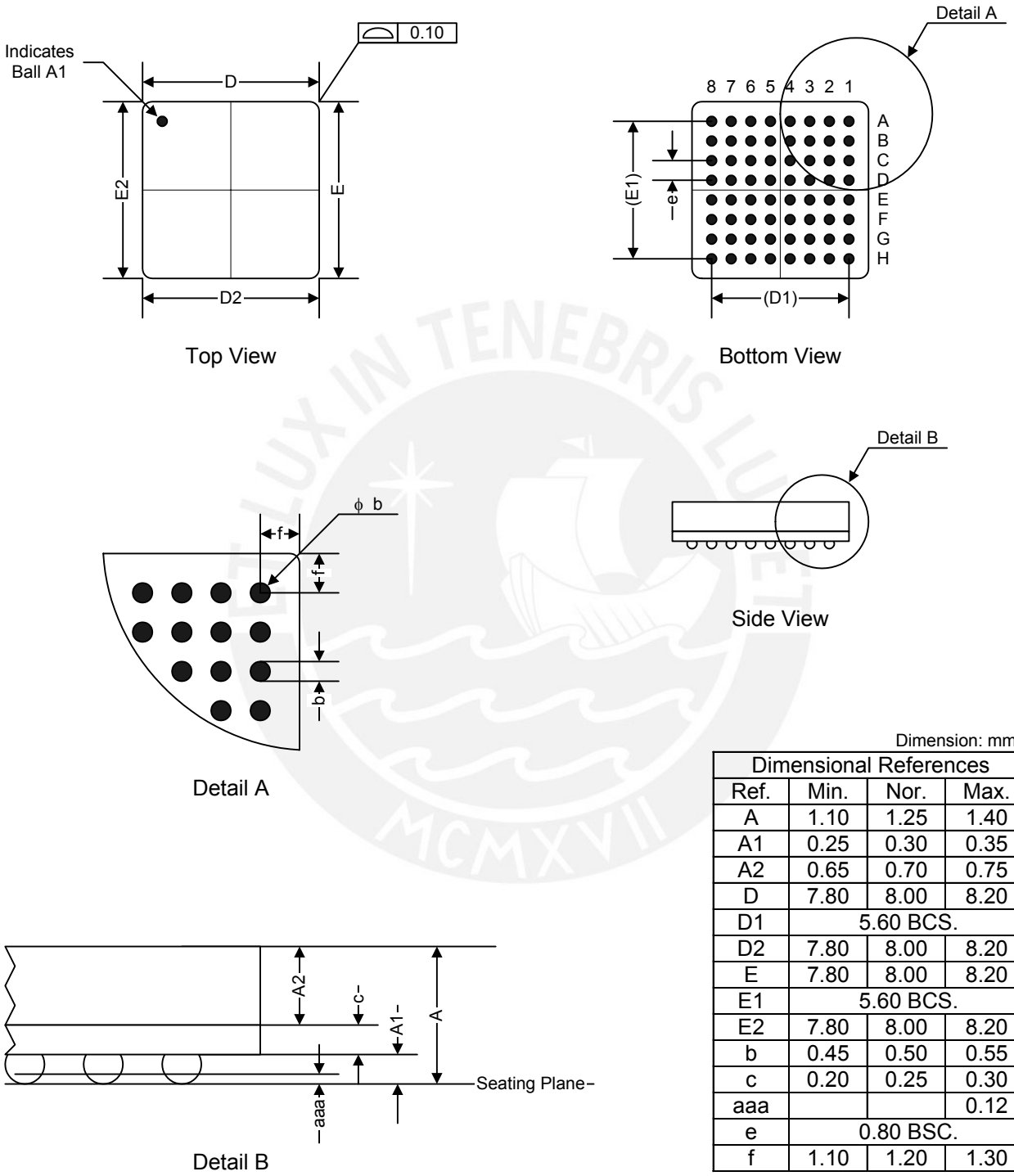
Figure 6. OV528-T100 Package

Dimension: mm



OV528-B64 Package

Figure 7. OV528-B64 Package



Dimension: mm

Dimensional References			
Ref.	Min.	Nor.	Max.
A	1.10	1.25	1.40
A1	0.25	0.30	0.35
A2	0.65	0.70	0.75
D	7.80	8.00	8.20
D1	5.60 BCS.		
D2	7.80	8.00	8.20
E	7.80	8.00	8.20
E1	5.60 BCS.		
E2	7.80	8.00	8.20
b	0.45	0.50	0.55
c	0.20	0.25	0.30
aaa			0.12
e	0.80 BSC.		
f	1.10	1.20	1.30

Revision History

Rev No.	Date	Author	Description
1.0	Apr. 10, 2002	Nicholas S. Nam Stripe Dibble	Initial Version
1.1	May 23, 2002	Nicholas S. Nam	Change Register Address FFxx -> xx (xx is register address)
1.2	Jun. 28, 2002	Nicholas S. Nam	Append Pin Descriptions for B64 & B100 Append Mechanical Information for B64 & B100
1.3	Oct. 10, 2002	Nicholas S. Nam	Removed Pin Descriptions for B100 Removed Mechanical Information for B100

OmniVision™

Advanced Information
Preliminary Datasheet

OV7640 Color CMOS VGA (640 x 480) CAMERACHIP™
OV7141 B&W CMOS VGA (640 x 480) CAMERACHIP™

General Description

The OV7640 (color) and OV7141 (black and white) CAMERACHIPS™ are low voltage CMOS image sensors that provide the full functionality of a single-chip VGA (640 x 480) camera and image processor in a small footprint package. The OV7640/OV7141 provides full-frame, sub-sampled or windowed 8-bit images in a wide range of formats, controlled through OmniVision's Serial Camera Control Bus (SCCB) interface.

This product family has an image array capable of operating at up to 30 frames per second (fps) with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control and more, are also programmable through the SCCB interface. In addition, OmniVision CAMERACHIPS use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination such as fixed pattern noise, smearing, blooming, etc. to produce a clean, fully stable color image.

Features

- High sensitivity for low-light operation
- 2.5V operating voltage for embedded portable applications
- Standard Serial Camera Control Bus (SCCB) interface
- VGA, QVGA (sub-sampled) and Windowed outputs with Raw RGB, RGB (GRB 4:2:2), YUV (4:2:2) and YCbCr (4:2:2) formats
- Automatic image control functions including: Automatic Exposure Control (AEC), Automatic Gain Control (AGC), Automatic White Balance (AWB), Automatic Brightness Control (ABC), Automatic Band Filter (ABF) for 60Hz noise and Automatic Black-Level Calibration (ABLC)
- Image quality controls including color saturation, hue, gamma, sharpness (edge enhancement), anti-blooming and zero smearing

Ordering Information

Product	Package
OV7640 (Color)	PLCC-28
OV7141 (B&W)	PLCC-28

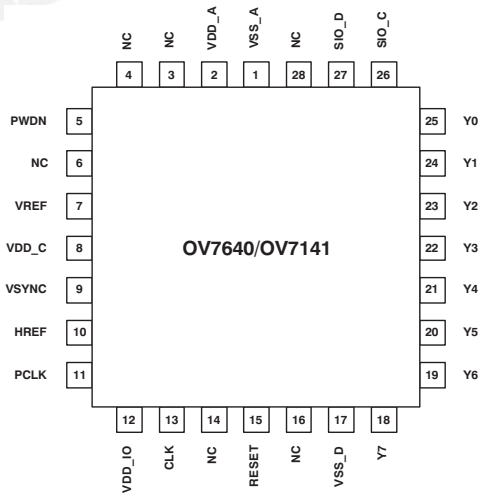
Applications

- Cellular and Picture Phones
- Toys
- PC Multimedia

Key Specifications

	Array Size	640 x 480 (VGA)
Power Supply	**Core**	2.5VDC ± 10%
	Analog	2.5VDC ± 4%
	I/O	2.25V to 3.3V
Power Requirements	**Active**	40 mW (30 fps, including I/O power)
	Standby	30 µW
Temperature Range	**Operation**	-10°C to 70°C
	Stable Image	0°C to 50°C
Output Formats (8-bit)		• YUV/YCbCr 4:2:2 • RGB 4:2:2 • Raw RGB Data
	Lens Size	1/4"
Maximum Image Transfer Rate	**VGA**	30 fps
	QVGA	60 fps
Sensitivity	**B&W**	3.0 V/Lux-sec
	Color	1.12 V/Lux-sec
	S/N Ratio	46 dB
	Dynamic Range	62 dB
	Scan Mode	Progressive/Interlaced
	Maximum Exposure Interval	523 x t_{ROW}
	Gamma Correction	0.45
	Pixel Size	5.6 µm x 5.6 µm
	Dark Current	30 mV/s
	Well Capacity	60 Ke
	Fixed Pattern Noise	< 0.03% of $V_{PEAK-TO-PEAK}$
	Image Area	3.6 mm x 2.7 mm
	Package Dimensions	11.43 mm x 11.43 mm

Figure 1 OV7640/OV7141 Pin Diagram



Functional Description

Figure 2 shows the functional block diagram of the OV7640/OV7141 image sensor. The OV7640/OV7141 includes:

- Image Sensor Array (640 x 480 resolution)
- Timing Generator
- Analog Processing Block
- A/D Converters
- Output Formatter
- Digital Video Port
- SCCB Interface

Figure 2 OV7640/OV7141 Functional Block Diagram

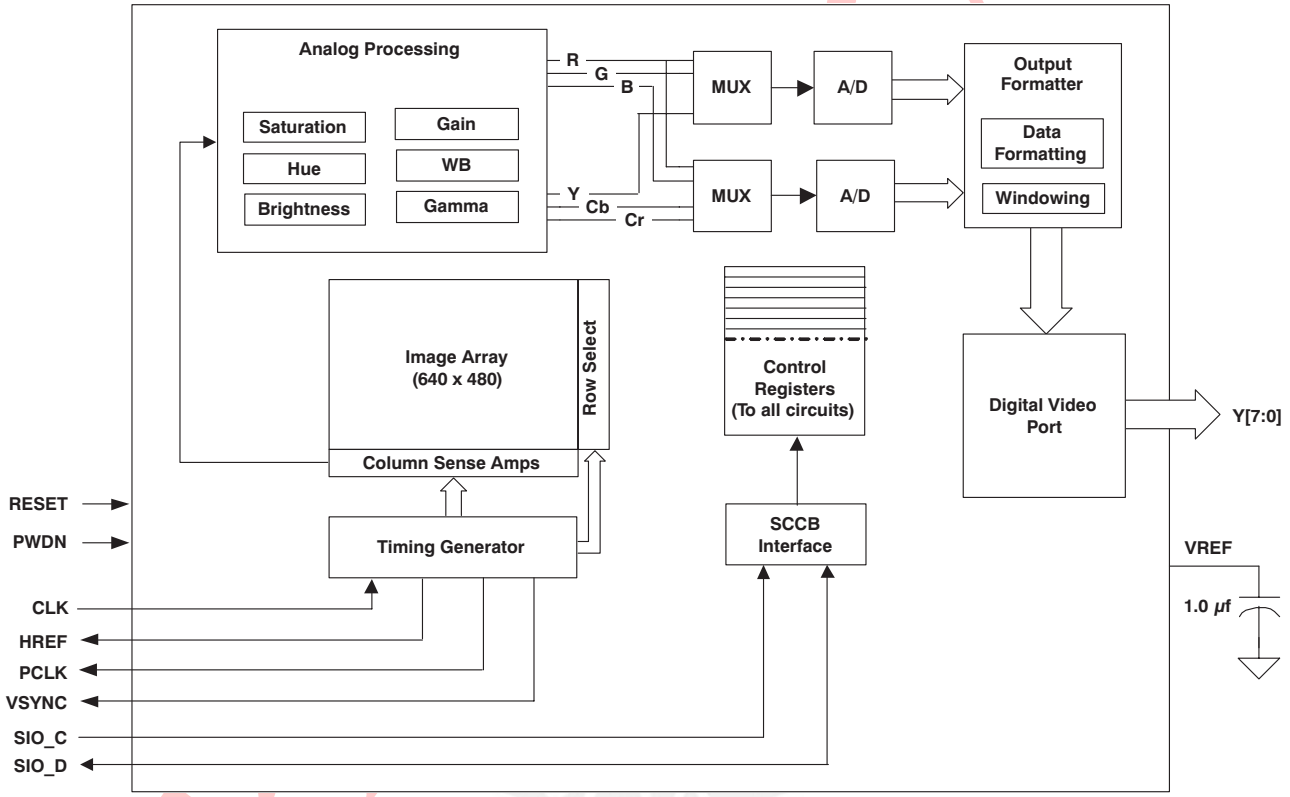
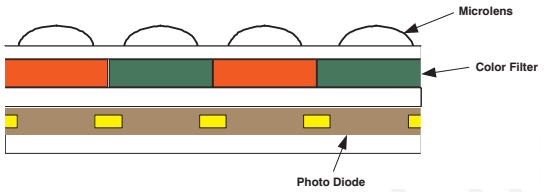


Image Sensor Array

The OV7640/OV7141 CAMERACHIPS has an active image array size of 640 columns x 480 rows (307,200 pixels). However, the full array contains 652 columns and 486 rows, with the extra 6 rows used for black-level calibration ("Optical Black") and color interpolation information. Figure 3 shows a cross-section of the image sensor array.

Figure 3 Image Sensor Array



Timing Generator

In general, the timing generator controls these functions:

- Array control and frame generation (VGA and QVGA outputs)
- Internal timing signal generation and distribution
- Frame rate timing
- Automatic Exposure Control (AEC)
- External timing outputs (VSYNC, HREF and PCLK)

Analog Processing Block

This block performs all analog image functions including:

- Automatic Gain Control (AGC)
- Automatic White Balance (AWB)
- Image quality controls including:
  - Color saturation
  - Hue
  - Gamma
  - Sharpness (edge enhancement)
  - Anti-blooming
  - Zero smearing

A/D Converters

After the Analog Processing Block, the color channel data signal is fed to two 8-bit Analog-to-Digital (A/D) converters via the multiplexers, one for the Y/G channel and one shared by the CrCb/BR channels. These A/D converters operate at speeds up to 12MHz, and are fully synchronous to the pixel rate (actual conversion rate is related to the frame rate).

In addition to the A/D conversion, this block also has the following functions:

- Digital Black-Level Calibration (BLC)
- Optional U/V channel delay
- Additional A/D range controls

In general, the combination of the A/D Range Multiplier and A/D Range Control sets the A/D range and maximum value to allow the user to adjust the final image brightness as a function of the individual application.

Output Formatter

This block controls all output and data formatting required prior to sending the image out.

Digital Video Port

These two bits increase I_{OL} / I_{OH} drive current and can be adjusted as a function of the customer's loading:

SCCB Interface

The Serial Camera Control Bus (SCCB) interface controls the CAMERACHIP operation. Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

Pin Description

Table 1 Pin Description

Pin Number	Name	Pin Type	Function/Description
01	VSS_A	Ground	Analog ground
02	VDD_A	V_{DD}	Analog VDD
03	NC	—	No connection
04	NC	—	No connection
05	PWDN	Input	Sets device to power down standby mode
06	NC	—	No connection
07	VREF	V_{REF}	Internal voltage reference (2.3V). Connect to ground through 1µF capacitor
08	VDD_C	V_{DD}	Core VDD
09	VSYNC	Output	Vertical sync output
10	HREF	Output	HREF output
11	PCLK	Output	Pixel clock output
12	VDD_IO	V_{DD}	I/O VDD
13	CLK	Input	External clock
14	NC	—	No connection
15	RESET	Input	Clears all registers and resets them to their default values.
16	NC	—	No connection
17	VSS_D	Ground	Digital ground
18	Y7	Output	Digital video output bit[7]
19	Y6	Output	Digital video output bit[6]
20	Y5	Output	Digital video output bit[5]
21	Y4	Output	Digital video output bit[4]
22	Y3	Output	Digital video output bit[3]
23	Y2	Output	Digital video output bit[2]
24	Y1	Output	Digital video output bit[1]
25	Y0	Output	Digital video output bit[0]
26	SIO_C	Input	SCCB serial interface clock
27	SIO_D	I/O	SCCB serial interface data I/O
28	NC	—	No connection

Electrical Characteristics

Table 2 Absolute Maximum Ratings

Ambient Storage Temperature		-40ºC to +125ºC
Supply Voltages (with respect to Ground)	**V_{DD-A}**	3V
	V_{DD-C}	3V
	V_{DD-IO}	4V
All Input/Output Voltages (with respect to Ground)		-0.3V to VDD_IO+1V
Lead Temperature, Surface-mount process		+230ºC
ESD Rating, Human Body model		2000V

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 3 DC Characteristics (0°C < T_A < 70°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD-A}	DC supply voltage – Analog	—	2.40	2.5	2.60	V
V_{DD-C}	DC supply voltage – Core	—	2.25	2.5	2.75	V
V_{DD-IO}	DC supply voltage – I/O	—	2.25	—	3.3	V
I_{DDA}	Active (Operating) Current	See Note [a]		15		mA
$I_{DDS-SCCB}$	Standby Current	See Note [b]		1		mA
$I_{DDS-PWDN}$	Standby Current			10		µA
V_{IH}	Input voltage HIGH	CMOS	0.7 x V_{DD-IO}			V
V_{IL}	Input voltage LOW				0.3 x V_{DD-IO}	V
V_{OH}	Output voltage HIGH	CMOS (I_{OH} / I_{OL})	0.9 x V_{DD-IO}			V
V_{OL}	Output voltage LOW				0.1 x V_{DD-IO}	V
I_{OH}	Output current HIGH	See Note [c]	8			mA
I_{OL}	Output current LOW		15			mA
I_L	Input/Output Leakage	GND to V_{DD-IO}			± 1	µA

a. V_{DD-A} = V_{DD-C} = 2.5V, V_{DD-IO} = 3.0V
$I_{DDA} = \Sigma\{I_{DD-IO} + I_{DD-C} + I_{DD-A}\}$, f_{CLK} = 24MHz at 30 fps, no I/O loading

b. V_{DD-A} = V_{DD-C} = 2.5V, V_{DD-IO} = 3.0V
$I_{DDS:SCCB}$ refers to a SCCB-initiated Standby, while $I_{DDS:PWDN}$ refers to a PWDN pin-initiated Standby

c. Standard Output Loading = 25pF, 1.2KΩ to 3V

Table 4 Functional and AC Characteristics (0°C < T_A < 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
Functional Characteristics					
	A/D Differential Non-Linearity		± 1/2		LSB
	A/D Integral Non-Linearity		± 1		LSB
	AGC Range			21	dB
	Red/Blue Adjustment Range			12	dB
Inputs (PWDN, CLK, RESET)					
f_{CLK}	Input Clock Frequency	10	24	27	MHz
t_{CLK}	Input Clock Period	100	42	37	ns
$t_{CLK:DC}$	Clock Duty Cycle	45	50	55	%
$t_{S:RESET}$	Setting time after software/hardware reset			1	ms
$t_{S:REG}$	Settling time for register change (10 frames required)			300	ms
SCCB (SIO_C and SIO_D - see Figure 4)					
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIO_C low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_R, t_F	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns
Outputs (VSYNC, HREF, PCLK, and Y[7:0] - see Figure 5, Figure 6, and Figure 7)					
t_{PDV}	PCLK[↓] to Data-out Valid			5	ns
t_{SU}	Y[7:0] Setup time	15			ns
t_{HD}	Y[7:0] Hold time	8			ns
t_{PHH}	PCLK[↓] to HREF[↑]	0		5	ns
t_{PHL}	PCLK[↓] to HREF[↓]	0		5	ns
AC Conditions:	• V_{DD}: V_{DD-A} = V_{DD-C} = 2.5V, V_{DD-IO} = 3.3V • Rise/Fall Times: I/O: 5ns, Maximum SCCB: 300ns, Maximum • Input Capacitance: 10pf • Output Loading: 25pF, 1.2KΩ to 3V • f_{CLK}: 24MHz				

Timing Specifications

Figure 4 SCCB Timing Diagram

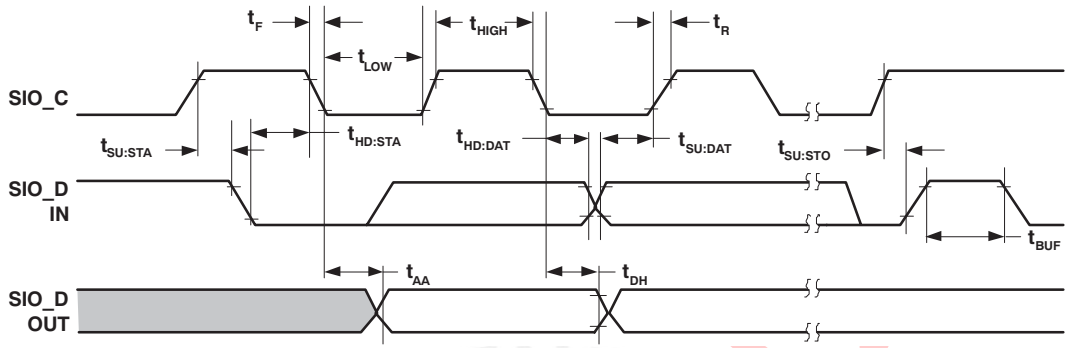


Figure 5 Row Output Timing Diagram

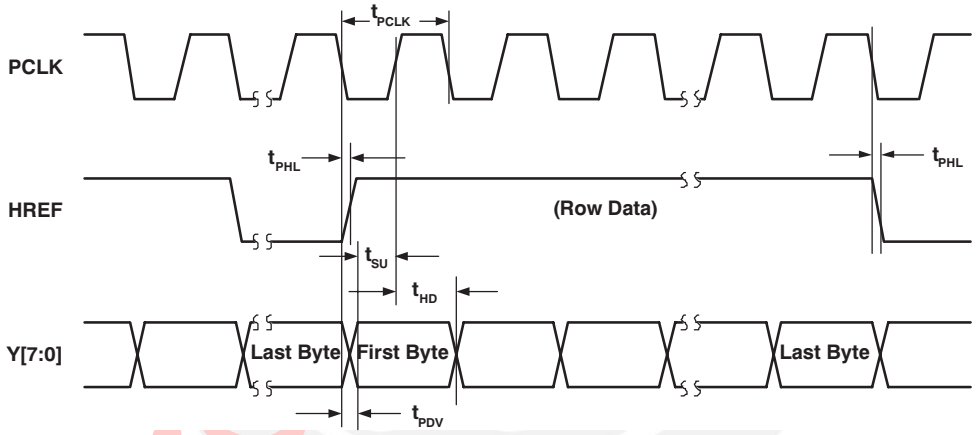


Figure 6 VGA Frame Timing Diagram

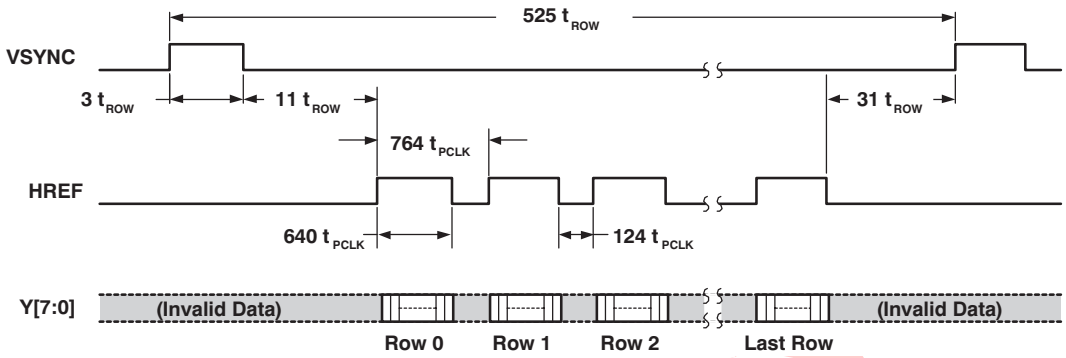
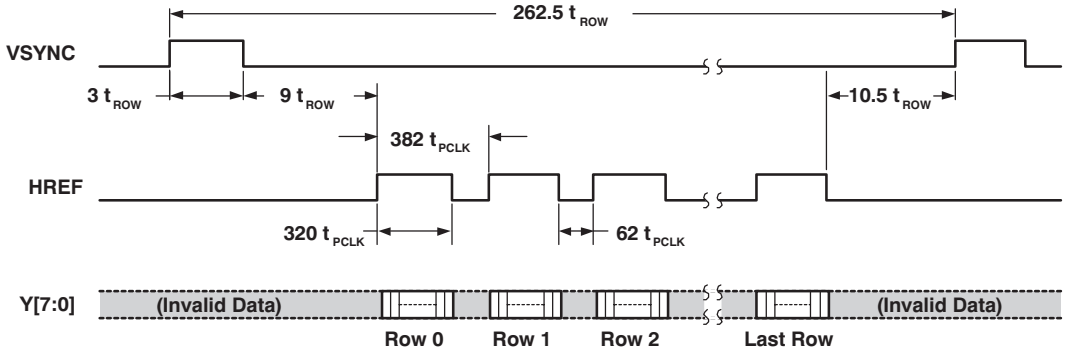


Figure 7 QVGA Frame Timing Diagram



Note: As the RGB, YUV and YCbCr formats use the Bayer pattern for interpolation, the first row transferred out on the Y[7:0] bus will be invalid, as there is no row above Row #1 to provide the 'pair data' required. Because of this, the OV7640 does not enable the HREF signal during the first row read (shown above in the 'invalid data' zone).

Figure 8 RGB 565 Output Timing Diagram

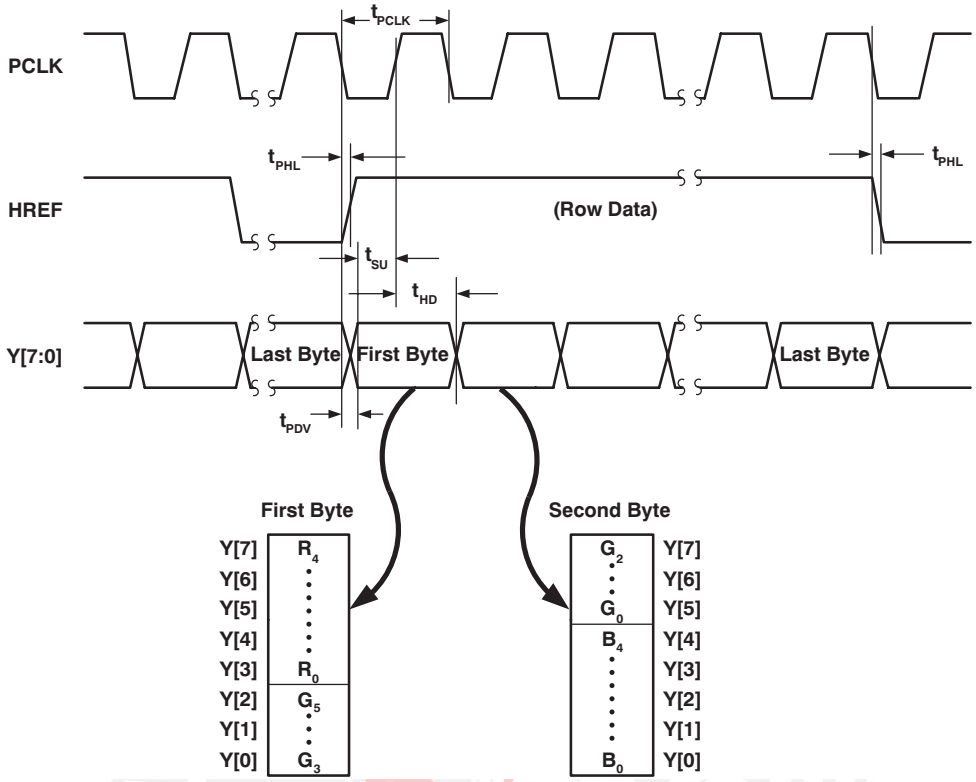
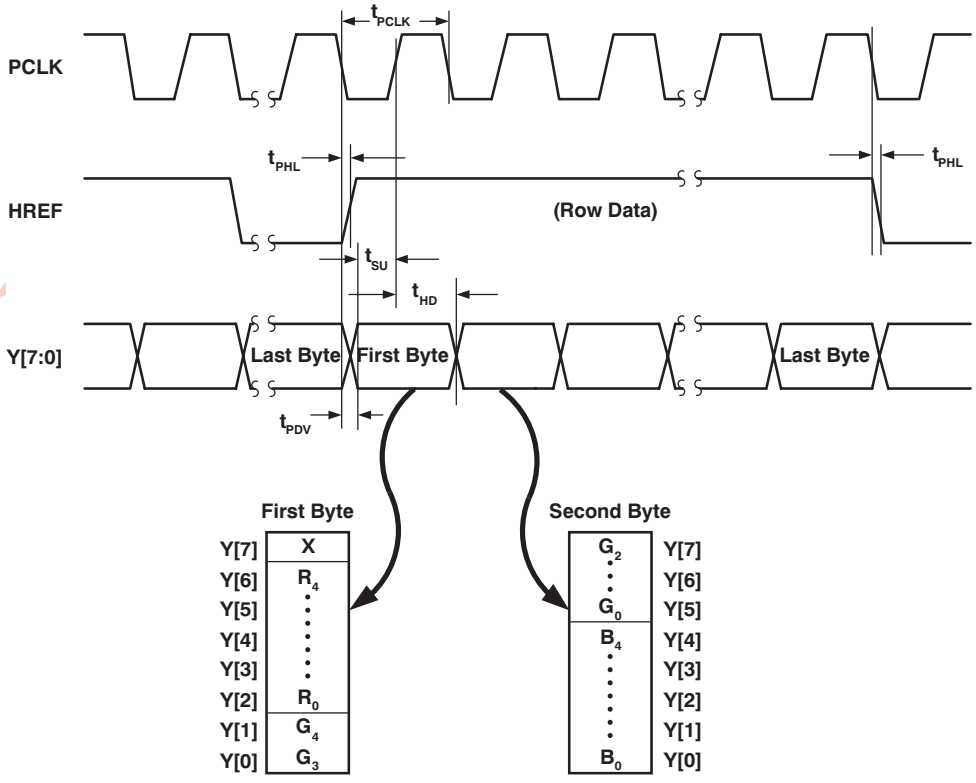


Figure 9 RGB 555 Output Timing Diagram



Register Set

Table 5 provides a list and description of the Device Control registers contained in the OV7640/OV7141. For all register Enable/Disable bits, ENABLE=1 and DISABLE=0. The device slave addresses for the OV7640/OV7141 are 42 for write and 43 for read.

Table 5 SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC – Gain control gain setting • Range: [00] to [FF]
01	BLUE	80	RW	AWB – Blue channel gain setting • Range: [00] to [FF] ***Note:*** *This function is not available on the B&W OV7141.*
02	RED	80	RW	AWB – Red channel gain setting • Range: [00] to [FF] ***Note:*** *This function is not available on the B&W OV7141.*
03	SAT	84	RW	Image Format – Color saturation value Bit[7:4]: Saturation value • Range: [0] to [F] Bit[3:0]: Reserved ***Note:*** *This function is not available on the B&W OV7141.*
04	HUE	34	RW	Image Format – Color hue control Bit[7:6]: Reserved Bit[5]: Hue Enable Bit[4:0]: Hue setting ***Note:*** *This function is not available on the B&W OV7141.*
05	CWF	3E	RW	AWB – Red/Blue Pre-Amplifier gain setting Bit[7:4]: Red channel pre-amplifier gain setting • Range: [0] to [F] Bit[3:0]: Blue channel pre-amplifier gain setting • Range: [0] to [F] ***Note:*** *This function is not available on the B&W OV7141.*
06	BRT	80	RW	ABC – Brightness setting • Range: [00] to [FF]
07-09	RSVD	XX	–	Reserved
0A	PID	76	R	Product ID number (Read only)
0B	VER	48	R	Product version number (Read only)
0C-0F	RSVD	XX	–	Reserved
10	AECH	41	RW	Exposure Value

Table 5 SCCB Register List

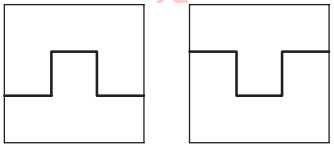
Address (Hex)	Register Name	Default (Hex)	R/W	Description
11	CLKRC	00	RW	Data Format and Internal Clock Bit[7:6]: Data Format – HSYNC/VSYNC Polarity_ 00: HSYNC = NEG VSYNC = POS 01: HSYNC = NEG VSYNC = NEG 10: HSYNC = POS VSYNC = POS 11: HSYNC = POS VSYNC = POS  POS NEG Bit[5:0]: Internal Clock Pre-Scalar • Range: [0 0000] to [F FFFF]
12	COMA	14	RW	Common Control A Bit[7]: SCCB – Register Reset 0: No change 1: Reset all registers to default values Bit[6]: Output Format – Mirror Image Enable Bit[5]: Reserved Bit[4]: Data Format – YUV formatting 0: Y U Y V Y U Y V 1: U Y V Y U Y V Y (default) Bit[3]: Output Format – Output Channel Select A 0: YUV/YCbCr 1: RGB/Raw RGB Bit[2]: AWB – Enable Bit[1:0]: Reserved ***Note:*** *This function is not available on the B&W OV7141.*
13	COMB	A3	RW	Common Control B Bit[7:5]: Reserved Bit[4]: Data Format – ITU-656 Format Enable Bit[3]: Reserved Bit[2]: SCCB – Tri-State Enable – Y[7:0] Bit[1]: AGC – Enable Bit[0]: AEC – Enable

Table 5 SCCB Register List

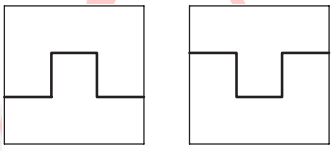
Address (Hex)	Register Name	Default (Hex)	R/W	Description
14	COMC	04	RW	Common Control C Bit[7:6]: Reserved Bit[5]: Output Format – Resolution 0: VGA (640x480) 1: QVGA (320x240) Bit[4]: Reserved Bit[3]: Data Format – HREF Polarity 0: HREF Positive 1: HREF Negative  POS NEG Bit[2:0]: Reserved
15	COMD	00	RW	Common Control D Bit[7]: Data Format – Output Flag Bit Disable 0: Frame = 254 data bits (00/FF = Reserved flag bits) 1: Frame = 256 data bits Bit[6]: Data Format – Y[7:0]-PCLK Reference Edge 0: Y[7:0] data out on PCLK falling edge 1: Y[7:0] data out on PCLK rising edge Bit[5:1]: Reserved Bit[0]: Data Format – UV Sequence Exchange 0: V Y U Y V Y U Y 1: U Y V Y U Y V Y ***Note:*** *Bit[0] is not programmable on the B&W OV7141.*
16	RSVD	XX	–	Reserved
17	HSTART	1A	RW	Output Format – Horizontal Frame (HREF Column) Start
18	HSTOP	BA	RW	Output Format – Horizontal Frame (HREF Column) Stop
19	VSTRT	03	RW	Output Format – Vertical Frame (Row) Start
1A	VSTOP	F3	RW	Output Format – Vertical Frame (Row) Stop
1B	PSHFT	00	RW	Data Format – Pixel Delay Select (Delays timing of the Y[7:0] data relative to HREF in pixel units) • Range: [00] (No delay) to [FF] (256 pixel delay)
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E	RSVD	XX	–	Reserved

Table 5 SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
1F	FACT	01	RW	Output Format – Format Control Bit[7:5]: Reserved Bit[4]: Output Format – RGB:565 Enable ***Note:*** *Bit[4] is not programmable on the B&W OV7141.* Bit[3]: Reserved Bit[2]: Output Format – RGB:555 Enable ***Note:*** *Bit[2] is not programmable on the B&W OV7141.* Bit[1:0]: Reserved
20	COME	C0	RW	Common Control E Bit[7]: Reserved Bit[6]: AEC – Digital Averaging Enable Bit[5]: Reserved Bit[4]: Image Quality – Edge Enhancement Enable Bit[3:1]: Reserved Bit[0]: Y[7:0] 2X I_{OL} / I_{OH} Enable
21-23	RSVD	XX	–	Reserved
24	AEW	10	RW	AGC/AEC – Stable Operating Region – Upper Limit
25	AEB	8A	RW	AGC/AEC – Stable Operating Region – Lower Limit
26	COMF	A2	RW	Common Control F Bit[7:3]: Reserved Bit[2]: Data Format – Output Data MSB/LSB Swap Enable (LSB → MSB (Y[7]) and MSB → LSB (Y[0])) Bit[1:0]: Reserved
27	COMG	E2	RW	Common Control G Bit[7:5]: Reserved Bit[4]: Color Matrix – RGB Crosstalk Compensation Enable (Used to increase each color filter's efficiency) ***Note:*** *Bit[4] is not programmable on the B&W OV7141.* Bit[3:2]: Reserved Bit[1]: Data Format – Output Full Range Enable 0: Output Range = [10] to [F0] (224 bits) 1: Output Range = [01] to [FE] (254/256 bits) Bit[0]: Reserved
28	COMH	20	RW	Common Control H Bit[7]: Output Format – RGB Output Select 0: RGB 1: Raw RGB Bit[6]: Device Select 0: OV7640 1: OV7141 Bit[5]: Output Format – Scan Select 0: Interlaced 1: Progressive Bit[4:0]: Reserved

Table 5 SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
29	COMI	00	R	Common Control I Bit[7:2]: Reserved Bit[1:0]: Device Version (Read-only)
2A	FRARH	00	RW	Output Format – Frame Rate Adjust High Bit[7]: Data Format – Frame Rate Adjust Enable Bit[6:5]: Data Format – Frame Rate Adjust Setting MSB FRA[9:0] = MSB + LSB = FRARH[6:5] + FRARL[7:0] Bit[4]: A/D – UV Channel '2 Pixel Delay' Enable ***Note:*** *Bit[4] is not programmable on the B&W OV7141.* Bit[3:0]: Reserved
2B	FRARL	00	RW	Data Format – Frame Rate Adjust Setting LSB FRA[9:0] = MSB + LSB = FRARH[6:5] + FRARL[7:0]
2C	RSVD	XX	–	Reserved
2D	COMJ	81	RW	Common Control J Bit[7:3]: Reserved Bit[2]: AEC – Band Filter Enable Bit[1:0]: Reserved
2E-5F	RSVD	XX	–	Reserved
60	SPCB	06	RW	Signal Process Control B Bit[7]: AGC – 1.5x Multiplier (Pre-amplifier) Enable Bit[6:0]: Reserved
61-6B	RSVD	XX	–	Reserved
6C	RMCO	11	RW	Color Matrix – RGB Crosstalk Compensation – R Channel ***Note:*** *This function is not available on the B&W OV7141.*
6D	GMCO	01	RW	Color Matrix – RGB Crosstalk Compensation – G Channel ***Note:*** *This function is not available on the B&W OV7141.*
6E	BMCO	06	RW	Color Matrix – RGB Crosstalk Compensation– B Channel ***Note:*** *This function is not available on the B&W OV7141.*
6F-70	RSVD	XX	–	Reserved
71	COML	00	RW	Common Mode Control L Bit[7]: Reserved Bit[6]: Data Format – PCLK output gated by HREF Enable Bit[5]: Data Format – Output HSYNC on HREF Pin Enable Bit[4]: Reserved Bit[3:2]: Data Format – HSYNC Rising Edge Delay MSB Bit[1:0]: Data Format – HSYNC Falling Edge Delay MSB
72	HSDYR	10	RW	Data Format – HSYNC Rising Edge Delay LSB HSYNCR[9:0] = MSB + LSB = COML[3:2] + HSDYR[7:0] • Range 000 to 762 pixel delays

Table 5 SCCB Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
73	HSDYF	50	RW	Data Format – HSYNC Falling Edge Delay LSB HSYNCF[9:0] = MSB + LSB = COML[1:0] + HSDYF[7:0] • Range 000 to 762 pixel delays
74	COMM	20	RW	Common Mode Control M Bit[7]: Reserved Bit[6:5]: AGC – Maximum Gain Select 00: +6 dB 01: +12 dB 10: +6 dB 11: +18 dB Bit[4:0]: Reserved
75	COMN	02	RW	Common Mode Control N Bit[7]: Output Format – Vertical Flip Enable Bit[6:0]: Reserved
76	COMO	00	RW	Common Mode Control O Bit[7:6]: Reserved Bit[5]: Standby Mode Enable Bit[4:3]: Reserved Bit[2]: SCCB – Tri-State Enable – VSYNC, HREF and PCLK Bit[1:0]: Reserved
77-7D	RSVD	XX	–	Reserved
7E	AVGY	00	RW	AEC – Digital Y/G Channel Average (Automatically updated by AGC/AEC, user can only read the values)
7F	AVGR	00	RW	AEC – Digital R/V Channel Average (Automatically updated by AGC/AEC, user can only read the values) ***Note:*** *This function is not available on the B&W OV7141.*
80	AVGB	00	RW	AEC – Digital B/U Channel Average (Automatically updated by AGC/AEC, user can only read the values) ***Note:*** *This function is not available on the B&W OV7141.*
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV7640/OV7141 uses a 28-pin plastic package. Refer to Figure 10 for package information, Table 6 for package dimensions, and Figure 11 for the array center on the chip.

Figure 10 OV7640OV7141 Plastic Package Specifications

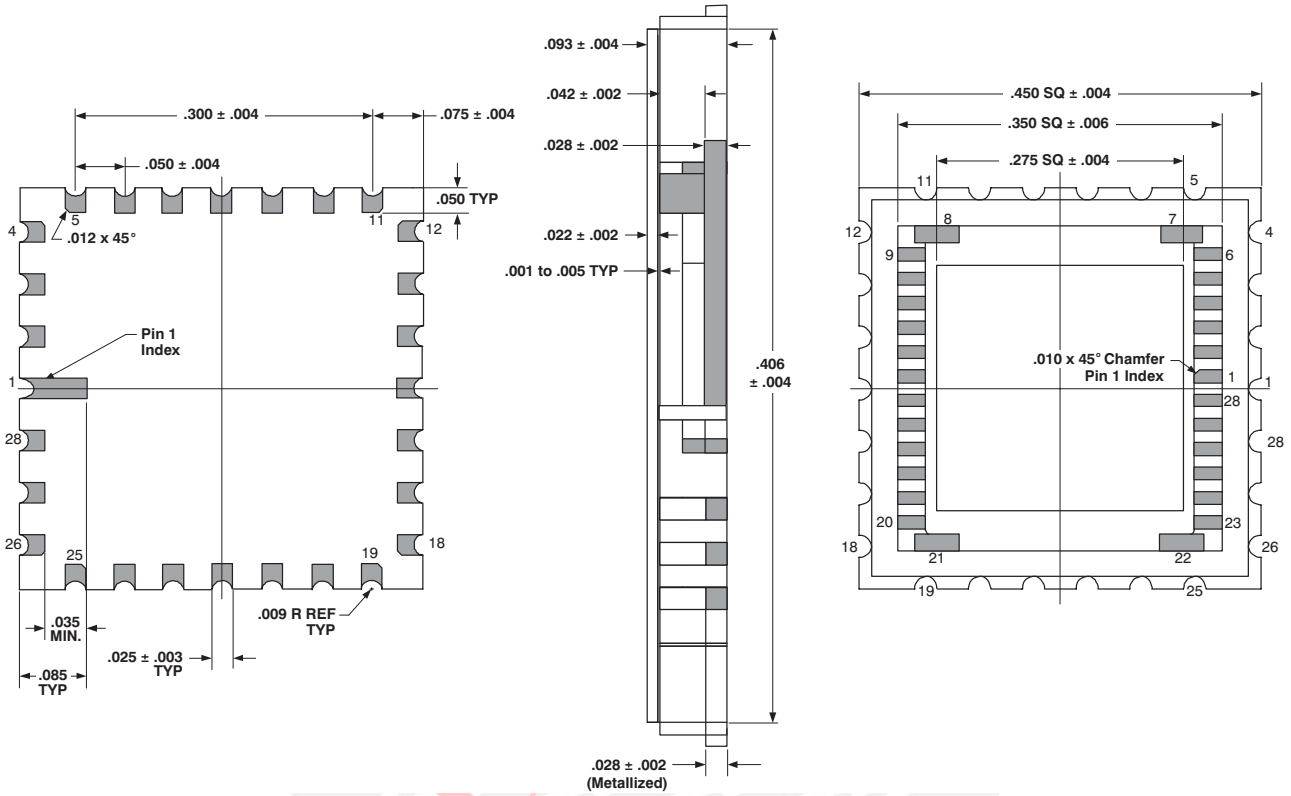
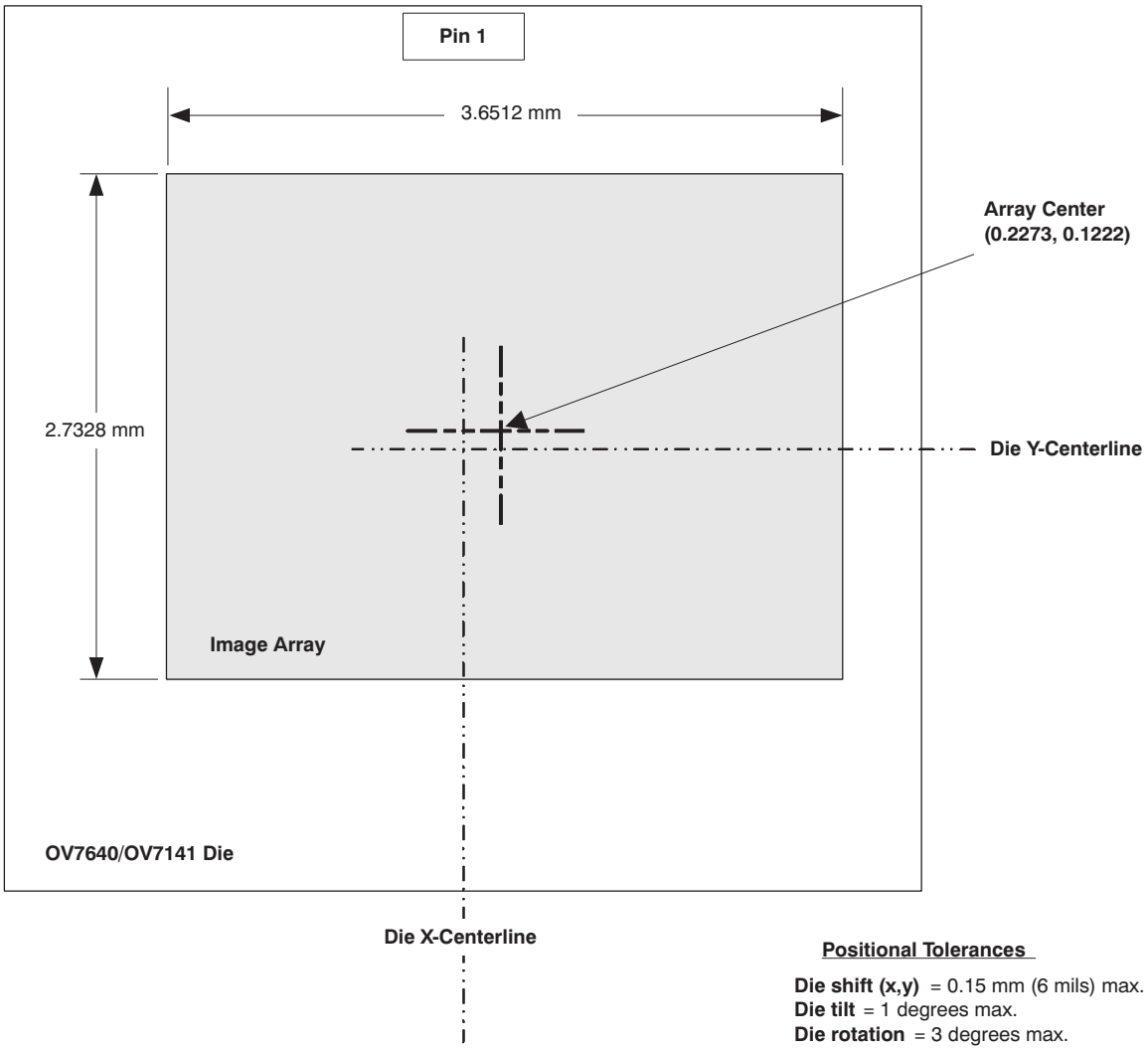


Table 6 OV7640/OV7141 Plastic Package Dimensions

Dimensions	Millimeters (mm)	Inches (in.)
Package Size	11.43 ± 0.10 SQ	.450 ± .004 SQ
Package Height	2.35 ± 0.1	.093 ± .004
Substrate Height	0.70 ± 0.05	.028 ± .002
Cavity Size	7.00 ± 0.10 SQ	.275 ± .004 SQ
Castellation Height	1.07 ± 0.05	.042 ± .002
Pin #1 Pad Size	0.64 x 2.16	.025 x .085
Pad Size	0.64 x 1.27	.025 x .050
Pad Pitch	1.27 ± 0.10	.050 ± .004
Package Edge to First Lead Center	1.90 ± 0.10	.075 ± .004
End-to-End Pad Center-Center	7.62 ± 0.10	.300 ± .004
Glass Size	10.30 ± 0.10 SQ	.406 ± .004 SQ
Glass Height	0.55 ± 0.05	.022 ± .002

Sensor Array Center

Figure 11 OV7640/OV7141 Sensor Array Center

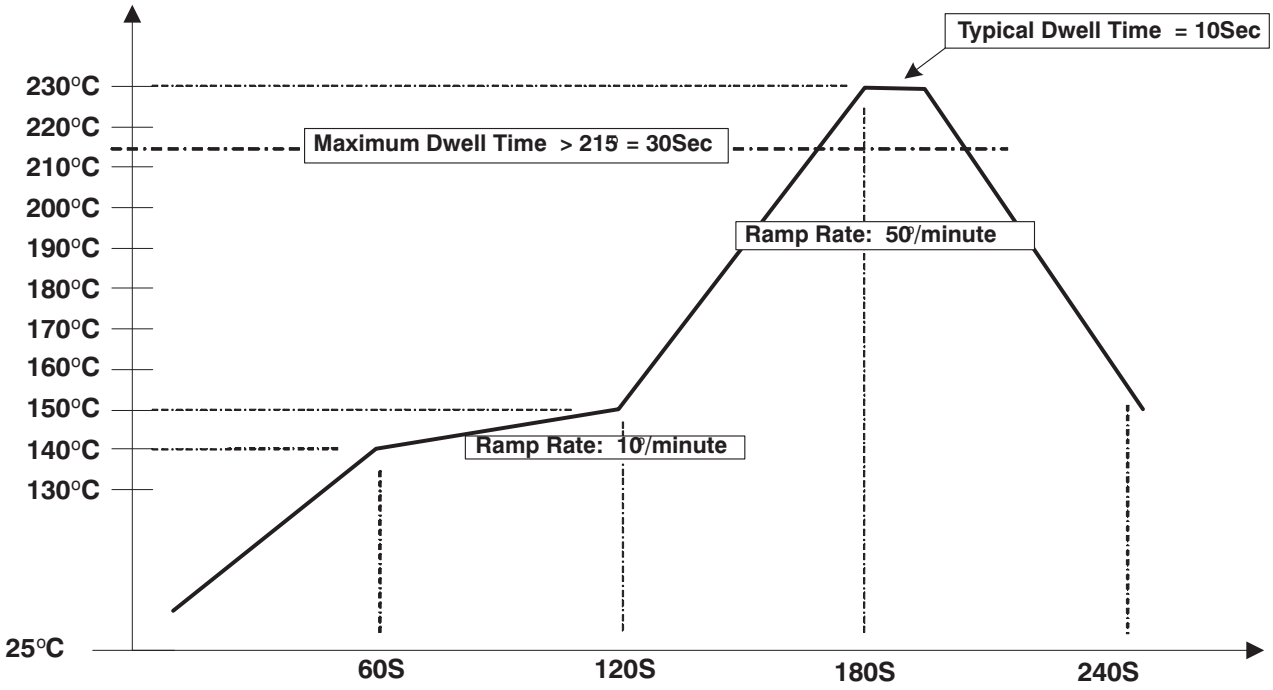


NOTES: Due to the lens inversion, in order for the image to be right-side up, the OV7640/OV7140 must be mounted Pin 1 down.

Picture is for reference only, not to scale.

IR Reflow Ramp Rate Requirements

Figure 12 IR Reflow Ramp Rate Requirements



Note:

All temperatures = ± 10°C
All times show the fastest allowable ramp rate

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

- *OmniVision Technologies, Inc. reserves the right to make changes to their products or to discontinue any product or service without further notice (It is advisable to obtain current product documentation prior to placing orders).*

- *Reproduction of information in OmniVision product documentation and specifications is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. In such cases, OmniVision is not responsible or liable for any information reproduced.*

- *This document is provided with no warranties whatsoever, including any warranty of merchantability, non-infringement, fitness for any particular purpose, or any warranty otherwise arising out of any proposal, specification or sample. Furthermore, OmniVision Technologies Inc. disclaims all liability, including liability for infringement of any proprietary rights, relating to use of information in this document. No license, expressed or implied, by estoppels or otherwise, to any intellectual property rights is granted herein.*

- *'OmniVision', 'CameraChip' are trademarks of OmniVision Technologies, Inc. All other trade, product or service names referenced in this release may be trademarks or registered trademarks of their respective holders. Third-party brands, names, and trademarks are the property of their respective owners.*

For further information, please feel free to contact OmniVision at info@ovt.com.

OmniVision Technologies, Inc.
Sunnyvale, CA USA
(408) 733-3030

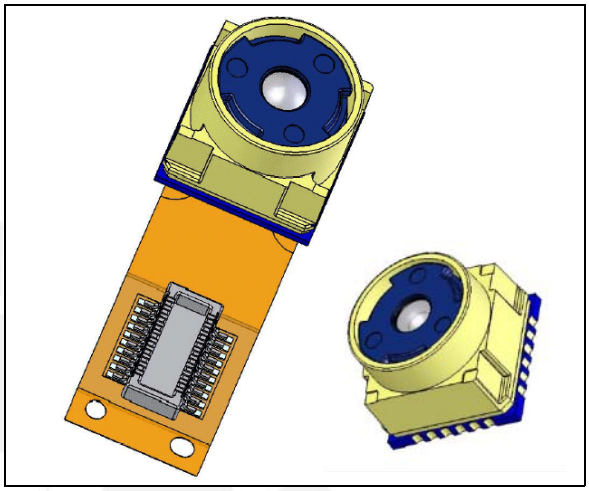
VS6624

1.3 Megapixel Mobile Camera Module

PRELIMINARY DATA

Features

- 1280H x 1024V active pixels
- 3.0 µm pixel size, 1/3 inch optical format
- RGB Bayer color filter array
- Integrated 10-bit ADC
- Integrated digital image processing functions, including defect correction, lens shading correction, image scaling, demosaicing, sharpening, gamma correction and color space conversion
- Embedded camera controller for automatic exposure control, automatic white balance control, black level compensation, 50/60 Hz flicker cancelling and flashgun support
- Fully programmable frame rate and output derating functions
- Up to 15 fps SXGA progressive scan
- Low power 30fps VGA progressive scan
- ITU-R BT.656-4 YUV (YCbCr) 4:2:2 with embedded syncs, YUV (YCbCr) 4:0:0, RGB 565, RGB 444, Bayer 10-bit or Bayer 8-bit output formats
- 8-bit parallel video interface, horizontal and vertical syncs, 54MHz (max) clock
- Two-wire serial control interface
- On-chip PLL, 6.5 to 54 MHz clock input
- Analog power supply, from 2.4 to 3.0 V
- Separate I/O power supply, 1.8 or 2.8 V levels
- Integrated power management with power switch, automatic power-on reset and power-safe pins
- Low power consumption, ultra low standby current
- Triple-element plastic lens, F# 3.2, 52° Horizontal field of view
- 8.0 x 8.0 x 6.1mm fixed focus camera module with embedded passives



- 20-wire FPC attachment with board-to-board connector, 22 mm total length
- 24-pin (ITU) shielded socket options

Description

The VS6624 is an SXGA CMOS color digital camera featuring low size and low power consumption targeting mobile applications. This complete camera module is ready to connect to camera enabled baseband processors, back-end IC devices or PDA engines.

Applications

- Mobile phone
- PDA

Ordering codes

Part number	Description
VS6624P0LP	SMOP2 VGA 8x8, flex
VS6624Q0KP	SMOP2 VGA 8x8, socket

Contents

List of tables

List of figures

1 Overview

1.1 Description

The VS6624 is a SXGA resolution CMOS imaging device designed for low power systems, particularly mobile phone applications.

Manufactured using ST 0.18 µm CMOS Imaging process, it integrates a high-sensitivity pixel array, a digital image processor and camera control functions.

The VS6624 is capable of streaming SXGA video up to 15 fps, with ITU-R BT.656-4 YUV 4:2:2 frame format. It supports both 1.8 V and 2.8 V interface and requires a 2.4 to 3.0 V analog power supply. Typically, the VS6624 can operate as a 2.8 V single supply camera or as a 1.8 V interface / 2.8 V supply camera. The integrated PLL allows for low frequency system clock, and flexibility for successful EMC integration.

The VS6624 camera module uses ST's 2nd generation "SmOP2" packaging technology: the sensor, lens and passives are assembled, tested and focused in a fully automated process, allowing high volume and low cost production.

The device contains an embedded video processor and delivers fully color processed images at up to 15 frames per second SXGA and up to 30 fps VGA.

The video data is output over an 8-bit parallel bus in RGB, YCbCr or bayer formats.

The VS6624 requires an analogue power supply of between 2.4 V to 3.0 V and a digital supply of either 1.8 V or 2.8 V (dependant on interface levels required). An input clock is required in the range 6.5 MHz to 54 MHz.

The VS6624 is controlled via an I²C interface.

It also includes a wide range of image enhancement functions, designed to ensure high image quality, these include:

- Automatic exposure control
- Automatic white balance
- Lens shading compensation
- Defect correction algorithms
- Demosaic (Bayer to RGB conversion)
- Colour space conversion
- Sharpening
- Gamma correction
- Flicker cancellation
- NoRA Noise Reduction Algorithm
- Intelligent image scaling

2 Electrical interface

The VS6624 FPC board to board connector has 20 electrical connections which are listed in *Table 1*. the package details of the flex connector are shown in *Figure 38* and*Figure 39*.

Table 1. VS6624 signal description of 20-pin flex connector
Table 2:

Pad	Pad name	I/O	Description
1	GND	PWR	Analogue ground
2	HSYNC	OUT	Horizontal synchronization output
3	VSYNC	OUT	Vertical synchronization output
4	SCL	IN	I²C clock input
5	CLK	IN	Clock input - 6.5MHz to 54MHz
6	SDA	I/O	I²C data line
7	VDD	PWR	Digital supply 1.8 V OR 2.8 V
8	AVDD	PWR	Analogue supply 2.4 V to 3.0 V
9	PCLK	OUT	Pixel qualification clock
10	CE	IN	Chip enable signal active HIGH
11	D5	OUT	Data output D5
12	D4	OUT	Data output D4
13	GND	PWR	Digital ground
14	D3	OUT	Data output D3
15	D2	OUT	Data output D2
16	D1	OUT	Data output D1
17	D0	OUT	Data output D0
18	D6	OUT	Data output D6
19	D7	OUT	Data output D7
20	FSO	OUT	Flash output

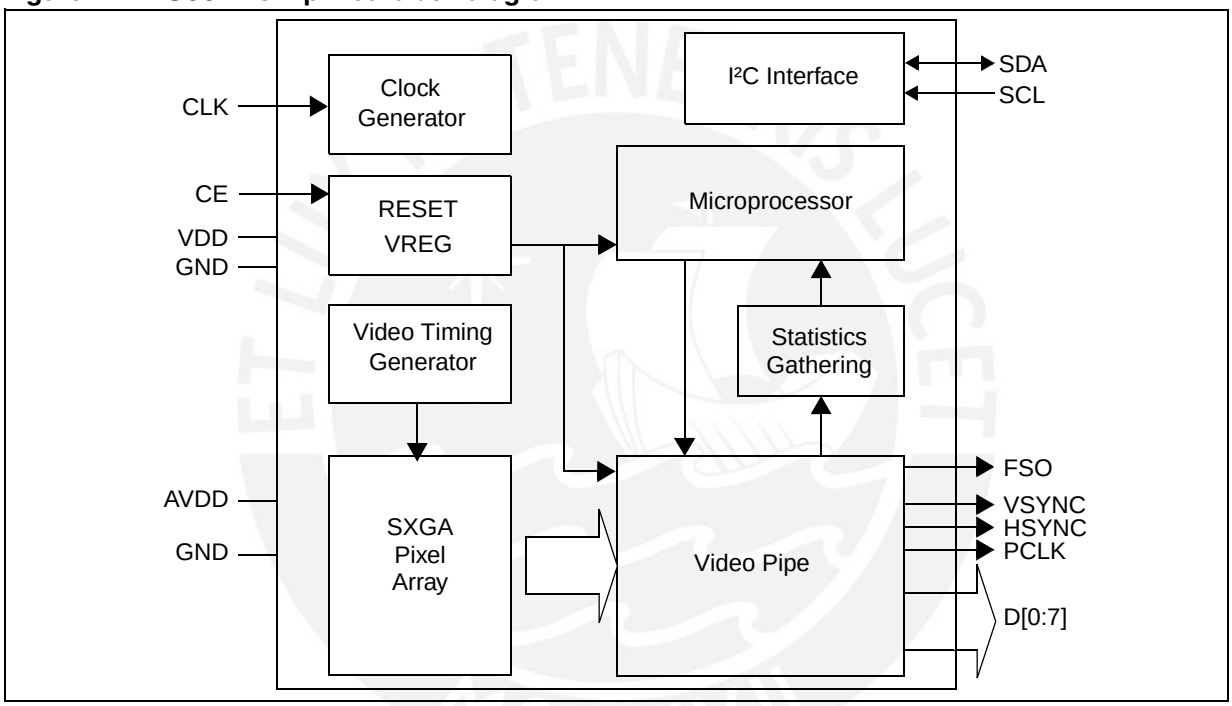
The package details and electrical connections of the 24pin socket device are shown in *Figure 36* and *Figure 37*.

3 System architecture

The simplified block diagram of VS6624 is shown in *Figure 1*. VS6624 includes the following main blocks:

- SXGA-sized pixel array
- Video timing generator
- Video pipe
- Statistics gathering unit
- Clock generator
- Microprocessor

Figure 1. VS6624 simplified block diagram



3.1 Operation

A video timing generator controls a SXGA-sized pixel array to produce raw bayer images. The analogue pixel information is digitized and passed into the video pipe. The video pipe contains a number of different functions (explained in detail later). At the end of the video pipe data is output to the host system over an 8-bit parallel interface along with qualification signals.

The whole system is controlled by an embedded microprocessor that is running firmware stored in an internal ROM. The external host communicates with this microprocessor over an I²C interface. The microprocessor does not handle the video data itself but is able to control all the functions within the video pipe. Real-time information about the video data is gathered by a statistics engine and is available to the microprocessor. The processor uses this information to perform real-time image control tasks such as automatic exposure control.

3.2 Video pipe

The main functions contained within the VS6624 video processing pipe are as follows.

Gain and offset This function is used to apply gain and offset to data coming from the sensor array. The microprocessor applies gain and offset values are controlled by the automatic exposure and white balance algorithms.

Anti-vignette This function is used to compensate for the radial roll-off in intensity caused by the lens. By default the anti-vignette setting matches the lens used in this module and does not need to be adjusted.

Crop This function allows the user to select an arbitrary Window Of Interest (WOI) from the SXGA-sized pixel array, note that the crop size should not be smaller that the output size. It is fully accessible to the user.

Scaler The scaler module performs real time downscaling, in both the horizontal and vertical domain, of the bayer image data this is achieved by sample-rate conversion. The scaler is capable of downscaling from 1.0x to 10x the input number of pixels and lines, in steps of 1/16.

Derating The VS6624 contains an internal derating module. This is designed to reduce the peak output data rate of the device by spreading the data over the whole frame period and allowing a subsequent reduction in output clock frequency.

The maximum achievable derating factor is x100 for an equivalent scale factor of x10 downscale. As a general rule the allowable derating factor is equal to the square of the scaling factor.

Note: The interline period is not guaranteed consistent for all derating ratios. This means the host capture system must be able to cope with use of the sync signals or embedded codes rather than relying on fixed line counts.

Defect correction This function runs a defect correction filter over the data in order to remove defects from the final output. This function has been optimized to attain the minimum level of defects from the system and does not need to be adjusted.

NoRA The noise reduction module implements an algorithm based on the human-visual system and adaptive pixel filtering that reduces perceived noise in an image whilst maintaining areas of high definition.

Demosaic This module performs an interpolation on the Bayer data from the sensor array to produce a sRGB data. At this point an anti-alias filter is applied.

Anti-Zipper The demosaic process produces an RGB frame with a noise signal at pixel frequency. To remove this artefact an anti-zipper filter is employed.

Sharpening This module increases the high frequency content of the image in order to compensate for the low-pass filtering effects of the previous modules.

Gamma This module applies a programmable gain curve to the output data. It is user adjustable.

YUV conversion This module performs color space conversion from RGB to YUV. It is used to control the contrast and color saturation of the output image as well as the fade to black feature.

Dither This module is used to reduce the contouring effect seen in RGB images with truncated data.

Output formatter This module controls the embedded codes which are inserted into the data stream to allow the host system to synchronize with the output data. It also controls the optional HSYNC and VSYNC output signals.

3.3 Microprocessor functions

The microprocessor inside the VS6624 performs the following tasks:

Host communication handles the I²C communication with the host processor.

Video pipe configuration configures the video pipe modules to produce the output required by the host.

Automatic exposure control In normal operation the VS6624 determines the appropriate exposure settings for a particular scene and outputs correctly exposed images.

Flicker cancellation The 50/60Hz flicker frequency present in the lighting (due to fluorescent lighting) can be cancelled by the system.

Automatic white balance The microprocessor adjusts the gains applied to the individual color channels in order to achieve a correctly color balanced image.

Frame rate control VS6624 contains a firmware based programmable timing generator. This automatically designs internal video timings, PLL multipliers, clock dividers etc. to achieve a target frame rate with a given input clock frequency.

Optionally an automatic frame rate controller can be enabled. This system examines the current exposure status, integration time and gain and adapts the frame rate based on that. This function is typically useful in low-light scenarios where reducing the frame rate extends the useful integration period. This reduces the need for the application of analog and digital gain and results in better quality images.

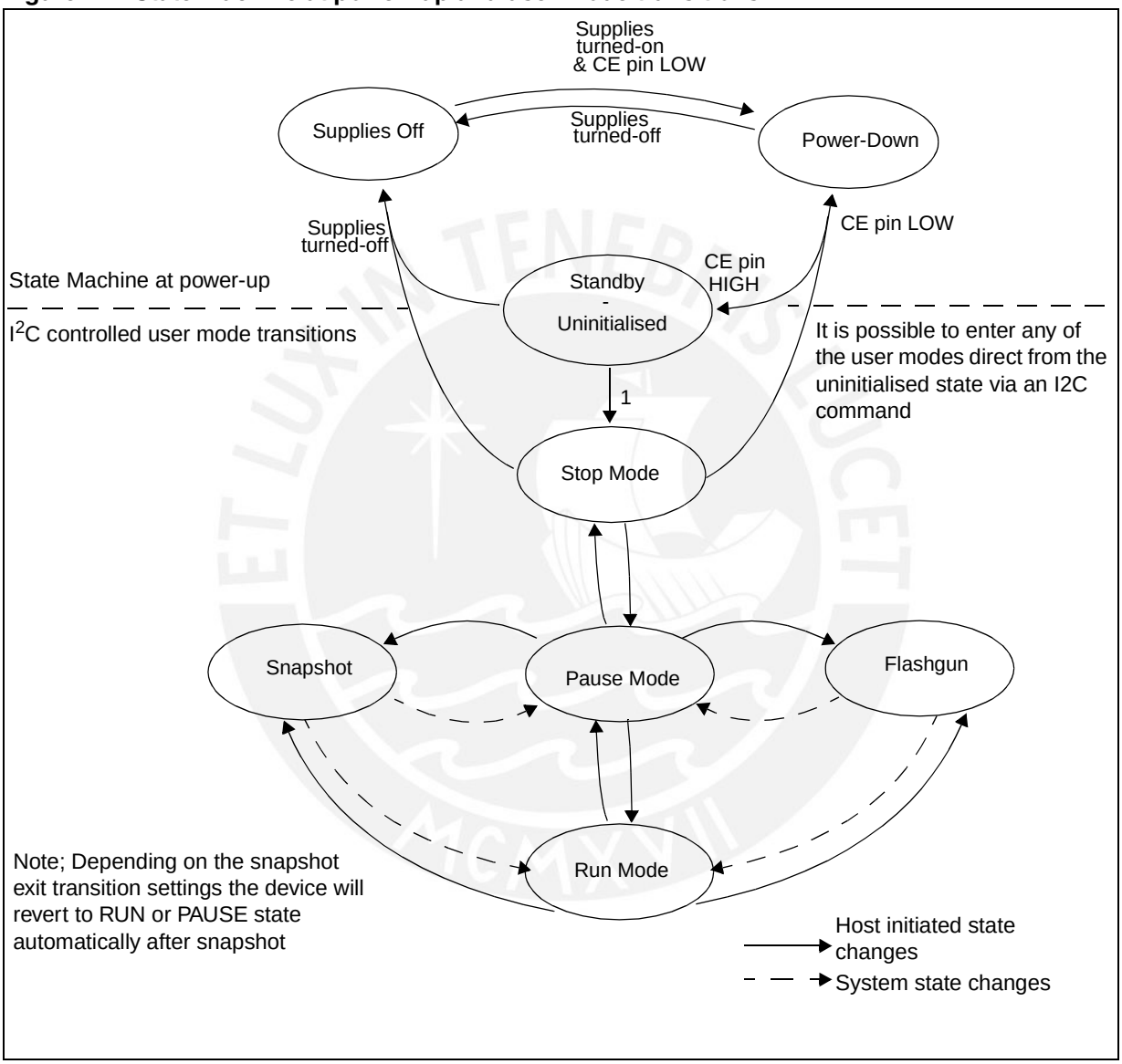
Dark calibration The microprocessor uses information from special dark lines within the pixel array to apply an offset to the video data and ensure a consistent ‘black’ level.

Active noise management The microprocessor is able to modify certain video pipe functions according to the current exposure settings determined by the automatic exposure controller. The main purpose of this is to improve the noise level in the system under low lighting conditions. Functions which ‘strength’ is reduced under low lighting conditions (e.g. sharpening) are controlled by ‘dampers’. Functions which ‘strength’ is increased under low lighting conditions are controlled by ‘promoters’. The fade to black operation is also controlled by the microprocessor

4 Operational modes

VS6624 has a number of operational modes. The power down mode is entered and exited by driving the hardware CE signal. Transitions between all other modes are initiated by I²C transactions from the host system or automatically after time-outs.

Figure 2. State machine at power -up and user mode transitions



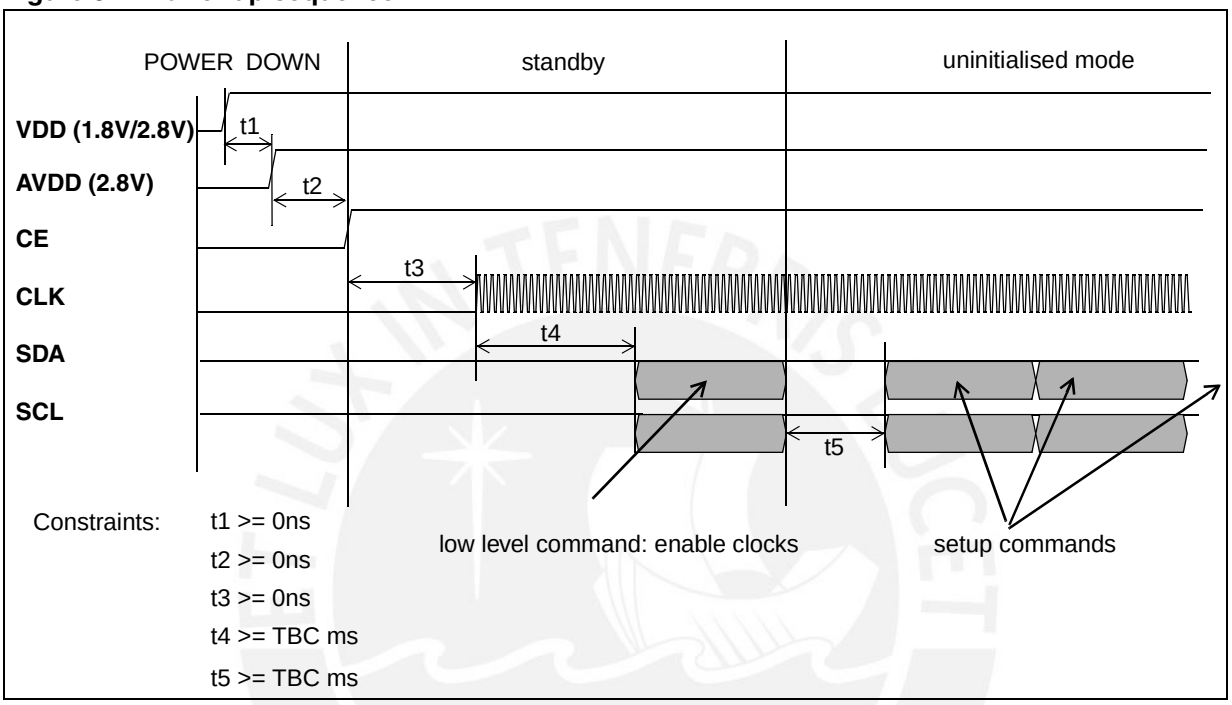
Power Down/Up The power down state is entered from all other modes when CE is pulled low or the supplies are removed.
During the power-down state (CE = logic 0)

- The internal digital supply of the VS6624 is shut down by an internal switch mechanism. This method allows a very low power-down current value.
- The device input / outputs are fail-safe, and consequently can be considered high impedance.

During the power-up sequence (CE = logic 1)

- The digital supplies must be on and stable.
- The internal digital supply of the VS6624 is enabled by an internal switch mechanism.
- All internal registers are reset to default values by an internal power on reset cell.

Figure 3. Power up sequence



STANDBY mode The VS6624 enters STANDBY mode when the CE pin on the device is pulled HIGH. Power consumption is very low, most clocks inside the device are switched off.
In this state I²C communication is possible when CLK is present and when the microprocessor is enabled.

All registers are reset to their default values. The device I/O pins have a very high-impedance.

Uninitialised = RAW The initialize mode is defined as supplies present, the CE signal is logic 1 and the microcontroller clock has been activated.

During initialize mode the device firmware may be patched. This state is provided as an intermediary configuration state and is not central to regular operation of the device.
The analogue video block is powered down, leading to a lower global consumption

STOP mode This is a low power mode. The analogue section of the VS6624 is switched off and all registers are accessed over the I²C interface. A run command received in this state automatically sets a transition through the Pause state to the run mode.

Note: The device must be in Stop mode to adjust output size.

The analogue video block is powered down, leading to a lower global consumption.

Pause mode In this mode all VS6624 clocks are running and all registers are accessible but no data is output from the device. The device is ready to start streaming but is halted. This mode is used to set up the required output format before outputting any data.

The analogue video block is powered down, leading to a lower global consumption

Note: The PowerManagement register can be adjusted in PAUSE mode but has no effect until the next RUN to PAUSE transition.

4.1 Streaming modes

RUN mode This is the fully operational mode. In running mode the device outputs a continuous stream of images, according to the set image format parameters and frame rate control parameters. The image size is derived through downscaling of the SXGA image from the pixel array.

ViewLive this feature allows different sizes, formats and reconstruction settings to be applied to alternate frames of data, while in run mode.

Snapshot mode The device can be configured to output a single frame according to the size, format and reconstruction settings in the relevant pipe setup bank. In normal operation this frame will be output, once the exposure, white balance and dark-cal systems are stable. To reduce the latency to output, the user may manually override the stability flags.

The snapshot mode command can be issued in either Run or Stop mode and the device will automatically return previous state after the snapshot is taken. The snapshot mode must not be entered into while viewlive is selected.

FLASHGUN mode In flashgun mode, the array is configured for use with an external flashgun. A flash is triggered and a single frame of data is output and the device automatically switches to Pause Mode.

VS6624 supports the following flashgun configurations:

- Torch Mode - user can manually switch on/off the FSO IO pin via a register setting. Independent of mode.
- Pulsed Mode - the flash output is synchronized to the image stream. There are two options available:
  - Pulsed flash with snapshot. Device outputs a single frame synchronized to flash.
  - Pulsed flash with viewfinder. Device outputs a flash pulse synchronized to a single frame in the image stream.
  - In the pulsed mode there are two possible pulse configurations:
  - Single pulse during the interframe period when all image lines are exposed. This is suitable for SCR and IGBT flash configurations. The falling edge of the pulse can be programmed to vary the width of the pulse.
  - Single pulse over entire integration period of frame. This is suitable for LED flash configurations.

4.2 Mode transitions

Transitions between operating modes are normally controlled by the host by writing to the *Host interface manager control* register. Some transitions can occur automatically after a time out. If there is no activity in the Pause state then an automatic transition to the Stop state occurs. This functionality is controlled by the Power management register, writing 0xFF disables the automatic transition to Stop.

The users control allows a transition between Stop and Run, at the state level the system will transition through a Pause state.

5 Clock control

Input clock

The VS6624 requires provision of an external reference clock. The external clock should be a DC coupled square wave. The clock signal may have been RC filtered. The clock input is fail-safe in power down mode.

The VS6624 contains an internal PLL allowing it to produce accurate frame rates from a wide range of input clock frequencies. The allowable input range is from 6.5MHz to 54MHz. The input clock frequency must be programmed in the registers. To program an input frequency of 6.5 MHz, the numerator can be set to 13 and the denominator to 2. The default input frequency is 12 MHz.

The VS6624 may be configured as a master or slave device. In normal (master operation) the input clock can be a different frequency to the output PCLK and all output clock configuration is based on the internal PLL. In slave configuration, the input clock is the same frequency and phase as the output PCLK. i.e. parallel output data is synchronized to the input clock.

6 Frame control

Sensor mode control

The VS6624 device can operate it's sensor array in three modes controlled by register SensorMode within *Mode setup*.

- SensorMode_SXGA - the full array is readout and the max frame rate achievable is 15fps
- SensorMode_VGA_analogue binning - the full array operates and a technique of analogue binning is used to output VGA at up to 30fps
- SensorMode_VGA_subsampled - the array is sub-sampled to output VGA at up to 30fps

Image size

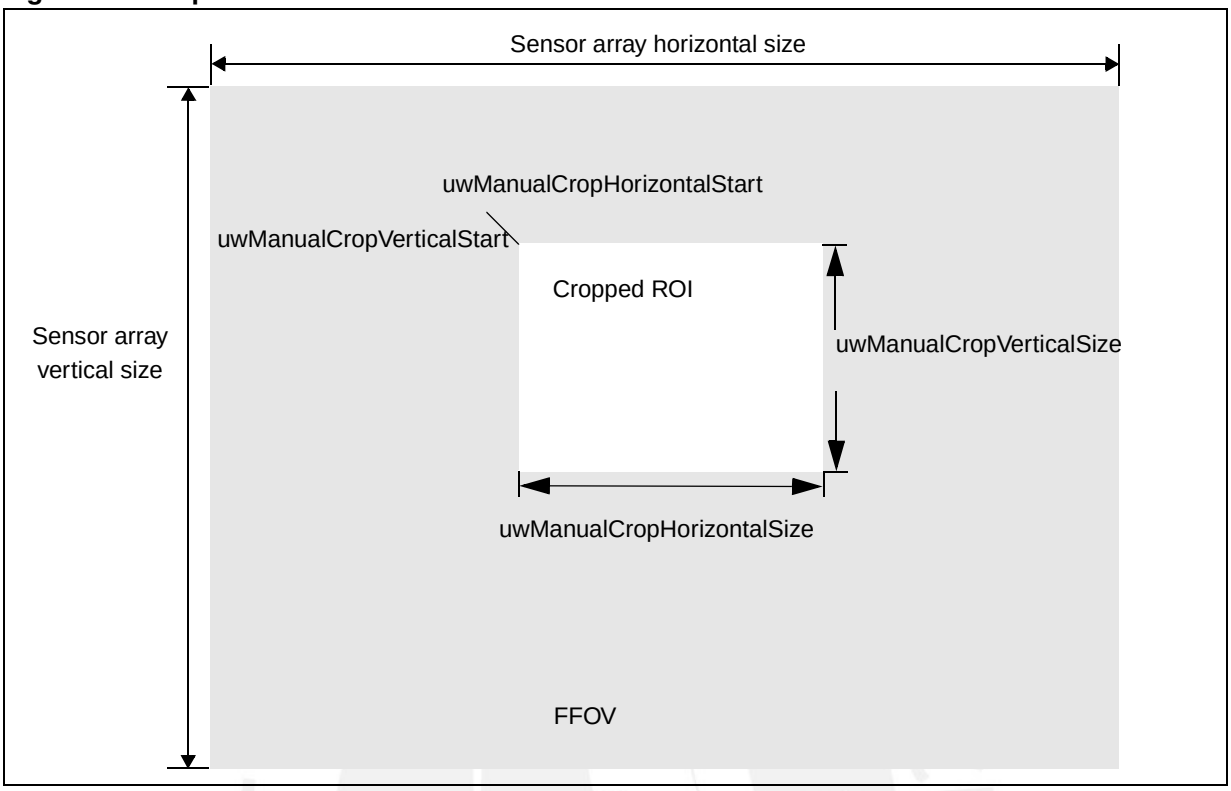
An output frame consists of a number of active lines and a number of interframe lines. Each line consists of embedded line codes (if selected), active pixel data and interline blank data. Note that by default the interline blanking data is *not* qualified by the PCLK and therefore is not captured by the host system.

The image size can be either the full output from the sensor, depending on sensor mode, or a scaled output, The output image size can be chosen from one of 7 pre-selected sizes or a manual image size can be input.

Cropping module

The VS6624 contains a cropping module which can be used to define a window of interest within the full SXGA array size. The user can set a start location and the required output size. *Figure 4* shows the example with pipe setup bank0.

Figure 4. Crop controls



Zoom

It is possible to zoom between the sensor size selected and the output size (if the output size selected equals the sensor mode size then no zoom can take place).

The zoom step size in both the horizontal and vertical directions are selectable and zoom controlled with the commands zoom_in, zoom_out and zoom_stop.

Pan

It is possible to pan left, right, up and down when the output size selected is smaller than the sensor size selected. (if the output size selected equals the sensor mode size then no pan can take place).

The pan step size in both the horizontal and vertical directions are selectable.

Frame rate control

The VS6624 features an extremely flexible frame rate controller. Using registers uwDesiredFrameRate_Num, and uwDesiredFrameRate_Den any desired frame rate between 2 and 15 fps can be selected for the SXGA sensor mode and between 1 and 30fps for a VGA sensor mode. To program a required frame rate of 7.5 fps the numerator can be set to 15 and the denominator to 2.

Horizontal mirror and vertical flip

The image data output from the VS6624 can be mirrored horizontally or flipped vertically (or both).

Video pipe setup

The VS6624 has a single video pipe, the control of this pipe can be loaded from either of two possible setups Pipesetupbank0 and Pipesetupbank1;

Pipe setup bank0 and *Pipe setup bank1*, control the operations shown below,

- image size
- zoom control
- pan control
- Crop control
- Image format (YUV 4:2:2, RGB565, etc....)
- Image controls (Contrast, Color saturation, Horizontal and vertical flip)

Pipe 0 RGB to YUV matrix manual control and *Pipe 1 RGB to YUV matrix manual control*, allow different RGB to YUV matrixes to be used for each pipe setup,

Pipe 0 gamma manual control and *Pipe 1 Gamma manual control*, allow different gamma settings to be used for each pipe setup.

Context switching

In normal operation, it is possible to control which pipe setup bank is used and to switch between banks without the need to stop streaming, the change will occur at the next frame boundary after the change to the register has been made.

For example this function allows the VS6624 to stream an output targeting a display (e.g. QQVGA RGB 444) then switch to capture an image (e.g. SXGA YUV 4:2:2) with no need to stop streaming or enter any other operating mode.

It is important to note the output size selected for both pipe setups must be appropriate to the sensor mode used, i.e. to configure PipeSetupBank0 to QQVGA and PipeSetupBank1 to SXGA the sensor mode must be set to SXGA.

The register *Mode setup* allows selection of the pipe setup bank, by default the Pipe setup bank 0 is used.

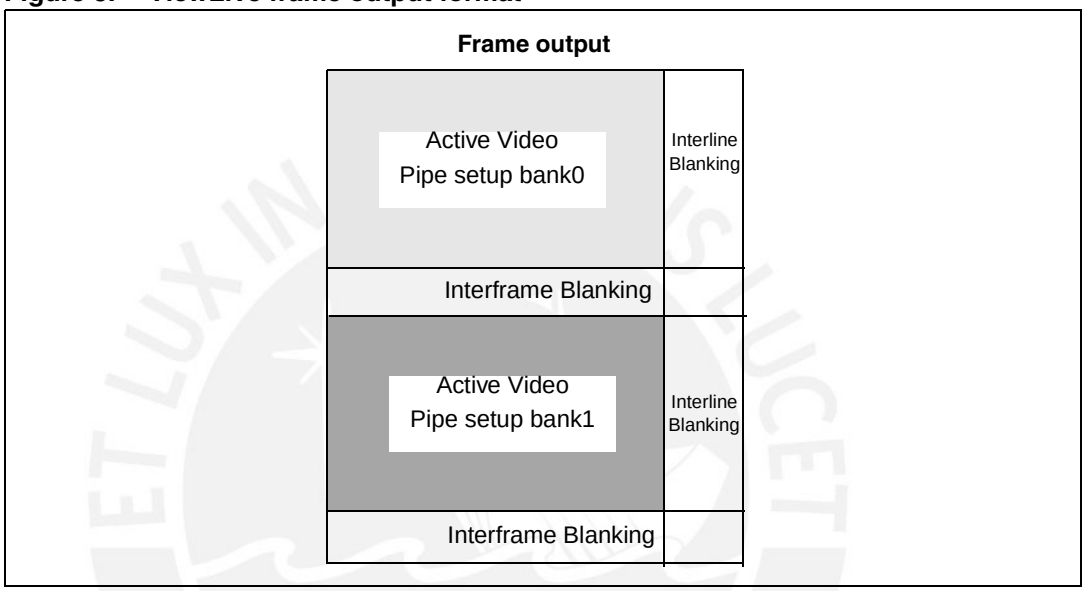
ViewLive Operation

ViewLive is an option which allows a different pipe setup bank to be applied to alternate frames of the output data.

The controls for VIewLive function are found in the register bank where the fEnable register allows the host to enable or disable the function and the binitialPipeSetupBank register selects which pipe setup bank is output first.

When ViewLive is enabled the output data switches between *Pipe setup bank0* and *Pipe setup bank1* on each alternate frame.

Figure 5. ViewLive frame output format



7 Output data formats

The VS6624 supports the following data formats:

- YUV4:2:2
- YUV4:0:0
- RGB565
- RGB444 (encapsulated as 565)
- RGB444 (zero padded)
- Bayer 10-bit
- Bayer 8-bit

The required data format is selected using the bdataFomat control found in the pipe setup bank registers. The various options available for each format are controlled using the bRgbsetup and bYuvSetup registers found in the *Output formatter control* registers.

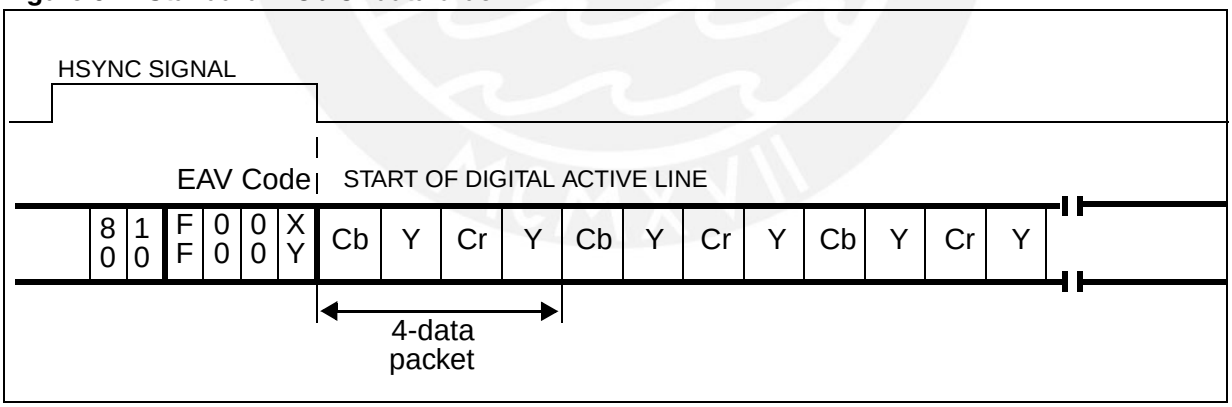
Line / Frame Blanking Data

The values which are output during line and frame blanking are an alternating pattern of 0x10 and 0x80 by default. These values may be changed by writing to the BlankData_MSB and BlankData_LSB registers in the *Output formatter control* bank.

YUV 4:2:2 data format

YUV 422 data format requires 4 bytes of data to represent 2 adjacent pixels. ITU601-656 defines the order of the Y, Cb and Cr components as shown in *Figure 6*.

Figure 6. Standard Y Cb Cr data order



The VS6624 bYuvSetup register can be programmed to change the order of the components as follows:

Figure 7. Y Cb Cr data swapping options register 0x2294 bYuvSetup

	Bit [1] Y first	Bit [0] Cb first	Components order in 4-byte data packet 1st	2nd	3rd	4th
	1	1	Y	Cb	Y	Cr
DEFAULT	0	1	Cb	Y	Cr	Y
	1	0	Y	Cr	Y	Cb
	0	0	Cr	Y	Cb	Y

YUV 4:0:0

The ITU protocol allows the encapsulation of various data formats over the link. The following data formats are also proposed encapsulated in ITU601-656 protocol:

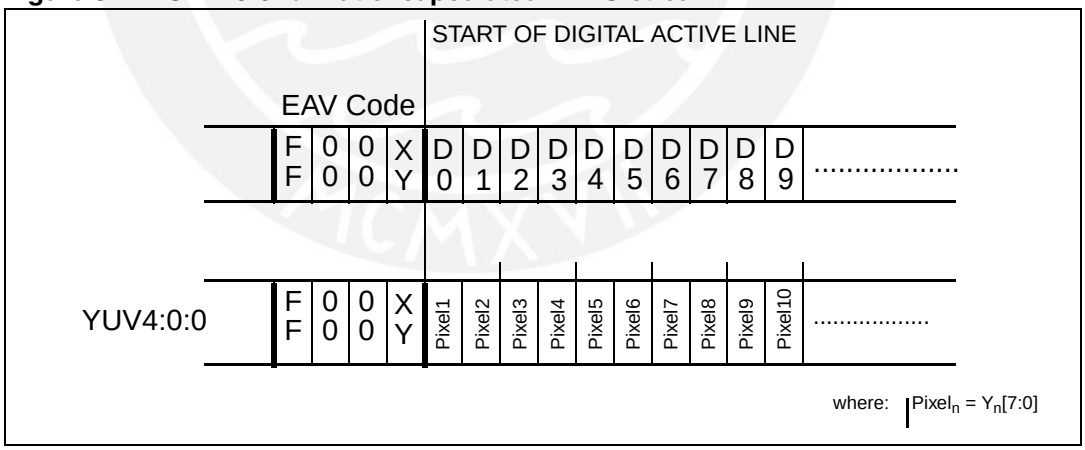
- YUV 4:0:0 - luminance data channel

This is done as described in *Figure 8*. In this output mode the output data per pixel is a single byte. Therefore the output PCLK and data rate is halved.

It is possible to reverse the overall bit order of the component through a register programming.

Note: False synchronization codes are avoided in the LSByte by adding or subtracting a value of one, dependent on detection of a 0 code or 255 code respectively.

Figure 8. YUV 4:0:0 format encapsulated in ITU stream



See *Output formatter control* for user interface control of output data formats.

RGB and Bayer 10 bit data formats

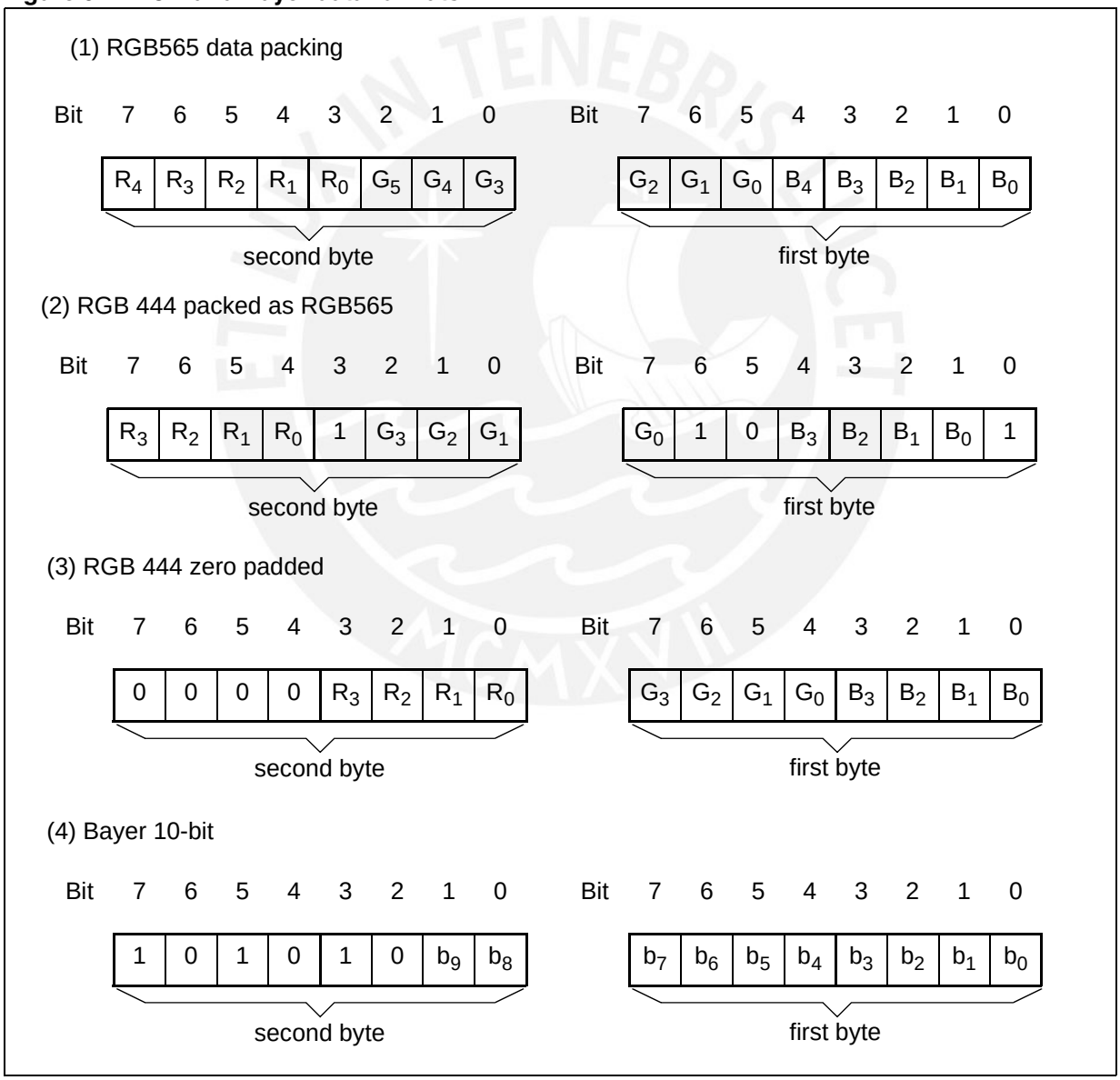
The VS6624 can output data in the following formats:

- RGB565
- RGB444 (encapsulated as RGB565)
- RGB444 (zero padded)
- Bayer 10-bit

Note: Pixels in Bayer 10-bit data output are defect corrected, correctly exposed and white balanced. Any or all of these functions can be disabled.

In each of these modes 2 bytes of data are required for each output pixel. The encapsulation of the data is shown in *Table 9*.

Figure 9. RGB and Bayer data formats



Manipulation of RGB data

It is possible to modify the encapsulation of the RGB data in a number of ways:

- swap the location of the RED and BLUE data
- reverse the bit order of the individual color channel data
- reverse the order of the data bytes themselves

Dithering

An optional dithering function can be enabled for each RGB output mode to reduce the appearance of contours produced by RGB data truncation. This is enabled through the DitherControl register.

Bayer 8-bit

The ITU protocol allows the encapsulation of various data formats over the link. The following data formats are also proposed encapsulated in ITU601-656 protocol:

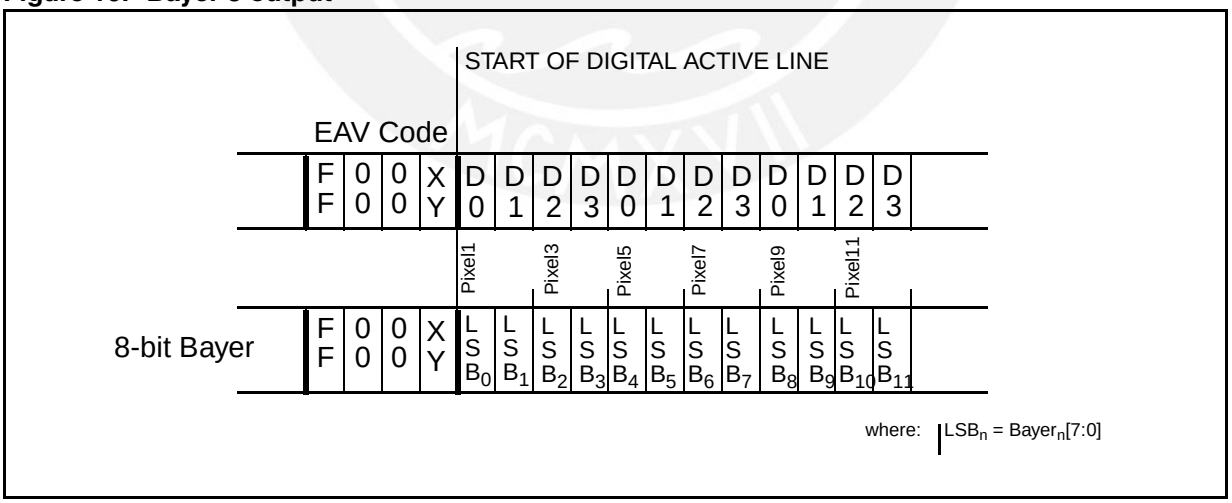
- RAW 8-bit bayer
- Truncated from 10-bit
- DPCM encoded from 10-bit

This is done as described in *Figure 10*. In this output mode the output data per pixel is a single byte. Therefore the output PCLK and data rate is halved.

It is possible to reverse the overall bit order of the individual bayer pixels through a register programming.

Note: False synchronization codes are avoided in the LSByte by adding or subtracting a value of one, dependent on detection of a 0 code or 255 code respectively.

Figure 10. Bayer 8 output



8 Data synchronization methods

External capture systems can synchronize with the data output from VS6624 in one of two ways:

1. Synchronization codes are embedded in the output data
2. Via the use of two additional synchronization signals: VSYNC and HSYNC

Both methods of synchronization can be programmed to meet the needs of the host system.

Embedded codes

The embedded code sequence can be inserted into the output data stream to enable the external host system to synchronize with the output frames. The code consists of a 4-byte sequence starting with 0xFF, 0x00, 0x00. The final byte in the sequence depends on the mode selected.

Two types of embedded codes are supported by the VS6624: Mode 1 (ITU656) and Mode 2. The bSyncCodeSetup register is used to select whether codes are inserted or not and to select the type of code to insert.

When embedded codes are selected each line of data output contains 8 additional clocks: 4 before the active video data and 4 after it.

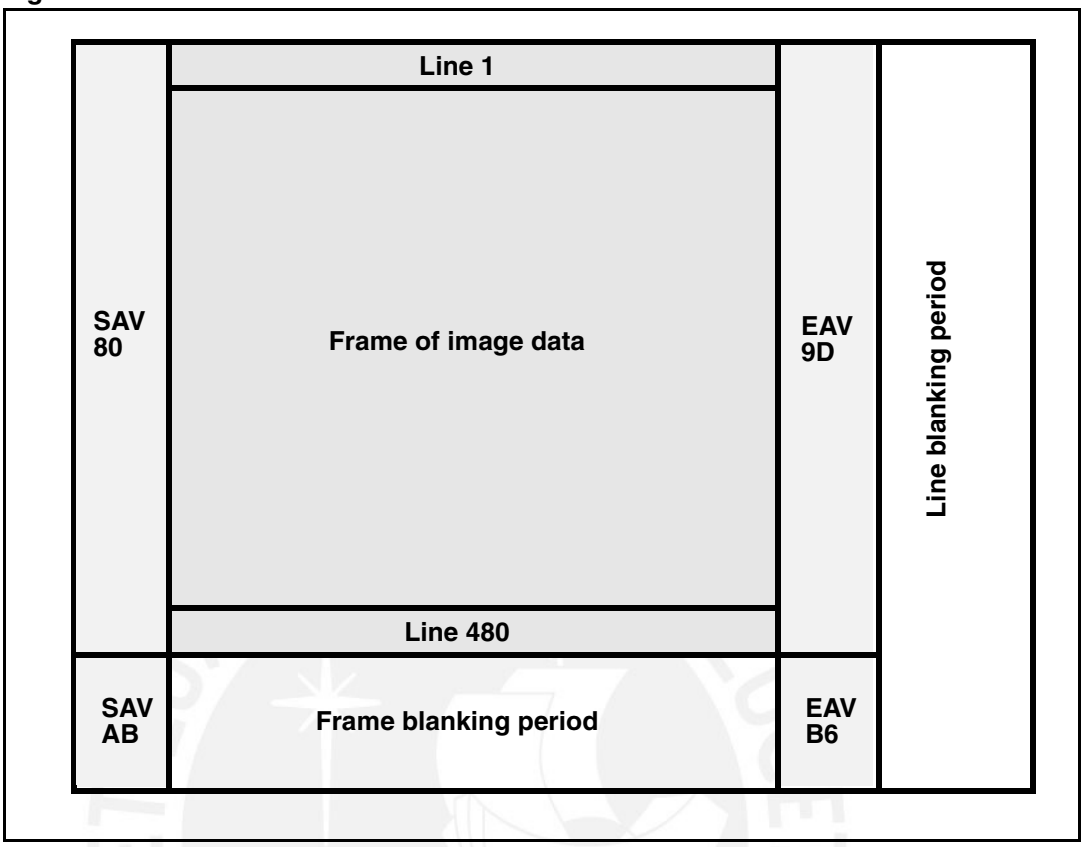
Prevention of false synchronization codes

The VS6624 is able to prevent the output of 0xFF and/or 0x00 data from being misinterpreted by a host system as the start of synchronization data. This function is controlled the bCodeCheckEnable register.

Mode 1 (ITU656 compatible)

The structure of an image frame with ITU656 codes is shown in *Figure 11*.

Figure 11. ITU656 frame structure with even codes



The synchronization codes for odd and even frames are listed in *Table 3* and *Table 4*. By default all frames output from the VS6624 are EVEN. It is possible to set all frames to be ODD or to alternate between ODD and EVEN using the SyncCodeSetup register in the *Output formatter control* register bank.

Table 3. ITU656 embedded synchronization code definition (even frames)

Name	Description	4-byte sequence
SAV	Line start - active	FF 00 00 80
EAV	Line end - active	FF 00 00 9D
SAV (blanking)	Line start - blanking	FF 00 00 AB
EAV (blanking)	Line end - blanking	FF 00 00 B6

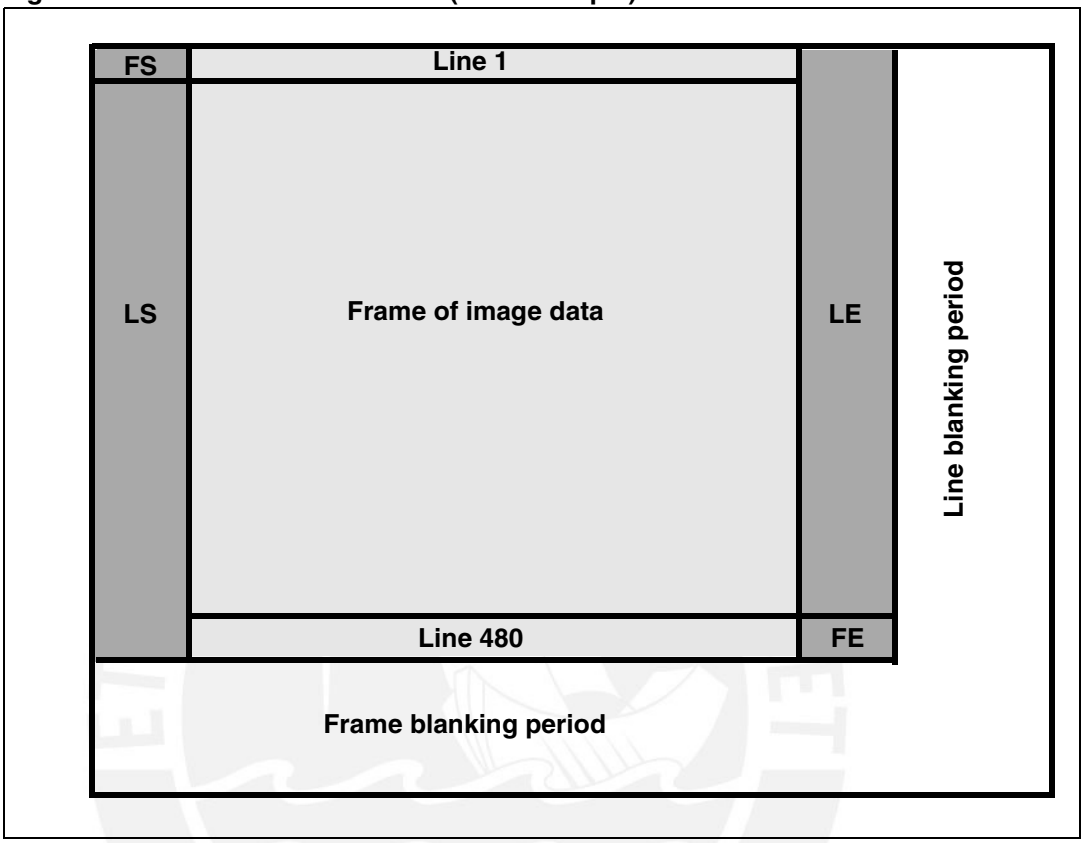
Table 4. ITU656 embedded synchronization code definition (odd frames)

Name	Description	4-byte sequence
SAV	Line start - active	FF 00 00 C7
EAV	Line end - active	FF 00 00 DA
SAV (blanking)	Line start - blanking	FF 00 00 EC
EAV (blanking)	Line end - blanking	FF 00 00 F1

Mode 2

The structure of a mode 2 image frame is shown *Figure 12*.

Figure 12. Mode 2 frame structure (VGA example)



For mode 2, the synchronization codes are as listed in *Table 5*.

Table 5. Mode 2 - embedded synchronization code definition

Name	Description	4-byte sequence
LS	Line start	FF 00 00 00
LE	Line end	FF 00 00 01
FS	Frame Start	FF 00 00 02
FE	Frame End	FF 00 00 03

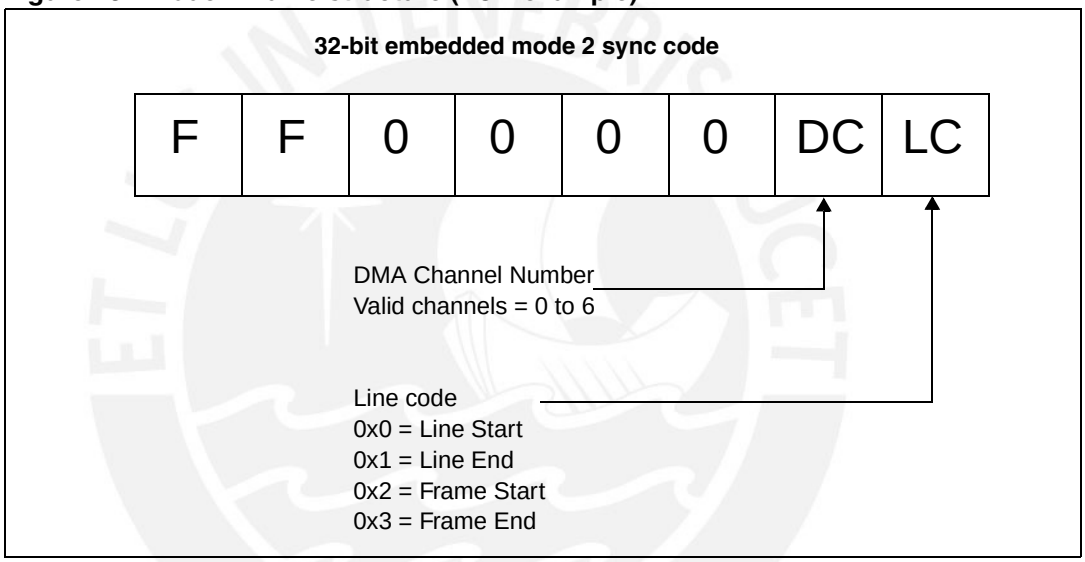
Mode 2 Logical DMA channels

The purpose of logical channels is to separate different data flows which are interleaved in the data stream, in the case of the VS6624 this allows the identification of the pipe setup bank used for an image frame. The DMA channel identifier number is directly encoded in the 4-byte mode2 embedded sync codes. The receiver can then monitor the DMA channel identifier and de-multiplex the interleaved video streams to their appropriate DMA channel. The bChannelID register can have the value 0 to 6. The DMA channel identifier must be fully programmable to allow the host to configure which DMA channels the different video data stream use.

- Logical channel control

The channel identifier is a part of Mode2 synchronization code, upper four bits of last byte of synchronization code. *Figure 13.* illustrates the synchronization code with logical channel identifiers.

Figure 13. Mode 2 frame structure (VGA example)



VSYNC and HSYNC

The VS6624 can provide two programmable hardware synchronization signals: VSYNC and HSYNC. The position of these signals within the output frame can be programmed by the user or an automatic setting can be used where the signals track the active video portion of the output frame regardless of its size.

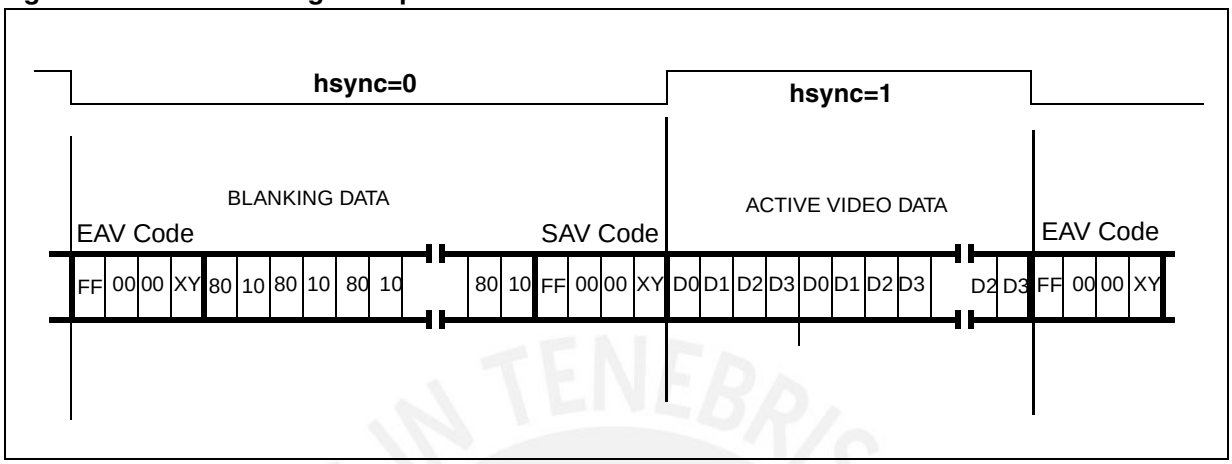
Horizontal synchronization signal (HSYNC)

The HSYNC signal is controlled by the bHSyncSetup register. The following options are available:

- enable/disable
- select polarity
- all lines or active lines only
- manual or automatic

In automatic mode the HSYNC signal envelops all the active video data on every line in the output frame regardless of the programmed image size. Line codes (if selected) fall outside the HSYNC envelope as shown in *Figure 14*.

Figure 14. HSYNC timing example



If manual mode is selected then the pixel positions for HSYNC rising edge and falling edge are programmable. The pixel position for the rising edge of HSYNC is programmed in the bHSyncRising registers. The pixel position for the falling edge of HSYNC is programmed in the bHSyncFalling registers.

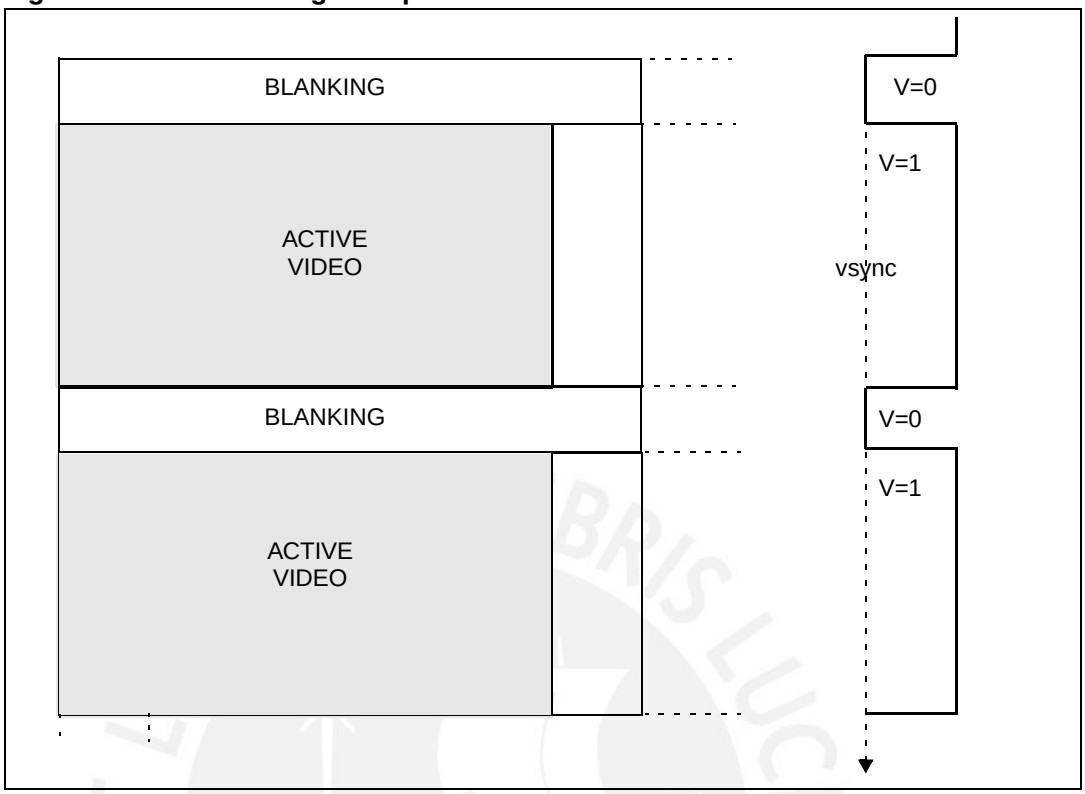
Vertical synchronization (VSYNC)

The VSYNC signal is controlled by the bSyncSetup register. The following options are available:

- enable/disable
- select polarity
- manual or automatic

In automatic mode the VSYNC signal envelops all the active video lines in the output frame regardless of the programmed image size as shown in *Figure 15*.

Figure 15. VSYNC timing example



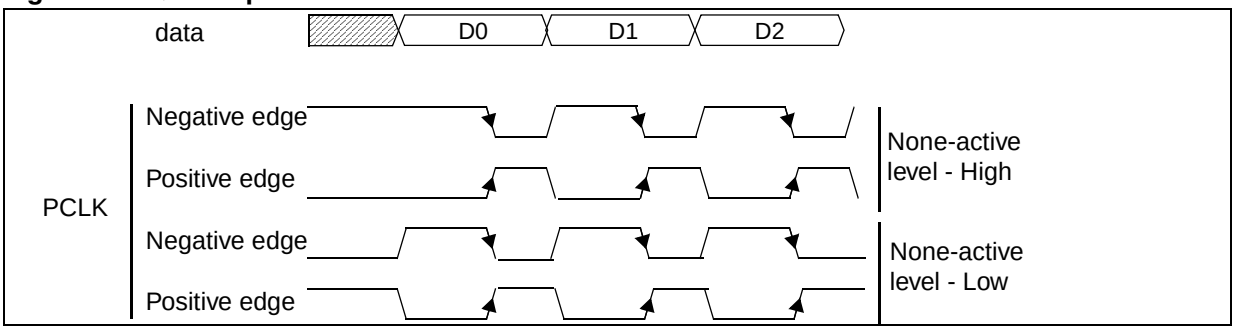
If manual mode is selected then the line number for VSYNC rising edge and falling edge is programmable. The rising edge of VSYNC is programmed in the bVsyncRisingLine registers, the pixel position for VSYNC rising edge is programmed in the bVsyncRisingPixel registers. Similarly the line count for the falling edge position is specified in the bVsyncFallingLine registers, and the pixel count is specified in the bVsyncFallingPixel registers.

Pixel clock (PCLK)

The PCLK signal is controlled by the *Output formatter control* register. The following options are available:

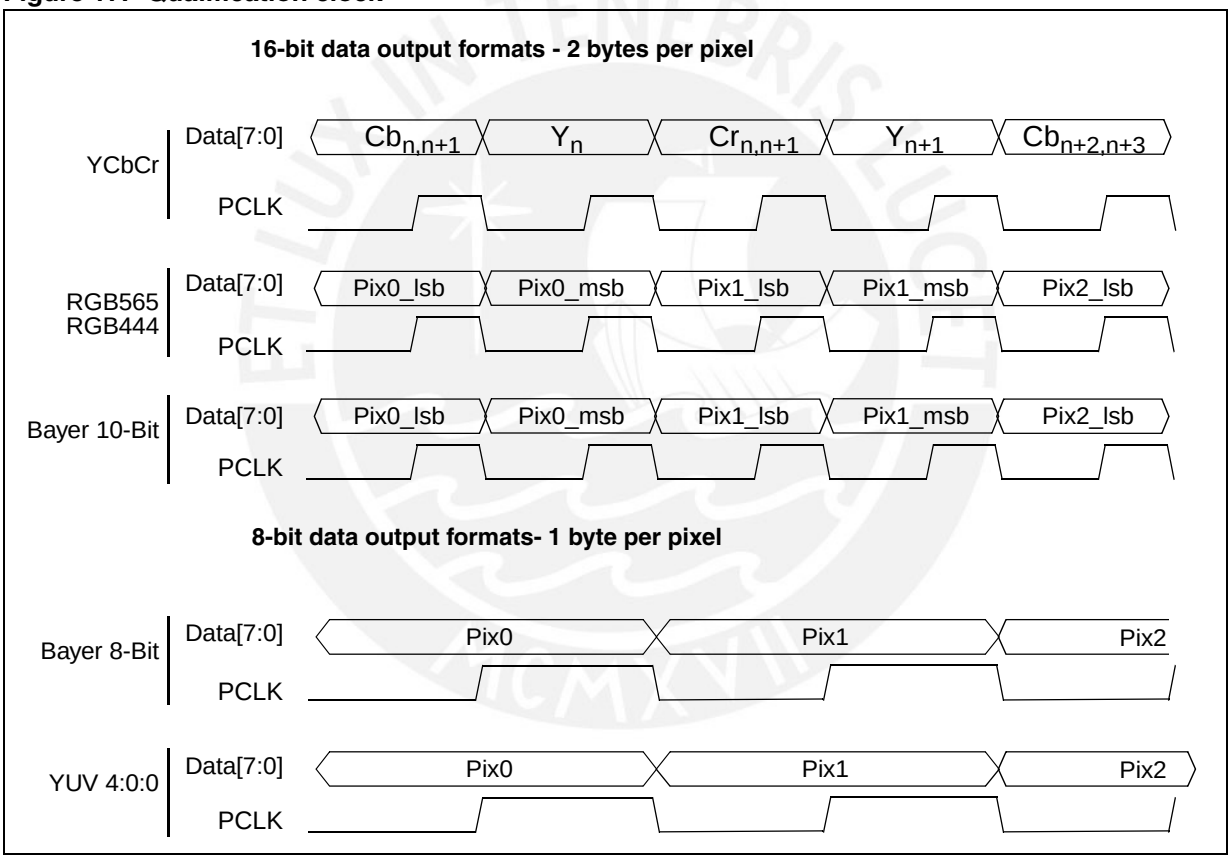
- enable/disable
- select polarity
- select starting phase
- qualify/don't qualify embedded synchronization codes
- enable/disable during horizontal blanking

Figure 16. QCLK options



The YUV, RGB and bayer timings are represented on *Figure 17*, with the associated qualifying pclk clock. The output clock rate is effectively halved for the bayer 8-bit and YUV4:0:0 modes where only one byte of output data is required per pixel.

Figure 17. Qualification clock



Master / Slave operation of PLCK

In normal operation VS6624 acts as a master. PCLK is independent of the input clock frequency and does not have a determined phase relation to the input clock.

In SLAVE operation the input clock frequency is the same as the output clock frequency and the output data is guaranteed with a certain phase relationship to the input clock. Internally, the VS6624 uses clocks generated from the internal PLL, but a retiming stage is used to re-sync the output to the input clock. In this output mode, derating is not possible.

9 Getting started

Initial power up

Before any communication is possible with the VS6624 the following steps must take place:

1. Apply VDD (1.8V or 2.8V)
2. Apply AVDD (2.8V)
3. Apply an external CLOCK (6.5MHz to 54MHz)
4. Assert CE line HIGH

These steps can all take place simultaneously. After these steps are complete a delay of 200 µs is required before any I²C communication can take place, see *Figure 3: Power up sequence*.

Minimum startup command sequence

1. Enable the microprocessor - before any commands can be sent to the VS6624, the internal microprocessor must be enabled by writing the value 0x02 to the MicroEnable register 0xC003 found in the *Low level control registers* Section.
2. Enable the digital I/O - after power up the digital I/O of the VS6624 is in a high-impedance state ('tri-state'). The I/O are enabled by writing the value 0x01 to the DIO_Enable register 0xC044 found in the *Low level control registers* Section.
3. The user can then program the system clock frequency and setup the required output format before placing the VS6624 in RUN mode by writing 0x02 to the *Host interface manager control* register 0x0180.

The above three commands represent the absolute minimum required to get video data output.

The default configuration results in an output of SXGA, 15 fps, YUV data format with ITU embedded codes requiring a external clock frequency of 12MHz.

In practice the user is likely to require to write some additional setup information prior to receive the required data output.

10 Host communication - I²C control interface

The interface used on the VS6624 is a subset of the I²C standard. Higher level protocol adaptations have been made to allow for greater addressing flexibility. This extended interface is known as the V2W interface.

10.1 Protocol

A message contains two or more bytes of data preceded by a START (S) condition and followed by either a STOP (P) or a repeated START (Sr) condition followed by another message.

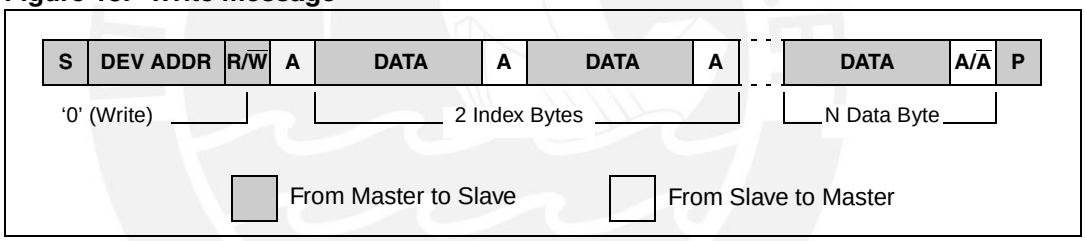
STOP and START conditions can only be generated by a V2W master.

After every byte transferred the receiving device must output an acknowledge bit which tells the transmitter if the data byte has been successfully received or not.

The first byte of the message is called the device address byte and contains the 7-bit address of the V2W slave to be addressed plus a read/write bit which defines the direction of the data flow between the master and the slave.

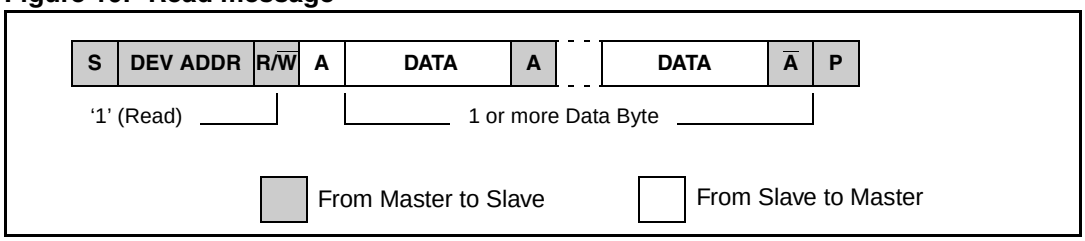
The meaning of the data bytes that follow device address changes depending whether the master is writing to or reading from the slave.

Figure 18. Write message



For the master writing to the slave the device address byte is followed by 2 bytes which specify the 16-bit internal location (index) for the data write. The next byte of data contains the value to be written to that register index. If multiple data bytes are written then the internal register index is automatically incremented after each byte of data transferred. The master can send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a STOP condition or sends a repeated START (Sr).

Figure 19. Read message



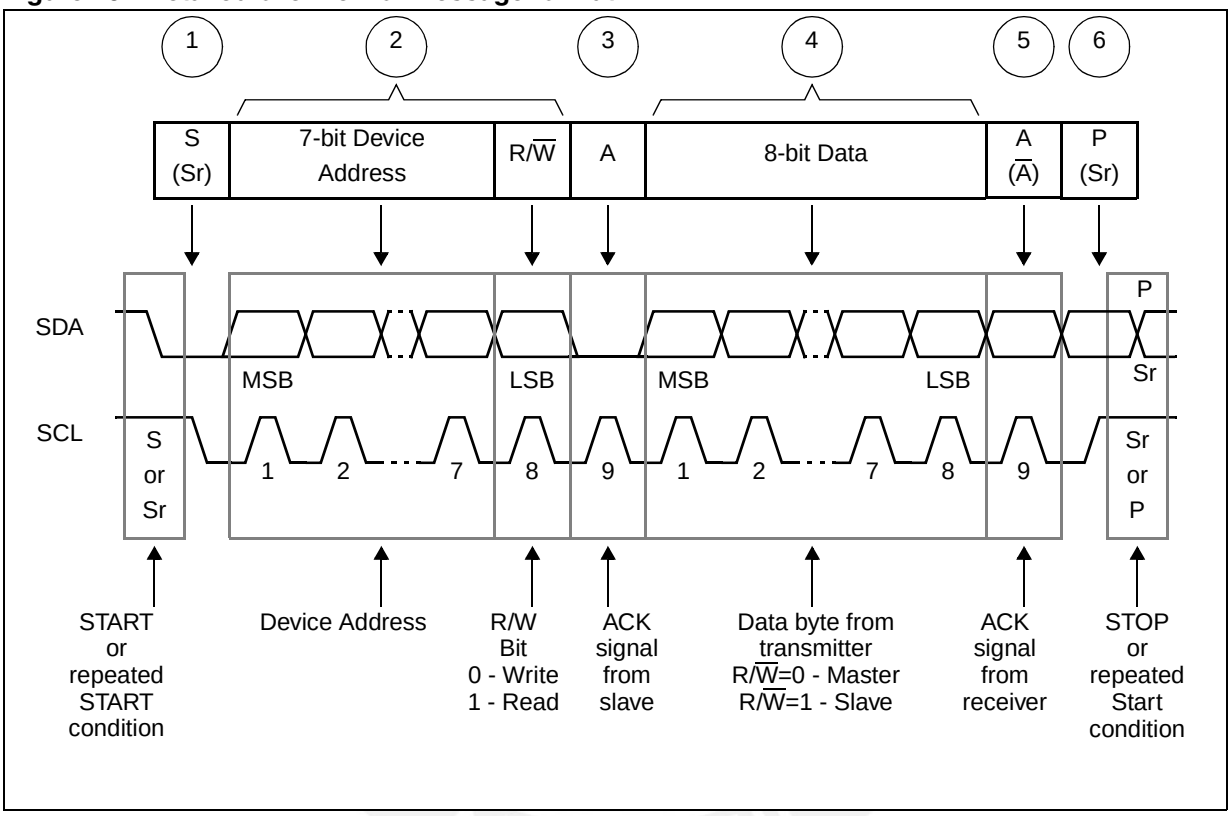
For the master reading from the slave the device address is followed by the contents of last register index that the previous read or write message accessed. If multiple data bytes are read then the internal register index is automatically incremented after each byte of data

read. A read message is terminated by the bus master generating a negative acknowledge after reading a final byte of data.

A message can only be terminated by the bus master, either by issuing a stop condition, a repeated start condition or by a negative acknowledge after reading a complete byte during a read operation.

10.2 Detailed overview of the message format

Figure 20. Detailed overview of message format



The V2W generic message format consists of the following sequence

1. Master generates a START condition to signal the start of new message.
2. Master outputs, MS bit first, a 7-bit device address of the slave the master is trying to communicate with followed by a R/$\overline{W}$ bit.
   a) R/$\overline{W}$ = 0 then the master (transmitter) is writing to the slave (receiver).
   b) R/$\overline{W}$ = 1 the master (receiver) is reading from the slave (transmitter).
3. The addressed slave acknowledges the device address.
4. Data transmitted on the bus
   a) When a write is performed then master outputs 8-bits of data on SDA (MS Bit first).
   b) When a read is performed then slave outputs 8-bits of data on SDA (MS Bit First).
5. Data receive acknowledge
   a) When a write is performed slave acknowledges data.
   b) When a read is performed master acknowledges data.

Repeat 4 and 5 until all the required data has been written or read.

Minimum number of data bytes for a read =1 (Shortest Message length is 2-bytes).

The master outputs a negative acknowledge for the data when reading the last byte of data. This causes the slave to stop the output of data and allows the master to generate a STOP condition.

6. Master generates a STOP condition or a repeated START.

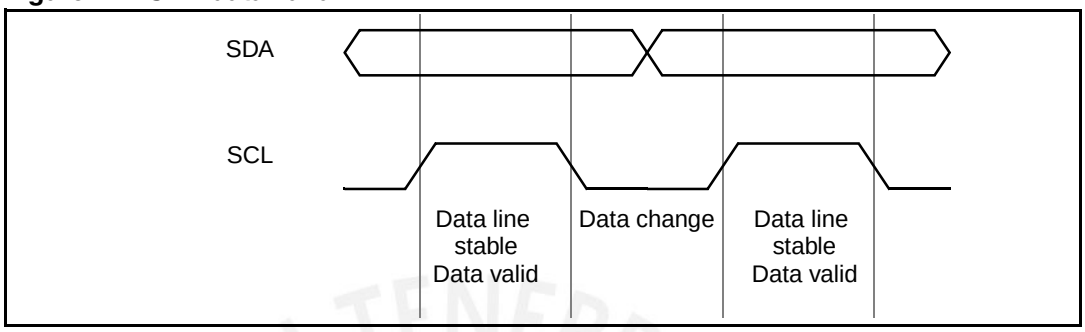
Figure 21. Device addresses

Sensor address	0	0	1	0	0	0	0	R/$\overline{W}$
Sensor write address 20_H	0	0	1	0	0	0	0	0
Sensor read address 21_H	0	0	1	0	0	0	0	1

10.3 Data valid

The data on SDA is stable during the high period of SCL. The state of SDA is changed during the low phase of SCL. The only exceptions to this are the start (S) and stop (P) conditions as defined below. (See *I²C slave interface* for full timing specification).

Figure 22. SDA data valid



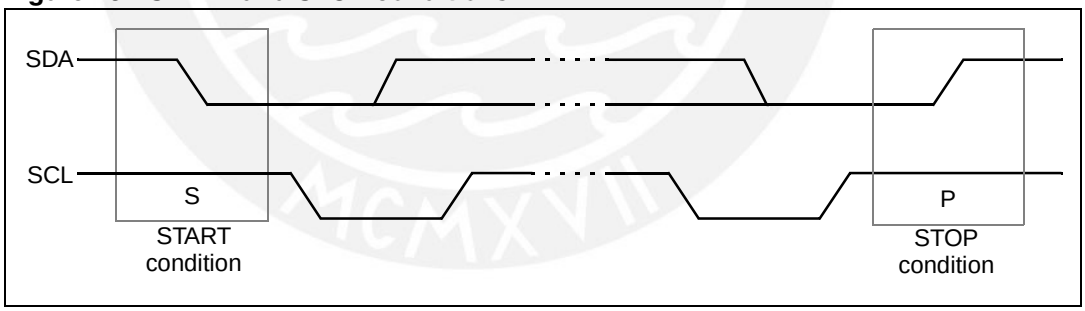
10.4 Start (S) and Stop (P) conditions

A START (S) condition defines the start of a V2W message. It consists of a high to low transition on SDA while SCL is high.

A STOP (P) condition defines the end of a V2W message. It consists of a low to high transition on SDA while SCL is high.

After STOP condition the bus is considered free for use by other devices. If a repeated START (Sr) is used instead of a stop then the bus stays busy. A START (S) and a repeated START (Sr) are considered to be functionally equivalent.

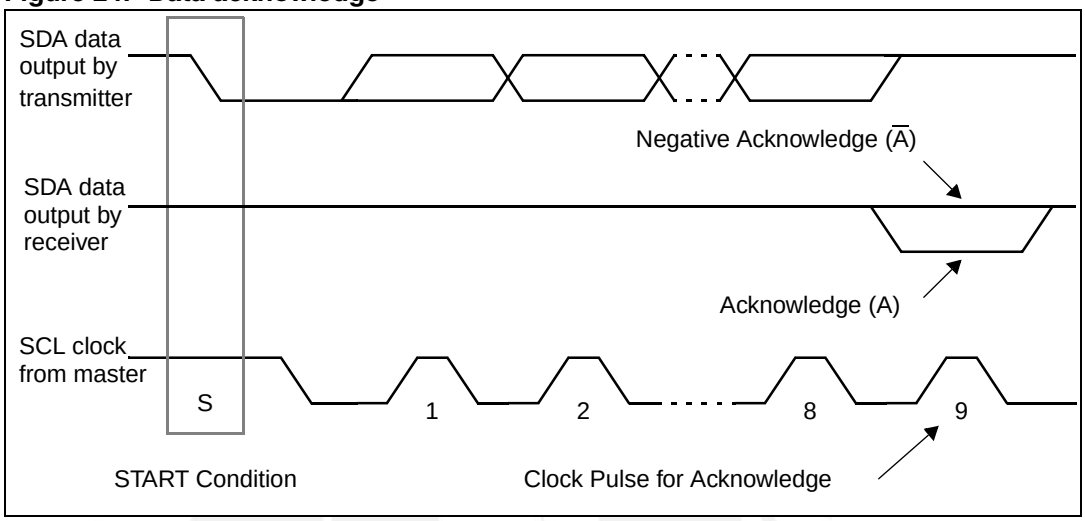
Figure 23. START and STOP conditions



10.5 Acknowledge

After every byte transferred the receiver must output an acknowledge bit. To acknowledge the data byte receiver pulls SDA during the 9th SCL clock cycle generated by the master. If SDA is not pulled low then the transmitter stops the output of data and releases control of the bus back to the master so that it can either generate a STOP or a repeated START condition.

Figure 24. Data acknowledge

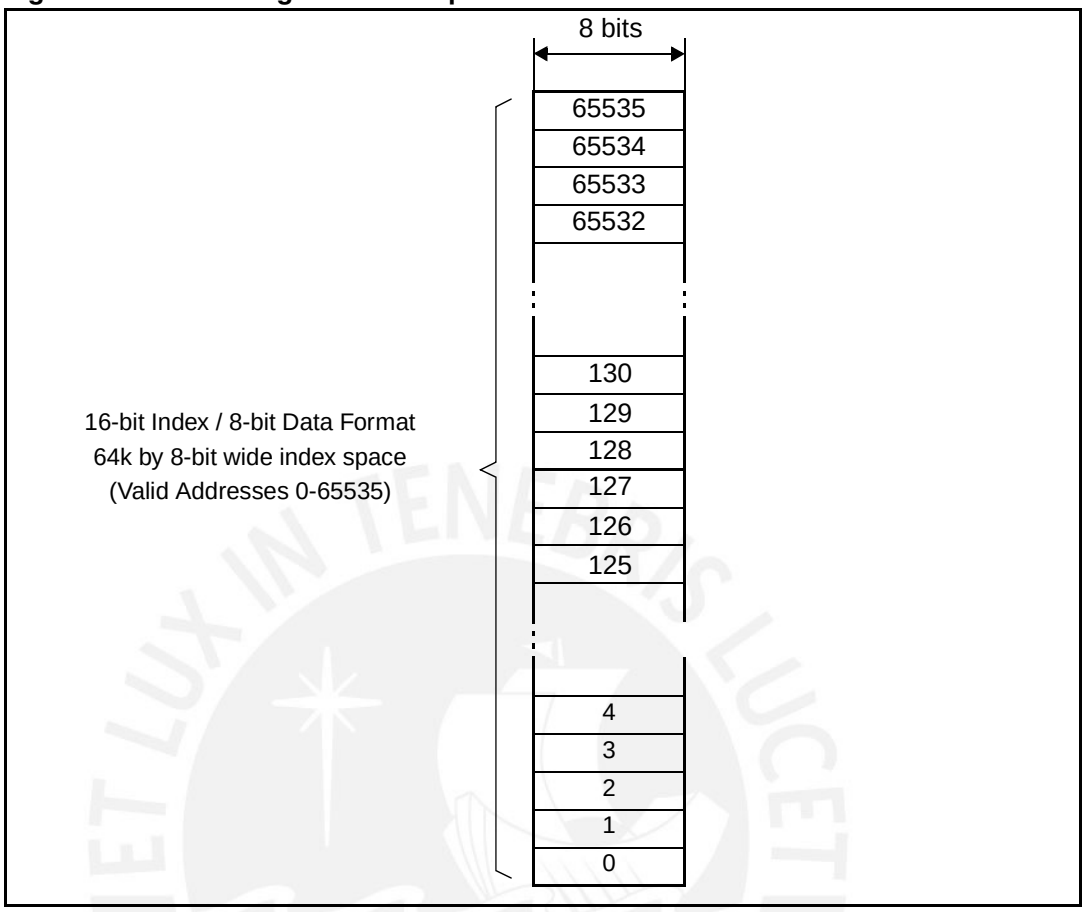


10.6 Index space

Communication using the serial bus centres around a number of registers internal to the either the sensor or the co-processor. These registers store sensor status, set-up, exposure and system information. Most of the registers are read/write allowing the receiving equipment to change their contents. Others (such as the chip id) are read only.

The internal register locations are organized in a 64k by 8-bit wide space. This space includes “real” registers, SRAM, ROM and/or micro controller values.

Figure 25. Internal register index space



10.7 Types of messages

This section gives guidelines on the basic operations to read data from and write data to VS6624.

The serial interface supports variable length messages. A message contains no data bytes or one data byte or many data bytes. This data can be written to or read from common or different locations within the sensor. The range of instructions available are detailed below.

- Single location, single byte data read or write.
- Write no data byte. Only sets the index for a subsequent read message.
- Multiple location, multiple data read or write for fast information transfers.

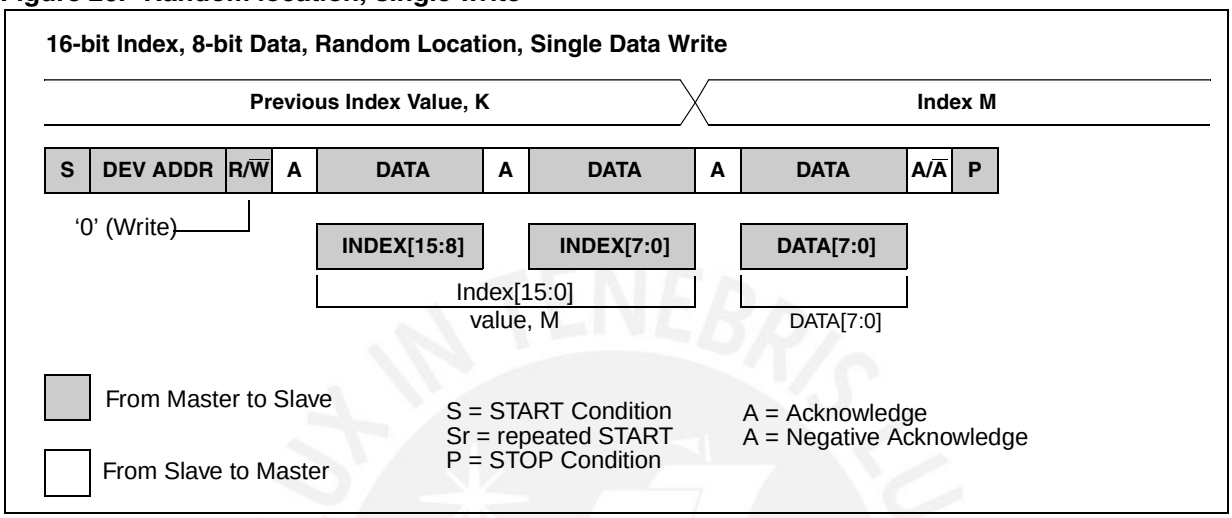
Any messages formats other than those specified in the following section should be considered illegal.

10.8 Random location, single data write

For the master writing to the slave the R/$\overline{W}$ bit is set to zero.

The register index value written is preserved and is used by a subsequent read. The write message is terminated with a stop condition from the master.

Figure 26. Random location, single write



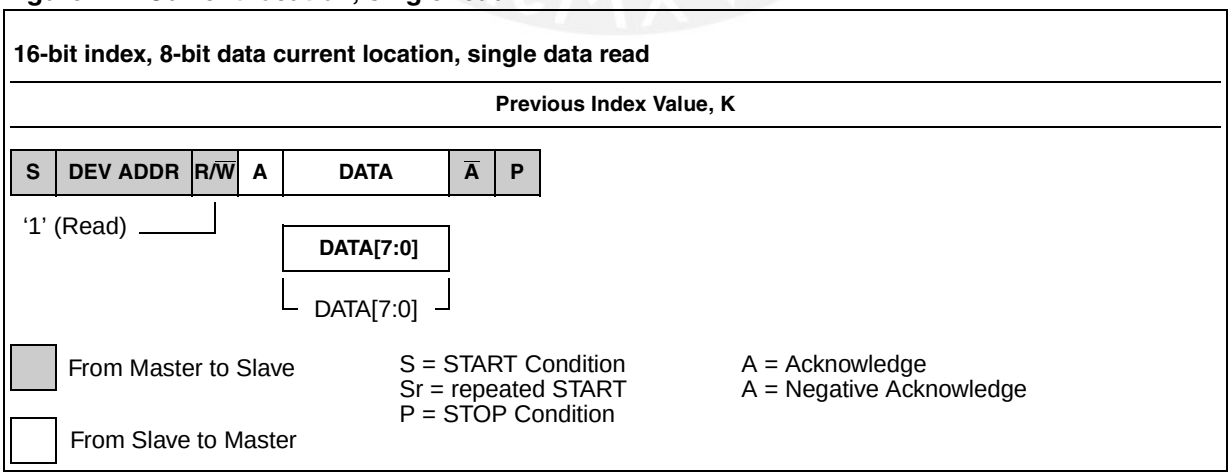
10.9 Current location, single data read

For the master reading from the slave the R/$\overline{W}$ bit is set to one. The register index of the data returned is that accessed by the previous read or write message.

The first data byte returned by a read message is the contents of the internal index value and NOT the index value. This was the case in older V2W implementations.

Note that the read message is terminated with a negative acknowledge ($\overline{A}$) from the master: it is not guaranteed that the master will be able to issue a stop condition at any other time during a read message. This is because if the data sent by the slave is all zeros, the SDA line cannot rise, which is part of the stop condition.

Figure 27. Current location, single read

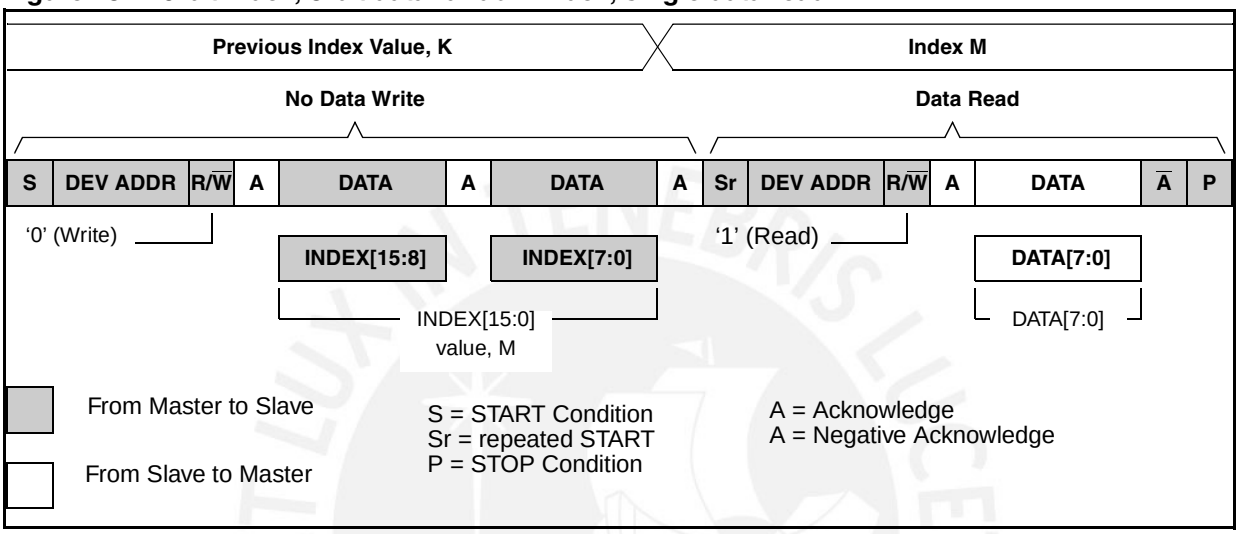


10.10 Random location, single data read

When a location is to be read, but the value of the stored index is not known, a write message with no data byte must be written first, specifying the index. The read message then completes the message sequence. To avoid relinquishing the serial to bus to another master a repeated start condition is asserted between the write and read messages.

As mentioned in the previous example, the read message is terminated with a negative acknowledge ($\overline{A}$) from the master.

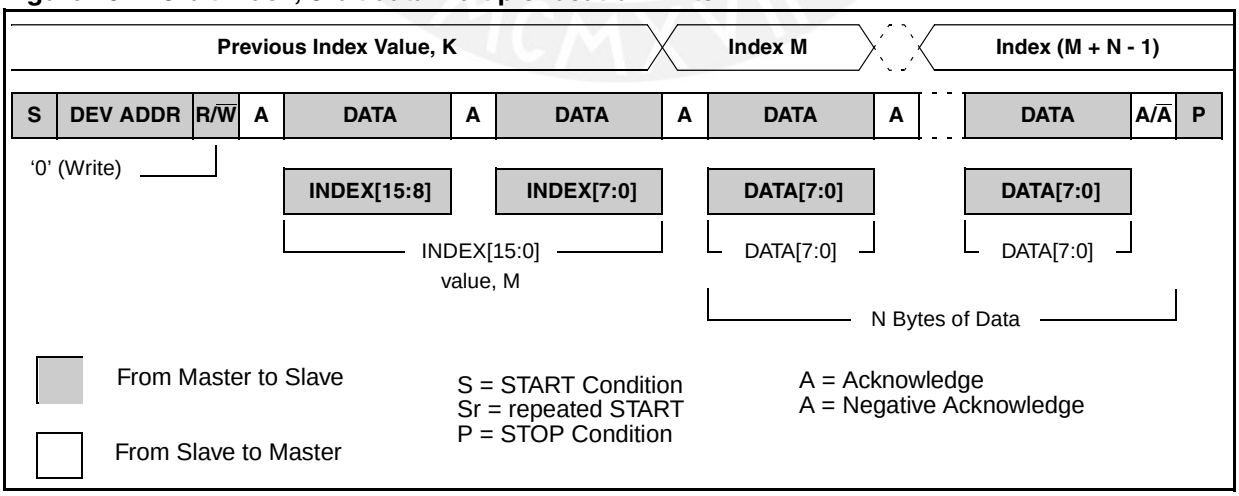
Figure 28. 16-bit index, 8-bit data random index, single data read



10.11 Multiple location write

For messages with more than 1 data byte the internal register index is automatically incremented for each byte of data output, making it possible to write data bytes to consecutive adjacent internal registers without having to send explicit indexes prior to sending each data byte.

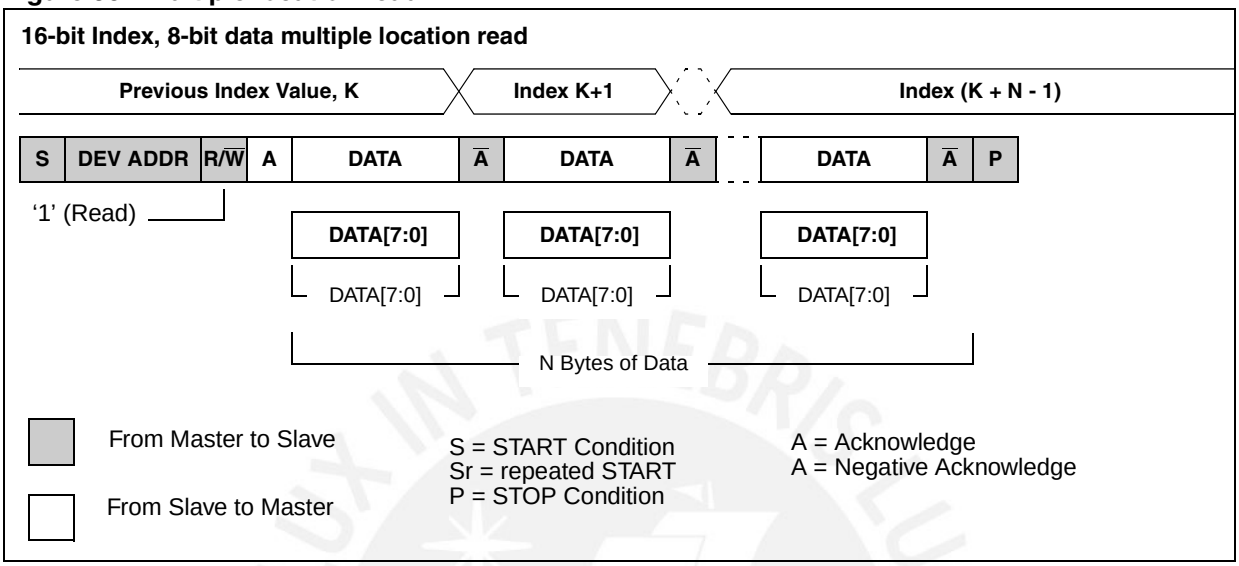
Figure 29. 16-bit index, 8-bit data multiple location write



10.12 Multiple location read stating from the current location

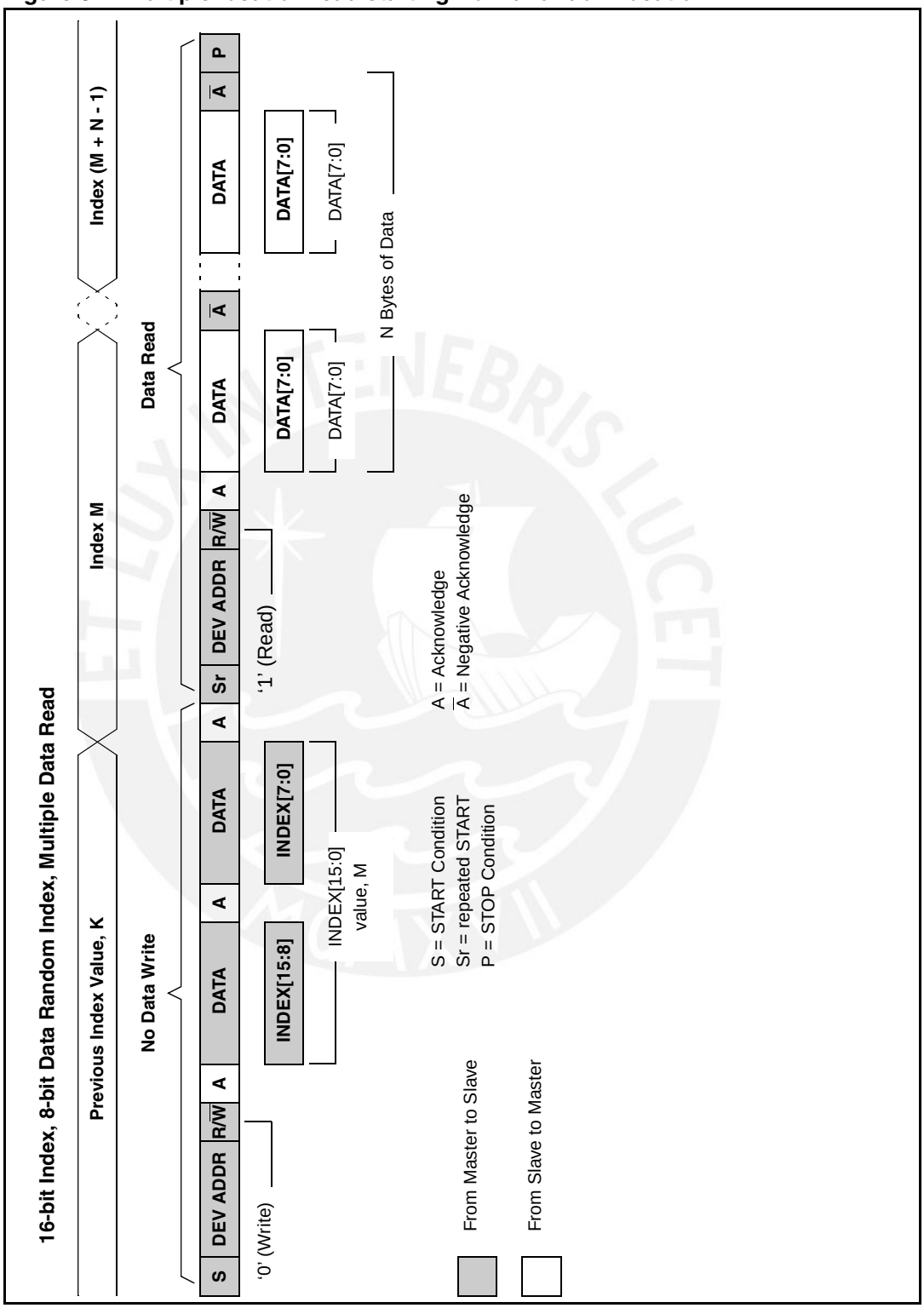
In the same manner to multiple location writes, multiple locations can be read with a single read message.

Figure 30. Multiple location read



10.13 Multiple location read starting from a random location

Figure 31. Multiple location read starting from a random location



11 Register map

The VS6624 I²C write address is 0x20.

To read or write to registers other than those in *Low level control registers* section the device must be switched on, this is done by writing 0x02 to 0xC003. Information on initial power up for the device can be found in the *Section 9: Getting started*.

All I²C locations contain an 8-bit byte. However, certain parameters require 16 bits to represent them and are therefore stored in more than 1 location.

Note: For all 16 bit parameters the MSB register must be written before the LSB register.

The data stored in each location can be interpreted in different ways as shown below. Register contents represent different data types as described in *Table 6*.

Table 6. Data type

Data Type	Description
BYTE	Single field register 8 bit parameter
UINT_16	Multiple field registers - 16 bit parameter
FLAG_e	Bit 0 of register must be set/cleared
CODED	Coded register - function depends on value written
FLOAT	Float Value

Float number format

Float 900 is used in ST co-processors to represent floating point numbers in 2 bytes of data. It conforms to the following structure:

Bit[15] = Sign bit (1 represents negative)

Bit[14:9] = 6 bits of exponent, biased at decimal 31

Bit[8:0] = 9 bits of mantissa

To convert a floating point number to Float 900, use the following procedure:

- represent the number as a binary floating point number. Normalize the mantissa and calculate the exponent to give a binary scientific representation of 1.xxxxxxxxx * 2^y.
- The x symbols should represent 9 binary digits of the mantissa, round or pad with zeros to achieve 9 digits in total. Remove the leading 1 from the mantissa as it is redundant.
- To calculate the y value Bias the exponent by adding to 31 decimal then converting to binary.
- The data can then be placed in the structure above.

Example

Convert -0.41 to Float 900

Convert the fraction into binary by successive multiplication by 2 and removal of integer component

0.41 * 2 = 0.82	0
0.82 * 2 = 1.64	1
0.64 * 2 = 1.28	1
0.28 * 2 = 0.56	0
0.56 * 2 = 1.12	1
0.12 * 2 = 0.24	0
0.24 * 2 = 0.48	0
0.48 * 2 = 0.96	0
0.96 * 2 = 1.92	1
0.92 * 2 = 1.84	1
0.84 * 2 = 1.68	1
0.68 * 2 = 1.36	1
0.36 * 2 = 0.72	0

This gives us -0.0110100011110.

We then normalize by moving the decimal point to give - 1.10100011110 * 2^-2.

The mantissa is rounded and the leading zero removed to give 101001000.
We add the exponent to the bias of 31 that gives us 29 or 11101.
A leading zero is added to give 6 bits 011101.

The sign bit is set at 1 as the number is negative.

This gives us 1011 1011 0100 1000 as our Float 900 representation or BB48 in hex.

To convert the encoded representation back to a decimal floating point, we can use the following formula.

Real is = (-1)^sign * ((512+mantissae)>> 9) * 2^(exp-31)

Thus to convert BB48 back to decimal, the following procedure is followed:

Note that >>9 right shift is equal to division by 2^9.

Sign = 1

Exponent = 11101 (29 decimal)

Mantissa = 101001000 (328 decimal)

This gives us:

real = (-1)^1 * ((512+328)/2^9) * 2^(29-31)

real = -1 * (840/512) * 2^(-2)

real = -1 * 1.640625 * 0.25

real = -0.41015625

When compared to the original -0.41, we see that some rounding errors have been introduced.

Low level control registers

Table 7. Low-level control registers

Index	LowLevelControlRegisters(1)	
0xC003	**MicroEnable**	
	Default value	0x1c
	Purpose	Used to power up the device
	Type	CODED
	Possible values	<0x1c> initial state after low to high transition of CE pin <0x02> Power enable for all MCU Clock- start device
0xC044	**DIO_Enable**	
	Default value	0x00
	Purpose	Enables the digital I/O of the device
	Type	CODED
	Possible values	<0> IO pins in a high impedance state ‘Tri-state’ <1> IO pins enabled

1. Can be controlled in all stable states.

Note: The default values for the above registers are true when the device is powered on, Ext. Clk input is present and the CE pin is high. All other registers can be read when the MicroEnable register is set to 0x02.

User interface map

Device parameters [read only]

Table 8. Device parameters [read only]

Index	DeviceParameters [read only](1)	
0x0001 (MSByte) 0x0002 (LSByte)	**uwDeviceId**	
	Purpose	device id e.g. 624
	Type	UINT
0x0004	**bFirmwareVsnMajor**	
	Type	BYTE
0x0006	**bFirmwareVsnMinor**	
	Type	BYTE
0x0008	**bPatchVsnMajor**	
	Type	BYTE
0x000a	**bPatchVsnMinor**	
	Type	BYTE

1. Can be accessed in all stable state.

Host interface manager control

Table 9. Host interface manager control

Index	HostInterfaceManagerControl(1)	
0x0180	**bUserCommand**	
	Default value	<0> UNINITIALISED
	Purpose	User level control of operating states
	Type	CODED
	Possible values	<0> UNINITIALISED - powerup default <1> BOOT - the boot command will identify the sensor & setup low level handlers <2> RUN - stream video <3> PAUSE- stop video streaming <4> STOP - low power mode, analogue powered down <3> SNAPSHOT- grab one frame at correct exposure without flashgun <6> FLASHGUN - grab one frame at correct exposure for flashgun

1. Can be controlled in all stable states

Host interface manager status

Table 10. Host interface manager status [Read only]

Index	HostInterfaceManagerStatus [Read only](1)	
0x0202	**bState**	
	Default Value	<16>_RAW
	Purpose	The current state of the mode manager.
	Type	CODED
	Possible values	<16>_RAW - default powerup state. <33> WAITING_FOR_BOOT - Waiting for ModeManager to signal BOOT event. <34> PAUSED - Booted, the input pipe is idle. <38>WAITING_FOR_RUN - Waiting for ModeManager to complete RUN setup. <49> RUNNING - The pipe is active. <50> WAITING_FOR_PAUSE - The host has issued a PAUSE command. The HostInterfaceManager is waiting for the ModeManager to signal PAUSE processing complete. <64> FLASHGUN - Grabbing a single frame. <80> STOPPED - Low power

1. Can be accessed in all stable states

Run mode control

Table 11. Run mode control

Index	RunModeControl(1)	
0x0280	**fMeteringOn**	
	Default Value:	<1> TRUE
	Purpose	If metering is off the Auto Exposure (AE) and Auto White Balance (AWB) tasks are disabled
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE

1. Can be controlled in all stable states

Mode setup

Table 12. Mode setup

Index	ModeSetup	
0x0302	**bNonViewLive_ActivePipeSetupBank (Can be controlled in all stable states)**	
	Default Value:	<0> PipeSetupbank_0
	Purpose	Select the active bank for non view live mode
	Type	CODED
	Possible values	<0> PipeSetupbank_0 <1>PipeSetupbank_1
0x0308	**SensorMode (Must be configured in STOP mode)**	
	Default value	<0>SensorMode_SXGA
	Purpose	Select the different sensor mode
	Type	CODED
	Possible values	<0>SensorMode_SXGA <1>SensorMode_VGA <2>SensorMode_VGANormal

Pipe setup bank0

Table 13. Pipe setup bank0

Index	PipeSetupBank0(1)	
0x0380	**bImageSize0 #**	
	Default value	<1> ImageSize_SXGA
	Purpose	required output dimension.
	Type	CODED
	Possible values	<1> ImageSize_SXGA <2> ImageSize_VGA <3> ImageSize_CIF <4> ImageSize_QVGA <5> ImageSize_QCIF <6> ImageSize_QQVGA <7> ImageSize_QQCIF <8> ImageSize_Manual - to use ManualSubSample and ManualCrop controls select Manual mode.
0x0383(MSB) 0x0384(LSB)	**uwManualHSize0 #**	
	Default value	0x00
	Purpose	if ImageSize_Manual selected, input required manual H size
	Type	UINT16

Table 13. Pipe setup bank0

Index	PipeSetupBank0(1)	
0x0387(MSB) 0x0388(LSB)	**uwManualVSize0 #**	
	Default value	0x00
	Purpose	if ImageSize_Manual selected, input required manual V size
	Type	UINT16
0x038b(MSB) 0x038c(LSB)	**uwZoomStepHSize0**	
	Default value	0x01
	Purpose	Set the zoom H step
	Type	UINT16
0x038f(MSB) 0x0390(LSB)	**uwZoomStepVSize0**	
	Default value	0x01
	Purpose	Set the zoom V step
	Type	UINT16
0x0392	**bZoomControl0**	
	Default value	<0> ZoomStop
	Purpose	control zoom in, zoom out and zoom stop
	Type	C
	Possible values	<0> ZoomStop <1> ZoomStart_In <2> ZoomStart_Out
0x0395(MSB) 0x0396(LSB)	**uwPanSteplHSize0**	
	Default value	0x00
	Purpose	Set the pan H step
	Type	UINT16
0x0399(MSB) 0x039a(LSB)	**uwPanStepVSize0**	
	Default value	0x00
	Purpose	Set the PanV step
	Type	UINT16

Table 13. Pipe setup bank0

Index	PipeSetupBank0(1)	
0x039c	**bPanControl0**	
	Default value	<0> Pan_Disable
	Purpose	control pandisable, pan right, pan left, pan up, pan down
	Type	C
	Possible values	<0> Pan_Disable <1> Pan_Right <2> Pan_Left <3> Pan_Down <4> Pan_Up
0x039e	**bCropControl0**	
	Default value	<1> Crop_auto
	Purpose	Select cropping manual or auto
	Type	C
	Possible values	<0> Crop_manual <1> Crop_auto
0x03a1(MSB) 0x03a2(LSB)	**uwManualCropHorizontalStart0**	
	Default value	0x00
	Purpose	Set the cropping H start address
	Type	UINT16
0x03a5(MSB) 0x03a6(LSB)	**uwManualCropHorizontalSize0**	
	Default value	0x00
	Purpose	Set the cropping H size
	Type	UINT16
0x03a9(MSB) 0x03aa(LSB)	**uwManualCropVerticalStart0**	
	Default value	0x00
	Purpose	Set the cropping Vstart address
	Type	UINT16
0x03ad(MSB) 0x03ae(LSB)	**uwManualCropVerticalSize0**	
	Default value	0x00
	Purpose	Set the cropping Vsize
	Type	UINT16

Table 13. Pipe setup bank0

Index	PipeSetupBank0[1]	
0x03b0	**bImageFormat0 #[2]**	
	Default value	<0> ImageFormat_YCbCr_JFIF
	Purpose	select required output image format.
	Type	CODED
	Possible values	<0> ImageFormat_YCbCr_JFIF <1> ImageFormat_YCbCr_Rec601 <2> ImageFormat_YCbCr_Custom - to use custom output select required RgbToYuvOutputSignalRange from 'PipeSetupBank' page. <3> ImageFormat_YCbCr_400 <4> ImageFormat_RGB_565 <5> ImageFormat_RGB_565_Custom - to use custom output select required RgbToYuvOutputSignalRange from 'PipeSetupBank' page. <6> ImageFormat_RGB_444 <7> ImageFormat_RGB_444_Custom - to use custom output select required RgbToYuvOutputSignalRange from 'PipeSetupBank' page. <9> ImageFormat_Bayer10_ThroughVP <10> ImageFormat_Bayer8_CompThroughVP-- to compress bayer data to 8 bits data <11> ImageFormat_Bayer8_TranThroughVP-- to truncate bayer data to 8 bits data
0x03b2	**bBayerOutputAlignment0**	
	Default value	<4> BayerOutputAlignment_RightShifted
	Purpose	set bayer output alignment
	Type	CODED
	Possible values	<4> BayerOutputAlignment_RightShifted <5> BayerOutputAlignment_LeftShifted
0x03b4	**bContrast0**	
	Default value	0x87
	Purpose	contrast control for both YCbCr and RGB output.
	Type	BYTE
0x03b6	**bColourSaturation0**	
	Default value	0x78
	Purpose	colour saturation control for both YCbCr and RGB output.
	Type	BYTE
0x03b8	**bGamma0**	
	Default value	0x0f
	Purpose	gamma settings.
	Type	BYTE
	Possible values	0 to 31

Table 13. Pipe setup bank0

Index	PipeSetupBank0(1)	
0x03ba	**fHorizontalMirror0**	
	Default Value:	0x00
	Purpose	Horizontal image orientation flip
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x03bc	**fVerticalFlip0**	
	Default Value:	0x00
	Purpose	Vertical image orientation flip
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x03be	**bChannelID**	
	Default value	0x00
	Purpose	Logical DMA Channel Number
	Type	BYTE
	Possible values	0 to 6

1. Can be controlled in all stable state.
   # denotes registers where changes will only be consumed during the transition to a RUN state.
2. It is possible to switch between any YCrCb (422) mode, RGB mode and Bayer 10bit or move between YCrCb 400 and a bayer8 mode without a requiring a transition to STOP, it is not possible to move between these groups of modes without first a transition to STOP then a BOOT.

Pipe setup bank1

Table 14. Pipe setup bank1

Index	PipeSetupBank1(1)	
0x0400	**bImageSize1 #**	
	Default value	<1> ImageSize_SXGA
	Purpose	required output dimension.
	Type	CODED
	Possible values	<1> ImageSize_SXGA <2> ImageSize_VGA <3> ImageSize_CIF <4> ImageSize_QVGA <5> ImageSize_QCIF <6> ImageSize_QQVGA <7> ImageSize_QQCIF <8> ImageSize_Manual - to use ManualSubSample and ManualCrop controls select Manual mode.
0x0403(MSB) 0x0404(LSB)	**uwManualHSize1 #**	
	Default value	0x00
	Purpose	if ImageSize_Manual selected, input required manual H size
	Type	UINT16
0x0407(MSB) 0x0408(LSB)	**uwManualVSize1 #**	
	Default value	0x00
	Purpose	if ImageSize_Manual selected, input required manual V size
	Type	UINT16
0x040b(MSB) 0x040c(LSB)	**uwZoomStepHSize1**	
	Default value	0x01
	Purpose	Set the zoom H step
	Type	UINT16
0x040f(MSB) 0x0410(LSB)	**uwZoomStepVSize1**	
	Default value	0x01
	Purpose	Set the zoom V step
	Type	UINT16

Table 14. Pipe setup bank1

Index	PipeSetupBank1(1)	
0x0412	**bZoomControl1**	
	Default value	<0> ZoomStop
	Purpose	control zoom in, zoom out, zoom stop
	Type	CODED
	Possible values	<0> ZoomStop <1> ZoomStart_In <2> ZoomStart_Out
0x0415(MSB) 0x0416(LSB)	**uwPanSteplHSize1**	
	Default value	0x00
	Purpose	Set the pan H step
	Type	UINT16
0x0419(MSB) 0x041a(LSB)	**uwPanStepVSize1**	
	Default value	0x00
	Purpose	Set the PanV step
	Type	UINT16
0x041c	**bPanControl1**	
	Default value	<0> Pan_Disable
	Purpose	control pandisable, pan right, pan left, pan up, pan down
	Type	C
	Possible values	<0> Pan_Disable <1> Pan_Right <2> Pan_Left <3> Pan_Down <4> Pan_Up
0x041e	**bCropControl1**	
	Default value	<1> Crop_auto
	Purpose	Select cropping manual or auto
	Type	C
	Possible values	<0> Crop_manual <1> Crop_auto
0x0421(MSB) 0x0422(LSB)	**uwManualCropHorizontalStart1**	
	Default value	0x00
	Purpose	Set the cropping H start address
	Type	UINT16

Table 14. Pipe setup bank1

Index	PipeSetupBank1[1]	
0x0425(MSB) 0x0426(LSB)	**uwManualCropHorizontalSize1**	
	Default value	0x00
	Purpose	Set the cropping H size
	Type	UINT16
0x0429(MSB) 0x042a(LSB)	**uwManualCropVerticalStart1**	
	Default value	0x00
	Purpose	Set the cropping Vstart address
	Type	UINT16
0x042d(MSB) 0x042e(LSB)	**uwManualCropVerticalSize1**	
	Default value	0x00
	Purpose	Set the cropping Vsize
	Type	UINT16
0x0430	**bImageFormat1[2]**	
	Default value	<0> ImageFormat_YCbCr_JFIF
	Purpose	select required output image format.
	Type	CODED
	Possible values	<0> ImageFormat_YCbCr_JFIF <1> ImageFormat_YCbCr_Rec601 <2> ImageFormat_YCbCr_Custom - to use custom output select required RgbToYuvOutputSignalRange from 'PipeSetupBank' page. <3> ImageFormat_YCbCr_400 <4> ImageFormat_RGB_565 <5> ImageFormat_RGB_565_Custom - to use custom output select required RgbToYuvOutputSignalRange from 'PipeSetupBank' page. <6> ImageFormat_RGB_444 <7> ImageFormat_RGB_444_Custom - to use custom output select required RgbToYuvOutputSignalRange from 'PipeSetupBank' page. <9> ImageFormat_Bayer10ThroughVP <10> ImageFormat_Bayer8CompThroughVP-- to compress bayer data to 8 bits data <11> ImageFormat_Bayer8TranThroughVP-- to truncate bayer data to 8 bits data
0x0432	**bBayerOutputAlignment1**	
	Default value	<4> BayerOutputAlignment_RightShifted
	Purpose	set bayer output alignment
	Type	CODED
	Possible values	<4> BayerOutputAlignment_RightShifted <5> BayerOutputAlignment_LeftShifted

Table 14. Pipe setup bank1

Index	PipeSetupBank1(1)	
0x0434	**bContrast1**	
	Default value	0x87
	Purpose	contrast control for both YCbCr and RGB output.
	Type	BYTE
0x0436	**bColourSaturation1**	
	Default value	0x78
	Purpose	colour saturation control for both YCbCr and RGB output.
	Type	BYTE
0x0438	**bGamma1**	
	Default value	0x0f
	Purpose	gamma settings.
	Type	BYTE
	Possible values	0 to 31
0x043a	**fHorizontalMirror1**	
	Default value	0x00
	Purpose	Horizontal image orientation flip
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x043c	**fVerticalFlip1**	
	Default value	0x00
	Purpose	Vertical image orientation flip
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x043e	**bChannelID**	
	Default value	0x00
	Purpose	Logical DMA Channel Number
	Type	BYTE
	Possible values	0 to 6

1. Can be controlled in all stable state. # denotes registers where changes will only be consumed during the transition to a RUN state.
2. It is possible to switch between any YCrCb (422) mode, RGB mode and Bayer 10bit or move between YCrCb 400 and a bayer8 mode without a requiring a transition to STOP, it is not possible to move between these groups of modes without first a transition to STOP then a BOOT.

Viewlive control

Table 15. ViewLive control

Index	ViewLiveControl	
0x0480	**fEnable (Can be controlled in all stable states)**	
	Default value	<0> FALSE
	Purpose	set to enable the View Live mode.
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x0482	**bInitialPipeSetupBank (must be setup in PAUSE or STOP mode)**	
	Default value	<0> PipeSetupBank_0
	Purpose	First frame output will be from PipeSetupBank selected by 'bInitialPipeSetupBank'. if ViewLive is enabled the next frame will be from the other PipeSetupBank, otherwise only one PipeSetupBank will be used.
	Type	CODED
	Possible values	<0> PipeSetupBank_0 <1> PipeSetupBank_1

Viewlive status [read only]

Table 16. Viewlive status

Index	ViewLiveStatus [read only]	
0x0500	**CurrentPipeSetupBank**	
	Default value	<0> PipeSetupBank_0
	Purpose	indicates the PipeSetupBank which has most recently been applied to the pixel pipe hardware.
	Type	CODED
	Possible values	<0> PipeSetupBank_0 <1> PipeSetupBank_1

Power management

Table 17. Power management

Index	PowerManagement(1)	
0x0580	**bTimeToPowerdown**	
	Default value	0x0f
	Purpose	Time (mSecs) from entering Pause mode until the system automatically transitions stop mode. 0xff disables the automatic transition.
	Type	BYTE

1. Must be configured in STOP mode

Video timing parameter host inputs

Table 18. Video timing parameter host inputs

Index	VideoTimingParameterHostInputs(1)	
0x0605 (MSByte) 0x0606 (LSByte)	**uwExternalClockFrequencyMhzNumerator**	
	Default value	0x0c
	Purpose	specifies the External Clock Frequency... external clock frequency = uwExternalClockFrequencyMhzNumerator/bExternalClockFrequencyMhzDenominator
	Type	UINT16
0x0608	**bExternalClockFrequencyMhzDenominator**	
	Default value	0x01
	Type	BYTE

1. Should be configured in the RAW state

Video timing control

Table 19. Video timing control

Index	VideoTimingControl(1)	
0x0880	**bSysClkMode**	
	Default value	0x00
	Purpose	Decides system centre clock frequency
	Type	CODED
	Possible values	<0>12MHz Mode <1>13MHz Mode <2>13.5MHz Mode <3>Slave Mode

1. Should be configured in the RAW state

Frame dimension parameter host inputs

Table 20. Frame dimension parameter host inputs

Index	FrameDimensionParameterHostInputs(1)	
0x0c80	**bLightingFrequencyHz**	
	Default value	0x00
	Purpose	AC Frequency - used for flicker free time period calculations this mains frequency determines the flicker free time period.
	Type	BYTE
0x0c82	**fFlickerCompatibleFrameLength**	
	Default value	<0> FALSE
	Purpose	flicker_compatible_frame_length
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE

1. Can be controlled in all stable states

Static frame rate control

Table 21. Static frame rate control

Index	StaticFrameRateControl(1)	
0x0d81 (MSByte) 0x0d82 (LSByte)	**uwDesiredFrameRate_Num**	
	Default value	0x0f
	Purpose	Numerator for the Frame Rate
	Type	UINT16
0x0d84	**bDesiredFrameRate_Den**	
	Default value	0x01
	Purpose	Denominator for the Frame Rate
	Type	BYTE

1. Can be controlled in all stable states

Automatic Frame rate control

Table 22. Automatic Frame Rate Control

Index	AutomaticFrameRateControl(1)	
0x0e80	**bDisableFrameRateDamper**	
	Default value	0x00
	Purpose	Defines the mode in which the framerate of the system would work
	Type	
	Possible values	<0> Manual <1> Auto
0x0e8c (MSByte) 0x0e8a (LSByte)	**bMinimumDamperOutput**	
	Default value	0x00
	Purpose	Sets the minimum framerate employed when in automatic framerate mode.
	Type	UINT16

1. Can be controlled in all stable states

Exposure controls

Table 23. Exposure controls

Index	ExposureControls(1)	
0x1180	**bMode**	
	Default value	<0> AUTOMATIC_MODE
	Purpose	Sets the mode for the Exposure Algorithm
	Type	CODED
	possible values	<0> AUTOMATIC_MODE - Automatic Mode of Exposure which includes computation of Relative Step <1> COMPILED_MANUAL_MODE - Compiled Manual Mode in which the desired exposure is given and not calculated by algorithm <2> DIRECT_MANUAL_MODE - Mode in which the exposure parameters are input directly and not calculated by compiler <3> FLASHGUN_MODE - Flash Gun Mode in which the exposure parameters are set to fixed values

Table 23. Exposure controls

Index	ExposureControls[1]	
0x1182	**bMetering**	
	Default value	<0> ExposureMetering_flat
	Purpose	Weights to be associated with the zones for calculating the mean statistics Exposure Weight could Centered, Backlit or Flat
	Type	C
	possible values	<0> ExposureMetering_flat - Uniform gain associated with all pixels <1> ExposureMetering_backlit - more gain associated with centre pixels and bottom pixels <2> ExposureMetering_centred - more gain associated with centre pixels
0x1184	**bManualExposureTime_Num**	
	Default value	0x01
	Purpose	Exposure Time for Compiled Manual Mode in seconds. Num/Den gives required exposure time
	Type	BYTE
0x1186	**bManualExposureTime_Den**	
	Default value	0x1e
	Type	BYTE
0x1189 (MSByte) 0x118a (LSByte)	**fpManualFloatExposureTime**	
	Default value	0x59aa (15008)
	Purpose	Exposure Time for the Manual Mode. This value is in uSecs
	Type	FLOAT
0x1190	**iExposureCompensation**	
	Default value	0x00
	Purpose	Exposure Compensation - a user choice for setting the runtime target. A unit of exposure compensation corresponds to 1/6 EV. Default value according to the Nominal Target of 30 is 0. Coded Value of Exposure compensation can take values from -25 to 12.
	Type	INT8
0x1195 (MSByte) 0x1196 (LSByte)	**uwDirectModeCoarseIntegrationLines**	
	Default value	0x00
	Purpose	Coarse Integration Lines to be set for Direct Mode
	Type	UINT16

Table 23. Exposure controls

Index	ExposureControls[1]	
0x1199 (MSByte) 0x119a (LSByte)	**uwDirectModeFineIntegrationPixels**	
	Default value	0x00
	Purpose	Fine Integration Pixels to be set for Direct Mode
	Type	UINT16
0x119d (MSByte) 0x119e (LSByte)	**fpDirectModeAnalogGain**	
	Default value	0x00
	Purpose	Analog Gain to be set for Direct Mode
	Type	FLOAT
0x11a1 (MSByte) 0x11a2 (LSByte)	**fpDirectModeDigitalGain**	
	Default value	0x00
	Purpose	Digital Gain to be set for Direct Mode
	Type	FLOAT
0x11a5 (MSByte) 0x11a6 (LSByte)	**uwFlashGunModeCoarseIntLines**	
	Default value	0x00
	Purpose	Coarse Integration Lines to be set for Flash Gun Mode
	Type	UINT16
0x11a9 (MSByte) 0x11aa (LSByte)	**uwFlashGunModeFineIntPixels**	
	Default value	0x00
	Purpose	Fine Integration Pixels to be set for Flash Gun Mode
	Type	UINT16
0x11ad (MSByte) 0x11ae (LSByte)	**fpFlashGunModeAnalogGain**	
	Default value	0x00
	Purpose	Analog Gain to be set for Flash Gun Mode
	Type	FLOAT
0x11b1 (MSByte) 0x11b2 (LSByte)	**fpFlashGunModeDigitalGain**	
	Default value	0x00
	Purpose	Digital Gain to be set for Flash Gun Mode
	Type	FLOAT

Table 23. Exposure controls

Index	ExposureControls[1]	
0x11b4	**fFreezeAutoExposure**	
	Default value	<0> FALSE
	Purpose	Freeze auto exposure
	Type	Flag_e
	possible values	<0> FALSE <1> TRUE
0x11b7 (MSByte) 0x11b8 (LSByte)	**fpUserMaximumIntegrationTime**	
	Default value	0x647f (654336)
	Purpose	User Maximum Integration Time in microseconds. This control takes in the maximum integration time that host would like to support. This would in turn give an idea of the degree of “wobbly pencil effect” acceptable to Host.
	Type	FLOAT
0x11bb (MSByte) 0x11bc (LSByte)	**fpRecommendFlashGunAnalogGainThreshold**	
	Default value	0x4200 (4)
	Purpose	Recommend flash gun analog gain threshold value
	Type	FLOAT
0x11c0	**bAntiFlickerMode**	
	Default value	<0> AntiFlickerMode_Inhibit
	Purpose	Anti flicker mode
	Type	CODED
	Possible values	<0> AntiFlickerMode_Inhibit <1> AntiFlickerMode_ManualEnable <2>AntiFlickerMode_AutomaticEnable

1. Can be controlled in all stable states

White balance control

Table 24. White balance control parameters

Index	WBControlParameters(1)	
0x1480	**bMode**	
	Default value	<1> AUTOMATIC
	Purpose	For setting Mode of the white balance
	Type	CODED
	possible values	<0> OFF - No White balance, all gains will be unity in this mode <1> AUTOMATIC - Automatic mode, relative step is computed here <3> MANUAL_RGB - User manual mode, gains are applied manually <4> DAYLIGHT_PRESET - DAYLIGHT and all the modes below, fixed value of gains are applied here. <5> TUNGSTEN_PRESET <6> FLUORESCENT_PRESET <7> HORIZON_PRESET <8> MANUAL_COLOUR_TEMP <9> FLASHGUN_PRESET
0x1482	**bManualRedGain**	
	Default value	0x00
	Purpose	User setting for Red Channel gain
	Type	BYTE
0x1484	**bManualGreenGain**	
	Default value	0x00
	Purpose	User setting for Green Channel gain
	Type	BYTE
0x1486	**bManualBlueGain**	
	Default value	0x00
	Purpose	User setting for Blue Channel gain
	Type	BYTE
0x148b (MSByte) 0x148c (LSByte)	**fpFlashRedGain**	
	Default value	0x3e80 (1.250)
	Purpose	RedGain For FlashGun
	Type	FLOAT
0x148f (MSByte) 0x1490 (LSByte)	**fpFlashGreenGain**	
	Default value	0x3e00 (1.000)
	Purpose	Green Gain For FlashGun
	Type	FLOAT

Table 24. White balance control parameters

Index	WBControlParameters(1)	
0x1493 (MSByte) 0x1494 (LSByte)	**fpFlashBlueGain**	
	Default value	0x3e8a (1.269531)
	Purpose	BlueGain For FlashGun
	Type	FLOAT

1. Can be controlled in all stable states

Sensor setup

Table 25. Sensor setup

Index	SensorSetup(1)	
0x1990	**bBlackCorrectionOffset**	
	Default value	0x00
	Purpose	Black Correction Offset which would be added to the sensor pedestal to get the RE Offset. This is to improve the black level.
	Type	BYTE

1. Can be controlled in all stable states

Image Stability [read only]

Table 26. Image stability [read only]

Index	Image stability [read only]	
0x1900	**fWhiteBalanceStable**	
	Default value	0x00
	Purpose	Specifies that white balance system is stable/unstable
	Type	CODED
	Possible values	<0> Unstable <1>Stable
0x1902	**fExposureStable**	
	Default value	0x00
	Purpose	Specifies that white balance system is stable/unstable
	Type	CODED
	Possible values	<0> Unstable <1>Stable

Table 26. Image stability [read only]

Index	Image stability [read only]	
0x1906	**fStable**	
	Default value	0x00
	Purpose	Consolidated flag to indicate whether the system is stable/unstable
	Type	CODED
	Possible values	<0> Unstable <1>Stable

Flash control

Table 27. Flash control

Index	FlashControl(1)	
0x1a80	**bFlashMode**	
	Default value	<0> FLASH_OFF
	Purpose	Select the flash type and on/off
	Type	CODED
	Possible values	<0> FLASH_OFF <1>FLASH_TORCH <2>FLASH_PULSE
0x1a83(MSB) 0x1a84(LSB)	**uwFlashOffLine**	
	Default value	0x021c (540)
	Purpose	At flash_pulse mode, used to control off line
	Type	UINT16

1. Can be controlled in all stable states

Flash status [read only]

Table 28. Flash status

Index	FlashStatus [read only]	
0x1b00	**fFlashRecommend**	
	Default value	<0> FALSE
	Purpose	This flag is set if the Exposure Control system reports that the image is underexposed and so the flashgun is recommended to the Host. It is at the discretion of Host to use it or not for the following still grab.
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x1b02	**fFlashGrabComplete**	
	Default value	<0> FALSE
	Purpose	This flag indicates that the FlashGun Image has been grabbed.
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE

Scythe filter controls

Table 29. Scythe filter controls

Index	ScytheFilterControls(1)	
0x1d80	**fDisableFilter**	
	Default value	<0> FALSE
	Purpose	Disable Scythe Defect Correction
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE

1. Can be controlled in all stable state

Jack filter controls

Table 30. Jack filter controls

Index	JackFilterControls(1)	
0x1e00	**fDisableFilter**	
	Default value	<0> FALSE
	Purpose	Disable Jack Defect Correction
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE

1. Can be controlled in all stable state

Demosaic control

Table 31. Demosaic control

Index	DemosaicControl(1)	
0x1e80	**bAntiAliasFilterSuppress**	
	Default value	0x08
	Purpose	Anti alias filter suppress
	Type	BYTE

1. Can be controlled in all stable state

Colour matrix dampers

Table 32. Colour matrix dampers

Index	ColourMatrixDamper(1)	
0x1f00	**fDisable**	
	Default value	<0> FALSE
	Purpose	set to disable colour matrix damper and therefore ensure that all the Colour matrix coefficients remain constant under all conditions.
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x1f03 (MSByte) 0x1f04 (LSByte)	**fpLowThreshold**	
	Default value	0x67d1 (2000896)
	Purpose	Low Threshold for exposure for calculating the damper slope
	Type	FLOAT
0x1f07 (MSByte) 0x1f08 (LSByte)	**fpHighThreshold**	
	Default value	0x6862 (2498560)
	Purpose	High Threshold for exposure for calculating the damper slope
	Type	FLOAT
0x1f0b (MSByte) 0x1f0c (LSByte)	**fpMinimumOutput**	
	Default value	0x3acd (0.350098)
	Purpose	Minimum possible damper output for the ColourMatrix
	Type	FLOAT

1. Can be controlled in all stable state

Peaking control

Table 33. Peaking control

Index	Peaking control(1)	
0x2000	**bUserPeakGain**	
	Default value	0x0e
	Purpose	controls peaking gain / sharpness applied to the image
	Type	BYTE
0x2002	**fDisableGainDamping**	
	Default value	<0> FALSE
	Purpose	set to disable damping and therefore ensure that the peaking gain applied remains constant under all conditions
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x2005 (MSByte) 0x2006 (LSByte)	**fpDamperLowThreshold_Gain**	
	Default value	0x62ac (350208)
	Purpose	Low Threshold for exposure for calculating the damper slope - for gain
	Type	FLOAT
0x2009 (MSByte) 0x200a (LSByte)	**fpDamperHighThreshold_Gain**	
	Default value	0x65d1 (10004488)
	Purpose	High Threshold for exposure for calculating the damper slope - for gain
	Type	FLOAT
0x200d (MSByte) 0x200e (LSByte)	**fpMinimumDamperOutput_Gain**	
	Default value	0x3d33 (0.799805)
	Purpose	Minimum possible damper output for the gain.
	Type	FLOAT
0x2010	**bUserPeakLoThresh**	
	Default value	0x1e
	Purpose	Adjust degree of coring. range: 0 - 63
	Type	BYTE
0x2012	**fDisableCoringDamping**	
	Default value	<0> FALSE
	Purpose	set to ensure that bUserPeakLoThresh is applied to gain block
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE

Table 33. Peaking control

Index	Peaking control[1]	
0x2014	**bUserPeakHiThresh**	
	Default value	0x30
	Purpose	adjust maximum gain that can be applied. range: 0 - 63
	Type	BYTE
0x2017 (MSByte) 0x2018 (LSByte)	**fpDamperLowThreshold_Coring**	
	Default value	0x624a (300032)
	Purpose	Low Threshold for exposure for calculating the damper slope - for coring
	Type	FLOAT
0x201b (MSByte) 0x201c (LSByte)	**fpDamperHighThreshold_Coring**	
	Default value	0x656f (900096)
	Purpose	High Threshold for exposure for calculating the damper slope - for coring
	Type	FLOAT
0x201f (MSByte) 0x2020 (LSByte)	**fpMinimumDamperOutput_Coring**	
	Default value	0x3a00 (0.2500)
	Purpose	Minimum possible damper output for the Coring.
	Type	FLOAT

1. Can be controlled in all stable states

Pipe 0 RGB to YUV matrix manual control

Table 34. Pipe0 RGB to YUV matrix manual control

Index	Pipe0RGB to YUV matrix (1)	
0x2180	**fRgbToYuvManuCtrl**	
	Default value	<0> FALSE
	Purpose	Enables manual RGB to YUV matrix for PipeSetupBank0
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x2183 (MSByte) 0x2184(LSByte)	**w0_0**	
	Default value	0x00
	Purpose	Row 0 Column 0 of YUV matrix
	Type	UINT_16
0x2187 (MSByte) 0x2188 (LSByte)	**w0_1**	
	Default value	0x00
	Purpose	Row 0 Column 1 of YUV matrix
	Type	UINT_16
0x218c (MSByte) 0x218d (LSByte)	**w0_2**	
	Default value	0x00
	Purpose	Row 0 Column 2 of YUV matrix
	Type	UINT_16
0x2190 (MSByte) 0x218f (LSByte)	**w1_0**	
	Default value	0x00
	Purpose	Row 1 Column 0 of YUV matrix
	Type	UINT_16
0x2193 (MSByte) 0x2194 (LSByte)	**w1_1**	
	Default value	0x00
	Purpose	Row 1 Column 1 of YUV matrix
	Type	UINT_16
0x2197 (MSByte) 0x2198 (LSByte)	**w1_2**	
	Default value	0x00
	Purpose	Row 1 Column 2 of YUV matrix
	Type	UINT_16

Table 34. Pipe0 RGB to YUV matrix manual control

Index	Pipe0RGB to YUV matrix (1)	
0x219b (MSByte) 0x219c (LSByte)	**w2_0**	
	Default value	0x00
	Purpose	Row 2 Column 0 of YUV matrix
	Type	UINT_16
0x21a0 (MSByte) 0x219f (LSByte)	**w2_1**	
	Default value	0x00
	Purpose	Row 2 Column 1 of YUV matrix
	Type	UINT_16
0x21a3 (MSByte) 0x21a4 (LSByte)	**w2_2**	
	Default value	0x00
	Purpose	Row 2 Column 2 of YUV matrix
	Type	UINT_16
0x21a7 (MSByte) 0x21a8 (LSByte)	**YinY**	
	Default value	0x00
	Purpose	Y in Y
	Type	UINT_16
0x21ab (MSByte) 0x21ac (LSByte)	**YinCb**	
	Default value	0x00
	Purpose	Y in Cb
	Type	UINT_16
0x21b0 (MSByte) 0x21af (LSByte)	**YinCr**	
	Default value	0x00
	Purpose	Y in Cr
	Type	UINT_16

1. Can be controlled in all stable states

Pipe 1 RGB to YUV matrix manual control

Table 35. Pipe1 RGB To YUV matrix manual control

Index	Pipe1RgbToYuv(1)	
0x2200	**fRgbToYuvManuCtrl**	
	Default value	<0> FALSE
	Purpose	Enables manual RGB to YUV matrix for PipeSetupBank1
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x2203 (MSByte) 0x2204(LSByte)	**w0_0**	
	Default value	0x00
	Purpose	Row 0 Column 0 of YUV matrix
	Type	UINT_16
0x2207 (MSByte) 0x2208 (LSByte)	**w0_1**	
	Default value	0x00
	Purpose	Row 0 Column 1 of YUV matrix
	Type	UINT_16
0x220c (MSByte) 0x220d (LSByte)	**w0_2**	
	Default value	0x00
	Purpose	Row 0 Column 2 of YUV matrix
	Type	UINT_16
0x2210 (MSByte) 0x220f (LSByte)	**w1_0**	
	Default value	0x00
	Purpose	Row 1 Column 0 of YUV matrix
	Type	UINT_16
0x2213 (MSByte) 0x2214 (LSByte)	**w1_1**	
	Default value	0x00
	Purpose	Row 1 Column 1 of YUV matrix
	Type	UINT_16
0x2217 (MSByte) 0x2218 (LSByte)	**w1_2**	
	Default value	0x00
	Purpose	Row 1 Column 2 of YUV matrix
	Type	UINT_16

Table 35. Pipe1 RGB To YUV matrix manual control

Index	Pipe1RgbToYuv(1)	
0x221b (MSByte) 0x221c (LSByte)	**w2_0**	
	Default value	0x00
	Purpose	Row 2 Column 0 of YUV matrix
	Type	UINT_16
0x2220 (MSByte) 0x221f (LSByte)	**w2_1**	
	Default value	0x00
	Purpose	Row 2 Column 1 of YUV matrix
	Type	UINT_16
0x2223 (MSByte) 0x2224 (LSByte)	**w2_2**	
	Default value	0x00
	Purpose	Row 2 Column 2 of YUV matrix
	Type	UINT_16
0x2227 (MSByte) 0x2228 (LSByte)	**YinY**	
	Default value	0x00
	Purpose	Y in Y
	Type	UINT_16
0x222b (MSByte) 0x222c (LSByte)	**YinCb**	
	Default value	0x00
	Purpose	Y in Cb
	Type	UINT_16
0x2220 (MSByte) 0x222f (LSByte)	**YinCr**	
	Default value	0x00
	Purpose	Y in Cr
	Type	UINT_16

1. Can be controlled in all stable states

Pipe 0 gamma manual control

Table 36. Pipe 0 gamma manual control

Index	Pipe0 GammaManuControl(1)	
0x2280	**fGammaManuCtrl**	
	Default value	<0> FALSE
	Purpose	Enables manual Gamma Setup for PipeSetupBank0
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x2282	**bRPeakGamma**	
	Default value	0x00
	Purpose	Peaked Red channel gamma value
	Type	BYTE
0x2284	**bGPeakGamma**	
	Default value	0x00
	Purpose	Peaked Green channel gamma value
	Type	BYTE
0x2286	**bBPeakGamma**	
	Default value	0x00
	Purpose	Peaked Blue channel gamma value
	Type	BYTE
0x2288	**bRUnPeakGamma**	
	Default value	0x00
	Purpose	Unpeaked Red channel gamma value
	Type	BYTE
0x228a	**bGUnPeakGamma**	
	Default value	0x00
	Purpose	Unpeaked Green channel gamma value
	Type	BYTE
0x228c	**bBUnPeakGamma**	
	Default value	0x00
	Purpose	Unpeaked Blue channel gamma value
	Type	BYTE

1. Can be controlled in all stable states

Pipe 1 Gamma manual control

Table 37. Pipe 1 Gamma manual control

Index	Pipe1GammaManuControl(1)	
0x2300	**fGammaManuCtrl**	
	Default value	<0> FALSE
	Purpose	Enables manual Gamma Setup for PipeSetupBank1
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x2302	**bRPeakGamma**	
	Default value	0x00
	Purpose	Peaked Red channel gamma value
	Type	BYTE
0x2304	**bGPeakGamma**	
	Default value	0x00
	Purpose	Peaked Green channel gamma value
	Type	BYTE
0x2306	**bBPeakGamma**	
	Default value	0x00
	Purpose	Peaked Blue channel gamma value
	Type	BYTE
0x2308	**bRUnPeakGamma**	
	Default value	0x00
	Purpose	Unpeaked Red channel gamma value
	Type	BYTE
0x230a	**bGUnPeakGamma**	
	Default value	0x00
	Purpose	Unpeaked Green channel gamma value
	Type	BYTE
0x230c	**bBUnPeakGamma**	
	Default value	0x00
	Purpose	Unpeaked Blue channel gamma value
	Type	BYTE

1. Can be controlled in all stable states

Fade to black

Table 38. Fade to black

Index	FadeToBlack[1]	
0x2480	**fDisable**	
	Default value	<0> FALSE
	Purpose	Flag_e
	Type	<0> FALSE <1> TRUE
0x2483 (MSByte) 0x2484(LSByte)	**fpBlackValue**	
	Default value	0x0000 (0.000)
	Purpose	Black value
	Type	FLOAT
0x2487 (MSByte) 0x2488 (LSByte)	**fpDamperLowThreshold**	
	Default value	0x6d56 (6995968)
	Purpose	Low Threshold for exposure for calculating the damper slope
	Type	FLOAT
0x248b (MSByte) 0x248c (LSByte)	**fpDamperHighThreshold**	
	Default value	0x6cdc (11993088)
	Purpose	High Threshold for exposure for calculating the damper slope
	Type	FLOAT
0x248f (MSByte) 0x2490 (LSByte)	**fpDamperOutput**	
	Default value	0x0 (0.0000)
	Purpose	Minimum possible damper output.
	Type	FLOAT

1. Can be controlled in all stable states

Output formatter control

Table 39. Output formatter control

Index	OutputFormatterControl(1)	
0x2580	**bCodeCheckEn**	
	Default value	0x07
	Type	BYTE
0x2582	**bBlankFormat**	
	Default value	0x00
	Type	BYTE
0x2584	**bSyncCodeSetup**	
	Default value	0x01
	Type	CODED
	flag bits	[0] SyncCodeSetup_ins_code_en - set for embedded sync codes. [1] SyncCodeSetup_frame_mode - 0 for ITU. 1 for mode2 [2] SyncCodeSetup_field_bit [3] SyncCodeSetup_field_tag [4] SyncCodeSetup_field_load
0x2586	**bHSyncSetup**	
	Default value	0x0b
	Type	CODED
	flag bits	[0] HSyncSetup_sync_en [1] HSyncSetup_sync_pol [2] HSyncSetup_only_activelines [3] HSyncSetup_track_henv
0x2588	**bVSyncSetup**	
	Default value	0x07
	Type	CODED
	flag bits	[0] VSyncSetup_sync_en [1] VSyncSetup_pol [2] VSyncSetup_2_sel

Table 39. Output formatter control

Index	OutputFormatterControl(1)	
0x258a	**bPClkSetup**	
	Default value	0x05
	Type	CODED
	flag bits	[0] PClkSetup_prog_lo [1] PClkSetup_prog_hi [2] PClkSetup_sync_en [3] PClkSetup_hsync_en_n [4] PClkSetup_hsync_en_n_track_internal [5] PClkSetup_vsync_n [6] PClkSetup_vsync_n_track_internal [7] PClkSetup_freer
0x258c	**fPclkEn**	
	Default value	<1> TRUE
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x258e	**bOpfSpSetup**	
	Default value	0x00
	type	BYTE
0x2590	**bBlankData_MSB**	
	Default value	0x10
	Type	CODED
	Possible values	<16> BlankingMSB_Default
0x2592	**bBlankData_LSB**	
	Default value	0x80
	Type	CODED
	Possible values	<128> BlankingLSB_Default
0x2594	**bRgbSetup**	
	Default value	0x00
	Type	CODED
	flag bits	[0] RgbSetup_rgb444_itu_zp [1] RgbSetup_rb_swap [2] RgbSetup_bit_reverse [3] RgbSetup_softreset

Table 39. Output formatter control

Index	OutputFormatterControl(1)	
0x2596	**bYuvSetup**	
	Default value	0x00
	Type	CODED
	flag bits	[0] YuvSetup_u_first [1] YuvSetup_y_first
0x2598	**bVsyncRisingCoarseH**	
	Default value	0x00
	Type	BYTE
0x259a	**bVsyncRisingCoarseL**	
	Default value	0x00
	Type	BYTE
0x259c	**bVsyncRisingFineH**	
	Default value	0x00
	Type	BYTE
0x259e	**bVsyncRisingFineL**	
	Default value	0x01
	Type	BYTE
0x25a0	**bVsyncFallingCoarseH**	
	Default value	0x01
	Type	BYTE
0x25a2	**bVsyncFallingCoarseL**	
	Default value	0xf2
	Type	BYTE
0x25a4	**bVsyncFallingFineH**	
	Default value	0x00
	Type	BYTE
0x25a6	**bVsyncFallingFineL**	
	Default value	0x01
	Type	BYTE
0x25a8	**bHsyncRisingH**	
	Default value	0x00
	Type	BYTE

Table 39. Output formatter control

Index	OutputFormatterControl[1]	
0x25aa	**bHsyncRisingL**	
	Default value	0x03
	Type	BYTE
0x25ac	**bHsyncFallingH**	
	Default value	0x00
	Type	BYTE
0x25ae	**bHsyncFallingL**	
	Default value	0x07
	type	BYTE
0x25b0	**bOutputInterface**	
	Default value	[0] OutputInterface_ITU
	Type	CODED
	flag bits	[0] OutputInterface_ITU [1] OutputInterface_CCP_DataStrobe [2] OutputInterface_CCP_DataClock
0x25b2	**bCCPExtraData**	
	Default value	0x08
	Type	BYTE

1. Can be controlled in all stable states

NoRA controls

Table 40. NoRA controls

Index	NoRAControls(1)	
0x2600	**fDisable**	
	Default value	<0> NoraCtrl_auto
	Type	Flag_e
	Possible values	<0> NoraCtrl_auto - switches off NoRA for scaled outputs <1> NoraCtrl_ManuDisable - Always off <2> NoraCtrl_ManuEnable - Always on
0x2602	**bUsage**	
	Default value	0x04
	Purpose	
	Type	BYTE
0x2604	**bSplit_Kn**	
	Default value	0x01
	Purpose	
	Type	BYTE
0x2606	**bSplit_NI**	
	Default value	0x01
	Purpose	
	Type	BYTE
0x2608	**bTight_Green**	
	Default value	0x01
	Purpose	
	Type	BYTE
0x260a	**fDisableNoroPromoting**	
	Default value	<0> FALSE
	Type	Flag_e
	Possible values	<0> FALSE <1> TRUE
0x260d (MSByte) 0x260e (LSByte)	**fpDamperLowThreshold**	
	Default value	0x6862 (2498560)
	Purpose	Low Threshold for exposure for calculating the damper slope
	Type	FLOAT

Table 40. NoRA controls

Index	NoRAControls[1]	
0x2611 (MSByte) 0x2612 (LSByte)	**fpDamperHighThreshold**	
	Default value	0x6a62 (4997120)
	Purpose	High Threshold for exposure for calculating the damper slope
	Type	FLOAT
0x2615 (MSByte) 0x2616 (LSByte)	**MinimumDamperOutput**	
	Default value	0x3a00 (0.2500)
	Purpose	Minimum possible damper output.
	Type	FLOAT

1. Can be controlled in all stable states

12 Optical specifications

Table 41. Optical specifications(1)

Parameter	Min.	Typ.	Max.	Unit
Optical format		1/5		inch
Effective focal length				mm
Aperture (F number)		3.2		
Horizontal field of view		52		deg.
Depth of field	60		infinity	cm
TV distortion			1	%

1. All measurements made at 23°C ± 2°C

13 Electrical characteristics

13.1 Absolute maximum ratings

Table 42. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STO}	Storage temperature	-40	85	°C
V_{DD}	Digital power supplies	-0.5	3.3	V
AVDD	Analog power supplies	-0.5	3.3	V

Caution: Stress above those listed under “Absolute Maximum Ratings” can cause permanent damage to the device. This is a stress rating only and functional operations of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

13.2 Operating conditions

Table 43. Supply specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{AF}	Operating temperature, functional (Camera is electrically functional)	-30	25	70	°C
T_{AN}	Operating temperature, nominal (Camera produces acceptable images)	-25	25	55	°C
T_{AO}	Operating temperature, optimal (Camera produces optimal optical performance)	5	25	30	°C
V_{DD}	Digital power supplies operating range (@ module pin(1))	1.7	1.8	2.0	V
		2.4	2.8	3.0	V
AVDD	Analog power supplies operating range (@ module pin(1))	2.4	2.8	3.0	V

1. Module can contain routing resistance up to 5 Ω

13.3 DC electrical characteristics

Note: Over operating conditions unless otherwise specified.

Table 44. DC electrical characteristics

Symbol	Description	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage		-0.3		0.3 V_{DD}	V
V_{IH}	Input high voltage		0.7 V_{DD}		V_{DD} + 0.3	V
V_{OL}	Output low voltage	I_{OL} < 2 mA I_{OL} < 4 mA			0.2 V_{DD} 0.4 V_{DD}	V
V_{OH}	Output high voltage	I_{OH}< 4 mA	0.8 V_{DD}			V
I_{IL}	Input leakage current Input pins I/O pins	0 < V_{IN} < V_{DD}			 +/- 10 +/- 1	 µA µA
C_{IN}	Input capacitance, SCL	T_A = 25 °C, freq = 1 MHz			6	pF
C_{OUT}	Output capacitance	T_A = 25 °C, freq = 1 MHz			6	pF
$C_{I/O}$	I/O capacitance, SDA	T_A = 25 °C, freq = 1 MHz			8	pF

Table 45. Typical current consumption - Sensor mode VGA 30 fps

Symbol	Description	Test conditions	I_{AVDD}	I_{VDD}		Units
			V_{DD} = 2.8V	V_{DD} = 1.8V	V_{DD} = 2.8V	
I_{PD}	supply current in power down mode	CE=0, CLK = 12 MHz	1.4	0.05	0.07	µA
I_{stanby}	supply current in Standby mode	CE=1, CLK = 12 MHz	0.0014	1.3	8	mA
I_{Stop}	supply current in Stop mode	CE=1, CLK = 12 MHz	0.0014	4.1	4.2	mA
I_{Pause}	supply current in Pause mode	CE=1, CLK = 12 MHz	0.00175	43.8	43.3	mA
I_{run}	supply current in active streaming run mode	CE=1, CLK = 12 MHz streaming VGA @30 fps	11.3	55.1	54.8	mA

Table 46. Typical current consumption - Sensor mode SXGA 15 fps

Symbol	Description	Test conditions	I_{AVDD}	I_{VDD}		Units
			V_{DD} = 2.8V	V_{DD} = 1.8V	V_{DD} = 2.8V	
I_{PD}	supply current in power down mode	CE=0, CLK = 12 MHz	1.4	0.05	0.07	µA
I_{stanby}	supply current in Standby mode	CE=1, CLK = 12 MHz	0.0014	1.3	8	mA
I_{Stop}	supply current in Stop mode	CE=1, CLK = 12 MHz	0.0014	4.1	4	mA
I_{Pause}	supply current in Pause mode	CE=1, CLK = 12 MHz	0.0195	63.4	64.7	mA
I_{run}	supply current in active streaming run mode	CE=1, CLK = 12 MHz streaming VGA @30 fps	11.5	84.5	87	mA

13.4 External clock

The VS6624 requires an external clock. This clock is a CMOS digital input. The clock input is fail-safe in power down mode.

Table 47. External clock

CLK	Range			Unit
	Min.	Typ.	Max.	
DC coupled square wave		VDD		V
Clock frequency (normal operation)	6.50	6.50, 8.40, 9.60, 9.72, 12.00, 13.00, 16.80, 19.20, 19.44	54	MHz

13.5 Chip enable

CE is a CMOS digital input. The module is powered down when a logic 0 is applied to CE. See *Power up sequence* for further information.

13.6 I²C slave interface

VS6624 contains an I²C-type interface using two signals: a bidirectional serial data line (SDA) and an input-only serial clock line (SCL). See *Host communication - I²C control interface* for detailed description of protocol.

Table 48. Serial interface voltage levels(1)

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
V_{HYS}	Hysteresis of Schmitt Trigger Inputs V_{DD} > 2 V V_{DD} < 2V	 N/A N/A	 N/A N/A	 0.05 V_{DD} 0.1 V_{DD}	 - -	 V V
V_{OL1} V_{OL3}	LOW level output voltage (open drain) at 3mA sink current V_{DD} > 2 V V_{DD} < 2V	 0 N/A	 0.4 N/A	 0 0	 0.4 0.2 V_{DD}	 V V
V_{OH}	HIGH level output voltage	N/A	N/A	0.8 V_{DD}		V
t_{OF}	Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10 pF to 400 pF	-	250	20+0.1C_b(2)	250	ns
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	N/A	N/A	0	50	ns

1. Maximum $V_{IH} = V_{DDmax}$ + 0.5 V
2. C_b = capacitance of one bus line in pF

Figure 32. Voltage level specification

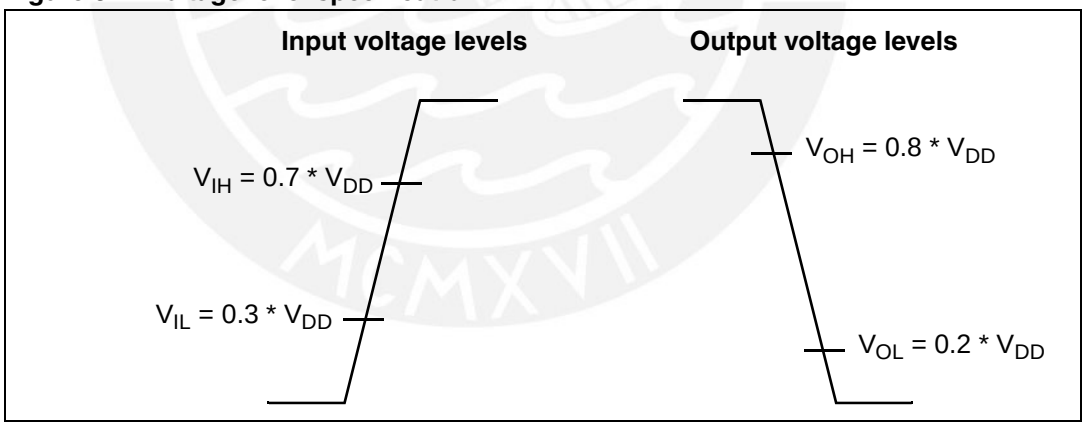


Table 49. Timing specification(1)

Symbol	Parameter	Standard mode		Fast mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	Hold time for a repeated ***start***	4.0	-	0.6	-	µs
t_{LOW}	LOW period of SCL	4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of SCL	4.0	-	0.6	-	µs
$t_{SU;STA}$	Set-up time for a repeated ***start***	4.7	-	0.6	-	µs
$t_{HD;DAT}$	Data hold time (1)	300	-	300	-	ns
$t_{SU;DAT}$	Data Set-up time (1)	250	-	100	-	ns
t_r	Rise time of SCL, SDA	-	1000	$20+0.1C_b$(2)	300	ns
t_f	Fall time of SCL, SDA	-	300	$20+0.1C_b$(2)	300	ns
$t_{SU;STO}$	Set-up time for a ***stop***	4.0	-	0.6	-	µs
t_{BUF}	Bus free time between a ***stop*** and a ***start***	4.7	-	1.3	-	µs
C_b	Capacitive Load for each bus line	-	400	-	400	pF
V_{nL}	Noise Margin at the LOW level for each connected device (including hysteresis)	0.1 V_{DD}	-	0.1 V_{DD}	-	V
V_{nH}	Noise Margin at the HIGH level for each connected device (including hysteresis)	0.2 V_{DD}	-	0.2 V_{DD}	-	V

1. All values are referred to a V_{IHmin} = 0.9 V_{DD} and V_{ILmax} = 0.1 V_{DD}
2. C_b = capacitance of one bus line in pF

Figure 33. Timing specification

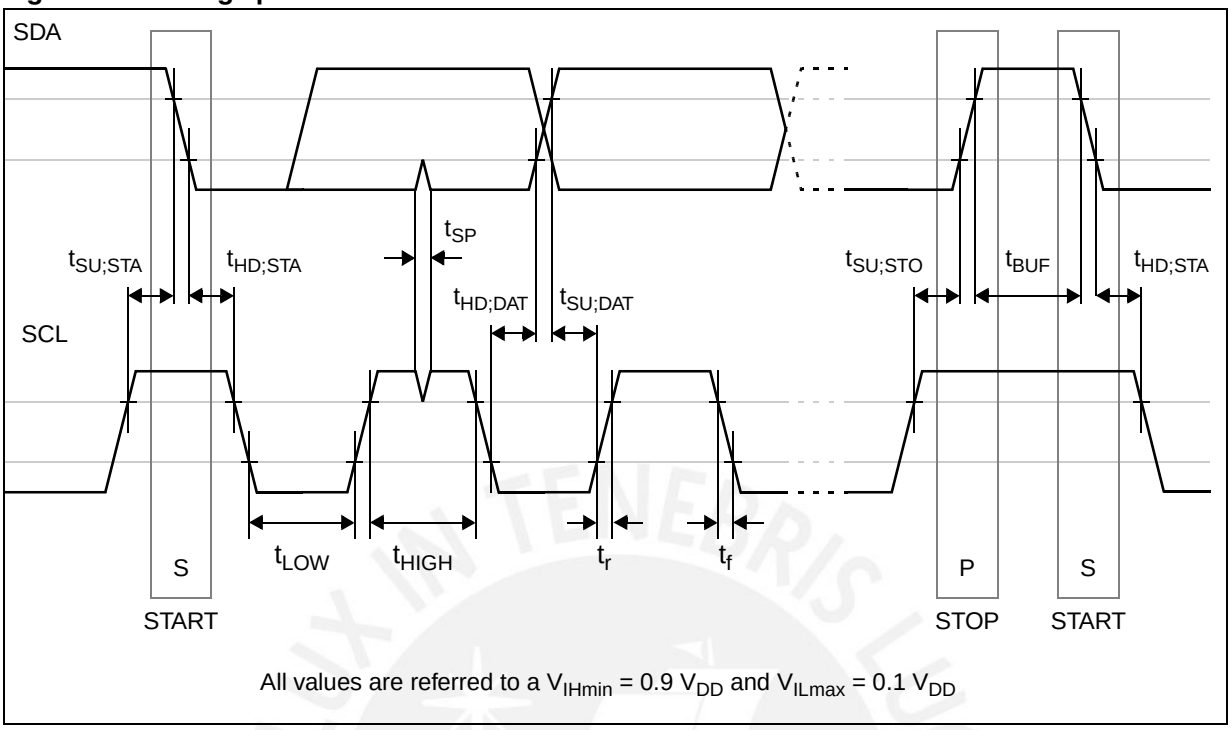
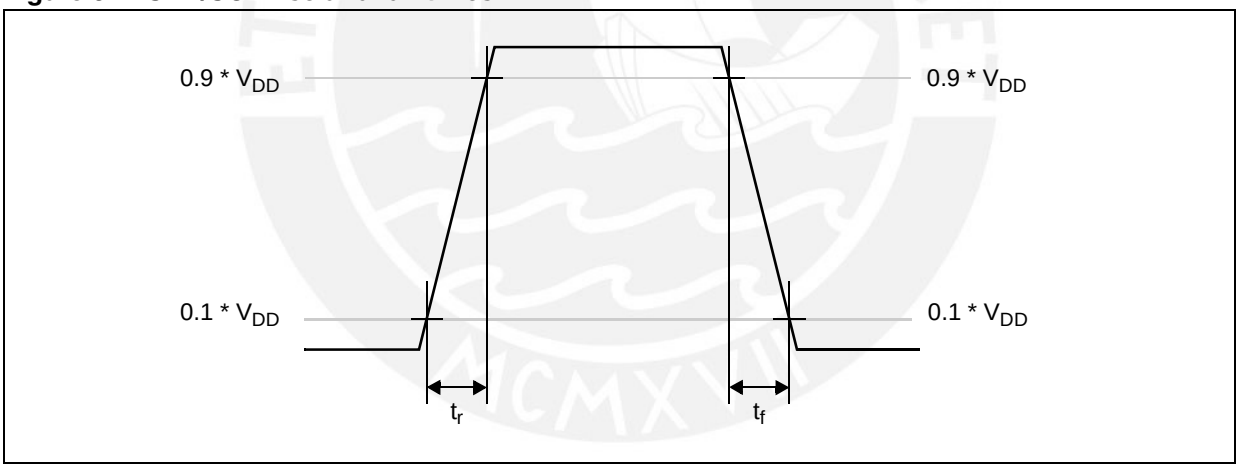


Figure 34. SDA/SCL rise and fall times



13.7 Parallel data interface timing

VS6624 contains a parallel data output port (D[7:0]) and associated qualification signals (HSYNC, VSYNC, PCLK and FSO).

This port can be enabled and disabled (tri-stated) to facilitate multiple camera systems or bit-serial output configurations. The port is disabled (high impedance) upon reset.

Figure 35. Parallel data output video timing

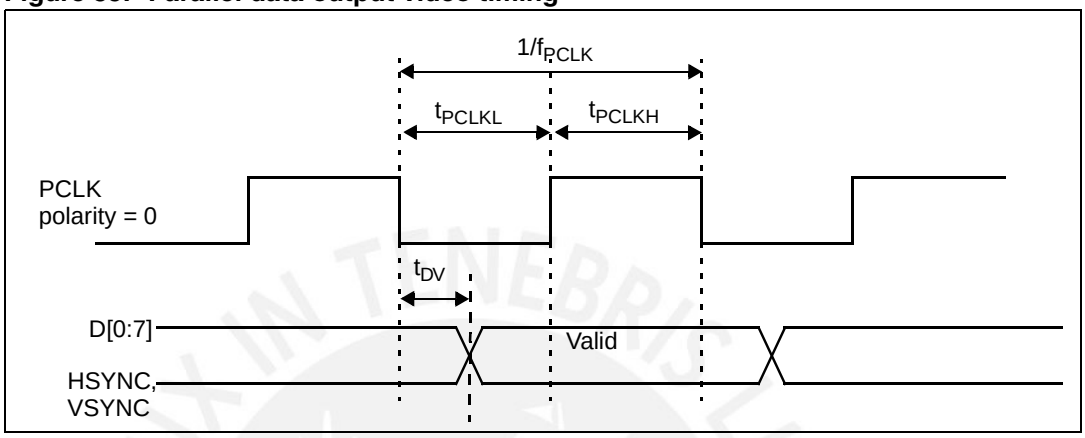


Table 50. Parallel data interface timings

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
f_{PCLK}	PCLK frequency				54	MHz
t_{PCLKL}	PCLK low width					ns
t_{PCLKH}	PCLK high width					ns
t_{DV}	PCLK to output valid					ns

14 Package mechanical data

Figure 36 and *Figure 37* present the package outline socket module VS6624Q0KP.

Figure 38 and *Figure 39* present the package outline FPC module VS6624P0LP.

Figure 36. Package outline socket module VS6624Q0KP

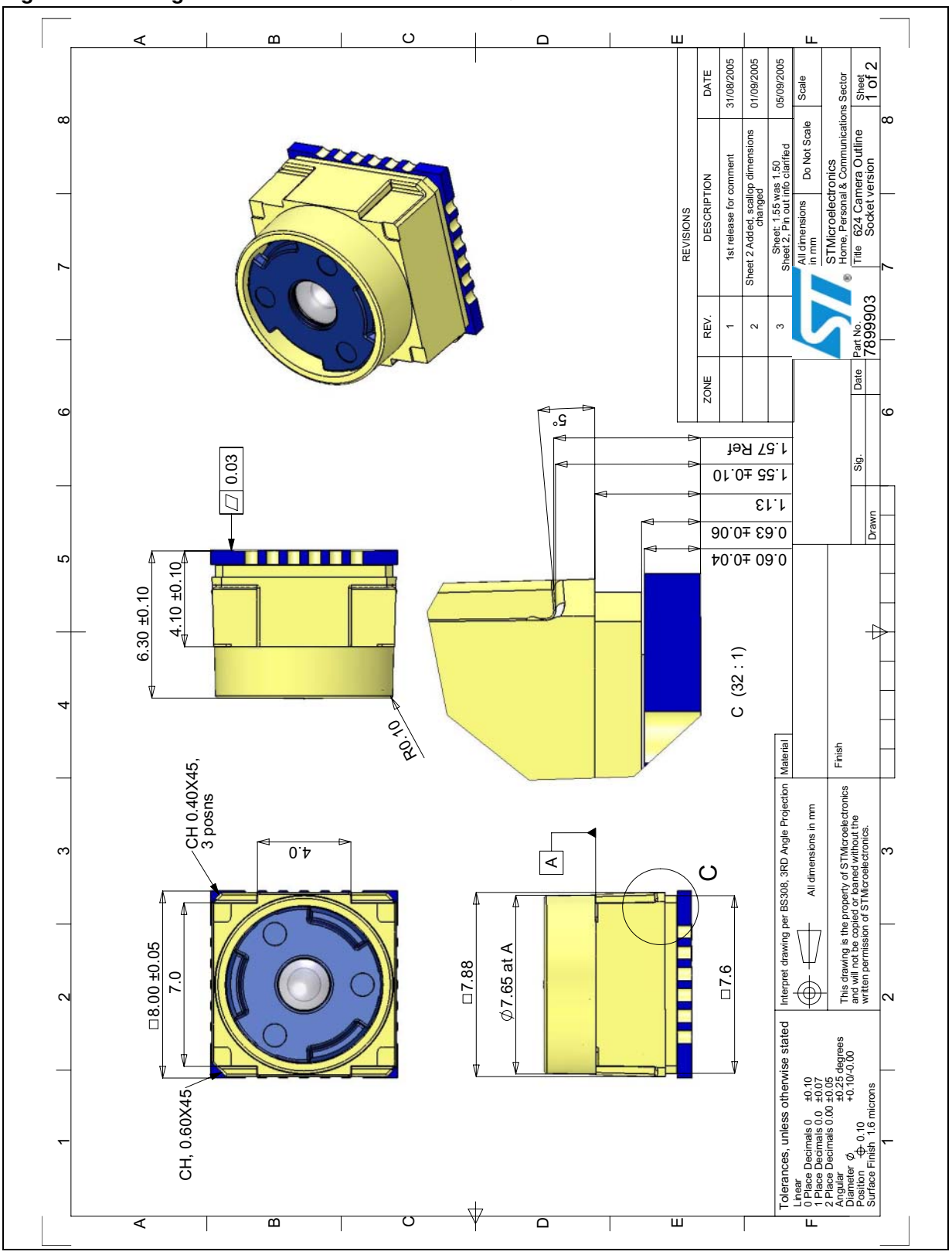


Figure 37. Package outline socket module VS6624Q0KP

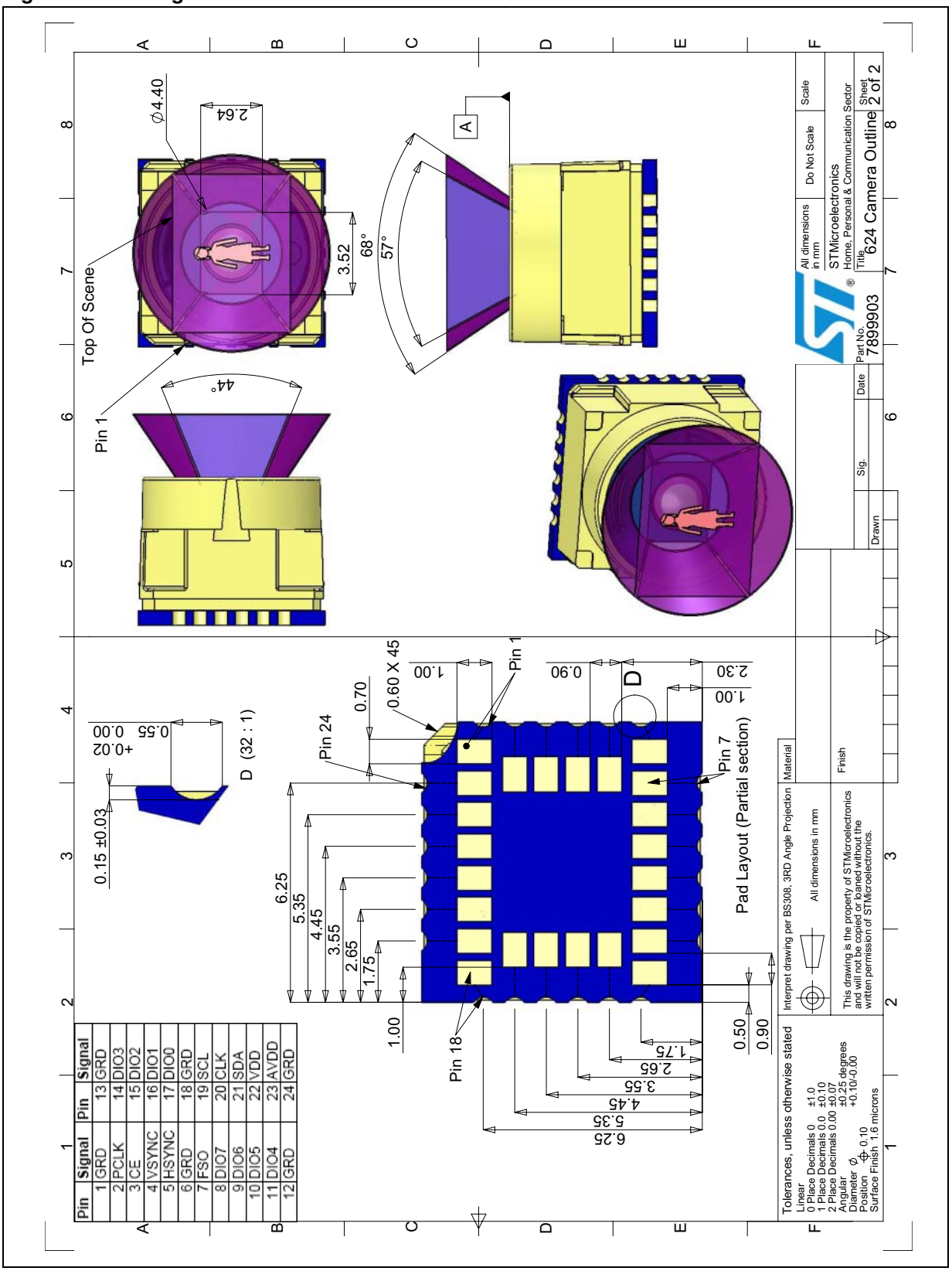


Figure 38. Package outline FPC module VS6624P0LP

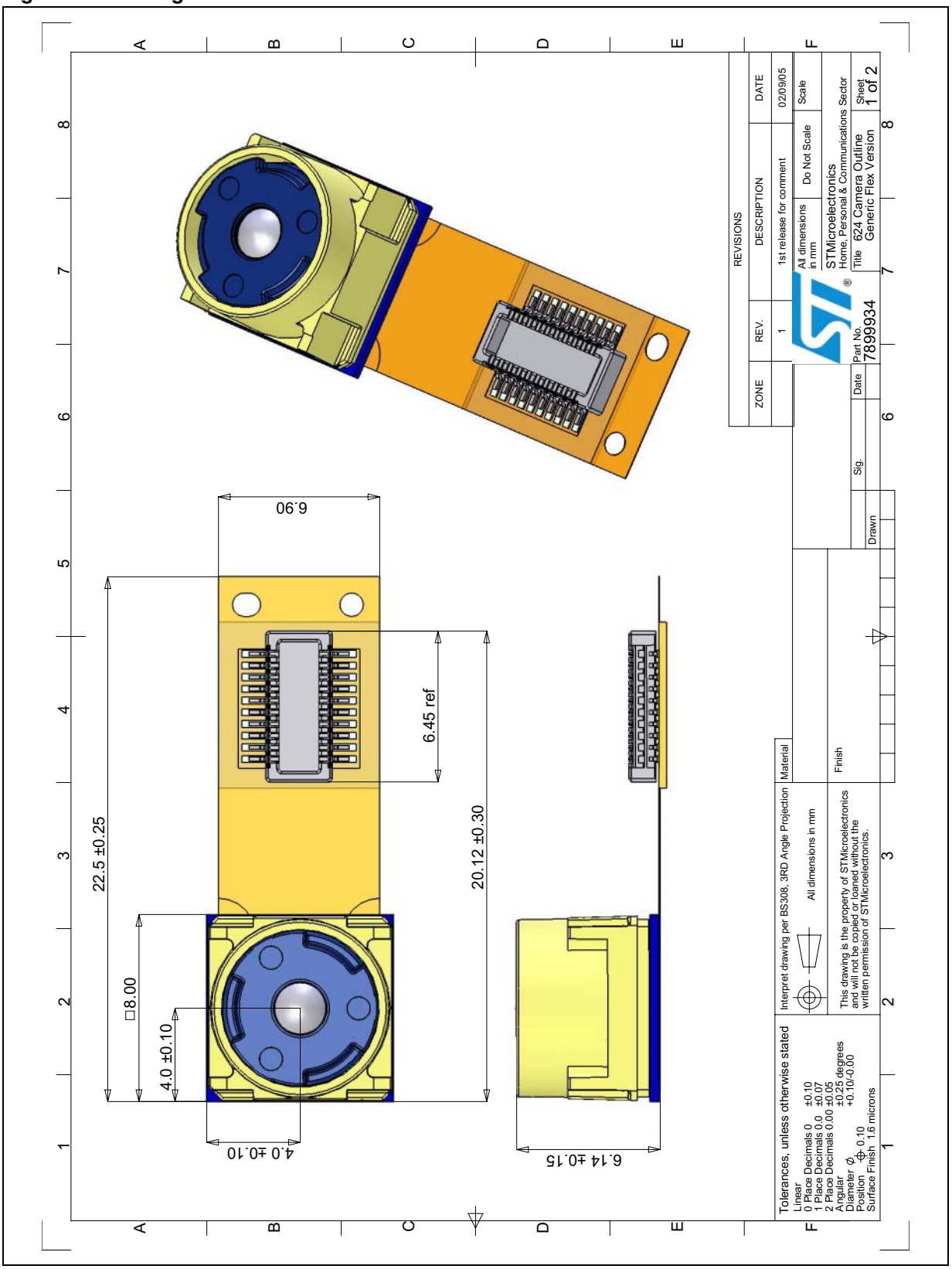
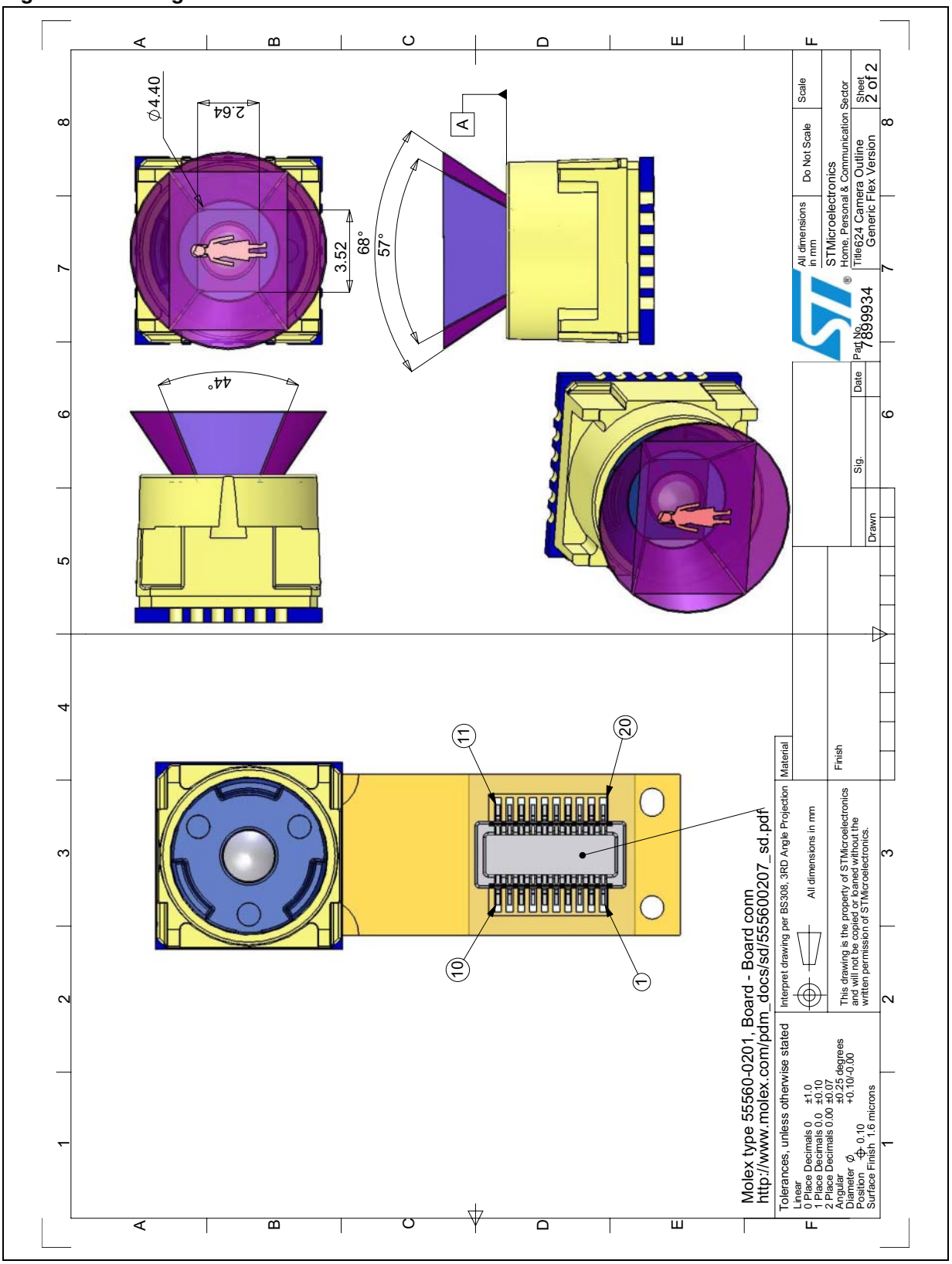


Figure 39. Package outline FPC module VS6624P0LP



15 Revision history

Table 51. Document revision history

Date	Revision	Changes
1-Feb-2006	1	Initial release.

Industrial Grade
Secure Digital Cards

W7SDxxxx1XA-H60Px Series

INFORMATION IN THIS DOCUMENT IS PROVIDED IN RELATION TO WINTEC INDUSTRIES PRODUCTS, AND IS SUBJECT TO CHANGE WITHOUT NOTICE.

NOTHING IN THIS DOCUMENT SHALL BE CONTRUED AS GRANTING ANY LICENSE, EXPRESS OR IMPLIED.

ALL INFORMATION IN THIS DOCUMENT IS PROVIDED ON AN "AS-IS" BASIS WITHOUT GUARANTEE OR WARRANTY OF ANY KIND.

- Please contact your nearest Wintec representative for the latest updates or additional product information.

Revision History

Revision	Month	Year	History
1.0	January	2009	-Preliminary Release
1.1	February	2010	-Updated Ordering Guide

Secure Digital Card

W7SDxxxx1XA-H60Px ROHS Compliant

Features

GENERAL

- Density up to 8GB
- 32-bit RISC/DSP Controller
- Solid State Data Storage
- Dual 3.3V / 1.8V Interface
- Industry Standard Compatibility
- ROHS Compliant

Wintec Secure Digital Card

PERFORMANCE

- High Performance 24 MB/s (Sustained Read)
- High Performance 23 MB/s (Sustained Write)
- Dual Channel operation
- Low Power Consumption

RELIABILITY

- > 2,000,000 Program/Erase Cycles
- Industrial Wear Leveling
  - Includes Static Block Management
- Spares & Bad Block Management
- On-chip ECC and CRC16 unit for flash data protection
- Hardware support for CPRM

COMPATIBILITY

- SD standard, rev. 1.01 /1.10 / 2.0

Description

The Wintec Industries W7SDxxxxx1XA-H60Px series of ROHS Compliant Secure Digital Cards are constructed with Samsung NAND-type single-level-cell (SLC) flash memory devices paired to a powerful 32-bit RISC/DSP-based system controller for virtual-to-physical address mapping and other flash management functions.

Wintec Secure Digital Cards employ a variety of sophisticated error checking and flash management utilities allowing for maximum levels of data reliability and card endurance. Patented wear-leveling methods ensure even wear of flash blocks across the entire card capacity. Background operations track erase counts, prioritize new writes to blocks with lower wear, and relocate static data to blocks with higher wear. Bad-block Management routines replace worn

blocks with spare blocks reserved by the controller on card initialization. Reed-Solomon based ECC algorithms capable of correcting 4 bytes in a 512 byte sector are implemented on the fly without performance degradation to ensure data reliability through user data transfers and background wear-leveling operations. Additional information regarding the specifics of wear leveling, ECC methods, and application-specific card life calculations are available upon request and under NDA.

1.0 General Product Specification

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

Table 1: Performance Specifications

Parameter		Spec
Burst Transfer Rate To/From Host: Read		24 MB/s
Write		23 MB/s
Burst Transfer Rate To/From Flash		40.0 MB/s per channel
Active-to-Sleep Delay after processing the last command		0 s
Startup Times	**Sleep-to-Write (Max.)**	No Delay
	Sleep-to-Read (Max.)	No Delay
	Reset-to-Ready (Typical)	100.0 ms
	Reset-to-Ready (Max.)	500.0 ms

Table 2: Card Endurance

Parameter	Spec
Program/Erase Cycles	> 2,000,000 Cycles
Read Cycles	Unlimited
Data Retention	10 Years (Min.)

Table 3: Card Data Reliability

Parameter	Spec
Non-Recoverable Errors	< 1 in 10^{20} Bytes Read
Erroneous Correction	< 1 in 10^{20} Bytes Read
ECC Correctability	4 Random Bytes/Sector

Table 4: Environmental Specifications

Parameters	Operating	Non-Operating
Temperature (Commercial Temp)	0°C to 70°C	-40°C to 125°C
Temperature (Extended Temp)	-25°C to 85°C	-40°C to 125°C
Relative Humidity	25% to 95% (Non-Condensing)	40% to 93% (Non-Condensing)
Vibration	15 G rms	15 G rms
Altitude	80,000 ft. (Max.)	N/A
Shock	1,000 G (Max.)	1,000 G (Max.)
Acoustic	0 db	N/A

NOTE:
1. Input voltage 3.3V (±5%) or 1.8V (±10%) with a maximum ripple of 100mV peak-to-peak.
2. All values listed are at 25°C and nominal supply voltage.
3. Stated figures are based on primary configurations and may vary as larger density component NAND flashes are released.

2.0 Architecture

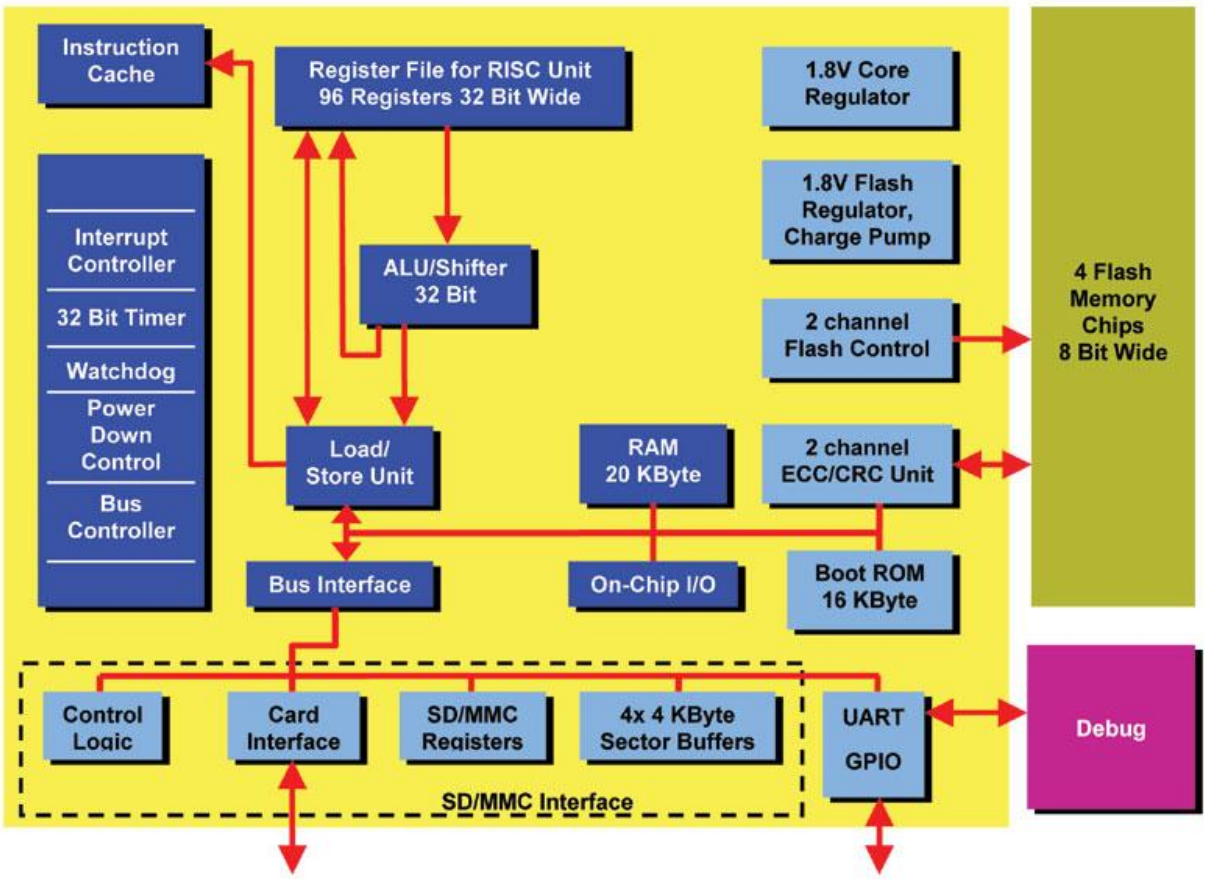


Figure 1: Card Block Diagram

Table 5: Card Pin Assignment

PIN NO	NAME	TYPE	DESCRIPTION
1	CD/DAT	I/O/PP3	Card Detect/Data Line [Bit3]
2	CMD	PP	Command / Response
3	VSS1	S	Supply voltage ground
4	VDD	S	Supply voltage
5	CLK	I	Clock
6	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit0]
8	DAT1	I/O/PP	Data Line [Bit1]
9	DAT2	I/O/PP	Data Line [Bit2]

1) S : power supply ; I : input ; O : output ; PP : push-pull ; OD : open-drain NC : Not connected (or logical high)
2) The DAT line for read - when card is in output mode only

3.0 Ordering Information

Table 6: Product Availability List & Naming

Card Capacity	Part Number
128 MB	W7SD128M1XA(I)-H60PC-002.01
256 MB	W7SD256M1XA(I)-H60PB-002.01
512 MB	W7SD512M1XA(I)-H60PB-002.01
1 GB	W7SD001G1XA(I)-H60PB-002.01
2 GB	W7SD002G1XA(I)-H60PB-02D.01
4 GB	W7SD004GHXA(I)-H60PB-2Q2.01
8 GB	W7SD008GHXA(I)-H60PB-2Q2.01

Contact Us (US & Int'l)

Wintec Industries OEM Sales
675 Sycamore Drive,
Milpitas, CA 95035
Ph: 408-856-0500
Fx: 408-856-0518

oemsales@wintecind.com
http://www.wintecind.com/oem

About Wintec Industries, Inc.

Wintec, founded in 1988, is headquartered in Milpitas, California. Wintec, a leading third party memory module manufacturer, specializes in a variety of module design and manufacturing, such as memory module, flash module, Handspring module, modem module, game module, etc. Besides a complete line of DDR, SDR, and EDO/FPM legacy memory modules, Wintec also distribute CPU, motherboard, peripherals, PC software, and consumer Flash products (such as MMC, SD, SMC, CompactFlash, PC Card, etc.). With excellent design engineering and manufacturing capability, Wintec provides a wide range of design and manufacturing services for our valuable customers from concept design to final product delivery. Wintec is ISO9001-2000 certified.

Important Notice