TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

```
clear all;
close all;
clc;

%Lectura de la señal de banda base
[Y,FS,NBITS] = wavread('muestreo_exterior');
%[Y,FS,NBITS] = wavread('muestreo_interior');

%Constantes
c = 3E8; %velocidad de la luz
Tp = 20E-3; %tiempo de pulso o medio periodo de moduación
N = Tp*FS; %numero de muestreas por tiempo de pulso
fstart = 2315E6; %frecuencia mínima
fstop = 2615E6; %frecuencia máxima
BW = fstop-fstart; %ancho de banda
f = linspace(fstart, fstop, N/2); %grupo de frecuencias

%Resolución de rango
rr = c/(2*BW);
%Máximo rango teórico
max_range = rr*N/2;

%Acondicionamiento
trig = -1*Y(:,2);
s = -1*Y(:,1);

%Selección de grupos de muestreo
count = 0;
thresh = 0;
start = (trig > thresh);
for ii = 100:(size(start,1)-N)
    if start(ii) == 1 & mean(start(ii-11:ii-1)) == 0
        count = count + 1;
        sif(count,:) = s(ii:ii+N-1);
        time(count) = ii*1/FS;
    end
end

zpad = 8*N/2;

%Gráfica de distancia sin rechazo de clutter
figure(30);
v = dbv(fft(sif,zpad,2));
S = v(:,1:size(v,2)/2);
m = max(max(v));
imagesc(linspace(0,max_range,zpad),time,S-m,[-80, 0]);
colorbar;
ylabel('time (s)');
xlabel('range (m)');
title('RTI without clutter rejection');

%Gráfica de distancia con rechazo de clutter
figure(40);
sif2 = sif(2:size(sif,1),:)-sif(1:size(sif,1)-1,:);
```

Tesis publicada con autorización del autor
No olvide citar esta tesis

```
v = fft(sif2,zpad,2);
S=v;
R = linspace(0,max_range,zpad);
S = dbv(S(:,1:size(v,2)/2));
m = max(max(S));
imagesc(R,time,S-m,[-80, 0]);
colorbar;
ylabel('time (s)');
xlabel('range (m)');
title('RTI with 2-pulse cancelor clutter rejection');
```

Tesis publicada con autorización del autor
No olvide citar esta tesis

```
clear all;
close all;
clc;

%Lecturas de la señal de banda baser
[Y,FS,NBITS] = wavread('velocidad_10.wav');
%[Y,FS,NBITS] = wavread('velocidad_20.wav');
%[Y,FS,NBITS] = wavread('velocidad_30.wav');

%Constantes
c = 3E8; %velocidad de la luz
Tp = 0.125; %tiempo de pulso
N = Tp*FS; %número de muestrar por tiempo de pulso
fc=26311E6; %frecuencia de salida del VCO a 5v

%Acondicionamiento de la señal
s = -1*Y(:,1);

%Creación de grupos
for ii = 1:round(size(s,1)/N)-1
    sif(ii,:) = s(1+(ii-1)*N:ii*N);
end

%Restar el promedio DC
sif = sif - mean(s);
zpad = 8*N/2;

%Grádica velocidad versus tiempo
v1=fft(sif,zpad,2);
v = dbv(v1);
v = v(:,1:size(v,2)/2);
mmax = max(max(v));
delta_f = linspace(0, 22100, size(v,2)); %
lambda=c/fc;
velocity = (delta_f*lambda/2)*(18/5)*11.88;% 11.88 término de calibración
time = linspace(1,Tp*size(v,1),size(v,1)); %
figure(2);
imagesc(velocity,time,v-mmax,[-35, 0]);
colorbar;
xlim([0 100]);
xlabel('Velocity (km/h)');
ylabel('time (sec)');
```

Tesis publicada con autorización del autor
No olvide citar esta tesis

Vendor P/N is CX20671-21Z , Page. 10
Pin Define : Page. 18
Dimension : Page. 42

CX20671

Low-Power Codec SoC with Integrated Class-D Stereo Amplifier for High Definition Audio

Data Sheet

DSH-202291p1
July 2010

CONEXANT

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

Revision History

Revision	Date	Description
A	February 19, 2010	Initial release
B	March 11, 2010	Revision B release
C	March 29, 2010	Revision C release
D	May 25, 2010	Revision D release *Changed all occurrences of Ns to ns (representing nanoseconds) in Tables 17-19. *Removed "Audio only" from Table 21. *Added SPDIF Out feature. *Added new bullet to the list on page 32, Section 2.5.1. *Changed EPSS-supported items in Sections 3.2.2- 3.2.14 from green to **bold-type**.
E	May 27, 2010	Revision E release *Added further information to the second-to-the-last bullet (DVDD_3.3) on page 32.
p1	July 22, 2010	Preliminary p1 release *Updated to include information on -21Z devices.

© 2010, Conexant Systems, Inc.
All Rights Reserved.

Information in this document is provided in connection with Conexant Systems, Inc. ("Conexant") products. These materials are provided by Conexant as a service to its customers and may be used for informational purposes only. Conexant assumes no responsibility for errors or omissions in these materials. Conexant may make changes to this document at any time, without notice. Conexant advises all customers to ensure that they have the latest version of this document and to verify, before placing orders, that information being relied on is current and complete. Conexant makes no commitment to update the information and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to its specifications and product descriptions.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Conexant's Terms and Conditions of Sale for such products, Conexant assumes no liability whatsoever.

THESE MATERIALS ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, RELATING TO SALE AND/OR USE OF CONEXANT PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, CONSEQUENTIAL OR INCIDENTAL DAMAGES, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. CONEXANT FURTHER DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CONTAINED WITHIN THESE MATERIALS. CONEXANT SHALL NOT BE LIABLE FOR ANY SPECIAL, INDIRECT, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVENUES OR LOST PROFITS, WHICH MAY RESULT FROM THE USE OF THESE MATERIALS.

Conexant products are not intended for use in medical, lifesaving or life sustaining applications. Conexant customers using or selling Conexant products for use in such applications do so at their own risk and agree to fully indemnify Conexant for any damages resulting from such improper use or sale.

The following are trademarks of Conexant Systems, Inc.: Conexant® and the Conexant C symbol. Product names or services listed in this publication are for identification purposes only, and may be trademarks of third parties. Third-party brands and names are the property of their respective owners.

For additional disclaimer information, please consult Conexant's Legal Information posted at www.conexant.com which is incorporated by reference.

Conexant Lead-free products are China RoHS Compliant:

Reader Response: Conexant strives to produce quality documentation and welcomes your feedback. Please send comments and suggestions to tech.pubs@conexant.com. For technical questions, contact your local Conexant sales office or field applications engineer.

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

Contents

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

Figures

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

Tables

Tesis publicada con autorización del autor
No olvide citar esta tesis

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

1 Introduction

1.1 Overview

Conexant's CX20671 HD Audio codec SoC is a low-power,102 dB SNR, high-performance audio codec with integrated 2-WRMS (per channel) stereo speaker amplifier with Spread Spectrum EMI dispersion technology. Two independent pairs of DACs and three independent pairs of ADCs support Multi-Streaming and Real Time Communications applications. The audio fidelity of the device exceeds Microsoft WLP 4.0 Desktop and Notebook Premium Logo requirements. Additionally, the device achieves a high level of integration by featuring an integrated 5 V to 3.3 V Low-dropout (LDO) voltage regulator that guarantees high performance analog audio performance without incurring external BOM, and an integrated 3.3 V to 1.8 V low-dropout voltage regulator used to power internal digital blocks.

The device features a ProCoustic capless headphone driver. This high-output power headphone driver delivers 50 mW per channel into a 32 Ω load, eliminating the need for an external headphone amplifier and DC-blocking capacitors, and produces a full range frequency response without sacrificing the output level. The ProCoustic headphone driver provides a true high-definition listening experience from the PC for the audio aficionado. All output ports feature PopShield circuitry that eliminates pops or clicks.

The CX20671 also features Conexant's D-Flex power management scheme, which allows the system to exceed the power savings specified in the Intel ECR 15B requirement. The entire audio SOC consumes 16.79 mW during S0-idle. The internal Wake-on-PC-Beep logic resumes the analog paths for the external PC-Beep to propagate through to the output ports.

The CX20671 features one single-bit stream digital microphone interface, which allows interfacing to two digital microphones for dual microphone array implementations. The Digital Microphone Interface (DMI) is optimized with a hardware DC-level filter, which compensates for digital microphones with DC offset limitations. Conexant has qualified many digital microphones and listed them on the Approved Vendor List (AVL), providing the OEM and the ODM with more selections and flexibility. The audio codec features an independent SPDIF out supporting sample rates up to 96 kHz, 16-24-bit resolution.

The device is compliant with Intel's High Definition Audio Specification (Revision 1.0), as well as the ECR 15B power management scheme.

Conexant offers the most comprehensive software options:

- In-house developed Voice Processing Algorithms enhances the clarity of VoIP calls and improves the accuracy of voice commands and dictation.
- SoftEQ with Dynamic Range Compression improves the sound quality of low cost speakers.
- 3D Expander widens the audio stage for fuller and richer sound.
- Audio Director augments multi-streaming capability; and third-party end point redirection/switching (i.e., HDMI and Bluetooth). Third party software APO support includes SRS, Dolby, Creative Labs, and others.

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

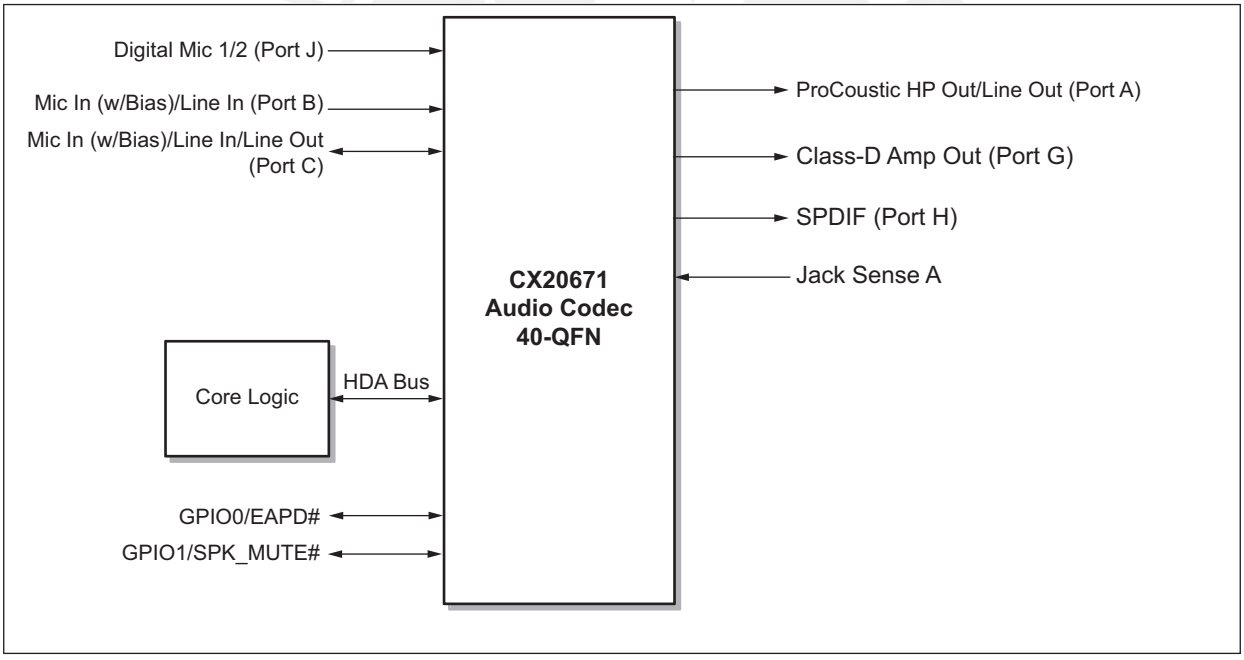
Table 1 shows the different devices and the functions that are supported for each.
Figure 1 illustrates the CX20671 devices and major signal interfaces.

Table 1. CX20671 Models and Functions

Model/Order/Part Numbers						Supported Functions	
Device Set Order Number	Audio Codec Part Number	Codec Revision	Audio Codec Package Type	SmartDAA4 Line Side Device (LSD) [16-Pin QFN] Part Number	V.92 Modem	Number of DACs/ADCs	Digital Mic
CX20671-11Z	CX20671	-11Z	40-QFN	None	N	4/6	2
CX20671-21Z	CX20671	-21Z	40-QFN	None	N	4/6	2

GENERAL NOTES:
1. Supported functions (Y = Supported; N = Not supported).
2. All devices are lead-free (Pb-free) and RoHS-compliant, and are compatible with leaded reflow processes.
3. Contact local Conexant Sales office for advanced software options.

Figure 1. CX20671 Devices and Major Signal Interfaces



Tesis publicada con autorización del autor
No olvide citar esta tesis

1.2 CX20671 Audio Codec Features

- 24-bit, two pairs of independent DACs and three pairs of independent ADCs
- ProCoustic headphone driver, which delivers 50 mW into 32 Ω load with no pop, eliminating the need for an external amplifier and DC-blocking capacitors
- Integrated 5 V to 3.3 V low-dropout voltage regulator for improved audio performance, eliminating need for external regulator or power transistor
- Integrated 3.3 V to 1.8 V low-dropout voltage regulator, used to power digital blocks
- Integrated 2 WRMS (per channel) class-D stereo speaker amplifier with Spread Spectrum and 10-kV ESD withstand capability
- Digital Microphone interface with internal MIC boost supporting 2 digital microphone elements
- Independent Sony Philips Digital Interface (SPDIF) Output supporting sample rates 44.1 kHz, 48 kHz, and 96 kHz, 16, 20, and 24-bit resolution
- Internal microphone boost
  - Digital: 0, 12, 24, 36, 48 dB
  - Analog: 0, 10, 20, 30, 40 dB
- Microphone Security Control (Contact Conexant Sales/FAE for additional information).
- Exceeds Vista/Windows 7 Desktop and Notebook Premium Logo Requirements, WLP4.0
- D-Flex power management exceeds Intel ECR 15B requirements, and features Wake-On-PCBeep functionality
- Hardware Headphone limiter bit (supports GS Mark EN50332-2)
- Compliant with Intel High Definition Audio Specification Rev. 1.0
- Supports both 1.5 V and 3.3 V signaling with the core logic chipset
- Retaskable ports
  - Configure between Headphone and Line-out or between Mic and Line-in
- Independent sampling rate for DAC and ADC; supports audio formats ranging from 16-bit, 44.1 kHz to 24-bit, 192 kHz
- Pop Shield: pops and clicks reduction circuitry, including class-D speaker outputs
- Jack sense detects up to four jacks using only one sense pin
- Digital Mixer
- +3.3 V analog and I/O operation; uses Vaux for power management modes
- Audio Director for Headphone and Internal Speakers Redirection (optional).
  - Supporting Classic Mode
  - Vista/Windows 7 Multi-Stream
  - Custom Multi-Stream Mode
- Voice Processing Algorithms (optional)

Tesis publicada con autorización del autor
No olvide citar esta tesis

  - End-to-end Noise Reduction (patent pending)
  - Multi-band Acoustic Echo Cancellation
  - Side Noise Rejection Beam Forming
- SmartAudio GUI (optional) - advanced audio control
- Digital Parametric SmartEQ with Dynamic Compression DSP (optional)
  - Enhances the sound quality on low cost speakers
  - Night Mode
- 3D Expander
- Third Party Logo Software support includes
  - SRS
  - Dolby
  - Creative Labs
  - ForteMedia
  - Andrea
  - MaaxAudio
  - Virage Logic
- Supports 32-bit/64-bit Windows OS and Linux
- Available in 40-pad thermally-enhanced QFN package

1.3 System Compatibility

- System compatibility
  - Windows XP/Vista/Windows 7 operating system on a 1 GHz-based computer with 512 MB RAM, or equivalent
  - Microsoft Vista/Windows 7 Premium Logo compliant, WLP4.0
  - Linux Kernel (contact local Conexant Sales Office for details)

1.4 Hardware Qualification Process

The Hardware Qualification Process (HQP) is intended to improve the quality and reliability of ODM custom boards being shipped to PC OEMs. The goals of this process are to:

- Eliminate common design mistakes
- Ensure boards perform well and pass DTM Fidelity requirements with good margin
- Eliminate potential manufacturing issues that may result from a marginal design
- Eliminate country specific issues
- Eliminate common INF problems
- Converge towards standard designs

Tesis publicada con autorización del autor
No olvide citar esta tesis

The HQP includes review of schematics, board layout, and BOM (Bill of Material). All boards must meet the pre-defined criteria. Contact the local Conexant Sales office for more details about the HQP process.

HQP *must* be performed for all OEM designs.

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

2 Hardware Interface

2.1 General

2.1.1 HD Audio Host Interface

The HD Audio host interface conforms to HD Audio (Rev. 1.0)

The supported HD Audio signals are as follows:

- Bit Clock (BIT_CLK), input
- Frame Sync (SYNC), input
- Serial Data Output (SDATA_OUT), input
- Serial Data Input (SDATA_IN), input/output
- Master Hardware Reset (RESET#), input

2.1.2 Control Signals

Control signals supported from straps or the host are as follows:

- External Amplifier Power Down (EAPD#), output
- Class-D speaker mute (SPK_MUTE#), input
- Jack sensing (SENSEA), input
- General-purpose inputs/outputs (GPIO0, GPIO1)

2.1.3 Audio Signals

Audio interface signals supported are as follows:

- Port A (PORTA_L and PORTA_R), ProCoustic headphone output/line output
- Port B (PORTB_L and PORTB_R), microphone input/line input, with microphone bias voltage
- Port C (PORTC_L and PORTC_R), microphone input/line input/line output, with microphone bias voltage
- Port G (LEFT± and RIGHT±), Class-D speaker amplifier stereo output
- Digital Stereo Microphone (DIGITAL_MIC_1/2), digital microphone input, dual array
- PC Speaker Beep pass-through (PC_BEEP), input
- Sony Philips Digital Interface (SPDIF) Output

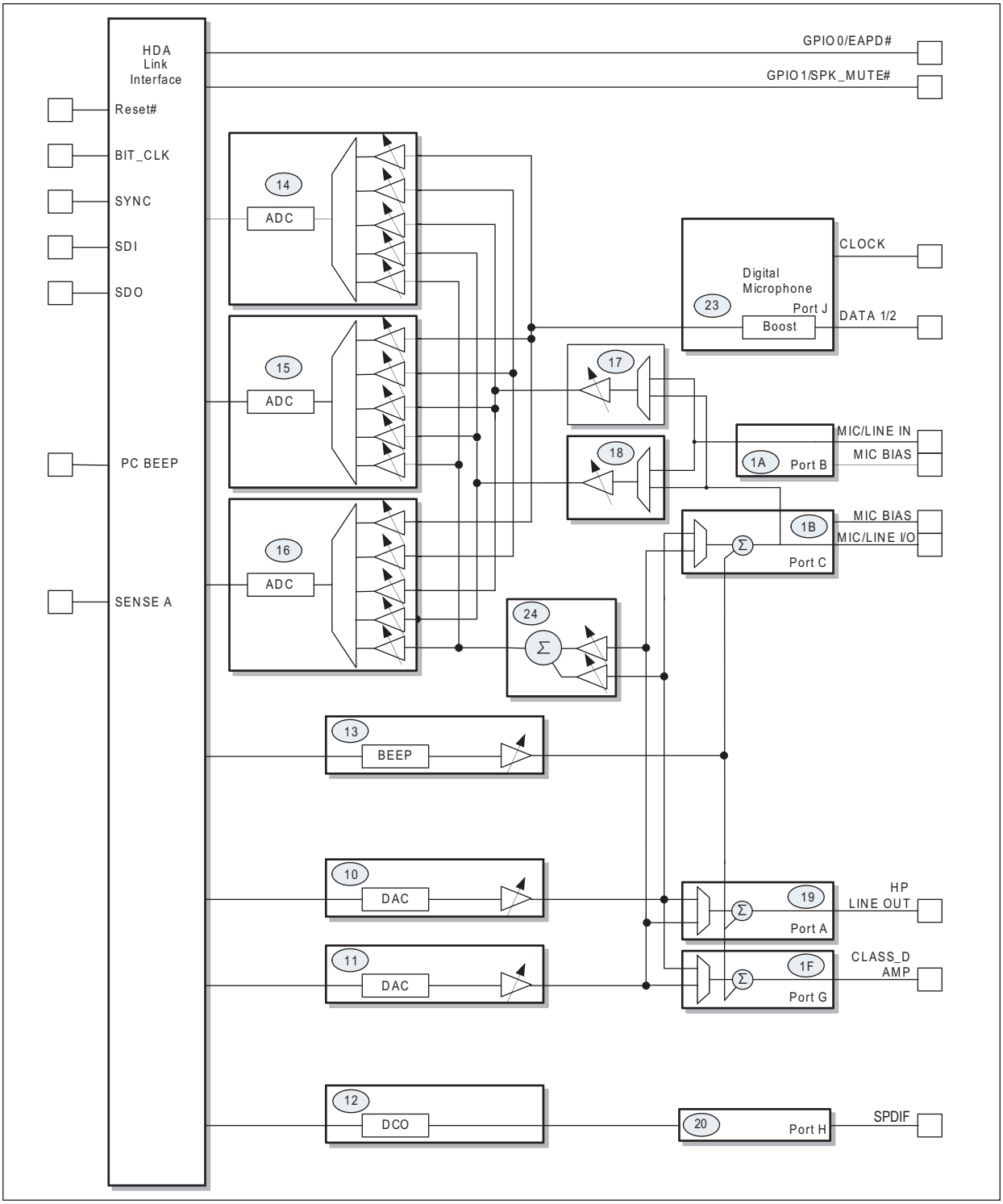
Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

2.2 CX20671 Block Diagram

Figure 2 provides a simplified block diagram of the CX20671.

Figure 2. CX20671 Block Diagram



Tesis publicada con autorización del autor
No olvide citar esta tesis

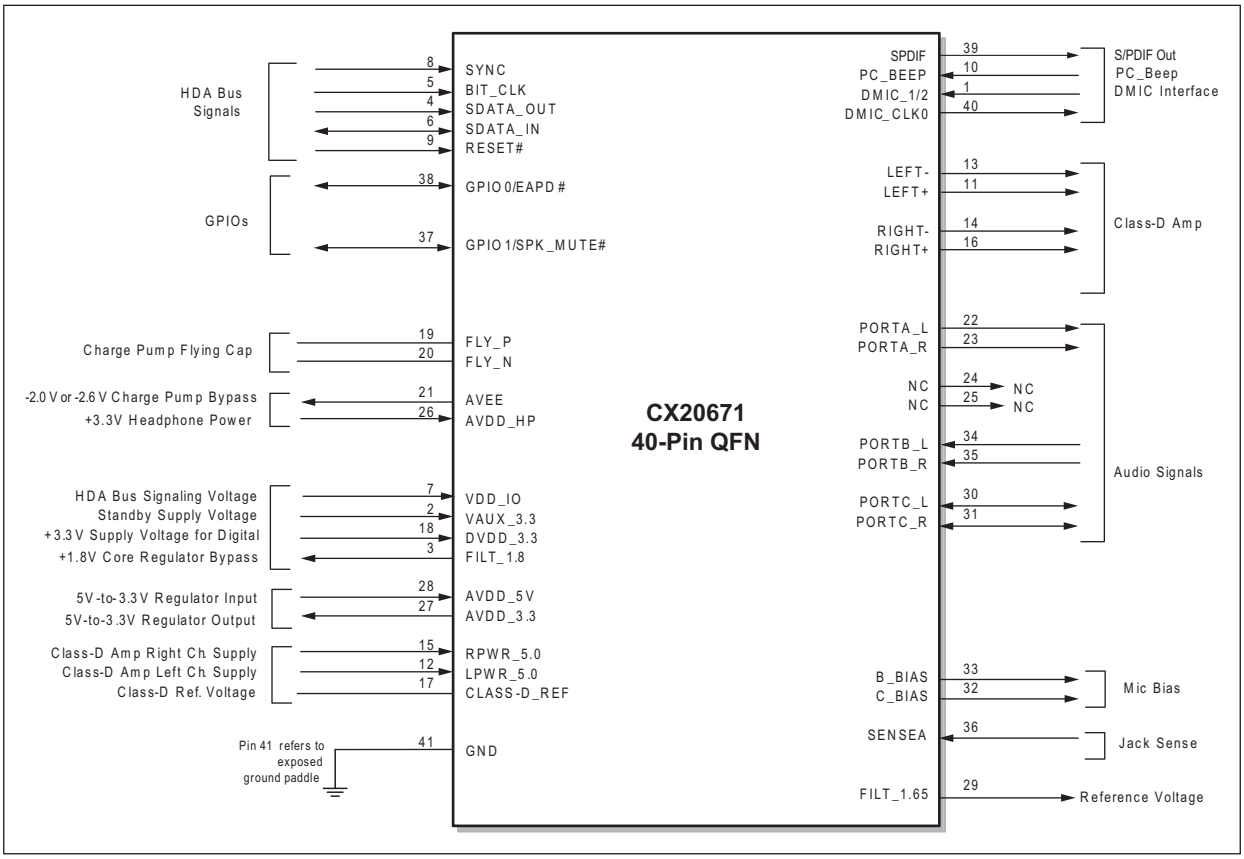
TESIS PUCP

2.3 CX20671 Pin Assignments, Signal Definitions, and Electrical Characteristics

The CX20671 40-QFN device signals are shown by major interface in Figure 3, by pin number in Figure 4, and are listed by pin number in Table 2.

Hardware interface signals are defined in Table 3.

Figure 3. CX20671 40-QFN Hardware Interface Signals

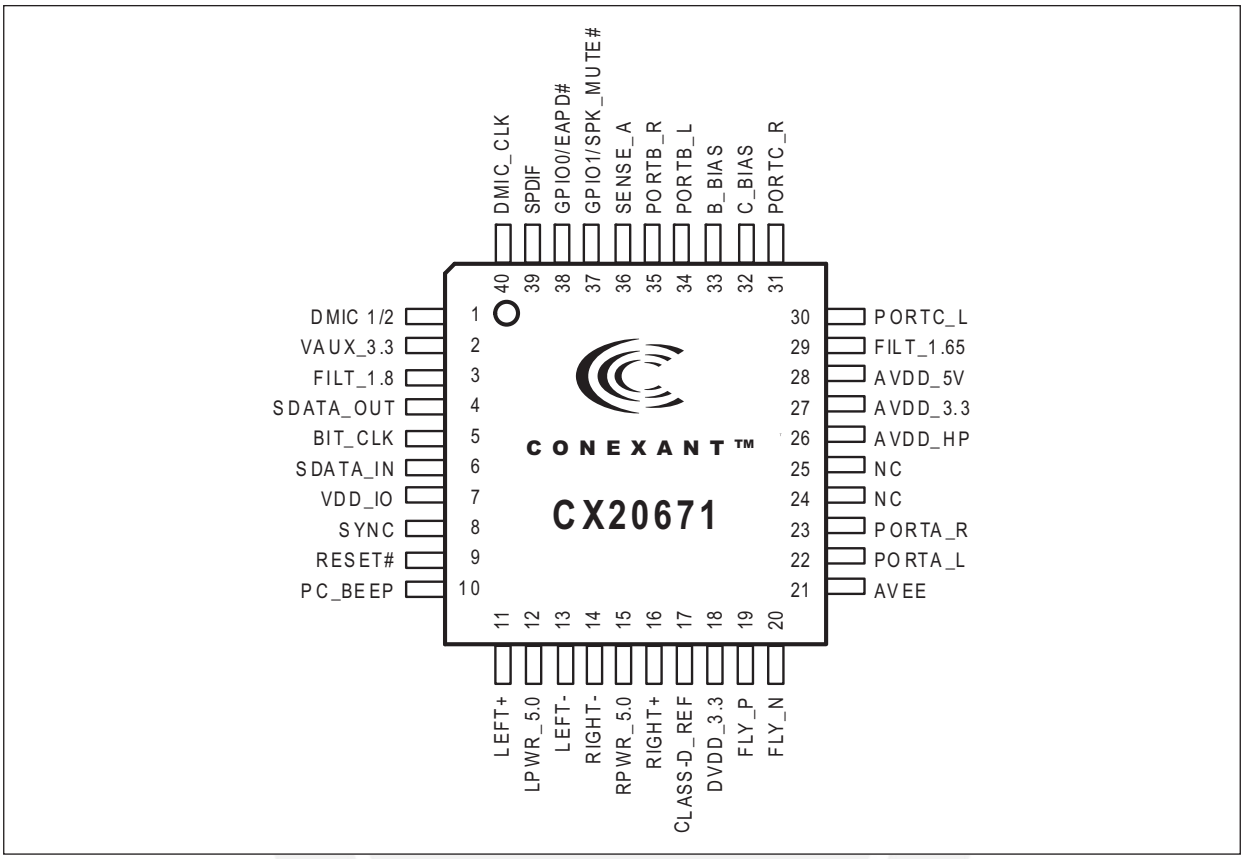


Tesis publicada con autorización del autor
No olvide citar esta tesis

Figure 4. CX20671 40-QFN Pad Signals

Pin Define

Please help add Pin41 GND for Thermal Pad



Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

Table 2. CX20671 Pad Signals

Pad Number	Signal Name	Pad Number	Signal Name
1	DMIC_1/2	21	AVEE
2	VAUX_3.3	22	PORTA_L
3	FILT_1.8	23	PORTA_R
4	SDATA_OUT	24	NC
5	BIT_CLK	25	NC
6	SDATA_IN	26	AVDD_HP
7	VDD_IO	27	AVDD_3.3
8	SYNC	28	AVDD_5V
9	RESET#	29	FILT_1.65
10	PC_BEEP	30	PORTC_L
11	LEFT+	31	PORTC_R
12	LPWR_5.0	32	C_BIAS
13	LEFT-	33	B_BIAS
14	RIGHT-	34	PORTB_L
15	RPWR_5.0	35	PORTB_R
16	RIGHT+	36	SENSE_A
17	CLASS-D_REF	37	GPIO1/SPK_MUTE#
18	DVDD_3.3	38	GPIO0/EAPD#
19	FLY_P	39	SPDIF
20	FLY_N	40	DMIC_CLK
		41[(1)]	GND (Note 1)

FOOTNOTES:

(1) Pad 41 refers to the exposed pad at the bottom of the device. This thermal/electrical pad must be connected to PCB ground plane with enough vias. It is recommended that a 4x4 grid of such vias be used.

Tesis publicada con autorización del autor
No olvide citar esta tesis

Table 3. CX20671 Pad Signal Definitions (1 of 4)

Label	Pad Number	Type	I/O Type	Signal Name/Description
Power				
DVDD_3.3	18	PWR	PWR	**Digital Supply Voltage.** +3.3 V. Connect to system +3.3 V.
~~VAUX_3.3~~	~~2~~	~~PWR~~	~~PWR~~	~~**Standby Supply Voltage.** +3.3 V. Connect to system's +3.3 V Standby supply. This power pin is used to support Wake-on-Jack functions.~~
VDD_IO	7	PWR	PWR	**Input/Output Signaling Voltage Supply.** Determines the signaling voltage that is being used on the host system. When VDD_IO is +1.5 V, the device will use 1.5 V signaling on the HDA interface pins; when VDD_IO is +3.3 V, the device will use 3.3 V signaling on the HDA interface pins.
FILT_1.8	3	PWR	PWR	**Internally Regulated Digital Core Supply Voltage.** +1.8 V ± 5%. Connect to external decoupling capacitor.
AVDD_5V	28	PWR	PWR	**Analog Supply Input Voltage for LDO.** +5.0 V. Connect to system +5.0 V supply.
~~AVDD_3.3~~	~~27~~	~~PWR~~	~~PWR~~	~~**Output Voltage from LDO.** +3.3 V ± 5%. Connect to external decoupling capacitor.~~
~~AVDD_HP~~	26	PWR	PWR	**Supply Input Voltage for Headphone Amplifiers.** +3.3 V. Connect to system +3.3 V.
RPWR_5.0	15	PWR	PWR	**Supply Voltage for Class-D Amplifier, Right Channel.** +5.0 V. Connect to LPWR_5.0. Connect LPWR_5.0/RPWR_5.0 to system +5.0 V supply through a 0.1 Ω resistor.
LPWR_5.0	12	PWR	PWR	**Supply Voltage for Class-D Amplifier, Left Channel.** +5.0 V. Connect to RPWR_5.0. Connect LPWR_5.0/RPWR_5.0 to system +5.0 V supply through a 0.1 Ω resistor.
FLY_N	20	PWR	PWR	**Charge Pump Negative Transfer Charge.** Connected to FLY_P through a 2.2 µF or 1.0 µF capacitor.
FLY_P	19	PWR	PWR	**Charge Pump Positive Transfer Charge.** Connected to FLY_N through a 2.2 µF or 1.0 µF capacitor.
AVEE	21	PWR	PWR	**Internally Generated Analog Negative Supply.** Connect to external decoupling capacitor. -2.6 V when HP output set at 1.2 Vrms ± 10% -2.0 V when HP output set at 1.0 Vrms ± 10%

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

Table 3. CX20671 Pad Signal Definitions (2 of 4)

Label	Pad Number	Type	I/O Type	Signal Name/Description
Ground				
GND	41	GND	GND	**Audio Device Ground.** This is thermal/electrical GND paddle of device. Connect to audio ground.
High Definition Audio Interface				
BIT_CLK	5	I	Ihd	**Bit Clock**. 24 MHz serial data input bit clock from the HDA link. Connect to BITCLK.
SYNC	8	I	Ihd	**Frame Sync.** 48 kHz fixed rate sample HDA sync input. Synchronization pulse from an HDA compliant controller to all of the HDA compliant codecs on the link. This signal is nominally 0.167 µs wide pulse that is used to synchronize the HDA. Reset state = low. Standard load = 50 pF. SYNC is derived from dividing BITCLK by 500. Connect to SYNC.
SDATA_OUT	4	I	Ihd	**Serial Data Output.** Serial input data stream from an HDA controller. Reset state = low. Standard load = 50 pF. Connect to SDATA_OUT through 33 Ω
SDATA_IN	6	I/O	Ohd	**Serial Data Input.** Serial output data stream to the HDA controller. Functions as an input during codec initialization. Controller has a weak pull-down resistor to prevent spurious events in electrically noisy environments. Connect to SDATA_IN through 33 Ω
RESET#	9	I	Ihdl	**Master Hardware Reset.** Active low HDA link reset signal. The minimum width of this pulse must be 100 µs. Connect directly to RESET.
Reference Voltage Connections				
FILT_1.65	29	REF	REF	**Analog Reference Voltage.** 1.65 V ± 5%. Connect to external decoupling capacitor.
CLASS-D_REF	17	REF	REF	**Class-D Amplifier Reference Voltage.** Connect to RPWR_5.0/LPWR_5.0 voltage supply through external capacitor.

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

Table 3. CX20671 Pad Signal Definitions (3 of 4)

Label	Pad Number	Type	I/O Type	Signal Name/Description
General Purpose Input/Outputs				
GPIO0/EAPD#	38	I/O	It/Ot	**External Amplifier Power-Down Signal/ General Purpose I/O.** EAPD# is an active-low output. If EAPD = 0, power down the external amplifier. If EAPD = 1, power up the external amplifier
GPIO1/SPK_MUTE#	37	I/O	It/Ot	General Purpose I/O, Class-D Speaker Amplifier Mute Input. SPK_MUTE# is a active-low input.
Audio Digital Signals				
PC_BEEP	10	I	Id	PC Speaker Beep Pass-Through. Input. Logic-level BEEP signal needs to be ac-coupled to this pin.
DMIC_1/2	1	I	Id	**Stereo Digital Microphone Data.** Input
DMIC_CLK	40	O	Od	**Digital Microphone Clock.** Output
SPDIF	39	O	It/Ot	Sony Philips Digital Interface (SPDIF) output. Note: For -21Z devices only, a pull-down on this pin sets PC BEEP gain to -18 dB while the codec is in RESET.
Audio Analog Signals				
These signals connect to analog sources and sinks, including microphones and speakers.				
PORTB_L	34	I	Ia	**Microphone Input/Line Input, Left Channel.** With microphone bias voltage.
PORTB_R	35	I	Ia	**Microphone Input/Line Input, Right Channel.** With microphone bias voltage.
B_BIAS	33	REF	REF	Microphone Bias Voltage for Port B.
PORTC_L	30	I	Ia, Oa	**Microphone Input/Line Input/Line Output, Left Channel.** With microphone bias voltage.
PORTC_R	31	I	Ia, Oa	**Microphone Input/Line Input/Line Output, Right Channel.** With microphone bias voltage.
C_BIAS	32	REF	REF	Microphone Bias Voltage for Port C.
LEFT+	11	O	Oa	Class-D Amplifier Output, Left Channel, Positive.
LEFT-	13	O	Oa	Class-D Amplifier Output, Left Channel, Negative.
RIGHT+	16	O	Oa	Class-D Amplifier Output, Right Channel, Positive.
RIGHT-	14	O	Oa	Class-D Amplifier Output, Right Channel, Negative.
PORTA_L	22	O	Oa	**Headphone Output/Line Output, Left Channel.** This is a ProCoustic (cap-less) headphone output.
PORTA_R	23	O	Oa	**Headphone Output/Line Output, Right Channel.** This is a ProCoustic (cap-less) headphone output.

Tesis publicada con autorización del autor
No olvide citar esta tesis

Table 3. CX20671 Pad Signal Definitions (4 of 4)

Label	Pad Number	Type	I/O Type	Signal Name/Description
SENSE_A	36	I	Ia	SENSE A Input.
Reserved/Not Used				
NC	25	-	-	**Not Used.** Leave unconnected.
NC	24	-	-	**Not Used.** Leave unconnected.
NC	39	-	-	**Not Used.** Leave unconnected.

GENERAL NOTES:

I/O types:
Ia Analog input
Oa Analog output
Od Digital output
Ohd Digital output, HD Audio-compatible
Id Digital input, with pull-down
Ihd Digital input, HD Audio-compatible
It Digital input, TTL-compatible

Table 4 lists the device's absolute maximum ratings.
Table 5 lists the electrical characteristics for the Digital Mic interface.
Table 6 lists the devices' DC characteristics for the TTL-compatible I/Os.
Table 7 lists the host's required DC characteristics for the HD Audio interface signals.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	DVDD_3.3	3.6	V
	VAUX_3.3	3.6	
	VDD_IO	3.6/1.65(1)	
	AVDD_HP	3.6	
	AVDD_5V	5.5	
	RPWR_5.0	5.5	
	LPWR_5.0	5.5	
Digital Input Voltage	V_{ind}	-0.7 to 4.0	V
Analog Input Voltage	V_{ina}	-0.7 to 4.0	V
DC Clamp Current, Input	I_{ik}	± 20	mA
DC Clamp Current, Output	I_{ok}	± 20	mA
Storage Temperature Range	T_{stg}	-55 to 125	°C

FOOTNOTES:
(1) Depends on 3.3 volts or 1.5 volts HD Audio signaling level.

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

Table 5. DC Characteristics –Digital Microphone

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Input Voltage Low	V_{IL}	–0.3	—	0.94	V	Max. value adjustable
Input Voltage High	V_{IH}	1.2	—	3.3	V	
Output Voltage Low	V_{OL}	—	—	0.4	V	
Output Voltage High	V_{OH}	2.6	—	—	V	
Drive Strength		0.3	4	6.8	mA	Adjustable
GENERAL NOTES: Test Conditions unless otherwise stated: DVDD = +3.3 ± 0.165 VDC; TA = 0°C to 70°C.						

Table 6. DC Characteristics – TTL Compatible (EAPD#, GPIOs)

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Input Voltage	V_{IN}	—	—	4.0	V	
Input Voltage Low	V_{IL}	–0.5	—	0.8	V	
Input Voltage High	V_{IH}	2.0	—	Vdd+0.5	V	
Output Voltage Low	V_{OL}	0	—	0.4	V	
Output Voltage High	V_{OH}	2.4	—	Vdd	V	
GPIO Output sink current at 0.4 V maximum	—	—	—	12	mA	
GPIO Output source current at 2.97 V minimum	—	—	—	12	mA	
GPIO rise/fall time	—	—	—	4	ns	25% to 75%
GENERAL NOTES: Test Conditions unless otherwise stated: DVDD = +3.3 ± 0.165 VDC; TA = 0°C to 70°C; external load = 50 pF						

Tesis publicada con autorización del autor
No olvide citar esta tesis

Table 7. Host Signal Characteristics – HD Audio

Parameter	Symbol	Minimum	Maximum	Units	Test Conditions
HD Audio Signal Levels at 3.3 V					
VDD_IO	V_{CC}	3.135	3.465	V	V_{CC} < VDD + 0.5 V
Input High Voltage	V_{IH}	0.65 x V_{CC}		V	
Input Low Voltage	V_{IL}		0.35 x V_{CC}	V	
Output High Voltage	V_{OH}	0.9 x V_{CC}		V	I_{OUT} = 500 µA
Output Low Voltage	V_{OL}		0.10 x V_{CC}	V	I_{OUT} = 1500 µA
Output High Voltage - AC Drive Point	V_{OHAC}	0.7 x V_{CC}		V	I_{OUT} = -15 x V_{CC} mA
Output Low Voltage - AC Drive Point	V_{OLAC}		0.3 x V_{CC}	V	I_{OUT} = 15 x V_{CC} mA
Input leakage Current	I_{IL}		±10	µA	0 < V_{IN} < V_{CC}
HD Audio Signal Levels at 1.5 V					
VDD_IO	V_{CC}	1.35	1.65	V	V_{CC} < VDD + 0.5 V
Input High Voltage	V_{IH}	0.6 x V_{CC}		V	
Input Low Voltage	V_{IL}		0.4 x V_{CC}	V	
Output High Voltage	V_{OH}	0.9 x V_{CC}		V	I_{OUT} = 500 µA
Output Low Voltage	V_{OL}		0.10 x V_{CC}	V	I_{OUT} = 1500 µA
Output High Voltage - AC Drive Point	V_{OHAC}	0.7 x V_{CC}		V	I_{OUT} = -9.38 x V_{CC} mA
Output Low Voltage - AC Drive Point	V_{OLAC}		0.3 x V_{CC}	V	I_{OUT} = 9.38 x V_{CC} mA
Input leakage Current	I_{IL}		±10	µA	0 < V_{IN} < V_{CC}

GENERAL NOTES:

1. The supply voltage refers to the VDD_IO pin.
2. Test Conditions unless otherwise stated: DVDD = +3.135V to +3.465 V; TA = 0 °C to 70 °C.

Tesis publicada con autorización del autor
No olvide citar esta tesis

Figure 5. Output Butter for 3.3 V Signaling

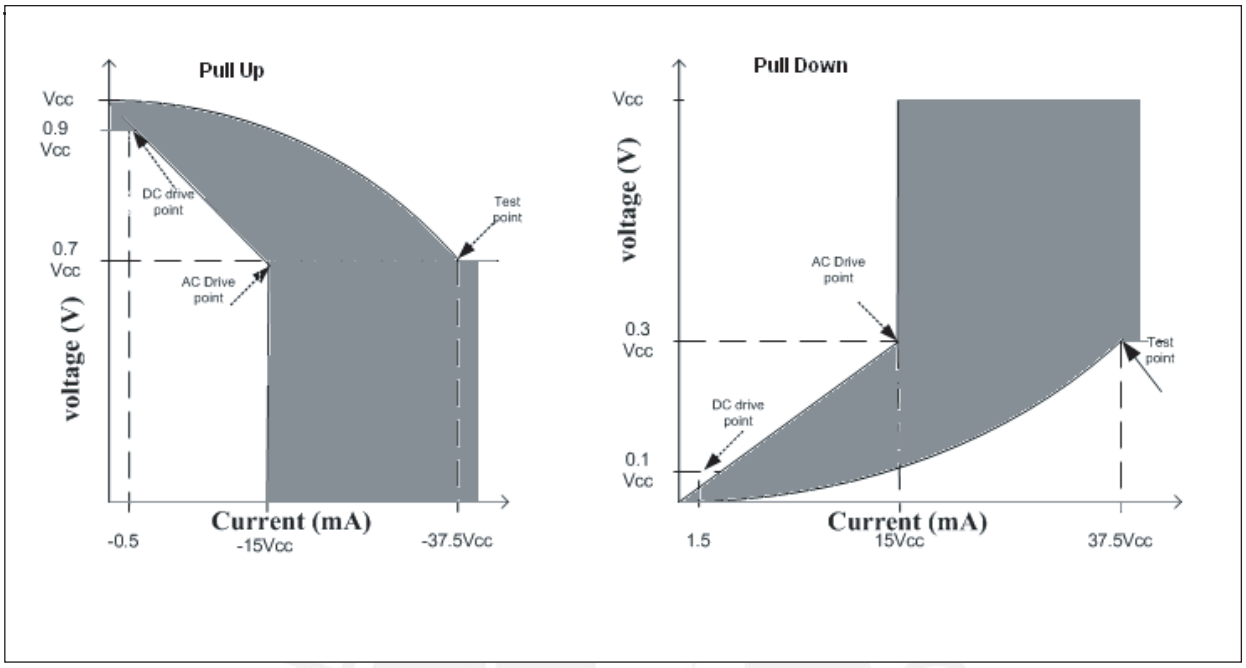
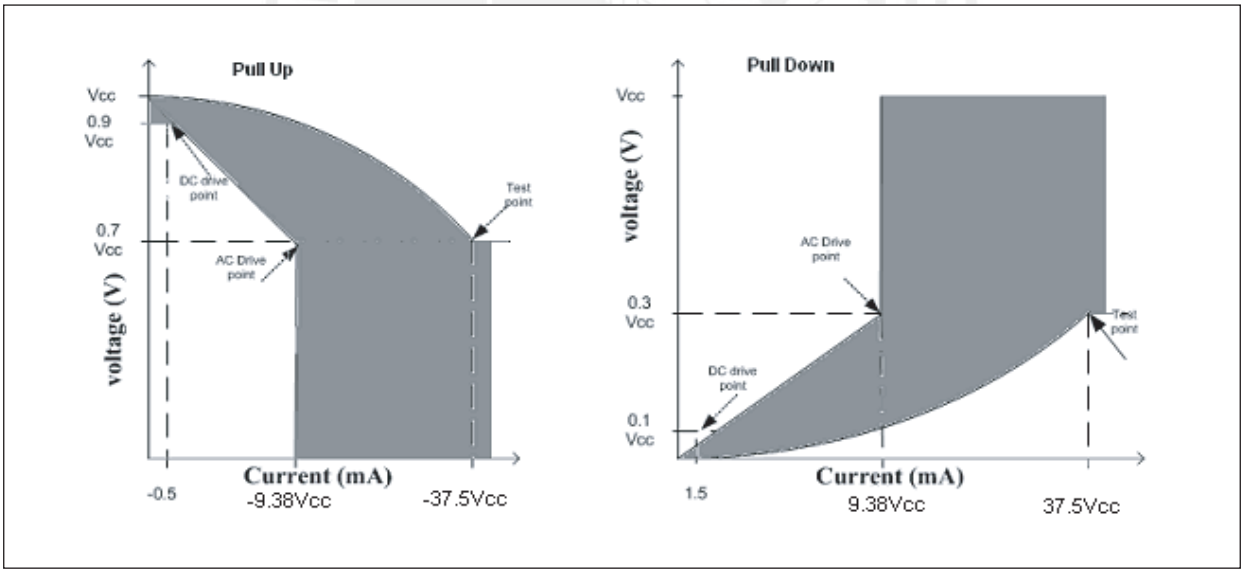


Figure 6. CX20671 Output Buffer for 1.5 V Signaling



Tesis publicada con autorización del autor
No olvide citar esta tesis

2.4 Device Performance Specifications

The following tables and graphs illustrate the device's analog performance.

Table 8. CX20671 Analog Performance Characteristics *(1 of 2)*

Parameter	Minimum	Typical	Maximum	Units
Line Outputs				
Full Scale Output Voltage	1.0			Vrms
Dynamic Range (measured with -60 dBFS signal present)		97		dBFS
Total Harmonic Distortion + Noise (THD + N), measured at -3 dBFS		-90	-93	dB
Channel Crosstalk		-84		dBFS
Analog Frequency Response (+/- 3 dB at 20 Hz, +/- 1 dB at 20000 Hz)	20		20000	Hz
Headphone Output				
Full Scale Output Voltage		1.2		Vrms
Dynamic Range (measured with -60 dBFS signal present)		97		dBFS
Total Harmonic Distortion + Noise (THD + N), measured at -3 dBFS		-85		dB
Channel Crosstalk		-75		dBFS
Analog Frequency Response (+/- 3 dB at 20 Hz, +/- 1 dB at 20000 Hz)	20		20000	Hz
Class-D Speaker Amplifier Outputs				
Full Scale Output Voltage (into 4 Ω)	3.96 2.83	4.0 2.90	4.2 3	Vp Vrms
Dynamic Range (measured with -60 dBFS signal present)		92		dBFS
Total Harmonic Distortion + Noise (THD + N, measured at -3 dBFS)		-70		dBFS
Analog Frequency Response (+/- 3 dB at 20 Hz, +/- 1 dB at 20000 Hz)	20		20000	Hz
Efficiency (Measured at 1 W/Ch)		85		%
Line Inputs				
Full Scale Input Voltage	1.0			Vrms
Dynamic Range (measured with -60 dBFS signal present)		89		dBFS
Total Harmonic Distortion + Noise (THD + N), measured at -3 dBFS		-87		dB
Channel Crosstalk		-84		dBFS
Analog Frequency Response (+/- 3 dB at 200 Hz, +/- 1 dB at 20000 Hz)	200		20000	Hz

Tesis publicada con autorización del autor
No olvide citar esta tesis

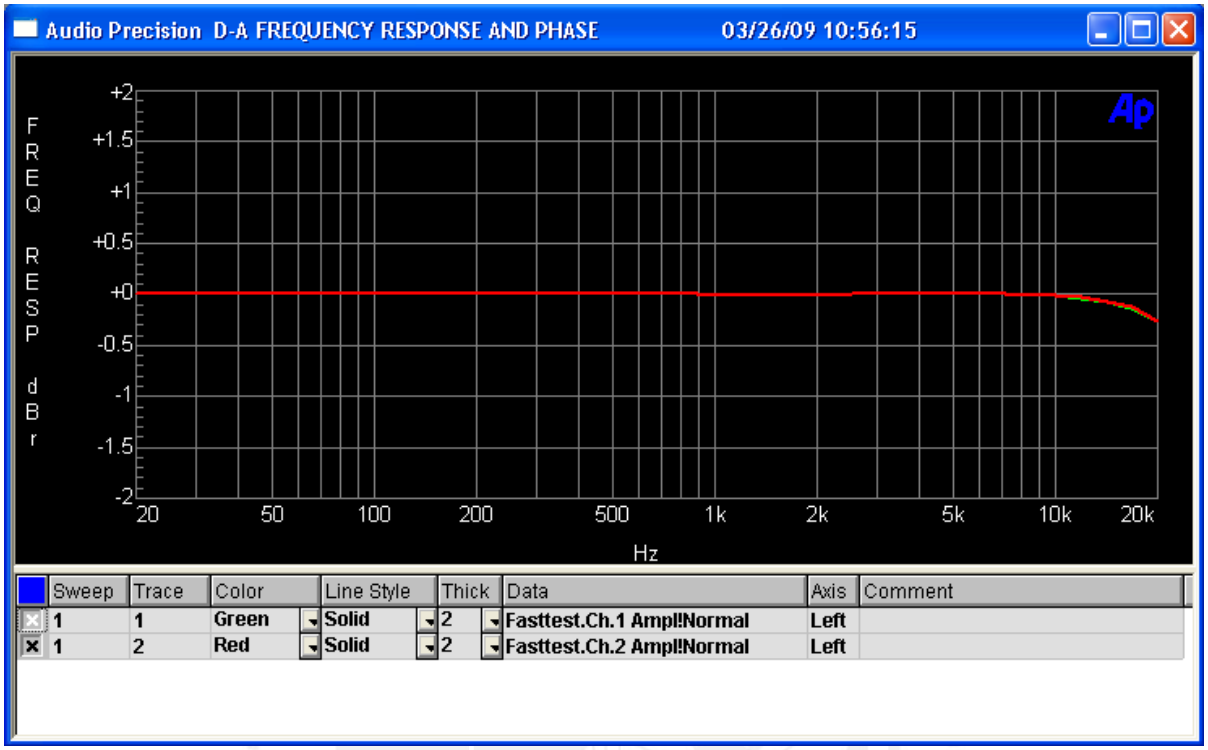
TESIS PUCP

Table 8. CX20671 Analog Performance Characteristics (2 of 2)

Parameter	Minimum	Typical	Maximum	Units
Line Inputs (continued)				
Input Resistance 0 dB 10-40 dB		 15.8 5.0		kΩ
Input Capacitance		5		pF
Microphone Inputs				
Full Scale Input Voltage (With 20 dB boost) Full Scale Input Voltage (With boost off)	0.1 1.0			Vrms
Dynamic Range (measured with -60 dBFS signal present)		89		dBFS
Total Harmonic Distortion + Noise (THD + N), measured at - 3 dBFS		-83.4		dBFS
Channel Crosstalk (measured at 1 kHz, 0 dB gain)		-84		dBFS
Analog Frequency Response (+/- 3 dB at 200 Hz, +/- 1 dB at 20000 Hz)	200		20000	Hz
Input Resistance 0 dB 10-40 dB		 15.8 5.0		kΩ
Input Capacitance		5		pF

Tesis publicada con autorización del autor
No olvide citar esta tesis

Figure 7. Class-D Speaker Amplifier Magnitude Frequency Response (16 bit, 48 kHz)



Tesis publicada con autorización del autor
No olvide citar esta tesis

Figure 8. CX20671 THD+N versus Frequency, for Class-D Amplifier Output

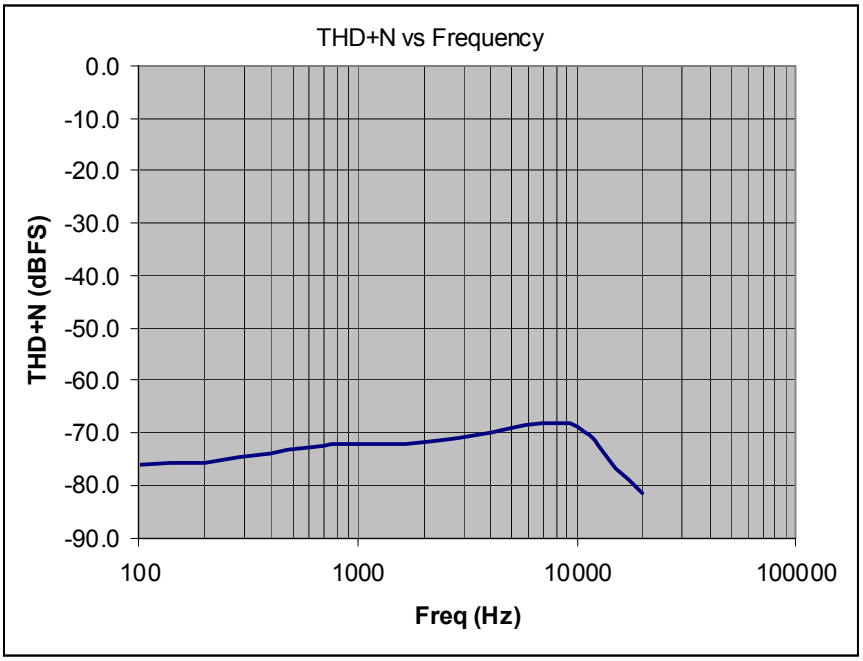
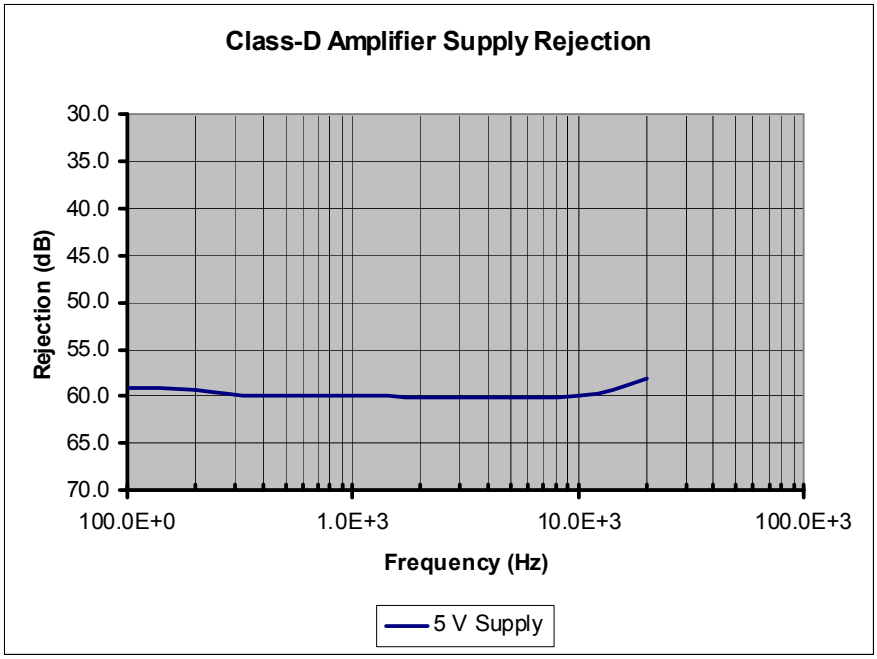


Figure 9. CX20671 Power Supply Rejection, for Class-D Amplifier Output



Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

Figure 10. CX20671 Power Supply Rejection, for Headphone Amplifier Output

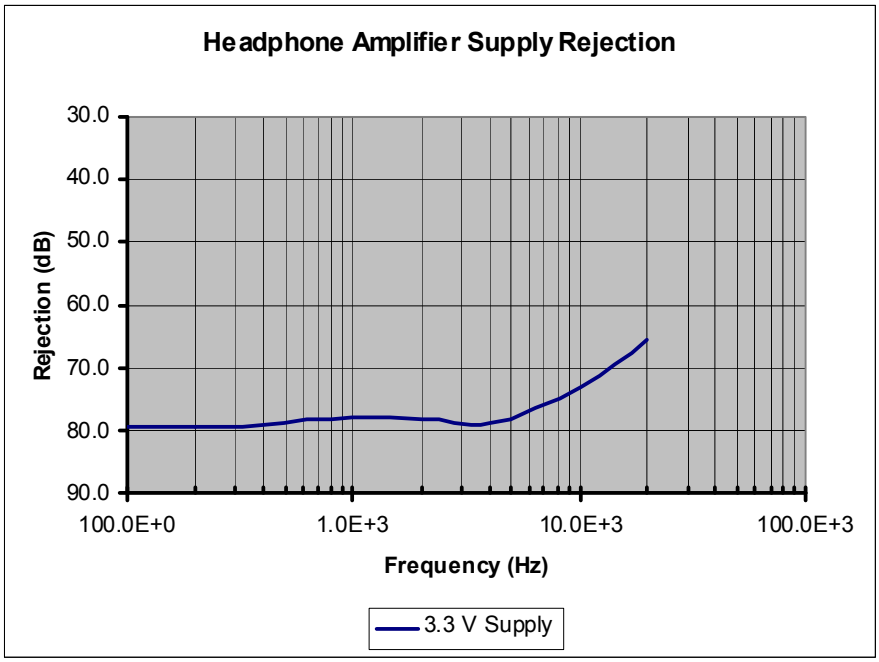
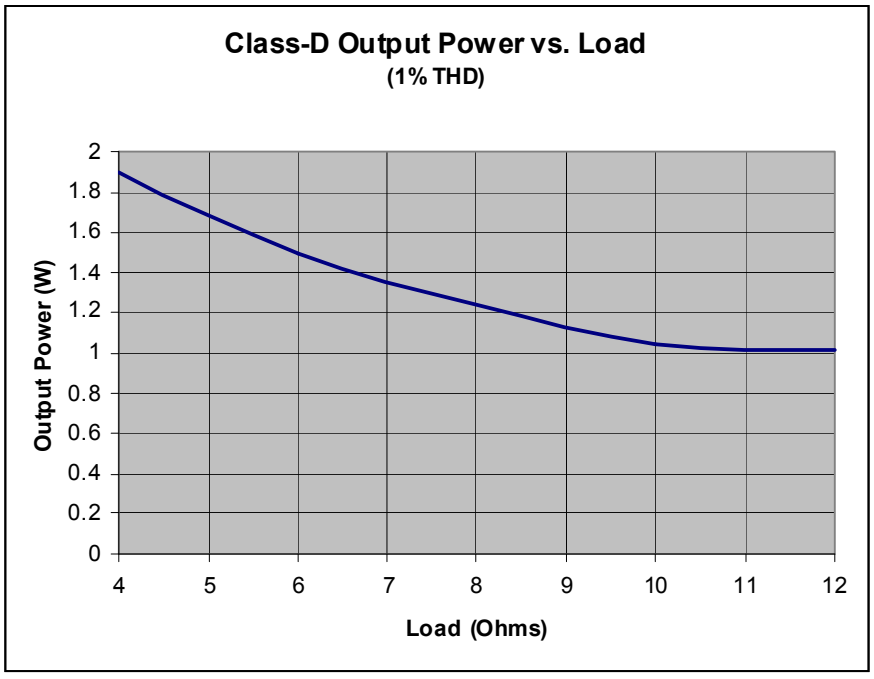


Figure 11. CX20671 Class-D Output Power vs. Load (1% THD)



Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

2.5 Power Management and Power Consumption

2.5.1 Power Management

Advanced power management features allow the device to conserve additional power by disabling/enabling individual functional blocks. This is shown in Table 9.

Table 9. Power Management

Functional Block	D0 (S0-Idle)	D2 (S0-Idle) Pre-ECR 15B	D3 (S0-Idle) EPSS ECR 15B	D-Flex(1)	D3 (S3) or D4 (S3)(2)	D3 (S4) or D4 (S4)(3)
DAC	On	Off	Off	Flex mode	Off	Off
ADC	On	Off	Off	Flex mode	Off	Off
Ports	On	Off	Off	Flex mode	Off	Off
Headphone Amps	On	Off	Off	Flex mode	Off	Off
5V LDO	On	On	On	On	Off[3]	Off[3]
Class-D Amp	On	Off	Off	Flex mode	Off	Off
Reference Voltage (1.65 V)	On	On	On	On	Off	Off
Port Sense	On	On	On	On	Off	Off
HD-Audio Bus	On	On	On	On	Off	Off
Reg Banks	On	On	On	On	On	Off
AVDD_HP Supply	On	On	On	On	Off(3)	Off
DVDD_3.3 Supply	On	On	On	On	Off(3)	Off
VDD_IO Supply	On	On	On	On	On	Off
VAUX_3.3 Supply	On	On	On	On	On	Off

FOOTNOTES:

(1) D-Flex mode requires loading Conexant proprietary driver. D-Flex will conserve additional power by disabling/enabling certain digital and analog blocks in the codec based on the audio activity.

(2) In EPSS ECR-15B, the device will be set to D4 when the system goes to S3 or S4.

(3) The supplies may remain on or off depending on the system.

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

Table 10. Device Power State Mapping

Device State (Pre-ECR 15B)	Device State (EPSS ECR 15B)	System State	Wake-up Time	Description
D0	D0	S0	--	Device is in Full Power
D1	D1, D2	S0-Idle	1 ms	Lower power standby (LP1). Transition time to full power is 1 ms.
D2	D3	S0-Idle	10 ms	Lowest power standby (LP2). Transition time to full power is 10 ms, and additional 75 ms for Full Fidelity.
			75 ms	
D3	D4	S3	200 ms	Standby, prepare for shutdown (SD). Transition time to full power 200 ms.
D3	D4	S4	200 ms	Hibernate, prepare for shutdown (SD). Transition time to full power 200 ms.

2.5.2 Power Supply Current Consumption

Table 11 shows the required voltages at the various supply input pins of the devices.

Table 11. CX20671 DC Supply Voltages

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Digital Voltage Supply	DVDD_3.3	3.165	3.3	3.465	V	
Standby Voltage Supply	VAUX_3.3	3.165	3.3	3.465	V	
HDA Bus Signaling Supply, 3.3V	VDD_IO	3.165	3.3	3.465	V	
HDA Bus Signaling Supply, 1.5 V	VDD_IO	1.425	1.5	1.575	V	
Class-D Amp Supply, Left Ch.	LPWR_5.0	4.75	5.0	5.25	V	
Class-D Amp Supply, Left Ch	RPWR_5.0	4.75	5.0	5.25	V	
Headphone Voltage Supply	AVDD_HP	3.165	3.3	3.465	V	
5V-to-3.3V Regulator Input	AVDD_5V	4.75	5.0	5.25	V	

Additionally, the following power-sequencing requirements must be met:

- For best performance of audible pop/click suppression, VAUX_3.3 supply should always ramp up before any of the other power supplies, and should ramp down after all other power supplies have ramped down. It is highly recommended that VAUX_3.3 voltage be near its final value before beginning ramp-up of AVDD_5V rail.
- DVDD_3.3 should always be present when AVDD_5V is present. If DVDD_3.3 is removed when AVDD_5V is present, the device may be damaged.

Tesis publicada con autorización del autor
No olvide citar esta tesis

- All 5 V supplies (AVDD_5V, LPWR_5.0, RPWR_5.0) can be removed while DVDD_3.3 is present.
- To support Wake-On-Jack functionality, VAUX_3.3 and VDD_IO should be powered from a power supply that is never removed (unless AC power is removed). If no such support is required, VAUX_3.3 and VDD_IO can be powered from same supply as DVDD_3.3. Sense resistors should ALWAYS use same supply as VAUX_3.3 power pin.

The current and power consumption for each of the power pins is shown in Tables 12 through 15.

Table 12. D0 (S0) Full-Duplex Power Consumption

	D0 (S0-Full Duplex)(1)		
	Pre ECR-15B Class Driver	**Pre ECR-15B CNXT Driver**	**EPSS (ECR-15B) Class Driver**
5V Class-D (mA)	1007.3	1008.01	1007.3
5V LDO (mA)	12.7	21.99	12.7
AVDD_HP (mA)	0.4	0.5	0.4
DVDD_3.3 (mA)	0.8	0.7	0.8
VDD_IO (mA)	0.031	0.061	0.031
VAUX_3.3 (mA)	48.7	46.2	48.7
Class-D Power (mW)	5036.50	5040.05	5036.50
LDO Power (mW)	21.59	37.38	21.59
Rest of the chip (mW)	206.68	229.19	206.68
Total Power (mW)	5264.77	5306.62	5264.77

FOOTNOTES:
(1) Transmitting full-scale sinewave from Class-D, recording using analog microphone.

Tesis publicada con autorización del autor
No olvide citar esta tesis

Table 13. Pre-ECR15B D-States Power Consumption With Class Driver

	Pre ECR-15B D-States (Class Driver)		
	D0 (S0-Idle)	**D3 (S3)(1)**	**D3 (S4)(1)**
5V Class-D (mA)	7.6	0.6	0
5V LDO (mA)	18.28	0.95	0
AVDD_HP (mA)	0.5	0.4	0
DVDD_3.3 (mA)	0.7	0.1	0
VDD_IO (mA)	0.035	0.007	0.000
VAUX_3.3 (mA)	46.9	2.2	0
Class-D Power (mW)	38.00	3.00	0.00
LDO Power (mW)	31.08	1.62	0.00
Rest of the chip (mW)	219.17	12.07	0.00
Total Power (mW)	288.25	16.68	0.00

FOOTNOTES:
(1) In Suspend mode (S3 or S4), the device state will be D3.

Table 14. Pre-ECR15B D-States Power Consumption With Conexant Driver

	Pre ECR-15B D-States (Conexant Driver)		
	D2 (S0-Idle)	**D3 (S3)(1)**	**D3 (S4)(1)**
5V Class-D (mA)	0.6	0.5	0
5V LDO (mA)	1.02	0.99	0
AVDD_HP (mA)	0.4	0.4	0
DVDD_3.3 (mA)	0.1	0.1	0
VDD_IO (mA)	0.036	0.007	0.000
VAUX_3.3 (mA)	6.8	2.1	0
Class-D Power (mW)	3.00	2.50	0.00
LDO Power (mW)	1.73	1.68	0.00
Rest of the chip (mW)	27.57	11.87	0.00
Total Power (mW)	32.31	16.05	0.00

FOOTNOTES:
(1) In Suspend mode (S3 or S4), the device state will be D3.

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

Table 15. EPSS ECR15B D-States Power Consumption with Conexant Driver

	EPSS ECR-15B D-States (Conexant Driver)		
	D3 (S0-Idle)(1)	D4 (S3)(2)	D4 (S4)(2)
5V Class-D (mA)	0.6	0.5	0
5V LDO (mA)	1.02	0.99	0
AVDD_HP (mA)	0.4	0.4	0
DVDD_3.3 (mA)	0.1	0.1	0
VDD_IO (mA)	0.134	0.007	0.000
VAUX_3.3 (mA)	2	2.1	0
Class-D Power (mW)	3.00	2.50	0.00
LDO Power (mW)	1.73	1.68	0.00
Rest of the chip (mW)	12.06	11.87	0.00
Total Power (mW)	16.79	16.05	0.00

FOOTNOTES:
(1) In S0-Idle mode, the device will be set to D3; BCLK is removed.
(2) In Suspend mode (S3 or S4), the device state will be D4. In S4 mode, power supplies are removed.

2.5.3 Integrated Low-Dropout Regulators

The devices feature two integrated low-dropout voltage regulators:

- A 5 V to 3.3 V regulator: The output of this voltage regulator (AVDD_3.3) can be used to power external circuitry (low-power analog for example). However, external current consumption from the regulator should be limited to no more than 30 mA. Additionally, caution should be used when powering external circuitry; use filtering (ferrite bead + capacitor, for example) to prevent the external circuitry from adding noise to the AVDD_3.3 voltage rail.
- A 3.3 V to 1.8 V regulator: The output of this voltage regulator (FILT_1.8) can also be used to power external circuitry (discrete logic, for example).

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

2.6 Integrated High-Pass Filter

The CX20671 device features a hardware digital high-pass filter, intended to be used with the class-D speaker amplifier. The cut-off frequency can be adjusted from 15 Hz to 945 Hz, in 15-Hz steps (30 Hz to1890 Hz, in 30-Hz steps for -21Z devices), depending on the value present in the appropriate 6-bit control register. Note that a setting of 000000b in the control register bypasses the filter.

By default, the high-pass filter is automatically applied to the DAC that is connected (mapped) to the class-D speaker amplifier. This “DAC tracking” mode can be disabled, and the high-pass filter can be applied to any DAC, regardless of the port connected to it. There are two ways to set the high-pass cut-off frequency:

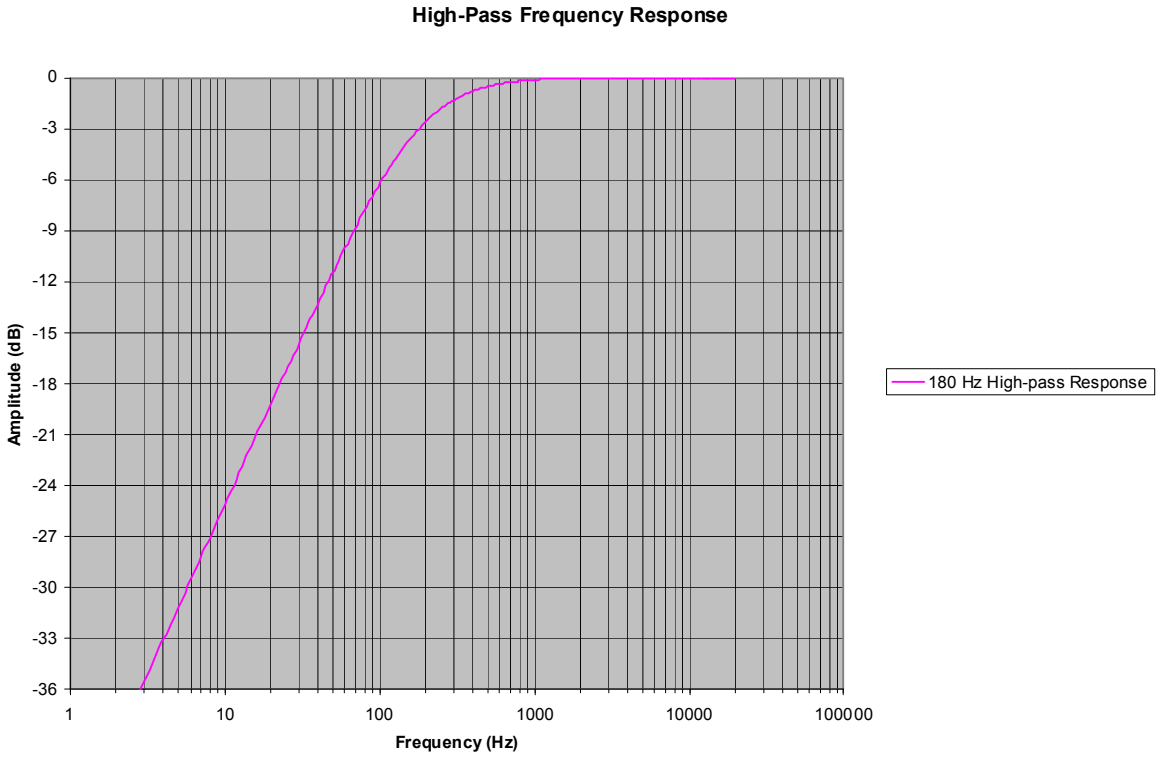
- DAC tracking mode: This is the typical mode of operation. This mode needs to be enabled, as it is not the default mode. The high-pass filter tracks the DAC that is connected to (mapped to) the class-D amplifier, but the 3 dB frequency is manually set by writing to the 6-bit control register.
- Fully manual mode: This mode needs to be enabled as it is not the default mode. The cut-off frequency can be set manually writing to the 6-bit control register. The DAC to which the filter is applied can also be selected manually by writing to the appropriate control register. Note that no typical application will use this mode.

The high-pass filter response for a specific setting is shown in the figure below. Note that, since it is a first-order filter, it rolls off at -20 dB/decade, or -6 dB/octave.

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

Figure 12. High-Pass Filter Response



The location of registers used to control the high-pass filter cut-off frequency is in Node ID 25h (-11Z devices) and Node ID 27h (-21Z devices)—the Vendor Widget. For additional details, contact Conexant for the application note.

Tesis publicada con autorización del autor
No olvide citar esta tesis

2.7 AC Timing Characteristics

2.7.1 Digital Microphone

The Conexant digital microphone interface on the CX20671 consists of a clock and data pin. The digital mic clock pin provides a 3.072 MHz clock to the digital mic. The digital mic data pin is an input, accepting multiplexed Pulse Density Modulation (PDM) data from the digital mic. Timing waveforms are illustrated in Figure 13, and timing parameters are listed in Table 16.

Contact Conexant Sales FAE for a list of qualified digital microphones.

Figure 13. Digital Mic Clock Timing Waveform

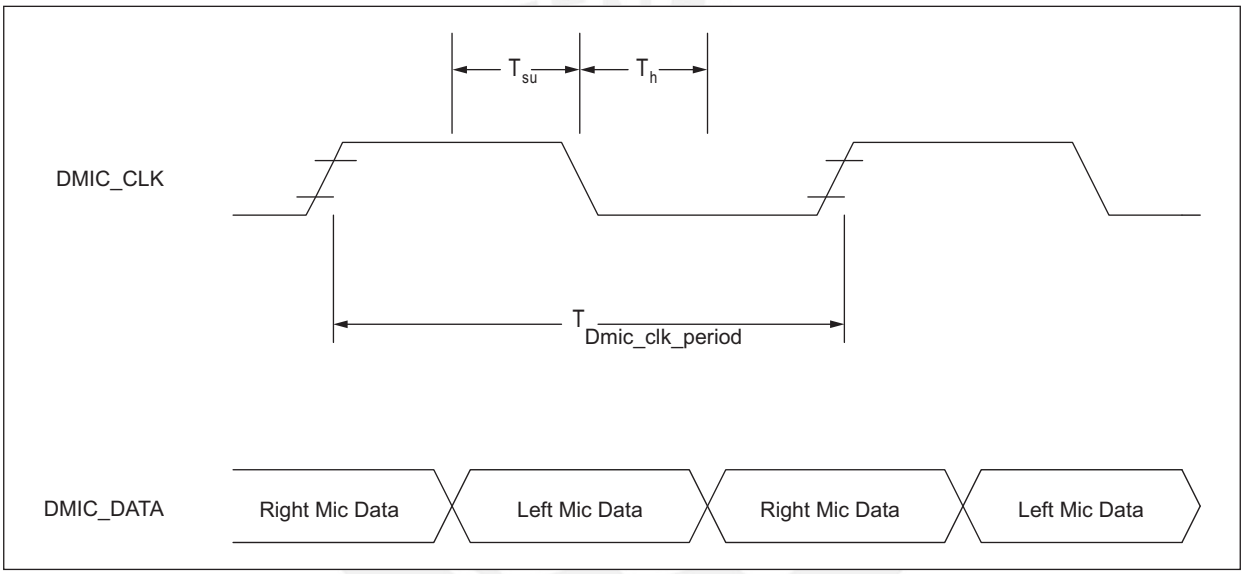


Table 16. Digital Mic Timing Parameters

Parameter	Symbol	Minimum	Typical	Maximum	Units
DMIC_CLK frequently(1)		3.0689	3.072	3.0751	MHz
DMIC_CLK period	TDmic_clk_period	325.19	325.52	325.85	ns
DMIC_CLK transition period @ 50 pF(2)		—	—	4	ns
DMIC_CLK transition period @ 20 pF(2)		—	—	1.9	ns
DMIC_CLK transition period @ 7 pF(2)		—	—	1	ns
DMIC_DATA setup time	Tsu	—	36	—	ns
DMIC_DATA hold time	Th	0	—	—	ns

FOOTNOTES:
(1) Worst case duty cycle restricted to 40/60.
(2) Measured between 25% and 75% full scale.

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

2.7.2 HD Audio Clocks

The BIT_CLK signal is a 24 MHz clock sourced from the HD Audio controller and connecting to all codecs on the link.

HD Audio clock waveforms and timing parameters are shown in Figure 14 and Table 17.

Figure 14. BIT_CLK and SYNC Timing Waveforms

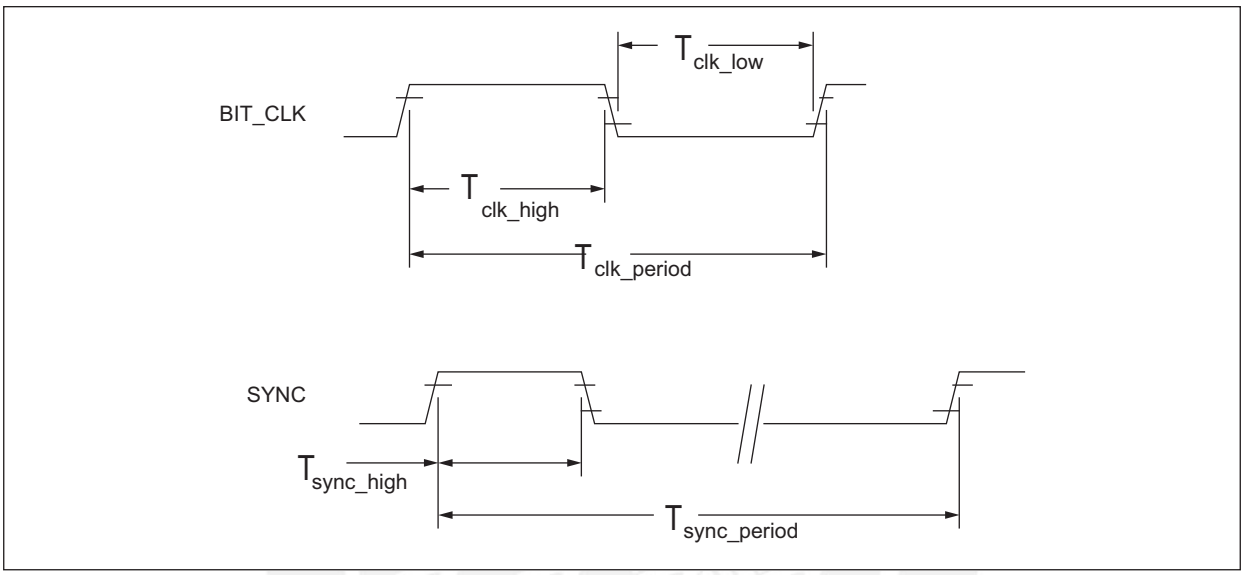


Table 17. BIT_CLK and SYNC Timing Parameters

Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK frequency		23.9976	24.0	24.0024	MHz
BIT_CLK period	Tclk_period	41.363	41.67	41.971	ns
BIT_CLK output jitter		—	150	500	Ps
BIT_CLK high pulse width (1) (2)	Tclk_high	18.75	—	22.91	ns
BIT_CLK low pulse width (1) (2)	Tclk_low	18.75	—	22.91	ns
SYNC frequency (3)		—	48	—	kHz
SYNC period	Tsync_period	—	20.8	—	µs
SYNC high pulse width	Tsync_high	—	4 x Tclk_period	—	µs

FOOTNOTES:
(1) 47.5–70 pF external load.
(2) Worst case duty cycle restricted to 40/60.
(3) The SYNC frequency is equal to the BIT_CLK frequency divided by 500.

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

2.7.3 Data Output and Input

Data output and input waveforms are illustrated in Figure 15. Timing parameters are listed in Tables 18 and 19.

Figure 15. Data Output and Input Timing Waveforms

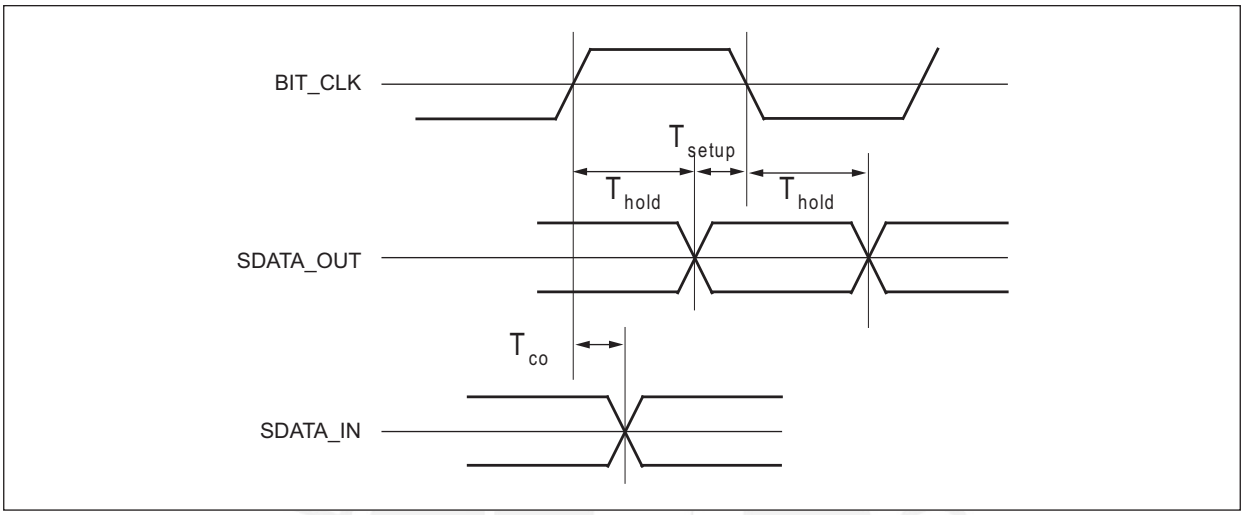


Table 18. HD Audio Output Valid Delay Timing Parameters

Parameter	Symbol	Minimum	Typical	Maximum	Units
Output Valid Delay from rising edge of BIT_CLK	Tco	3	—	11	ns
GENERAL NOTES: 1. Timing is for SDATA and SYNC outputs with respect to BIT_CLK at the device driving the output. 2. 50 pF external load.					

Table 19. HD Audio Input Setup and Hold Timing Parameters

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Setup at both rising and falling edge of BIT_CLK	Tsetup	5	—	—	ns
Input Hold at both rising and falling edge of BIT_CLK	Thold	5	—	—	ns
GENERAL NOTES: 1. Timing is for SDATA and SYNC inputs with respect to BIT_CLK at the device latching the input. 2. The CX20671 does not impose a maximum value on the system.					

Tesis publicada con autorización del autor
No olvide citar esta tesis

2.8 CX20671 Package Dimensions

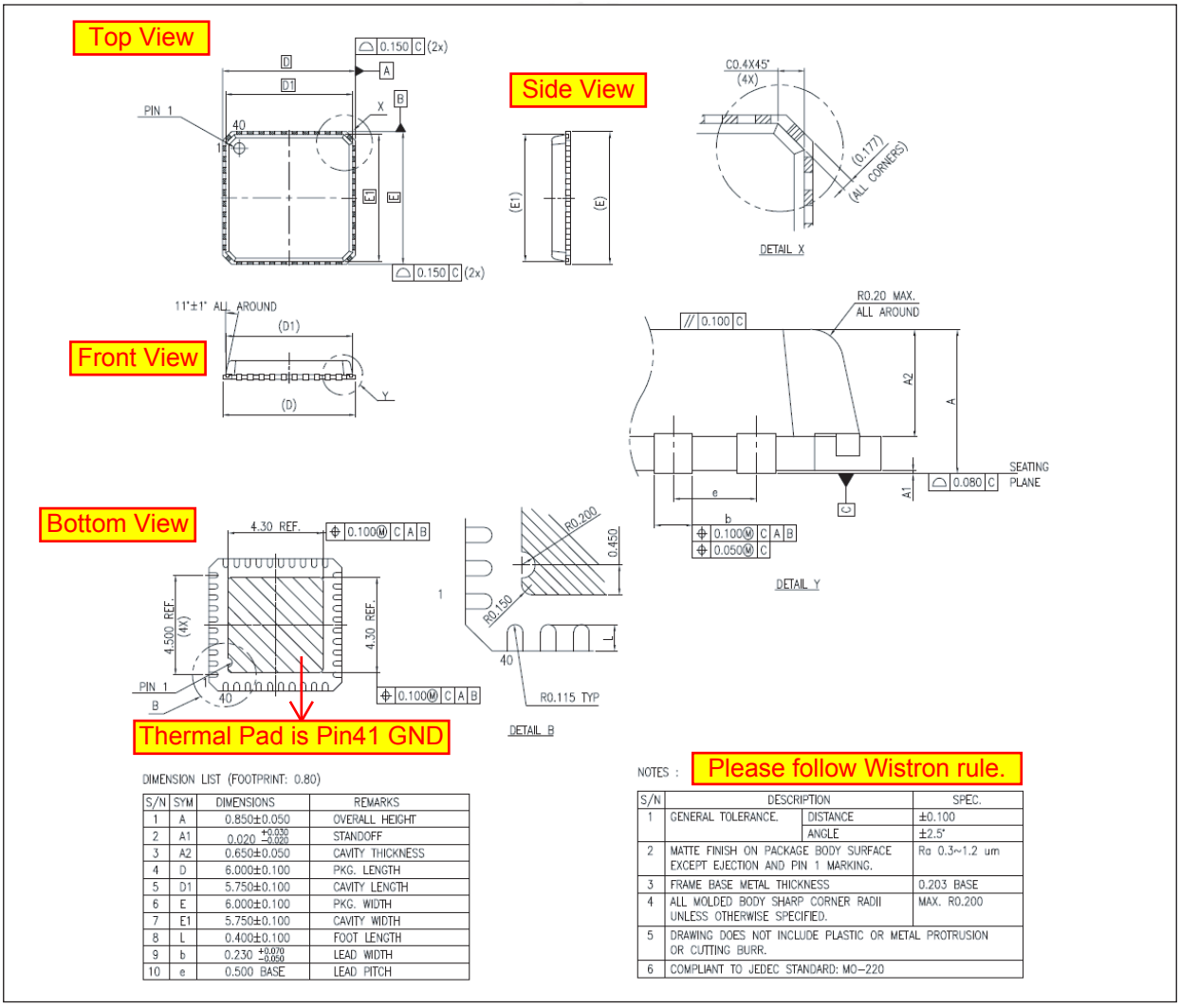
The devices are packaged as shown in Table 20.

Table 20. Package Dimensions

Device	Package Description	Package Length/Width/ Overall Height (mm)	Lead Width/Lead Pitch (mm)
CX20671	40-QFN	6.00/6.00/0.85	0.230/0.500

The package drawing for the device is shown in Figure 16.

Figure 16. CX20671 40-QFN Package Drawing



S/N	SYM	DIMENSIONS	REMARKS
1	A	0.850±0.050	OVERALL HEIGHT
2	A1	0.020 +0.030 −0.020	STANDOFF
3	A2	0.650±0.050	CAVITY THICKNESS
4	D	6.000±0.100	PKG. LENGTH
5	D1	5.750±0.100	CAVITY LENGTH
6	E	6.000±0.100	PKG. WIDTH
7	E1	5.750±0.100	CAVITY WIDTH
8	L	0.400±0.100	FOOT LENGTH
9	b	0.230 +0.070 −0.050	LEAD WIDTH
10	e	0.500 BASE	LEAD PITCH

S/N	DESCRIPTION		SPEC.
1	GENERAL TOLERANCE.	DISTANCE	±0.100
		ANGLE	±2.5°
2	MATTE FINISH ON PACKAGE BODY SURFACE EXCEPT EJECTION AND PIN 1 MARKING.		Ra 0.3~1.2 um
3	FRAME BASE METAL THICKNESS		0.203 BASE
4	ALL MOLDED BODY SHARP CORNER RADII UNLESS OTHERWISE SPECIFIED.		MAX. R0.200
5	DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OR CUTTING BURR.		
6	COMPLIANT TO JEDEC STANDARD: MO−220		

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

3 HD Audio Interface

Verbs are commands and queries that are passed from the HD Audio Controller to the codecs on the HD Audio bus. Responses are data-passed from the HD Audio codec to the HD Audio Controller. All Controller Verbs must be followed by a Codec Response, Unsolicited Responses from the codec is data transmitted without a Controller verb request.

A “1” in the Valid bit position indicates the Response Field contains a valid response. A “1” in the UnSol bit position is meaningful only when the Valid bit is set and indicates that the response is Unsolicited rather than in reply to a verb. The 32 actual response bits vary in format and are each documented in the HD Audio Specification defined by Intel.

For more information regarding verbs and Controller and Codec Command and Control protocol, refer to the HD Audio Specification from Intel Corporation.

3.1 HD Audio Interface Overview

The HD Audio interface is a 5-pin interface: Clock (BIT_CLK), serial data in (SDATA_IN), serial data out (SDATA_OUT), SYNC, and RESET#. The clock is provided by the controller at a frequency of 24 MHz. The SDATA_OUT signal is provided by the controller and contains data for every edge of the 24 MHz clock. Therefore, the CX20671 must sample data on both rising and falling edges of SDATA_OUT.

Sync not only signals the beginning of the 500 clock frame; it designates the beginning of the data for each stream and indicates which stream of data will be on SDATA_OUT next. (Streams do not need to appear in order, the controller may do as it likes.) Channels are another way of organizing the serial data. Each stream has at least one channel. Each stream must start with channel 0 and proceed without interruption until all the assigned channels are exhausted. A stereo pair takes two adjacent channels. So, if DAC1 is in stereo mode and DAC1 is assigned channel 0 then the left data will be on channel 0 and the right on channel1. If DAC2 were then assigned channel 2 and it were also stereo (and the same stream as DAC1) its left data would be on channel 2 and its right on channel 3.

SDATA_IN contains the CX20671 data headed towards the controller. It is only generated on rising edges. This includes information read from the HD Audio “registers”, ADC and incoming modem data. Stream and channel is indicated before the data is transmitted on SDATA_IN. See the HD Audio specification for that format. SDATA_IN is also responsible for knowing which device number (CAD in the HD Audio specification). During the last clock of the first sync after a power on reset, the SDATA_IN is driven high by CX20671 for one clock cycle. This indicates to the controller the need for a CAD. The CX20671 then stops driving the SDATA_IN signal and the controller begins to drive it. The controller drives SDATA_IN high through the

Tesis publicada con autorización del autor
No olvide citar esta tesis

next sync, and the CAD is assigned by the number of clocks after the fall of sync that it takes for the SDATA_IN to fall. Then, the interface turns around again, and SDATA_IN is an output from CX20671 until reset.

The HD Audio specification also contains one other concept that is worth mentioning. That is the concept of an unsolicited message. Unsolicited messages can occur for a number of reasons: timers, ringing phones, answers from the CX20548 device to a register read (etc.). Since the bus has no interrupt, these are taken care of in unsolicited messages. If the controller was not addressing the CAD assigned to the CX20671 during the previous frame, and if one of these unsolicited messages is needed (and enabled), the CX20671 will use the first cycles after the sync on SDATA_IN to alert the controller to the event. Only one event can be signaled in a frame.

The CX20671 will send the message once and only once. It does not expect any sort of acknowledgement from the controller.

3.2 Verbs

This section describes how this device interacts with the Verbs defined in the *High Definition Audio Specification revision 1.0*. Each of the following subsections describes the Verb ID's, parameters/payload, and corresponding responses that apply to that node.

Each node in the codec is addressed using a Codec Address (CAd), assigned to the codec during initialization, and the Node's Unique ID (NID). The concatenation of CAd and NID provide a unique address allowing commands to reference a single specific node within the audio subsystem.

The entire Verb is formed by pre-pending the CAd and the NID to the Verb ID and parameter/payload. In the following tables and descriptions, the CAd and NID are not listed as part of the Verb.

Register values may have up to five letters included with their default value. These letters indicate which of the possible reset events will force the register to its default value. The five resets are as follows:

- 'P' for power-on reset
- 'R' for HD Audio reset pin assertion
- 'V' for single verb reset
- W' for double verb reset
- 'D' for D-state change reset

Only the letters in the list will force the register to its default value.

Bold values in the tables below, related to Supported Power States, apply when Extended Power State Support (**EPSS**) is enabled. **EPSS** is enabled by default on -21Z devices. For -11Z devices, the indication of **EPSS** support can be enabled in the Test Registers (Vendor-defined Node 25); it is disabled by default.

Tesis publicada con autorización del autor
No olvide citar esta tesis

3.2.1 Node ID 00: Root Node

Table 21 describes a root node that has two function groups, an Audio Function Group (AFG) and a Modem Function Group (MFG).

Table 21. Root Node Parameters and Responses

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Vendor ID	F00h	00h	14F1 5069h		CX20671-11Z
Get Vendor ID	F00h	00h	14F1 506Eh		CX20671-21Z
Get Revision ID	F00h	02h	0010 0301h 0010 0000h		-11Z devices -21Z devices Supports Intel HD Audio 1.0
Get Subordinate Node Count	F00h	04h	0001 0001h		

3.2.2 Node ID 01: Audio Function Group

Table 22 describes an Audio Function Group (AFG).

Table 22. Audio Function Group Node Parameters and Responses *(1 of 3)*

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Subordinate Node Count	F00h	04h	0010 0016h		Starting Node is 10h Node count is 22
Get Function Group Type	F00h	05h	0000 0101h		Node Type is Audio Function Group UnSol Capable is 1
Get Audio Function Group Capabilities	F00h	08h	0001 0F0Fh		PC Beep generator is present Input sample delay is 0Fh Output sample delay is 0Fh
Get Supported PCM Size, Rates	F00h	0Ah	000E 0160h		16, 20, and 24 bit audio formats supported 44.1, 48, and 96 kHz sample rates supported
Get Supported Stream Formats	F00h	0Bh	0000 0001h		PCM format is supported
Get Supported Power States	F00h	0Fh	**C000 001Fh** 4000 001Fh		EPSS, clock stop, D0, D1, D2, D3, and D4 **Bold** is with EPSS supported (default for -21Z)
Get GPIO Count	F00h	11h	4000 0004h		Four (4) GPIOs with GPIOUnSol capability

Tesis publicada con autorización del autor
No olvide citar esta tesis

Table 22. Audio Function Group Node Parameters and Responses (2 of 3)

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Power State	F05h	00h	0000 0abch	0000 0633h (P,W)	Gets power state of node to which it refers a = Settings reset b = Actual power state c = Requested power state Settings reset cleared by this verb or any write to this node
Set Power State	705h	0ah	0000 0000h		Sets power state of node to which it refers a = Requested power state
Get Unsolicited Response	F08h	00h	0000 00aah	0000 0000h (P,W)	aa = Unsolicited Response enable and tag
Set Unsolicited Response	708h	aah	0000 0000h		aa = Unsolicited Response enable and tag
Get GPIO Data	F15h	00h	0000 000ah	0000 0000h (P,W)	a = GPIO data
Set GPIO Data	715h	0ah	0000 0000h		a = GPIO data
Get GPIO Enable	F16h	00h	0000 000ah	0000 0000h (P,W)	a = GPIO enable
Set GPIO Enable	716h	0ah	0000 0000h		a = GPIO enable
Get GPIO Direction	F17h	00h	0000 000ah	0000 0000h (P,W)	a = GPIO direction
Set GPIO Direction	717h	0ah	0000 0000h		a = GPIO direction
Get GPIO Unsolicited Mask Enable	F19h	00h	0000 000ah	0000 0000h (P,W)	a = UnSol Enable
Set GPIO Unsolicited Mask Enable	719h	0ah	0000 0000h		a = UnSol Enable
Get GPIO Sticky Mask	F1Ah	00h	0000 000ah	0000 0000h (P,W)	a = GPIO sticky mask
Set GPIO Sticky Mask	71Ah	0ah	0000 0000h		a = GPIO sticky mask
Get Configuration Default	F1Ch F1Dh F1Eh F1Fh	00h	aabb ccddh	0000 0000h (P)	aa = Configuration 4 bb = Configuration 3 cc = Configuration 2 dd = Configuration 1 Response is the same to all Verb IDs
Set Configuration Default 1	71Ch	aah	0000 0000h		aa = Configuration 1

Tesis publicada con autorización del autor
No olvide citar esta tesis

Table 22. Audio Function Group Node Parameters and Responses (3 of 3)

Description	Verb ID	Parameter	Response	Default Value	Comment
Set Configuration Default 2	71Dh	aah	0000 0000h		aa = Configuration 2
Set Configuration Default 3	71Eh	aah	0000 0000h		aa = Configuration 3
Set Configuration Default 4	71Fh	aah	0000 0000h		aa = Configuration 4
Get Subsystem ID	F20h F21h F22h F23h	00h	aaaa bbcch	14F1 0101h (P)	aaaa = Subsystem ID bb = SKU ID cc = Assembly ID Response is the same to all Verb IDs
Set Subsystem ID 1	720h	aah	0000 0000h		aa = Assembly ID
Set Subsystem ID 2	721h	aah	0000 0000h		aa = SKU ID
Set Subsystem ID 3	722h	aah	0000 0000h		aa = Subsystem ID low byte
Set Subsystem ID 4	723h	aah	0000 0000h		aa = Subsystem ID high byte
Function Reset	7FFh	00h	0000 0000h		Soft reset
GENERAL NOTES: The Configuration Default registers in the Audio Function Group Node are not normally used, but can be used to implement Secure Microphone function. Contact Conexant FAE/Sales to obtain additional information.					

3.2.3 Node ID 10, 11: DAC 1, DAC 2 Widget

Table 23 describes a stereo DAC that supports 16, 20, and 24 bit widths and 44.1, 48, 96, and 192 kHz sample rates.

Table 23. DAC 1, DAC2 Widget Parameters and Responses (1 of 2)

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Converter Format	Ah	0000h	0000 aaaah	0000 0011h (P,W)	aaaa = Converter format
Set Converter Format	2h	aaaah	0000 0000h		aaaa = Converter format
Get Amplifier Gain/Mute	Bh	8000h A000h	0000 00aah 0000 00bbh	0000 003Ch (P,W)	aa = Right gain bb = Left gain Bit 7 is Mute setting
Set Amplifier Gain/Mute	3h	90aah A0bbh B0cch	0000 0000h		aa = Right gain bb = Left gain cc = Right and Left gain
Get Audio Widget Capabilities	F00h	09h	0000 0C1Dh		DAC—analog
Get Supported PCM Size, Rates	F00h	0Ah	000E 0560h		16, 20, and 24 bit 44.1, 48, 96, and 192 kHz sample rate
Get Supported Stream Formats	F00h	0Bh	0000 0001h		PCM format is supported

Tesis publicada con autorización del autor
No olvide citar esta tesis

Table 23. DAC 1, DAC2 Widget Parameters and Responses (2 of 2)

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Supported Power States	F00h	0Fh	**8000 001Fh** 0000 001Fh		EPSS, D0, D1, D2, D3 and D4 **Bold** is with EPSS supported (default for -21Z)
Get Output Amplifier Capabilities	F00h	12h	8003 4A4Ah		Mute capable, 1-dB steps, step 74 is 0 dB, 74 of 80 steps exposed
Get Power State	F05h	00h	0000 0abch	0000 0433h (P, W)	a = Settings reset b = Actual state c = Requested state Settings reset cleared by this verb or any write to this node
Set Power State	705h	0ah	0000 0000h		a = Requested state
Get Converter Stream, Channel	F06h	00h	0000 00abh	0000 0000h (P, R, V, W, D)	a = Stream b = Channel
Set Converter Stream, Channel	706h	abh	0000 0000h		a = Stream b = Channel
Get EAPD Enable	F0Ch	00h	0000 000ah	0000 0000h (P, W)	a = Left/right swap
Set EAPD Enable	70Ch	0ah	0000 0000h		a = Left/right swap

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

3.2.4 Node ID 12: S/PDIF Output Widget

Table 24 describes an S/PDIF DAC that supports 16, 20, and 24 bit widths, and 44.1, 48, and 96 kHz sample rates.

Table 24. S/PDIF Output Widgets Parameters and Responses

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Converter Format	Ah	0000h	0000 aaaah	0000 0011h (P, W)	aaaa = Converter format
Set Converter Format	2h	aaaah	0000 0000h		aaaa = Converter format
Get Audio Widget Capabilities	F00h	09h	0000 0611h		DAC—digital
Get Supported PCM Size, Rates	F00h	0Ah	000E 0160h		16, 20, and 24 bit widths 44.1, 48, and 96 kHz sample rates
Get Supported Stream Formats	F00h	0Bh	0000 0005h		PCM and AC-3 formats are supported
Get Supported Power States	F00h	0Fh	**8000 001Fh** 0000 001Fh		EPSS, D0, D1, D2, D3 and D4 **Bold** is with EPSS supported (default for -21Z)
Get Power State	F05h	00h	0000 0abch	0000 0433h (P,W)	a = Settings reset b = Actual state c = Requested state Settings reset cleared by this verb or any write to this node
Set Power State	705h	0ah	0000 0000h		a = Requested state
Get Converter Stream, Channel	F06h	00h	0000 00abh	0000 0000h (P,R,V,W,D)	a = Stream b = Channel
Set Converter Stream, Channel	706h	abh	0000 0000h		a = Stream b = Channel
Get S/PDIF Converter Control	F0Dh F0Eh	00h	aabb ccddh	0000 0000h (P,W)	aa = Reserved bb = Coding mode cc = Category code dd = Header information
Set S/PDIF Converter Control 1	70Dh	aah	0000 0000h		aa = Header information
Set S/PDIF Converter Control 2	70Eh	aah	0000 0000h		aa = Category code
Set S/PDIF Converter Control 3	73Eh	aah	0000 0000h		aa = IEC coding type and Keep Alive Enable
Set S/PDIF Converter Control 4	73Fh	00h	0000 0000h		Reserved, read as 0

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

3.2.5 Node ID 13: PC Beep Generator Widget

Table 25 describes a beep generator. PC Beep is a mono signal, so writing either left, right, or both will set the single gain setting. Reading the left channel will return the current value; reading the right channel will return all zeros. Beep Generator widget's output is mixed in with all output ports.

NOTE:

The two entries under Default for “Get Amplifier Gain/Mute” are because this is a mono widget. Only the left channel request is valid. Any request, read or write, having to do with only the right channel, should be ignored and will return 0000 0000h. If both left and right are present in the request only consider the value from the left side.

This PC Beep Generator Widget is unrelated to the Analog Beep pin. Refer to the Application Note describing the Analog Beep pin.

Table 25. Beep Generator Widget Parameters and Responses

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Amplifier Gain/Mute	Bh	8000h A000h	0000 0000h 0000 00aah	0000 0000h 0000 0002h (P,W)	00 = Right gain (NA) aa = Left gain -24 dB
Set Amplifier Gain/Mute	3h	90aah A0aah B0aah	0000 0000h		aa = Right gain (NA) aa = Left gain aa = Left gain
Get Audio Widget Capabilities	F00h	09h	0070 000Ch		PC Beep Generator with output amplifier
Get PC Beep Output Amplifier Capabilities	F00h	12h	000F 0707h		4 dB steps, 8 steps, step 8 is -4 dB
Get Beep Generation	F0Ah	00h	0000 00aah	0000 0000h (P,W)	aa = Divider
Set Beep Generation	70Ah	aah	0000 0000h		aa = Divider
GENERAL NOTES: When the codec is in RESET the PC BEEP gain is -46 dB. A pull-down on SPDIF pin for -21Z devices only will set the gain to -18 dB while the codec is in RESET.					

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

3.2.6 Node ID 14, 15, and 16: ADC1, ADC2, and ADC3 Widgets

Table 26 describes a stereo ADC that supports 16-, 20-, and 24-bit widths and 44.1, 48, and 96 kHz sample rates. The ADC has a gain stage and a stereo one-of-four input selector.

Table 26. ADC Widget Parameters and Responses *(1 of 2)*

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Converter Format	Ah	0000h	0000 aaaah	0000 0011h (P,W)	aaaa = Converter format
Set Converter Format	2h	aaaah	0000 0000h		aaaa = Converter format
Get Amplifier Gain/Mute	Bh	000ah 200ah	0000 00bbh 0000 00bbh	0000 004Ah (P,W)	bb = Right amp gain/mute bb = Left amp gain/mute a = Input index (0, 1, 2, 3, or 4)
Set Amplifier Gain/Mute	3h	5abbh 6abbh 7abbh	0000 0000h		bb = Right gain/mute bb = Left gain/mute bb = Right & Left gain/ mute a = Input index (0, 1, 2, 3, or 4)
Get Audio Widget Capabilities	F00h	09h	0010 0D1Bh		Audio input, analog
Get Supported PCM Size, Rates	F00h	0Ah	000E 0160h		16, 20, and 24 bits 44.1, 48, and 96 kHz
Get Supported Stream Formats	F00h	0Bh	0000 0001h		PCM only
Get Input Amplifier Capabilities	F00h	0Dh	8003 504Ah		Mute, 1-dB steps, 80 steps, step 74 is 0 dB
Get Connection List Length	F00h	0Eh	0000 0004h		Connected to 4 widgets
Get Supported Power States	F00h	0Fh	**8000 001Fh** 0000 001Fh		EPSS, D0, D1, D2, D3 and D4 **Bold** is with EPSS supported (default for -21Z)
Get Connection Select	F01h	00h	0000 000ah	0000 0000h (P,W)	a = Connection Index
Set Connection Select	701h	0ah	0000 0000h		a = Connection Index
Get Connection List Entry	F02h	00h	2423 1817h		Four connections
Get Connection List Entry	F02h	04h	0000 0000h		Four connections

Tesis publicada con autorización del autor
No olvide citar esta tesis

Table 26. ADC Widget Parameters and Responses *(2 of 2)*

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Power Sate	F05h	00h	0000 0abch	0000 0433h (P,W)	a = Settings reset b = Actual state c = Requested state Settings reset cleared by this verb or any write to this node
Set Power State	705h	0ah	0000 0000h		a = Requested state
Get Converter Stream/Channel	F06h	00h	0000 00abh	0000 0000h (P,R,V,W,D)	a = Stream b = Channel position
Set Converter Stream/Channel	706h	abh	0000 0000h		a = Stream b = Channel position
Get EAPD/BTL	F0Ch	00h	0000 000a	0000 0000h (P,W)	a = Left/right swap
Set EAPD/BTL	70Ch	0ah	0000 0000h		a = Left/right swap

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

3.2.7 Node ID 17 and 18: Selector Widgets

Table 27. Selector Widgets Parameters and Responses

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Amplifier Gain/Mute	Bh	8000h A000h	0000 000ah 0000 000ah	0000 0000h (P,W)	a = Right gain a = Left gain
Set Amplifier Gain/Mute	3h	900ah A00ah B00ah	0000 0000h		a = Right gain a = Left gain a = Right/Left gain
Get Audio Widget Capabilities	F00h	09h	0030 050Dh		Selector with output amplifier
Get Selector Output Amplifier Capabilities	F00h	12h	0027 0400h		10-dB steps, 5 steps, step 0 is 0 dB
Get Connection List Length	F00h	0Eh	0000 0004h		Connected to 4 widgets
Get Supported Power States	F00h	0Fh	**8000 001Fh** 0000 001Fh		EPSS, D0, D1, D2, D3 and D4 **Bold** is with EPSS supported (default for -21Z)
Get Connection Select	F01h	00h	0000 000ah	0000 0000h (P,W)	Port B selected
Set Connection Select	701h	0ah	0000 0000h		0 = Port B 1 = Port C 2 = Port E 3 = Port F
Get Connection List Entry	F02h	00h	1E1D 1B1Ah		Connected to Ports B, C, E, and F
Get Power Sate	F05h	00h	0000 0abch	0000 0433 (P,W)	a = Settings reset b = Actual state c = Requested state Settings reset cleared by this verb or any write to this node
Set Power State	705h	0ah	0000 0000h		a = Requested state

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

3.2.8 Node ID 19: Port A Pin Widget

Table 28 describes a Pin Widget that has a gain stage. The Port A Pin Widget has selectable headphone or line drive and supports jack sensing.

Table 28. Port A Pin Widget Parameters and Responses *(1 of 2)*

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Audio Widget Capabilities	F00h	09h	0040 0581		Pin Widget – Analog
Get Pin Capabilities	F00h	0Ch	0000 001Ch		Output, HP, sense (Port A)
Get Connection List Length	F00h	0Eh	0000 0002h		Connected to 2 widgets
Get Supported Power States	F00h	0Fh	**8000 001Fh** 0000 001Fh		EPSS, D0, D1, D2, D3 and D4 **Bold** is with EPSS supported (default for -21Z)
Get Connection Select	F01h	00h	0000 000ah	0000 0000h (P,W)	DAC1 selected
Set Connection Select	701h	0ah	0000 0000h		0 = DAC1 1 = DAC2
Get Connection List Entry	F02h	00h	0000 1110h		DAC1, DAC2
Get Power Sate	F05h	00h	0000 0abch	0000 0433 (P,W)	a = Settings reset b = Actual state c = Requested state Settings reset cleared by this verb or any write to this node
Set Power State	705h	0ah	0000 0000h		a = Requested state
Get Pin Widget Control	F07h	00h	0000 00a0h	0000 0000h (P,W)	a = Headphone and output enable
Set Pin Widget Control	707h	a0h	0000 0000h		a = Headphone and output enable
Get Unsolicited Response	F08h	00h	0000 00aah	0000 0000h (P,W)	aa = Unsolicited enable and tag
Set Unsolicited Response	708h	aah	0000 0000h		aa = Unsolicited enable and tag
Get Pin Sense	F09h	00h	aFFF FFFF		a = Presence detect (bit 31) F = present, 7 = missing

Tesis publicada con autorización del autor
No olvide citar esta tesis

Table 28. Port A Pin Widget Parameters and Responses (2 of 2)

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Configuration Default	F1Ch F1Dh F1Eh F1Fh	00h	aabb ccddh	Node 19: 0421 401Fh (P)	aa = Configuration 4 bb = Configuration 3 cc = Configuration 2 dd = Configuration 1 Response is the same to all Verb IDs
Set Configuration Default 1	71Ch	aah	0000 0000h		aa = Configuration 1
Set Configuration Default 2	71Dh	aah	0000 0000h		aa = Configuration 2
Set Configuration Default 3	71Eh	aah	0000 0000h		aa = Configuration 3
Set Configuration Default 4	71Fh	aah	0000 0000h		aa = Configuration 4

3.2.9 Node ID 1A: Port B Widget

Table 29 describes a stereo input Pin Widget that can be configured to be a line input or microphone input. There is a microphone boost control and microphone bias. This Pin Widget supports jack sensing.

Table 29. Port B Pin Widget Parameters and Responses (1 of 2)

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Audio Widget Capabilities	F00h	09h	0040 0481h		Pin Widget – Analog
Get Pin Capabilities	F00h	0Ch	0000 1324h		Vref, input, jack sense
Get Supported Power States	F00h	0Fh	**8000 001Fh** 0000 001Fh		EPSS, D0, D1, D2, D3 and D4 **Bold** is with EPSS supported (default for -21Z)
Get Power Sate	F05h	00h	0000 0abch	0000 0433 (P,W)	a = Settings reset b = Actual state c = Requested state Settings reset cleared by this verb or any write to this node
Set Power State	705h	0ah	0000 0000h		a = Requested state
Get Pin Widget Control	F07h	00h	0000 00aah	0000 0000h (P,W)	a = Vref, input enable
Set Pin Widget Control	707h	aah	0000 0000h		a = Vref, input enable
Get Unsolicited Response	F08h	00h	0000 00aah	0000 0000h (P,W)	aa = Unsolicited enable and tag

Tesis publicada con autorización del autor
No olvide citar esta tesis

Table 29. Port B Pin Widget Parameters and Responses *(2 of 2)*

Description	Verb ID	Parameter	Response	Default Value	Comment
Set Unsolicited Response	708h	aah	0000 0000h		aa = Unsolicited enable and tag
Get Pin Sense	F09h	00h	aFFF FFFF		a = Presence detect (bit 31) F = present, 7 = missing
Get Configuration Default	F1Ch F1Dh F1Eh F1Fh	00h	aabb ccddh	04A1 902Eh (P)	aa = Configuration 4 bb = Configuration 3 cc = Configuration 2 dd = Configuration 1 Response is the same to all Verb IDs
Set Configuration Default 1	71Ch	aah	0000 0000h		aa = Configuration 1
Set Configuration Default 2	71Dh	aah	0000 0000h		aa = Configuration 2
Set Configuration Default 3	71Eh	aah	0000 0000h		aa = Configuration 3
Set Configuration Default 4	71Fh	aah	0000 0000h		aa = Configuration 4

Tesis publicada con autorización del autor
No olvide citar esta tesis

3.2.10 Node ID 1B: Port C Widget

Table 30 describes a stereo input Pin Widget that can be configured to be a line input, microphone input, or line output. There is a microphone boost control and microphone bias. This Pin Widget supports jack sensing.

NOTE: The EAPD pin is shared with GPIO_0. In order for the EAPD to be active, GPIO_0 must have its enable bit set to 0, which disables GPIO_0.

Table 30. Port C Pin Widget Parameters and Responses *(1 of 2)*

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Audio Widget Capabilities	F00h	09h	0040 0581h		Pin Widget – Analog
Get Pin Capabilities	F00h	0Ch	0001 1334h		EAPD, Vref, input, output, jack sense
Get Connection List Length	F00h	0Eh	0000 0002h		Connected to 2 widgets
Get Supported Power States	F00h	0Fh	**8000 001Fh** 0000 001Fh		EPSS, D0, D1, D2, D3 and D4 **Bold** is with EPSS supported (default for -21Z)
Get Connection Select	F01h	00h	0000 000ah	0000 0000h (P,W)	DAC1 selected
Set Connection Select	701h	0ah	0000 0000h		0 = DAC1 1 = DAC2
Get Connection List Entry	F02h	00h	0000 1110h		DAC1, DAC2
Get Power Sate	F05h	00h	0000 0abch	0000 0433 (P,W)	a = Settings reset b = Actual state c = Requested state Settings reset cleared by this verb or any write to this node
Set Power State	705h	0ah	0000 0000h		a = Requested state
Get Pin Widget Control	F07h	00h	0000 00aah	0000 0000h (P,W)	aa = Vref, input, output enable
Set Pin Widget Control	707h	aah	0000 0000h		aa = Vref, input, output enable
Get Unsolicited Response	F08h	00h	0000 00aah	0000 0000h (P,W)	aa = Unsolicited enable and tag
Set Unsolicited Response	708h	aah	0000 0000h		aa = Unsolicited enable and tag
Get Pin Sense	F09h	00h	aFFF FFFF		a = Presence detect (bit 31) F = present, 7 = missing

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

Table 30. Port C Pin Widget Parameters and Responses *(2 of 2)*

Description	Verb ID	Parameter	Response	Default Value	Comment
Get EAPD/BTL	F0Ch	00h	0000 000ah	0000 0000h (P,W)	a = EAPD
Set EAPD/BTL	70Ch	0ah	0000 0000h		a = EAPD
Get Configuration Default	F1Ch F1Dh F1Eh F1Fh	00h	aabb ccddh	21A1 90F0h (P)	aa = Configuration 4 bb = Configuration 3 cc = Configuration 2 dd = Configuration 1 Response is the same to all Verb IDs
Set Configuration Default 1	71Ch	aah	0000 0000h		aa = Configuration 1
Set Configuration Default 2	71Dh	aah	0000 0000h		aa = Configuration 2
Set Configuration Default 3	71Eh	aah	0000 0000h		aa = Configuration 3
Set Configuration Default 4	71Fh	aah	0000 0000h		aa = Configuration 4

Tesis publicada con autorización del autor
No olvide citar esta tesis

3.2.11 Node ID 20: Port H, S/PDIF Digital Pin Widget

The following table describes a digital output Pin Widget with jack sense.

NOTE: The two entries in "Get Pin Capabilities" are controlled by an HDMI enable bit in the Vendor Test Node (25). Power-on reset will default the HDMI bit to be off (top entry). Writing a 1 to the test bit will add the HDMI indication to the pin capabilities.

Setting the Pin Widget output enable to 0 (disable output) should act as if the S/PDIF Vcfg bit was set to 0 and the V bit set to 1. This "mutes" the transmitter by marking all the data as invalid. But the S/PDIF clock, header, and data must still be sent. Setting the Pin Widget output enable to 1 allows the transmitter to behave as requested by the V and Vcfg bits.

Table 31. S/PDIF Pin Widgets Parameters and Responses *(1 of 2)*

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Audio Widget Capabilities	F00h	09h	0040 0781h		Pin Widget – Digital with jack sense
Get Pin Capabilities	F00h	0Ch	0000 0014h		Both nodes are output only
Get Connection List Length	F00h	0Eh	0000 0001h		Connected to 1 widget
Get Supported Power States	F00h	0Fh	**8000 001Fh** 0000 001Fh		EPSS, D0, D1, D2, D3 and D4 **Bold** is with EPSS supported (default for -21Z)
Get Connection List Entry	F02h	00h	0000 0012h 0000 0021h		S/PDIF1 S/PDIF2
Get Power Sate	F05h	00h	0000 0abch	0000 0433 (P,W)	a = Settings reset b = Actual state c = Requested state Settings reset cleared by this verb or any write to this node
Set Power State	705h	0ah	0000 0000h		a = Requested state
Get Pin Widget Control	F07h	00h	0000 00a0h	0000 0000h (P,W)	a = Output enable
Set Pin Widget Control	707h	a0h	0000 0000h		a = Output enable
Get Unsolicited Response	F08h	00h	0000 00aah	0000 0000h (P,W)	aa = Unsolicited enable and tag
Set Unsolicited Response	708h	aah	0000 0000h		aa = Unsolicited enable and tag

Tesis publicada con autorización del autor
No olvide citar esta tesis

Table 31. S/PDIF Pin Widgets Parameters and Responses *(2 of 2)*

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Pin Sense	F09h	00h	aFFF FFFF		a = Presence detect (bit 31) F = present, 7 = missing
Get Configuration Default	F1Ch F1Dh F1Eh F1Fh	00h	aabb ccddh	Node 20: 0445 71F0h (P)	aa = Configuration 4 bb = Configuration 3 cc = Configuration 2 dd = Configuration 1 Response is the same to all Verb ID's
Set Configuration Default 1	71Ch	aah	0000 0000h		aa = Configuration 1
Set Configuration Default 2	71Dh	aah	0000 0000h		aa = Configuration 2
Set Configuration Default 3	71Eh	aah	0000 0000h		aa = Configuration 3
Set Configuration Default 4	71Fh	aah	0000 0000h		aa = Configuration 4

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

3.2.12 Node ID 23: Port J Digital Microphone Widget

Table 32 describes a stereo microphone Pin Widget.

Table 32. Port J Pin Widget Parameters and Responses

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Amplifier Gain/Mute	Bh	0000h 2000h	0000 00aah 0000 00aah	0000 0000h (P,W)	aa = Right gain aa = Left gain
Set Amplifier Gain/Mute	3h	50aah 60aah 70aah	0000 0000h		aa = Right gain aa = Left gain aa = Right/Left gain
Get Audio Widget Capabilities	F00h	09h	0040 040Bh		Pin Widget – Analog
Get Pin Capabilities	F00h	0Ch	0000 0020h		Input only
Get Input Amplifier Capabilities	F00h	0Dh	002F 0400h		12-dB steps, 5 steps, step 0 is 0 dB
Get Supported Power States	F00h	0Fh	**8000 001Fh** 0000 001Fh		EPSS, D0, D1, D2, D3 and D4 **Bold** is with EPSS supported (default for -21Z)
Get Power State	F05h	00h	0000 0abch	0000 0433 (P,W)	a = Settings reset b = Actual state c = Requested state Settings reset cleared by this verb or any write to this node
Set Power State	705h	0ah	0000 0000h		a = Requested state
Get Pin Widget Control	F07h	00h	0000 00a0h	0000 0000h (P,W)	a = Input enable
Set Pin Widget Control	707h	a0h	0000 0000h		a = Input enable
Get Configuration Default	F1Ch F1Dh F1Eh F1Fh	00h	aabb ccddh	90A7 00F0h (P)	aa = Configuration 4 bb = Configuration 3 cc = Configuration 2 dd = Configuration 1 Response is the same to all Verb IDs
Set Configuration Default 1	71Ch	aah	0000 0000h		aa = Configuration 1
Set Configuration Default 2	71Dh	aah	0000 0000h		aa = Configuration 2
Set Configuration Default 3	71Eh	aah	0000 0000h		aa = Configuration 3
Set Configuration Default 4	71Fh	aah	0000 0000h		aa = Configuration 4

Tesis publicada con autorización del autor
No olvide citar esta tesis

3.2.13 Node ID 1F: Port G Widget

Table 33 describes a Pin Widget that is a dedicated stereo speaker driver.

Table 33. Port G Pin Widget Parameters and Responses

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Audio Widget Capabilities	F00h	09h	0040 0501h		Pin Widget – Analog
Get Pin Capabilities	F00h	0Ch	0000 0010h		Output only
Get Connection List Length	F00h	0Eh	0000 0002h		Connected to 2 widgets
Get Supported Power States	F00h	0Fh	**8000 001Fh** 0000 001Fh		EPSS, D0, D1, D2, D3 and D4 **Bold** is with EPSS supported (default for -21Z)
Get Connection Select	F01h	00h	0000 000ah	0000 0000h (P,W)	DAC1 selected
Set Connection Select	701h	0ah	0000 0000h		0 = DAC1 1 = DAC2
Get Connection List Entry	F02h	00h	0000 1110h		Connected to DAC1, DAC2
Get Power Sate	F05h	00h	0000 0abch	0000 0433 (P,W)	a = Settings reset b = Actual state c = Requested state Settings reset cleared by this verb or any write to this node
Set Power State	705h	0ah	0000 0000h		a = Requested state
Get Pin Widget Control	F07h	00h	0000 00a0h	0000 0040h (P,W)	a = Output enable
Set Pin Widget Control	707h	a0h	0000 0000h		a = Output enable
Get Configuration Default	F1Ch F1Dh F1Eh F1Fh	00h	aabb ccddh	9017 0010h (P)	aa = Configuration 4 bb = Configuration 3 cc = Configuration 2 dd = Configuration 1 Response is the same to all Verb IDs
Set Configuration Default 1	71Ch	aah	0000 0000h		aa = Configuration 1
Set Configuration Default 2	71Dh	aah	0000 0000h		aa = Configuration 2
Set Configuration Default 3	71Eh	aah	0000 0000h		aa = Configuration 3
Set Configuration Default 4	71Fh	aah	0000 0000h		aa = Configuration 4

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

3.2.14 Node ID 24: Mixer Widget

Table 34 describes a Mixer (Summing) Widget.

Table 34. Mixer Widget Parameters and Responses

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Amplifier Gain/Mute	Bh	000ah 200ah	0000 00bbh 0000 00bbh	0000 0000h (P,W)	bb = Right amp gain/mute bb = Left amp gain/mute a = Input index (0, 1, or 2)
Set Amplifier Gain/Mute	3h	5abbh 6abbh 7abbh	0000 0000h		bb = Right gain/mute bb = Left gain/mute bb = Right & Left gain/ mute a = Input index (0, 1, or 2)
Get Audio Widget Capabilities	F00h	09h	0020 050Bh		Mixer with input amplifier
Get Input Amplifier Capabilities	F00h	0Dh	8003 4A4Ah		Mute, 1-dB steps, 74 steps, step 74 is 0 dB
Get Connection List Length	F00h	0Eh	0000 0002h		Connected to 2 widgets
Get Supported Power States	F00h	0Fh	**8000 001Fh** 0000 001Fh		EPSS, D0, D1, D2, D3 and D4 **Bold** is with EPSS supported (default for -21Z)
Get Connection List Entry	F02h	00h	0000 1110h		Connected to DAC1, DAC2
Get Power Sate	F05h	00h	0000 0abch	0000 0433 (P,W)	a = Settings reset b = Actual state c = Requested state Settings reset cleared by this verb or any write to this node
Set Power State	705h	0ah	0000 0000h		a = Requested state

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

3.2.15 Node ID 25, 27: Vendor (Device Test) Widgets

Table 35 describes a Vendor Widget. This node is used for software support and device testing. Contact Conexant FAE/Sales to get additional documentation describing the contents and usage of the registers contained here.

Table 35. Vendor (Device Test) Widget Parameters and Responses

Description	Verb ID	Parameter	Response	Default Value	Comment
Get Timer	900h	00h	0000 00aah	0000 0000h (P,W)	aa = Bus timer value
Get Timer	100h	aah	0000 0000h		aa = Bus timer value
Get Test Codec	Ah	a000h	0000 0bbbh	0000 0000h (P)	a = Register number bbb = 12-bit value
Set Test Codec	2h	abbbh	0000 0000h		a = Register number bbb = 12-bit value
Get Test Analog	Bh	a000h	0000 0bbbh	0000 0000h (P)	a = Register number bbb = 12-bit value
Set Test Analog	3h	abbbh	0000 0000h		a = Register number bbb = 12-bit value
Get Test Digital	Ch	a000h	0000 0bbbh	0000 0000h (P)	a = Register number bbb = 12-bit value
Set Test Digital	4h	abbbh	0000 0000h		a = Register number bbb = 12-bit value
Get Audio Widget Capabilities	F00h	09h	00F0 0000h		Type is vendor-defined widget

Tesis publicada con autorización del autor
No olvide citar esta tesis

3.3 Unsolicited Messages

3.3.1 Audio Unsolicited Messages

Table 37 describes all possible bit coding and sources of unsolicited messages for the audio function group. The “Tag” comes from the unsolicited message tag stored in the node that generated the event.

Table 36. Audio Unsolicited Messages Tag Fields

[31:26]	[25:4]	[3:0]
Tag	Res	data

Table 37. Audio Unsolicited Messages Bit Coding and Sources

Tag ID	Data:3	Data:2	Data:1	Data:0	Description
Node 1	Bus Timer	—	GPIO 1 change	GPIO 0 change	
Node 19	0	0	0	Jack change	0 = jack removed 1 = jack inserted
Node 1A	0	0	0	Jack change	0 = jack removed 1 = jack inserted
Node 1B	0	0	0	Jack change	0 = jack removed 1 = jack inserted

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

www.conexant.com
General Information:
U.S. and Canada: (888) 855-4562
International: (949) 483-4600
Headquarters – Newport Beach
4000 MacArthur Blvd.
Newport Beach, CA 92660

CONEXANT®

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

Lenovo® G460 (0677) - Windows 7 (web only models)

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ
Personal Systems Reference (PSREF)

Type-model	Pro-cessor	GHz	Max turbo (GHz)	Memory	Widescreen display	Cam-era	Graphics	SATA disk	SATA optical	PCIe Mini Card 802.11	Top color	HDMI con-nector	Blue-tooth	Battery cells	Win7 preload	Avail date
0677-9UU	i3-380M	2.53		*4GB*	14.0" HD	0.3M	Intel HD	500GB[8]	DVD±RW	11b/g/n[28]	Black	HDMI	Blue	6-cell	Prem 64	Dec 10
0677-9XU	i5-480M	2.66		*4GB*	14.0" HD	0.3M	Intel HD	500GB	DVD±RW	11b/g/n	Black	HDMI	Blue	6-cell	Prem 64	Dec 10

- ***14.0" widescreen, glossy display***
- ***Integrated 0.3 megapixel camera and Lenovo's VeriFace facial recognition software helps control access to your notebook by recognizing your face***
- ***Lenovo Rescue System provides OneKey recovery and OneKey Antivirus without booting into Windows***
- ***This system is Microsoft® Office 2010 Product Key Ready (O10PKR)***

Positioning	*Widescreen flexibility; two-spindle*
Processo	**Intel® Core™ i3 processor i3-380M** with **dual-core**, DMI (Direct Media Interface), integrated DDR3 memory controller (up to 1066MHz), Hyper-Threading technology, and 3MB cache **Intel Core i5 processor i5-480M** with **dual-core**, DMI (Direct Media Interface), integrated DDR3 memory controller (up to 1066MHz), Intel Turbo Boost, Hyper-Threading technology, and 3MB cache
Memory	**4GB** std / 8GB max[7] / **PC3-8500 1066MHz DDR3**, non-parity, dual-channel capable, two 204-pin SO-DIMM sockets; *Italics: 2GB* standard memory in both sockets; no sockets available
Diskette drive	None
SATA DVD±RW	DVD burner, dual-layer support, fixed, not removable, 12.7mm high, tray-in
SATA disk	**500GB** (5400 rpm), or **750GB** (5400 rpm) / SATA 2.0Gb/s, 9.5mm high
Widescreen display	**14.0"** (355.6mm) **HD (1366x768) TFT color**, **VibrantView** (glossy), **LED backlight,** 220 nits, 16:9 aspect ratio, 500:1 contrast ratio
Camera	Camera on top of screen, 0.3-megapixel, fixed focus
Graphics	*Some:* **Intel HD Graphics in processor,** *external analog monitor support via VGA DB-15 connector and* digital monitor support via HDMI connector
Keyboard	Full-size keyboard, multimedia Fn keys, recovery key
Numeric keypad	None
Touch controls	OneKey Theater, mute, volume up, and volume down buttons
Touch pad	Two-button touch pad with scroll feature (no TrackPoint®)
Dimensions[3]	*(WxDxH):* 13.4" x 9.13" x 0.68" to 1.35"; 340.0mm x 231.8mm x 17.2 to 34.4mm
Weight[2]	with optical drive and battery: *6-cell:* from 4.85 lb (2.2kg)
Case color	Black top, black bottom
Case material	Polycarbonate/Acrylonitrile-Butadiene-Styrene (PC/ABS) plastic
Battery - type	Lithium Ion **6-cell**
Battery - life[10]	*Discrete models:* up to 3.5 hr; *Integrated models:* up to 4 hr
Chipset	**Mobile Intel HM55 Express Chipset**
ExpressCard/34	One slot (ExpressCard/34)
Multicard reader	5-in-1 reader (MMC, Memory Stick®, Memory Stick PRO™, Secure Digital Card, xD-Picture Card™)
Ports	Two USB 2.0, one USB 2.0/eSATA combo port, external monitor (VGA DB-15, HDMI), ethernet (RJ-45)
TV tuner	None
PCIe Mini Card 11b/g/n[28]	One PCI Express Mini Card slot 11b/g/n wireless[4], PCIe Mini Card adapter
Bluetooth™	Bluetooth 2.1 wireless, USB 2.0 interface
Modem	None
Ethernet	10/100 ethernet, RealTek® RTL8103EL
Audio support	High Definition (HD) Audio, Conexant® CX20671 codec / stereo speakers (2 watt x 2) / microphone, microphone input jack (3.5 mm), headphone jack (3.5 mm)
Security	Power-on password, hard disk password, supervisor password, security lockhole
Fingerprint reader	None

Preloaded operating system[20]
- Genuine Windows® 7 Home Premium 64

Preloaded applications[14] (only some listed)
- Lenovo OneKey Recovery
- Lenovo ReadyComm
- ooVoo™
- McAfee® VirusScan® Plus (60 days of virus definitions)
- Adobe® Reader®
- CyberLink YouCam
- Microsoft Office 2010 preloaded; purchase product key to activate
- VeriFace™
- Lenovo Energy Management Software
- Lenovo DirectShare
- Cyberlink Power2Go (DVD±RW)

65-watt AC adapter
Wireless on/off switch
ENERGY STAR® 5.0-compliant
RoHS-compliant

Limited Warranty[12]

- **1-year warranty*:**
  *** 1- year on major electronic components (including battery), 90-day on keyboard, hinges, plastics, power cord, AC adapter**
- **Mail In repair service**
- **Service upgrade options**[58] **(in eligible locations):**[9]
  - **3-year Depot warranty** 78Y1538
  - **1-year Mail In with accidental damage protection** 55Y2511
  - **3-year Mail In with accidental damage protection** 78Y1539
  - **3-year Onsite warranty** 78Y1540
  - **1-year Onsite with accidental damage protection** 78Y1533
- **Toll-free support for warranty issues during the warranty period**[12] **via 877-453-6686**

See footnotes for important warranty information
US models announced December 1, 2010

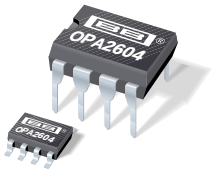
© Lenovo
(EFL1-1) February 2011

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

BURR - BROWN®



OPA2604

www.burr-brown.com/databook/OPA2604.html

Dual FET-Input, Low Distortion OPERATIONAL AMPLIFIER

FEATURES

- LOW DISTORTION: 0.0003% at 1kHz
- LOW NOISE: 10nV/√Hz
- HIGH SLEW RATE: 25V/μs
- WIDE GAIN-BANDWIDTH: 20MHz
- UNITY-GAIN STABLE
- WIDE SUPPLY RANGE: V_S = ±4.5 to ±24V
- DRIVES 600Ω LOADS

APPLICATIONS

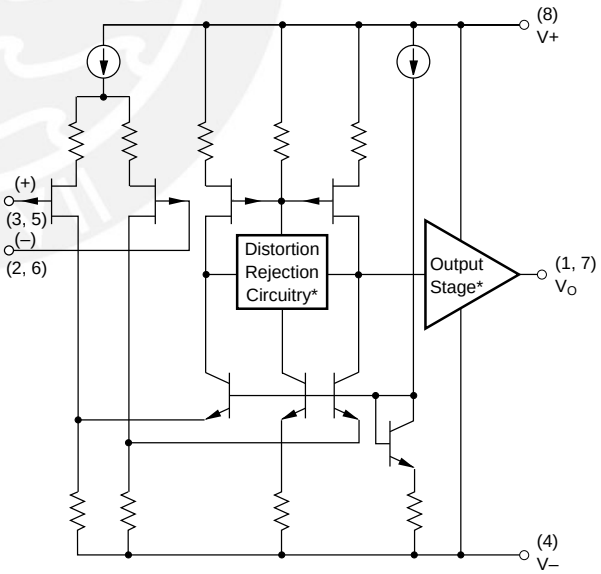
- PROFESSIONAL AUDIO EQUIPMENT
- PCM DAC I/V CONVERTER
- SPECTRAL ANALYSIS EQUIPMENT
- ACTIVE FILTERS
- TRANSDUCER AMPLIFIER
- DATA ACQUISITION

DESCRIPTION

The OPA2604 is a dual, FET-input operational amplifier designed for enhanced AC performance. Very low distortion, low noise and wide bandwidth provide superior performance in high quality audio and other applications requiring excellent dynamic performance.

New circuit techniques and special laser trimming of dynamic circuit performance yield very low harmonic distortion. The result is an op amp with exceptional sound quality. The low-noise FET input of the OPA2604 provides wide dynamic range, even with high source impedance. Offset voltage is laser-trimmed to minimize the need for interstage coupling capacitors.

The OPA2604 is available in 8-pin plastic mini-DIP and SO-8 surface-mount packages, specified for the –25°C to +85°C temperature range.



* Patents Granted:
#5053718, 5019789

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

© 1991 Burr-Brown Corporation
PDS-1069E
Printed in U.S.A. October, 1997

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

PARAMETER	CONDITION	OPA2604AP, AU MIN	OPA2604AP, AU TYP	OPA2604AP, AU MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage			±1	±5	mV
Average Drift			±8		µV/°C
Power Supply Rejection	V_S = ±5 to ±24V	70	80		dB
INPUT BIAS CURRENT(1)					
Input Bias Current	V_{CM} = 0V		100		pA
Input Offset Current	V_{CM} = 0V		±4		pA
NOISE					
Input Voltage Noise					
Noise Density: f = 10Hz			25		nV/√Hz
f = 100Hz			15		nV/√Hz
f = 1kHz			11		nV/√Hz
f = 10kHz			10		nV/√Hz
Voltage Noise, BW = 20Hz to 20kHz			1.5		µVp-p
Input Bias Current Noise					
Current Noise Density, f = 0.1Hz to 20kHz			6		fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range		±12	±13		V
Common-Mode Rejection	V_{CM} = ±12V	80	100		dB
INPUT IMPEDANCE					
Differential			10^{12} || 8		Ω || pF
Common-Mode			10^{12} || 10		Ω || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = ±10V, R_L = 1kΩ	80	100		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product	G = 100		20		MHz
Slew Rate	20Vp-p, R_L = 1kΩ	15	25		V/µs
Settling Time: 0.01%	G = –1, 10V Step		1.5		µs
0.1%			1		µs
Total Harmonic Distortion + Noise (THD+N)	G = 1, f = 1kHz		0.0003		%
	V_O = 3.5Vrms, R_L = 1kΩ				
Channel Separation	f = 1kHz, R_L = 1kΩ		142		dB
OUTPUT					
Voltage Output	R_L = 600Ω	±11	±12		V
Current Output	V_O = ±12V		±35		mA
Short Circuit Current			±40		mA
Output Resistance, Open-Loop			25		Ω
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±4.5		±24	V
Current, Total Both Amplifiers	I_O = 0		±10.5	±12	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Storage		–40		+125	°C
Thermal Resistance(2), θ_{JA}			90		°C/W

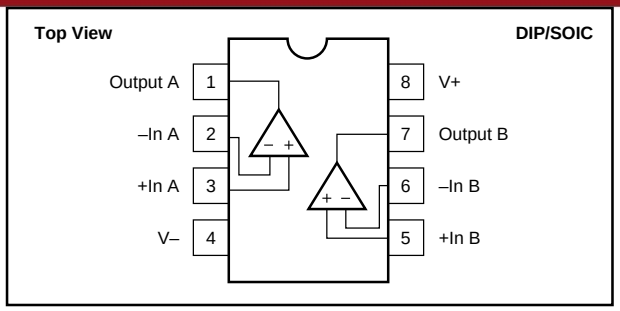
NOTES: (1) Typical performance, measured fully warmed-up. (2) Soldered to circuit board—see text.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PIN CONFIGURATION



ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Power Supply Voltage	±25V
Input Voltage	(V–)–1V to (V+)+1V
Output Short Circuit to Ground	Continuous
Operating Temperature	–40°C to +100°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s) AP	+300°C
Lead Temperature (soldering, 3s) AU	+260°C

NOTE: (1) Stresses above these ratings may cause permanent damage.

ORDERING INFORMATION

PRODUCT	PACKAGE	TEMP. RANGE
OPA2604AP	8-Pin Plastic DIP	–25°C to +85°C
OPA2604AU	SO-8 Surface-Mount	–25°C to +85°C

PACKAGING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA2604AP	8-Pin Plastic DIP	006
OPA2604AU	SO-8 Surface-Mount	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

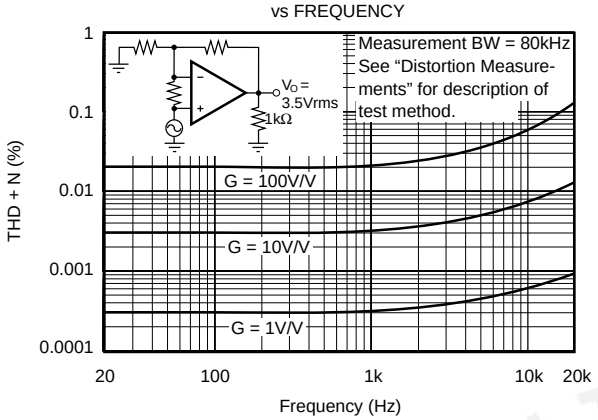
Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

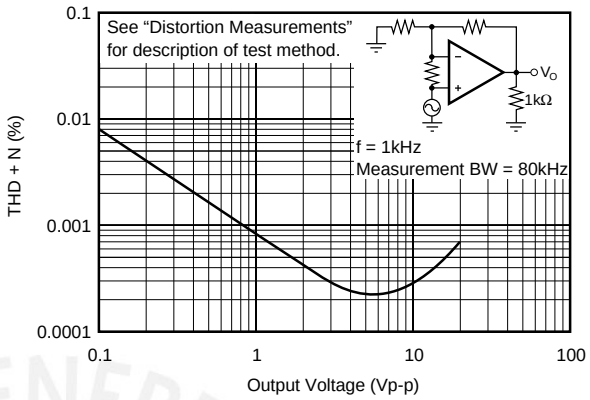
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

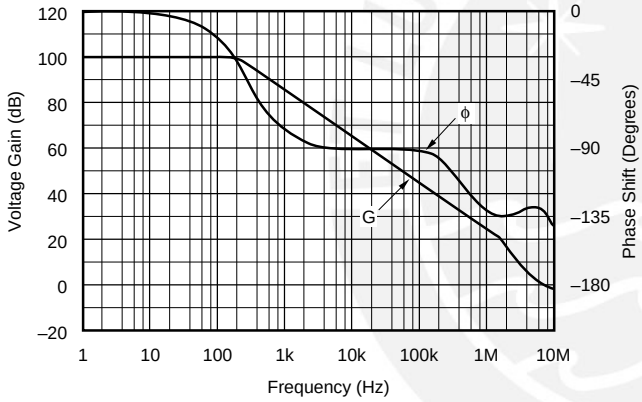
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



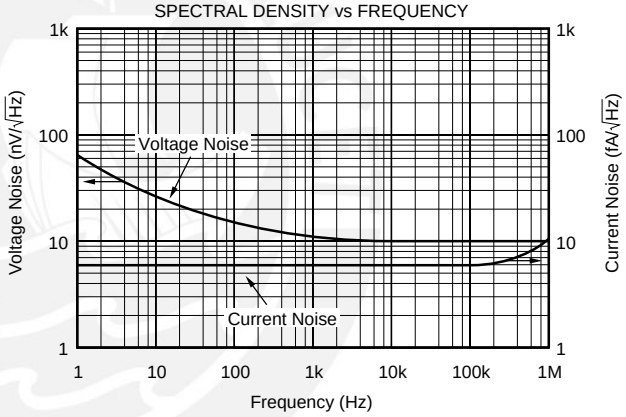
TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE



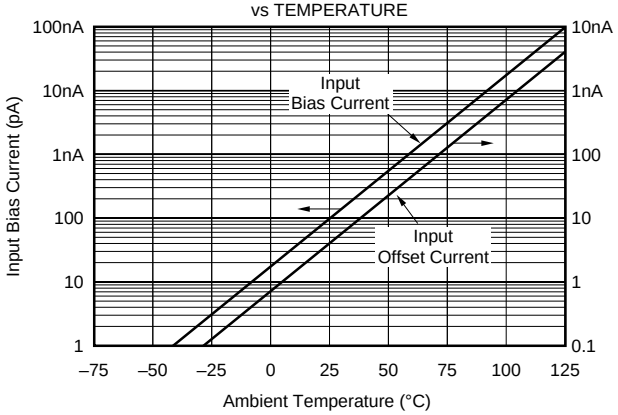
OPEN-LOOP GAIN/PHASE vs FREQUENCY



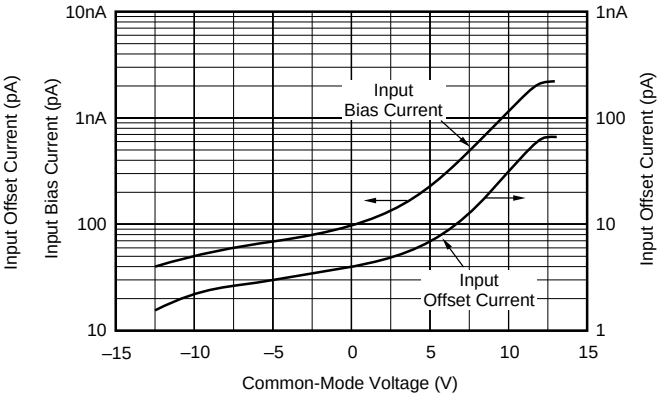
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



INPUT BIAS AND INPUT OFFSET CURRENT vs TEMPERATURE



INPUT BIAS AND INPUT OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



Tesis publicada con autorización del autor
No olvide citar esta tesis

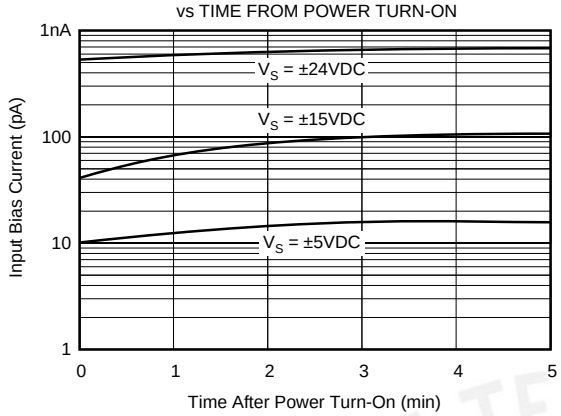
TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

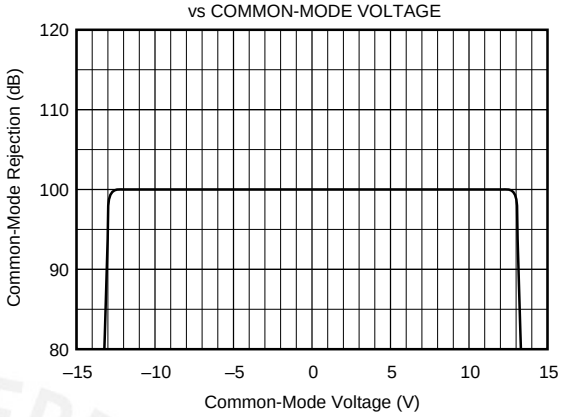
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

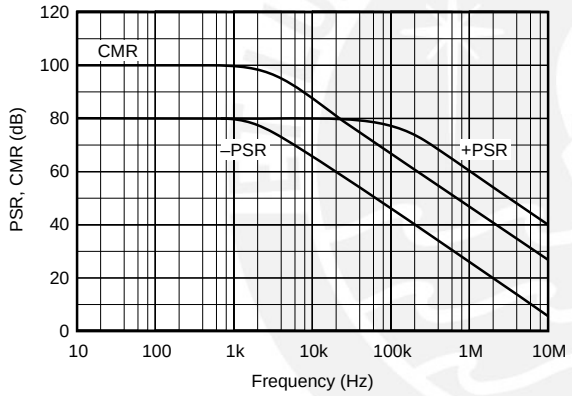
INPUT BIAS CURRENT
vs TIME FROM POWER TURN-ON



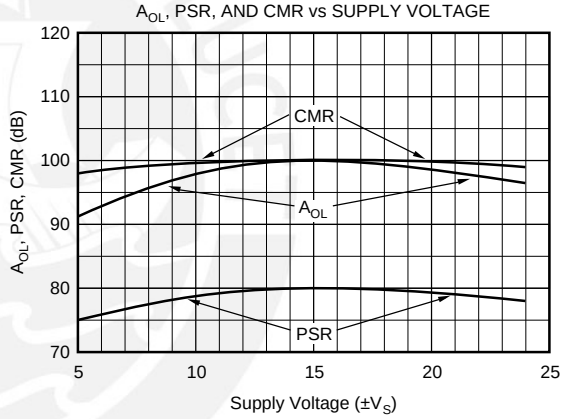
COMMON-MODE REJECTION
vs COMMON-MODE VOLTAGE



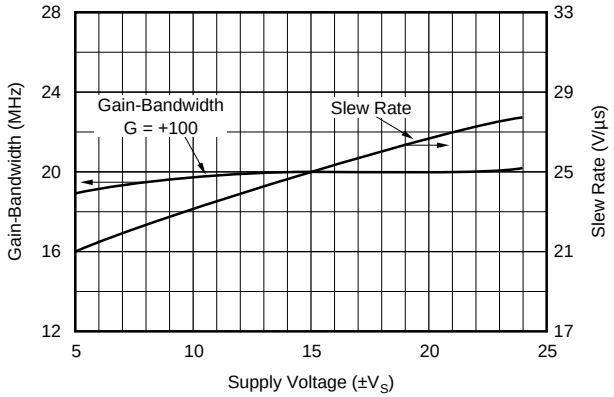
POWER SUPPLY AND COMMON-MODE
REJECTION vs FREQUENCY



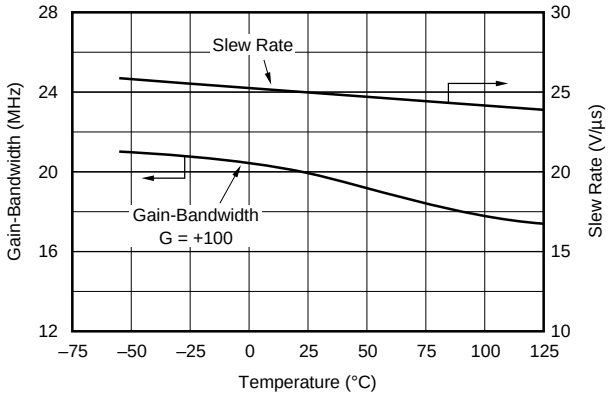
A_{OL}, PSR, AND CMR vs SUPPLY VOLTAGE



GAIN-BANDWIDTH AND SLEW RATE
vs SUPPLY VOLTAGE



GAIN-BANDWIDTH AND SLEW RATE
vs TEMPERATURE



BURR-BROWN®

Tesis publicada con autorización del autor
No olvide citar esta tesis

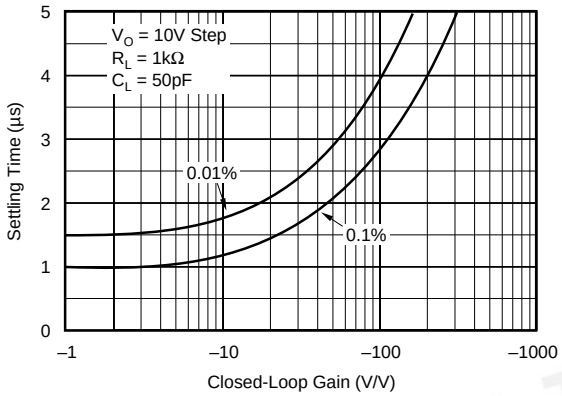
TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

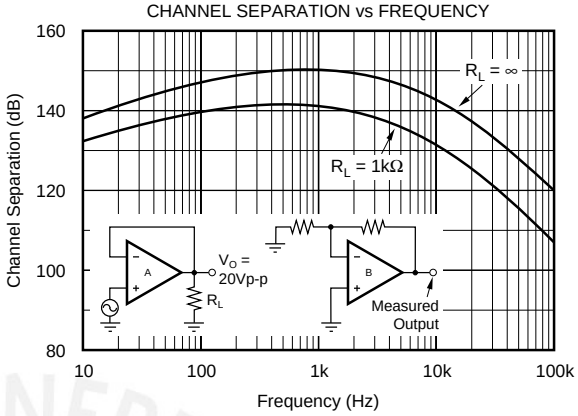
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

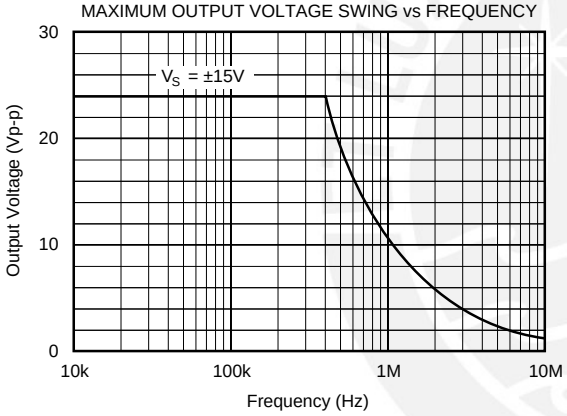
SETTLING TIME vs CLOSED-LOOP GAIN



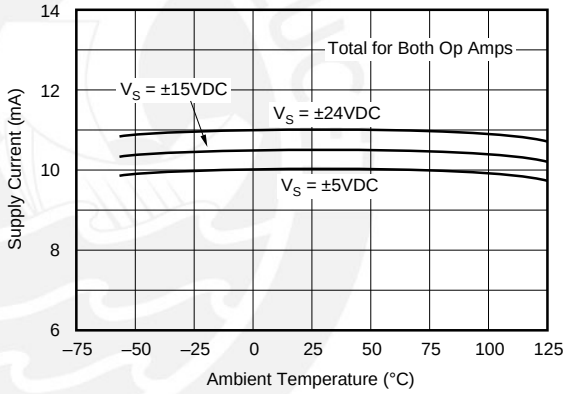
CHANNEL SEPARATION vs FREQUENCY



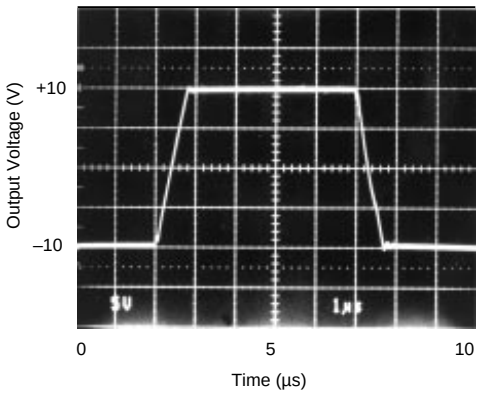
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



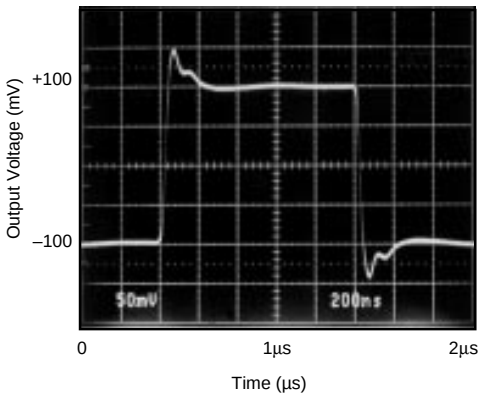
SUPPLY CURRENT vs TEMPERATURE



LARGE-SIGNAL TRANSIENT RESPONSE



SMALL-SIGNAL TRANSIENT RESPONSE



30
25
20
15
10
Slew Rate (V/µs)
25

Tesis publicada con autorización del autor
No olvide citar esta tesis

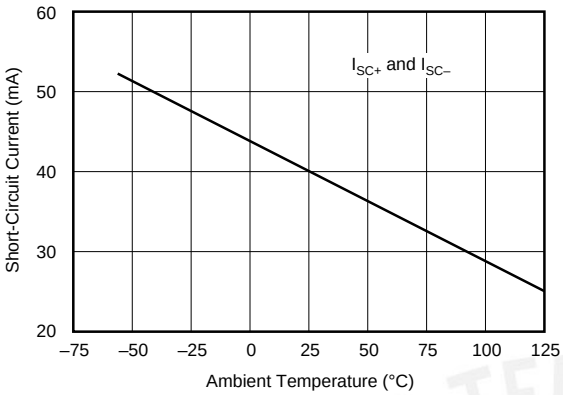
TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

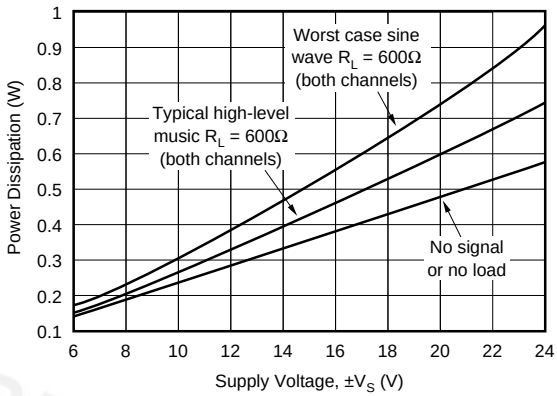
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

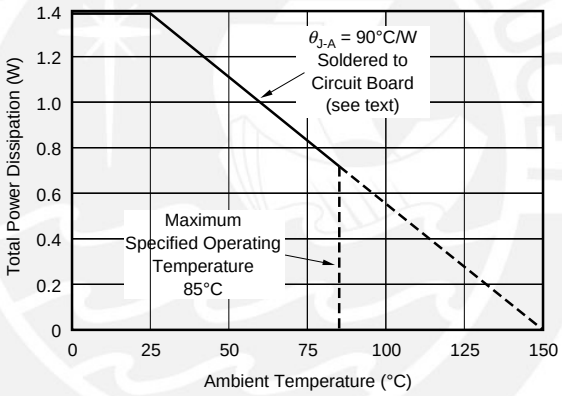
SHORT-CIRCUIT CURRENT vs TEMPERATURE



POWER DISSIPATION vs SUPPLY VOLTAGE



MAXIMUM POWER DISSIPATION vs TEMPERATURE



Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

APPLICATIONS INFORMATION

The OPA2604 is unity-gain stable, making it easy to use in a wide range of circuitry. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins. In most cases 1µF tantalum capacitors are adequate.

DISTORTION MEASUREMENTS

The distortion produced by the OPA2604 is below the measurement limit of virtually all commercially available equipment. A special test circuit, however, can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source which can be referred to the input. Figure 1 shows a circuit which causes the op amp distortion to be 101 times greater than normally produced by the op amp. The addition of R_3 to the otherwise standard non-inverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101. This extends the measurement limit, including the effects of the signal-source purity, by a factor of 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with the Audio Precision System One which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

CAPACITIVE LOADS

The dynamic characteristics of the OPA2604 have been optimized for commonly encountered gains, loads and operating conditions. The combination of low closed-loop gain and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Load capacitance reacts with the op amp's open-loop output resistance to form an additional pole in the feedback loop. Figure 2 shows various circuits which preserve phase margin with capacitive load. Request Application Bulletin AB-028 for details of analysis techniques and applications circuits.

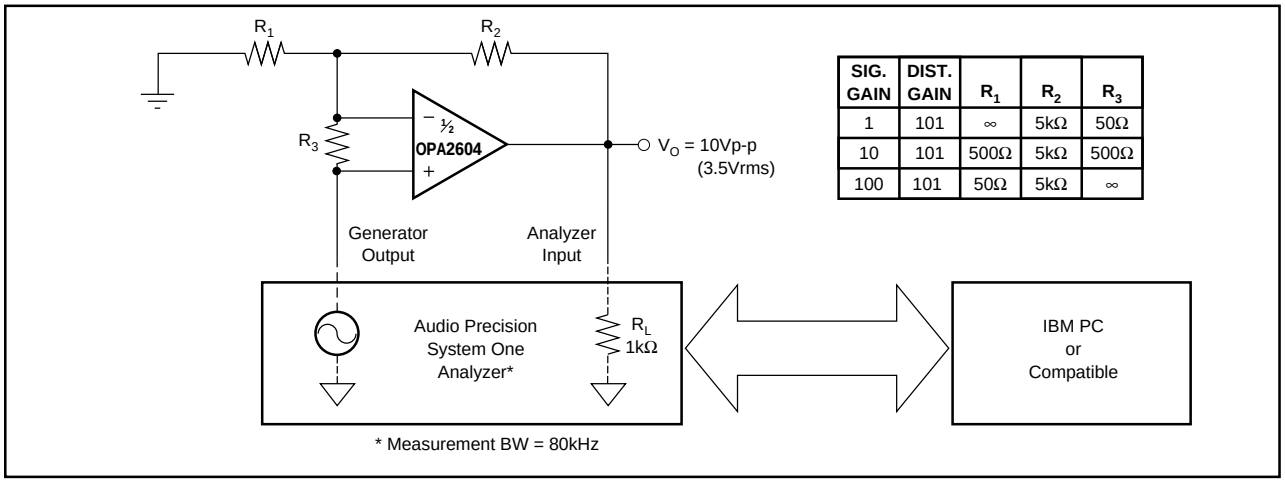
For the unity-gain buffer, Figure 2a, stability is preserved by adding a phase-lead network, R_C and C_C. Voltage drop across R_C will reduce output voltage swing with heavy loads. An alternate circuit, Figure 2b, does not limit the output with low load impedance. It provides a small amount of positive feedback to reduce the net feedback factor. Input impedance of this circuit falls at high frequency as op amp gain rolloff reduces the bootstrap action on the compensation network.

Figures 2c and 2d show compensation techniques for noninverting amplifiers. Like the follower circuits, the circuit in Figure 2d eliminates voltage drop due to load current, but at the penalty of somewhat reduced input impedance at high frequency.

Figures 2e and 2f show input lead compensation networks for inverting and difference amplifier configurations.

NOISE PERFORMANCE

Op amp noise is described by two parameters—noise voltage and noise current. The voltage noise determines the noise performance with low source impedance. Low noise bipolar-input op amps such as the OPA27 and OPA37 provide very low voltage noise. But if source impedance is greater than a few thousand ohms, the current noise of bipolar-input op amps react with the source impedance and will dominate. At a few thousand ohms source impedance and above, the OPA2604 will generally provide lower noise.

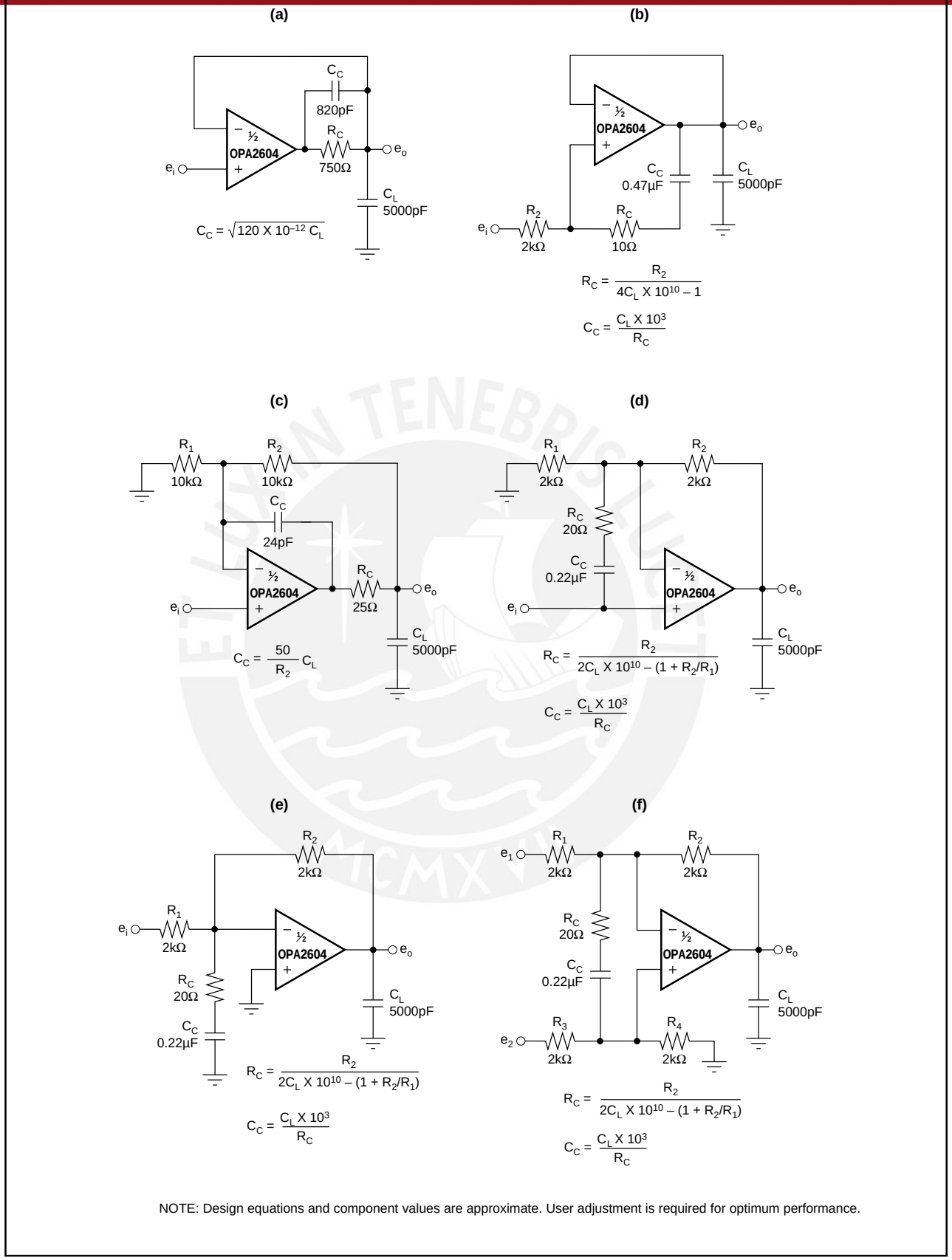


SIG. GAIN	DIST. GAIN	R_1	R_2	R_3
1	101	∞	5kΩ	50Ω
10	101	500Ω	5kΩ	500Ω
100	101	50Ω	5kΩ	∞

FIGURE 1. Distortion Test Circuit.

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP



NOTE: Design equations and component values are approximate. User adjustment is required for optimum performance.

FIGURE 2. Driving Large Capacitive Loads.

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

POWER DISSIPATION

The OPA2604 is capable of driving 600Ω loads with power supply voltages up to ±24V. Internal power dissipation is increased when operating at high power supply voltage. The typical performance curve, Power Dissipation vs Power Supply Voltage, shows quiescent dissipation (no signal or no load) as well as dissipation with a worst case continuous sine wave. Continuous high-level music signals typically produce dissipation significantly less than worst case sine waves.

Copper leadframe construction used in the OPA2604 improves heat dissipation compared to conventional plastic packages. To achieve best heat dissipation, solder the device directly to the circuit board and use wide circuit board traces.

OUTPUT CURRENT LIMIT

Output current is limited by internal circuitry to approximately ±40mA at 25°C. The limit current decreases with increasing temperature as shown in the typical curves.

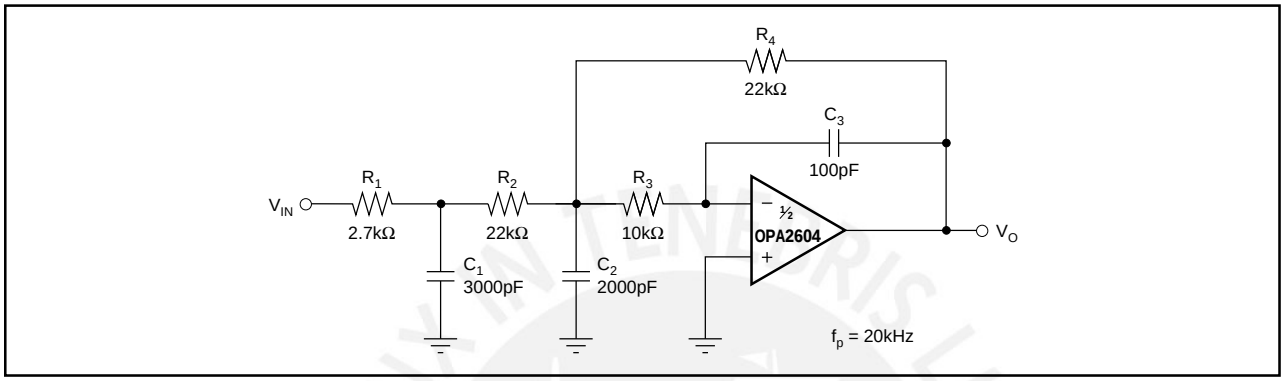


FIGURE 3. Three-Pole Low-Pass Filter.

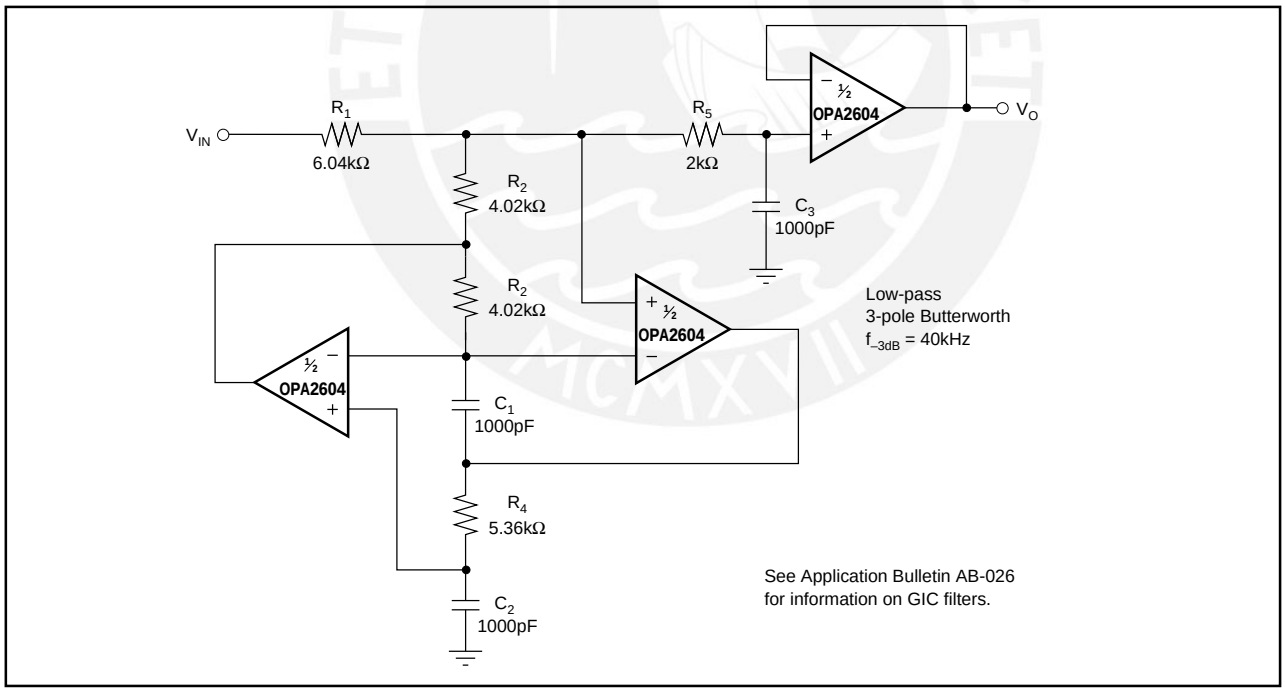


FIGURE 4. Three-Pole Generalized Immittance Converter (GIC) Low-Pass Filter.

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

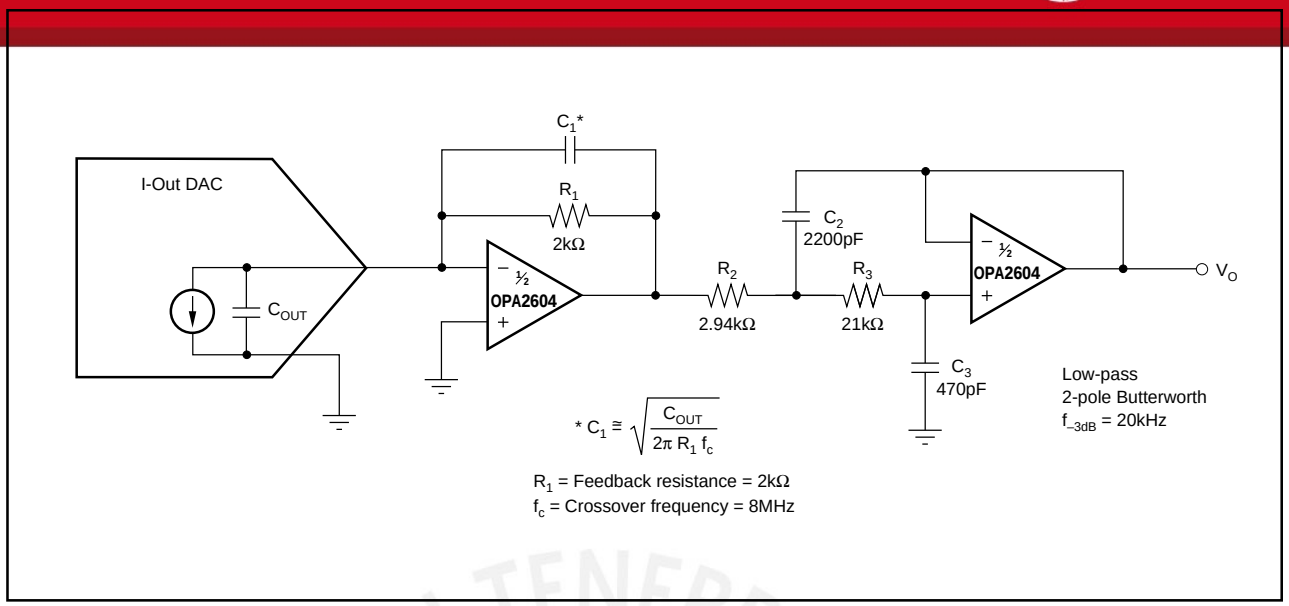


FIGURE 5. DAC I/V Amplifier and Low-Pass Filter.

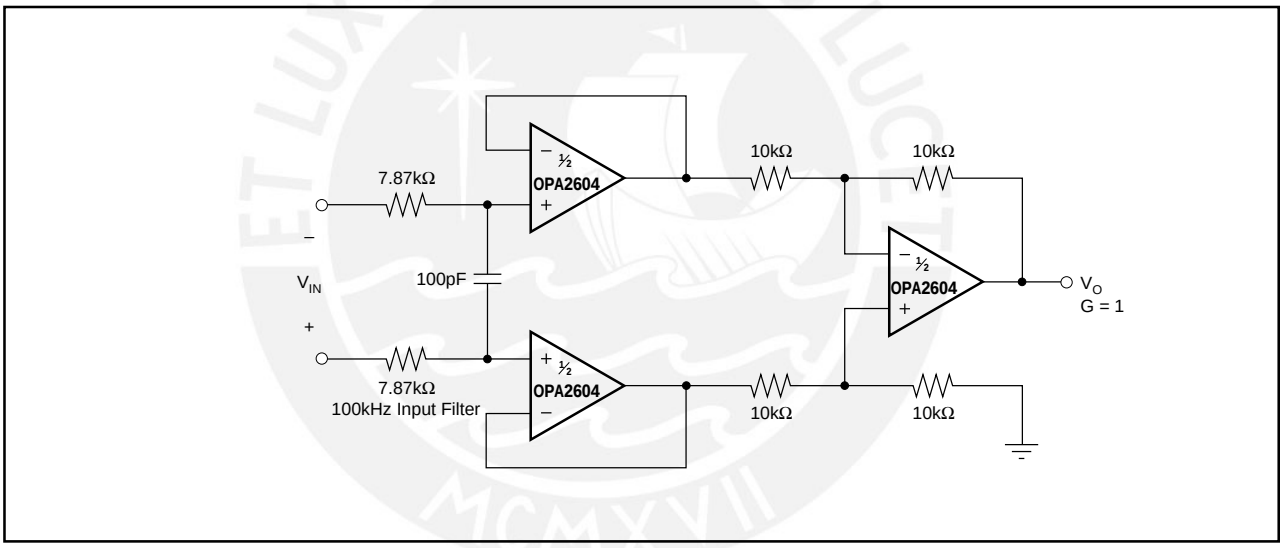


FIGURE 6. Differential Amplifier with Low-Pass Filter.

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

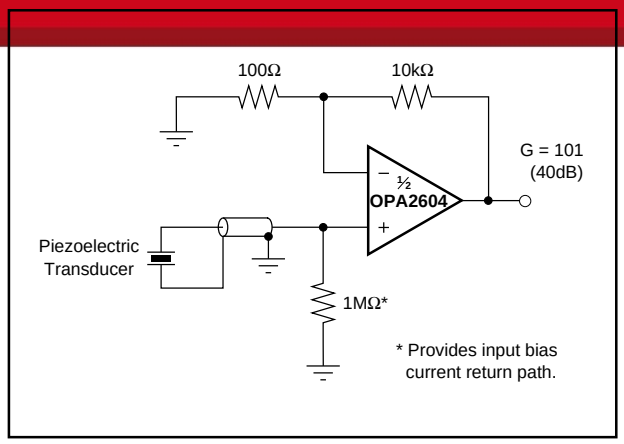


FIGURE 7. High Impedance Amplifier.

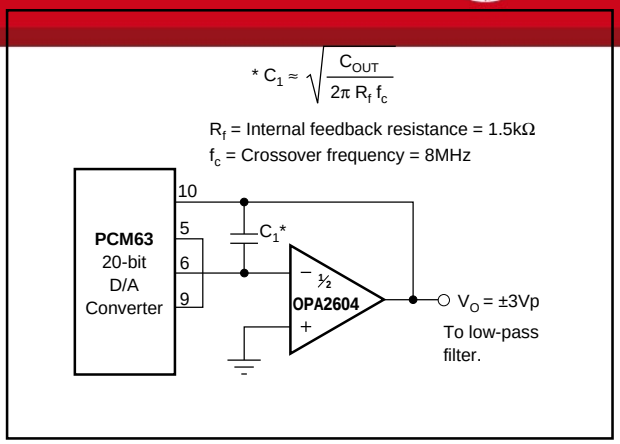


FIGURE 8. Digital Audio DAC I-V Amplifier.

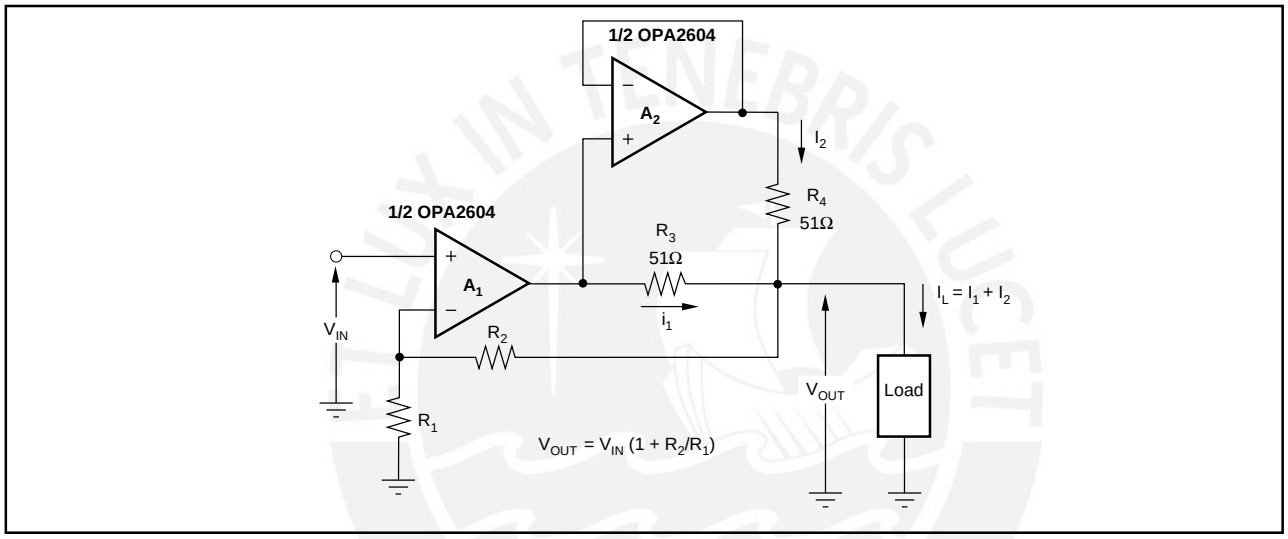


FIGURE 9. Using the Dual OPA2604 Op Amp to Double the Output Current to a Load.

Tesis publicada con autorización del autor
No olvide citar esta tesis

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA2604AP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2604APG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2604AU	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2604AU/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2604AU/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2604AUE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2604AUG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

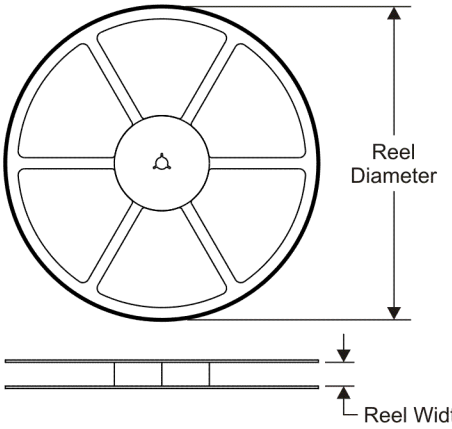
OTHER QUALIFIED VERSIONS OF OPA2604 :
- Automotive: OPA2604-Q1

NOTE: Qualified Version Definitions:
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

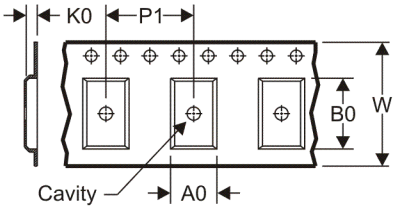
Tesis publicada con autorización del autor
No olvide citar esta tesis

TAPE AND REEL INFORMATION

REEL DIMENSIONS

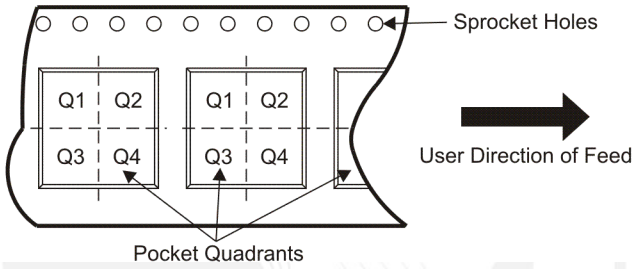


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

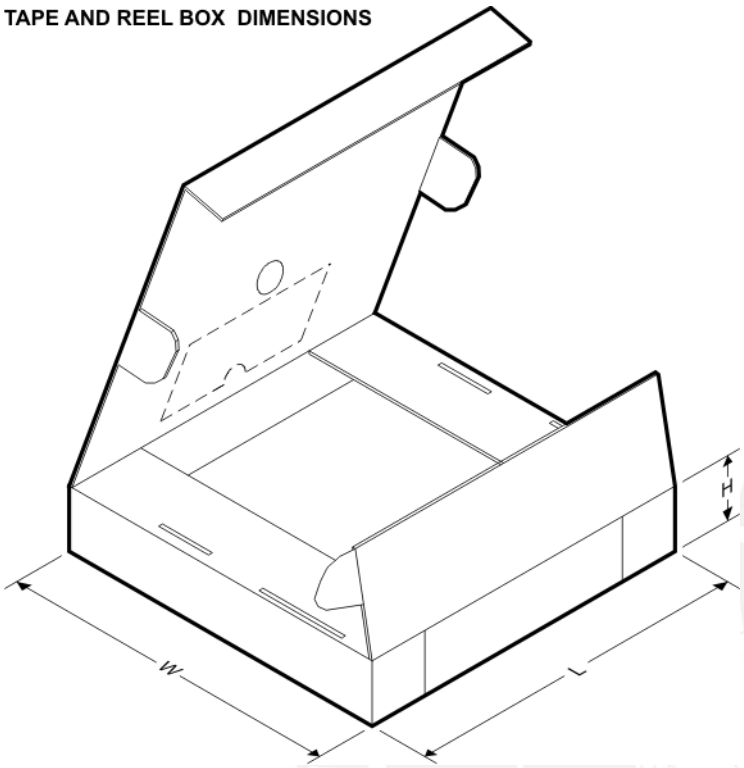


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2604AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Tesis publicada con autorización del autor
No olvide citar esta tesis

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2604AU/2K5	SOIC	D	8	2500	346.0	346.0	29.0

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated

Tesis publicada con autorización del autor
No olvide citar esta tesis

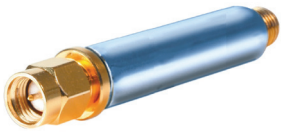
Coaxial
TESIS PUCP

Bandpass Filter

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

VBFZ-2340+

50Ω 2020 to 2660 MHz



CASE STYLE: FF1145

Connectors	Model	Price	Qty.
SMA	VBFZ-2340-S+	$39.95 ea.	(1-9)

Maximum Ratings

Operating Temperature	-55°C to 100°C
Storage Temperature	-55°C to 100°C
RF Power Input*	7W at 25°C

*Passband rating, derate linearly to 3W at 100°C ambient.
Permanent damage may occur if any of these limits are exceeded.

Features

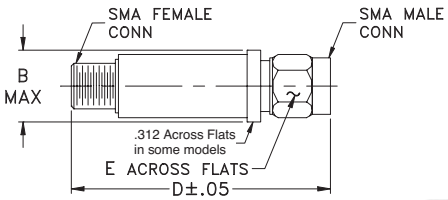
- Good Rejection, 30dB up to 8.5GHz
- Low insertion loss
- Excellent power handling, 7W
- Temperature stable LTCC internal structure
- Rugged stainless steel unibody
- Protected by US Patent 6,943,646

Application

- Harmonic rejection
- Transmitters/receivers
- Lab use
- Test instrumentation

+RoHS Compliant
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Outline Drawing



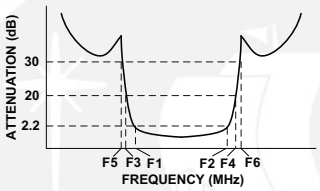
Outline Dimensions (inch / mm)

B	D	E	wt.
.410	**1.91**	**.312**	grams
10.41	48.51	7.92	11.8

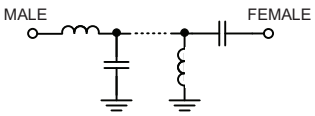
Bandpass Filter Electrical Specifications (T_{AMB}= 25°C)

CENTER FREQ. (MHz)	PASSBAND (MHz) (Loss < 2.2dB)	STOPBANDS (MHz) (Loss > 20dB)		(Loss 30dB Typ)		VSWR (:1) Passband		Stopband
Fc	F1 - F2	F3	F4	F5	F6	Typ.	Max.	Typ.
2340	2020 - 2660	1450	3750	1400	3800 - 8500	1.5	2.4	20

Typical Frequency Response



Functional Schematic

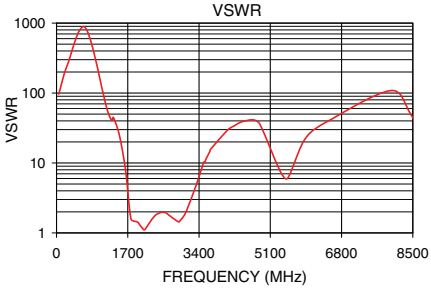


Typical Performance Data at 25°C

Frequency (MHz)	Insertion Loss (dB)	VSWR (:1)
50	79.11	99.13
500	75.05	492.28
1000	55.64	162.13
1400	35.23	33.55
1450	29.70	30.82
1514	23.17	21.16
1630	12.16	9.28
1700	6.35	3.91
1785	2.64	1.47
2020	1.39	1.25
2340	1.51	1.74
2660	1.79	1.89
3145	3.94	2.37
3315	8.89	4.64
3480	16.47	9.08
3750	30.45	17.37
3800	32.80	21.11
3815	33.59	20.28
6000	35.17	30.31
8500	29.30	44.23

VBFZ-2340+
INSERTION LOSS

VBFZ-2340+
VSWR



For detailed performance specs & shopping online see web site

Notes: 1. Performance and quality attributes and conditions not expressly stated in this specification sheet are intended to be excluded and do not form a part of this specification sheet. 2. Electrical specifications and performance data contained herein are based on Mini-Circuit's applicable established test performance criteria and measurement instructions. 3. The parts covered by this specification sheet are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and Conditions, including limitation of warranty and exclusive remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/MCLStore/terms.jsp.

REV. B
M131709
EDR-8452U
VBFZ-2340+
URJ/RAV
121016
Page 1 of 1

Tesis publicada con autorización del autor
No olvide citar esta tesis

XR-2206

Monolithic
Function Generator

...the analog plus company™

June 1997-3

FEATURES

- Low-Sine Wave Distortion, 0.5%, Typical
- Excellent Temperature Stability, 20ppm/°C, Typ.
- Wide Sweep Range, 2000:1, Typical
- Low-Supply Sensitivity, 0.01%V, Typ.
- Linear Amplitude Modulation
- TTL Compatible FSK Controls
- Wide Supply Range, 10V to 26V
- Adjustable Duty Cycle, 1% TO 99%

APPLICATIONS

- Waveform Generation
- Sweep Generation
- AM/FM Generation
- V/F Conversion
- FSK Generation
- Phase-Locked Loops (VCO)

GENERAL DESCRIPTION

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high-stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01Hz to more than 1MHz.

The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. It has a typical drift specification of 20ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range with an external control voltage, while maintaining low distortion.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-2206M	16 Lead 300 Mil CDIP	-55°C to +125°C
XR-2206P	16 Lead 300 Mil PDIP	–40°C to +85°C
XR-2206CP	16 Lead 300 Mil PDIP	0°C to +70°C
XR-2206D	16 Lead 300 Mil JEDEC SOIC	0°C to +70°C

©1972
EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ (510) 668-7017

TESIS PUCP

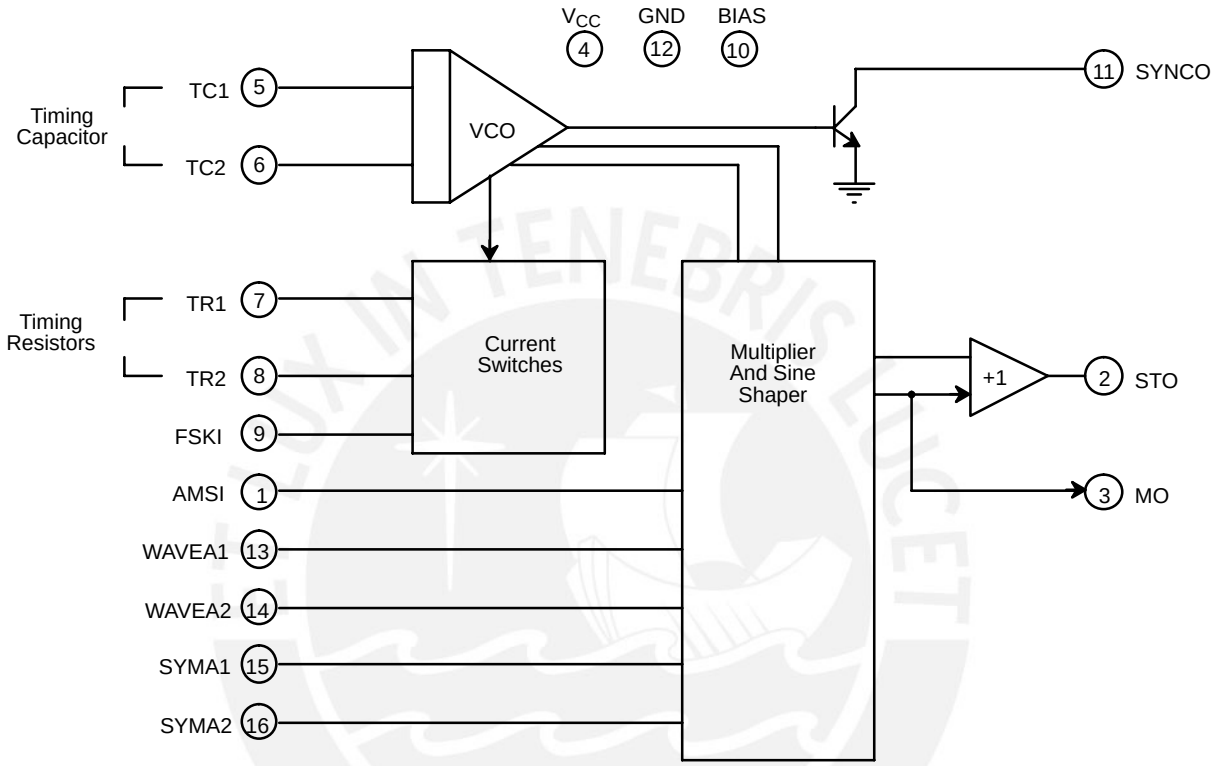
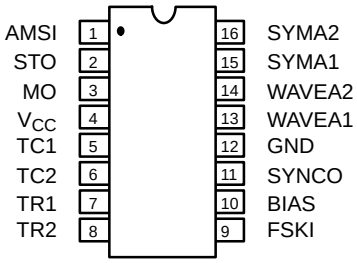
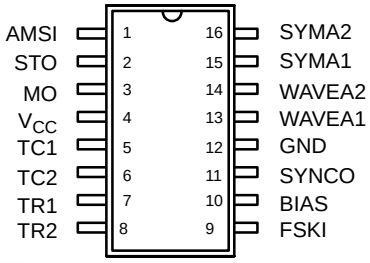


Figure 1. XR-2206 Block Diagram

Tesis publicada con autorización del autor
No olvide citar esta tesis



16 Lead PDIP, CDIP (0.300")



16 Lead SOIC (Jedec, 0.300")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	AMSI	I	**Amplitude Modulating Signal Input.**
2	STO	O	**Sine or Triangle Wave Output.**
3	MO	O	**Multiplier Output.**
4	V_{CC}		**Positive Power Supply.**
5	TC1	I	**Timing Capacitor Input.**
6	TC2	I	**Timing Capacitor Input.**
7	TR1	O	**Timing Resistor 1 Output.**
8	TR2	O	**Timing Resistor 2 Output.**
9	FSKI	I	**Frequency Shift Keying Input.**
10	BIAS	O	**Internal Voltage Reference.**
11	SYNCO	O	**Sync Output.** This output is a open collector and needs a pull up resistor to V_{CC}.
12	GND		**Ground pin.**
13	WAVEA1	I	**Wave Form Adjust Input 1.**
14	WAVEA2	I	**Wave Form Adjust Input 2.**
15	SYMA1	I	**Wave Symetry Adjust 1.**
16	SYMA2	I	**Wave Symetry Adjust 2.**

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

DC ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of *Figure 2* **Vcc = 12V, T_A = 25°C, C = 0.01µF, R_1 = 100kΩ, R_2 = 10kΩ, R_3 = 25kΩ** Unless Otherwise Specified. S_1 open for triangle, closed for sine wave.

Parameters	XR-2206M/P			XR-2206CP/D			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
General Characteristics								
Single Supply Voltage	**10**		**26**	10		26	V	
Split-Supply Voltage	**±5**		**±13**	±5		±13	V	
Supply Current		12	**17**		14	20	mA	$R_1 \geq 10k\Omega$
Oscillator Section								
Max. Operating Frequency	**0.5**	1		0.5	1		MHz	C = 1000pF, R_1 = 1kΩ
Lowest Practical Frequency		0.01			0.01		Hz	C = 50µF, R_1 = 2MΩ
Frequency Accuracy		±1	**±4**		±2		% of f_o	$f_o = 1/R_1C$
Temperature Stability Frequency		±10	**±50**		±20		ppm/°C	0°C ≤ T_A ≤ 70°C $R_1 = R_2$ = 20kΩ
Sine Wave Amplitude Stability[2]		4800			4800		ppm/°C	
Supply Sensitivity		0.01	**0.1**		0.01		%/V	V_{LOW} = 10V, V_{HIGH} = 20V, $R_1 = R_2$ = 20kΩ
Sweep Range	1000:1	2000:1			2000:1		$f_H = f_L$	f_H @ R_1 = 1kΩ f_L @ R_1 = 2MΩ
Sweep Linearity								
10:1 Sweep		2			2		%	f_L = 1kHz, f_H = 10kHz
1000:1 Sweep		8			8		%	f_L = 100Hz, f_H = 100kHz
FM Distortion		0.1			0.1		%	±10% Deviation
Recommended Timing Components								
Timing Capacitor: C	**0.001**		100	0.001		100	µF	*Figure 5*
Timing Resistors: R_1 & R_2	**1**		2000	1		2000	kΩ	
Triangle Sine Wave Output[1]								*Figure 3*
Triangle Amplitude		160			160		mV/kΩ	*Figure 2*, S_1 Open
Sine Wave Amplitude	**40**	60	80		60		mV/kΩ	*Figure 2*, S_1 Closed
Max. Output Swing		6			6		Vp-p	
Output Impedance		600			600		Ω	
Triangle Linearity		1			1		%	
Amplitude Stability		0.5			0.5		dB	For 1000:1 Sweep
Sine Wave Distortion								
Without Adjustment		2.5			2.5		%	R_1 = 30kΩ
With Adjustment		0.4	**1.0**		0.5	1.5	%	See *Figure 7* and *Figure 8*

Notes

[1] Output amplitude is directly proportional to the resistance, R_3, on Pin 3. See Figure 3.

[2] For maximum amplitude stability, R_3 should be a positive temperature coefficient resistor.

***Bold face parameters** are covered by production test and guaranteed over operating temperature range.*

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

DC ELECTRICAL CHARACTERISTICS (CONT'D)

Parameters	XR-2206M/P			XR-2206CP/D			Units	Conditions
	Min.	Typ.	Max.	Min.	Typ.	Max.		
Amplitude Modulation								
Input Impedance	50	100		50	100		kΩ	
Modulation Range		100			100		%	
Carrier Suppression		55			55		dB	
Linearity		2			2		%	For 95% modulation
Square-Wave Output								
Amplitude		12			12		Vp-p	Measured at Pin 11.
Rise Time		250			250		ns	C_L = 10pF
Fall Time		50			50		ns	C_L = 10pF
Saturation Voltage		0.2	**0.4**		0.2	0.6	V	I_L = 2mA
Leakage Current		0.1	**20**		0.1	100	μA	V_{CC} = 26V
FSK Keying Level (Pin 9)	0.8	1.4	**2.4**	0.8	1.4	2.4	V	See section on circuit controls
Reference Bypass Voltage	2.9	3.1	**3.3**	2.5	3	3.5	V	Measured at Pin 10.

Notes
[1] Output amplitude is directly proportional to the resistance, R_3, on Pin 3. See Figure 3.
[2] For maximum amplitude stability, R_3 should be a positive temperature coefficient resistor.
***Bold face parameters** are covered by production test and guaranteed over operating temperature range.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Power Supply 26V
Power Dissipation 750mW
Derate Above 25°C . . . . . 5mW/°C
Total Timing Current 6mA
Storage Temperature . . . . . -65°C to +150°C

SYSTEM DESCRIPTION

The XR-2206 is comprised of four functional blocks; a voltage-controlled oscillator (VCO), an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches.

The VCO produces an output frequency proportional to an input current, which is set by a resistor from the timing terminals to ground. With two timing pins, two discrete output frequencies can be independently produced for FSK generation applications by using the FSK input control pin. This input controls the current switches which select one of the timing resistor currents, and routes it to the VCO.

Tesis publicada con autorización del autor
No olvide citar esta tesis

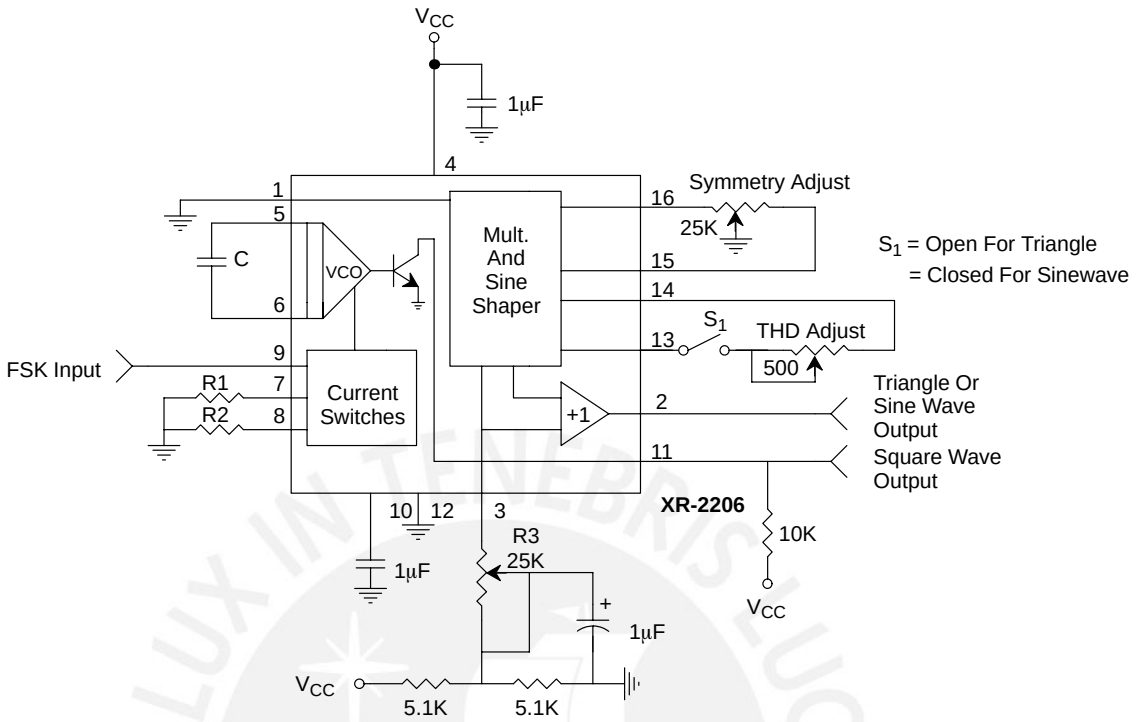


Figure 2. Basic Test Circuit

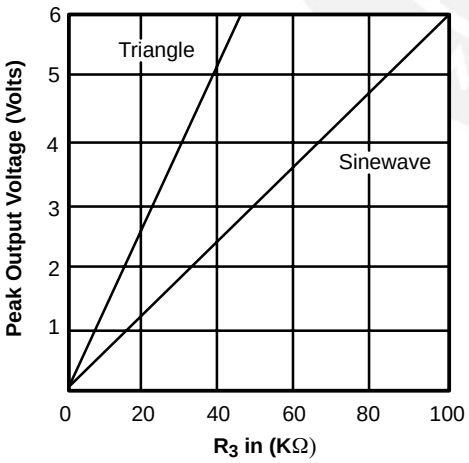


Figure 3. Output Amplitude as a Function of the Resistor, R3, at Pin 3

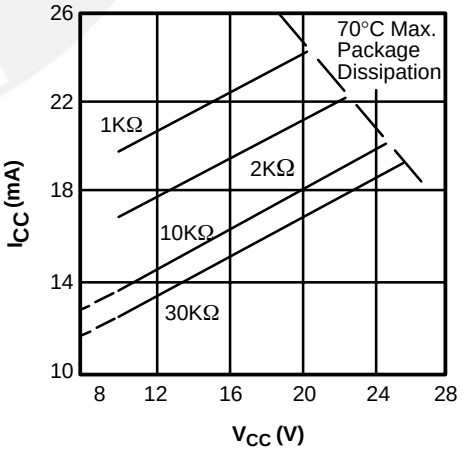


Figure 4. Supply Current vs Supply Voltage, Timing, R

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

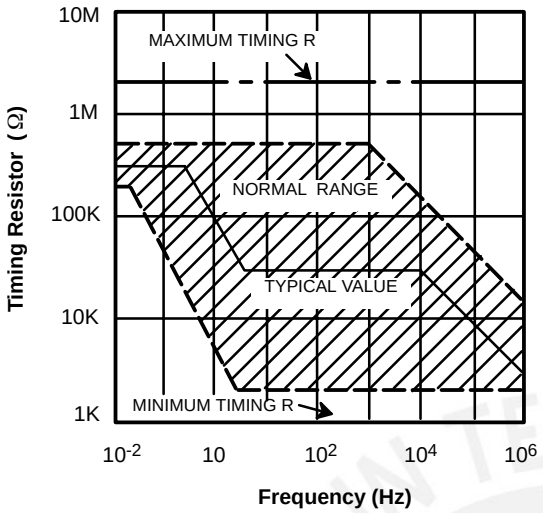


Figure 5. R versus Oscillation Frequency.

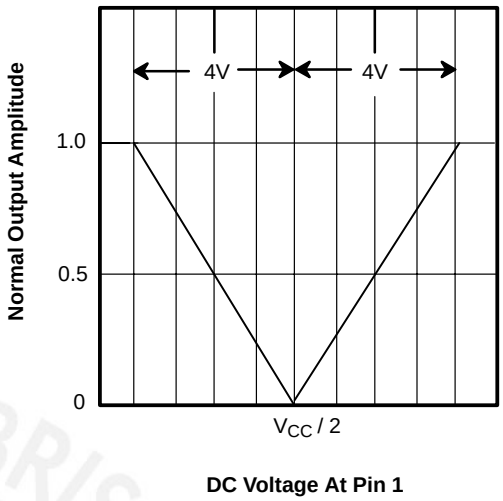


Figure 6. Normalized Output Amplitude versus DC Bias at AM Input (Pin 1)

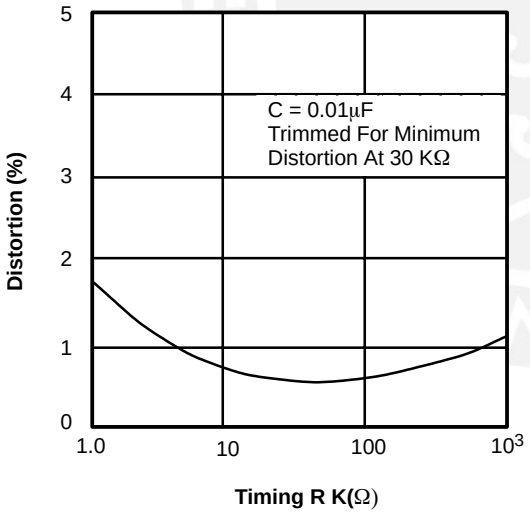


Figure 7. Trimmed Distortion versus Timing Resistor.

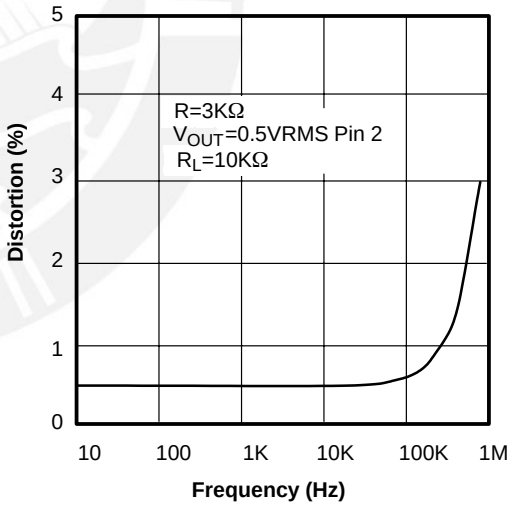


Figure 8. Sine Wave Distortion versus Operating Frequency with Timing Capacitors Varied.

Tesis publicada con autorización del autor
No olvide citar esta tesis

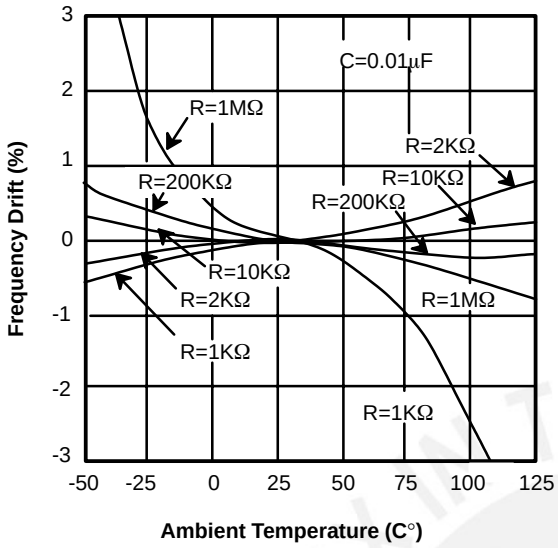


Figure 9. Frequency Drift versus Temperature.

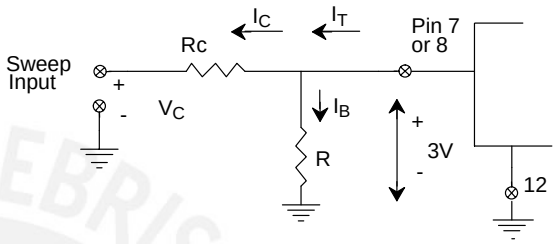


Figure 10. Circuit Connection for Frequency Sweep.

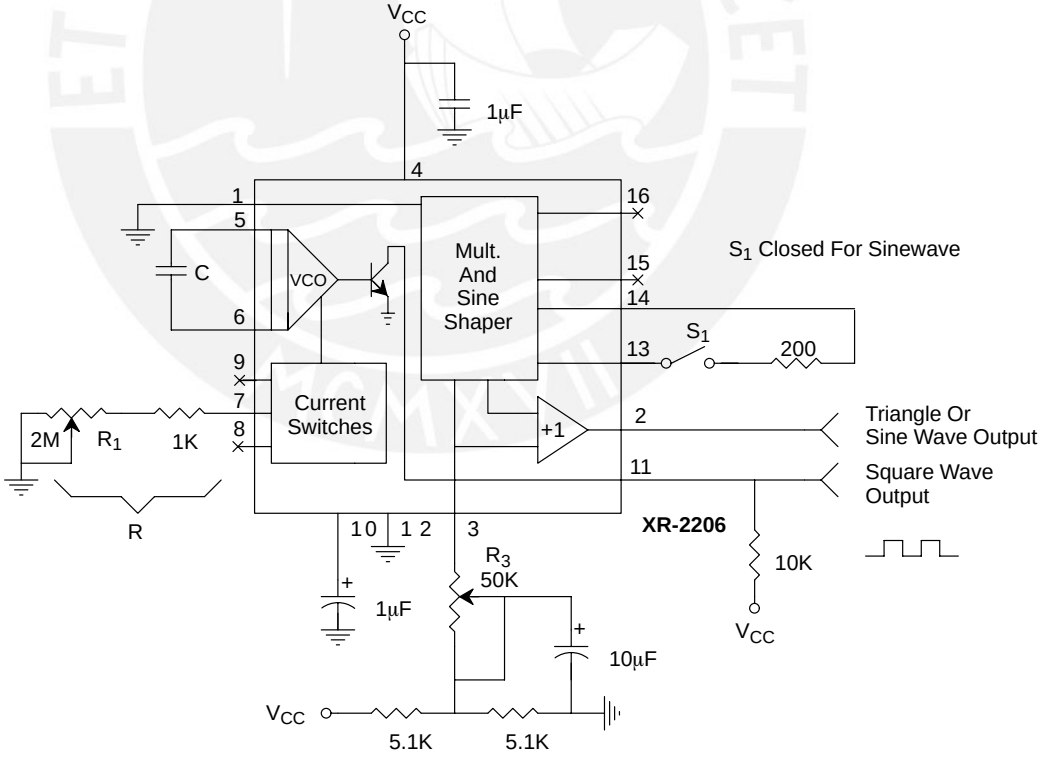


Figure 11. Circuit tor Sine Wave Generation without External Adjustment. (See *Figure 3* for Choice of R_3)

Tesis publicada con autorización del autor
No olvide citar esta tesis

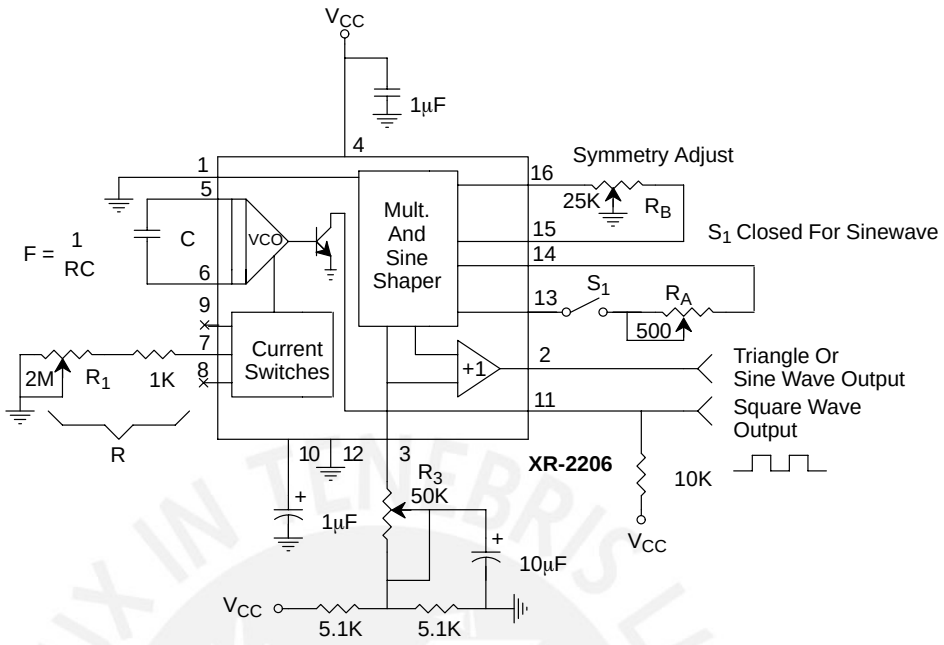


Figure 12. Circuit for Sine Wave Generation with Minimum Harmonic Distortion. (R_3 Determines Output Swing - See *Figure 3*)

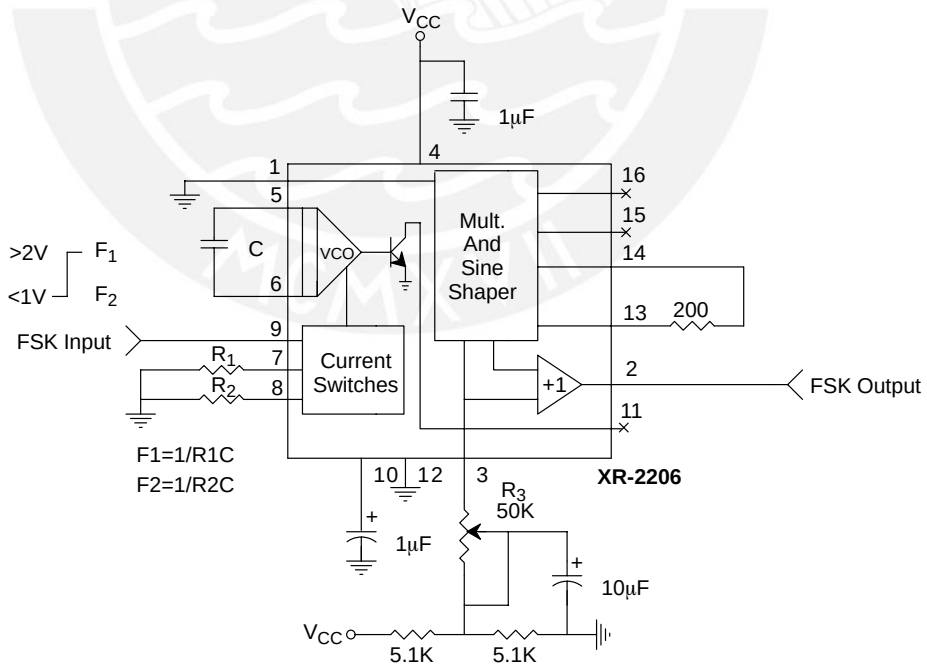


Figure 13. Sinusoidal FSK Generator

Tesis publicada con autorización del autor
No olvide citar esta tesis

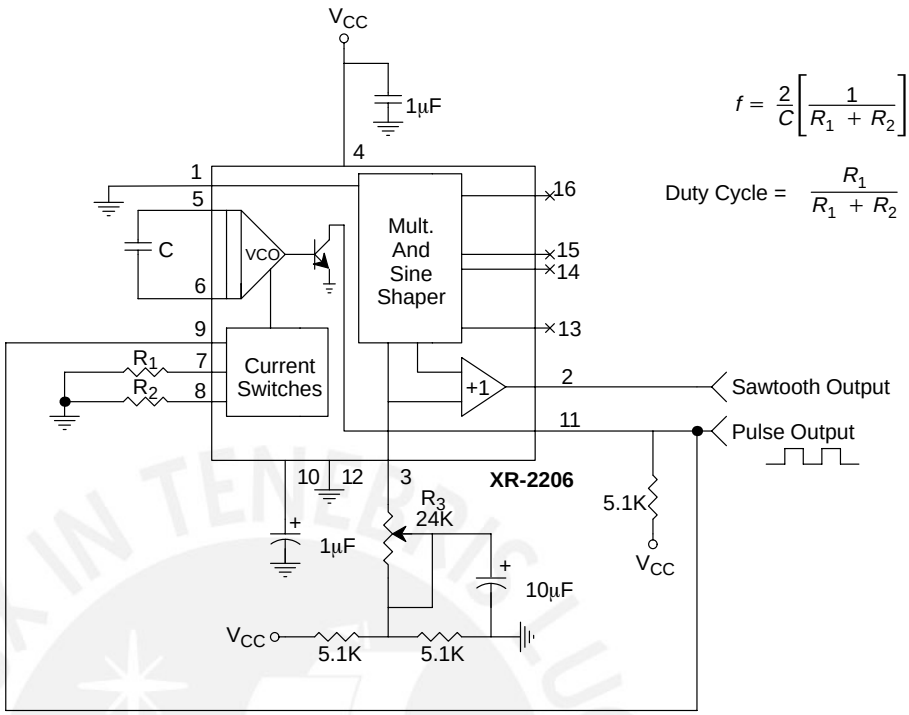


Figure 14. Circuit for Pulse and Ramp Generation.

Frequency-Shift Keying

The XR-2206 can be operated with two separate timing resistors, R_1 and R_2, connected to the timing Pin 7 and 8, respectively, as shown in *Figure 13.* Depending on the polarity of the logic signal at Pin 9, either one or the other of these timing resistors is activated. If Pin 9 is open-circuited or connected to a bias voltage $\geq$ 2V, only R_1 is activated. Similarly, if the voltage level at Pin 9 is $\leq$1V, only R_2 is activated. Thus, the output frequency can be keyed between two levels. f_1 and f_2, as:

$f_1 = 1/R_1C$ and $f_2 = 1/R_2C$

For split-supply operation, the keying voltage at Pin 9 is referenced to V^-.

Output DC Level Control

The dc level at the output (Pin 2) is approximately the same as the dc bias at Pin 3. In *Figure 11*, *Figure 12* and *Figure 13*, Pin 3 is biased midway between V+ and ground, to give an output dc level of $\approx V^+/2$.

APPLICATIONS INFORMATION

Sine Wave Generation

Without External Adjustment

Figure 11 shows the circuit connection for generating a sinusoidal output from the XR-2206. The potentiometer, R_1 at Pin 7, provides the desired frequency tuning. The maximum output swing is greater than $V^+/2$, and the typical distortion (THD) is < 2.5%. If lower sine wave distortion is desired, additional adjustments can be provided as described in the following section.

The circuit of *Figure 11* can be converted to split-supply operation, simply by replacing all ground connections with V^-. For split-supply operation, R_3 can be directly connected to ground.

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

With External Adjustment:

The harmonic content of sinusoidal output can be reduced to -0.5% by additional adjustments as shown in *Figure 12.* The potentiometer, R_A, adjusts the sine-shaping resistor, and R_B provides the fine adjustment for the waveform symmetry. The adjustment procedure is as follows:

1. Set R_B at midpoint and adjust R_A for minimum distortion.
2. With R_A set as above, adjust R_B to further reduce distortion.

Triangle Wave Generation

The circuits of *Figure 11* and *Figure 12* can be converted to triangle wave generation, by simply open-circuiting Pin 13 and 14 (i.e., S_1 open). Amplitude of the triangle is approximately twice the sine wave output.

FSK Generation

Figure 13 shows the circuit connection for sinusoidal FSK signal operation. Mark and space frequencies can be independently adjusted by the choice of timing resistors, R_1 and R_2; the output is phase-continuous during transitions. The keying signal is applied to Pin 9. The circuit can be converted to split-supply operation by simply replacing ground with V^-.

Pulse and Ramp Generation

Figure 14 shows the circuit for pulse and ramp waveform generation. In this mode of operation, the FSK keying terminal (Pin 9) is shorted to the square-wave output (Pin 11), and the circuit automatically frequency-shift keys itself between two separate frequencies during the positive-going and negative-going output waveforms. The pulse width and duty cycle can be adjusted from 1% to 99% by the choice of R_1 and R_2. The values of R_1 and R_2 should be in the range of 1kΩ to 2MΩ.

PRINCIPLES OF OPERATION

Description of Controls

Frequency of Operation:

The frequency of oscillation, f_0, is determined by the external timing capacitor, C, across Pin 5 and 6, and by the timing resistor, R, connected to either Pin 7 or 8. The frequency is given as:

$$f_0 = \frac{1}{RC}\ Hz$$

and can be adjusted by varying either R or C. The recommended values of R, for a given frequency range, as shown in *Figure 5.* Temperature stability is optimum for 4kΩ < R < 200kΩ. Recommended values of C are from 1000pF to 100μF.

Frequency Sweep and Modulation:

Frequency of oscillation is proportional to the total timing current, I_T, drawn from Pin 7 or 8:

$$f = \frac{320 I_T(mA)}{C(\mu F)}\ Hz$$

Timing terminals (Pin 7 or 8) are low-impedance points, and are internally biased at +3V, with respect to Pin 12. Frequency varies linearly with IT, over a wide range of current values, from 1μA to 3mA. The frequency can be controlled by applying a control voltage, V_C, to the activated timing pin as shown in *Figure 10.* The frequency of oscillation is related to VC as:

$$f = \frac{1}{RC}\left(1 + \frac{R}{R_C}\left(1 - \frac{V_C}{3}\right)\right) Hz$$

where V_C is in volts. The voltage-to-frequency conversion gain, K, is given as:

$$K = \partial f / \partial V_C = -\frac{0.32}{R_C C}\ \ Hz/V$$

CAUTION: *For safety operation of the circuit, I_T should be limited to ≤ 3mA.*

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

Output Amplitude:

Maximum output amplitude is inversely proportional to the external resistor, R_3, connected to Pin 3 (see *Figure 3*). For sine wave output, amplitude is approximately 60mV peak per kΩ of R_3; for triangle, the peak amplitude is approximately 160mV peak per kΩ of R_3. Thus, for example, R_3 = 50kΩ would produce approximately 13V sinusoidal output amplitude.

Amplitude Modulation:

Output amplitude can be modulated by applying a dc bias and a modulating signal to Pin 1. The internal impedance at Pin 1 is approximately 100kΩ. Output amplitude varies linearly with the applied voltage at Pin 1, for values of dc bias at this pin, within 14 volts of $V_{CC}/2$ as shown in *Figure 6.* As this bias level approaches $V_{CC}/2$, the phase of the output signal is reversed, and the amplitude goes through zero. This property is suitable for phase-shift keying and suppressed-carrier AM generation. Total dynamic range of amplitude modulation is approximately 55dB.

CAUTION: *AM control must be used in conjunction with a well-regulated supply, since the output amplitude now becomes a function of* V_{CC}.

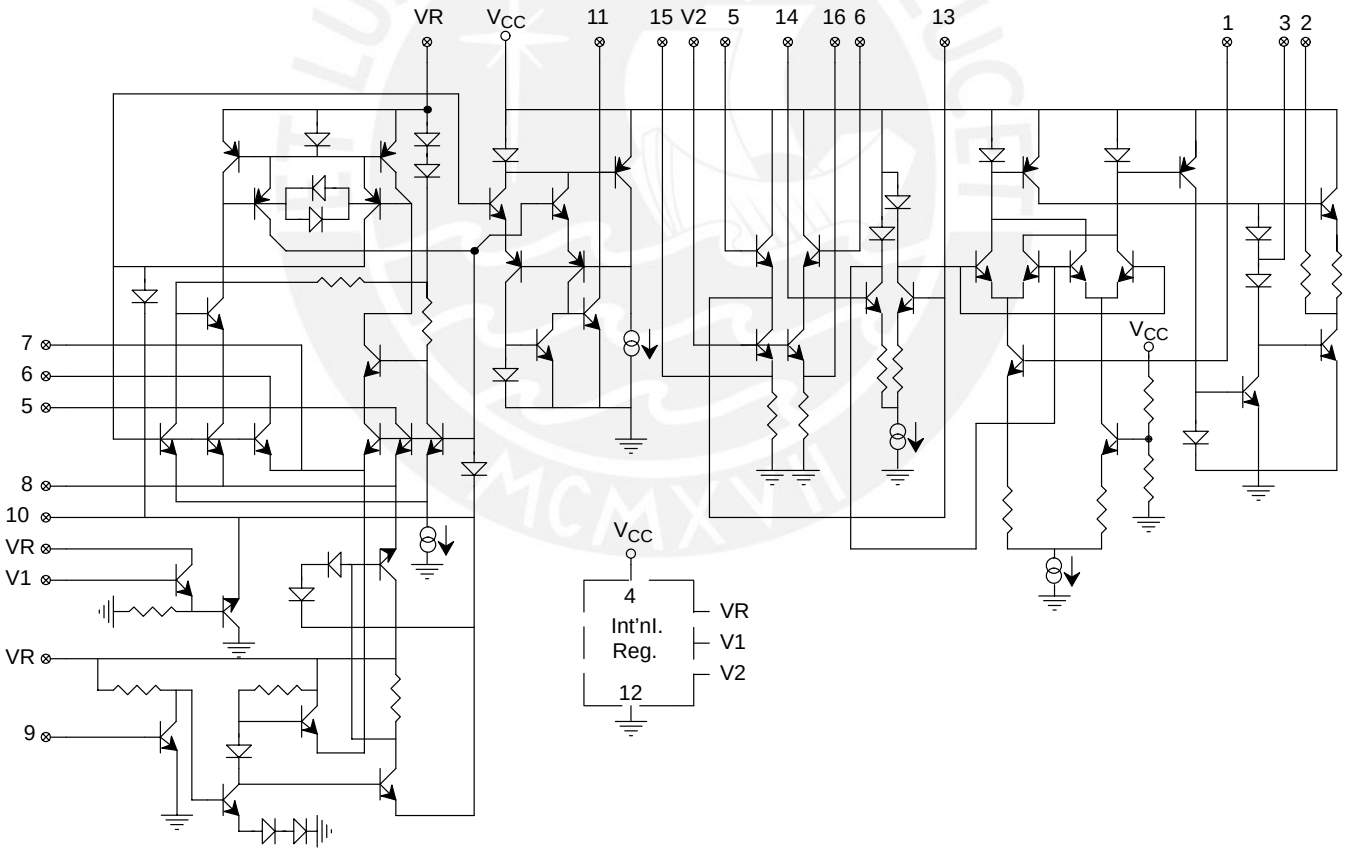


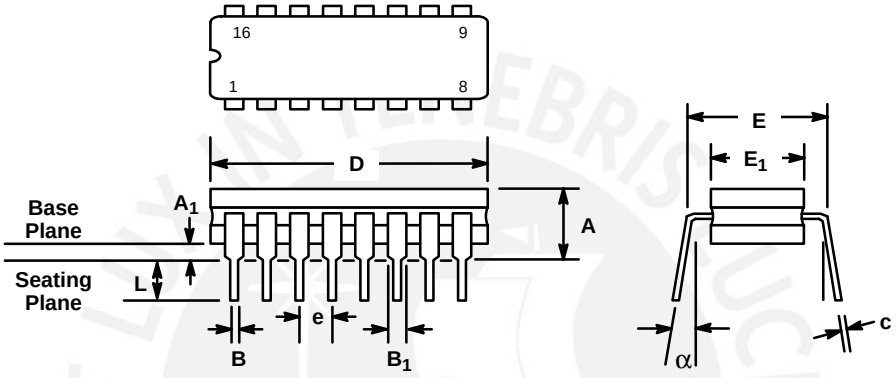
Figure 15. Equivalent Schematic Diagram

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

16 LEAD CERAMIC DUAL-IN-LINE (300 MIL CDIP)

Rev. 1.00



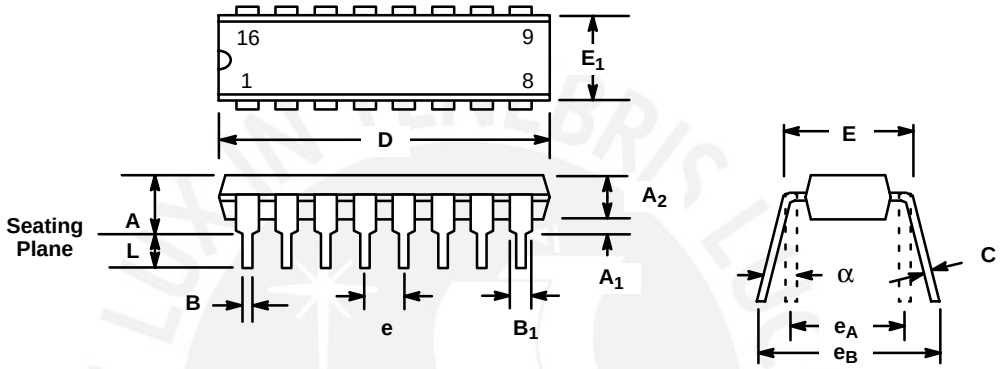
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.100	0.200	2.54	5.08
A_1	0.015	0.060	0.38	1.52
B	0.014	0.026	0.36	0.66
B_1	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	0.740	0.840	18.80	21.34
E_1	0.250	0.310	6.35	7.87
E	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

Tesis publicada con autorización del autor
No olvide citar esta tesis

16 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00



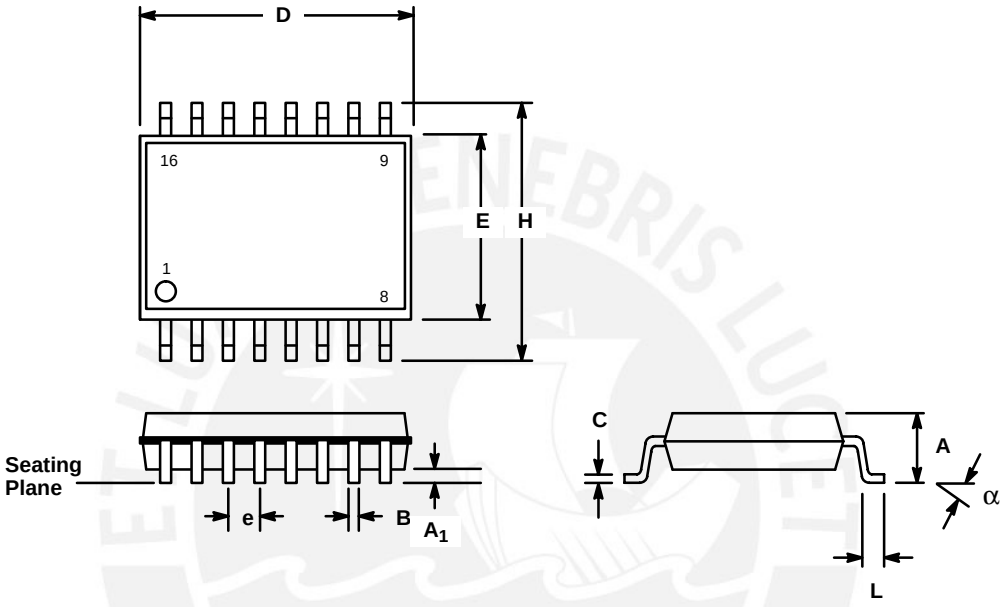
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.38	1.78
A_2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.745	0.840	18.92	21.34
E	0.300	0.325	7.62	8.26
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

Tesis publicada con autorización del autor
No olvide citar esta tesis

16 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC)

Rev. 1.00



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.093	0.104	2.35	2.65
A_1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.398	0.413	10.10	10.50
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Copyright 1972 EXAR Corporation
Datasheet June 1997
Reproduction, in part or whole, without the prior written consent of EXAR Corporation is prohibited.

Tesis publicada con autorización del autor
No olvide citar esta tesis

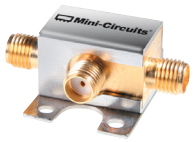
TESIS PUCP
PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

Coaxial

Frequency Mixer

ZX05-C42MH+

Level 13 (LO Power +13 dBm) 1000 to 4200 MHz



CASE STYLE: FL905

Connectors	Model	Price	Qty.
SMA	ZX05-C42MH-S+	$39.95 ea.	(1-24)

+RoHS Compliant
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Maximum Ratings

Operating Temperature	-40°C to 85°C
Storage Temperature	-55°C to 100°C
RF Power	200mW
IF Current	40mA

Permanent damage may occur if any of these limits are exceeded.

Coaxial Connections

LO	1
RF	2
IF	3

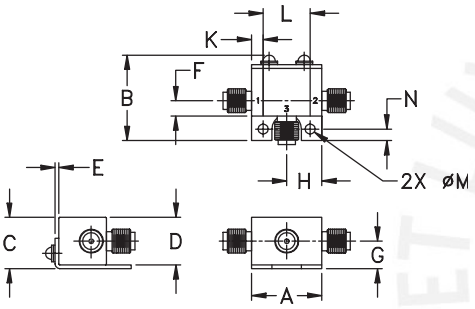
Features

- rugged construction
- small size
- low conversion loss
- high L-R isolation
- protected by US Patents 6,790,049 & 7,027,795

Applications

- cellular
- PCS
- instrumentation
- satellite communication

Outline Drawing



Outline Dimensions (inch / mm)

A	B	C	D	E	F	G
.74	.90	.54	.50	.04	.16	.29
18.80	22.86	13.72	12.70	1.02	4.06	7.37

H	J	K	L	M	N	wt
.37	--	.122	.496	.106	.122	grams
9.40	--	3.10	12.60	2.69	3.10	20.0

Electrical Specifications (T_{AMB}=25°C)

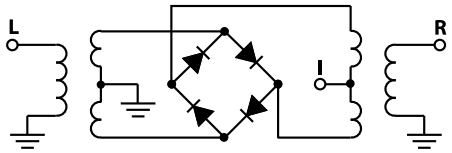
FREQUENCY (MHz)		CONVERSION LOSS (dB)			LO-RF ISOLATION (dB)		LO-IF ISOLATION (dB)		IP3 at center band (dBm)
LO/RF f_L-f_U	IF	Mid-Band $\overline{X}$	Mid-Band σ	Total Range Max.	Typ.	Min.	Typ.	Min.	Typ.
1000-4200	DC-1500	6.2	0.1	8.9	35	15	20	10	16

1 dB COMP.: +9 dBm typ.

Typical Performance Data

Frequency (MHz)		Conversion Loss (dB)	Isolation L-R (dB)	Isolation L-I (dB)	VSWR RF Port (:1)	VSWR LO Port (:1)
RF	LO	LO +13dBm	LO +13dBm	LO +13dBm	LO +13dBm	LO +13dBm
1000.10	1030.11	5.54	34.65	22.99	2.57	4.54
1164.20	1194.21	5.75	42.95	25.97	3.33	3.62
1328.31	1358.32	5.65	45.06	24.23	3.36	2.88
1492.41	1522.42	5.52	41.94	21.25	3.20	2.69
1656.51	1686.52	5.86	37.88	21.97	2.96	2.79
1820.61	1850.62	5.56	39.58	20.83	2.49	2.93
1984.72	2014.73	5.74	36.47	22.17	2.29	3.21
2148.82	2178.83	5.69	35.35	22.92	2.29	3.47
2312.92	2342.93	6.00	34.88	19.04	2.64	4.03
2559.07	2589.08	6.38	40.91	18.95	2.91	6.03
2723.18	2753.19	6.54	41.04	19.81	3.33	8.33
2887.28	2917.29	6.61	43.02	19.85	3.18	6.06
3051.38	3081.39	6.05	39.81	21.17	2.88	5.33
3215.49	3245.50	6.05	36.34	21.37	3.14	5.53
3379.59	3409.60	6.11	32.23	22.06	3.12	4.32
3543.69	3573.70	6.37	29.28	22.17	3.22	3.15
3707.79	3737.80	6.65	26.88	23.67	3.50	2.83
3871.90	3901.91	7.05	24.86	25.01	3.97	3.22
4036.00	4066.01	7.51	24.53	21.27	3.87	4.02
4200.10	4170.09	7.37	24.55	18.50	3.78	5.45

Electrical Schematic



Notes
A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
C. The parts covered by this specification document are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/MCLStore/terms.jsp

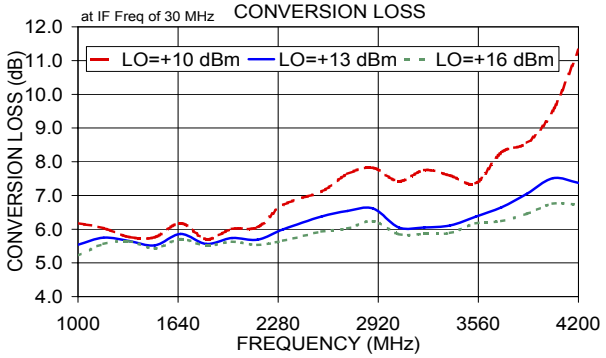
Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

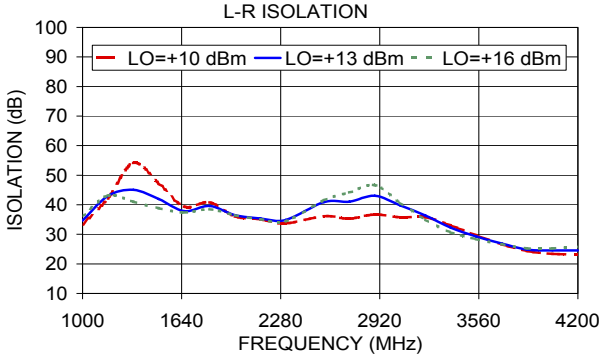
Performance Charts

ZX05-C42MH+

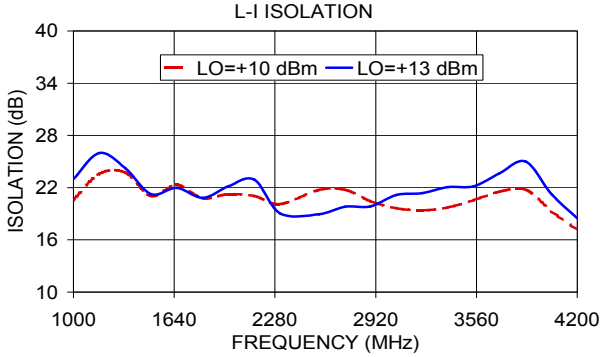
ZX05-C42MH+
CONVERSION LOSS
at IF Freq of 30 MHz



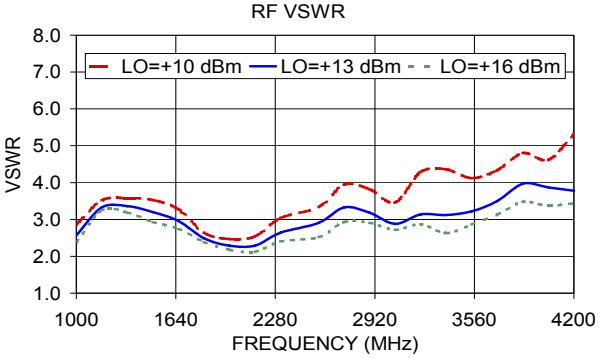
ZX05-C42MH+
L-R ISOLATION



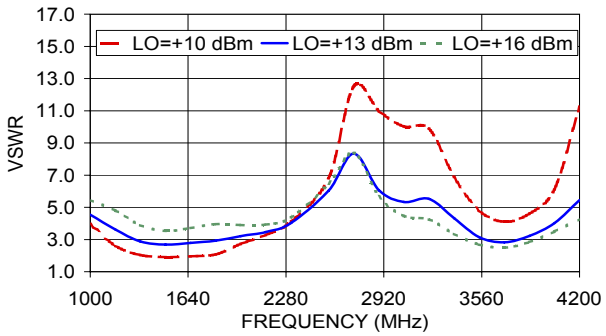
ZX05-C42MH+
L-I ISOLATION



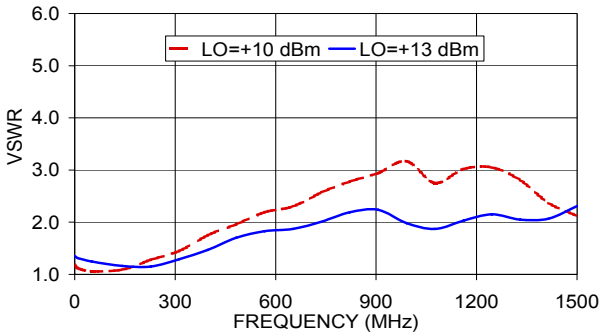
ZX05-C42MH+
RF VSWR



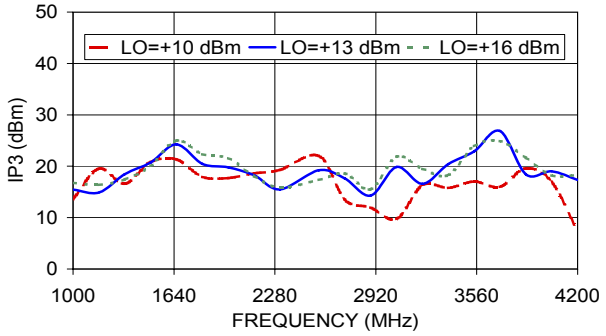
ZX05-C42MH+
LO VSWR



ZX05-C42MH+
IF VSWR



ZX05-C42MH+
IP3



Notes
A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
C. The parts covered by this specification document are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/MCLStore/terms.jsp

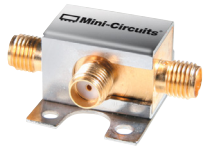
Tesis publicada con autorización del autor
No olvide citar esta tesis

DC Pass
TESIS PUCP

Power Splitter/Combiner

ZX10-2-42+

2 Way-0° 50Ω 1900 to 4200 MHz



CASE STYLE: FL905

Connectors	Model	Price	Qty.
SMA	ZX10-2-42-S+	$34.95	(1-24)

+RoHS Compliant
The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Maximum Ratings

Operating Temperature	-40°C to 85°C
Storage Temperature	-55°C to 100°C
Power Input (as a splitter)	1.0W max.
Internal Dissipation (as a combiner)	0.1W max.
DC Current	800 mA (400mA for each port)

Permanent damage may occur if any of these limits are exceeded.

DC Pass Connections

SUM PORT	3
PORT 1	1
PORT 2	2

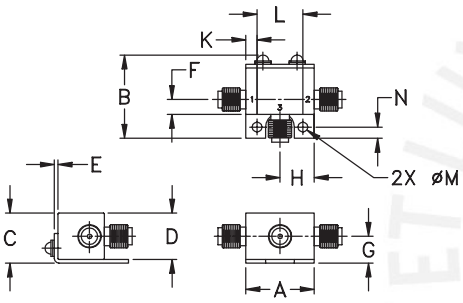
Features

- low insertion loss, 0.2 dB typ.
- excellent amplitude unbalance
- very good phase unbalance
- small size
- low cost
- protected under U.S. Patent 6,790,049 & 6,963,255

Applications

- communications
- defense
- PCS/DCS
- DECT

Outline Drawing



Outline Dimensions (inch / mm)

A	B	C	D	E	F	G
.74	.90	.54	.50	.04	.16	.29
18.80	22.86	13.72	12.70	1.02	4.06	7.37

H	J	K	L	M	N	wt
.37	--	.122	.496	.106	.122	grams
9.40	--	3.10	12.60	2.69	3.10	20.0

Electrical Specifications (T_{AMB}=25°C)

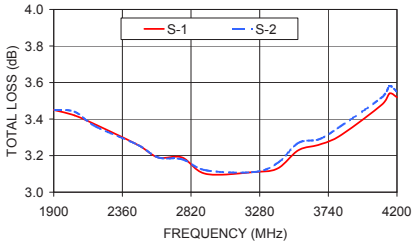
FREQ. RANGE (MHz)	ISOLATION (dB)		INSERTION LOSS (dB) ABOVE 3.0 dB		PHASE UNBALANCE (Degrees)	AMPLITUDE UNBALANCE (dB)
f_L-f_U	Typ.	Min	Typ.	Max.	Max.	Max.
1900-4200	**23**	**10**	**0.2**	**1.2**	**5.0**	**0.3**
2600-3400	23	17	0.2	0.6	4.0	0.3

Typical Performance Data

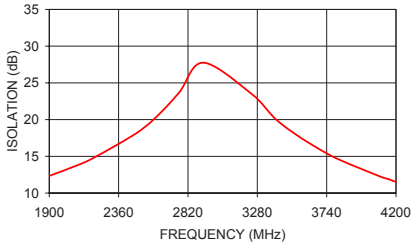
Frequency (MHz)	Total Loss[1] (dB)		Amplitude Unbalance (dB)	Isolation (dB)	Phase Unbalance (deg.)	VSWR S	VSWR 1	VSWR 2
	S-1	S-2						
1900.00	3.45	3.45	0.00	12.33	0.70	1.79	1.08	1.07
2040.00	3.42	3.44	0.02	13.42	0.71	1.71	1.09	1.08
2180.00	3.37	3.36	0.01	14.64	0.74	1.62	1.10	1.09
2460.00	3.26	3.26	0.01	17.92	0.91	1.47	1.09	1.08
2600.00	3.19	3.19	0.00	20.16	1.05	1.39	1.08	1.08
2760.00	3.19	3.18	0.01	23.66	1.02	1.26	1.05	1.05
2920.00	3.10	3.12	0.02	27.75	1.18	1.14	1.02	1.03
3240.00	3.11	3.11	0.00	23.53	1.50	1.07	1.03	1.02
3400.00	3.13	3.16	0.03	20.10	1.54	1.19	1.05	1.10
3540.00	3.23	3.27	0.04	17.91	1.30	1.31	1.07	1.05
3680.00	3.26	3.29	0.03	16.12	1.55	1.40	1.07	1.06
3820.00	3.31	3.36	0.05	14.58	1.52	1.51	1.09	1.08
4100.00	3.48	3.52	0.03	12.21	1.48	1.78	1.15	1.15
4150.00	3.54	3.58	0.04	11.90	1.37	1.83	1.16	1.16
4200.00	3.52	3.55	0.03	11.51	1.50	1.87	1.17	1.18

1. Total Loss = Insertion Loss + 3dB splitter loss.

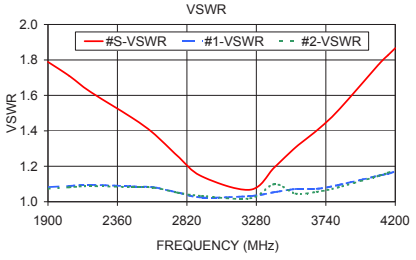
ZX10-2-42+
TOTAL LOSS



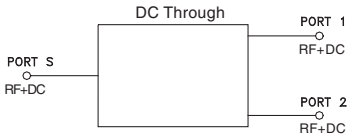
ZX10-2-42+
ISOLATION



ZX10-2-42+
VSWR



electrical schematic



Notes
A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
C. The parts covered by this specification document are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/MCLStore/terms.jsp

Tesis p
No olv

TESIS PUCP
Coaxial

Low Noise Amplifier

ZX60-272LN+

50Ω 2300 to 2700 MHz

Features

- Ultra low noise figure, 0.8 dB typ.
- Output power, up to +18.5 dBm typ.
- Good output IP3, 31.5 dBm typ.
- Good return loss
- Unconditionally stable
- Protected by US patent 6,790,049

Applications

- WiMAX 2.5GHz
- Base transceiver station, tower mounted amplifier, repeater
- General purpose low noise amplifier
- Lab
- Instrumentation
- Test equipment

Case Style: GA955

Connectors	Model	Price	Qty.
SMA	ZX60-272LN-S+	$39.95 ea.	(1-9)

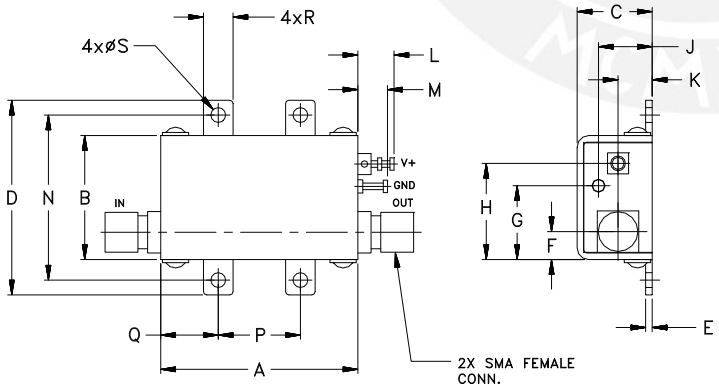
+RoHS Compliant

The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Electrical Specifications at 25°C

Parameter	Condition (MHz)	Min.	Typ.	Max.	Units
Frequency Range		2300		2700	MHz
Noise Figure	2300-2700		0.8	1.1	dB
Gain	2300-2700	11.5	14.0		dB
Gain Flatness	2300-2700		± 0.55	± 1.1	dB
Output Power at 1dB compression	2300-2700	16.0	18.5		dBm
Output third order intercept point (OIP3)	2300-2700		31.5		dBm
Input VSWR	2300-2700		1.2		:1
Output VSWR	2300-2700		1.6		:1
Active Directivity	2300-2700		7		dB
DC Supply Voltage			5.0		V
Supply Current			55	70	mA

Outline Drawing



Maximum Ratings

Parameter	Ratings
Operating Temperature	-40°C to 85°C Case
Storage Temperature	-55°C to 100°C
DC Voltage	5.5 V
Input RF Power (no damage)	+17 dBm
Power Consumption	400 mW

Permanent damage may occur if any of these limits are exceeded.

Outline Dimensions (inch / mm)

A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	wt.
1.20	.75	.46	1.18	.04	.17	.45	.59	.33	.21	.22	.18	1.00	.50	.35	.18	.106	grams
30.48	19.05	11.68	29.97	1.02	4.32	11.43	14.99	8.38	5.33	5.59	4.57	25.40	12.70	8.89	4.57	2.69	35.0

Notes: 1. Performance and quality attributes and conditions not expressly stated in this specification sheet are intended to be excluded and do not form a part of this specification sheet. **2.** Electrical specifications and performance data contained herein are based on Mini-Circuit's applicable established test performance criteria and measurement instructions. **3.** The parts covered by this specification sheet are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/MCLStore/terms.jsp.

REV. A
M124841
EDR-9796/5
ZX60-272LN+
RAV
121022

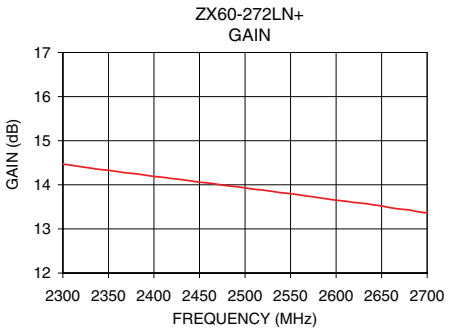
Tesis publicada con autorización del autor
No olvide citar esta tesis

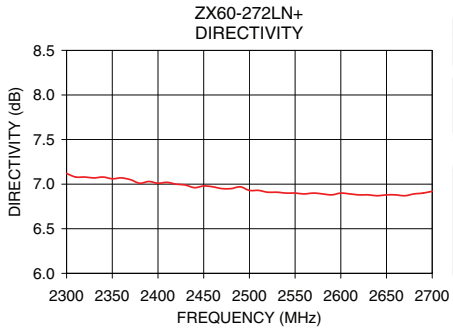
TESIS PUCP

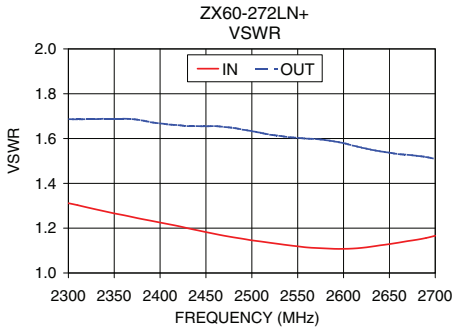
Typical Performance Data/Curves

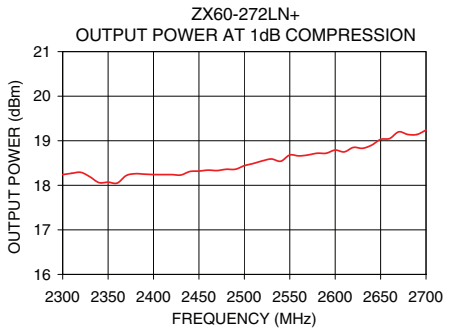
ZX60-272LN+

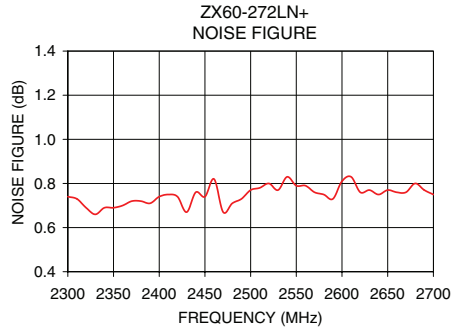
FREQUENCY (MHz)	GAIN (dB)	DIRECTIVITY (dB)	VSWR IN (:1)	VSWR OUT (:1)	POWER OUT @ 1dB COMPRESSION (dBm)	OUTPUT IP3 (dBm)	NF (dB)
2300.00	14.47	7.12	1.31	1.69	18.24	31.83	0.74
2320.00	14.41	7.08	1.29	1.69	18.29	31.42	0.69
2340.00	14.35	7.08	1.27	1.69	18.06	31.78	0.69
2360.00	14.30	7.07	1.26	1.69	18.05	32.10	0.70
2380.00	14.25	7.01	1.24	1.68	18.26	30.83	0.72
2400.00	14.19	7.01	1.23	1.67	18.24	31.89	0.74
2420.00	14.14	7.00	1.21	1.66	18.24	32.98	0.74
2440.00	14.09	6.96	1.19	1.66	18.31	29.71	0.76
2460.00	14.04	6.97	1.17	1.66	18.34	30.51	0.82
2480.00	13.98	6.95	1.16	1.65	18.36	34.00	0.71
2500.00	13.93	6.93	1.15	1.63	18.44	30.84	0.77
2520.00	13.88	6.91	1.13	1.62	18.55	30.31	0.80
2540.00	13.82	6.90	1.12	1.61	18.54	30.79	0.83
2560.00	13.77	6.89	1.11	1.60	18.66	31.57	0.79
2580.00	13.71	6.89	1.11	1.59	18.72	31.01	0.75
2600.00	13.65	6.90	1.11	1.58	18.79	31.36	0.81
2620.00	13.60	6.88	1.11	1.56	18.85	31.41	0.76
2640.00	13.55	6.87	1.12	1.54	18.90	30.90	0.75
2680.00	13.43	6.89	1.15	1.52	19.14	30.29	0.80
2700.00	13.36	6.92	1.17	1.51	19.24	31.47	0.75

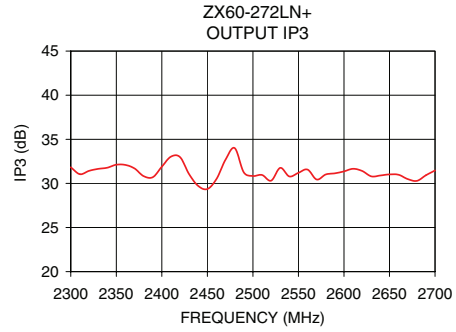












Notes: 1. Performance and quality attributes and conditions not expressly stated in this specification sheet are intended to be excluded and do not form a part of this specification sheet. **2.** Electrical specifications and performance data contained herein are based on Mini-Circuit's applicable established test performance criteria and measurement instructions. **3.** The parts covered by this specification sheet are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/MCLStore/terms.jsp.

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

Coaxial

Voltage Controlled Oscillator ZX95-2510+

5V Tuning for PLL IC's 2300 to 2510 MHz

Features

- low phase noise
- low pulling
- low pushing
- protected by US patent 6,790,049

Applications

- r & d
- lab
- instrumentation
- wireless communications
- WiMAX 2.5 GHz

CASE STYLE: GB956

Connectors	Model	Price	Qty.
SMA	ZX95-2510-S+	$ 44.95 ea.	(1-9)

+RoHS Compliant

The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Electrical Specifications

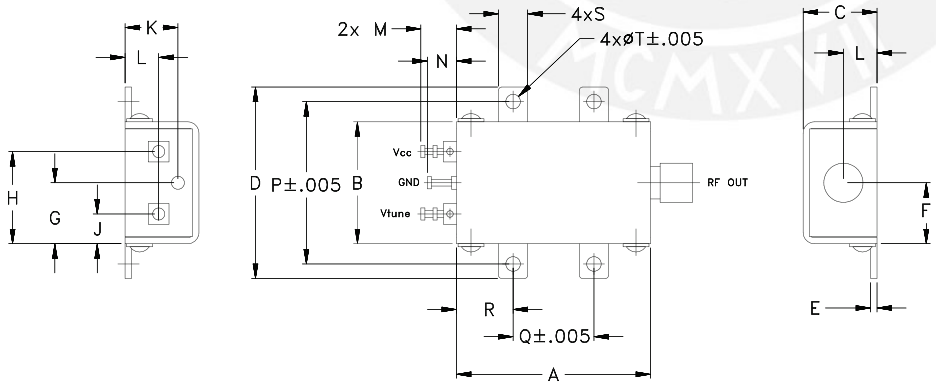
MODEL NO.	FREQ. (MHz)		POWER OUTPUT (dBm)	PHASE NOISE dBc/Hz SSB at offset frequencies,kHz Typ.				TUNING					NON HARMONIC SPURIOUS (dBc)	HARMONICS (dBc)		PULLING pk-pk @12 dBr (MHz)	PUSHING (MHz/V)	DC OPERATING POWER	
								VOLTAGE RANGE (V)		SENSI-TIVITY (MHz/V)	PORT CAP (pF)	3 dB MODULATION BANDWIDTH (MHz)						Vcc (volts)	Current (mA)
	Min.	Max.	Typ.	1	10	100	1000	Min.	Max.	Typ.	Typ.	Typ.	Typ.	Typ.	Max.	Typ.	Typ.		Max.
ZX95-2510+	2300	2510	+4	-69	-96	-118	-138	0.5	5	85-103	40	35	-90	-18	-10	0.8	1	5	40

Maximum Ratings

Operating Temperature	-55°C to 85°C
Storage Temperature	-55°C to 100°C
Absolute Max. Supply Voltage (Vcc)	7V
Absolute Max. Tuning Voltage (Vtune)	7V
All specifications	50 ohm system

Permanent damage may occur if any of these limits are exceeded.

Outline Drawing



Outline Dimensions (inch / mm)

A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	wt.
1.20	**.75**	**.46**	**1.18**	**.04**	**.38**	**.38**	**.57**	**.18**	**.33**	**.21**	**.22**	**.18**	**1.00**	**.50**	**.35**	**.18**	**.106**	grams
30.48	19.05	11.68	29.97	1.02	9.65	9.65	14.48	4.57	8.38	5.33	5.59	4.57	25.40	12.70	8.89	4.57	2.69	35.0

Notes: 1. Performance and quality attributes and conditions not expressly stated in this specification sheet are intended to be excluded and do not form a part of this specification sheet. 2. Electrical specifications and performance data contained herein are based on Mini-Circuit's applicable established test performance criteria and measurement instructions. 3. The parts covered by this specification sheet are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and warranty information and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/MCLStore/terms.jsp.

Tesis publicada con autorización del autor
No olvide citar esta tesis

TESIS PUCP

PONTIFICIA UNIVERSIDAD CATÓLICA DEL PERÚ

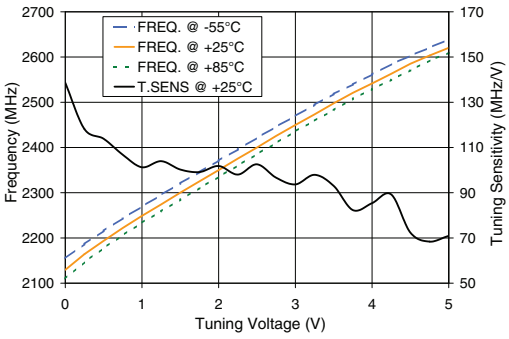
Performance Data & Curves*

ZX95-2510+

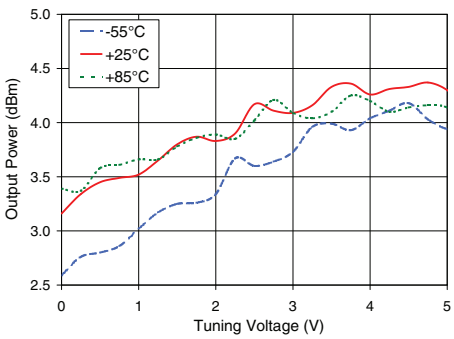
V TUNE	TUNE SENS (MHz/V)	FREQUENCY (MHz)			POWER OUTPUT (dBm)			Icc (mA)	HARMONICS (dBc)			FREQ. PUSH (MHz/V)	FREQ. PULL (MHz)	PHASE NOISE (dBc/Hz) at offsets				FREQ OFFSET (KHz)	PHASE NOISE at 2405 MHz (dBc/Hz)
		-55°C	+25°C	+85°C	-55°C	+25°C	+85°C		F2	F3	F4			1kHz	10kHz	100kHz	1MHz		
0.00	138.62	2155.0	2129.5	2110.1	2.59	3.16	3.39	32.59	-20.7	-16.4	-32.3	3.70	0.36	-69.2	-96.2	-118.5	-138.6	1.0	-69.22
0.50	113.85	2216.0	2193.7	2177.7	2.80	3.45	3.58	32.72	-20.0	-18.7	-32.6	1.15	0.50	-70.6	-97.0	-119.2	-139.3	2.0	-78.04
0.75	106.77	2243.7	2222.2	2205.9	2.86	3.49	3.61	32.69	-20.7	-18.4	-31.0	0.77	0.19	-68.5	-96.8	-118.9	-139.0	3.5	-85.27
1.00	101.26	2269.4	2248.9	2233.7	3.02	3.52	3.66	32.74	-19.0	-19.7	-29.1	0.64	0.52	-70.0	-97.2	-119.4	-139.4	6.0	-91.04
1.25	103.96	2295.5	2274.2	2259.2	3.17	3.65	3.66	32.69	-19.4	-21.7	-30.1	0.50	0.10	-69.8	-96.8	-118.8	-138.8	8.5	-94.71
1.50	100.26	2320.9	2300.2	2284.5	3.25	3.80	3.78	32.61	-18.8	-24.1	-32.3	0.33	0.52	-69.0	-96.0	-118.4	-138.4	10.0	-96.30
1.75	99.13	2345.6	2325.3	2310.5	3.26	3.87	3.86	32.62	-18.8	-25.3	-33.6	0.35	0.45	-68.6	-96.7	-118.8	-138.9	20.8	-103.44
2.00	101.80	2371.1	2350.1	2335.1	3.34	3.83	3.89	32.54	-17.8	-30.4	-36.4	0.32	0.40	-68.8	-96.3	-118.3	-138.4	35.5	-108.50
2.25	98.02	2395.8	2375.5	2360.3	3.67	3.90	3.85	32.47	-18.2	-35.8	-41.9	0.39	0.80	-69.0	-96.3	-118.4	-138.5	60.7	-113.24
2.50	102.57	2421.3	2400.0	2385.4	3.60	4.17	4.02	32.38	-17.9	-36.4	-43.8	0.70	0.45	-69.4	-96.2	-118.1	-138.1	85.2	-116.48
2.75	96.65	2446.1	2425.6	2410.0	3.64	4.11	4.21	32.29	-18.2	-32.4	-54.1	1.11	0.87	-68.2	-95.1	-117.1	-137.2	100.0	-117.94
3.00	93.70	2469.8	2449.8	2436.0	3.73	4.09	4.09	32.27	-17.1	-29.7	-57.5	1.68	1.18	-69.2	-96.1	-118.1	-138.2	142.9	-121.06
3.25	97.94	2494.4	2473.2	2459.1	3.96	4.16	4.04	32.14	-17.2	-26.8	-56.6	2.31	0.64	-69.8	-95.5	-117.3	-137.4	167.8	-122.56
3.50	93.02	2518.3	2497.7	2482.7	3.99	4.33	4.10	31.98	-17.1	-26.7	-50.2	2.87	1.58	-69.9	-96.3	-118.1	-138.2	200.6	-124.04
3.75	82.31	2539.4	2521.0	2507.8	3.93	4.36	4.25	32.01	-17.2	-25.7	-47.9	3.41	1.50	-69.5	-96.5	-118.2	-138.4	281.6	-127.09
4.00	85.38	2561.3	2541.6	2528.9	4.04	4.26	4.20	31.92	-16.6	-25.7	-47.8	4.00	0.90	-68.5	-95.4	-117.3	-137.4	330.7	-128.56
4.25	89.27	2584.2	2562.9	2549.6	4.11	4.31	4.10	31.78	-16.7	-25.7	-48.4	4.34	1.69	-68.6	-94.3	-116.5	-136.7	464.2	-131.46
4.50	72.37	2602.8	2585.2	2570.7	4.18	4.33	4.14	31.66	-17.3	-26.3	-48.5	4.73	2.18	-69.2	-95.4	-117.1	-137.3	554.9	-132.99
4.75	68.40	2620.7	2603.3	2592.2	4.03	4.37	4.16	31.65	-16.8	-27.2	-47.5	3.98	1.61	-70.4	-95.9	-117.4	-137.6	914.6	-137.22
5.00	70.90	2638.9	2620.4	2609.2	3.94	4.30	4.14	31.55	-17.4	-26.9	-48.3	4.08	1.74	-70.4	-94.8	-116.4	-136.6	1000.0	-138.00

*at 25°C unless mentioned otherwise

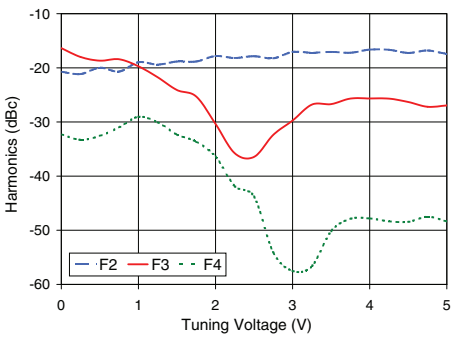
ZX95-2510+
Frequency and Tuning Sensitivity



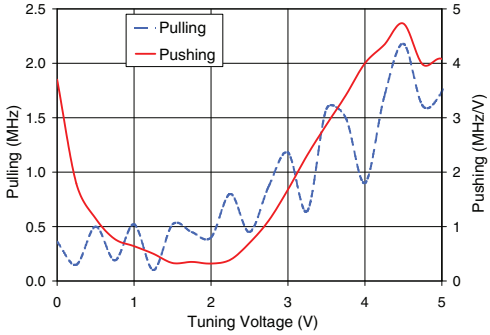
ZX95-2510+
Power Output



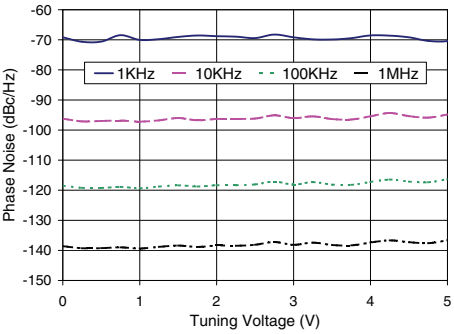
ZX95-2510+
Harmonics Level



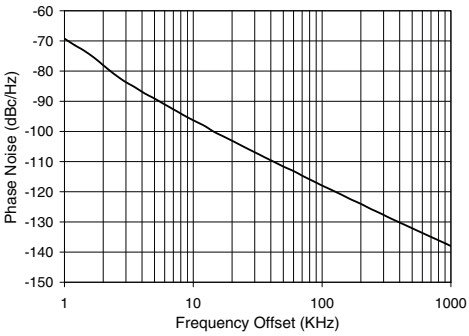
ZX95-2510+
Frequency Pulling & Pushing (Vcc ± 5%)



ZX95-2510+
Phase Noise Vs. Tuning Voltage



ZX95-2510+
Phase Noise



Mini-Circuits®
ISO 9001 ISO 14001 AS 9100 CERTIFIED

For detailed performance specs & shopping online see web site

P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4661 The Design Engineers Search Engine Provides ACTUAL Data Instantly at minicircuits.com

IF/RF MICROWAVE COMPONENTS

Notes: 1. Performance and quality attributes and conditions not expressly stated in this specification sheet are intended to be excluded and do not form a part of this specification sheet. 2. Electrical specifications and performance data contained herein are based on Mini-Circuit's applicable established test performance criteria and measurement instructions. 3. The parts covered by this specification sheet are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and your rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/MCLStore/terms.jsp.

Tesis publicada con autorización del autor
No olvide citar esta tesis