ANALOG DEVICES

Low Cost, Low Power Instrumentation Amplifier

AD620

FEATURES

EASY TO USE
- Gain Set with One External Resistor (Gain Range 1 to 1000)
- Wide Power Supply Range (±2.3 V to ±18 V)
- Higher Performance than Three Op Amp IA Designs
- Available in 8-Lead DIP and SOIC Packaging
- Low Power, 1.3 mA max Supply Current

EXCELLENT DC PERFORMANCE ("B GRADE")
- 50 μV max, Input Offset Voltage
- 0.6 μV/°C max, Input Offset Drift
- 1.0 nA max, Input Bias Current
- 100 dB min Common-Mode Rejection Ratio (G = 10)

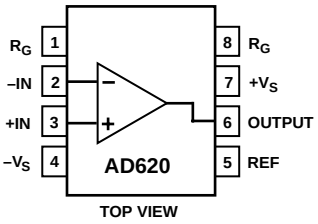
LOW NOISE
- 9 nV/√Hz, @ 1 kHz, Input Voltage Noise
- 0.28 μV p-p Noise (0.1 Hz to 10 Hz)

EXCELLENT AC SPECIFICATIONS
- 120 kHz Bandwidth (G = 100)
- 15 μs Settling Time to 0.01%

APPLICATIONS
- Weigh Scales
- ECG and Medical Instrumentation
- Transducer Interface
- Data Acquisition Systems
- Industrial Process Controls
- Battery Powered and Portable Equipment

CONNECTION DIAGRAM

8-Lead Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



TOP VIEW

PRODUCT DESCRIPTION

The AD620 is a low cost, high accuracy instrumentation amplifier that requires only one external resistor to set gains of 1 to 1000. Furthermore, the AD620 features 8-lead SOIC and DIP packaging that is smaller than discrete designs, and offers lower power (only 1.3 mA max supply current), making it a good fit for battery powered, portable (or remote) applications.

The AD620, with its high accuracy of 40 ppm maximum nonlinearity, low offset voltage of 50 μV max and offset drift of 0.6 μV/°C max, is ideal for use in precision data acquisition systems, such as weigh scales and transducer interfaces. Furthermore, the low noise, low input bias current, and low power of the AD620 make it well suited for medical applications such as ECG and noninvasive blood pressure monitors.

The low input bias current of 1.0 nA max is made possible with the use of Superβeta processing in the input stage. The AD620 works well as a preamplifier due to its low input voltage noise of 9 nV/√Hz at 1 kHz, 0.28 μV p-p in the 0.1 Hz to 10 Hz band, 0.1 pA/√Hz input current noise. Also, the AD620 is well suited for multiplexed applications with its settling time of 15 μs to 0.01% and its cost is low enough to enable designs with one in-amp per channel.

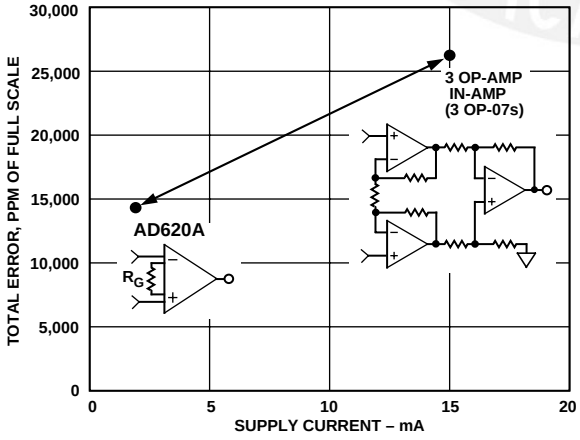


Figure 1. Three Op Amp IA Designs vs. AD620

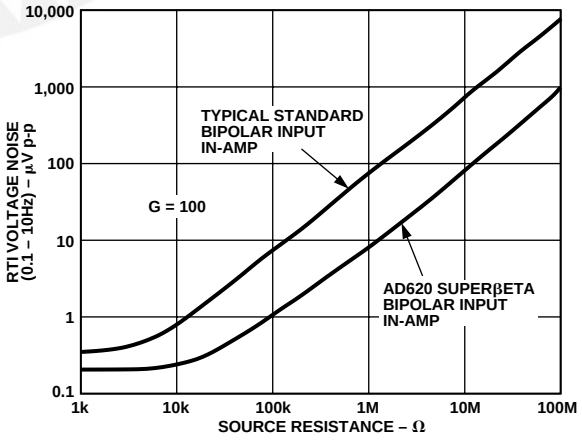


Figure 2. Total Voltage Noise vs. Source Resistance

REV. E

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AD620—SPECIFICATIONS

(Typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted)

Model	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Units
GAIN	G = 1 + (49.4 k/R_G)										
Gain Range		1		10,000	1		10,000	1		10,000	
Gain Error[2]	V_{OUT} = ±10 V										
G = 1			0.03	0.10		0.01	0.02		0.03	0.10	%
G = 10			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 100			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 1000			0.40	0.70		0.35	0.50		0.40	0.70	%
Nonlinearity,	V_{OUT} = –10 V to +10 V,										
G = 1–1000	R_L = 10 kΩ		10	40		10	40		10	40	ppm
G = 1–100	R_L = 2 kΩ		10	95		10	95		10	95	ppm
Gain vs. Temperature											
	G =1			10			10			10	ppm/°C
	Gain >1[2]			–50			–50			–50	ppm/°C
VOLTAGE OFFSET	(Total RTI Error = V_{OSI} + V_{OSO}/G)										
Input Offset, V_{OSI}	V_S = ±5 V to ±15 V		30	125		15	50		30	125	µV
Over Temperature	V_S = ±5 V to ±15 V			185			85			225	µV
Average TC	V_S = ±5 V to ±15 V		0.3	1.0		0.1	0.6		0.3	1.0	µV/°C
Output Offset, V_{OSO}	V_S = ±15 V		400	1000		200	500		400	1000	µV
	V_S = ±5 V			1500			750			1500	µV
Over Temperature	V_S = ±5 V to ±15 V			2000			1000			2000	µV
Average TC	V_S = ±5 V to ±15 V		5.0	15		2.5	7.0		5.0	15	µV/°C
Offset Referred to the Input vs. Supply (PSR)	V_S = ±2.3 V to ±18 V										
G = 1		80	100		80	100		80	100		dB
G = 10		95	120		100	120		95	120		dB
G = 100		110	140		120	140		110	140		dB
G = 1000		110	140		120	140		110	140		dB
INPUT CURRENT											
Input Bias Current			0.5	2.0		0.5	1.0		0.5	2	nA
Over Temperature				2.5			1.5			4	nA
Average TC			3.0			3.0			8.0		pA/°C
Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
Over Temperature				1.5			0.75			2.0	nA
Average TC			1.5			1.5			8.0		pA/°C
INPUT											
Input Impedance											
Differential			10‖2			10‖2			10‖2		GΩ‖pF
Common-Mode			10‖2			10‖2			10‖2		GΩ‖pF
Input Voltage Range[3]	V_S = ±2.3 V to ±5 V	$–V_S$ + 1.9		$+V_S$ – 1.2	$–V_S$ + 1.9		$+V_S$ – 1.2	$–V_S$ + 1.9		$+V_S$ – 1.2	V
Over Temperature		$–V_S$ + 2.1		$+V_S$ – 1.3	$–V_S$ + 2.1		$+V_S$ – 1.3	$–V_S$ + 2.1		$+V_S$ – 1.3	V
	V_S = ±5 V to ±18 V	$–V_S$ + 1.9		$+V_S$ – 1.4	$–V_S$ + 1.9		$+V_S$ – 1.4	$–V_S$ + 1.9		$+V_S$ – 1.4	V
Over Temperature		$–V_S$ + 2.1		$+V_S$ – 1.4	$–V_S$ + 2.1		$+V_S$ – 1.4	$–V_S$ + 2.3		$+V_S$ – 1.4	V
Common-Mode Rejection Ratio DC to 60 Hz with I kΩ Source Imbalance	V_{CM} = 0 V to ±10 V										
G = 1		73	90		80	90		73	90		dB
G = 10		93	110		100	110		93	110		dB
G = 100		110	130		120	130		110	130		dB
G = 1000		110	130		120	130		110	130		dB
OUTPUT											
Output Swing	R_L = 10 kΩ,										
	V_S = ±2.3 V to ±5 V	$–V_S$ + 1.1		$+V_S$ – 1.2	$–V_S$ + 1.1		$+V_S$ – 1.2	$–V_S$ + 1.1		$+V_S$ – 1.2	V
Over Temperature		$–V_S$ + 1.4		$+V_S$ – 1.3	$–V_S$ + 1.4		$+V_S$ – 1.3	$–V_S$ + 1.6		$+V_S$ – 1.3	V
	V_S = ±5 V to ±18 V	$–V_S$ + 1.2		$+V_S$ – 1.4	$–V_S$ + 1.2		$+V_S$ – 1.4	$–V_S$ + 1.2		$+V_S$ – 1.4	V
Over Temperature		$–V_S$ + 1.6		$+V_S$ – 1.5	$–V_S$ + 1.6		$+V_S$ – 1.5	$–V_S$ + 2.3		$+V_S$ – 1.5	V
Short Current Circuit			±18			±18			±18		mA

Model	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Units
DYNAMIC RESPONSE											
Small Signal –3 dB Bandwidth											
G = 1			1000			1000			1000		kHz
G = 10			800			800			800		kHz
G = 100			120			120			120		kHz
G = 1000			12			12			12		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/µs
Settling Time to 0.01%	10 V Step										
G = 1–100			15			15			15		µs
G = 1000			150			150			150		µs
NOISE											
Voltage Noise, 1 kHz	$Total\ RTI\ Noise = \sqrt{(e^2_{ni}) + (e_{no}/G)^2}$										
Input, Voltage Noise, e_{ni}			9	13		9	13		9	13	nV/√Hz
Output, Voltage Noise, e_{no}			72	100		72	100		72	100	nV/√Hz
RTI, 0.1 Hz to 10 Hz											
G = 1			3.0			3.0	6.0		3.0	6.0	µV p-p
G = 10			0.55			0.55	0.8		0.55	0.8	µV p-p
G = 100–1000			0.28			0.28	0.4		0.28	0.4	µV p-p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
0.1 Hz to 10 Hz			10			10			10		pA p-p
REFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN+}, V_{REF} = 0		+50	+60		+50	+60		+50	+60	µA
Voltage Range		$-V_S$ + 1.6		$+V_S$ – 1.6	$-V_S$ + 1.6		$+V_S$ – 1.6	$-V_S$ + 1.6		$+V_S$ – 1.6	V
Gain to Output			1 ± 0.0001			1 ± 0.0001			1 ± 0.0001		
POWER SUPPLY											
Operating Range[4]		±2.3		±18	±2.3		±18	±2.3		±18	V
Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
Over Temperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
For Specified Performance		–40 to +85			–40 to +85			–55 to +125			°C

NOTES
[1]See Analog Devices military data sheet for 883B tested specifications.
[2]Does not include effects of external resistor R_G.
[3]One input grounded. G = 1.
[4]This is defined as the same supply range which is used to specify PSR.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 650 mW
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±25 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range (Q) . . . . . –65°C to +150°C
Storage Temperature Range (N, R) . . . . . –65°C to +125°C
Operating Temperature Range
AD620 (A, B) . . . . . –40°C to +85°C
AD620 (S) . . . . . –55°C to +125°C
Lead Temperature Range
(Soldering 10 seconds) . . . . . +300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Lead Plastic Package: θ_{JA} = 95°C/W
8-Lead Cerdip Package: θ_{JA} = 110°C/W
8-Lead SOIC Package: θ_{JA} = 155°C/W

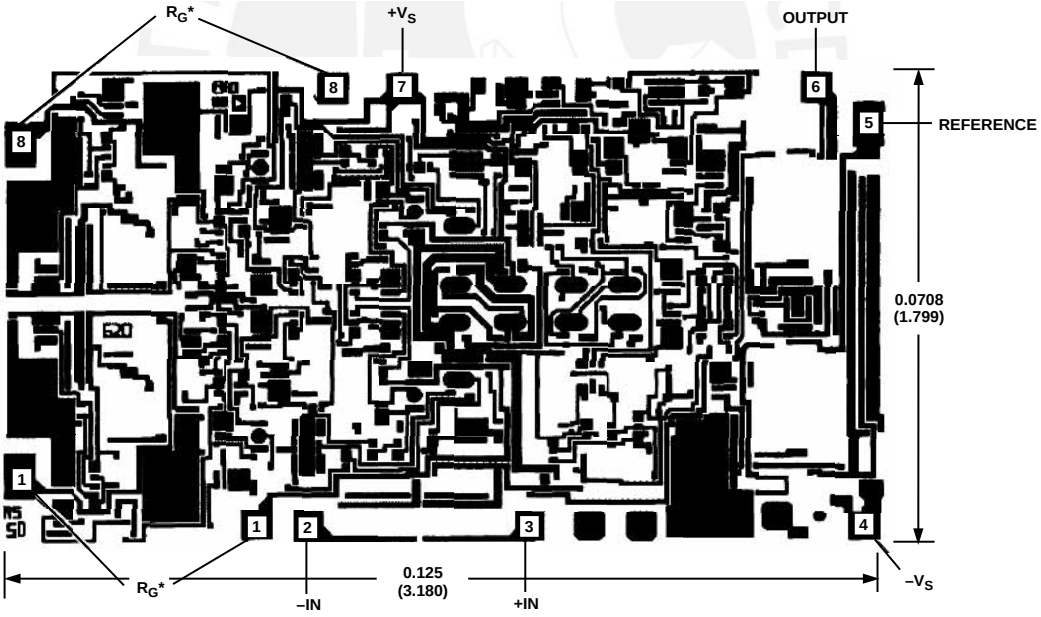
ORDERING GUIDE

Model	Temperature Ranges	Package Options*
AD620AN	–40°C to +85°C	N-8
AD620BN	–40°C to +85°C	N-8
AD620AR	–40°C to +85°C	SO-8
AD620AR-REEL	–40°C to +85°C	13" REEL
AD620AR-REEL7	–40°C to +85°C	7" REEL
AD620BR	–40°C to +85°C	SO-8
AD620BR-REEL	–40°C to +85°C	13" REEL
AD620BR-REEL7	–40°C to +85°C	7" REEL
AD620ACHIPS	–40°C to +85°C	Die Form
AD620SQ/883B	–55°C to +125°C	Q-8

*N = Plastic DIP; Q = Cerdip; SO = Small Outline.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



*FOR CHIP APPLICATIONS: THE PADS $1R_G$ AND $8R_G$ MUST BE CONNECTED IN PARALLEL TO THE EXTERNAL GAIN REGISTER R_G. DO NOT CONNECT THEM IN SERIES TO R_G. FOR UNITY GAIN APPLICATIONS WHERE R_G IS NOT REQUIRED, THE PADS $1R_G$ MAY SIMPLY BE BONDED TOGETHER, AS WELL AS THE PADS $8R_G$.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD620 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Typical Characteristics (@ +25°C, V_S = ±15 V, R_L = 2 kΩ, unless otherwise noted)

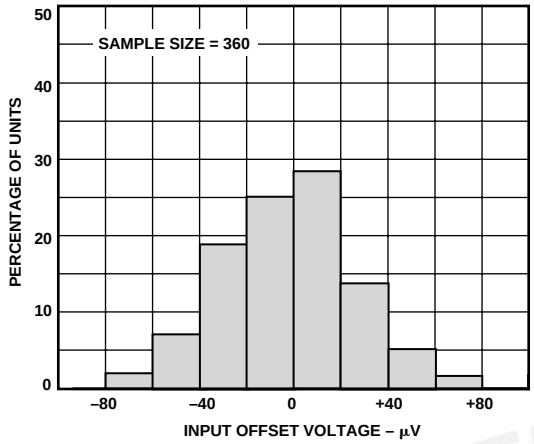


Figure 3. Typical Distribution of Input Offset Voltage

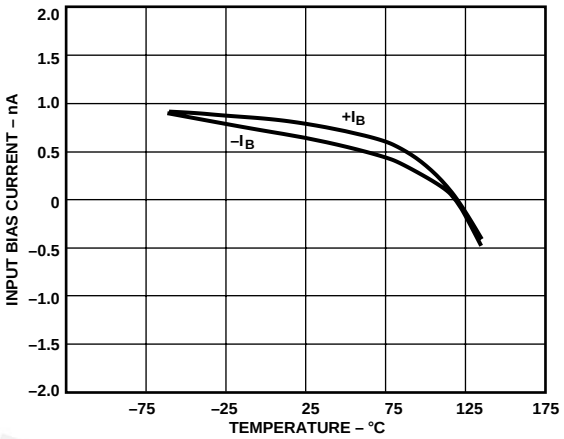


Figure 6. Input Bias Current vs. Temperature

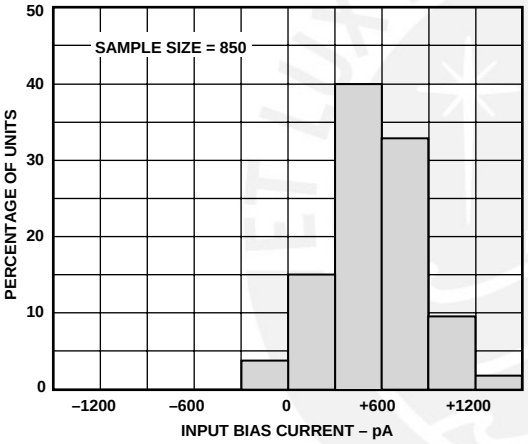


Figure 4. Typical Distribution of Input Bias Current

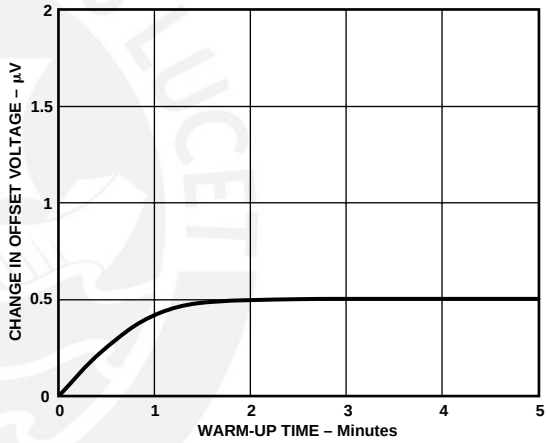


Figure 7. Change in Input Offset Voltage vs. Warm-Up Time

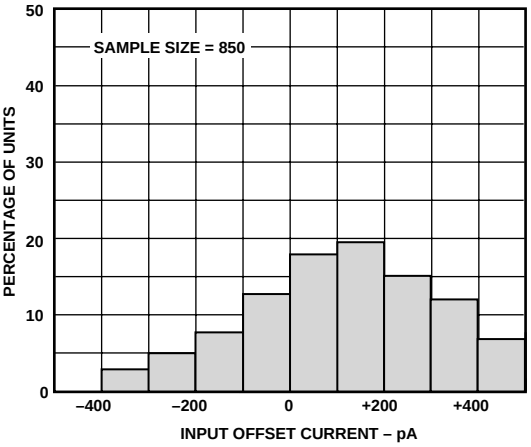


Figure 5. Typical Distribution of Input Offset Current

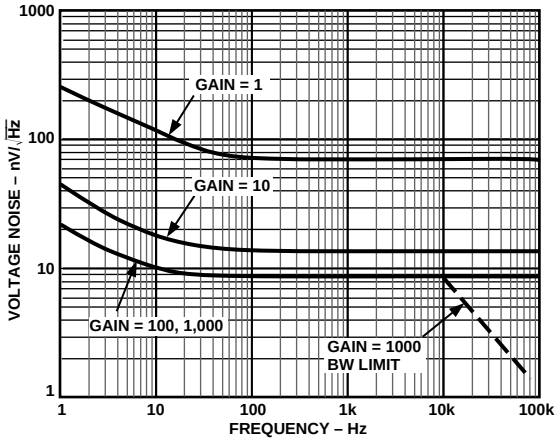


Figure 8. Voltage Noise Spectral Density vs. Frequency, (G = 1–1000)

AD620–Typical Characteristics

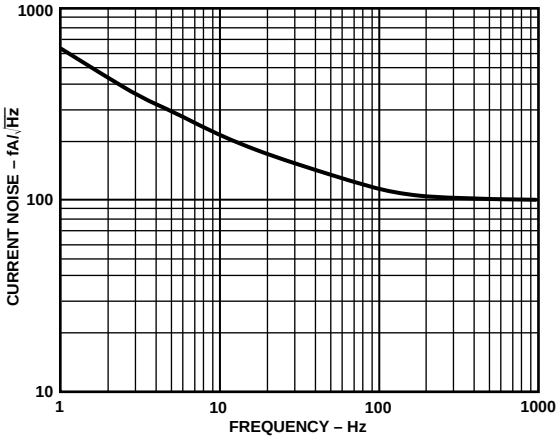


Figure 9. Current Noise Spectral Density vs. Frequency

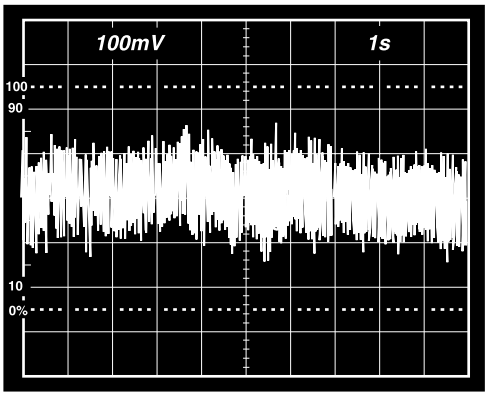


Figure 11. 0.1 Hz to 10 Hz Current Noise, 5 pA/Div

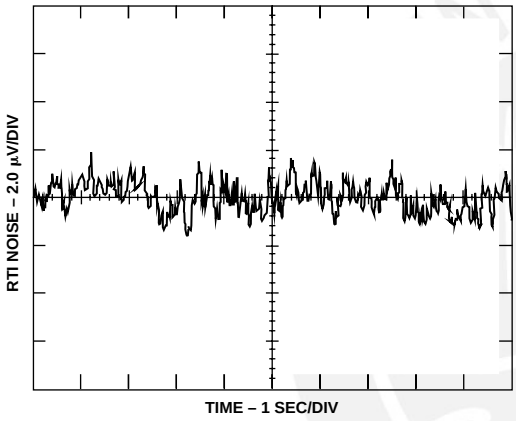


Figure 10a. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1)

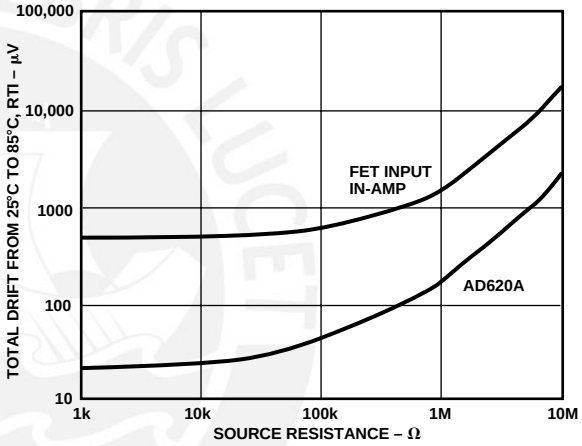


Figure 12. Total Drift vs. Source Resistance

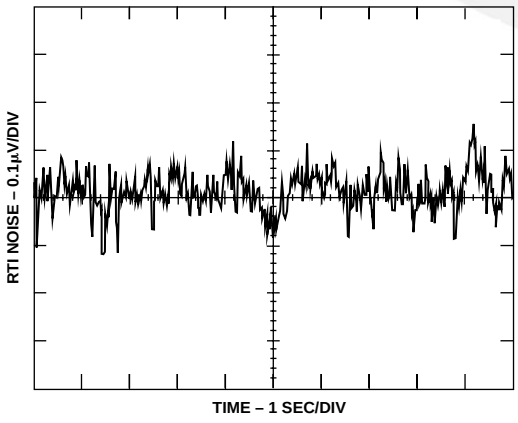


Figure 10b. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1000)

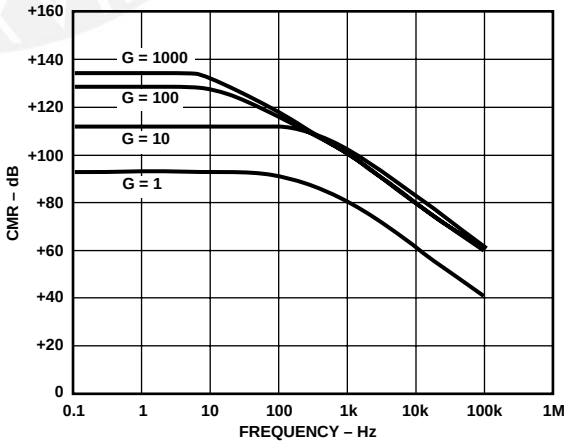


Figure 13. CMR vs. Frequency, RTI, Zero to 1 kΩ Source Imbalance

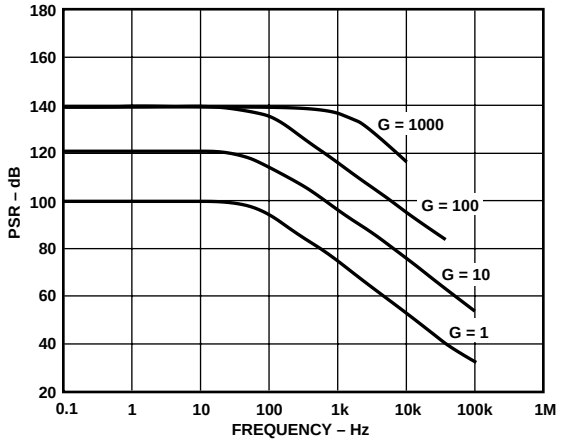


Figure 14. Positive PSR vs. Frequency, RTI (G = 1–1000)

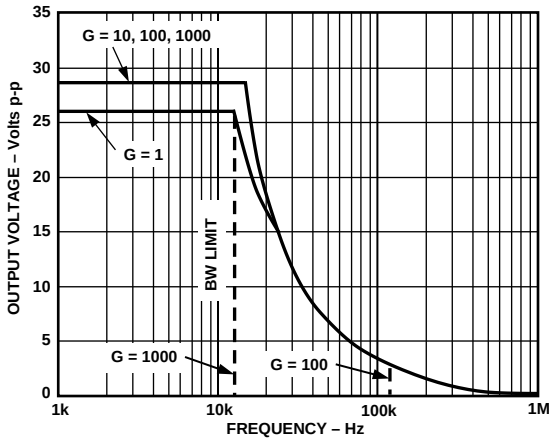


Figure 17. Large Signal Frequency Response

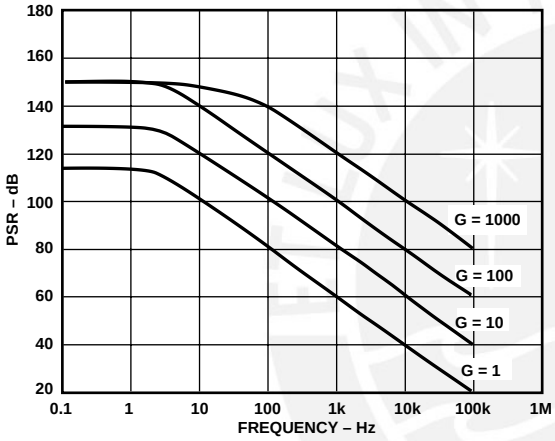


Figure 15. Negative PSR vs. Frequency, RTI (G = 1–1000)

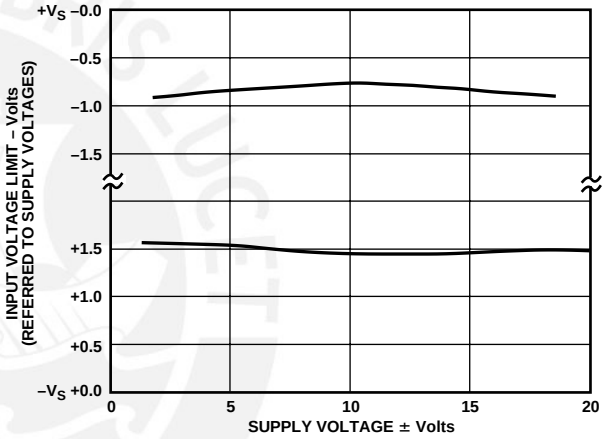


Figure 18. Input Voltage Range vs. Supply Voltage, G = 1

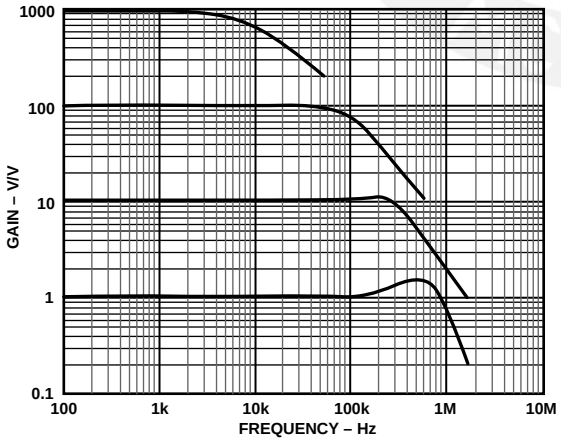


Figure 16. Gain vs. Frequency

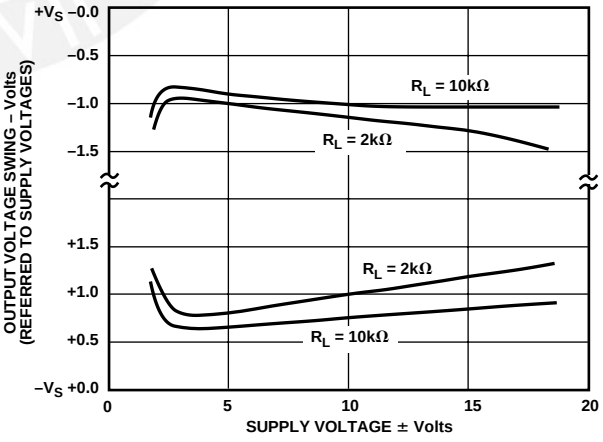


Figure 19. Output Voltage Swing vs. Supply Voltage, G = 10

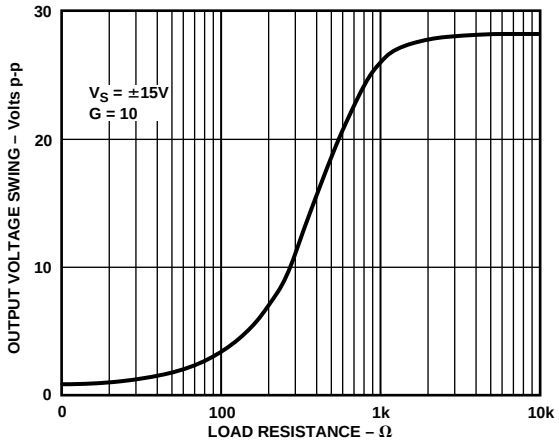


Figure 20. Output Voltage Swing vs. Load Resistance

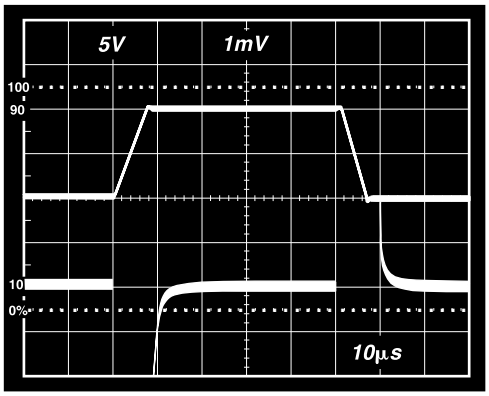


Figure 23. Large Signal Response and Settling Time, G = 10 (0.5 mV = 001%)

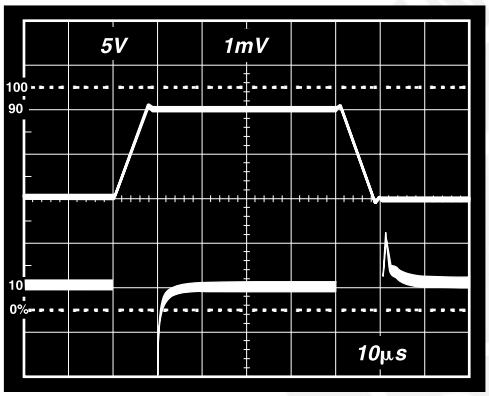


Figure 21. Large Signal Pulse Response and Settling Time G = 1 (0.5 mV = 0.01%)

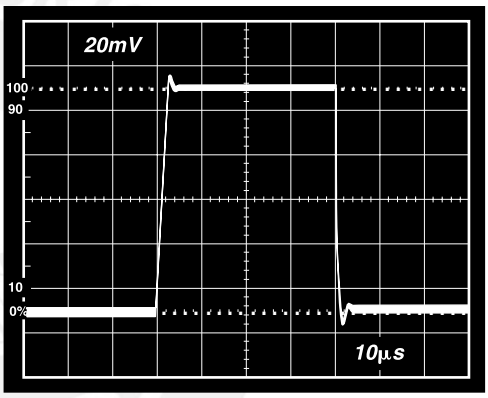


Figure 24. Small Signal Response, G = 10, R_L = 2 kΩ, C_L = 100 pF

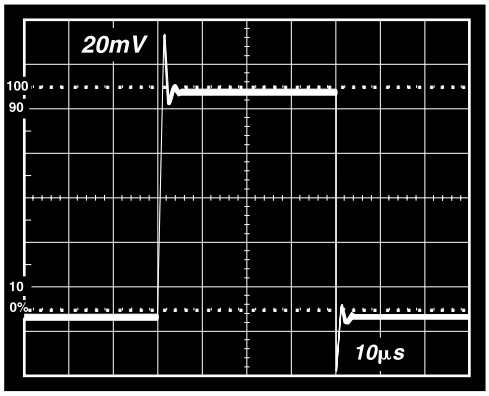


Figure 22. Small Signal Response, G = 1, R_L = 2 kΩ, C_L = 100 pF

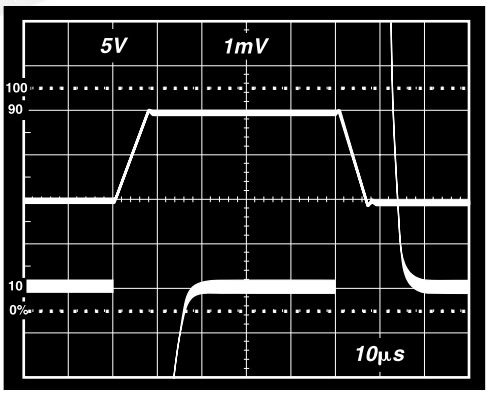


Figure 25. Large Signal Response and Settling Time, G = 100 (0.5 mV = 0.01%)

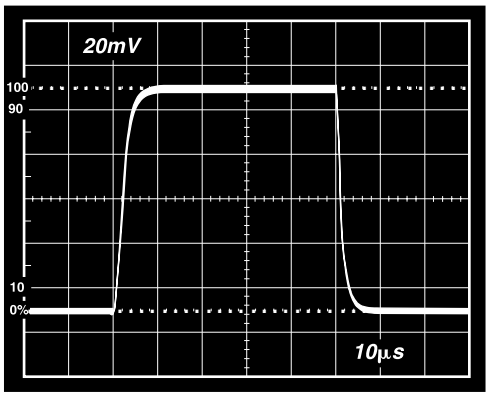


Figure 26. Small Signal Pulse Response, G = 100, R_L = 2 kΩ, C_L = 100 pF

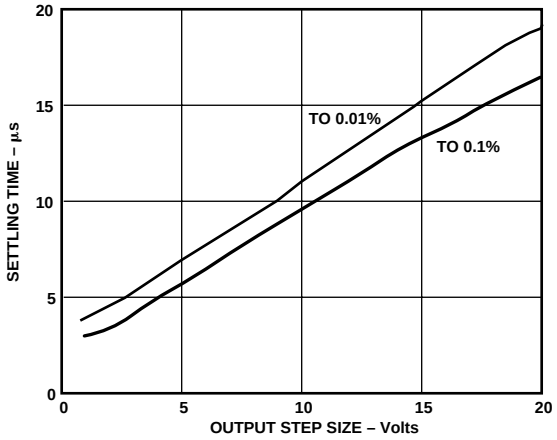


Figure 29. Settling Time vs. Step Size (G = 1)

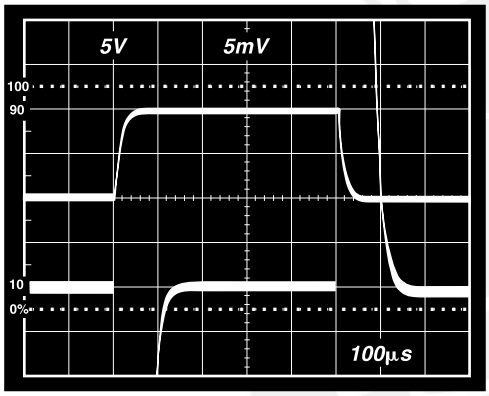


Figure 27. Large Signal Response and Settling Time, G = 1000 (0.5 mV = 0.01%)

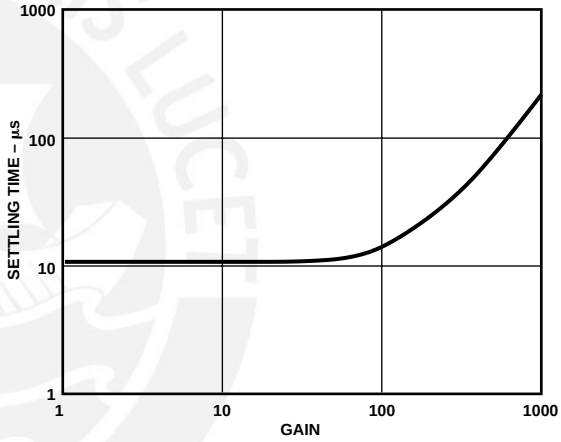


Figure 30. Settling Time to 0.01% vs. Gain, for a 10 V Step

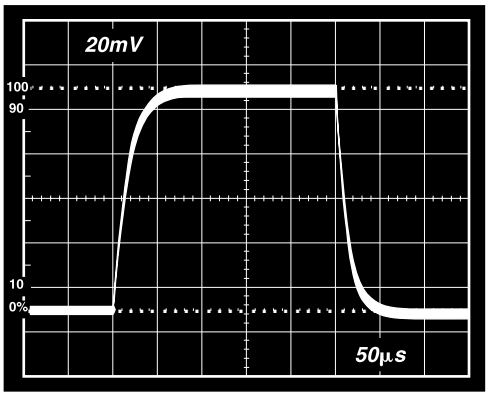


Figure 28. Small Signal Pulse Response, G = 1000, R_L = 2 kΩ, C_L = 100 pF

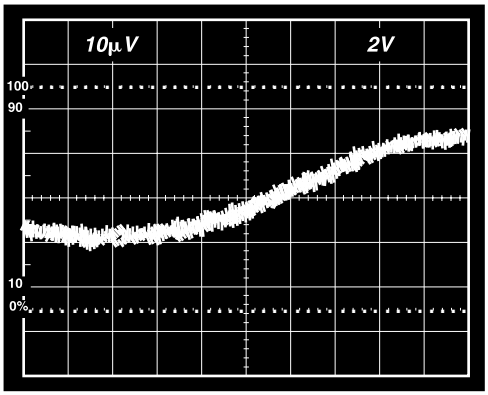


Figure 31a. Gain Nonlinearity, G = 1, R_L = 10 kΩ (10 µV = 1 ppm)

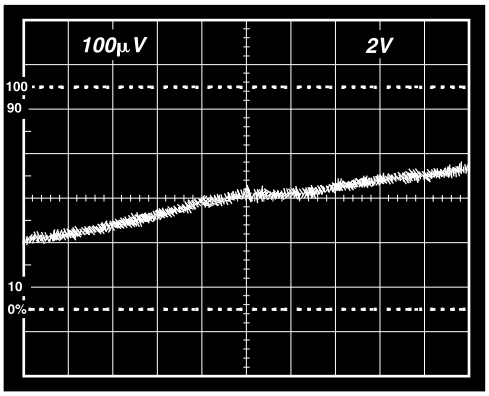


Figure 31b. Gain Nonlinearity, G = 100, R_L = 10 kΩ (100 µV = 10 ppm)

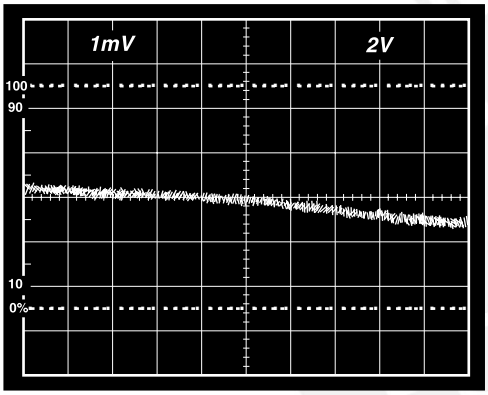


Figure 31c. Gain Nonlinearity, G = 1000, R_L = 10 kΩ (1 mV = 100 ppm)

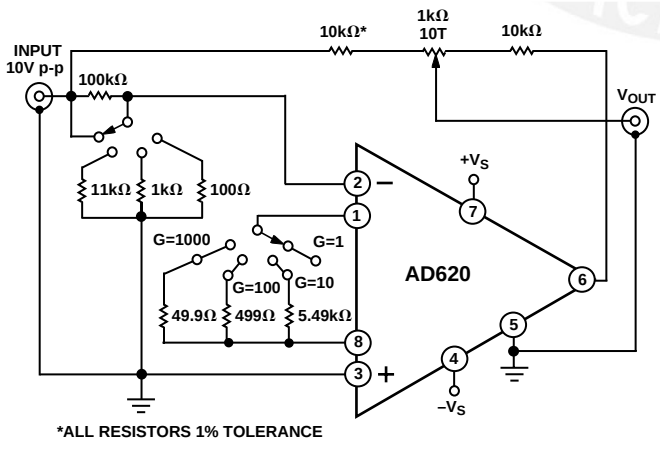


Figure 32. Settling Time Test Circuit

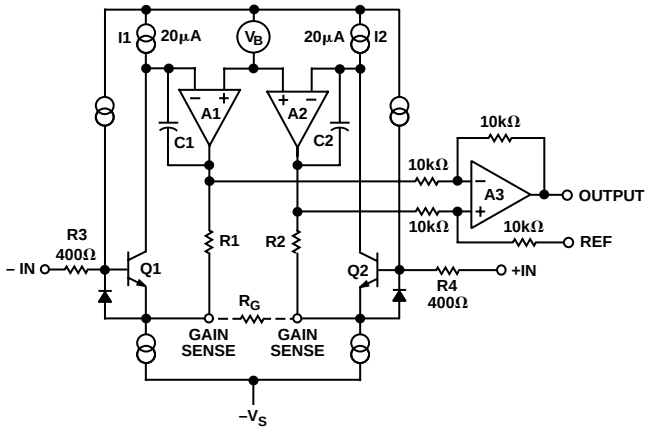


Figure 33. Simplified Schematic of AD620

THEORY OF OPERATION

The AD620 is a monolithic instrumentation amplifier based on a modification of the classic three op amp approach. Absolute value trimming allows the user to program gain *accurately* (to 0.15% at G = 100) with only one resistor. Monolithic construction and laser wafer trimming allow the tight matching and tracking of circuit components, thus ensuring the high level of performance inherent in this circuit.

The input transistors Q1 and Q2 provide a single differential-pair bipolar input for high precision (Figure 33), yet offer 10× lower Input Bias Current thanks to Superβeta processing. Feedback through the Q1-A1-R1 loop and the Q2-A2-R2 loop maintains constant collector current of the input devices Q1, Q2 thereby impressing the input voltage across the external gain setting resistor R_G. This creates a differential gain from the inputs to the A1/A2 outputs given by G = (R1 + R2)/R_G + 1. The unity-gain subtracter A3 removes any common-mode signal, yielding a single-ended output referred to the REF pin potential.

The value of R_G also determines the transconductance of the preamp stage. As R_G is reduced for larger gains, the transconductance increases asymptotically to that of the input transistors. This has three important advantages: (a) Open-loop gain is boosted for increasing programmed gain, thus reducing gain-related errors. (b) The gain-bandwidth product (determined by C1, C2 and the preamp transconductance) increases with programmed gain, thus optimizing frequency response. (c) The input voltage noise is reduced to a value of 9 nV/√Hz, determined mainly by the collector current and base resistance of the input devices.

The internal gain resistors, R1 and R2, are trimmed to an absolute value of 24.7 kΩ, allowing the gain to be programmed accurately with a single external resistor.

The gain equation is then

$$G = \frac{49.4\ k\Omega}{R_G} + 1$$

so that

$$R_G = \frac{49.4\ k\Omega}{G - 1}$$

Make vs. Buy: A Typical Bridge Application Error Budget

The AD620 offers improved performance over "homebrew" three op amp IA designs, along with smaller size, fewer components and 10× lower supply current. In the typical application, shown in Figure 34, a gain of 100 is required to amplify a bridge output of 20 mV full scale over the industrial temperature range of –40°C to +85°C. The error budget table below shows how to calculate the effect various error sources have on circuit accuracy.

Regardless of the system in which it is being used, the AD620 provides greater accuracy, and at low power and price. In simple systems, absolute accuracy and drift errors are by far the most significant contributors to error. In more complex systems with an intelligent processor, an autogain/autozero cycle will remove all absolute accuracy and drift errors leaving only the resolution errors of gain nonlinearity and noise, thus allowing full 14-bit accuracy.

Note that for the homebrew circuit, the OP07 specifications for input voltage offset and noise have been multiplied by $\sqrt{2}$. This is because a three op amp type in-amp has two op amps at its inputs, both contributing to the overall input error.

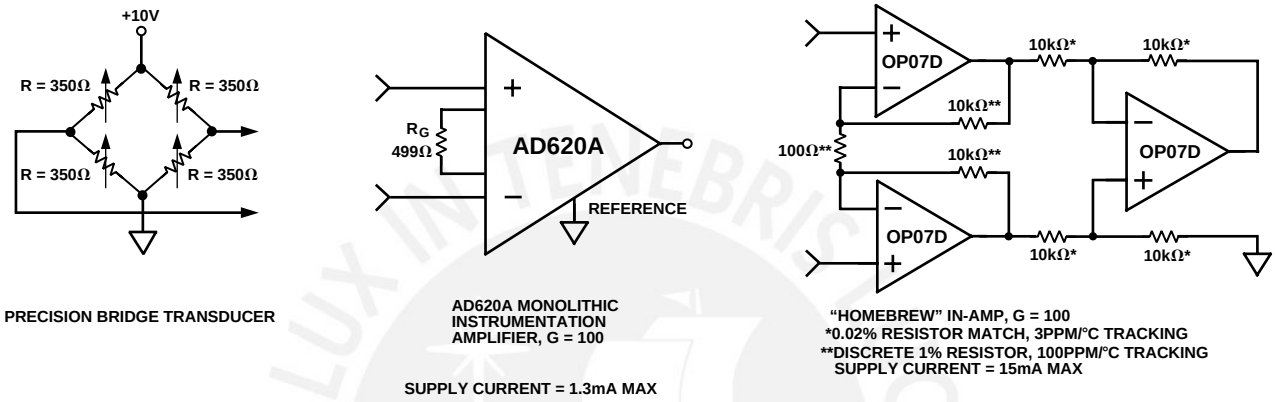


Figure 34. Make vs. Buy

Table I. Make vs. Buy Error Budget

Error Source	AD620 Circuit Calculation	"Homebrew" Circuit Calculation	Error, ppm of Full Scale AD620	Homebrew
ABSOLUTE ACCURACY at T_A = +25°C				
Input Offset Voltage, µV	125 µV/20 mV	(150 µV × $\sqrt{2}$)/20 mV	6,250	10,607
Output Offset Voltage, µV	1000 µV/100/20 mV	((150 µV × 2)/100)/20 mV	500	150
Input Offset Current, nA	2 nA × 350 Ω/20 mV	(6 nA × 350 Ω)/20 mV	18	53
CMR, dB	110 dB→3.16 ppm, × 5 V/20 mV	(0.02% Match × 5 V)/20 mV/100	791	500
		Total Absolute Error	7,558	11,310
DRIFT TO +85°C				
Gain Drift, ppm/°C	(50 ppm + 10 ppm) × 60°C	100 ppm/°C Track × 60°C	3,600	6,000
Input Offset Voltage Drift, µV/°C	1 µV/°C × 60°C/20 mV	(2.5 µV/°C × $\sqrt{2}$ × 60°C)/20 mV	3,000	10,607
Output Offset Voltage Drift, µV/°C	15 µV/°C × 60°C/100/20 mV	(2.5 µV/°C × 2 × 60°C)/100/20 mV	450	150
		Total Drift Error	7,050	16,757
RESOLUTION				
Gain Nonlinearity, ppm of Full Scale	40 ppm	40 ppm	40	40
Typ 0.1 Hz–10 Hz Voltage Noise, µV p-p	0.28 µV p-p/20 mV	(0.38 µV p-p × $\sqrt{2}$)/20 mV	14	27
		Total Resolution Error	54	67
		Grand Total Error	14,662	28,134

G = 100, V_S = ±15 V.

(All errors are min/max and referred to input.)

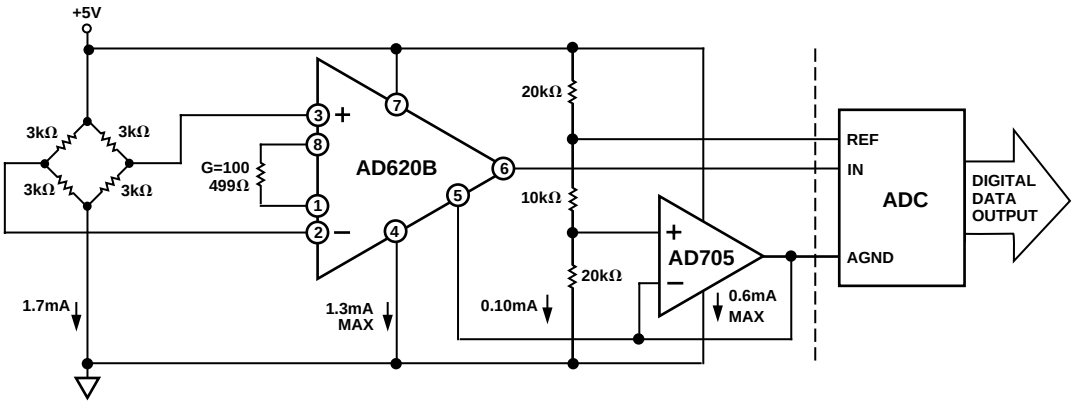


Figure 35. A Pressure Monitor Circuit which Operates on a +5 V Single Supply

Pressure Measurement

Although useful in many bridge applications such as weigh scales, the AD620 is especially suitable for higher resistance pressure sensors powered at lower voltages where small size and low power become more significant.

Figure 35 shows a 3 kΩ pressure transducer bridge powered from +5 V. In such a circuit, the bridge consumes only 1.7 mA. Adding the AD620 and a buffered voltage divider allows the signal to be conditioned for only 3.8 mA of total supply current.

Small size and low cost make the AD620 especially attractive for voltage output pressure transducers. Since it delivers low noise and drift, it will also serve applications such as diagnostic non-invasive blood pressure measurement.

Medical ECG

The low current noise of the AD620 allows its use in ECG monitors (Figure 36) where high source resistances of 1 MΩ or higher are not uncommon. The AD620's low power, low supply voltage requirements, and space-saving 8-lead mini-DIP and SOIC package offerings make it an excellent choice for battery powered data recorders.

Furthermore, the low bias currents and low current noise coupled with the low voltage noise of the AD620 improve the dynamic range for better performance.

The value of capacitor C1 is chosen to maintain stability of the right leg drive loop. Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

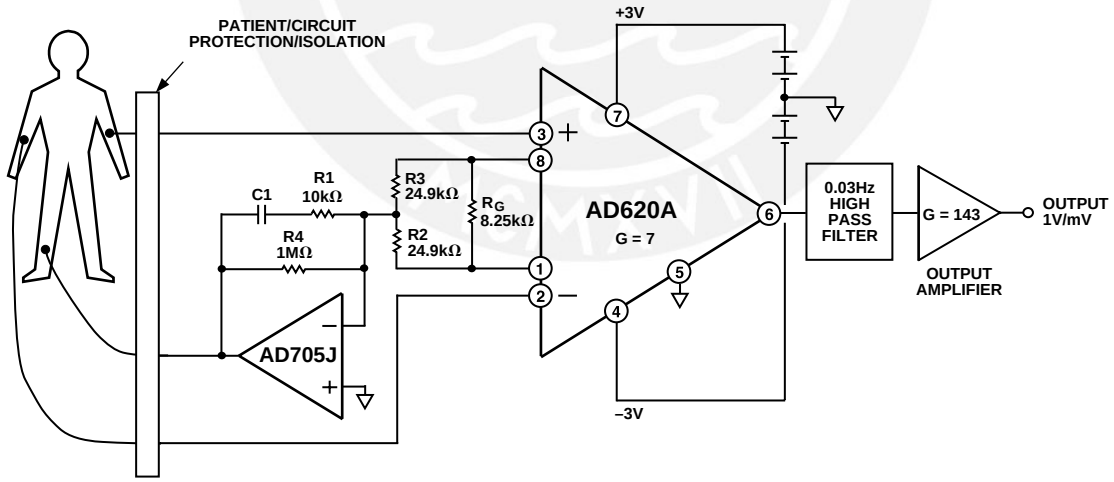


Figure 36. A Medical ECG Monitor Circuit

Precision V-I Converter

The AD620, along with another op amp and two resistors, makes a precision current source (Figure 37). The op amp buffers the reference terminal to maintain good CMR. The output voltage V_X of the AD620 appears across R1, which converts it to a current. This current less only, the input bias current of the op amp, then flows out to the load.

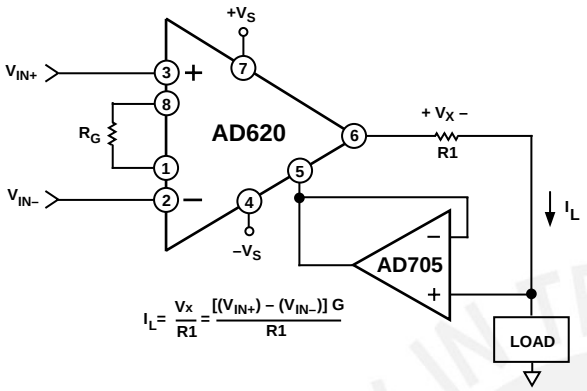


Figure 37. Precision Voltage-to-Current Converter (Operates on 1.8 mA, ±3 V)

GAIN SELECTION

The AD620's gain is resistor programmed by R_G, or more precisely, by whatever impedance appears between Pins 1 and 8. The AD620 is designed to offer accurate gains using 0.1%–1% resistors. Table II shows required values of R_G for various gains. Note that for G = 1, the R_G pins are unconnected ($R_G = \infty$). For any arbitrary gain R_G can be calculated by using the formula:

$$R_G = \frac{49.4\ k\Omega}{G-1}$$

To minimize gain error, avoid high parasitic resistance in series with R_G; to minimize gain drift, R_G should have a low TC—less than 10 ppm/°C—for the best performance.

Table II. Required Values of Gain Resistors

1% Std Table Value of R_G, Ω	Calculated Gain	0.1% Std Table Value of R_G, Ω	Calculated Gain
49.9 k	1.990	49.3 k	2.002
12.4 k	4.984	12.4 k	4.984
5.49 k	9.998	5.49 k	9.998
2.61 k	19.93	2.61 k	19.93
1.00 k	50.40	1.01 k	49.91
499	100.0	499	100.0
249	199.4	249	199.4
100	495.0	98.8	501.0
49.9	991.0	49.3	1,003

INPUT AND OUTPUT OFFSET VOLTAGE

The low errors of the AD620 are attributed to two sources, input and output errors. The output error is divided by G when referred to the input. In practice, the input errors dominate at high gains and the output errors dominate at low gains. The total V_{OS} for a given gain is calculated as:

Total Error RTI = input error + (output error/G)

Total Error RTO = (input error × G) + output error

REFERENCE TERMINAL

The reference terminal potential defines the zero output voltage, and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output, with an allowable range of 2 V within the supply voltages. Parasitic resistance should be kept to a minimum for optimum CMR.

INPUT PROTECTION

The AD620 features 400 Ω of series thin film resistance at its inputs, and will safely withstand input overloads of up to ±15 V or ±60 mA for several hours. This is true for all gains, and power on and off, which is particularly important since the signal source and amplifier may be powered separately. For longer time periods, the current should not exceed 6 mA ($I_{IN} \le V_{IN}/400\ \Omega$). For input overloads beyond the supplies, clamping the inputs to the supplies (using a low leakage diode such as an FD333) will reduce the required resistance, yielding lower noise.

RF INTERFERENCE

All instrumentation amplifiers can rectify out of band signals, and when amplifying small signals, these rectified voltages act as small dc offset errors. The AD620 allows direct access to the input transistor bases and emitters enabling the user to apply some first order filtering to unwanted RF signals (Figure 38), where $RC \approx 1/(2\ \pi f)$ and where f ≥ the bandwidth of the AD620; C ≤ 150 pF. Matching the extraneous capacitance at Pins 1 and 8 and Pins 2 and 3 helps to maintain high CMR.

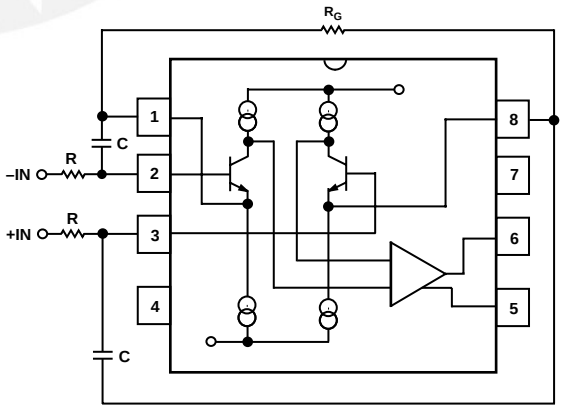


Figure 38. Circuit to Attenuate RF Interference

COMMON-MODE REJECTION

Instrumentation amplifiers like the AD620 offer high CMR, which is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance.

For optimal CMR the reference terminal should be tied to a low impedance point, and differences in capacitance and resistance should be kept to a minimum between the two inputs. In many applications shielded cables are used to minimize noise, and for best CMR over frequency the shield should be properly driven. Figures 39 and 40 show active data guards that are configured to improve ac common-mode rejections by "bootstrapping" the capacitances of input cable shields, thus minimizing the capacitance mismatch between the inputs.

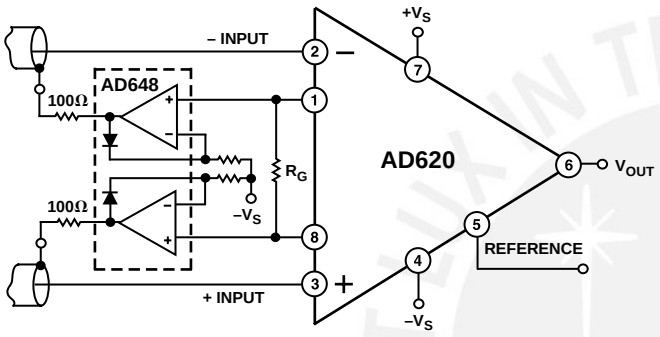


Figure 39. Differential Shield Driver

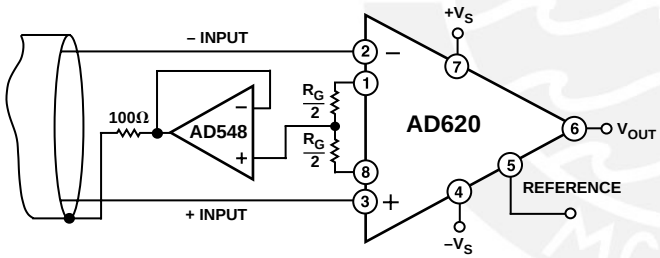


Figure 40. Common-Mode Shield Driver

GROUNDING

Since the AD620 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems by simply tying the REF pin to the appropriate "local ground."

In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have separate analog and digital ground pins (Figure 41). It would be convenient to use a single ground line; however, current through ground wires and PC runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground. These ground returns must be tied together at some point, usually best at the ADC package as shown.

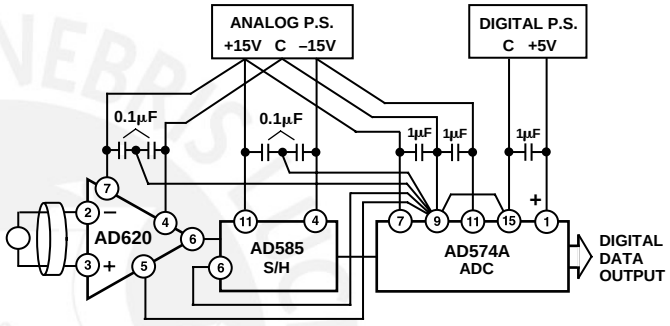


Figure 41. Basic Grounding Practice

GROUND RETURNS FOR INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of an amplifier. There must be a direct return path for these currents; therefore, when amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 42. Refer to the *Instrumentation Amplifier Application Guide* (free from Analog Devices) for more information regarding in amp applications.

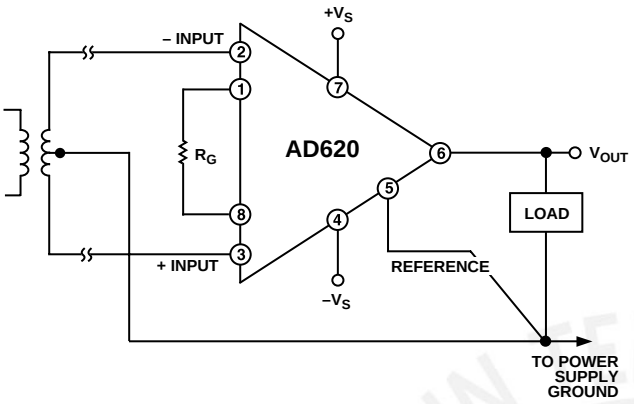


Figure 42a. Ground Returns for Bias Currents with Transformer Coupled Inputs

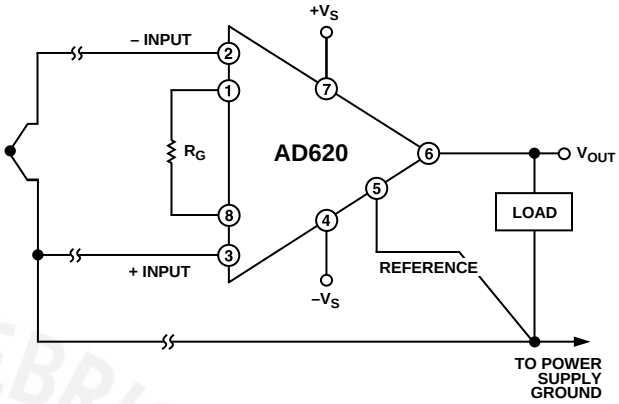


Figure 42b. Ground Returns for Bias Currents with Thermocouple Inputs

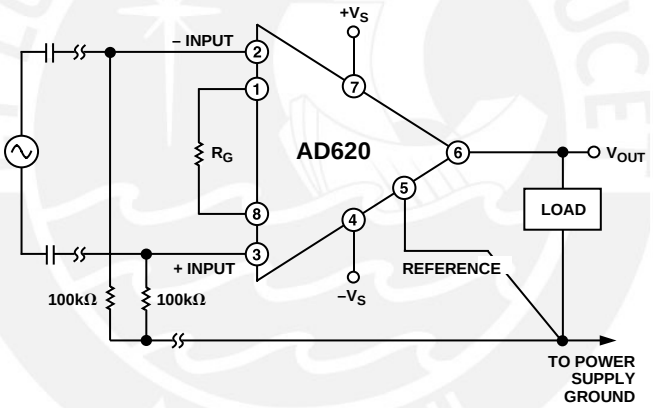
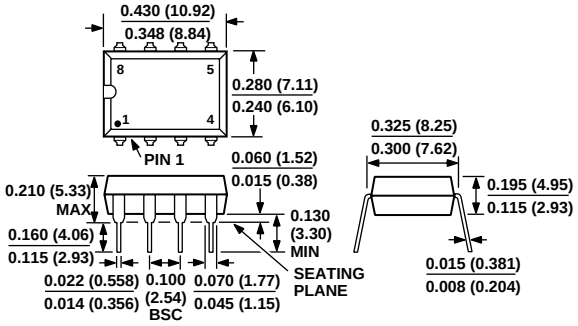


Figure 42c. Ground Returns for Bias Currents with AC Coupled Inputs

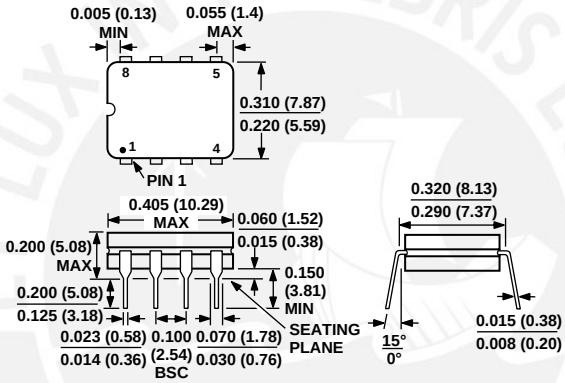
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

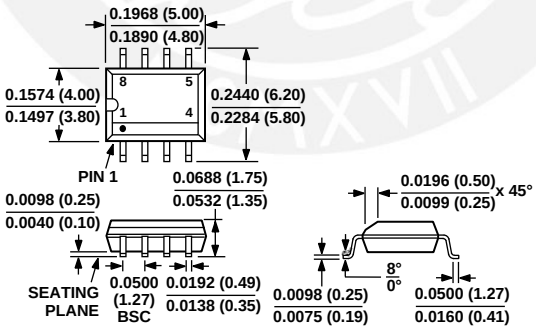
Plastic DIP (N-8) Package



Cerdip (Q-8) Package



SOIC (SO-8) Package



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  - 130 Powerful Instructions – Most Single-clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 16 MIPS Throughput at 16 MHz
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  - Optional Boot Code Section with Independent Lock Bits
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    True Read-While-Write Operation
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    Endurance: 100,000 Write/Erase Cycles
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  - Programming Lock for Software Security
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  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
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  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
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  - 23 Programmable I/O Lines
  - 28-lead PDIP, 32-lead TQFP, and 32-pad MLF
- Operating Voltages
  - 2.7 - 5.5V (ATmega8L)
  - 4.5 - 5.5V (ATmega8)
- Speed Grades
  - 0 - 8 MHz (ATmega8L)
  - 0 - 16 MHz (ATmega8)
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  - Active: 3.6 mA
  - Idle Mode: 1.0 mA
  - Power-down Mode: 0.5 µA

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Summary

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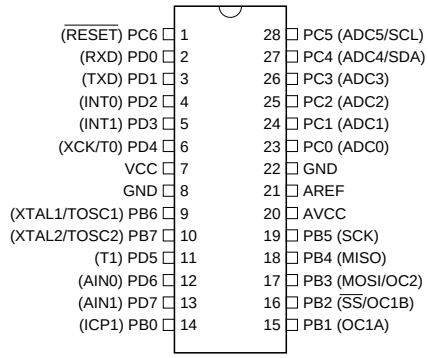
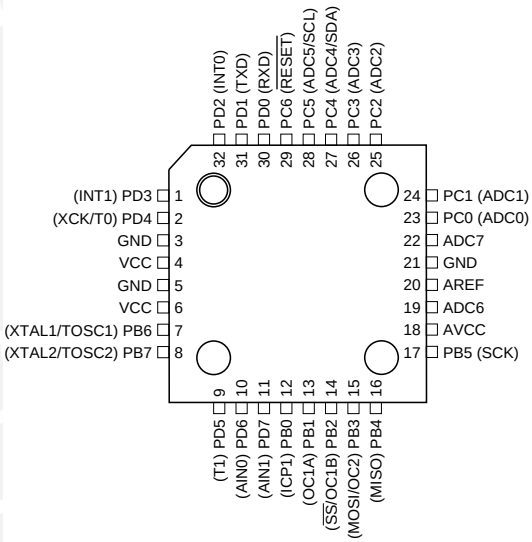
Pin Configurations

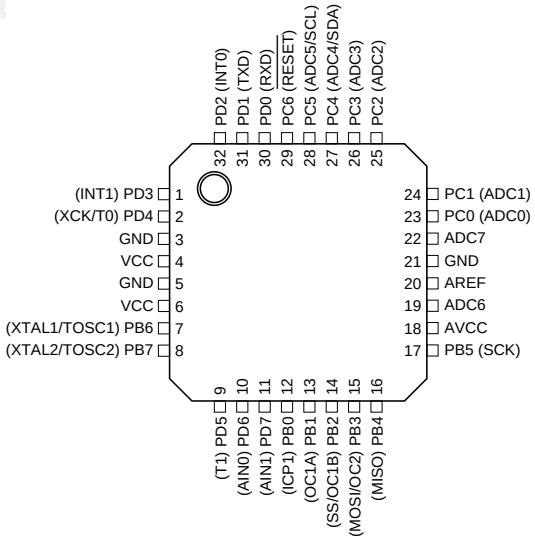
PDIP



TQFP Top View



MLF Top View

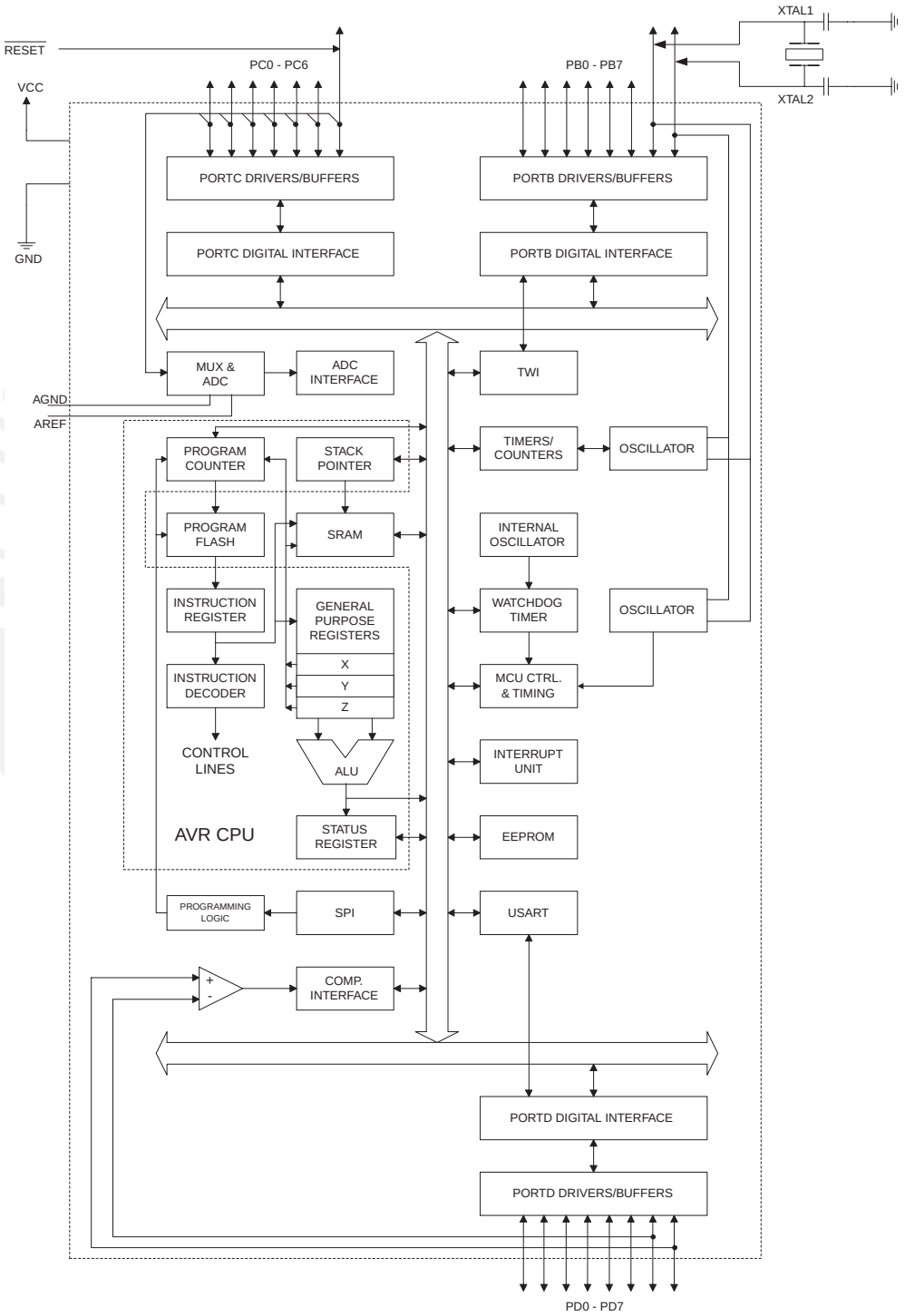


Overview

The ATmega8 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega8 achieves throughputs approaching 1 MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed.

Block Diagram

Figure 1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega8 provides the following features: 8K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes of EEPROM, 1K byte of SRAM, 23 general purpose I/O lines, 32 general purpose working registers, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, a byte oriented Two-wire Serial Interface, a 6-channel ADC (eight channels in TQFP and MLF packages) where four (six) channels have 10-bit accuracy and two channels have 8-bit accuracy, a programmable Watchdog Timer with Internal Oscillator, an SPI serial port, and five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next Interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The Flash Program memory can be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash Section will continue to run while the Application Flash Section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega8 is a powerful microcontroller that provides a highly-flexible and cost-effective solution to many embedded control applications.

The ATmega8 AVR is supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, In-Circuit Emulators, and evaluation kits.

Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

Pin Descriptions

VCC — Digital supply voltage.

GND — Ground.

Port B (PB7..PB0) XTAL1/ XTAL2/TOSC1/TOSC2

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Depending on the clock selection fuse settings, PB6 can be used as input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

Depending on the clock selection fuse settings, PB7 can be used as output from the inverting Oscillator amplifier.

If the Internal Calibrated RC Oscillator is used as chip clock source, PB7..6 is used as TOSC2..1 input for the Asynchronous Timer/Counter2 if the AS2 bit in ASSR is set.

The various special features of Port B are elaborated in “Alternate Functions of Port B” on page 56 and “System Clock and Clock Options” on page 23.

Port C (PC5..PC0)

Port C is an 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

PC6/$\overline{\text{RESET}}$

If the RSTDISBL Fuse is programmed, PC6 is used as an I/O pin. Note that the electrical characteristics of PC6 differ from those of the other pins of Port C.

If the RSTDISBL Fuse is unprogrammed, PC6 is used as a Reset input. A low level on this pin for longer than the minimum pulse length will generate a Reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 36. Shorter pulses are not guaranteed to generate a Reset.

The various special features of Port C are elaborated on page 59.

Port D (PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega8 as listed on page 61.

$\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 36. Shorter pulses are not guaranteed to generate a reset.

AVCC	AVCC is the supply voltage pin for the A/D Converter, Port C (3..0), and ADC (7..6). It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter. Note that Port C (5..4) use digital supply voltage, V_{CC}.
AREF	AREF is the analog reference pin for the A/D Converter.
ADC7..6 (TQFP and MLF Package Only)	In the TQFP and MLF package, ADC7..6 serve as analog inputs to the A/D converter. These pins are powered from the analog supply and serve as 10-bit ADC channels.

Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	9
0x3E (0x5E)	SPH	–	–	–	–	–	SP10	SP9	SP8	11
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	11
0x3C (0x5C)	Reserved									
0x3B (0x5B)	GICR	INT1	INT0	–	–	–	–	IVSEL	IVCE	47, 65
0x3A (0x5A)	GIFR	INTF1	INTF0	–	–	–	–	–	–	66
0x39 (0x59)	TIMSK	OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	–	TOIE0	70, 100, 120
0x38 (0x58)	TIFR	OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	–	TOV0	71, 101, 120
0x37 (0x57)	SPMCR	SPMIE	RWWSB	–	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	210
0x36 (0x56)	TWCR	TWINT	TWEA	TWSTA	TWSTO	TWWC	TWEN	–	TWIE	168
0x35 (0x55)	MCUCR	SE	SM2	SM1	SM0	ISC11	ISC10	ISC01	ISC00	31, 64
0x34 (0x54)	MCUCSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	39
0x33 (0x53)	TCCR0	–	–	–	–	–	CS02	CS01	CS00	70
0x32 (0x52)	TCNT0	Timer/Counter0 (8 Bits)								70
0x31 (0x51)	OSCCAL	Oscillator Calibration Register								29
0x30 (0x50)	SFIOR	–	–	–	–	ACME	PUD	PSR2	PSR10	56, 73, 121, 190
0x2F (0x4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	FOC1A	FOC1B	WGM11	WGM10	95
0x2E (0x4E)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	98
0x2D (0x4D)	TCNT1H	Timer/Counter1 – Counter Register High byte								99
0x2C (0x4C)	TCNT1L	Timer/Counter1 – Counter Register Low byte								99
0x2B (0x4B)	OCR1AH	Timer/Counter1 – Output Compare Register A High byte								99
0x2A (0x4A)	OCR1AL	Timer/Counter1 – Output Compare Register A Low byte								99
0x29 (0x49)	OCR1BH	Timer/Counter1 – Output Compare Register B High byte								99
0x28 (0x48)	OCR1BL	Timer/Counter1 – Output Compare Register B Low byte								99
0x27 (0x47)	ICR1H	Timer/Counter1 – Input Capture Register High byte								100
0x26 (0x46)	ICR1L	Timer/Counter1 – Input Capture Register Low byte								100
0x25 (0x45)	TCCR2	FOC2	WGM20	COM21	COM20	WGM21	CS22	CS21	CS20	115
0x24 (0x44)	TCNT2	Timer/Counter2 (8 Bits)								117
0x23 (0x43)	OCR2	Timer/Counter2 Output Compare Register								117
0x22 (0x42)	ASSR	–	–	–	–	AS2	TCN2UB	OCR2UB	TCR2UB	117
0x21 (0x41)	WDTCR	–	–	–	WDCE	WDE	WDP2	WDP1	WDP0	41
0x20[1] (0x40)[1]	UBRRH	URSEL	–	–	–	UBRR[11:8]				155
	UCSRC	URSEL	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL	153
0x1F (0x3F)	EEARH	–	–	–	–	–	–	–	EEAR8	18
0x1E (0x3E)	EEARL	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	18
0x1D (0x3D)	EEDR	EEPROM Data Register								18
0x1C (0x3C)	EECR	–	–	–	–	EERIE	EEMWE	EEWE	EERE	18
0x1B (0x3B)	Reserved									
0x1A (0x3A)	Reserved									
0x19 (0x39)	Reserved									
0x18 (0x38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	63
0x17 (0x37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	63
0x16 (0x36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	63
0x15 (0x35)	PORTC	–	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	63
0x14 (0x34)	DDRC	–	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	63
0x13 (0x33)	PINC	–	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	63
0x12 (0x32)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	63
0x11 (0x31)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	63
0x10 (0x30)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	63
0x0F (0x2F)	SPDR	SPI Data Register								128
0x0E (0x2E)	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X	128
0x0D (0x2D)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	126
0x0C (0x2C)	UDR	USART I/O Data Register								150
0x0B (0x2B)	UCSRA	RXC	TXC	UDRE	FE	DOR	PE	U2X	MPCM	151
0x0A (0x2A)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8	152
0x09 (0x29)	UBRRL	USART Baud Rate Register Low byte								155
0x08 (0x28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	191
0x07 (0x27)	ADMUX	REFS1	REFS0	ADLAR	–	MUX3	MUX2	MUX1	MUX0	202
0x06 (0x26)	ADCSRA	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	204
0x05 (0x25)	ADCH	ADC Data Register High byte								205
0x04 (0x24)	ADCL	ADC Data Register Low byte								205
0x03 (0x23)	TWDR	Two-wire Serial Interface Data Register								170
0x02 (0x22)	TWAR	TWA6	TWA5	TWA4	TWA3	TWA2	TWA1	TWA0	TWGCE	170

Register Summary (Continued)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x01 (0x21)	TWSR	TWS7	TWS6	TWS5	TWS4	TWS3	–	TWPS1	TWPS0	170
0x00 (0x20)	TWBR	Two-wire Serial Interface Bit Rate Register								168

Notes:
1. Refer to the USART description for details on how to access UBRRH and UCSRC.
2. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
3. Some of the Status Flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O Register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
COM	Rd	One's Complement	Rd ← 0xFF – Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← 0x00 – Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • (0xFF - K)	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd – 1	Z,N,V	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
SER	Rd	Set Register	Rd ← 0xFF	None	1
MUL	Rd, Rr	Multiply Unsigned	R1:R0 ← Rd x Rr	Z,C	2
MULS	Rd, Rr	Multiply Signed	R1:R0 ← Rd x Rr	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC ← Z	None	2
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
ICALL		Indirect Call to (Z)	PC ← Z	None	3
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1 / 2 / 3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC+k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
Mnemonics	**Operands**	**Description**	**Operation**	**Flags**	**#Clocks**

Instruction Set Summary (Continued)

BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	Rd ← (Z), Z ← Z+1	None	3
SPM		Store Program Memory	(Z) ← R1:R0	None	-
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
Mnemonics	**Operands**	**Description**	**Operation**	**Flags**	**#Clocks**

Instruction Set Summary (Continued)

CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
MCU CONTROL INSTRUCTIONS					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1

Ordering Information

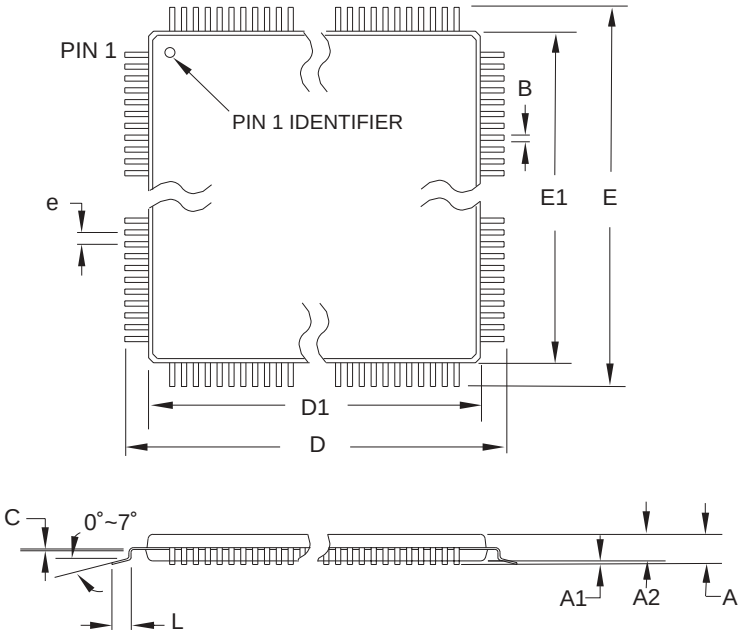
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
8	2.7 - 5.5	ATmega8L-8AC ATmega8L-8PC ATmega8L-8MC	32A 28P3 32M1-A	Commercial (0°C to 70°C)
		ATmega8L-8AI ATmega8L-8PI ATmega8L-8MI	32A 28P3 32M1-A	Industrial (-40°C to 85°C)
16	4.5 - 5.5	ATmega8-16AC ATmega8-16PC ATmega8-16MC	32A 28P3 32M1-A	Commercial (0°C to 70°C)
		ATmega8-16AI ATmega8-16PI ATmega8-16MI	32A 28P3 32M1-A	Industrial (-40°C to 85°C)

Note: This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

Package Type	
32A	32-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
28P3	28-lead, 0.300” Wide, Plastic Dual Inline Package (PDIP)
32M1-A	32-pad, 5 x 5 x 1.0 body, Lead Pitch 0.50 mm Micro Lead Frame Package (MLF)

Packaging Information

32A



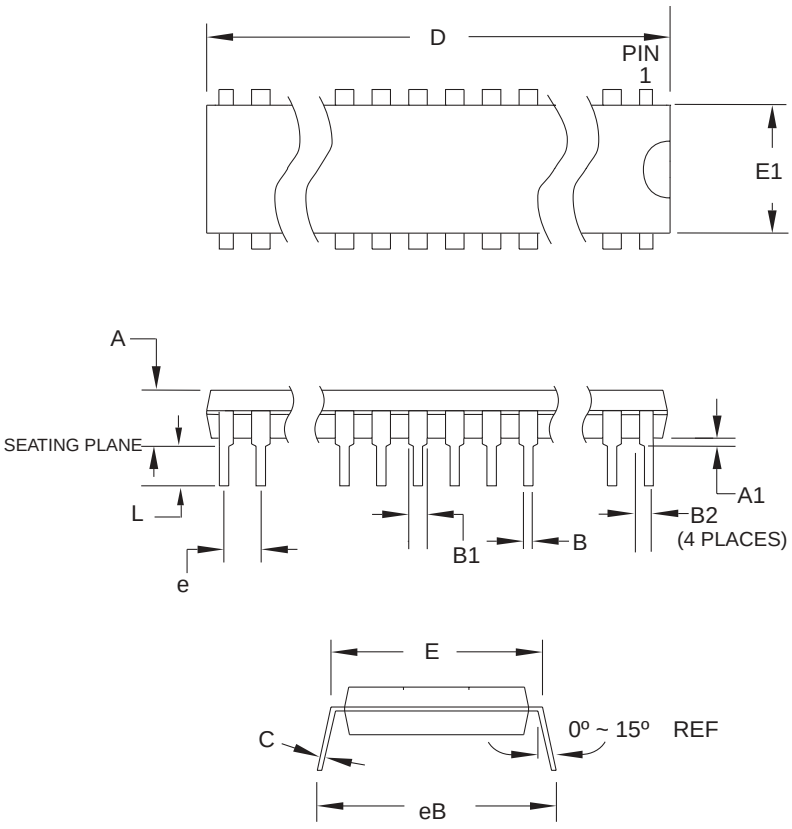
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32A,** 32-lead, 7 x 7 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	32A	B



COMMON DIMENSIONS
(Unit of Measure = mm)

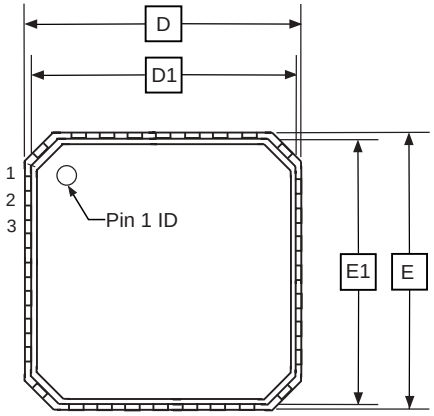
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.5724	
A1	0.508	–	–	
D	34.544	–	34.798	Note 1
E	7.620	–	8.255	
E1	7.112	–	7.493	Note 1
B	0.381	–	0.533	
B1	1.143	–	1.397	
B2	0.762	–	1.143	
L	3.175	–	3.429	
C	0.203	–	0.356	
eB	–	–	10.160	
e	2.540 TYP			

Note: 1. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

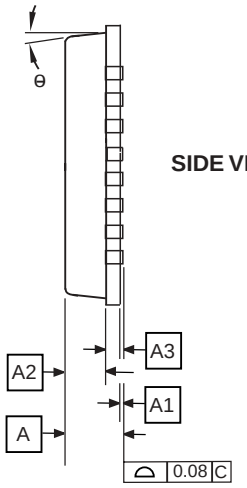
09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**28P3**, 28-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	28P3	B

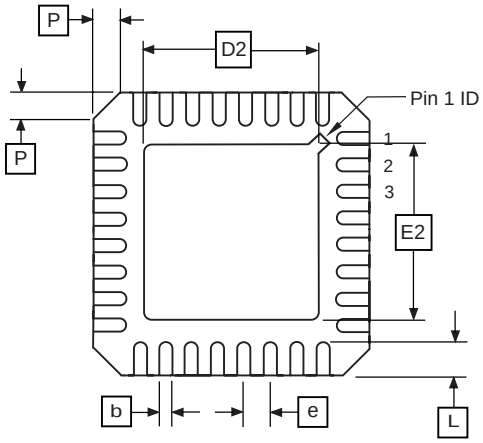
32M1-A



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A2	–	0.65	1.00	
A3		0.20 REF		
b	0.18	0.23	0.30	
D		5.00 BSC		
D1		4.75 BSC		
D2	2.95	3.10	3.25	
E		5.00 BSC		
E1		4.75BSC		
E2	2.95	3.10	3.25	
e		0.50 BSC		
L	0.30	0.40	0.50	
P	–	–	0.60	
θ	–	–	12^{o}	

Notes: 1. JEDEC Standard MO-220, Fig. 2 (Anvil Singulation), VHHD-2.

01/15/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32M1-A**, 32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm Micro Lead Frame Package (MLF)	32M1-A	C

Erratas

The revision letter in this section refers to the revision of the ATmega8 device.

ATmega8 Rev. D, E, F, and G

- **CKOPT Does not Enable Internal Capacitors on XTALn/TOSCn Pins when 32 KHz Oscillator is Used to Clock the Asynchronous Timer/Counter2**

1. CKOPT Does not Enable Internal Capacitors on XTALn/TOSCn Pins when 32 KHz Oscillator is Used to Clock the Asynchronous Timer/Counter2

When the internal RC Oscillator is used as the main clock source, it is possible to run the Timer/Counter2 asynchronously by connecting a 32 KHz Oscillator between XTAL1/TOSC1 and XTAL2/TOSC2. But when the internal RC Oscillator is selected as the main clock source, the CKOPT Fuse does not control the internal capacitors on XTAL1/TOSC1 and XTAL2/TOSC2. As long as there are no capacitors connected to XTAL1/TOSC1 and XTAL2/TOSC2, safe operation of the Oscillator is not guaranteed.

Problem fix/Workaround

Use external capacitors in the range of 20 - 36 pF on XTAL1/TOSC1 and XTAL2/TOSC2. This will be fixed in ATmega8 Rev. G where the CKOPT Fuse will control internal capacitors also when internal RC Oscillator is selected as main clock source. For ATmega8 Rev. G, CKOPT = 0 (programmed) will enable the internal capacitors on XTAL1 and XTAL2. Customers who want compatibility between Rev. G and older revisions, must ensure that CKOPT is unprogrammed (CKOPT = 1).

Datasheet Change Log for ATmega8

This document contains a log on the changes made to the datasheet for ATmega8.

Changes from Rev. 2486K-08/03 to Rev. 2486L-10/03

All page numbers refers to this document.

1. **Updated "Calibrated Internal RC Oscillator" on page 28.**

Changes from Rev. 2486K-08/03 to Rev. 2486L-10/03

All page numbers refers to this document.

1. **Removed "Preliminary" and TBDs from the datasheet.**
2. **Renamed ICP to ICP1 in the datasheet.**
3. **Removed instructions CALL and JMP from the datasheet.**
4. **Updated t_{RST} in Table 15 on page 36, V_{BG} in Table 16 on page 40, Table 100 on page 239 and Table 102 on page 241.**
5. **Replaced text "XTAL1 and XTAL2 should be left unconnected (NC)" after Table 9 in "Calibrated Internal RC Oscillator" on page 28. Added text regarding XTAL1/XTAL2 and CKOPT Fuse in "Timer/Counter Oscillator" on page 30.**
6. **Updated Watchdog Timer code examples in "Timed Sequences for Changing the Configuration of the Watchdog Timer" on page 43.**
7. **Removed bit 4, ADHSM, from "Special Function IO Register – SFIOR" on page 56.**
8. **Added note 2 to Figure 103 on page 212.**
9. **Updated item 4 in the "Serial Programming Algorithm" on page 233.**
10. **Added t_{WD_FUSE} to Table 97 on page 234 and updated Read Calibration Byte, Byte 3, in Table 98 on page 235.**
11. **Updated Absolute Maximum Ratings* and DC Characteristics in "Electrical Characteristics" on page 237.**

Changes from Rev. 2486J-02/03 to Rev. 2486K-08/03

All page numbers refers to this document.

1. **Updated V_{BOT} values in Table 15 on page 36.**
2. **Updated "ADC Characteristics" on page 243.**
3. **Updated "ATmega8 Typical Characteristics" on page 244.**
4. **Updated "Erratas" on page 16.**

Changes from Rev. 2486I-12/02 to Rev. 2486J-02/03

All page numbers refers to this document.

1. Improved the description of “Asynchronous Timer Clock – clkASY” on page 24.
2. Removed reference to the “Multipurpose Oscillator” application note and the “32 kHz Crystal Oscillator” application note, which do not exist.
3. Corrected OCn waveforms in Figure 38 on page 88.
4. Various minor Timer 1 corrections.
5. Various minor TWI corrections.
6. Added note under “Filling the Temporary Buffer (Page Loading)” on page 213 about writing to the EEPROM during an SPM Page load.
7. Removed ADHSM completely.
8. Added section “EEPROM Write during Power-down Sleep Mode” on page 21.
9. Removed XTAL1 and XTAL2 description on page 5 because they were already described as part of “Port B (PB7..PB0) XTAL1/ XTAL2/TOSC1/TOSC2” on page 5.
10. Improved the table under “SPI Timing Characteristics” on page 241 and removed the table under “SPI Serial Programming Characteristics” on page 236.
11. Corrected PC6 in “Alternate Functions of Port C” on page 59.
12. Corrected PB6 and PB7 in “Alternate Functions of Port B” on page 56.
13. Corrected 230.4 Mbps to 230.4 kbps under “Examples of Baud Rate Setting” on page 156.
14. Added information about PWM symmetry for Timer 2 in “Phase Correct PWM Mode” on page 111.
15. Added thick lines around accessible registers in Figure 76 on page 166.
16. Changed “will be ignored” to “must be written to zero” for unused Z-pointer bits under “Performing a Page Write” on page 213.
17. Added note for RSTDISBL Fuse in Table 87 on page 220.
18. Updated drawings in “Packaging Information” on page 13.

Changes from Rev. 2486H-09/02 to Rev. 2486I-12/02

1. Added errata for Rev D, E, and F on page 16.

Changes from Rev. 2486G-09/02 to Rev. 2486H-09/02

1. Changed the Endurance on the Flash to 10,000 Write/Erase Cycles.

Changes from Rev. 2486F-07/02 to Rev. 2486G-09/02

All page numbers refers to this document.

1 Updated Table 103, “ADC Characteristics,” on page 243.

Changes from Rev. 2486E-06/02 to Rev. 2486F-07/02

All page numbers refers to this document.

1 Changes in “Digital Input Enable and Sleep Modes” on page 53.

2 Addition of OCS2 in “MOSI/OC2 – Port B, Bit 3” on page 57.

3 The following tables has been updated:

Table 51, “CPOL and CPHA Functionality,” on page 129, Table 59, “UCPOL Bit Settings,” on page 155, Table 72, “Analog Comparator Multiplexed Input(1),” on page 192, Table 73, “ADC Conversion Time,” on page 197, Table 75, “Input Channel Selections,” on page 203, and Table 84, “Explanation of Different Variables used in Figure 103 and the Mapping to the Z-pointer,” on page 218.

5 Changes in “Reading the Calibration Byte” on page 230.

6 Corrected Errors in Cross References.

Changes from Rev. 2486D-03/02 to Rev. 2486E-06/02

All page numbers refers to this document.

1 Updated Some Preliminary Test Limits and Characterization Data

The following tables have been updated:

Table 15, “Reset Characteristics,” on page 36, Table 16, “Internal Voltage Reference Characteristics,” on page 40, DC Characteristics on page 237, Table , “ADC Characteristics,” on page 243.

2 Changes in External Clock Frequency

Added the description at the end of “External Clock” on page 30.

Added period changing data in Table 99, “External Clock Drive,” on page 239.

3 Updated TWI Chapter

More details regarding use of the TWI bit rate prescaler and a Table 65, “TWI Bit Rate Prescaler,” on page 170.

Changes from Rev. 2486C-03/02 to Rev. 2486D-03/02

All page numbers refers to this document.

1 Updated Typical Start-up Times.

The following tables has been updated:

Table 5, “Start-up Times for the Crystal Oscillator Clock Selection,” on page 26, Table 6, “Start-up Times for the Low-frequency Crystal Oscillator Clock Selection,” on page 26, Table 8, “Start-up Times for the External RC Oscillator Clock Selection,” on page 27, and Table 12, “Start-up Times for the External Clock Selection,” on page 30.

2 Added “ATmega8 Typical Characteristics” on page 244.

Changes from Rev. 2486B-12/01 to Rev. 2486C-03/02

All page numbers refers to this document.

1 **Updated TWI Chapter.**

More details regarding use of the TWI Power-down operation and using the TWI as Master with low TWBRR values are added into the datasheet.

Added the note at the end of the “Bit Rate Generator Unit” on page 167.

Added the description at the end of “Address Match Unit” on page 167.

2 **Updated Description of OSCCAL Calibration Byte.**

In the datasheet, it was not explained how to take advantage of the calibration bytes for 2, 4, and 8 MHz Oscillator selections. This is now added in the following sections:

Improved description of “Oscillator Calibration Register – OSCCAL” on page 29 and “Calibration Byte” on page 221.

3 **Added Some Preliminary Test Limits and Characterization Data.**

Removed some of the TBD’s in the following tables and pages:

Table 3 on page 24, Table 15 on page 36, Table 16 on page 40, Table 17 on page 42, “TA = -40×C to 85×C, VCC = 2.7V to 5.5V (unless otherwise noted)” on page 237, Table 99 on page 239, and Table 102 on page 241.

4 **Updated Programming Figures.**

Figure 104 on page 222 and Figure 112 on page 232 are updated to also reflect that AVCC must be connected during Programming mode.

5 **Added a Description on how to Enter Parallel Programming Mode if RESET Pin is Disabled or if External Oscillators are Selected.**

Added a note in section “Enter Programming Mode” on page 224.

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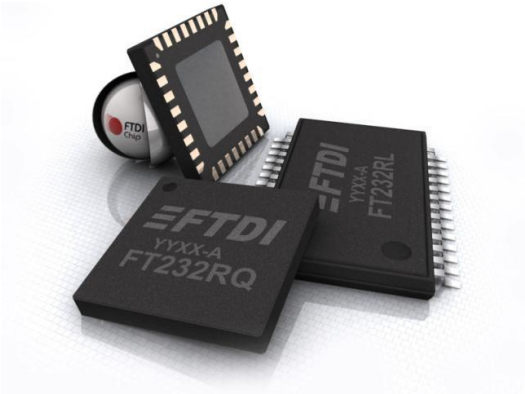
Literature Requests
www.atmel.com/literature

2486MS–AVR–12/03

Future Technology Devices International Ltd.

FT232R USB UART IC



The FT232R is a USB to serial UART interface with the following advanced features:

- Single chip USB to asynchronous serial data transfer interface.
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- Fully integrated 1024 bit EEPROM storing device descriptors and CBUS I/O configuration.
- Fully integrated USB termination resistors.
- Fully integrated clock generation with no external crystal required plus optional clock output selection enabling a glue-less interface to external MCU or FPGA.
- Data transfer rates from 300 baud to 3 Mbaud (RS422, RS485, RS232) at TTL levels.
- 128 byte receive buffer and 256 byte transmit buffer utilising buffer smoothing technology to allow for high data throughput.
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.
- Unique USB FTDIChip-ID™ feature.
- Configurable CBUS I/O pins.
- Transmit and receive LED drive signals.
- UART interface support for 7 or 8 data bits, 1 or 2 stop bits and odd / even / mark / space / no parity
- FIFO receive and transmit buffers for high data throughput.
- Synchronous and asynchronous bit bang interface options with RD# and WR# strobes.
- Device supplied pre-programmed with unique USB serial number.
- Supports bus powered, self powered and high-power bus powered USB configurations.
- Integrated +3.3V level converter for USB I/O.
- Integrated level converter on UART and CBUS for interfacing to between +1.8V and +5V logic.
- True 5V/3.3V/2.8V/1.8V CMOS drive output and TTL input.
- Configurable I/O pin output drive strength.
- Integrated power-on-reset circuit.
- Fully integrated AVCC supply filtering - no external filtering required.
- UART signal inversion option.
- +3.3V (using external oscillator) to +5.25V (internal oscillator) Single Supply Operation.
- Low operating and USB suspend current.
- Low USB bandwidth consumption.
- UHCI/OHCI/EHCI host controller compatible.
- USB 2.0 Full Speed compatible.
- -40°C to 85°C extended operating temperature range.
- Available in compact Pb-free 28 Pin SSOP and QFN-32 packages (both RoHS compliant).

1 Typical Applications

- USB to RS232/RS422/RS485 Converters
- Upgrading Legacy Peripherals to USB
- Cellular and Cordless Phone USB data transfer cables and interfaces
- Interfacing MCU/PLD/FPGA based designs to USB
- USB Audio and Low Bandwidth Video data transfer
- PDA to USB data transfer
- USB Smart Card Readers
- USB Instrumentation
- USB Industrial Control
- USB MP3 Player Interface
- USB FLASH Card Reader and Writers
- Set Top Box PC - USB interface
- USB Digital Camera Interface
- USB Hardware Modems
- USB Wireless Modems
- USB Bar Code Readers
- USB Software and Hardware Encryption Dongles

1.1 Driver Support

Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 98, 98SE, ME, 2000, Server 2003, XP and Server 2008
- Windows 7 32,64-bit
- Windows XP and XP 64-bit
- Windows Vista and Vista 64-bit
- Windows XP Embedded
- Windows CE 4.2, 5.0 and 6.0
- Mac OS 8/9, OS-X
- Linux 2.4 and greater

Royalty free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 98, 98SE, ME, 2000, Server 2003, XP and Server 2008
- Windows 7 32,64-bit
- Windows XP and XP 64-bit
- Windows Vista and Vista 64-bit
- Windows XP Embedded
- Windows CE 4.2, 5.0 and 6.0
- Linux 2.4 and greater

The drivers listed above are all available to download for free from FTDI website (www.ftdichip.com). Various 3rd party drivers are also available for other operating systems - see FTDI website (www.ftdichip.com) for details.

For driver installation, please refer to http://www.ftdichip.com/Documents/InstallGuides.htm

1.2 Part Numbers

Part Number	Package
FT232RQ-xxxx	32 Pin QFN
FT232RL-xxxx	28 Pin SSOP

Note: Packing codes for xxxx is:

- Reel: Taped and Reel, (SSOP is 2,000pcs per reel, QFN is 6,000pcs per reel).
- Tube: Tube packing, 47pcs per tube (SSOP only)
- Tray: Tray packing, 490pcs per tray (QFN only)

For example: FT232RQ-Reel is 6,000pcs taped and reel packing

1.3 USB Compliant

The FT232R is fully compliant with the USB 2.0 specification and has been given the USB-IF Test-ID (TID) 40680004 (Rev B) and 40770018 (Rev C).

2 FT232R Block Diagram

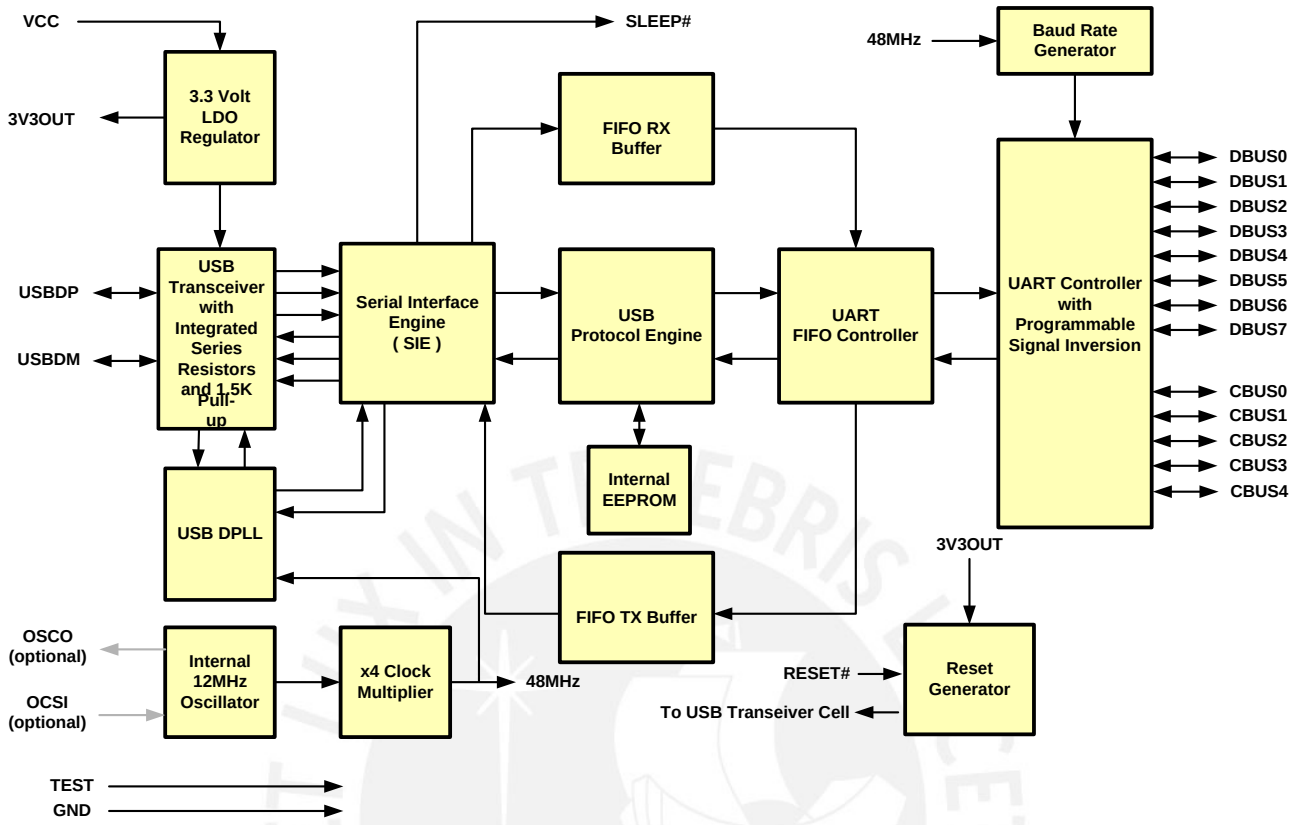


Figure 2.1 FT232R Block Diagram

For a description of each function please refer to Section 4.

Table of Contents

3 Device Pin Out and Signal Description

3.1 28-LD SSOP Package

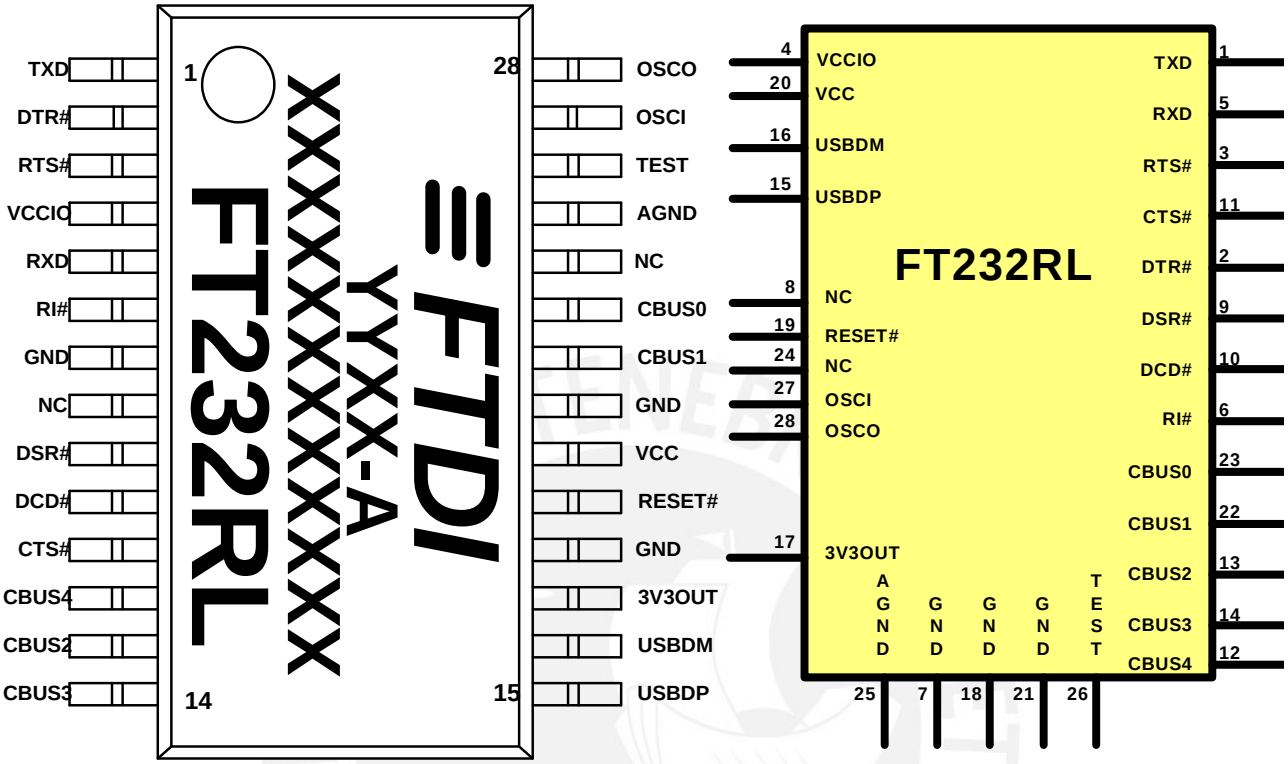


Figure 3.1 SSOP Package Pin Out and Schematic Symbol

3.2 SSOP Package Pin Out Description

Note: The convention used throughout this document for active low signals is the signal name followed by a #

Pin No.	Name	Type	Description
15	USBDP	I/O	USB Data Signal Plus, incorporating internal series resistor and 1.5kΩ pull up resistor to 3.3V.
16	USBDM	I/O	USB Data Signal Minus, incorporating internal series resistor.

Table 3.1 USB Interface Group

Pin No.	Name	Type	Description
4	VCCIO	PWR	+1.8V to +5.25V supply to the UART Interface and CBUS group pins (1...3, 5, 6, 9...14, 22, 23). In USB bus powered designs connect this pin to 3V3OUT pin to drive out at +3.3V levels, or connect to VCC to drive out at 5V CMOS level. This pin can also be supplied with an external +1.8V to +2.8V supply in order to drive outputs at lower levels. It should be noted that in this case this supply should originate from the same source as the supply to VCC. This means that in bus powered designs a regulator which is supplied by the +5V on the USB bus should be used.
7, 18, 21	GND	PWR	Device ground supply pins

Pin No.	Name	Type	Description
17	3V3OUT	Output	+3.3V output from integrated LDO regulator. This pin should be decoupled to ground using a 100nF capacitor. The main use of this pin is to provide the internal +3.3V supply to the USB transceiver cell and the internal 1.5kΩ pull up resistor on USBDP. Up to 50mA can be drawn from this pin to power external logic if required. This pin can also be used to supply the VCCIO pin.
20	VCC	PWR	+3.3V to +5.25V supply to the device core. (see Note 1)
25	AGND	PWR	Device analogue ground supply for internal clock multiplier

Table 3.2 Power and Ground Group

Pin No.	Name	Type	Description
8, 24	NC	NC	No internal connection
19	RESET#	Input	Active low reset pin. This can be used by an external device to reset the FT232R. If not required can be left unconnected, or pulled up to VCC.
26	TEST	Input	Puts the device into IC test mode. Must be tied to GND for normal operation, otherwise the device will appear to fail.
27	OSCI	Input	Input 12MHz Oscillator Cell. Optional – Can be left unconnected for normal operation. (see Note 2)
28	OSCO	Output	Output from 12MHZ Oscillator Cell. Optional – Can be left unconnected for normal operation if internal Oscillator is used. (see Note 2)

Table 3.3 Miscellaneous Signal Group

Pin No.	Name	Type	Description
1	TXD	Output	Transmit Asynchronous Data Output.
2	DTR#	Output	Data Terminal Ready Control Output / Handshake Signal.
3	RTS#	Output	Request to Send Control Output / Handshake Signal.
5	RXD	Input	Receiving Asynchronous Data Input.
6	RI#	Input	Ring Indicator Control Input. When remote wake up is enabled in the internal EEPROM taking RI# low (20ms active low pulse) can be used to resume the PC USB host controller from suspend.
9	DSR#	Input	Data Set Ready Control Input / Handshake Signal.
10	DCD#	Input	Data Carrier Detect Control Input.
11	CTS#	Input	Clear To Send Control Input / Handshake Signal.
12	CBUS4	I/O	Configurable CBUS output only Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is SLEEP#. See CBUS Signal Options, Table 3.9.
13	CBUS2	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is TXDEN. See CBUS Signal Options, Table 3.9.

Pin No.	Name	Type	Description
14	CBUS3	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is PWREN#. See CBUS Signal Options, Table 3.9. PWREN# should be used with a 10kΩ resistor pull up.
22	CBUS1	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is RXLED#. See CBUS Signal Options, Table 3.9.
23	CBUS0	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is TXLED#. See CBUS Signal Options, Table 3.9.

Table 3.4 UART Interface and CUSB Group (see note 3)

Notes:

1. The minimum operating voltage VCC must be +4.0V (could use VBUS=+5V) when using the internal clock generator. Operation at +3.3V is possible using an external crystal oscillator.
2. For details on how to use an external crystal, ceramic resonator, or oscillator with the FT232R, please refer Section 7.6
3. When used in Input Mode, the input pins are pulled to VCCIO via internal 200kΩ resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the internal EEPROM.

3.3 QFN-32 Package

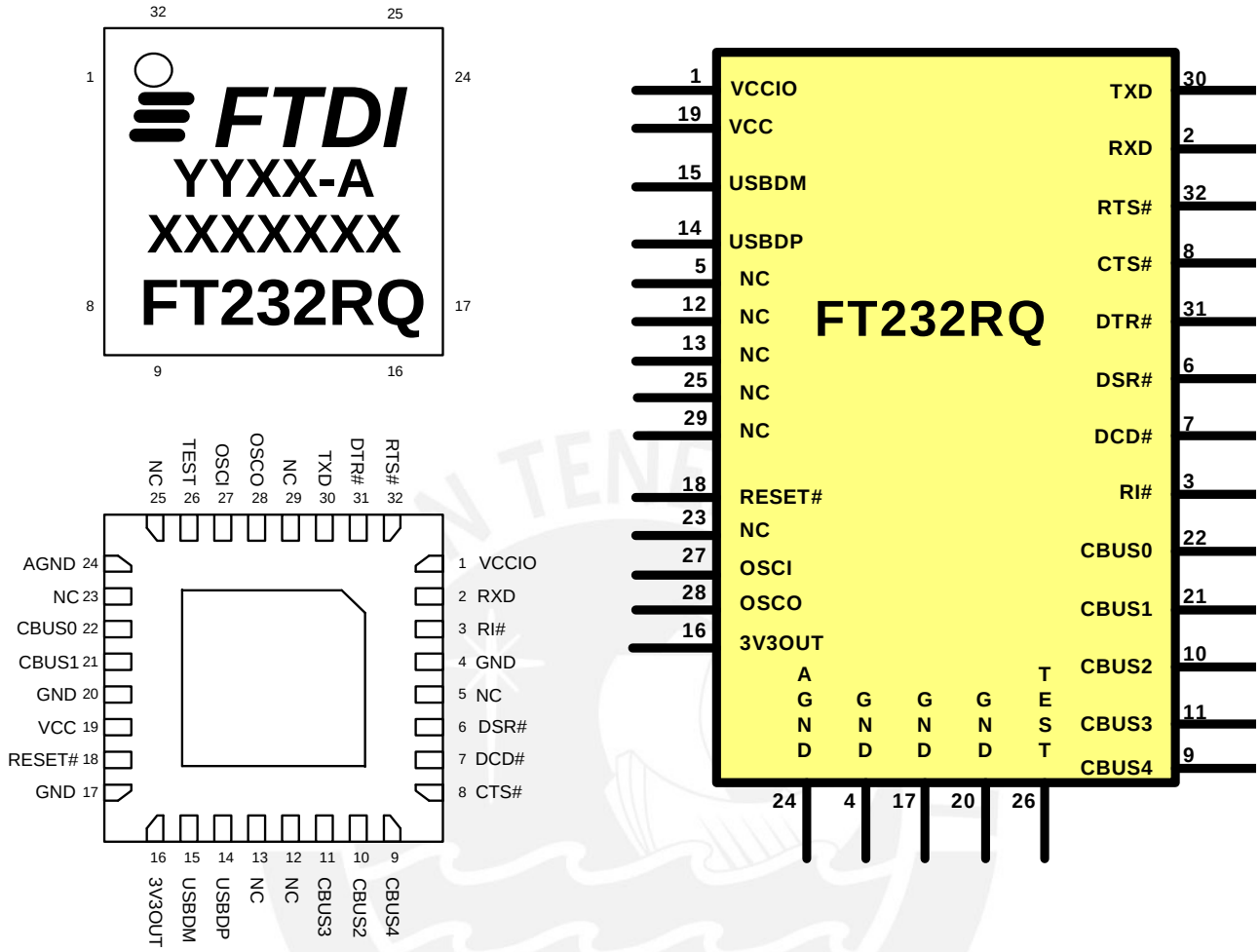


Figure 3.2 QFN-32 Package Pin Out and schematic symbol

3.4 QFN-32 Package Signal Description

Pin No.	Name	Type	Description
14	USBDP	I/O	USB Data Signal Plus, incorporating internal series resistor and 1.5kΩ pull up resistor to +3.3V.
15	USBDM	I/O	USB Data Signal Minus, incorporating internal series resistor.

Table 3.5 USB Interface Group

Pin No.	Name	Type	Description
1	VCCIO	PWR	+1.8V to +5.25V supply for the UART Interface and CBUS group pins (2, 3, 6,7,8,9,10 11, 21, 22, 30,31,32). In USB bus powered designs connect this pin to 3V3OUT to drive out at +3.3V levels, or connect to VCC to drive out at +5V CMOS level. This pin can also be supplied with an external +1.8V to +2.8V supply in order to drive out at lower levels. It should be noted that in this case this supply should originate from the same source as the supply to VCC. This means that in bus powered designs a regulator which is supplied by the +5V on the USB bus should be used.
4, 17, 20	GND	PWR	Device ground supply pins.

Pin No.	Name	Type	Description
16	3V3OUT	Output	+3.3V output from integrated LDO regulator. This pin should be decoupled to ground using a 100nF capacitor. The purpose of this output is to provide the internal +3.3V supply to the USB transceiver cell and the internal 1.5kΩ pull up resistor on USBDP. Up to 50mA can be drawn from this pin to power external logic if required. This pin can also be used to supply the VCCIO pin.
19	VCC	PWR	+3.3V to +5.25V supply to the device core. (See Note 1).
24	AGND	PWR	Device analogue ground supply for internal clock multiplier.

Table 3.6 Power and Ground Group

Pin No.	Name	Type	Description
5, 12, 13, 23, 25, 29	NC	NC	No internal connection. Do not connect.
18	RESET#	Input	Active low reset. Can be used by an external device to reset the FT232R. If not required can be left unconnected, or pulled up to VCC.
26	TEST	Input	Puts the device into IC test mode. Must be tied to GND for normal operation, otherwise the device will appear to fail.
27	OSCI	Input	Input 12MHz Oscillator Cell. Optional – Can be left unconnected for normal operation. (See Note 2).
28	OSCO	Output	Output from 12MHZ Oscillator Cell. Optional – Can be left unconnected for normal operation if internal Oscillator is used. (See Note 2).

Table 3.7 Miscellaneous Signal Group

Pin No.	Name	Type	Description
30	TXD	Output	Transmit Asynchronous Data Output.
31	DTR#	Output	Data Terminal Ready Control Output / Handshake Signal.
32	RTS#	Output	Request to Send Control Output / Handshake Signal.
2	RXD	Input	Receiving Asynchronous Data Input.
3	RI#	Input	Ring Indicator Control Input. When remote wake up is enabled in the internal EEPROM taking RI# low (20ms active low pulse) can be used to resume the PC USB host controller from suspend.
6	DSR#	Input	Data Set Ready Control Input / Handshake Signal.
7	DCD#	Input	Data Carrier Detect Control Input.
8	CTS#	Input	Clear To Send Control Input / Handshake Signal.
9	CBUS4	I/O	Configurable CBUS output only Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is SLEEP#. See CBUS Signal Options, Table 3.9.
10	CBUS2	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is TXDEN. See CBUS Signal Options, Table 3.9.

Pin No.	Name	Type	Description
11	CBUS3	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is PWREN#. See CBUS Signal Options, Table 3.9. PWREN# should be used with a 10kΩ resistor pull up.
21	CBUS1	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is RXLED#. See CBUS Signal Options, Table 3.9.
22	CBUS0	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device internal EEPROM. Factory default configuration is TXLED#. See CBUS Signal Options, Table 3.9.

Table 3.8 UART Interface and CBUS Group (see note 3)

Notes:

1. The minimum operating voltage VCC must be +4.0V (could use VBUS=+5V) when using the internal clock generator. Operation at +3.3V is possible using an external crystal oscillator.
2. For details on how to use an external crystal, ceramic resonator, or oscillator with the FT232R, please refer to Section 7.6.
3. When used in Input Mode, the input pins are pulled to VCCIO via internal 200kΩ resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the internal EEPROM.

3.5 CBUS Signal Options

The following options can be configured on the CBUS I/O pins. CBUS signal options are common to both package versions of the FT232R. These options can be configured in the internal EEPROM using the software utility FT_PPROG or MPROG, which can be downloaded from the FTDI Utilities (www.ftdichip.com). The default configuration is described in Section 8.

CBUS Signal Option	Available On CBUS Pin	Description
TXDEN	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Enable transmit data for RS485
PWREN#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Output is low after the device has been configured by USB, then high during USB suspend mode. This output can be used to control power to external logic P-Channel logic level MOSFET switch. Enable the interface pull-down option when using the PWREN# in this way.*
TXLED#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Transmit data LED drive: Data from USB Host to FT232R. Pulses low when transmitting data via USB. See Section 7.5 for more details.
RXLED#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Receive data LED drive: Data from FT232R to USB Host. Pulses low when receiving data via USB. See Section 7.5 for more details.
TX&RXLED#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	LED drive – pulses low when transmitting or receiving data via USB. See Section 7.5 for more details.
SLEEP#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	Goes low during USB suspend mode. Typically used to power down an external TTL to RS232 level converter IC in USB to RS232 converter designs.
CLK48	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	48MHz ±0.7% Clock output. **
CLK24	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	24 MHz Clock output.**
CLK12	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	12 MHz Clock output.**
CLK6	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4	6 MHz ±0.7% Clock output. **
CBitBangI/O	CBUS0, CBUS1, CBUS2, CBUS3	CBUS bit bang mode option. Allows up to 4 of the CBUS pins to be used as general purpose I/O. Configured individually for CBUS0, CBUS1, CBUS2 and CBUS3 in the internal EEPROM. A separate application note, AN232R-01, available from FTDI website (www.ftdichip.com) describes in more detail how to use CBUS bit bang mode.
BitBangWRn	CBUS0, CBUS1, CBUS2, CBUS3	Synchronous and asynchronous bit bang mode WR# strobe output.
BitBangRDn	CBUS0, CBUS1, CBUS2, CBUS3	Synchronous and asynchronous bit bang mode RD# strobe output.

Table 3.9 CBUS Configuration Control

* PWREN# must be used with a 10kΩ resistor pull up.

**When in USB suspend mode the outputs clocks are also suspended.

4 Function Description

The FT232R is a USB to serial UART interface device which simplifies USB to serial designs and reduces external component count by fully integrating an external EEPROM, USB termination resistors and an integrated clock circuit which requires no external crystal, into the device. It has been designed to operate efficiently with a USB host controller by using as little as possible of the total USB bandwidth available.

4.1 Key Features

Functional Integration. Fully integrated EEPROM, USB termination resistors, clock generation, AVCC filtering, POR and LDO regulator.

Configurable CBUS I/O Pin Options. The fully integrated EEPROM allows configuration of the Control Bus (CBUS) functionality, signal inversion and drive strength selection. There are 5 configurable CBUS I/O pins. These configurable options are

1. **TXDEN** - transmit enable for RS485 designs.
2. **PWREN#** - Power control for high power, bus powered designs.
3. **TXLED#** - for pulsing an LED upon transmission of data.
4. **RXLED#** - for pulsing an LED upon receiving data.
5. **TX&RXLED#** - which will pulse an LED upon transmission OR reception of data**.**
6. **SLEEP#** - indicates that the device going into USB suspend mode.
7. **CLK48 / CLK24 / CLK12 / CLK6** - 48MHz, 24MHz, 12MHz, and 6MHz clock output signal options.

The CBUS pins can also be individually configured as GPIO pins, similar to asynchronous bit bang mode. It is possible to use this mode while the UART interface is being used, thus providing up to 4 general purpose I/O pins which are available during normal operation. An application note, AN232R-01, available from FTDI website (www.ftdichip.com) describes this feature.

The CBUS lines can be configured with any one of these output options by setting bits in the internal EEPROM. The device is supplied with the most commonly used pin definitions pre-programmed - see Section 8 for details.

Asynchronous Bit Bang Mode with RD# and WR# Strobes. The FT232R supports FTDI's previous chip generation bit-bang mode. In bit-bang mode, the eight UART lines can be switched from the regular interface mode to an 8-bit general purpose I/O port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by an internal timer (equivalent to the baud rate pre-scaler). With the FT232R device this mode has been enhanced by outputting the internal RD# and WR# strobes signals which can be used to allow external logic to be clocked by accesses to the bit-bang I/O bus. This option will be described more fully in a separate application note available from FTDI website (www.ftdichip.com).

Synchronous Bit Bang Mode. The FT232R supports synchronous bit bang mode. This mode differs from asynchronous bit bang mode in that the interface pins are only read when the device is written to. This makes it easier for the controlling program to measure the response to an output stimulus as the data returned is synchronous to the output data. An application note, AN232R-01, available from FTDI website (www.ftdichip.com) describes this feature.

FTDIChip-ID™. The FT232R also includes the new FTDIChip-ID™ security dongle feature. This FTDIChip-ID™ feature allows a unique number to be burnt into each device during manufacture. This number cannot be reprogrammed. This number is only readable over USB and forms a basis of a security dongle which can be used to protect any customer application software being copied. This allows the possibility of using the FT232R in a dongle for software licensing. Further to this, a renewable license scheme can be implemented based on the FTDIChip-ID™ number when encrypted with other information. This encrypted number can be stored in the user area of the FT232R internal EEPROM, and can be decrypted, then compared with the protected FTDIChip-ID™ to verify that a license is valid. Web based applications can be used to maintain product licensing this way. An application note, AN232R-02, available from FTDI website (www.ftdichip.com) describes this feature.

The FT232R is capable of operating at a voltage supply between +3.3V and +5V with a nominal operational mode current of 15mA and a nominal USB suspend mode current of 70µA. This allows greater margin for peripheral designs to meet the USB suspend mode current limit of 2.5mA. An integrated level converter within the UART interface allows the FT232R to interface to UART logic running at +1.8V, 2.5V, +3.3V or +5V.

4.2 Functional Block Descriptions

The following paragraphs detail each function within the FT232R. Please refer to the block diagram shown in Figure 2.1

Internal EEPROM. The internal EEPROM in the FT232R is used to store USB Vendor ID (VID), Product ID (PID), device serial number, product description string and various other USB configuration descriptors. The internal EEPROM is also used to configure the CBUS pin functions. The FT232R is supplied with the internal EEPROM pre-programmed as described in Section 8. A user area of the internal EEPROM is available to system designers to allow storing additional data. The internal EEPROM descriptors can be programmed in circuit, over USB without any additional voltage requirement. It can be programmed using the FTDI utility software called MPROG, which can be downloaded from FTDI Utilities on the FTDI website (www.ftdichip.com).

+3.3V LDO Regulator. The +3.3V LDO regulator generates the +3.3V reference voltage for driving the USB transceiver cell output buffers. It requires an external decoupling capacitor to be attached to the 3V3OUT regulator output pin. It also provides +3.3V power to the 1.5kΩ internal pull up resistor on USBDP. The main function of the LDO is to power the USB Transceiver and the Reset Generator Cells rather than to power external logic. However, it can be used to supply external circuitry requiring a +3.3V nominal supply with a maximum current of 50mA.

USB Transceiver. The USB Transceiver Cell provides the USB 1.1 / USB 2.0 full-speed physical interface to the USB cable. The output drivers provide +3.3V level slew rate control signalling, whilst a differential input receiver and two single ended input receivers provide USB data in, Single-Ended-0 (SE0) and USB reset detection conditions respectfully. This function also incorporates the internal USB series termination resistors on the USB data lines and a 1.5kΩ pull up resistor on USBDP.

USB DPLL. The USB DPLL cell locks on to the incoming NRZI USB data and generates recovered clock and data signals for the Serial Interface Engine (SIE) block.

Internal 12MHz Oscillator - The Internal 12MHz Oscillator cell generates a 12MHz reference clock. This provides an input to the x4 Clock Multiplier function. The 12MHz Oscillator is also used as the reference clock for the SIE, USB Protocol Engine and UART FIFO controller blocks.

Clock Multiplier / Divider. The Clock Multiplier / Divider takes the 12MHz input from the Internal Oscillator function and generates the 48MHz, 24MHz, 12MHz and 6MHz reference clock signals. The 48Mz clock reference is used by the USB DPLL and the Baud Rate Generator blocks.

Serial Interface Engine (SIE). The Serial Interface Engine (SIE) block performs the parallel to serial and serial to parallel conversion of the USB data. In accordance with the USB 2.0 specification, it performs bit stuffing/un-stuffing and CRC5/CRC16 generation. It also checks the CRC on the USB data stream.

USB Protocol Engine. The USB Protocol Engine manages the data stream from the device USB control endpoint. It handles the low level USB protocol requests generated by the USB host controller and the commands for controlling the functional parameters of the UART in accordance with the USB 2.0 specification chapter 9.

FIFO RX Buffer (128 bytes). Data sent from the USB host controller to the UART via the USB data OUT endpoint is stored in the FIFO RX (receive) buffer. Data is removed from the buffer to the UART transmit register under control of the UART FIFO controller. (Rx relative to the USB interface).

FIFO TX Buffer (256 bytes). Data from the UART receive register is stored in the TX buffer. The USB host controller removes data from the FIFO TX Buffer by sending a USB request for data from the device data IN endpoint. (Tx relative to the USB interface).

UART FIFO Controller. The UART FIFO controller handles the transfer of data between the FIFO RX and TX buffers and the UART transmit and receive registers.

UART Controller with Programmable Signal Inversion and High Drive. Together with the UART FIFO Controller the UART Controller handles the transfer of data between the FIFO RX and FIFO TX buffers and the UART transmit and receive registers. It performs asynchronous 7 or 8 bit parallel to serial and serial to parallel conversion of the data on the RS232 (or RS422 or RS485) interface.

Control signals supported by UART mode include RTS, CTS, DSR, DTR, DCD and RI. The UART Controller also provides a transmitter enable control signal pin option (TXDEN) to assist with interfacing to RS485 transceivers. RTS/CTS, DSR/DTR and XON / XOFF handshaking options are also supported. Handshaking is handled in hardware to ensure fast response times. The UART interface also supports the RS232 BREAK setting and detection conditions.

Additionally, the UART signals can each be individually inverted and have a configurable high drive strength capability. Both these features are configurable in the EEPROM.

Baud Rate Generator - The Baud Rate Generator provides a 16x clock input to the UART Controller from the 48MHz reference clock. It consists of a 14 bit pre-scaler and 3 register bits which provide fine tuning of the baud rate (used to divide by a number plus a fraction or "sub-integer"). This determines the baud rate of the UART, which is programmable from 183 baud to 3 Mbaud.

The FT232R supports all standard baud rates and non-standard baud rates from 183 Baud up to 3 Mbaud. Achievable non-standard baud rates are calculated as follows -

Baud Rate = 3000000 / (n + *x*)

where 'n' can be any integer between 2 and 16,384 (= 2^{14}) and '*x*' can be a sub-integer of the value 0, 0.125, 0.25, 0.375, 0.5, 0.625, 0.75, or 0.875. When n = 1, *x* = 0, i.e. baud rate divisors with values between 1 and 2 are not possible.

This gives achievable baud rates in the range 183.1 baud to 3,000,000 baud. When a non-standard baud rate is required simply pass the required baud rate value to the driver as normal, and the FTDI driver will calculate the required divisor, and set the baud rate. See FTDI application note AN232B-05 on the FTDI website (www.ftdichip.com) for more details.

RESET Generator - The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET# input pin allows an external device to reset the FT232R.

RESET# can be tied to VCC or left unconnected if not being used.

5 Devices Characteristics and Ratings

5.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT232R devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit
Storage Temperature	-65°C to 150°C	Degrees C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours
Ambient Temperature (Power Applied)	-40°C to 85°C	Degrees C
MTTF FT232RL	11162037	hours
MTTF FT232RQ	4464815	hours
VCC Supply Voltage	-0.5 to +6.00	V
DC Input Voltage – USBDP and USBDM	-0.5 to +3.8	V
DC Input Voltage – High Impedance Bidirectionals	-0.5 to + (VCC +0.5)	V
DC Input Voltage – All Other Inputs	-0.5 to + (VCC +0.5)	V
DC Output Current – Outputs	24	mA
DC Output Current – Low Impedance Bidirectionals	24	mA
Power Dissipation (VCC = 5.25V)	500	mW

Table 5.1 Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

5.2 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCC1	VCC Operating Supply Voltage	4.0	---	5.25	V	Using Internal Oscillator
VCC1	VCC Operating Supply Voltage	3.3	---	5.25	V	Using External Crystal
VCC2	VCCIO Operating Supply Voltage	1.8	---	5.25	V	
Icc1	Operating Supply Current	---	15	---	mA	Normal Operation
Icc2	Operating Supply Current	50	70	100	µA	USB Suspend
3V3	3.3v regulator output	3.0	3.3	3.6	V	

Table 5.2 Operating Voltage and Current

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 2mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 2mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.3 UART and CBUS I/O Pin Characteristics (VCCIO = +5.0V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.2	2.7	3.2	V	I source = 1mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.4 UART and CBUS I/O Pin Characteristics (VCCIO = +3.3V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.1	2.6	2.8	V	I source = 1mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.5 UART and CBUS I/O Pin Characteristics (VCCIO = +2.8V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	1.32	1.62	1.8	V	I source = 0.2mA
Vol	Output Voltage Low	0.06	0.1	0.18	V	I sink = 0.5mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.6 UART and CBUS I/O Pin Characteristics (VCCIO = +1.8V, Standard Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 6mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 6mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.7 UART and CBUS I/O Pin Characteristics (VCCIO = +5.0V, High Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.2	2.8	3.2	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.8 UART and CBUS I/O Pin Characteristics (VCCIO = +3.3V, High Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.1	2.6	2.8	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.9 UART and CBUS I/O Pin Characteristics (VCCIO = +2.8V, High Drive Level)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	1.35	1.67	1.8	V	I source = 0.4mA
Vol	Output Voltage Low	0.12	0.18	0.35	V	I sink = 3mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 5.10 UART and CBUS I/O Pin Characteristics (VCCIO = +1.8V, High Drive Level)

** Only input pins have an internal 200KΩ pull-up resistor to VCCIO

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Vin	Input Switching Threshold	1.3	1.6	1.9	V	
VHys	Input Switching Hysteresis	50	55	60	mV	

Table 5.11 RESET# and TEST Pin Characteristics

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
UVoh	I/O Pins Static Output (High)	2.8		3.6	V	RI = 1.5kΩ to 3V3OUT (D+) RI = 15KΩ to GND (D-)
UVol	I/O Pins Static Output (Low)	0		0.3	V	RI = 1.5kΩ to 3V3OUT (D+) RI = 15kΩ to GND (D-)
UVse	Single Ended Rx Threshold	0.8		2.0	V	
UCom	Differential Common Mode	0.8		2.5	V	
UVDif	Differential Input Sensitivity	0.2			V	
UDrvZ	Driver Output Impedance	26	29	44	Ohms	See Note 1

Table 5.12 USB I/O Pin (USBDP, USBDM) Characteristics

5.3 EEPROM Reliability Characteristics

The internal 1024 Bit EEPROM has the following reliability characteristics:

Parameter	Value	Unit
Data Retention	10	Years
Read / Write Cycle	10,000	Cycles

Table 5.13 EEPROM Characteristics

5.4 Internal Clock Characteristics

The internal Clock Oscillator has the following characteristics:

Parameter	Value			Unit
	Minimum	Typical	Maximum	
Frequency of Operation (see Note 1)	11.98	12.00	12.02	MHz
Clock Period	83.19	83.33	83.47	ns
Duty Cycle	45	50	55	%

Table 5.14 Internal Clock Characteristics

Note 1: Equivalent to +/-1667ppm

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.1	2.8	3.2	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	

Table 5.15 OSCI, OSCO Pin Characteristics – see Note 1

Note1: When supplied, the FT232R is configured to use its internal clock oscillator. These characteristics only apply when an external oscillator or crystal is used.

6 USB Power Configurations

The following sections illustrate possible USB power configurations for the FT232R. The illustrations have omitted pin numbers for ease of understanding since the pins differ between the FT232RL and FT232RQ package options.

All USB power configurations illustrated apply to both package options for the FT232R device. Please refer to Section 3 for the package option pin-out and signal descriptions.

6.1 USB Bus Powered Configuration

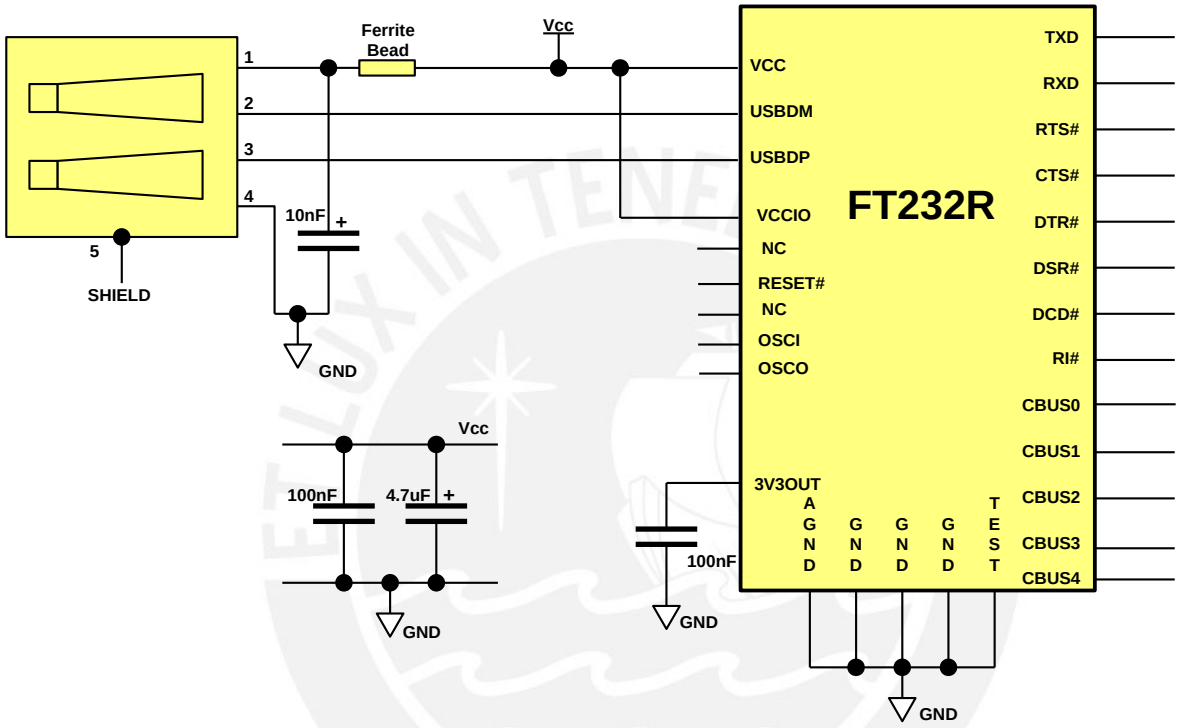


Figure 6.1 Bus Powered Configuration

Figure 6.1 Illustrates the FT232R in a typical USB bus powered design configuration. A USB bus powered device gets its power from the USB bus. Basic rules for USB bus power devices are as follows –

i) On plug-in to USB, the device should draw no more current than 100mA.
ii) In USB Suspend mode the device should draw no more than 2.5mA.
iii) A bus powered high power USB device (one that draws more than 100mA) should use one of the CBUS pins configured as PWREN# and use it to keep the current below 100mA on plug-in and 2.5mA on USB suspend.
iv) A device that consumes more than 100mA cannot be plugged into a USB bus powered hub.
v) No device can draw more than 500mA from the USB bus.

The power descriptors in the internal EEPROM of the FT232R should be programmed to match the current drawn by the device.

A ferrite bead is connected in series with the USB power supply to reduce EMI noise from the FT232R and associated circuitry being radiated down the USB cable to the USB host. The value of the Ferrite Bead depends on the total current drawn by the application. A suitable range of Ferrite Beads is available from Steward (www.steward.com), for example Steward Part # MI0805K400R-10.

Note: If using PWREN# (available using the CBUS) the pin should be pulled to VCCIO using a 10kΩ resistor.

6.2 Self Powered Configuration

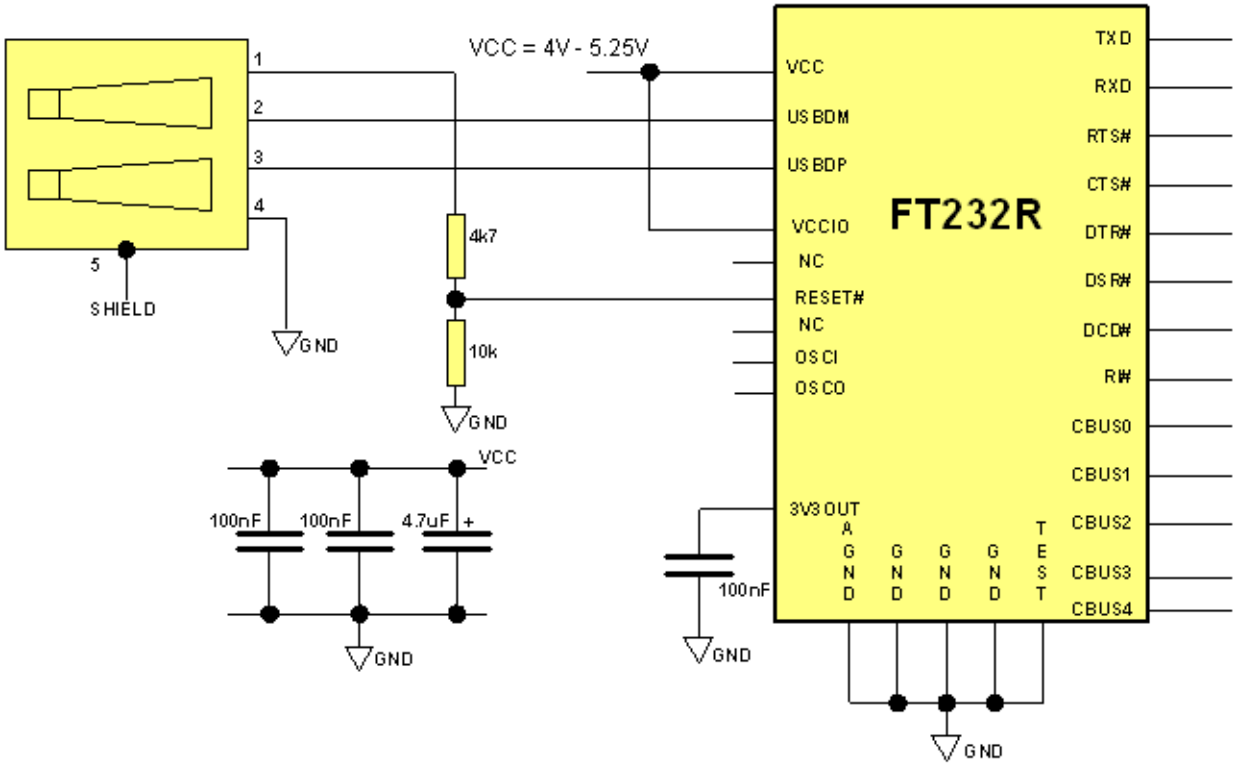


Figure 6.2 Self Powered Configuration

Figure 6.2 illustrates the FT232R in a typical USB self powered configuration. A USB self powered device gets its power from its own power supply, VCC, and does not draw current from the USB bus. The basic rules for USB self powered devices are as follows –

i) A self powered device should not force current down the USB bus when the USB host or hub controller is powered down.
ii) A self powered device can use as much current as it needs during normal operation and USB suspend as it has its own power supply.
iii) A self powered device can be used with any USB host, a bus powered USB hub or a self powered USB hub.

The power descriptor in the internal EEPROM of the FT232R should be programmed to a value of zero (self powered).

In order to comply with the first requirement above, the USB bus power (pin 1) is used to control the RESET# pin of the FT232R device. When the USB host or hub is powered up an internal 1.5kΩ resistor on USBDP is pulled up to +3.3V (generated using the 4K7 and 10k resistor network), thus identifying the device as a full speed device to the USB host or hub. When the USB host or hub is powered off, RESET# will be low and the FT232R is held in reset. Since RESET# is low, the internal 1.5kΩ resistor is not pulled up to any power supply (hub or host is powered down), so no current flows down USBDP via the 1.5kΩ pull-up resistor. Failure to do this may cause some USB host or hub controllers to power up erratically.

Figure 6.2 illustrates a self powered design which has a +4V to +5.25V supply.

Note:

1. When the FT232R is in reset, the UART interface I/O pins are tri-stated. Input pins have internal 200kΩ pull-up resistors to VCCIO, so they will gently pull high unless driven by some external logic.
2. When using internal FT232R oscillator the VCC supply voltage range must be +4.0V to 5.25V.
3. When using external oscillator the VCC supply voltage range must be +3.3V to 5.25V
   Any design which interfaces to +3.3 V or +1.8V would be having a +3.3V or +1.8V supply to VCCIO.

6.3 USB Bus Powered with Power Switching Configuration

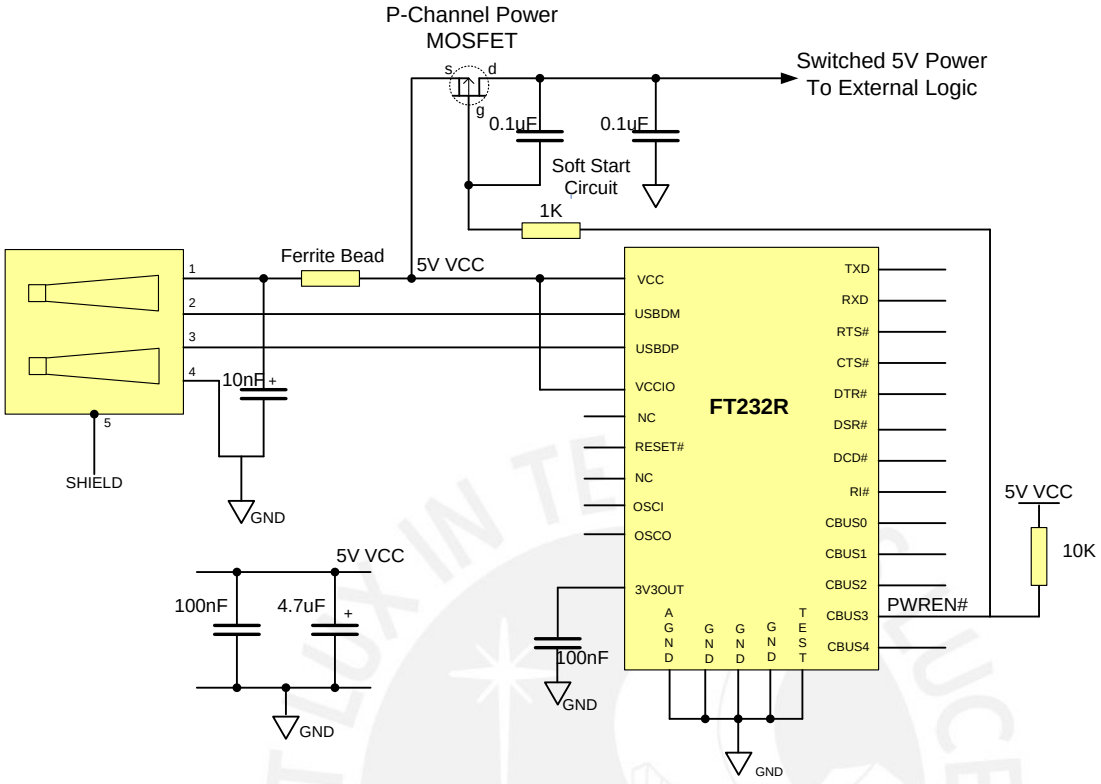


Figure 6.3 Bus Powered with Power Switching Configuration

A requirement of USB bus powered applications, is when in USB suspend mode, the application draws a total current of less than 2.5mA. This requirement includes external logic. Some external logic has the ability to power itself down into a low current state by monitoring the PWREN# signal. For external logic that cannot power itself down in this way, the FT232R provides a simple but effective method of turning off power during the USB suspend mode.

Figure 6.3 shows an example of using a discrete P-Channel MOSFET to control the power to external logic. A suitable device to do this is an International Rectifier (www.irf.com) IRLML6402, or equivalent. It is recommended that a "soft start" circuit consisting of a 1kΩ series resistor and a 0.1µF capacitor is used to limit the current surge when the MOSFET turns on. Without the soft start circuit it is possible that the transient power surge, caused when the MOSFET switches on, will reset the FT232R or the USB host/hub controller. The soft start circuit example shown in Figure 6.3 powers up with a slew rate of approximaely12.5V/ms. Thus supply voltage to external logic transitions from GND to +5V in approximately 400 microseconds.

As an alternative to the MOSFET, a dedicated power switch IC with inbuilt "soft-start" can be used. A suitable power switch IC for such an application is the Micrel (www.micrel.com) MIC2025-2BM or equivalent.

With power switching controlled designs the following should be noted:

i) The external logic to which the power is being switched should have its own reset circuitry to automatically reset the logic when power is re-applied when moving out of suspend mode.

ii) Set the Pull-down on Suspend option in the internal FT232R EEPROM.

iii) One of the CBUS Pins should be configured as PWREN# in the internal FT232R EEPROM, and used to switch the power supply to the external circuitry. This should be pulled high through a 10 kΩ resistor.

iv) For USB high-power bus powered applications (one that consumes greater than 100mA, and up to 500mA of current from the USB bus), the power consumption of the application must be set in the Max Power field in the internal FT232R EEPROM. A high-power bus powered application uses the descriptor in the internal FT232R EEPROM to inform the system of its power requirements.

v) PWREN# gets its VCC from VCCIO. For designs using 3V3 logic, ensure VCCIO is not powered down using the external logic. In this case use the +3V3OUT.

6.4 USB Bus Powered with Selectable External Logic Supply

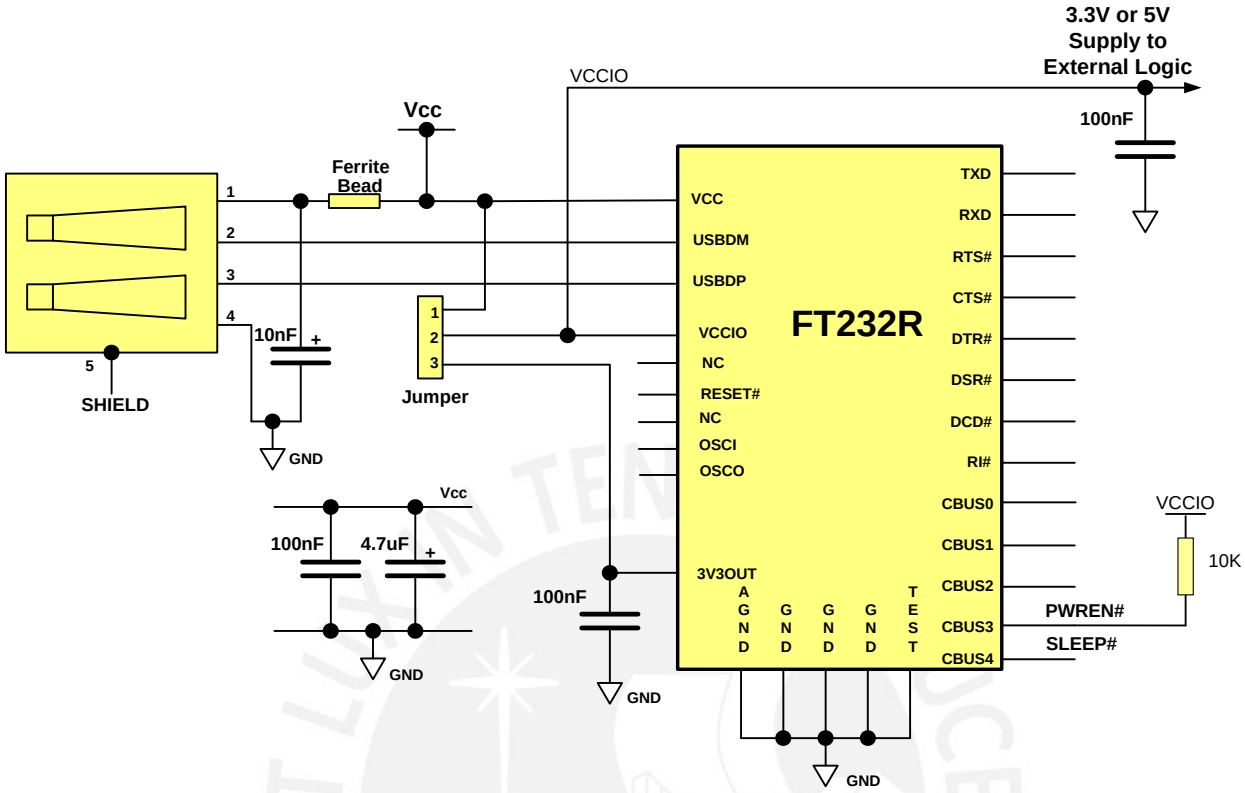


Figure 6.4 USB Bus Powered with +3.3V or +5V External Logic Power Supply

Figure 6.4 illustrates a USB bus power application with selectable external logic supply. The external logic can be selected between +3.3V and +5V using the jumper switch. This jumper is used to allow the FT232R to be interfaced with a +3.3V or +5V logic devices. The VCCIO pin is either supplied with +5V from the USB bus (jumper pins1 and 2 connected), or from the +3.3V output from the FT232R 3V3OUT pin (jumper pins 2 and 3 connected). The supply to VCCIO is also used to supply external logic.

With bus powered applications, the following should be noted:

i) To comply with the 2.5mA current supply limit during USB suspend mode, PWREN# or SLEEP# signals should be used to power down external logic in this mode. If this is not possible, use the configuration shown in Section 6.3.

ii) The maximum current sourced from the USB bus during normal operation should not exceed 100mA, otherwise a bus powered design with power switching (Section 6.3) should be used.

Another possible configuration could use a discrete low dropout (LDO) regulator which is supplied by the 5V on the USB bus to supply between +1.8V and +2.8V to the VCCIO pin and to the external logic. In this case VCC would be supplied with the +5V from the USB bus and the VCCIO would be supplied from the output of the LDO regulator. This results in the FT232R I/O pins driving out at between +1.8V and +2.8V logic levels.

For a USB bus powered application, it is important to consider the following when selecting the regulator:

i) The regulator must be capable of sustaining its output voltage with an input voltage of +4.35V. An Low Drop Out (LDO) regulator should be selected.

ii) The quiescent current of the regulator must be low enough to meet the total current requirement of <= 2.5mA during USB suspend mode.

A suitable series of LDO regulators that meets these requirements is the MicroChip/Telcom (www.microchip.com) TC55 series of devices. These devices can supply up to 250mA current and have a quiescent current of under 1µA.

7 Application Examples

The following sections illustrate possible applications of the FT232R. The illustrations have omitted pin numbers for ease of understanding since the pins differ between the FT232RL and FT232RQ package options.

7.1 USB to RS232 Converter

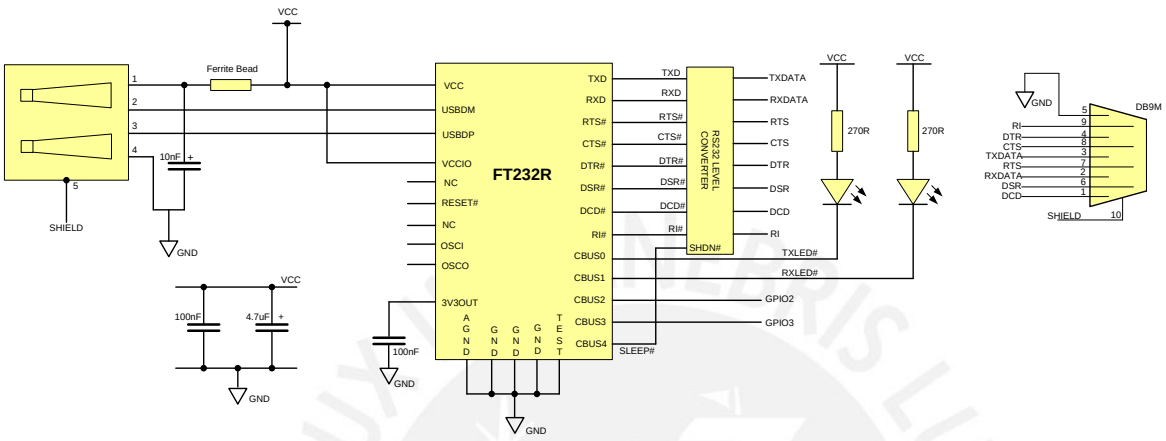


Figure 7.1 Application Example showing USB to RS232 Converter

An example of using the FT232R as a USB to RS232 converter is illustrated in Figure 7.1. In this application, a TTL to RS232 Level Converter IC is used on the serial UART interface of the FT232R to convert the TTL levels of the FT232R to RS232 levels. This level shift can be done using the popular "213" series of TTL to RS232 level converters. These "213" devices typically have 4 transmitters and 5 receivers in a 28-LD SSOP package and feature an in-built voltage converter to convert the +5V (nominal) VCC to the +/- 9 volts required by RS232. A useful feature of these devices is the SHDN# pin which can be used to power down the device to a low quiescent current during USB suspend mode.

A suitable level shifting device is the Sipex SP213EHCA which is capable of RS232 communication at up to 500k baud. If a lower baud rate is acceptable, then several pin compatible alternatives are available such as the Sipex SP213ECA, the Maxim MAX213CAI and the Analogue Devices ADM213E, which are all suitable for communication at up to 115.2k baud. If a higher baud rate is required, the Maxim MAX3245CAI device is capable of RS232 communication rates up to 1Mbaud. Note that the MAX3245 is not pin compatible with the 213 series devices and that the SHDN pin on the MAX device is active high and should be connect to PWREN# pin instead of SLEEP# pin.

In example shown, the CBUS0 and CBUS1 have been configured as TXLED# and RXLED# and are being used to drive two LEDs.

7.2 USB to RS485 Coverter

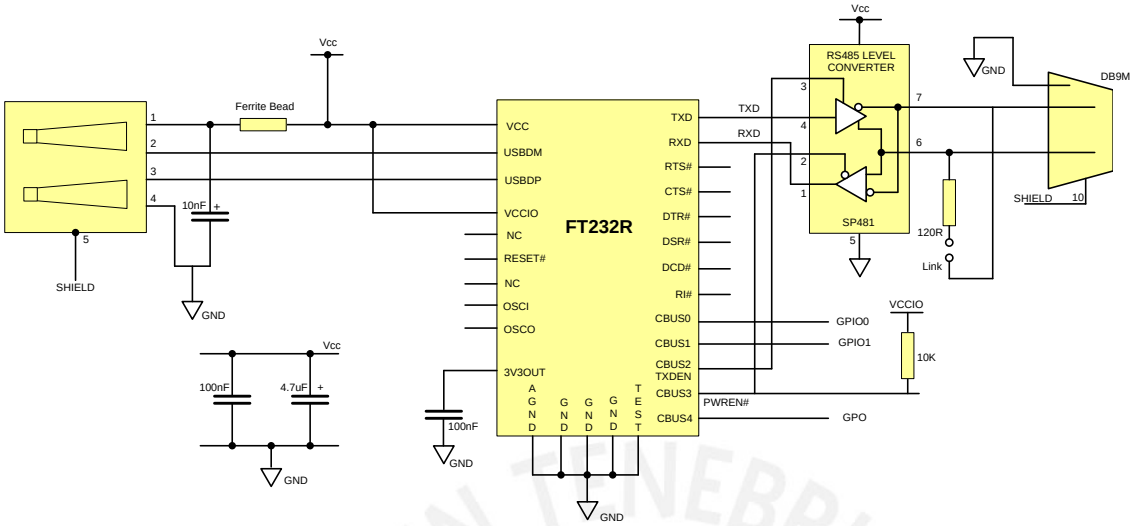


Figure 7.2 Application Example Showing USB to RS485 Converter

An example of using the FT232R as a USB to RS485 converter is shown in Figure 7.2. In this application, a TTL to RS485 level converter IC is used on the serial UART interface of the FT232R to convert the TTL levels of the FT232R to RS485 levels.

This example uses the Sipex SP481 device. Equivalent devices are available from Maxim and Analogue Devices. The SP481 is a RS485 device in a compact 8 pin SOP package. It has separate enables on both the transmitter and receiver. With RS485, the transmitter is only enabled when a character is being transmitted from the UART. The TXDEN signal CBUS pin option on the FT232R is provided for exactly this purpose and so the transmitter enable is wired to CBUS2 which has been configured as TXDEN. Similarly, CBUS3 has been configured as PWREN#. This signal is used to control the SP481's receiver enable. The receiver enable is active low, so it is wired to the PWREN# pin to disable the receiver when in USB suspend mode. CBUS2 = TXDEN and CBUS3 = PWREN# are the default device configurations of the FT232R pins.

RS485 is a multi-drop network; so many devices can communicate with each other over a two wire cable interface. The RS485 cable requires to be terminated at each end of the cable. A link (which provides the 120Ω termination) allows the cable to be terminated if the SP481 is physically positioned at either end of the cable.

In this example the data transmitted by the FT232R is also present on the receive path of the SP481.This is a common feature of RS485 and requires the application software to remove the transmitted data from the received data stream. With the FT232R it is possible to do this entirely in hardware by modifying the example shown in Figure 7.2 by logically OR'ing the FT232R TXDEN and the SP481 receiver output and connecting the output of the OR gate to the RXD of the FT232R.

Note that the TXDEN is activated 1 bit period before the start bit. TXDEN is deactivated at the same time as the stop bit. This is not configurable.

7.3 USB to RS422 Converter

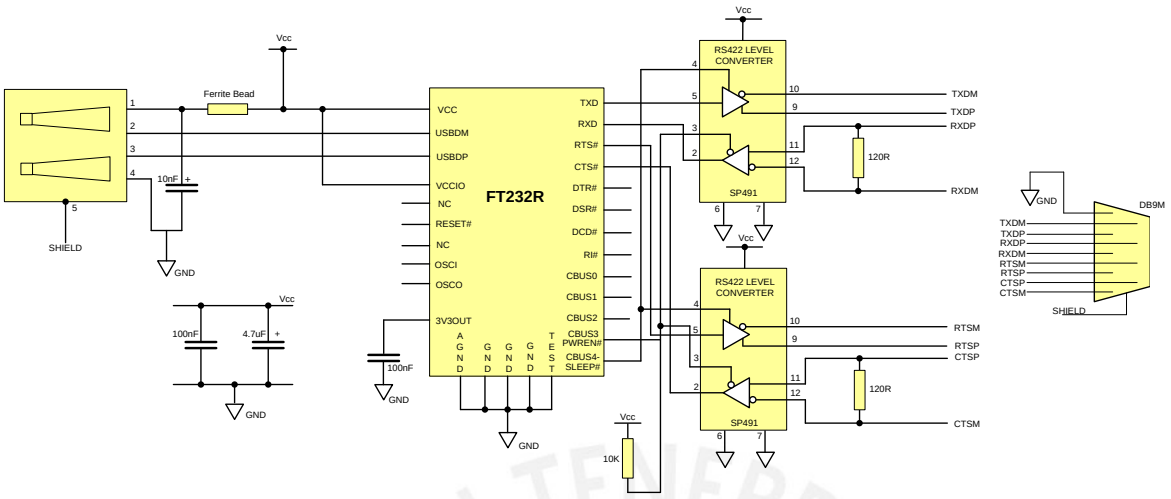


Figure 7.3 USB to RS422 Converter Configuration

An example of using the FT232R as a USB to RS422 converter is shown in Figure 7.3. In this application, two TTL to RS422 Level Converter ICs are used on the serial UART interface of the FT232R to convert the TTL levels of the FT232R to RS422 levels. There are many suitable level converter devices available. This example uses Sipex SP491 devices which have enables on both the transmitter and receiver. Since the SP491 transmitter enable is active high, it is connected to a CBUS pin in SLEEP# configuration. The SP491 receiver enable is active low and is therefore connected to a CBUS pin PWREN# configuration. This ensures that when both the SP491 transmitters and receivers are enabled then the device is active, and when the device is in USB suspend mode, the SP491 transmitters and receivers are disabled. If a similar application is used, but the design is USB BUS powered, it may be necessary to use a P-Channel logic level MOSFET (controlled by PWREN#) in the VCC line of the SP491 devices to ensure that the USB standby current of 2.5mA is met.

The SP491 is specified to transmit and receive data at a rate of up to 5 Mbaud. In this example the maximum data rate is limited to 3 Mbaud by the FT232R.

7.4 USB to MCU UART Interface

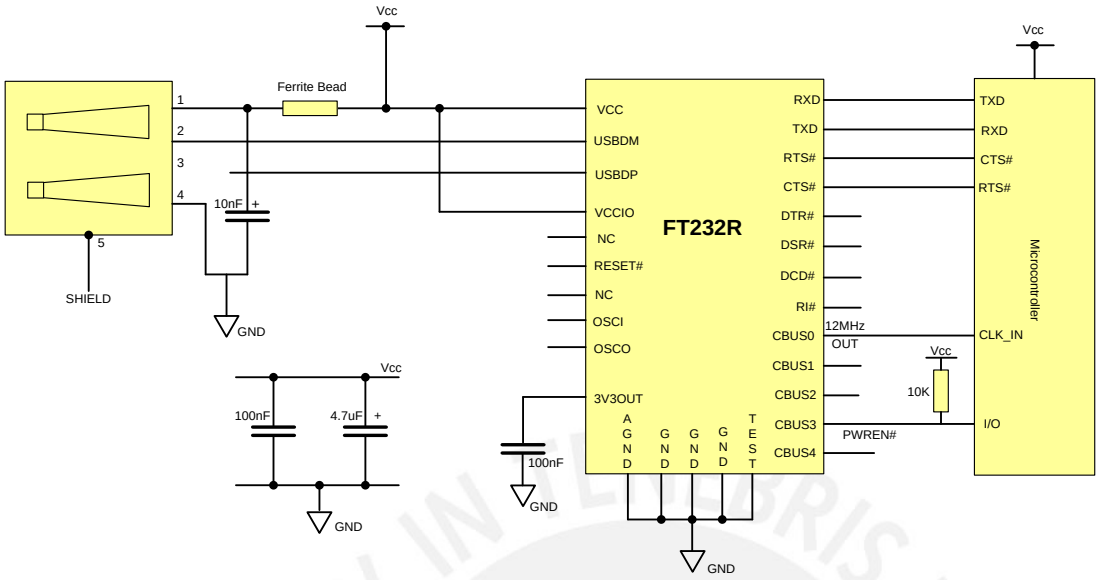


Figure 7.4 USB to MCU UART Interface

An example of using the FT232R as a USB to Microcontroller (MCU) UART interface is shown in Figure 7.4. In this application the FT232R uses TXD and RXD for transmission and reception of data, and RTS# / CTS# signals for hardware handshaking. Also in this example CBUS0 has been configured as a 12MHz output to clock the MCU.

Optionally, RI# could be connected to another I/O pin on the MCU and used to wake up the USB host controller from suspend mode. If the MCU is handling power management functions, then a CBUS pin can be configured as PWREN# and would also be connected to an I/O pin of the MCU.

7.5 LED Interface

Any of the CBUS I/O pins can be configured to drive an LED. The FT232R has 3 configuration options for driving LEDs from the CBUS. These are TXLED#, RXLED#, and TX&RXLED#. Refer to Section 3.5 for configuration options.

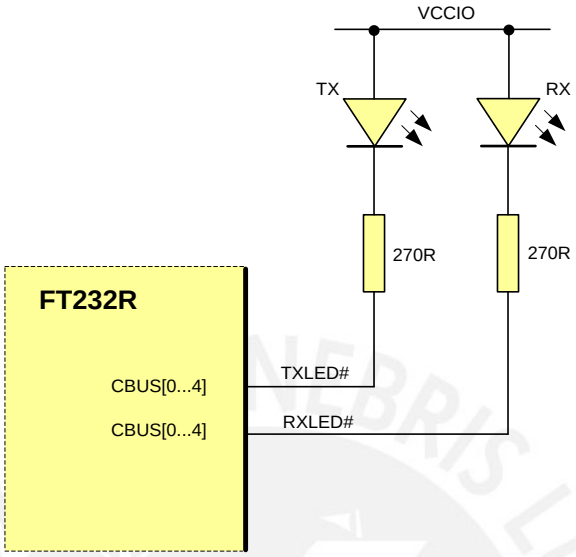


Figure 7.5 Dual LED Configuration

An example of using the FT232R to drive LEDs is shown in Figure 7.5. In this application one of the CBUS pins is used to indicate transmission of data (TXLED#) and another is used to indicate receiving data (RXLED#). When data is being transmitted or received the respective pins will drive from tri-state to low in order to provide indication on the LEDs of data transfer. A digital one-shot is used so that even a small percentage of data transfer is visible to the end user.

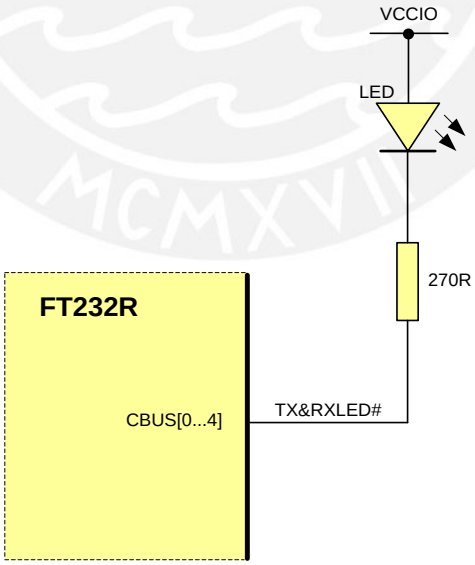


Figure 7.6 Single LED Configuration

Another example of using the FT232R to drive LEDs is shown in Figure 7.6. In this example one of the CBUS pins is used to indicate when data is being transmitted or received by the device (TX&RXLED). In this configuration the FT232R will drive only a single LED.

7.6 Using the External Oscillator

The FT232R defaults to operating using its own internal oscillator. This requires that the device is powered with VCC(min)=+4.0V. This supply voltage can be taken from the USB VBUS. Applications which require using an external oscillator, VCC= +3.3V, must do so in the following order:

1. When device powered for the very first time, it must have VCC > +4.0V. This supply is available from the USB VBUS supply = +5.0V.
2. The EEPROM must then be programmed to enable external oscillator. This EEPROM modification cannot be done using the FTDI programming utility, MPROG. The EEPROM can only be re-configured from a custom application. Please refer to the following applications note on how to do this:

   http://www.ftdichip.com/Documents/AppNotes/AN_100_Using_The_FT232_245R_With_External_Osc(FT_000067).pdf

3. The FT232R can then be powered from VCC=+3.3V and an external oscillator. This can be done using a link to switch the VCC supply.

The FT232R will fail to operate when the internal oscillator has been disabled, but no external oscillator has been connected.

8 Internal EEPROM Configuration

Following a power-on reset or a USB reset the FT232R will scan its internal EEPROM and read the USB configuration descriptors stored there. The default factory programmed values of the internal EEPROM are shown in Table 8.1.

Parameter	Value	Notes
USB Vendor ID (VID)	0403h	FTDI default VID (hex)
USB Product UD (PID)	6001h	FTDI default PID (hex)
Serial Number Enabled?	Yes	
Serial Number	See Note	A unique serial number is generated and programmed into the EEPROM during device final test.
Pull down I/O Pins in USB Suspend	Disabled	Enabling this option will make the device pull down on the UART interface lines when in USB suspend mode (PWREN# is high).
Manufacturer Name	FTDI	
Product Description	FT232R USB UART	
Max Bus Power Current	90mA	
Power Source	Bus Powered	
Device Type	FT232R	
USB Version	0200	Returns USB 2.0 device description to the host. Note: The device is a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 High Speed device (480Mb/s).
Remote Wake Up	Enabled	Taking RI# low will wake up the USB host controller from suspend in approximately 20 ms.
High Current I/Os	Disabled	Enables the high drive level on the UART and CBUS I/O pins.
Load VCP Driver	Enabled	Makes the device load the VCP driver interface for the device.
CBUS0	TXLED#	Default configuration of CBUS0 – Transmit LED drive.
CBUS1	RXLED#	Default configuration of CBUS1 – Receive LED drive.
CBUS2	TXDEN	Default configuration of CBUS2 – Transmit data enable for RS485
CBUS3	PWREN#	Default configuration of CBUS3 – Power enable. Low after USB enumeration, high during USB suspend mode.

Parameter	Value	Notes
CBUS4	SLEEP#	Default configuration of CBUS4 – Low during USB suspend mode.
Invert TXD	Disabled	Signal on this pin becomes TXD# if enable.
Invert RXD	Disabled	Signal on this pin becomes RXD# if enable.
Invert RTS#	Disabled	Signal on this pin becomes RTS if enable.
Invert CTS#	Disabled	Signal on this pin becomes CTS if enable.
Invert DTR#	Disabled	Signal on this pin becomes DTR if enable.
Invert DSR#	Disabled	Signal on this pin becomes DSR if enable.
Invert DCD#	Disabled	Signal on this pin becomes DCD if enable.
Invert RI#	Disabled	Signal on this pin becomes RI if enable.

Table 8.1 Default Internal EEPROM Configuration

The internal EEPROM in the FT232R can be programmed over USB using the FTDI utility program MPROG. MPROG can be downloaded from FTDI Utilities on the FTDI website (www.ftdichip.com). Version 2.8a or later is required for the FT232R chip. Users who do not have their own USB Vendor ID but who would like to use a unique Product ID in their design can apply to FTDI for a free block of unique PIDs. Contact FTDI support for this service.

9 Package Parameters

The FT232R is available in two different packages. The FT232RL is the SSOP-28 option and the FT232RQ is the QFN-32 package option. The solder reflow profile for both packages is described in Section 9.5.

9.1 SSOP-28 Package Dimensions

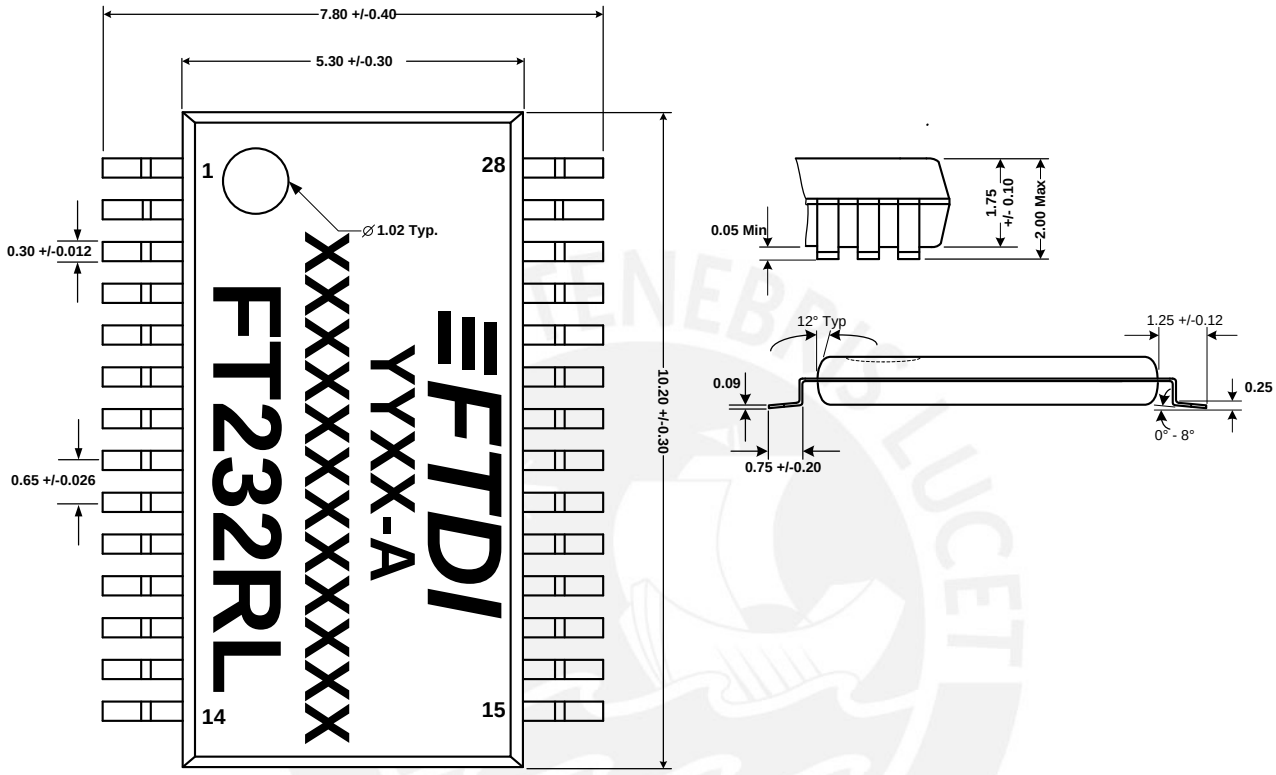


Figure 9.1 SSOP-28 Package Dimensions

The FT232RL is supplied in a RoHS compliant 28 pin SSOP package. The package is lead (Pb) free and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.

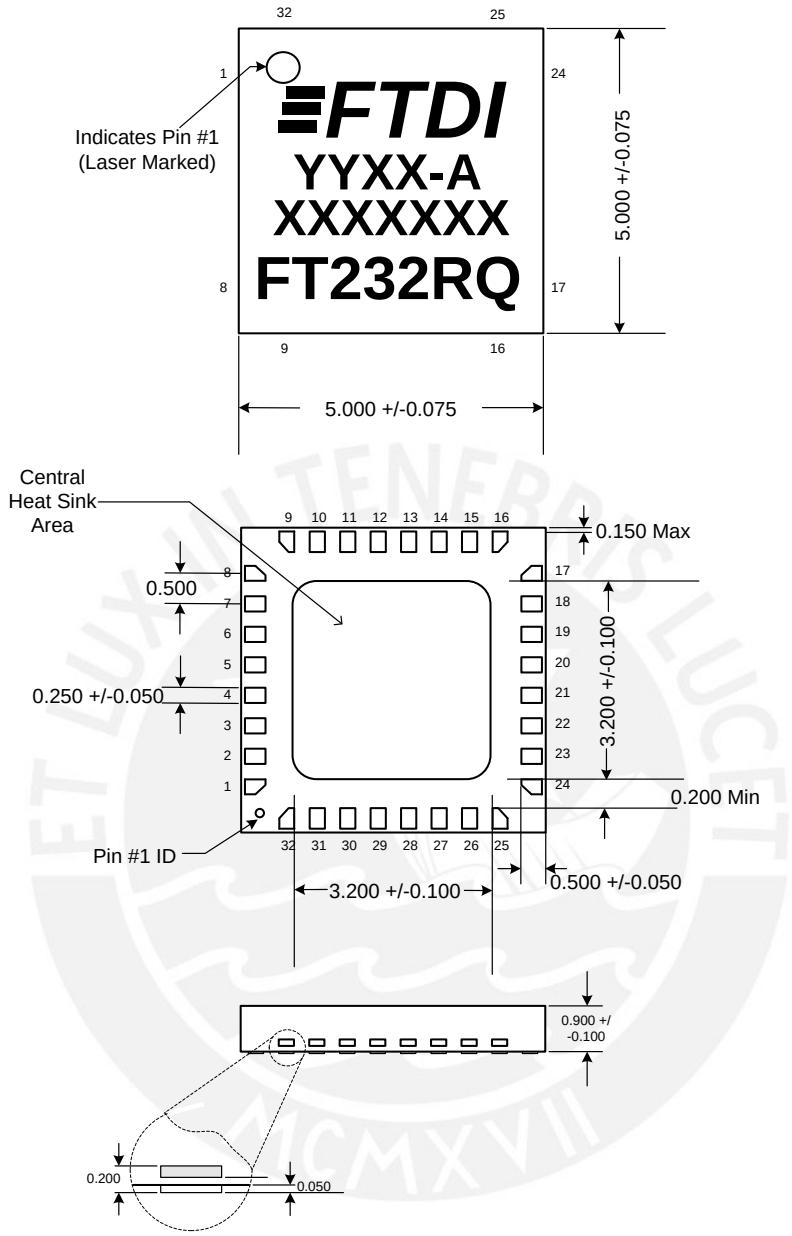
This package is nominally 5.30mm x 10.20mm body (7.80mm x 10.20mm including pins). The pins are on a 0.65 mm pitch. The above mechanical drawing shows the SSOP-28 package.

All dimensions are in millimetres.

The date code format is **YYXX** where XX = 2 digit week number, YY = 2 digit year number. This is followed by the revision number.

The code **XXXXXXXXXXXX** is the manufacturing LOT code. This only applies to devices manufactured after April 2009.

9.2 QFN-32 Package Dimensions



Note: The pin #1 ID is connected internally to the device's central heat sink area . It is recommended to ground the central heat sink area of the device.

Dimensions in mm.

Figure 9.2 QFN-32 Package Dimensions

The FT232RQ is supplied in a RoHS compliant leadless QFN-32 package. The package is lead (Pb) free, and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.

This package is nominally 5.00mm x 5.00mm. The solder pads are on a 0.50mm pitch. The above mechanical drawing shows the QFN-32 package. All dimensions are in millimetres.

The centre pad on the base of the FT232RQ is not internally connected, and can be left unconnected, or connected to ground (recommended).

The date code format is **YYXX** where XX = 2 digit week number, YY = 2 digit year number.

The code **XXXXXXX** is the manufacturing LOT code. This only applies to devices manufactured after April 2009.

9.3 QFN-32 Package Typical Pad Layout

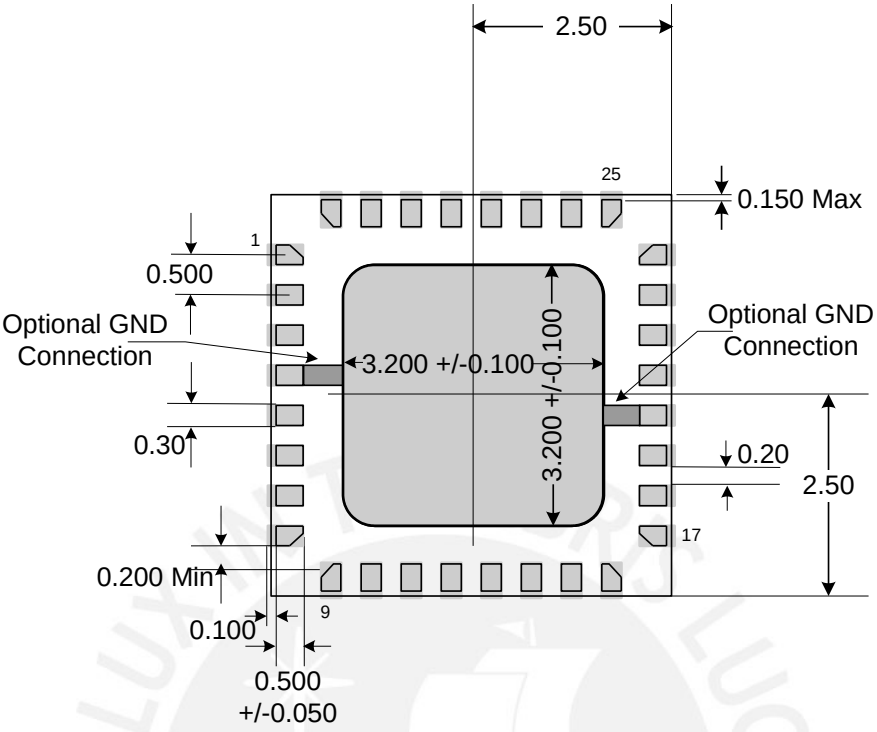


Figure 9.3 Typical Pad Layout for QFN-32 Package

9.4 QFN-32 Package Typical Solder Paste Diagram

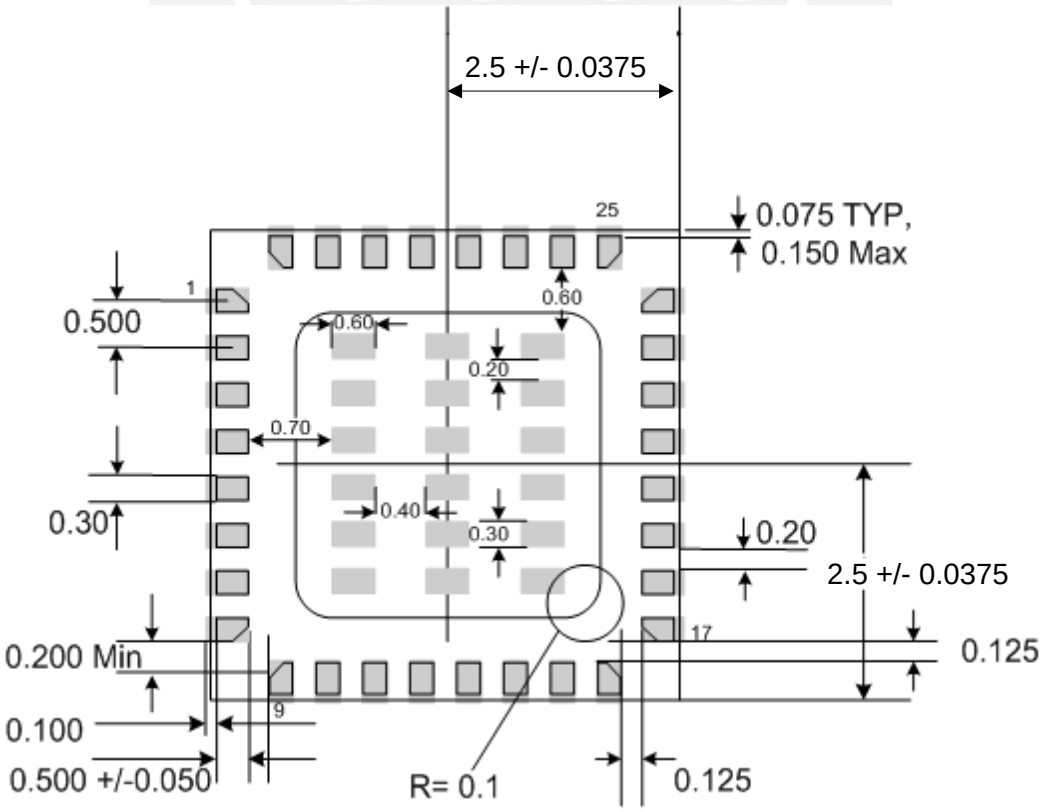


Figure 9.4 Typical Solder Paste Diagram for QFN-32 Package

9.5 Solder Reflow Profile

The FT232R is supplied in Pb free 28 LD SSOP and QFN-32 packages. The recommended solder reflow profile for both package options is shown in Figure 9.5.

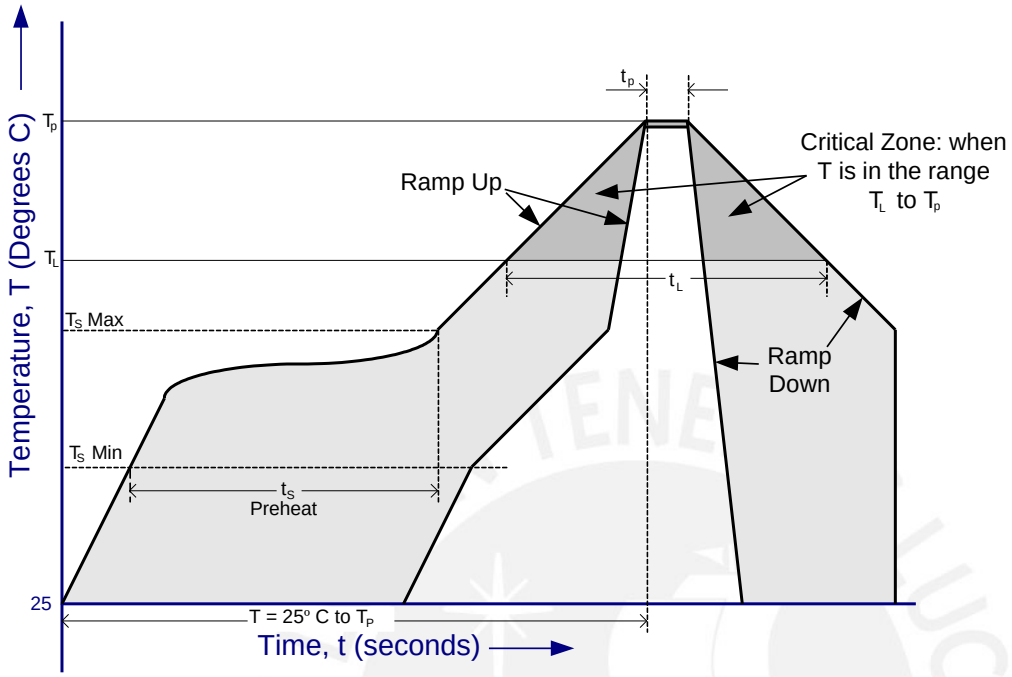


Figure 9.5 FT232R Solder Reflow Profile

The recommended values for the solder reflow profile are detailed in Table 9.1. Values are shown for both a completely Pb free solder process (i.e. the FT232R is used with Pb free solder), and for a non-Pb free solder process (i.e. the FT232R is used with non-Pb free solder).

Profile Feature	Pb Free Solder Process	Non-Pb Free Solder Process
Average Ramp Up Rate (T_s to T_p)	3°C / second Max.	3°C / Second Max.
Preheat - Temperature Min (T_s Min.) - Temperature Max (T_s Max.) - Time (t_s Min to t_s Max)	 150°C 200°C 60 to 120 seconds	 100°C 150°C 60 to 120 seconds
Time Maintained Above Critical Temperature T_L: - Temperature (T_L) - Time (t_L)	 217°C 60 to 150 seconds	 183°C 60 to 150 seconds
Peak Temperature (T_p)	260°C	240°C
Time within 5°C of actual Peak Temperature (t_p)	20 to 40 seconds	20 to 40 seconds
Ramp Down Rate	6°C / second Max.	6°C / second Max.
Time for T= 25°C to Peak Temperature, T_p	8 minutes Max.	6 minutes Max.

Table 9.1 Reflow Profile Parameter Values

10 Contact Information

Head Office – Glasgow, UK

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Web Shop URL http://www.ftdichip.com

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Web Site URL: http://www.ftdichip.com

Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – References

Useful Application Notes

http://www.ftdichip.com/Documents/AppNotes/AN232R-01_FT232RBitBangModes.pdf

http://www.ftdichip.com/Documents/AppNotes/AN_107_AdvancedDriverOptions_AN_000073.pdf

http://www.ftdichip.com/Documents/AppNotes/AN232R-02_FT232RChipID.pdf

http://www.ftdichip.com/Documents/AppNotes/AN_121_FTDI_Device_EEPROM_User_Area_Usage.pdf

http://www.ftdichip.com/Documents/AppNotes/AN_120_Aliasing_VCP_Baud_Rates.pdf

http://www.ftdichip.com/Documents/AppNotes/AN_100_Using_The_FT232_245R_With_External_Osc(FT_000067).pdf

http://www.ftdichip.com/Resources/Utilities/AN_126_User_Guide_For_FT232_Factory%20test%20utility.pdf

http://www.ftdichip.com/Documents/AppNotes/AN232B-05_BaudRates.pdf

http://www.ftdichip.com/Documents/InstallGuides.htm

Appendix B - List of Figures and Tables

List of Figures

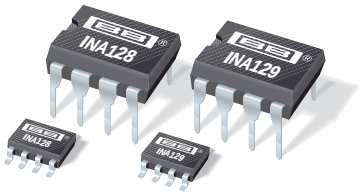
List of Tables

Appendix C - Revision History

Document Title:	USB UART IC FT232R
Document Reference No.:	FT_000053
Clearance No.:	FTDI# 38
Product Page:	http://www.ftdichip.com/FTProducts.htm
Document Feedback:	Send Feedback

Version 0.90	Initial Datasheet Created	August 2005
Version 0.96	Revised Pre-release datasheet	October 2005
Version 1.00	Full datasheet released	December 2005
Version 1.02	Minor revisions to datasheet	December 2005
Version 1.03	Manufacturer ID added to default EEPROM configuration; Buffer sizes added	January 2006
Version 1.04	QFN-32 Pad layout and solder paste diagrams added	January 2006
Version 2.00	Reformatted, updated package info, added notes for 3.3V operation; Part numbers, TID; added UART and CBUS characteristics for +1.8V; Corrected RESET#; Added MTTF data; Corrected the input switching threshold and input hysteresis values for VCCIO=5V	June 2008
Version 2.01	Corrected pin-out number in table3.2 for GND pin18. Improved graphics on some Figures. Add packing details. Changed USB suspend current spec from 500uA to 2.5mA Corrected Figure 9.2 QFN dimensions.	August 2008
Version 2.02	Corrected Tape and Reel quantities. Added comment "PWREN# should be used with a 10kΩ resistor pull up". Replaced TXDEN# with TXDEN since it is active high in various places. Added lot number to the device markings. Added 3V3 regulator output tolerance. Clarified VCC operation and added section headed "Using an external Oscillator" Updated company contact information.	April 2009
Version 2.03	Corrected the RX/TX buffer definitions to be relative to the USB interface	June 2009
Version 2.04	Additional dimensions added to QFN solder profile	June 2009
Version 2.05	Modified package dimensions to 5.0 x 5.0 +/-0.075mm. and Solder paste diagram to 2.50 x 2.50 +/-0.0375mm Added Windows 7 32, 64 bit driver support Added FT_PROG utility references Added Appendix A-references.Figure 2.1 updated. Updated USB-IF TID for Rev B	December 2009
Version 2.06	Updated section 6.2, Figure 6.2 and the note, Updated section 5.3, Table 5.13, EEPROM data retention time	May 2010
Version 2.07	Added USB Certification Logos	July 2010
Version 2.08	Updated USB-IF TID for Rev C	April 2011
Version 2.09	Corrected Rev C TID number	April 2011
Version 2.10	Table 3.9, added clock output frequency within ±0.7% Edited Table 3.9, TXLED# and TXLED# Description Added feedback links	March 2012

BURR - BROWN®



INA128
INA129

Precision, Low Power INSTRUMENTATION AMPLIFIERS

FEATURES

- LOW OFFSET VOLTAGE: 50µV max
- LOW DRIFT: 0.5µV/°C max
- LOW INPUT BIAS CURRENT: 5nA max
- HIGH CMR: 120dB min
- INPUTS PROTECTED TO ±40V
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 700µA
- 8-PIN PLASTIC DIP, SO-8

APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

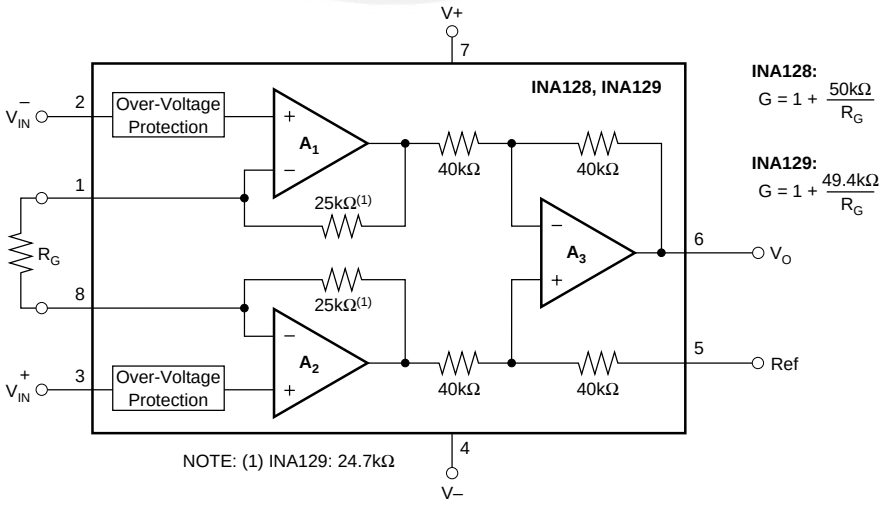
DESCRIPTION

The INA128 and INA129 are low power, general purpose instrumentation amplifiers offering excellent accuracy. Their versatile 3-op amp design and small size make them ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200kHz at G = 100).

A single external resistor sets any gain from 1 to 10,000. INA128 provides an industry standard gain equation; INA129's gain equation is compatible with the AD620.

The INA128/INA129 is laser trimmed for very low offset voltage (50µV), drift (0.5µV/°C) and high common-mode rejection (120dB at G ≥ 100). It operates with power supplies as low as ±2.25V, and quiescent current is only 700µA—ideal for battery operated systems. Internal input protection can withstand up to ±40V without damage.

The INA128/INA129 is available in 8-pin plastic DIP, and SO-8 surface-mount packages, specified for the –40°C to +85°C temperature range. The INA128 is also available in dual configuration, the INA2128.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1296C
Printed in U.S.A. October, 1996

SPECIFICATIONS

At T_A = +25°C, V_S = ±15V, R_L = 10kΩ, unless otherwise noted.

PARAMETER	CONDITIONS	INA128P, U INA129P, U MIN	INA128P, U INA129P, U TYP	INA128P, U INA129P, U MAX	INA128PA, UA INA129PA, UA MIN	INA128PA, UA INA129PA, UA TYP	INA128PA, UA INA129PA, UA MAX	UNITS
INPUT								
Offset Voltage, RTI								
Initial	T_A = +25°C		±10 ±100/G	±50 ±500/G		±25 ±100/G	±125 ±1000/G	µV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		±0.2 ± 2/G	±0.5 ± 20/G		±0.2 ± 5/G	±1 ± 20/G	µV/°C
vs Power Supply	V_S = ±2.25V to ±18V		±0.2 ±20/G	±1 ±100/G		*	±2 ±200/G	µV/V
Long-Term Stability			±0.1 ±3/G			*		µV/mo
Impedance, Differential			10^{10} || 2			*		Ω || pF
Common-Mode			10^{11} || 9			*		Ω || pF
Common-Mode Voltage Range[1]	V_O = 0V	(V+) – 2	(V+) – 1.4		*	*		V
		(V–) + 2	(V–) + 1.7		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	V_{CM} = ±13V, ΔR_S = 1kΩ							
	G=1	80	86		73	*		dB
	G=10	100	106		93	*		dB
	G=100	120	125		110	*		dB
	G=1000	120	130		110	*		dB
BIAS CURRENT			±2	±5		*	±10	nA
vs Temperature			±30			*		pA/°C
Offset Current			±1	±5		*	±10	nA
vs Temperature			±30			*		pA/°C
NOISE VOLTAGE, RTI	G = 1000, R_S = 0Ω							
f = 10Hz			10			*		nV/√Hz
f = 100Hz			8			*		nV/√Hz
f = 1kHz			8			*		nV/√Hz
f_B = 0.1Hz to 10Hz			0.2			*		µVp-p
Noise Current								
f=10Hz			0.9			*		pA/√Hz
f=1kHz			0.3			*		pA/√Hz
f_B = 0.1Hz to 10Hz			30			*		pAp-p
GAIN								
Gain Equation, INA128			1 + (50kΩ/R_G)			*		V/V
INA129			1 + (49.4kΩ/R_G)			*		V/V
Range of Gain		1		10000	*		*	V/V
Gain Error	G=1		±0.01	±0.024		*	±0.1	%
	G=10		±0.02	±0.4		*	±0.5	%
	G=100		±0.05	±0.5		*	±0.7	%
	G=1000		±0.5	±1		*	±2	%
Gain vs Temperature[2]	G=1		±1	±10		*	*	ppm/°C
50kΩ (or 49.4kΩ) Resistance[2, 3]			±25	±100		*	*	ppm/°C
Nonlinearity	V_O = ±13.6V, G=1		±0.0001	±0.001		*	±0.002	% of FSR
	G=10		±0.0003	±0.002		*	±0.004	% of FSR
	G=100		±0.0005	±0.002		*	±0.004	% of FSR
	G=1000		±0.001	(Note 4)		*	*	% of FSR
OUTPUT								
Voltage: Positive	R_L = 10kΩ	(V+) – 1.4	(V+) – 0.9		*	*		V
Negative	R_L = 10kΩ	(V–) + 1.4	(V–) + 0.8		*	*		V
Load Capacitance Stability			1000			*		pF
Short-Circuit Current			+6/–15			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G=1		1.3			*		MHz
	G=10		700			*		kHz
	G=100		200			*		kHz
	G=1000		20			*		kHz
Slew Rate	V_O = ±10V, G=10		4			*		V/µs
Settling Time, 0.01%	G=1		7			*		µs
	G=10		7			*		µs
	G=100		9			*		µs
	G=1000		80			*		µs
Overload Recovery	50% Overdrive		4			*		µs
POWER SUPPLY								
Voltage Range		±2.25	±15	±18	*	*	*	V
Current, Total	V_{IN} = 0V		±700	±750		*	*	µA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating		–40		125	*		*	°C
θ_{JA} 8-Pin Dip			80			*		°C/W
SO-8 SOIC			150			*		°C/W

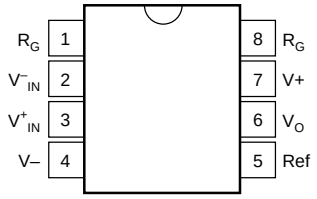
* Specification same as INA128P, U or INA129P, U.

NOTE: (1) Input common-mode range varies with output voltage—see typical curves. (2) Guaranteed by wafer test. (3) Temperature coefficient of the 50kΩ (or 49.4kΩ) term in the gain equation. (4) Nonlinearity measurements in G = 1000 are dominated by noise. Typical nonlinearity is ±0.001%.

PIN CONFIGURATION

8-Pin DIP and SO-8

Top View



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Analog Input Voltage Range	±40V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

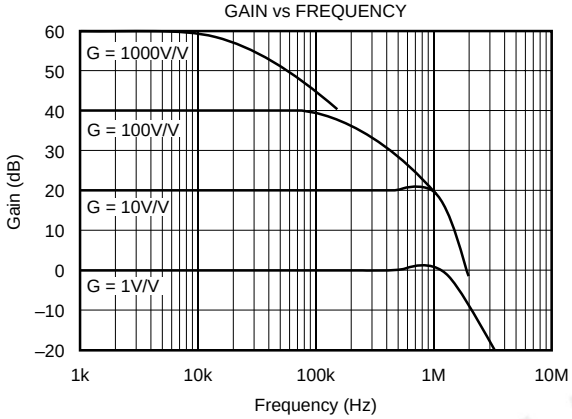
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
INA128PA	8-Pin Plastic DIP	006	–40°C to +85°C
INA128P	8-Pin Plastic DIP	006	–40°C to +85°C
INA128UA	SO-8 Surface-Mount	182	–40°C to +85°C
INA128U	SO-8 Surface-Mount	182	–40°C to +85°C
INA129PA	8-Pin Plastic DIP	006	–40°C to +85°C
INA129P	8-Pin Plastic DIP	006	–40°C to +85°C
INA129UA	SO-8 Surface-Mount	182	–40°C to +85°C
INA129U	SO-8 Surface-Mount	182	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

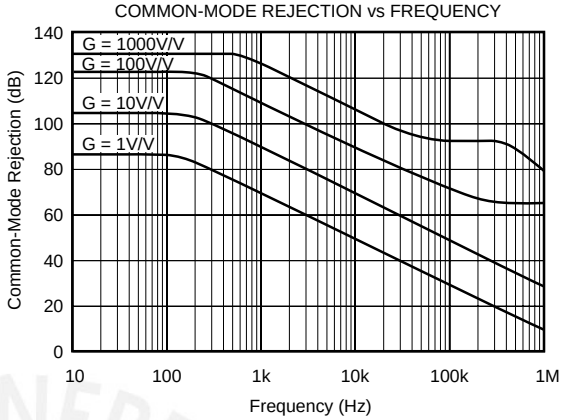
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

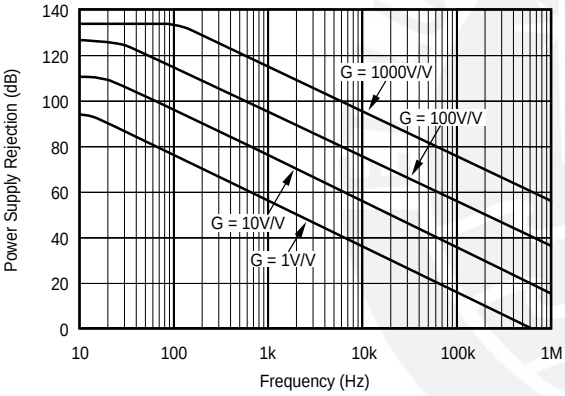
GAIN vs FREQUENCY



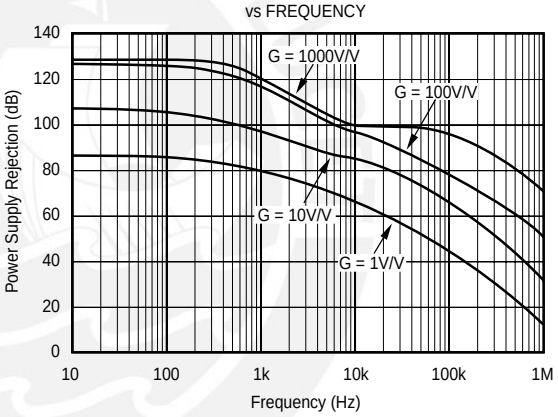
COMMON-MODE REJECTION vs FREQUENCY



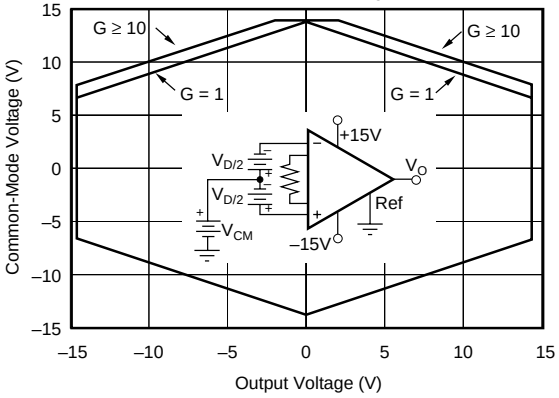
POSITIVE POWER SUPPLY REJECTION vs FREQUENCY



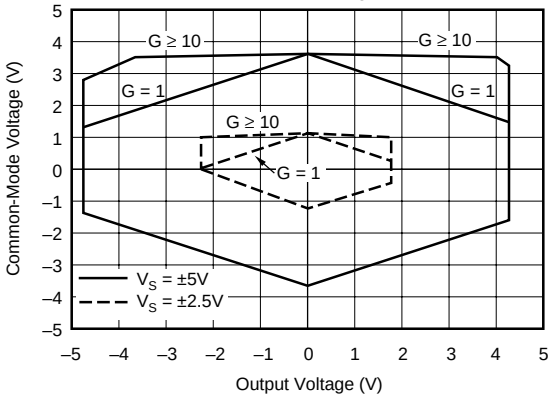
NEGATIVE POWER SUPPLY REJECTION vs FREQUENCY



INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE, V_S = ±15V



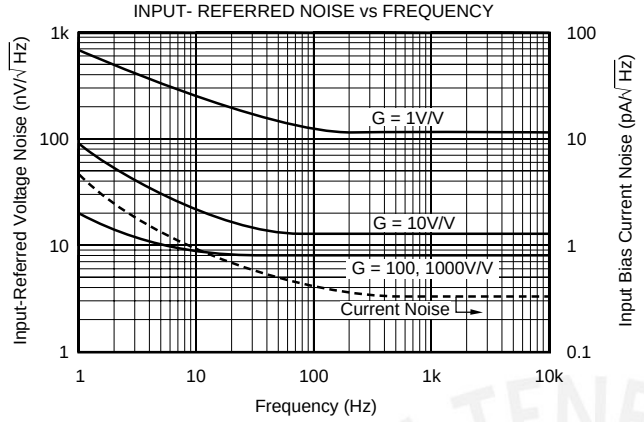
INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE, V_S = ±5, ±2.5V



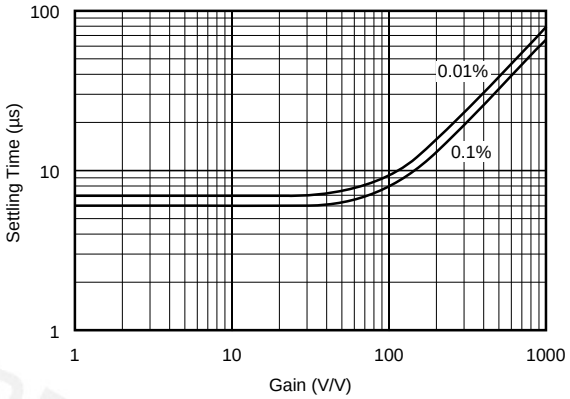
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

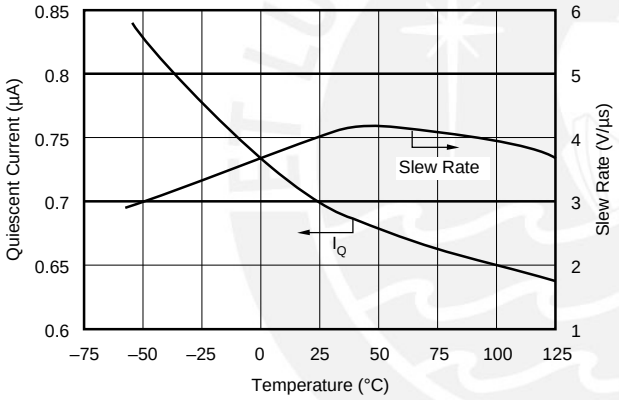
INPUT- REFERRED NOISE vs FREQUENCY



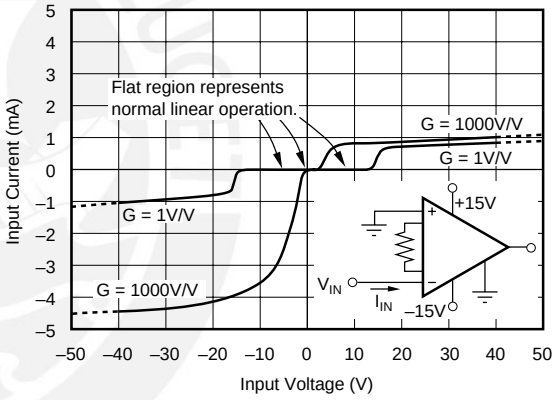
SETTLING TIME vs GAIN



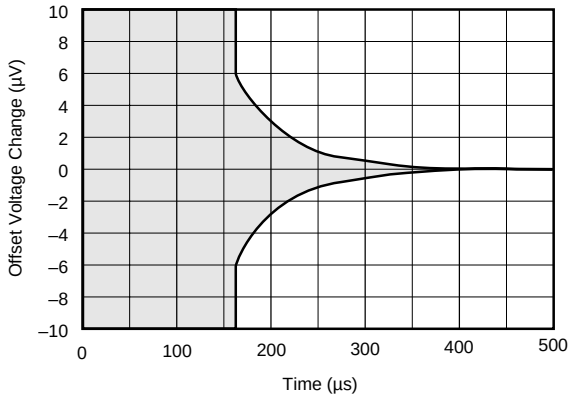
QUIESCENT CURRENT and SLEW RATE vs TEMPERATURE



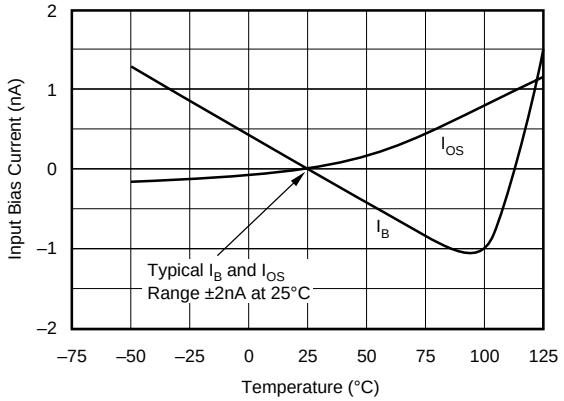
INPUT OVER-VOLTAGE V/I CHARACTERISTICS



INPUT OFFSET VOLTAGE WARM-UP



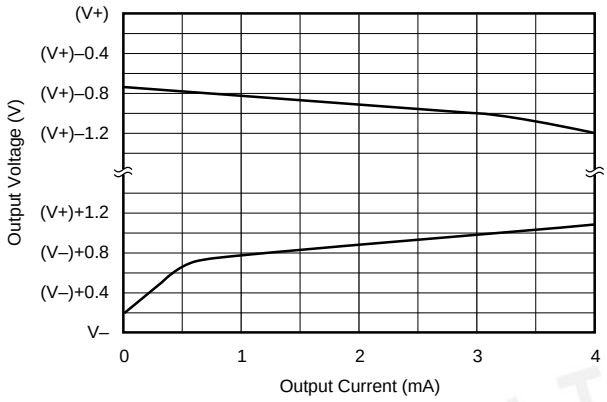
INPUT BIAS CURRENT vs TEMPERATURE



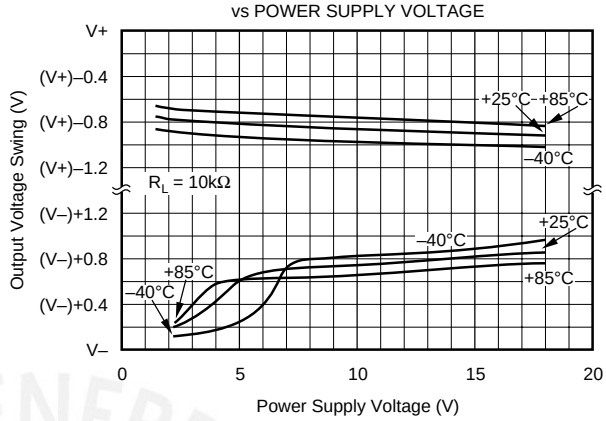
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

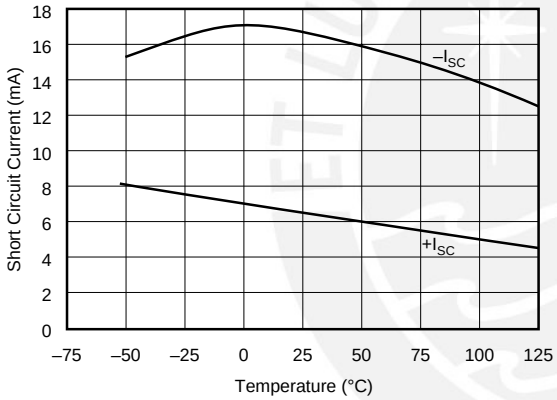
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



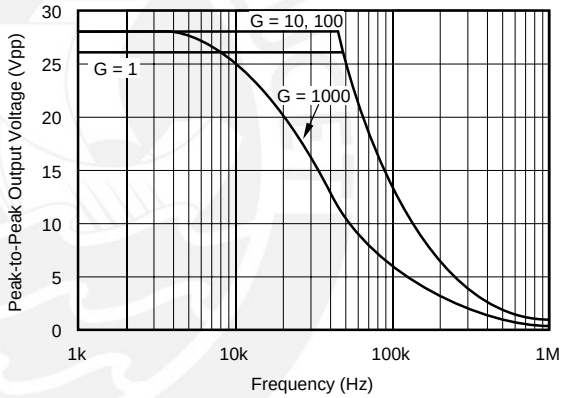
OUTPUT VOLTAGE SWING vs POWER SUPPLY VOLTAGE



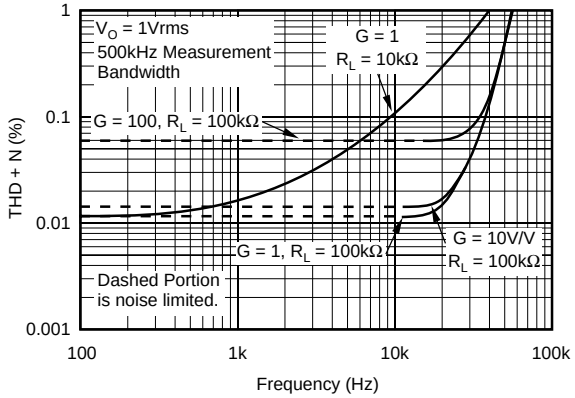
SHORT-CIRCUIT OUTPUT CURRENT vs TEMPERATURE



MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



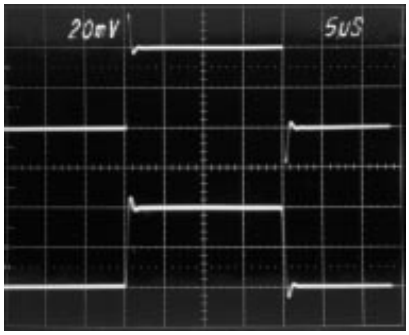
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

SMALL-SIGNAL
(G = 1, 10)



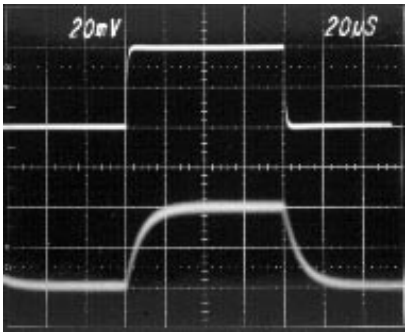
G = 1

20mV/div

G = 10

5µs/div

SMALL-SIGNAL
(G = 100, 1000)



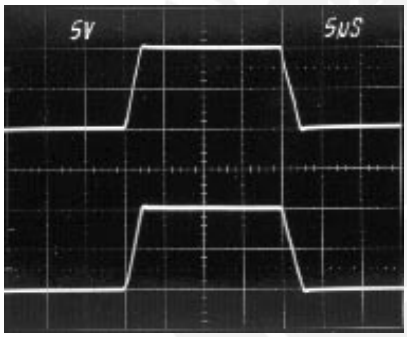
G = 100

20mV/div

G = 1000

20µs/div

LARGE-SIGNAL
(G = 1, 10)



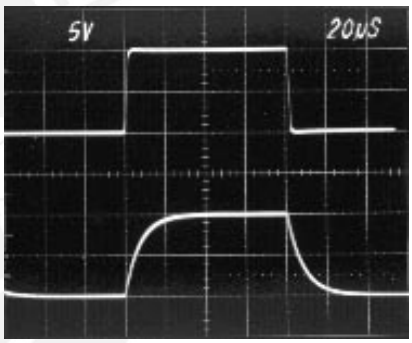
G = 1

5V/div

G = 10

5µs/div

LARGE-SIGNAL
(G = 100, 1000)



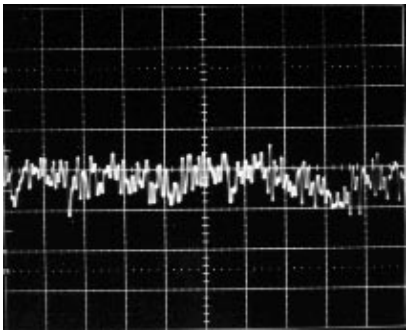
G = 100

5V/div

G = 1000

20µs/div

VOLTAGE NOISE 0.1 to 10Hz
INPUT-REFERRED, G ≥ 100



0.1µV/div

1s/div

APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA128/INA129. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 8Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

SETTING THE GAIN

Gain is set by connecting a single external resistor, R_G, connected between pins 1 and 8:

INA128:
$$G = 1 + \frac{50k\Omega}{R_G} \quad (1)$$

INA129:
$$G = 1 + \frac{49.4k\Omega}{R_G} \quad (2)$$

Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in Equation 1 (49.4kΩ in Equation 2) comes from the sum of the two internal feedback resistors of A_1 and A_2. These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these internal resistors are included in the gain accuracy and drift specifications of the INA128/INA129.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

DYNAMIC PERFORMANCE

The typical performance curve "Gain vs Frequency" shows that, despite its low quiescent current, the INA128/INA129 achieves wide bandwidth, even at high gain. This is due to the current-feedback topology of the input stage circuitry. Settling time also remains excellent at high gain.

NOISE PERFORMANCE

The INA128/INA129 provides very low noise in most applications. Low frequency noise is approximately 0.2µVp-p measured from 0.1 to 10Hz (G ≥ 100). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

INA128: $G = 1 + \frac{50k\Omega}{R_G}$ **INA129:** $G = 1 + \frac{49.4k\Omega}{R_G}$

DESIRED GAIN (V/V)	INA128 R_G (Ω)	INA128 NEAREST 1% R_G (Ω)	INA129 R_G (Ω)	INA129 NEAREST 1% R_G (Ω)
1	NC	NC	NC	NC
2	50.00k	49.9k	49.4k	49.9k
5	12.50k	12.4k	12.35k	12.4k
10	5.556k	5.62k	5489	5.49k
20	2.632k	2.61k	2600	2.61k
50	1.02k	1.02k	1008	1k
100	505.1	511	499	499
200	251.3	249	248	249
500	100.2	100	99	100
1000	50.05	49.9	49.5	49.9
2000	25.01	24.9	24.7	24.9
5000	10.00	10	9.88	9.76
10000	5.001	4.99	4.94	4.87

NC: No Connection.

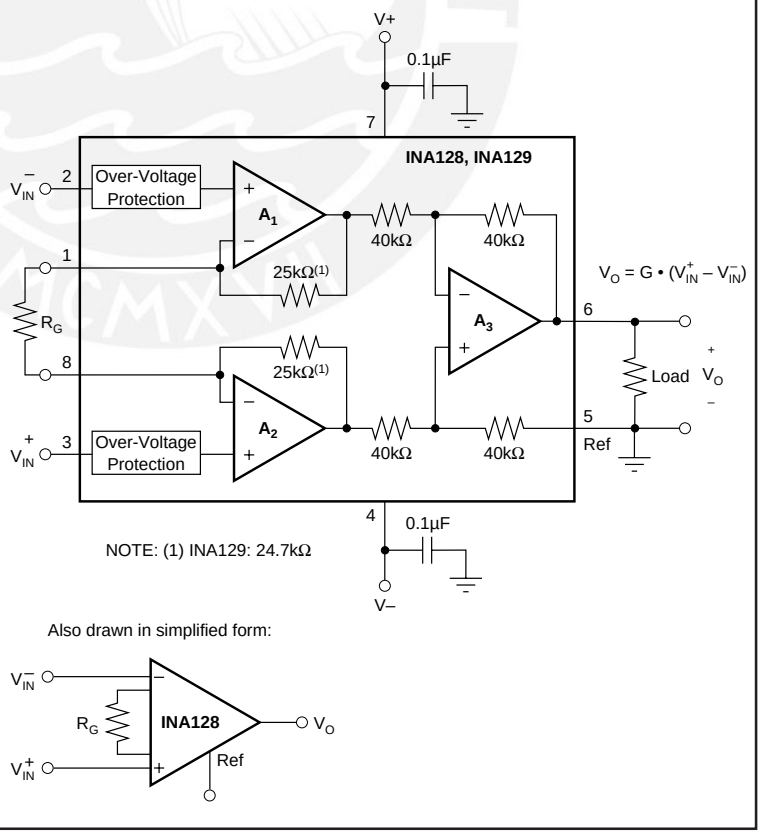


FIGURE 1. Basic Connections.

OFFSET TRIMMING

The INA128/INA129 is laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed with the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.

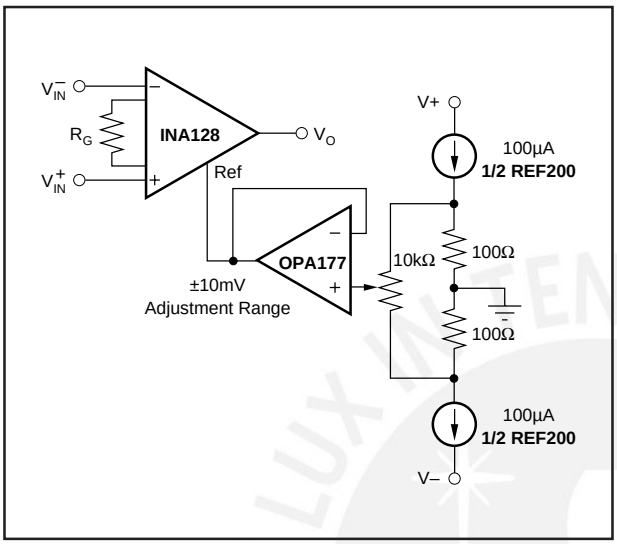


FIGURE 2. Optional Trimming of Output Offset Voltage.

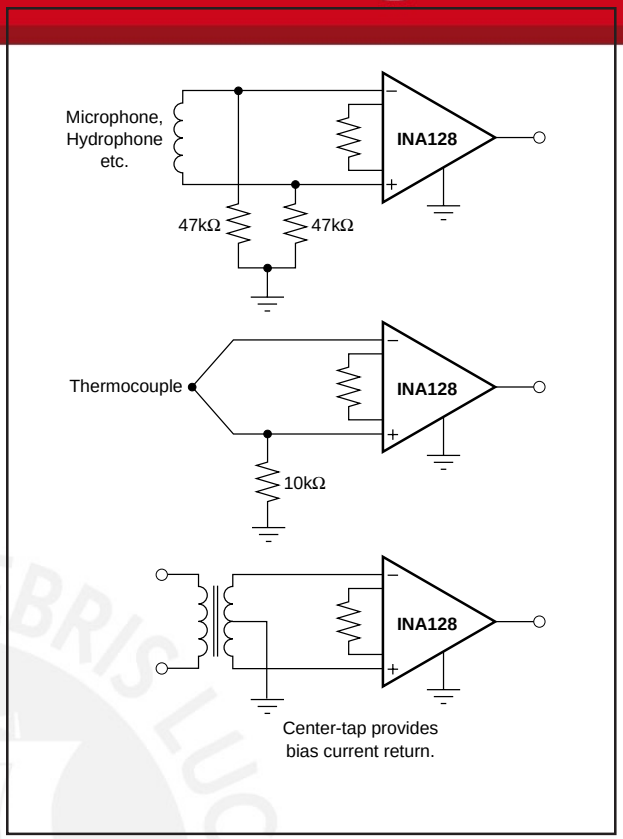


FIGURE 3. Providing an Input Common-Mode Current Path.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA128/INA129 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is approximately ±2nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range, and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA128/INA129 is from approximately 1.4V below the positive supply voltage to 1.7V above the negative supply. As a differential input voltage causes the output voltage increase, however, the linear input range will be limited by the output voltage swing of amplifiers A_1 and A_2. So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see performance curves “Input Common-Mode Range vs Output Voltage”.

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of A_3 will be near 0V even though both inputs are overloaded.

LOW VOLTAGE OPERATION

The INA128/INA129 can be operated on power supplies as low as ±2.25V. Performance remains excellent with power supplies ranging from ±2.25V to ±18V. Most parameters vary only slightly throughout this supply voltage range—see typical performance curves. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Typical performance curves, “Input Common-Mode Range vs Output Voltage” show the range of linear operation for ±15V, ±5V, and ±2.5V supplies.

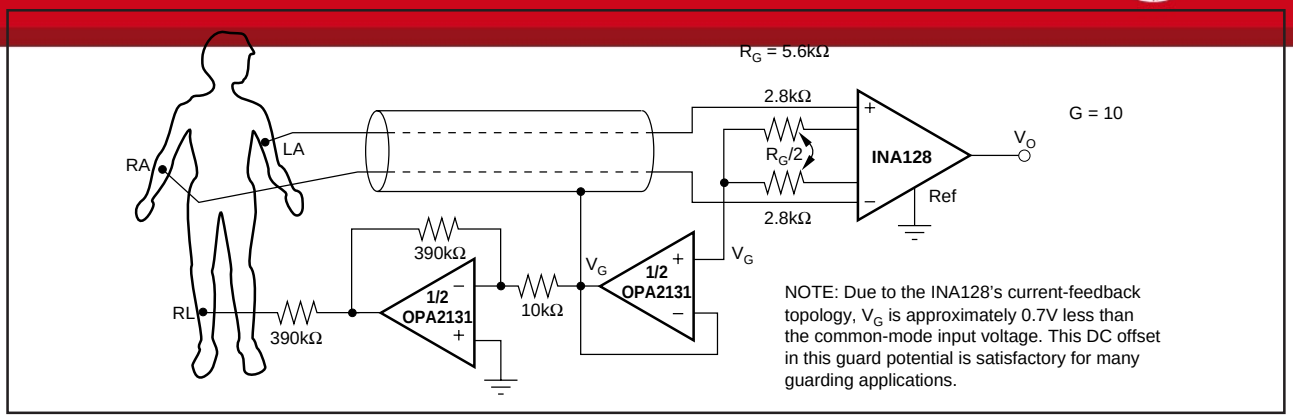


FIGURE 4. ECG Amplifier With Right-Leg Drive.

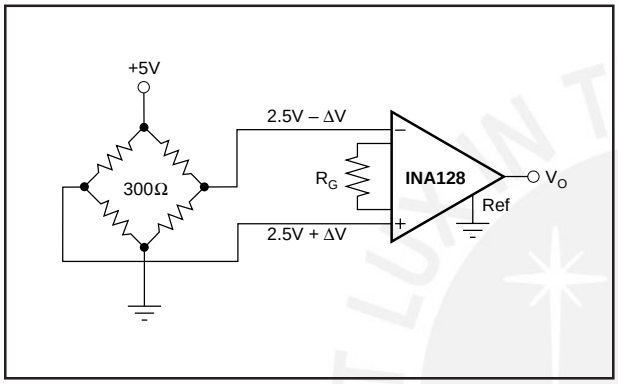


FIGURE 5. Bridge Amplifier.

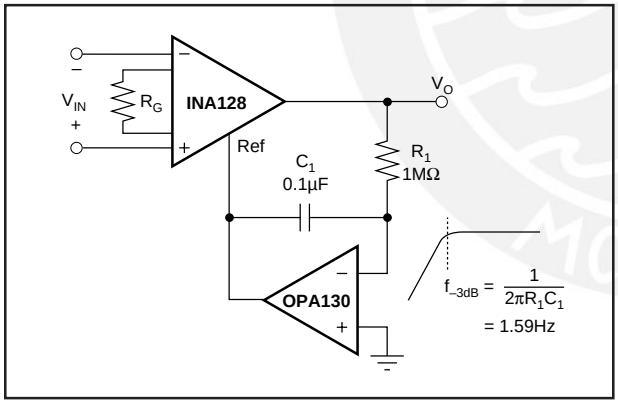
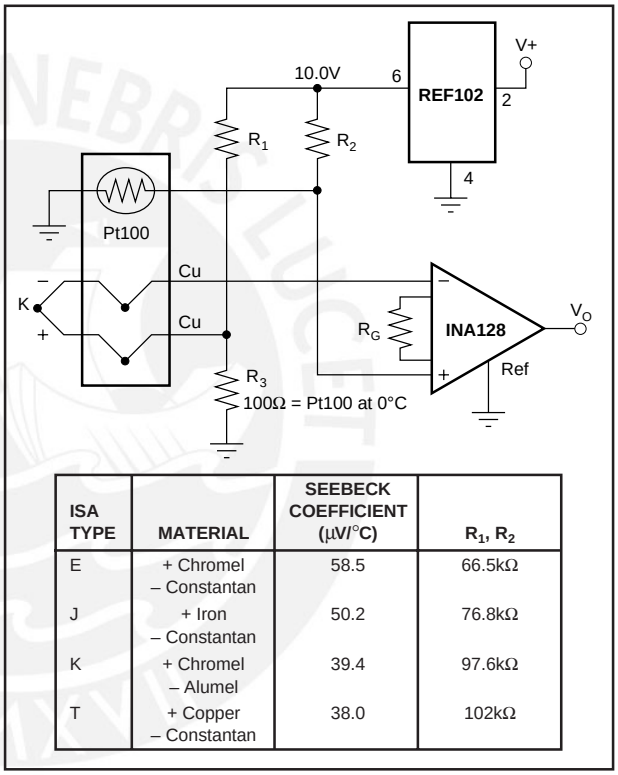
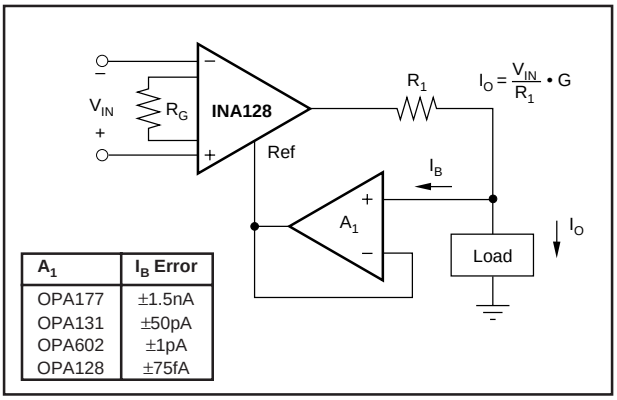


FIGURE 6. AC-Coupled Instrumentation Amplifier.



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (µV/°C)	R_1, R_2
E	+ Chromel – Constantan	58.5	66.5kΩ
J	+ Iron – Constantan	50.2	76.8kΩ
K	+ Chromel – Alumel	39.4	97.6kΩ
T	+ Copper – Constantan	38.0	102kΩ

FIGURE 7. Thermocouple Amplifier With RTD Cold-Junction Compensation.



A_1	I_B Error
OPA177	±1.5nA
OPA131	±50pA
OPA602	±1pA
OPA128	±75fA

FIGURE 8. Differential Voltage to Current Converter.

Low Power, Single Resistor Gain Programmable, Precision Instrumentation Amplifier

FEATURES

- **Supply Current: 530μA Max**
- **Meets IEC 1000-4-2 Level 4 (±15kV) ESD Tests with Two External 5k Resistors**
- **Single Gain Set Resistor: G = 1 to 10,000**
- **Gain Error: G = 10, 0.4% Max**
- **Input Offset Voltage Drift: 0.3μV/°C Max**
- Gain Nonlinearity: G = 10, 20ppm Max
- Input Offset Voltage: 40μV Max
- Input Bias Current: 250pA Max
- PSRR at A_V =1: 103dB Min
- CMRR at A_V = 1: 90dB Min
- Wide Supply Range: ±2.3V to ±18V
- 1kHz Voltage Noise: 10nV/√Hz
- 0.1Hz to 10Hz Noise: 0.28μV_{P-P}
- Available in 8-Pin PDIP and SO Packages

APPLICATIONS

- Bridge Amplifiers
- Strain Gauge Amplifiers
- Thermocouple Amplifiers
- Differential to Single-Ended Converters
- Differential Voltage to Current Converters
- Data Acquisition
- Battery-Powered and Portable Equipment
- Medical Instrumentation
- Scales

DESCRIPTION

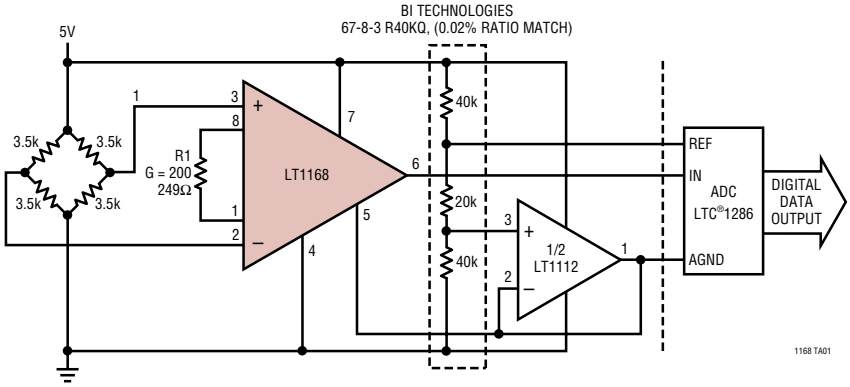
The LT®1168 is a micropower, precision instrumentation amplifier that requires only one external resistor to set gains of 1 to 10,000. The low voltage noise of 10nV/√Hz (at 1kHz) is not compromised by low power dissipation (350μA typical for ±15V supplies). The wide supply range of ±2.3V to ±18V allows the LT1168 to fit into a wide variety of industrial as well as battery-powered applications.

The high accuracy of the LT1168 is due to a 20ppm maximum nonlinearity and 0.4% max gain error (G = 10). Previous monolithic instrumentation amps cannot handle a 2k load resistor whereas the nonlinearity of the LT1168 is specified for loads as low as 2k. The LT1168 is laser trimmed for very low input offset voltage (40μV max), drift (0.3μV/°C), high CMRR (90dB, G = 1) and PSRR (103dB, G = 1). Low input bias currents of 250pA max are achieved with the use of superbeta processing. The output can handle capacitive loads up to 1000pF in any gain configuration while the inputs are ESD protected up to 13kV (human body). The LT1168 with two external 5k resistors passes the IEC 1000-4-2 level 4 specification.

The LT1168 is a pin-for-pin improved second source for the AD620 and INA118. The LT1168, offered in 8-pin PDIP and SO packages, requires significantly less PC board area than discrete op amp resistor designs. These advantages make the LT1168 the most cost effective solution for precision instrumentation amplifier applications.

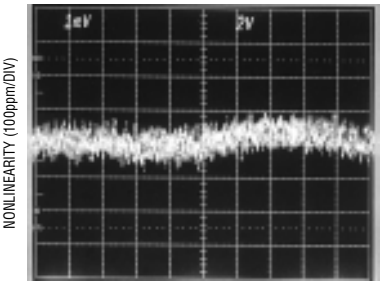
TYPICAL APPLICATION

Single Supply* Pressure Monitor



*See Theory of Operation section

Gain Nonlinearity



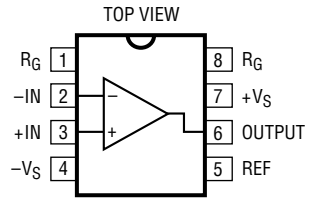
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage ..... ±20V
Differential Input Voltage (Within the Supply Voltage) ..... ±40V
Input Voltage (Equal to Supply Voltage) ..... ±20V
Input Current (Note 2) ..... ±20mA
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4) .. –40°C to 85°C
Specified Temperature Range
LT1168AC/LT1168C (Note 5) ..... –40°C to 85°C
LT1168AI/LT1168I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 150°C/ W (N8)
T_{JMAX} = 150°C, θ_{JA} = 190°C/ W (S8)

ORDER PART NUMBER
LT1168ACN8
LT1168ACS8
LT1168AIN8
LT1168AIS8
LT1168CN8
LT1168CS8
LT1168IN8
LT1168IS8

S8 PART MARKING	
1168A	1168
1168AI	1168I

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

T_A = 25°C. V_S = ±15V, V_{CM} = 0V, R_L = 10k unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 6)	LT1168AC/LT1168AI MIN	TYP	MAX	LT1168C/LT1168I MIN	TYP	MAX	UNITS
G	Gain Range	G = 1 + (49.4k/R_G)	1		10k	1		10k	
	Gain Error	G = 1		0.008	0.02		0.015	0.03	%
		G = 10 (Note 7)		0.04	0.4		0.05	0.5	%
		G = 100 (Note 7)		0.04	0.5		0.05	0.6	%
		G = 1000 (Note 7)		0.08	0.5		0.08	0.6	%
	Gain Nonlinearity (Notes 7, 8)	V_O = ±10V, G = 1		2	6		3	10	ppm
		V_O = ±10V,G = 10 and 100		10	20		15	25	ppm
		V_O = ±10V, G = 1000		20	40		25	60	ppm
		V_O = ±10V, G = 1, R_L = 2k		4	15		5	20	ppm
		V_O = ±10V,G = 10 and 100, R_L = 2k		20	40		30	60	ppm
		V_O = ±10V, G = 1000, R_L = 2k		40	75		50	90	ppm
V_{OST}	Total Input Referred Offset Voltage	$V_{OST} = V_{OSI} + V_{OSO}/G$							
V_{OSI}	Input Offset Voltage	G = 1000, V_S = ±5V to ±15V		15	40		20	60	µV
V_{OSO}	Output Offset Voltage	G = 1, V_S = ±5V to ±15V		40	200		50	300	µV
I_{OS}	Input Offset Current			50	300		60	450	pA
I_B	Input Bias Current			40	250		80	500	pA
e_n	Input Noise Voltage, RTI	0.1Hz to 10Hz, G = 1		2.00			2.00		μV_{P-P}
		0.1Hz to 10Hz, G = 1000		0.28			0.28		μV_{P-P}
	Input Noise Voltage Density, RTI	f_O = 1kHz		10	15		10	15	nV/√Hz
	Output Noise Voltage Density, RTI	f_O = 1kHz (Note 9)		165	220		165	220	nV/√Hz
i_n	Input Noise Current	f_O = 0.1Hz to 10Hz		5			5		pA_{P-P}
	Input Noise Current Density	f_O = 10Hz		74			74		fA/√Hz
R_{IN}	Input Resistance	V_{IN} = ±10V	300	1250		200	1250		GΩ

ELECTRICAL CHARACTERISTICS

T_A = 25°C. V_S = ±15V, V_{CM} = 0V, R_L = 10k unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 6)	LT1168AC/LT1168AI MIN	LT1168AC/LT1168AI TYP	LT1168AC/LT1168AI MAX	LT1168C/LT1168I MIN	LT1168C/LT1168I TYP	LT1168C/LT1168I MAX	UNITS
$C_{IN(DIFF)}$	Differential Input Capacitance	f_O = 100kHz		1.6			1.6		pF
$C_{IN(CM)}$	Common Mode Input Capacitance	f_O = 100kHz		1.6			1.6		pF
V_{CM}	Input Voltage Range	G = 1, Other Input Grounded							
		V_S = ±2.3V to ±5V	$-V_S$ + 1.9		$+V_S$ – 1.2	$-V_S$ + 1.9		$+V_S$ – 1.2	V
		V_S = ±5V to ±18V	$-V_S$ + 1.9		$+V_S$ – 1.4	$-V_S$ + 1.9		$+V_S$ – 1.4	V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, V_{CM} = 0V to ±10V							
		G = 1	90	95		85	95		dB
		G = 10	106	115		100	115		dB
		G = 100	120	135		110	135		dB
		G = 1000	126	140		120	140		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.3V to ±18V							
		G = 1	103	108		100	108		dB
		G = 10	122	128		118	128		dB
		G = 100	131	145		126	145		dB
		G = 1000	135	150		130	150		dB
I_S	Supply Current	V_S = ±2.3V to ±18V		350	530		350	530	µA
V_{OUT}	Output Voltage Swing	R_L = 10k							
		V_S = ±2.3V to ±5V	$-V_S$ + 1.1		$+V_S$ – 1.2	$-V_S$ + 1.1		$+V_S$ – 1.2	V
		V_S = ±5V to ±18V	$-V_S$ + 1.2		$+V_S$ – 1.3	$-V_S$ + 1.2		$+V_S$ – 1.3	V
I_{OUT}	Output Current		20	32		20	32		mA
BW	Bandwidth	G = 1		400			400		kHz
		G = 10		200			200		kHz
		G = 100		13			13		kHz
		G = 1000		1			1		kHz
SR	Slew Rate	G = 1, V_{OUT} = ±10V	0.3	0.5		0.3	0.5		V/µs
	Settling Time to 0.01%	10V Step							
		G = 1 to 100		30			30		µs
		G = 1000		200			200		µs
REFIN	Reference Input Resistance			60			60		kΩ
I_{REFIN}	Reference Input Current	V_{REF} = 0V		18			18		µA
V_{REF}	Reference Voltage Range		$-V_S$ + 1.6		$+V_S$ – 1.6	$-V_S$ + 1.6		$+V_S$ – 1.6	V
A_{VREF}	Reference Gain to Output			1 ± 0.0001			1 ± 0.0001		

The ● denotes the specifications which apply over the 0°C ≤ T_A ≤ 70°C temperature range. V_S = ±15V, V_{CM} = 0V, R_L = 10k unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 6)		LT1168AC MIN	LT1168AC TYP	LT1168AC MAX	LT1168C MIN	LT1168C TYP	LT1168C MAX	UNITS
	Gain Error	G = 1	●		0.01	0.03		0.012	0.04	%
		G = 10 (Note 7)	●		0.40	1.5		0.500	1.6	%
		G = 100 (Note 7)	●		0.45	1.6		0.550	1.7	%
		G = 1000 (Note 7)	●		0.50	1.7		0.600	1.8	%
	Gain Nonlinearity (Notes 7, 8)	V_{OUT} = ±10V, G = 1	●		2	15		3	20	ppm
		V_{OUT} = ±10V, G = 10 and 100	●		7	30		10	35	ppm
		V_{OUT} = ±10V, G = 1000	●		25	60		30	80	ppm
ΔG/ΔT	Gain vs Temperature	G < 1000 (Note 7)	●		100	200		100	200	ppm/°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the 0°C ≤ T_A ≤ 70°C temperature range. V_S = ±15V, V_{CM} = 0V, R_L = 10k unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 6)		LT1168AC MIN	LT1168AC TYP	LT1168AC MAX	LT1168C MIN	LT1168C TYP	LT1168C MAX	UNITS
V_{OST}	Total Input Referred Offset Voltage	$V_{OST} = V_{OSI} + V_{OSO}/G$								
V_{OSI}	Input Offset Voltage	V_S = ±5V to ±15V	●		18	60		23	80	µV
V_{OSIH}	Input Offset Voltage Hysteresis	(Notes 7, 10)	●		3.0			3.0		µV
V_{OSO}	Output Offset Voltage	V_S = ±5V to ±15V	●		60	380		70	500	µV
V_{OSOH}	Output Offset Voltage Hysteresis	(Notes 7, 10)	●		30			30		µV
V_{OSI}/T	Input Offset Drift (RTI)	(Note 9)	●		0.05	0.3		0.06	0.4	µV/°C
V_{OSO}/T	Output Offset Drift	(Note 9)	●		0.7	3		0.8	4	µV/°C
I_{OS}	Input Offset Current		●		100	400		120	550	pA
I_{OS}/T	Input Offset Current Drift		●		0.3			0.4		pA/°C
I_B	Input Bias Current		●		65	350		105	600	pA
I_B/T	Input Bias Current Drift		●		1.4			1.4		pA/°C
V_{CM}	Input Voltage Range	G = 1, Other Input Grounded								
		V_S = ±2.3V to ±5V	●	$-V_S$ + 2.1		$+V_S$ – 1.3	$-V_S$ + 2.1		$+V_S$ – 1.3	V
		V_S = ±5V to ±18V	●	$-V_S$ + 2.1		$+V_S$ – 1.4	$-V_S$ + 2.1		$+V_S$ – 1.4	V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, V_{CM} = 0V to ±10V								
		G = 1	●	88	92		83	92		dB
		G = 10	●	100	110		97	110		dB
		G = 100	●	115	120		113	120		dB
		G = 1000	●	117	135		114	135		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.3V to ±18V								
		G = 1	●	102	115		98	115		dB
		G = 10	●	123	130		118	130		dB
		G = 100	●	127	135		124	135		dB
		G = 1000	●	129	145		126	145		dB
I_S	Supply Current	V_S = ±2.3V to ±18V	●		390	615		390	615	µA
V_{OUT}	Output Voltage Swing	R_L = 10k								
		V_S = ±2.3V to ±5V	●	$-V_S$ + 1.4		$+V_S$ – 1.3	$-V_S$ + 1.4		$+V_S$ – 1.3	V
		V_S = ±5V to ±18V	●	$-V_S$ + 1.6		$+V_S$ – 1.5	$-V_S$ + 1.6		$+V_S$ – 1.5	V
I_{OUT}	Output Current		●	16	25		16	25		mA
SR	Slew Rate	G = 1, V_{OUT} = ±10V	●	0.25	0.48		0.25	0.48		V/µs
V_{REF}	Voltage Range	(Note 9)	●	$-V_S$ + 1.6		$+V_S$ – 1.6	$-V_S$ + 1.6		$+V_S$ – 1.6	V

The ● denotes the specifications which apply over the –40°C ≤ T_A ≤ 85°C temperature range. V_S = ±15V, V_{CM} = 0V, R_L = 10k unless otherwise noted. (Note 8)

SYMBOL	PARAMETER	CONDITIONS (Note 6)		LT1168AI MIN	LT1168AI TYP	LT1168AI MAX	LT1168I MIN	LT1168I TYP	LT1168I MAX	UNITS
	Gain Error	G = 1	●		0.014	0.04		0.015	0.05	%
		G = 10 (Note 7)	●		0.600	1.9		0.700	2.0	%
		G = 100 (Note 7)	●		0.600	2.0		0.700	2.1	%
		G = 1000 (Note 7)	●		0.600	2.1		0.700	2.2	%
G_N	Gain Nonlinearity (Notes 7, 8)	V_O = ±10V, G = 1	●		3	20		5	25	ppm
		V_O = ±10V, G = 10 and 100	●		10	35		15	40	ppm
		VO = ±10V, G = 1000	●		30	70		35	100	ppm
ΔG/ΔT	Gain vs Temperature	G < 1000 (Note 7)	●		100	200		100	200	ppm/°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C ≤ T_A ≤ 85°C temperature range. V_S = ±15V, V_{CM} = 0V, R_L = 10k unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS (Note 6)		LT1168AI MIN	LT1168AI TYP	LT1168AI MAX	LT1168I MIN	LT1168I TYP	LT1168I MAX	UNITS
V_{OST}	Total Input Referred Offset Voltage	$V_{OST} = V_{OSI} + V_{OSO}/G$								
V_{OSI}	Input Offset Voltage		●		20	75		25	100	µV
V_{OSIH}	Input Offset Voltage Hysteresis	(Notes 7, 10)	●		3.0			3.0		µV
V_{OSO}	Output Offset Voltage		●		180	500		200	600	µV
V_{OSOH}	Output Offset Voltage Hysteresis	(Notes 7, 10)	●		30			30		µV
V_{OSI}/T	Input Offset Drift (RTI)	(Note 9)	●		0.05	0.3		0.06	0.4	µV/°C
V_{OSO}/T	Output Offset Drift	(Note 9)	●		0.8	5		1	6	µV/°C
I_{OS}	Input Offset Current		●		110	550		120	700	pA
I_{OS}/T	Input Offset Current Drift		●		0.3			0.3		pA/°C
I_B	Input Bias Current		●		120	500		220	800	pA
I_B/T	Input Bias Current Drift		●		1.4			1.4		pA/°C
V_{CM}	Input Voltage Range	V_S = ±2.3V to ±5V V_S = ±5V to ±18V	● ●	$-V_S + 2.1$ $-V_S + 2.1$		$+V_S - 1.3$ $+V_S - 1.4$	$-V_S + 2.1$ $-V_S + 2.1$		$+V_S - 1.3$ $+V_S - 1.4$	V V
CMRR	Common Mode Rejection Ratio	1k Source Imbalance, V_{CM} = 0V to ±10V								
		G = 1	●	86	90		81	90		dB
		G = 10	●	98	105		95	105		dB
		G = 100	●	114	118		112	118		dB
		G = 1000	●	116	133		112	133		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.3V to ±18V								
		G = 1	●	100	112		95	112		dB
		G = 10	●	120	125		115	125		dB
		G = 100	●	125	132		120	132		dB
		G = 1000	●	128	140		125	140		dB
I_S	Supply Current		●		420	650		420	650	µA
V_{OUT}	Output Voltage Swing	V_S = ±2.3V to ±5V V_S = ±5V to ±18V	● ●	$-V_S + 1.4$ $-V_S + 1.6$		$+V_S - 1.3$ $+V_S - 1.5$	$-V_S + 1.4$ $-V_S + 1.6$		$+V_S - 1.3$ $+V_S - 1.5$	V V
I_{OUT}	Output Current		●	15	22		15	22		mA
SR	Slew Rate		●	0.22	0.41		0.22	0.42		V/µs
V_{REF}	Voltage Range	(Note 9)	●	$-V_S + 1.6$		$+V_S - 1.6$	$-V_S + 1.6$		$+V_S - 1.6$	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: If the input voltage exceeds the supplies, the input current should be limited to less than 20mA.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum.

Note 4: The LT1168AC/LT1168C are guaranteed functional over the operating temperature range of –40°C and 85°C.

Note 5: The LT1168AC/LT1168C are guaranteed to meet specified performance from 0°C to 70°C. The LT1168AC/LT1168C are designed, characterized and expected to meet specified performance from –40°C to 85°C but are not tested or QA sampled at these temperatures. The LT1168AI/LT1168I are guaranteed to meet specified performance from –40°C to 85°C.

Note 6: Typical parameters are defined as the 60% of the yield parameter distribution.

Note 7: Does not include the tolerance of the external gain resistor R_G.

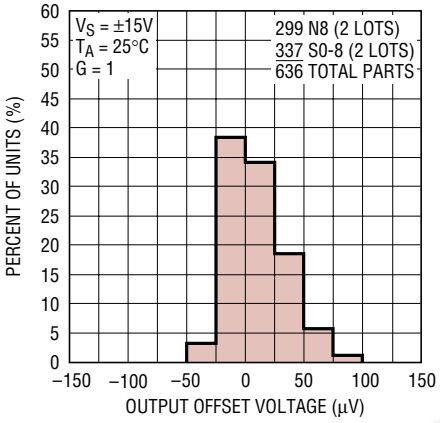
Note 8: This parameter is measured in a high speed automatic tester that does not measure the thermal effects with longer time constants. The magnitude of these thermal effects are dependent on the package used, heat sinking and air flow conditions.

Note 9: This parameter is not 100% tested.

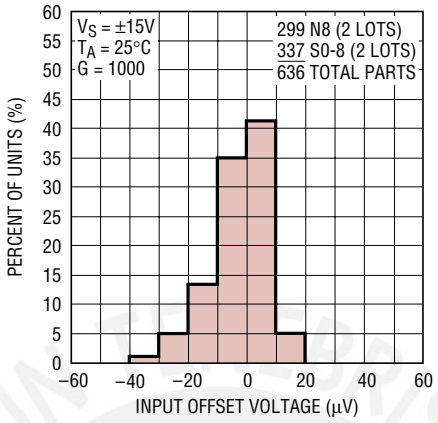
Note 10: Hysteresis in offset voltage is created by package stress that differs depending on whether the IC was previously at a higher or lower temperature. Offset voltage hysteresis is always measured at 25°C, but the IC is cycled to 85°C I-grade (or 70°C C-grade) or –40°C I-grade (0°C C-grade) before successive measurement. 60% of the parts will pass the typical limit on the data sheet.

TYPICAL PERFORMANCE CHARACTERISTICS

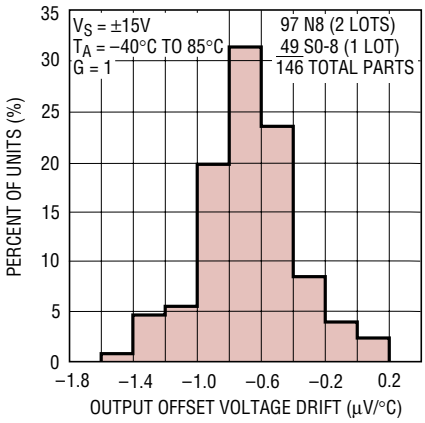
Distribution of Output Offset Voltage



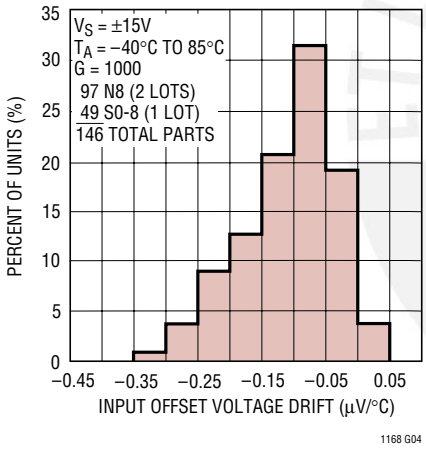
Distribution of Input Offset Voltage



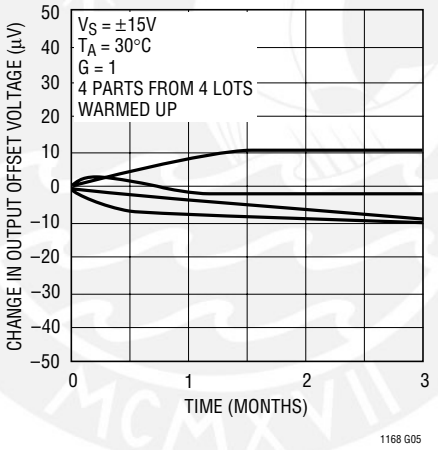
Distribution of Output Offset Voltage Drift



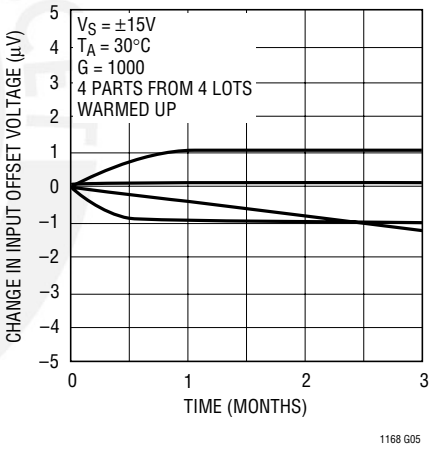
Distribution of Input Offset Voltage Drift



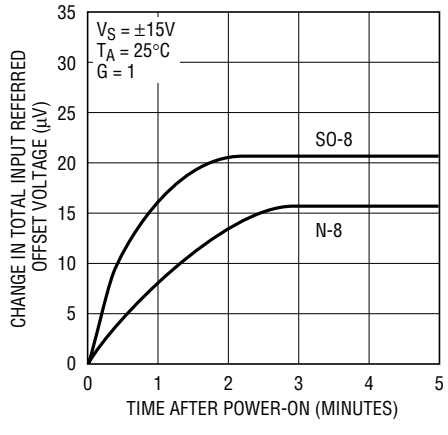
Output Offset Voltage Long-Term Drift



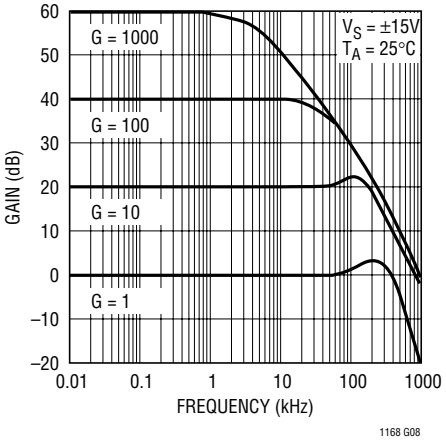
Input Offset Voltage Long-Term Drift



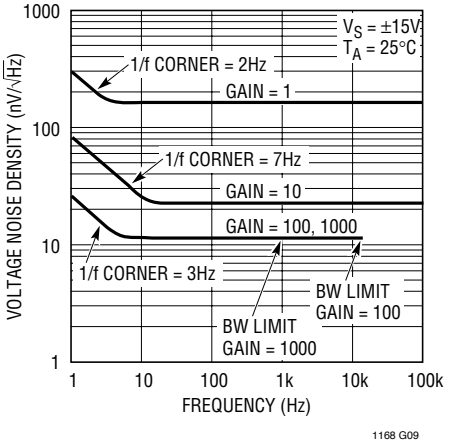
Warm-Up Drift



Gain vs Frequency

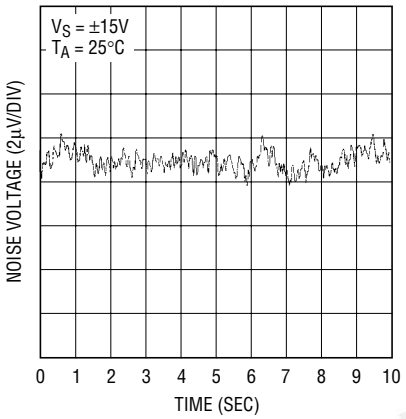


Voltage Noise Density vs Frequency

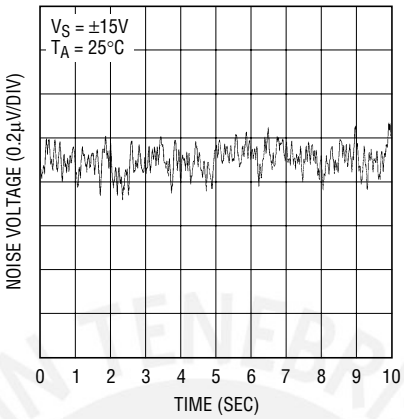


TYPICAL PERFORMANCE CHARACTERISTICS

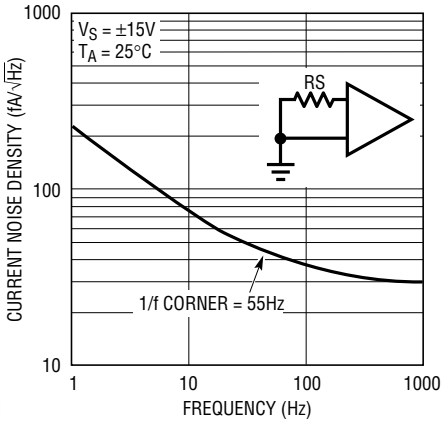
0.1Hz to 10Hz Noise Voltage, G = 1



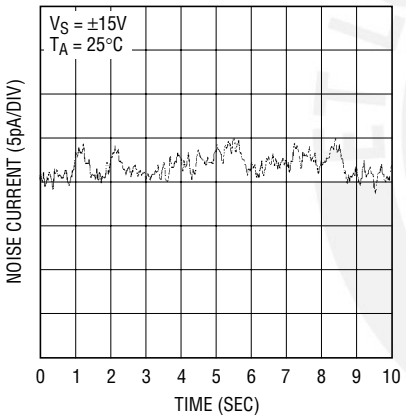
0.1Hz to 10Hz Noise Voltage, RTI G = 1000



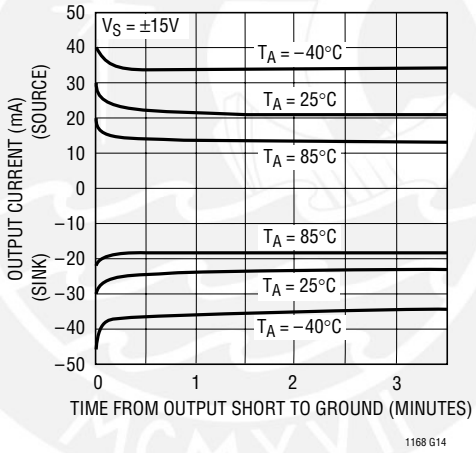
Current Noise Density vs Frequency



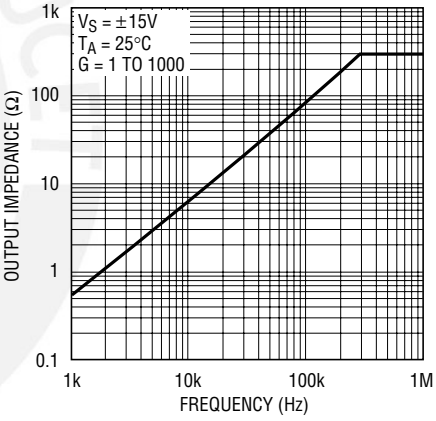
0.1Hz to 10Hz Current Noise



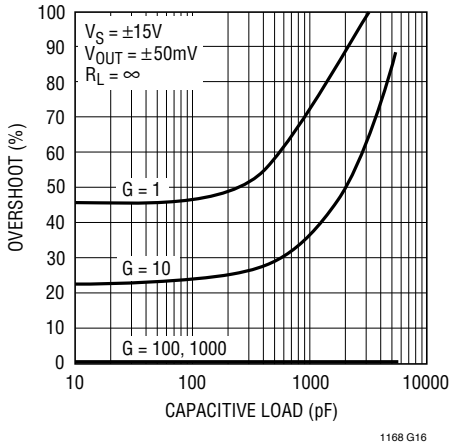
Short-Circuit Current vs Time



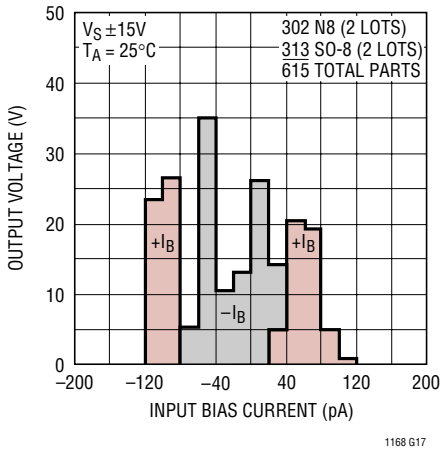
Output Impedance vs Frequency



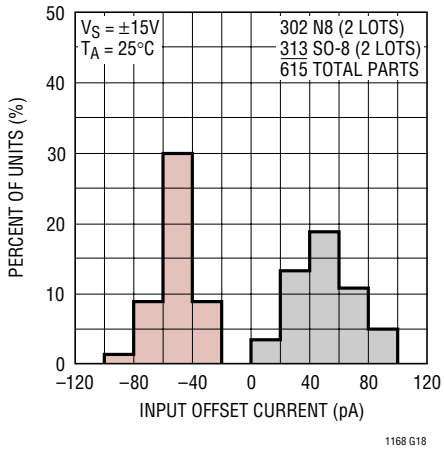
Overshoot vs Capacitive Load



Input Bias Current

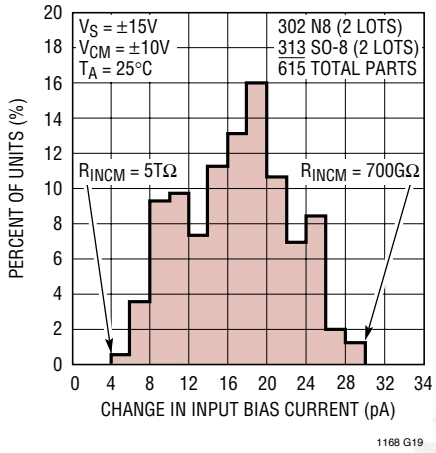


Input Offset Current

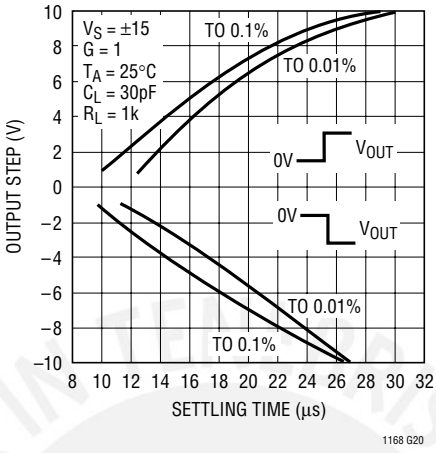


TYPICAL PERFORMANCE CHARACTERISTICS

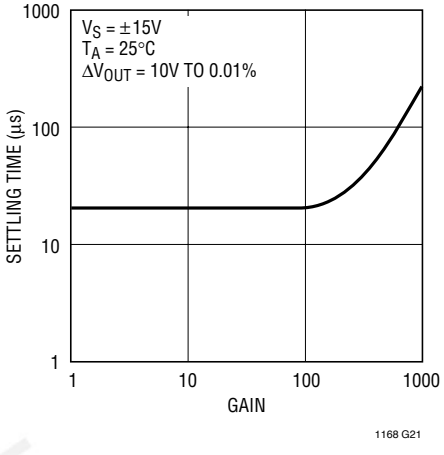
Change in Input Bias Current for V_{CM} = 20V



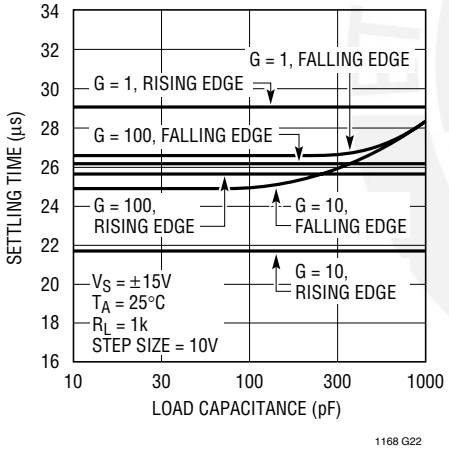
Settling Time vs Step Size



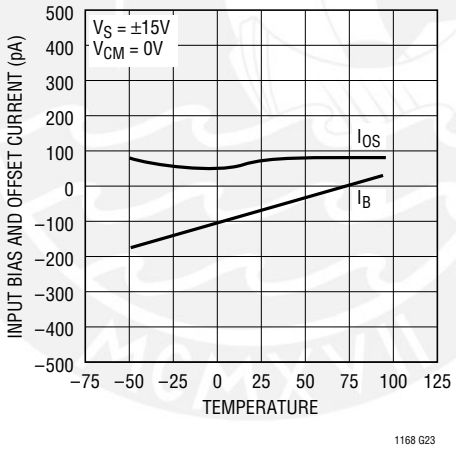
Settling Time vs Gain



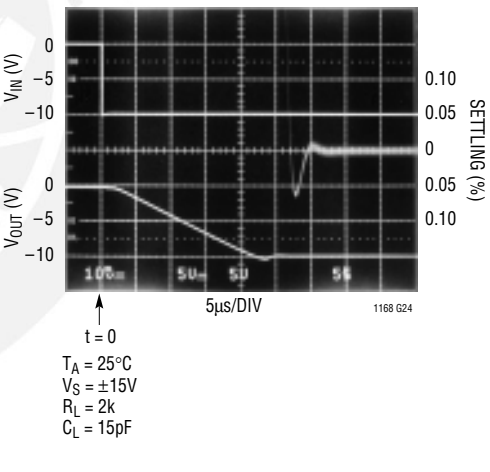
Settling Time (0.1%) vs Load Capacitance



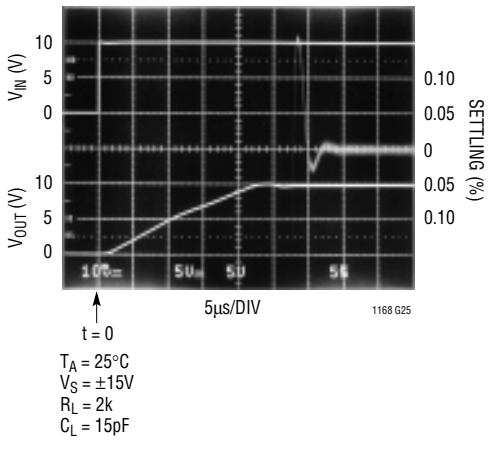
Input Bias and Offset Current vs Temperature



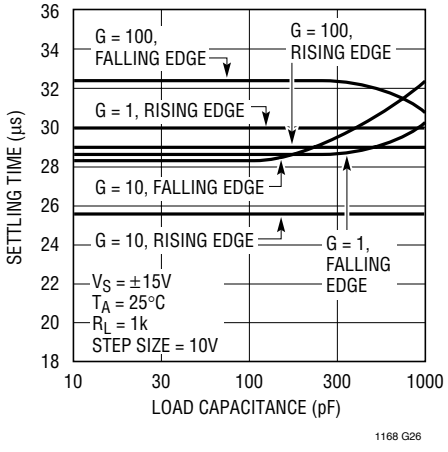
Falling Edge Settling Time (0.10%)



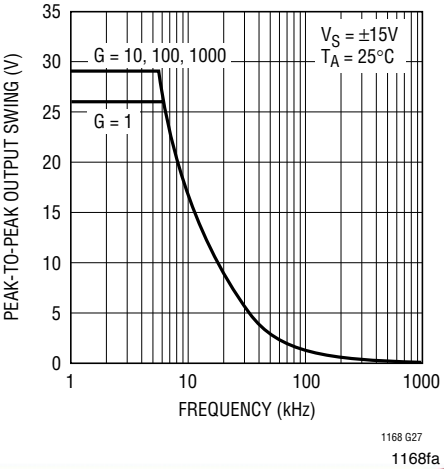
Rising Edge Settling Time (0.10%)



Settling Time (0.01%) vs Load Capacitance

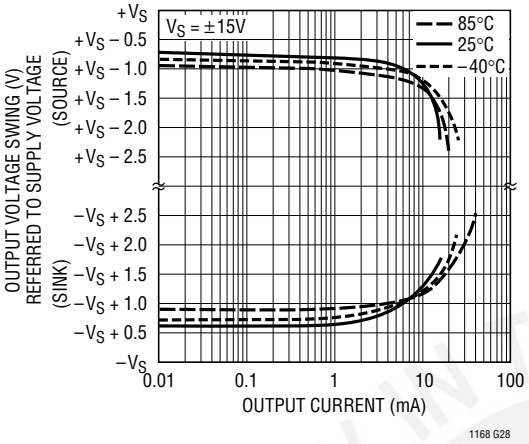


Undistorted Output Swing vs Frequency

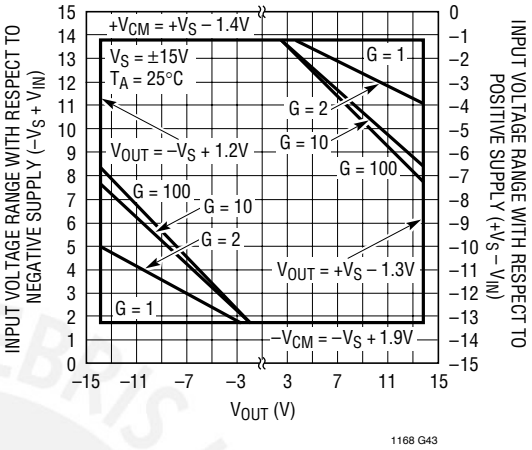


TYPICAL PERFORMANCE CHARACTERISTICS

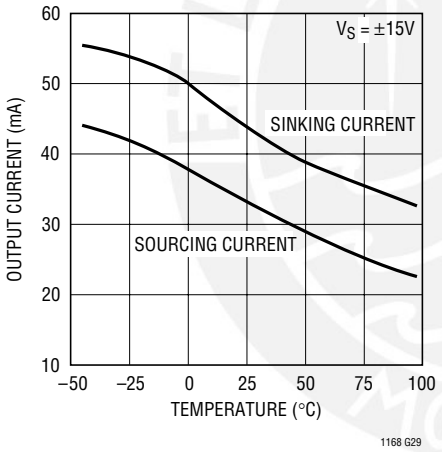
Output Voltage Swing vs Load Current



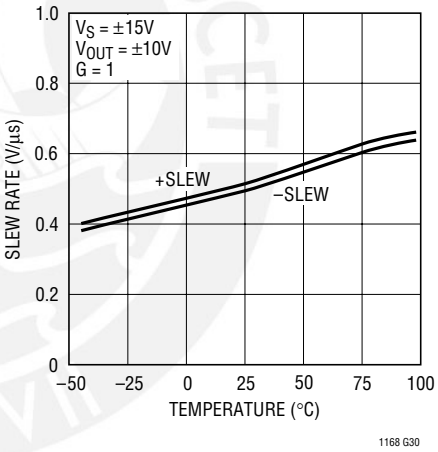
Input Voltage Range vs Output Voltage for Various Gains



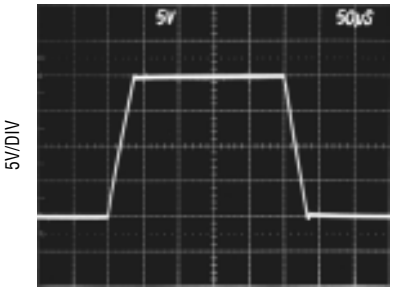
Output Short-Circuit Current vs Temperature



Slew Rate vs Temperature

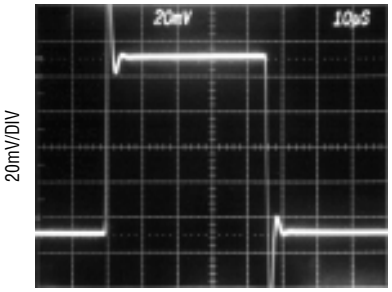


Large-Signal Transient Response



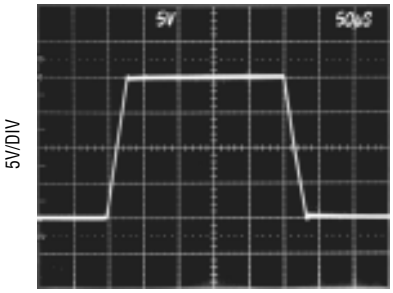
G = 1
V_S = ±15V
R_L = 2k
C_L = 60pF
50µs/DIV

Small-Signal Transient Response



G = 1
V_S = ±15V
R_L = 2k
C_L = 60pF
10µs/DIV

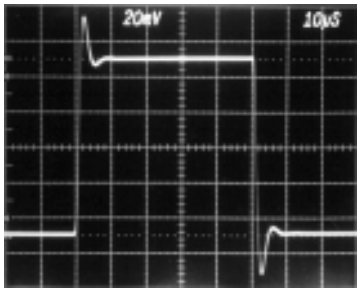
Large-Signal Transient Response



G = 10
V_S = ±15V
R_L = 2k
C_L = 60pF
50µs/DIV

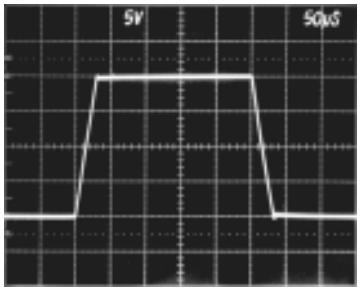
TYPICAL PERFORMANCE CHARACTERISTICS

Small-Signal Transient Response



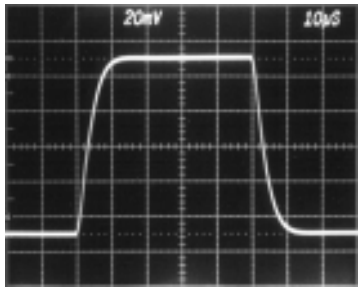
G = 10 10µs/DIV
V_S = ±15V
R_L = 2k
C_L = 60pF

Large-Signal Transient Response



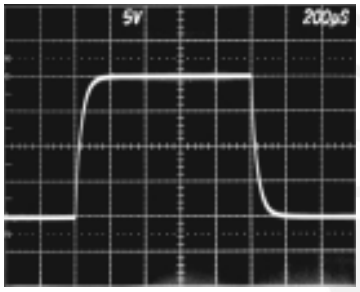
G = 100 50µs/DIV
V_S = ±15V
R_L = 2k
C_L = 60pF

Small-Signal Transient Response



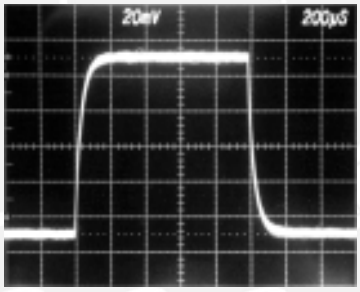
G = 100 10µs/DIV
V_S = ±15V
R_L = 2k
C_L = 60pF

Large-Signal Transient Response



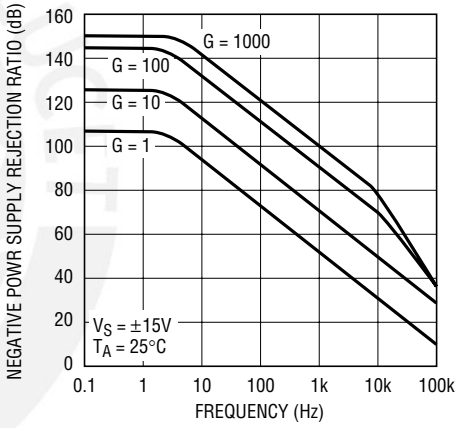
G = 1000 200µs/DIV
V_S = ±15V
R_L = 2k
C_L = 60pF

Small-Signal Transient Response

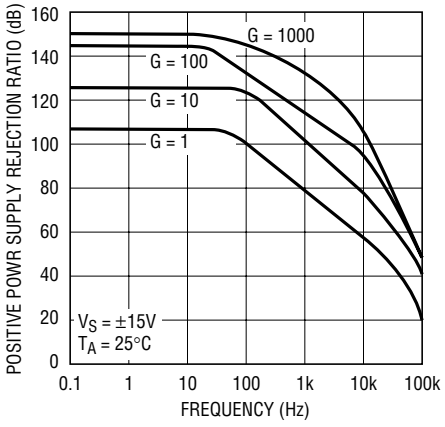


G = 1000 200µs/DIV
V_S = ±15V
R_L = 2k
C_L = 60pF

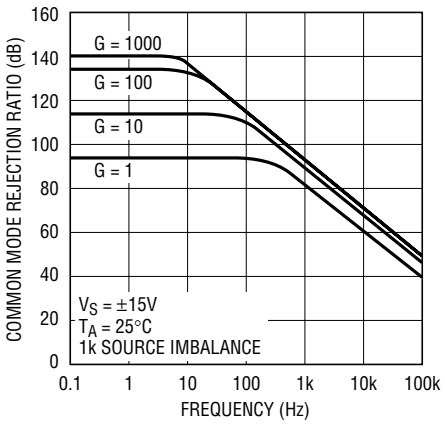
Negative Power Supply Rejection Ratio vs Frequency



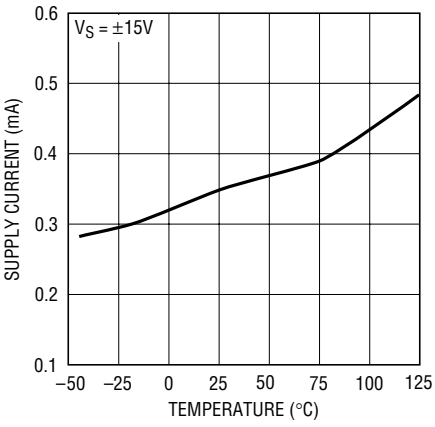
Positive Power Supply Rejection Ratio vs Frequency



Common Mode Rejection Ratio vs Frequency (1k Source Imbalance)



Supply Current vs Temperature



BLOCK DIAGRAM

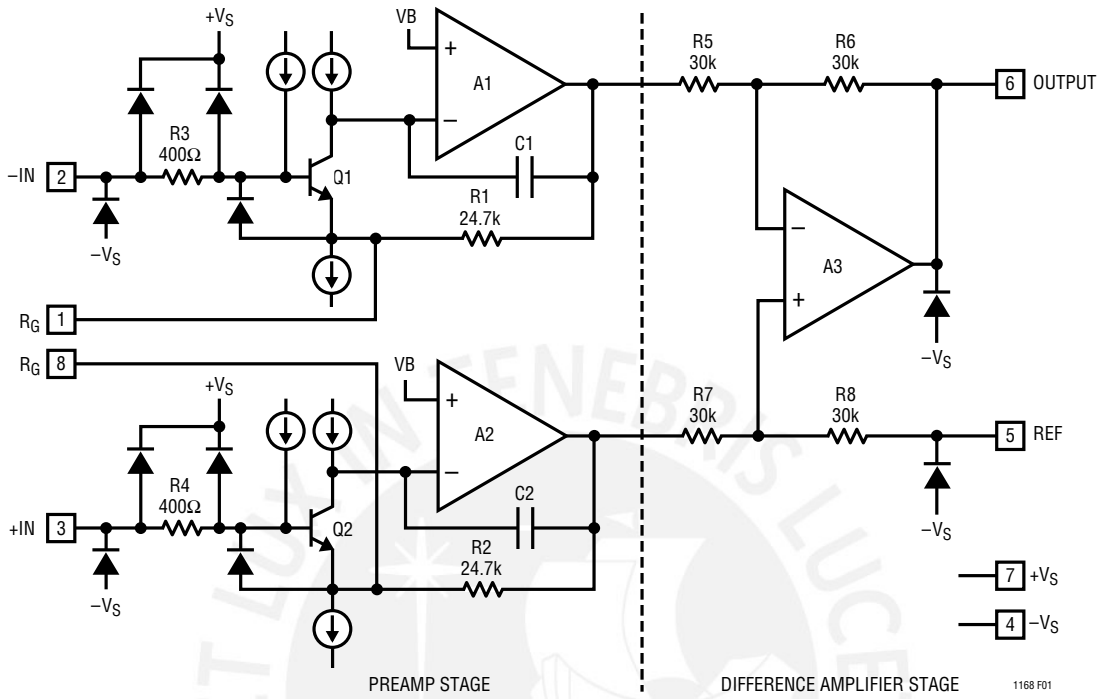


Figure 1. Block Diagram

THEORY OF OPERATION

The LT1168 is a modified version of the three op amp instrumentation amplifier. Laser trimming and monolithic construction allow tight matching and tracking of circuit parameters over the specified temperature range. Refer to the block diagram (Figure 1) to understand the following circuit description. The collector currents in Q1 and Q2 are trimmed to minimize offset voltage drift, thus assuring a high level of performance. R1 and R2 are trimmed to an absolute value of 24.7k to assure that the gain can be set accurately (0.6% at G = 100) with only one external resistor R_G. The value of R_G in parallel with R1 (R2) determines the transconductance of the preamp stage. As R_G is reduced for larger programmed gains, the transconductance of the input preamp stage increases to that of the input transistors Q1 and Q2. This increases the open-loop gain when the programmed gain is increased, reducing the input referred gain related errors and noise. The input voltage noise at gains greater than 50 is determined only by Q1 and Q2. At lower gains the noise of the difference amplifier and preamp gain setting resistors increase the noise. The gain bandwidth product is determined by C1, C2 and the preamp transconductance which increases with programmed gain. Therefore, the bandwidth does not drop proportionally with gain.

The input transistors Q1 and Q2 offer excellent matching, which is inherent in NPN bipolar transistors, as well as picoampere input bias current due to superbeta processing. The collector currents in Q1 and Q2 are held constant due to the feedback through the Q1-A1-R1 loop and Q2-A2-R2 loop which in turn impresses the differential input voltage across the external gain set resistor R_G. Since the current that flows through R_G also flows through R1 and R2, the ratios provide a gained-up differential

THEORY OF OPERATION

voltage, G = (R1 + R2)/R_G, to the unity-gain difference amplifier A3. The common mode voltage is removed by A3, resulting in a single-ended output voltage referenced to the voltage on the REF pin. The resulting gain equation is:

$$G = (49.4k\Omega/R_G) + 1$$

solving for the gain set resistor gives:

$$R_G = 49.4k\Omega/(G - 1)$$

Table 1 shows appropriate 1% resistor values for a variety of gains.

Table 1

DESIRED GAIN	R_G	CLOSEST 1% VALUE	RESULTANT GAIN
1	Open	Open	1
2	49400Ω	49900Ω	1.99
5	12350Ω	12400Ω	4.984
10	5488.89Ω	5490Ω	9.998
20	2600Ω	2610Ω	19.93
50	1008.16Ω	1000Ω	50.4
100	498.99Ω	499Ω	99.998
200	248.24Ω	249Ω	199.4
500	99Ω	100Ω	495
1000	49.95Ω	49.4Ω	1001

Input and Output Offset Voltage

The offset voltage of the LT1168 has two components: the output offset and the input offset. The total offset voltage referred to the input (RTI) is found by dividing the output offset by the programmed gain (G) and adding it to the input offset. At high gains the input offset voltage dominates, whereas at low gains the output offset voltage dominates. The total offset voltage is:

Total input offset voltage (RTI)
= input offset + (output offset/G)

Total output offset voltage (RTO)
= (input offset • G) + output offset

Reference Terminal

The reference terminal is one end of one of the four 30k resistors around the difference amplifier. The output voltage of the LT1168 (Pin 6) is referenced to the voltage on the reference terminal (Pin 5). Resistance in series with the REF pin must be minimized for best common mode rejection. For example, a 6Ω resistance from the REF pin to ground will not only increase the gain error by 0.02% but will lower the CMRR to 80dB.

Input Voltage Range

The input voltage range for the LT1168 is specified in the data sheet at 1.4V below the positive supply to 1.9V above the negative supply for a gain of one. As the gain increases the input voltage range decreases. This is due to the IR drop across the internal gain resistors R1 and R2 in Figure 1. For the unity gain condition there is no IR drop across the gain resistors R1 and R2, the output of the GM amplifiers is just the differential input voltage at Pin 2 and Pin 3 (level shifted by one V_{BE} from Q1 and Q2). When a gain resistor is connected across Pins 1 and 8, the output swing of the GM cells is now the differential input voltage (level shifted by V_{BE}) plus the differential voltage times the gain (ratio of the internal gain resistors to the external gain resistor across Pins 1 and 8). To calculate how close to the positive rail the input (V_{IN}) can swing for a gain of 2 and a maximum expected output swing of 10V, use the following equation:

$$+V_S - V_{IN} = -0.5 - (V_{OUT}/G) \bullet (G - 1)/2$$

Substituting yields:

$$-0.5 - (10/2) \bullet (1/2) = -3V$$

below the positive supply or 12V for a 15V supply. To calculate how far above the negative supply the input can swing for a gain of 10 with a maximum expected output swing of –10V, the equation for the negative case is:

$$-V_S + V_{IN} = 1.5 - (V_{OUT}/G) \bullet (G - 1)/2$$

Substituting yields:

$$1.5 - (-10/10) \bullet 9/2 = 6V$$

above the negative supply or –9V for a negative supply voltage of –15V. Figures 2 and 3 are for the positive common mode and negative common mode cases respectively.

THEORY OF OPERATION

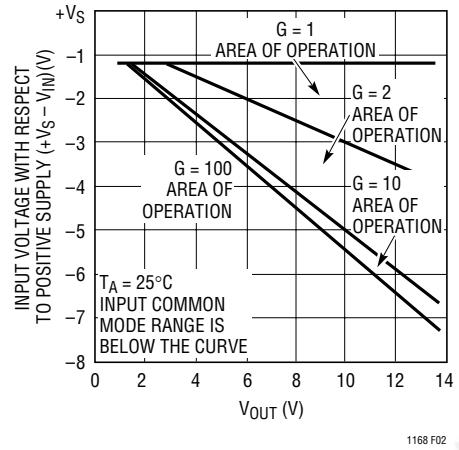


Figure 2. Positive Input Range vs Output Voltage for Different Gains

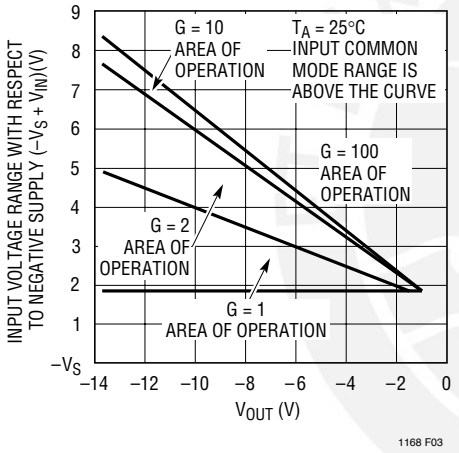


Figure 3. Negative Input Voltage Range vs Output Voltage for Various Gains

Single Supply Operation

For best results under single supply operation, the REF pin should be raised above the negative supply (Pin 4) and one of the inputs should be at least 2.5V above ground. The barometer application later in this data sheet is an example that satisfies these conditions. The resistance R_{SET} from the bridge transducer to ground sets the operating current for the bridge, and with R6, also has the effect of raising the input common mode voltage. The output of the LT1168 is always inside the specified range since the barometric pressure rarely goes low enough to cause the output to clip (30.00 inches of Hg corresponds to 3.000V). For applications that require the output to swing at or below the REF potential, the voltage on the REF pin can be further level shifted. The application in the front of this data sheet, Single Supply Pressure Monitor, is an example. An op amp is used to buffer the voltage on the REF pin since a parasitic series resistance will degrade the CMRR.

Output Offset Trimming

The LT1168 is laser trimmed for low offset voltage so that no external offset trimming is required for most applications. In the event that the offset needs to be adjusted, the circuit in Figure 4 is an example of an optional offset adjust circuit. The op amp buffer provides a low impedance to the REF pin where resistance must be kept to minimum for best CMRR and lowest gain error.

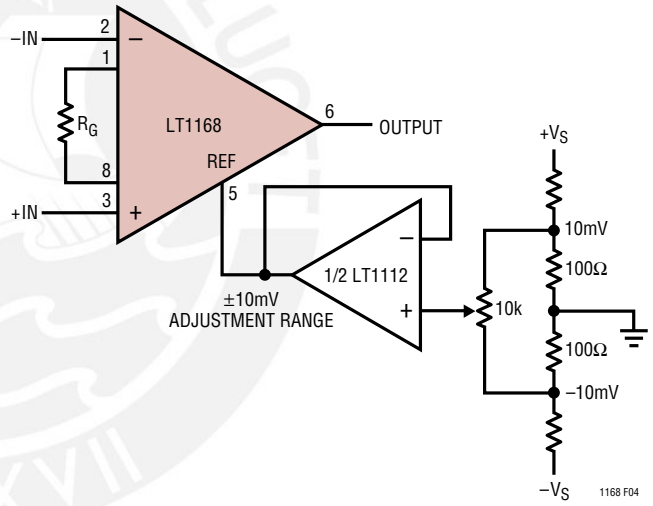


Figure 4. Optional Trimming of Output Offset Voltage

Input Bias Current Return Path

The low input bias current of the LT1168 (250pA) and the high input impedance (200GΩ) allow the use of high impedance sources without introducing additional offset voltage errors, even when the full common mode range is required. However, a path must be provided for the input bias currents of both inputs when a purely differential signal is being amplified. Without this path the inputs will float to either rail and exceed the input common mode range of the LT1168, resulting in a saturated input stage. Figure 5 shows three examples of an input bias current

THEORY OF OPERATION

path. The first example is of a purely differential signal source with a 10kΩ input current path to ground. Since the impedance of the signal source is low, only one resistor is needed. Two matching resistors are needed for higher impedance signal sources as shown in the second example. Balancing the input impedance improves both common mode rejection and DC offset.

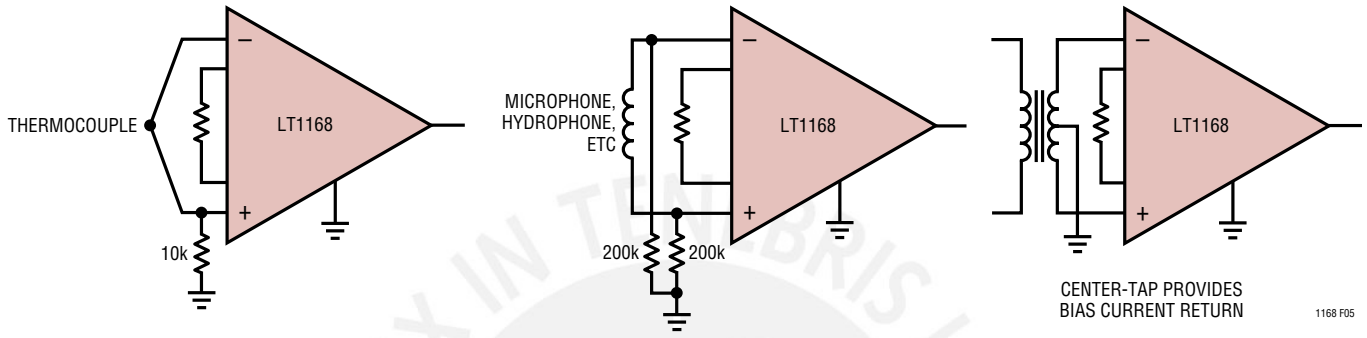


Figure 5. Providing an Input Common Mode Current Path

APPLICATIONS INFORMATION

The LT1168 is a low power precision instrumentation amplifier that requires only one external resistor to accurately set the gain anywhere from 1 to 1000. The LT1168 is trimmed for critical DC parameters such as gain error (0.04%, G = 10), input offset voltage (40μV, RTI), CMRR (90dB min, G = 1) and PSRR (103dB min, G = 1). These trims allow the amplifier to achieve very high DC accuracy. The LT1168 achieves low input bias current of just 250pA (max) through the use of superbeta processing. The output can handle capacitive loads up to 1000pF in any gain configuration and the inputs are protected against ESD strikes up to ±13kV (human body).

Input Protection

The LT1168 can safely handle up to ±20mA of input current in an overload condition. Adding an external 5k input resistor in series with each input allows DC input fault voltage up to ±100V and improves the ESD immunity to ±8kV (contact) and ±15kV (air discharge), which is the IEC 1000-4-2 level 4 specification. If lower value input resistors must be used, a clamp diode from the positive supply to each input will maintain the IEC 1000-4-2 specification to level 4 for both air and contact discharge. A 2N4393 drain/source to gate is a good low leakage diode for use with resistors between 1k and 20k, see Figure 6. The input resistors should be carbon and not metal film or carbon film in order to withstand the fault conditions.

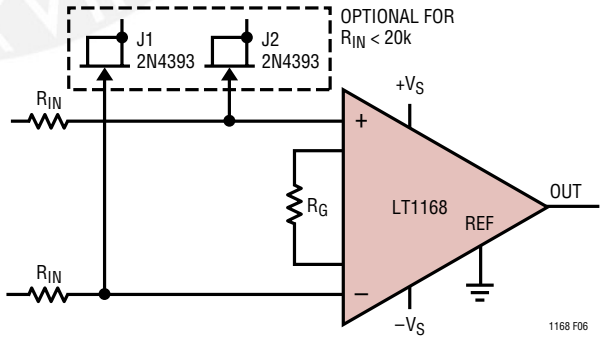


Figure 6. Input Protection

RFI Reduction

In many industrial and data acquisition applications, instrumentation amplifiers are used to accurately amplify small signals in the presence of large common mode

APPLICATIONS INFORMATION

voltages or high levels of noise. Typically, the sources of these very small signals (on the order of microvolts or millivolts) are sensors that can be a significant distance from the signal conditioning circuit. Although these sensors may be connected to signal conditioning circuitry, using shielded or unshielded twisted-pair cabling, the cabling may act as antennae, conveying very high frequency interference directly into the input stage of the LT1168.

The amplitude and frequency of the interference can have an adverse effect on an instrumentation amplifier's input stage by causing an unwanted DC shift in the amplifier's input offset voltage. This well known effect is called RFI rectification and is produced when out-of-band interference is coupled (inductively, capacitively or via radiation) and rectified by the instrumentation amplifier's input transistors. These transistors act as high frequency signal detectors, in the same way diodes were used as RF envelope detectors in early radio designs. Regardless of the type of interference or the method by which it is coupled into the circuit, an out-of-band error signal appears in series with the instrumentation amplifier's inputs.

To significantly reduce the effect of these out-of-band signals on the input offset voltage of instrumentation amplifiers, simple lowpass filters can be used at the inputs. This filter should be located very close to the input pins of the circuit. An effective filter configuration is illustrated in Figure 7, where three capacitors have been added to the inputs of the LT1168. Capacitors C_{XCM1} and C_{XCM2} form lowpass filters with the external series resistors $R_{S1,2}$ to any out-of-band signal appearing on each of the input traces. Capacitor C_{XD} forms a filter to reduce any unwanted signal that would appear across the input traces. An added benefit to using C_{XD} is that the circuit's AC common mode rejection is not degraded due to common mode capacitive imbalance. The differential mode and common mode time constants associated with the capacitors are:

$$t_{DM(LPF)} = (R_{S1} + R_{S2})(C_{XD} + C_{XCM1} + C_{XCM2})$$

$$t_{CM(LPF)} = (R_{S1} \| R_{S2})(C_{XCM1} + C_{XCM2})$$

Setting the time constants requires a knowledge of the frequency, or frequencies of the interference. Once this frequency is known, the common mode time constants can be set followed by the differential mode time constant. To avoid any possibility of inadvertently affecting the signal to be processed, set the common mode time constant an order of magnitude (or more) smaller than the differential mode time constant. Set the common mode time constants such that they do not degrade the LT1168 inherent AC CMR. Then the differential mode time constant can be set for the bandwidth required for the application. Setting the differential mode time constant close to the sensor's BW also minimizes any noise pickup along the leads. To avoid any possibility of common mode to differential mode signal conversion, match the common mode time constants to 1% or better. If the sensor is an RTD or a resistive strain gauge and is in proximity to the instrumentation amplifier, then the series resistors $R_{S1,2}$ can be omitted.

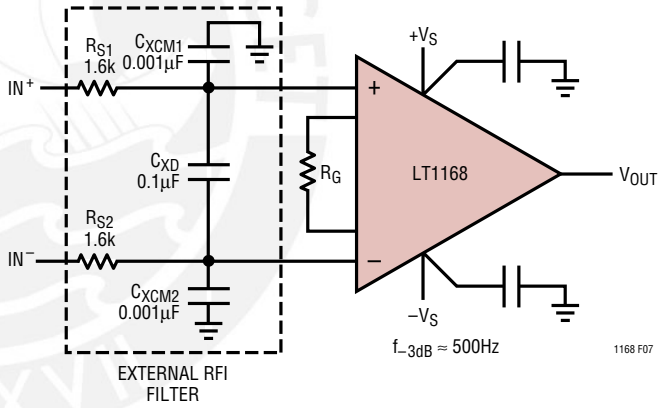


Figure 7. Adding a Simple RC Filter at the Inputs to an Instrumentation Amplifier is Effective in Reducing Rectification of High Frequency Out-of-Band Signals

Nerve Impulse Amplifier

The LT1168's low current noise makes it ideal for EMG monitors that have high source impedances. Demonstrating the LT1168's ability to amplify low level signals, the circuit in Figure 8 takes advantage of the amplifier's high gain and low noise operation. This circuit amplifies the low level nerve impulse signals received from a patient at Pins 2 and 3. R_G and the parallel combination of R3 and R4 set a gain of ten. The potential on LT1112's Pin 1 creates

APPLICATIONS INFORMATION

a ground for the common mode signal. C1 was chosen to maintain the stability of the patient ground. The LT1168's high CMRR ensures that the desired differential signal is amplified and unwanted common mode signals are attenuated. Since the DC portion of the signal is not important, R6 and C2 make up a 0.3Hz highpass filter. The AC signal at LT1112's Pin 5 is amplified by a gain of 101 set by R7/R8 +1. The parallel combination of C3 and R7 form a lowpass filter that decreases this gain at frequencies above 1kHz. The ability to operate at ±3V on 350µA of supply current makes the LT1168 ideal for battery-powered applications. Total supply current for this application is 1.05mA. Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

Low I_B Favors High Impedance Bridges, Lowers Dissipation

The LT1168's low supply current, low supply voltage operation and low input bias currents allow it to fit nicely into battery-powered applications. Low overall power dissipation necessitates using higher impedance bridges. The single supply pressure monitor application on the front of this data sheet, shows the LT1168 connected to the differential output of a 3.5k bridge. The picoampere input bias currents keep the error caused by offset current to a negligible level. The LT1112 level shifts the LT1168's reference pin and the ADC's analog ground pins above ground. The LT1168's and LT1112's combined power dissipation is still less than the bridge's. This circuit's total supply current is just 2.2mA.

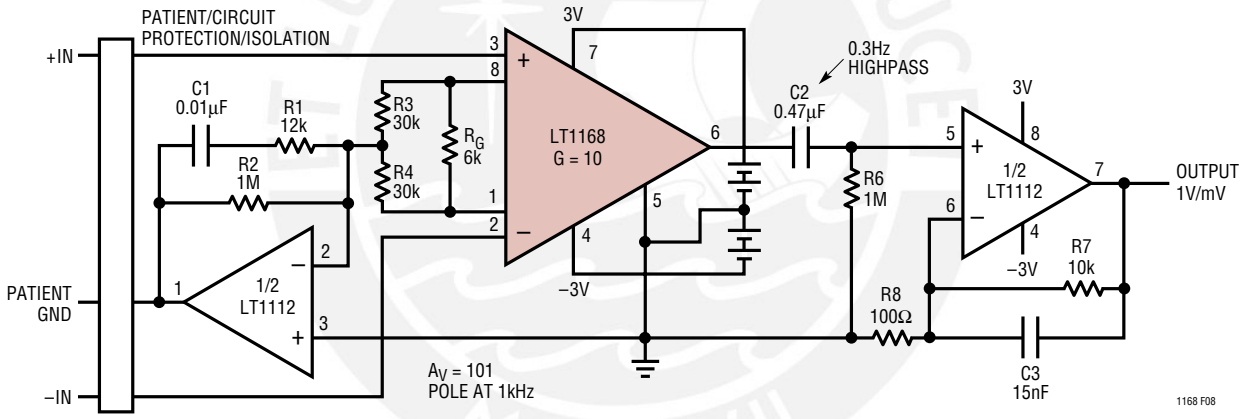


Figure 8. Nerve Impulse Amplifier

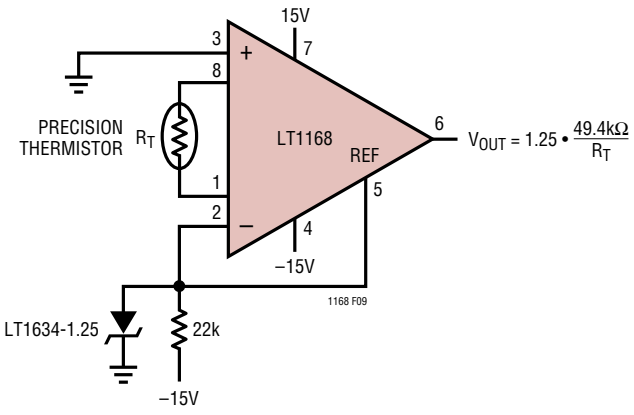


Figure 9. Precision Temperature Without Precision Resistors

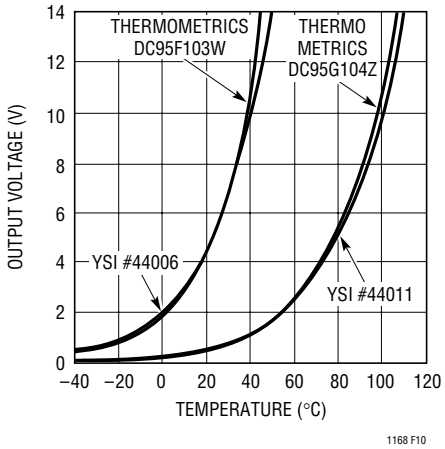
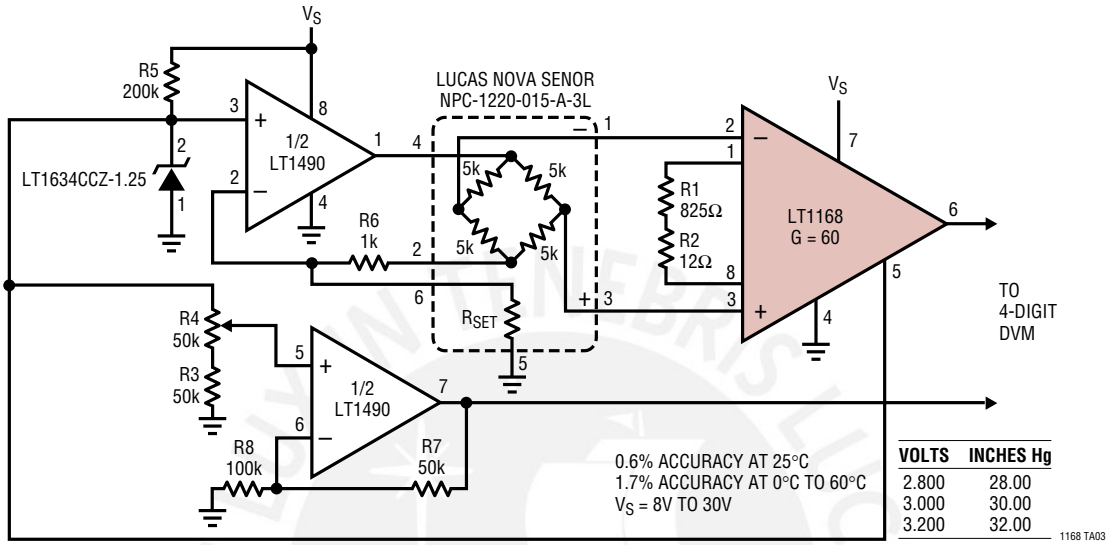


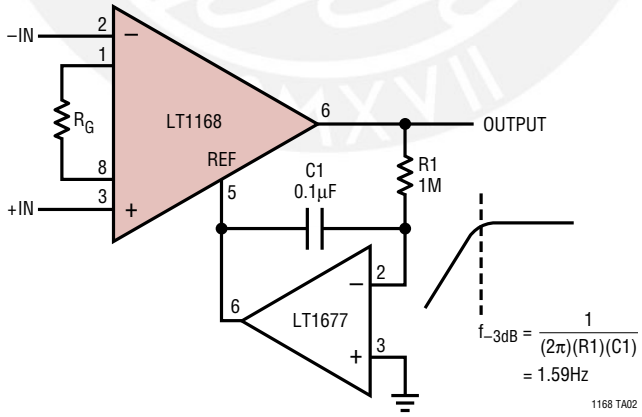
Figure 10. Response of Figure 9 for Various Thermistors

TYPICAL APPLICATIONS

Single Supply Barometer

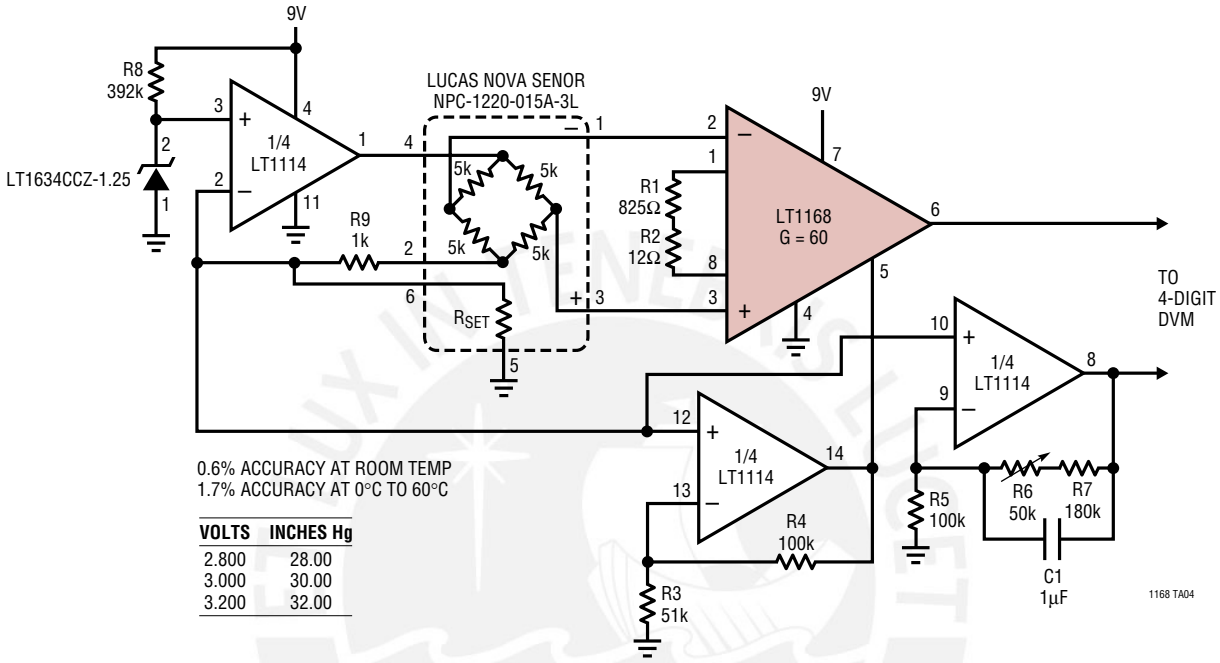


AC Coupled Instrumentation Amplifier



TYPICAL APPLICATIONS

4-Digit Pressure Sensor



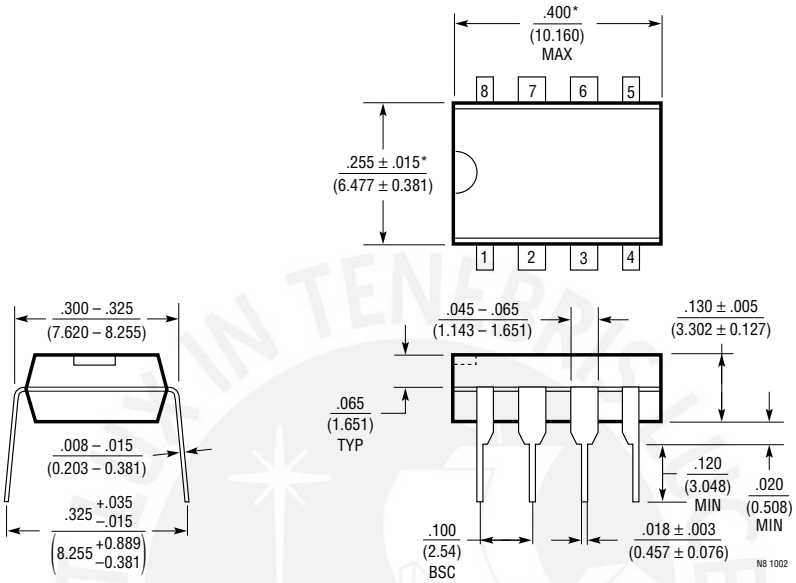
0.6% ACCURACY AT ROOM TEMP
1.7% ACCURACY AT 0°C TO 60°C

VOLTS	INCHES Hg
2.800	28.00
3.000	30.00
3.200	32.00

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

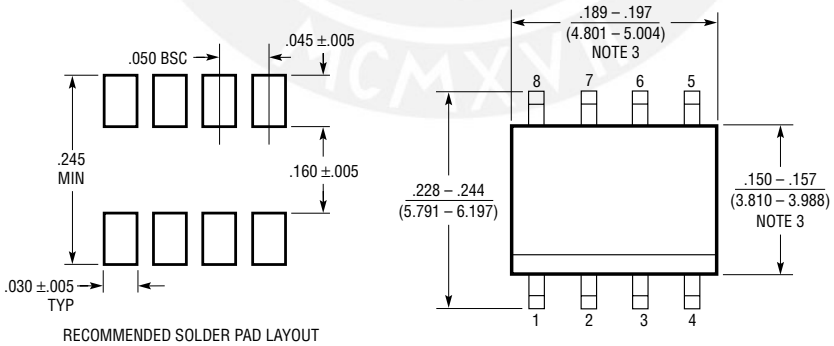
N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

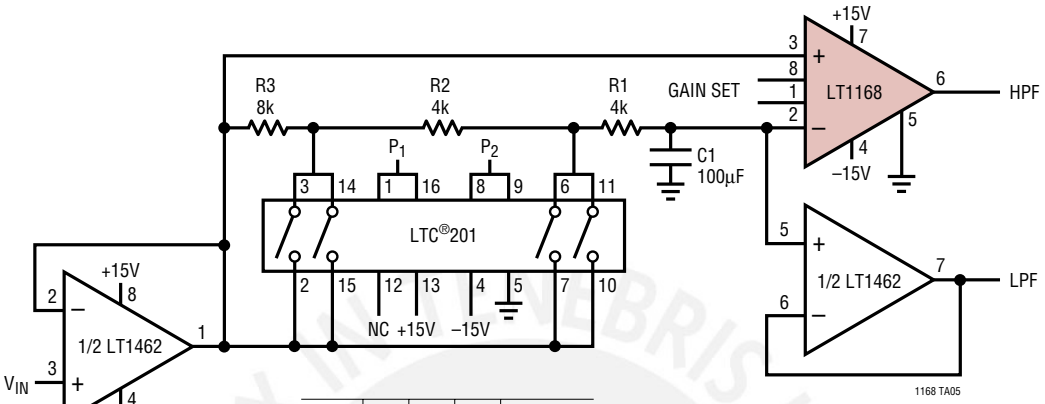
S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN INCHES / (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

TYPICAL APPLICATION

Low Power Programmable Audio HPF/LPF with "Pop-Less" Switching



P_1	—	0	1	0 < 0.8V
P_2	0	1	1	1 > 2.4V
POLE	100	200	400	Hz

TOTAL SUPPLY CURRENT < 400µA

RELATED PARTS

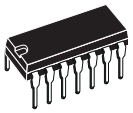
PART NUMBER	DESCRIPTION	COMMENTS
LTC1043	Dual Precision Instrumentation Building Block	Switched Capacitor, Rail-to-Rail Input, 120dB CMRR
LTC1100	Precision Chopper-Stabilized Instrumentation Amplifier	G = 10 or 100, V_{OS} = 10µV, I_B = 50pA
LT1101	Precision, Micropower, Single Supply Instrumentation Amplifier	G = 10 or 100, I_S = 105µA
LT1102	High Speed, JFET Instrumentation Amplifier	G = 10 or 100, Slew Rate = 30V/µs
LT1167	Single Resistor Programmable Precision Instrumentation Amplifier	Lower Noise than LT1168, $e_N = 7.5nV/\sqrt{Hz}$

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com
LT/LWI 0906 REV A • PRINTED IN USA

TL064
TL064A - TL064B

LOW POWER J-FET QUAD OPERATIONAL AMPLIFIERS

- VERY LOW POWER CONSUMPTION : 200µA
- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGES
- LOW INPUT BIAS AND OFFSET CURRENTS
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 3.5V/µs



N
DIP14
(Plastic Package)

D
SO14
(Plastic Micropackage)

DESCRIPTION

The TL064, TL064A and TL064B are high speed J-FET input quad operational amplifiers. Each of these J-FET input operational amplifiers incorporates well matched, high voltage J-FET and bipolar transistors in a monolithic integrated circuit.

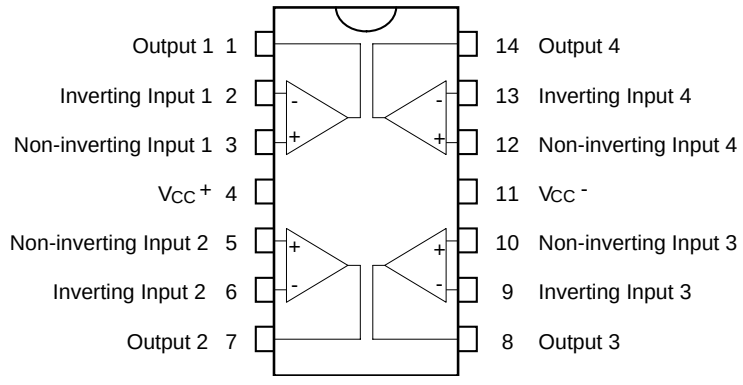
The device features high slew rate, low input bias and offset currents, and low offset voltage temperature coefficient.

ORDER CODE

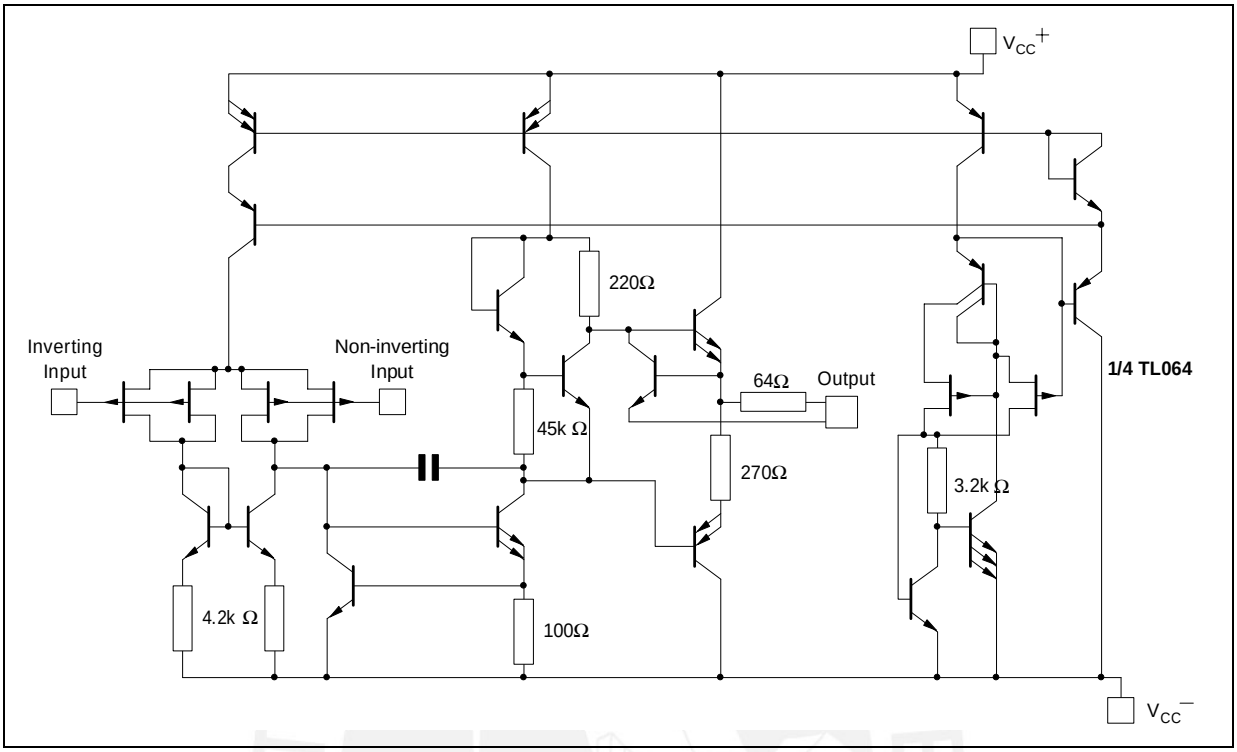
Part Number	Temperature Range	Package	
		N	D
TL064M/AM/BM	-55°C, +125°C	•	•
TL064I/AI/BI	-40°C, +105°C	•	•
TL064C/AC/BC	0°C, +70°C	•	•
Example : TL064IN			

N = Dual in Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)

PIN CONNECTIONS (top view)



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	TL064M, AM, BM	TL064I, AI, BI	TL064C, AC, BC	Unit
V_{CC}	Supply voltage - note 1)	±18			V
V_i	Input Voltage - note 2)	±15			V
V_{id}	Differential Input Voltage - note 3)	±30			V
P_{tot}	Power Dissipation	680			mW
	Output Short-circuit Duration - note 4)	Infinite			
T_{oper}	Operating Free-air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to +150			°C

1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
3. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	TL064M			TL064I			TL064C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage (R_S = 50Ω) T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$		3	6 15		3	6 9		3	15 20	mV
DV_{io}	Temperature Coefficient of Input Offset Voltage (R_S = 50Ω)		10			10			10		µV/°C
I_{io}	Input Offset Current - note 1) T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$		5	100 20		5	100 10		5	200 5	pA nA
I_{ib}	Input Bias Current - note 1 T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$		30	200 50		30	200 20		30	400 10	pA nA
V_{icm}	Input Common Mode Voltage Range	±11.5	+15 -12		±11.5	+15 -12		±11	+15 -12		V
V_{opp}	Output Voltage Swing (R_L = 10kΩ) T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$	20 20	27		20 20	27		20 20	27		V
A_{vd}	Large Signal Voltage Gain R_L = 10kΩ, V_o = ±10V, T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$	4 4	6		4 4	6		3 3	6		V/mV
GBP	Gain Bandwith Product T_{amb} = 25°C, R_L =10kΩ, C_L = 100pF		1			1			1		MHz
R_i	Input Resistance		10^{12}			10^{12}			10^{12}		Ω
CMR	Common Mode Rejection Ratio R_S = 50Ω	80	86		80	86		70	76		dB
SVR	Supply Voltage Rejection Ratio R_S = 50Ω	80	95		80	95		70	95		dB
I_{CC}	Supply Current, Per Amplifier T_{amb} = 25°C, no load, no signal		200	250		200	250		200	250	µA
V_{o1}/V_{o2}	Channel Separation A_V = 100, T_{amb} = 25°C		120			120			120		dB
P_D	Total Power Consumption T_{amb} = 25°C, no load, no signal		6	7.5		6	7.5		6	7.5	mW
SR	Slew Rate V_i = 10V, R_L = 10kΩ, C_L = 100pF, A_V = 1	1.5	3.5		1.5	3.5		1.5	3.5		V/µs
t_r	Rise Time 5 (see figure 1) V_i = 20mV, R_L = 10kΩ, C_L = 100pF, A_V = 1		0.2			0.2			0.2		µs
K_{ov}	Overshoot Factor (see figure 1) V_i = 20mV, R_L = 10kΩ, C_L = 100pF, A_V = 1 (see figure 1)		10			10			10		%
e_n	Equivalent Input Noise Voltage R_S = 100Ω, f = 1KHz		42			42			42		$\frac{nV}{\sqrt{Hz}}$

1. The input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

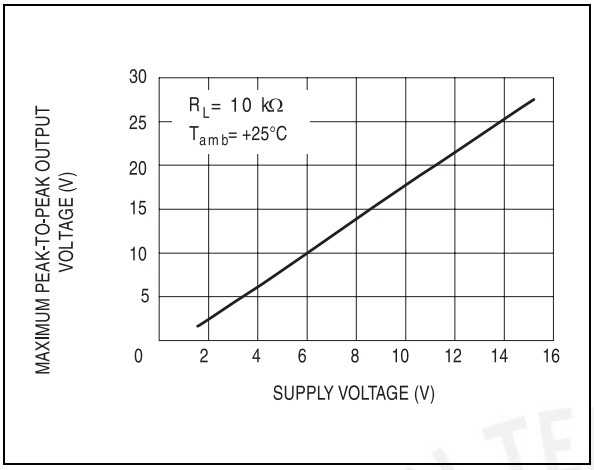
ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_{amb} = +25°C (unless otherwise specified)

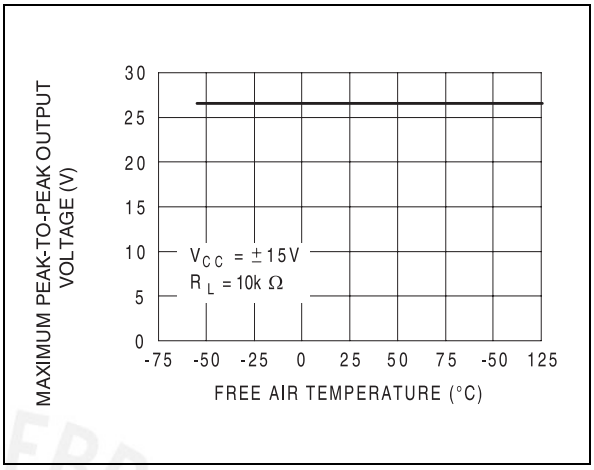
Symbol	Parameter	TL064AC, AI, AM			TL064BC, BI, BM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage (R_s = 50Ω) T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$		3	6 7.5		2	3 5	mV
DV_{io}	Temperature Coefficient of Input Offset Voltage (R_s = 50Ω)		10			10		µV/°C
I_{io}	Input Offset Current - note 1) T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$		5	100 3		5	100 3	pA nA
I_{ib}	Input Bias Current - note 1 T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$		30	200 7		30	200 7	pA nA
V_{icm}	Input Common Mode Voltage Range	±11.5	+15 -12		±11.5	+15 -12		V
V_{opp}	Output Voltage Swing (R_L = 10kΩ) T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$	20 20	27		20 20	27		V
A_{vd}	Large Signal Voltage Gain R_L = 10kΩ, V_o = ±10V, T_{amb} = 25°C $T_{min} \le T_{amb} \le T_{max}$	4 4	6		4 4	6		V/mV
GBP	Gain Bandwidth Product T_{amb} = 25°C, R_L =10kΩ, C_L = 100pF		1			1		MHz
R_i	Input Resistance		10^{12}			10^{12}		Ω
CMR	Common Mode Rejection Ratio R_S = 50Ω	80	86		80	86		dB
SVR	Supply Voltage Rejection Ratio R_S = 50Ω	80	95		80	95		dB
I_{CC}	Supply Current (Per Amplifier) T_{amb} = +25°C, no load, no signal		200	250		200	250	µA
V_{o1}/V_{o2}	Channel Separation A_v = 100, T_{amb} = +25°C		120			120		dB
P_D	Total Power Consumption (Each Amplifier) T_{amb} = 25°C, no load, no signal		6	7.5		6	7.5	mW
SR	Slew Rate V_i = 10V, R_L = 10kΩ, C_L = 100pF, A_v = 1	1.5	3.5		1.5	3.5		V/µs
t_r	Rise Time V_i = 20mV, R_L = 10kΩ, C_L = 100pF, A_v = 1		0.2			0.2		µs
K_{ov}	Overshoot Factor (see figure 1) V_i = 20mV, R_L = 10kΩ, C_L = 100pF, A_v = 1		10			10		%
e_n	Equivalent Input Noise Voltage R_S = 100Ω, f = 1KHz		42			42		$\frac{nV}{\sqrt{Hz}}$

1. The input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

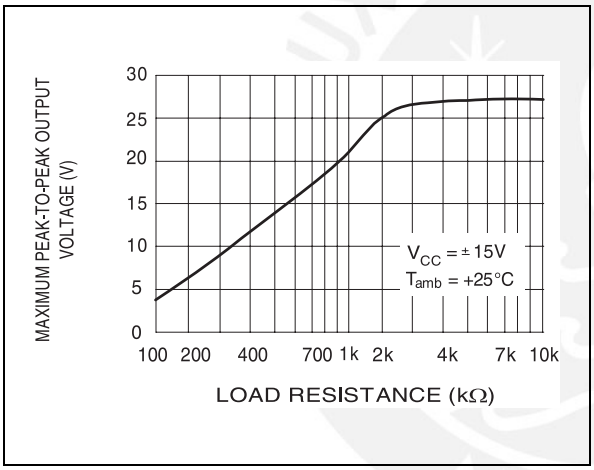
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus SUPPLY VOLTAGE



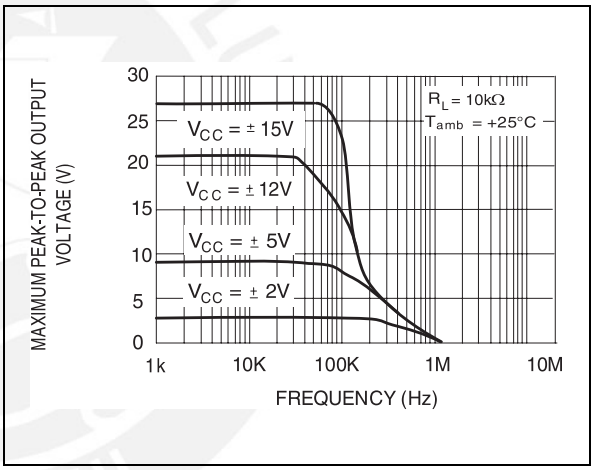
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus FREE AIR TEMPERATURE



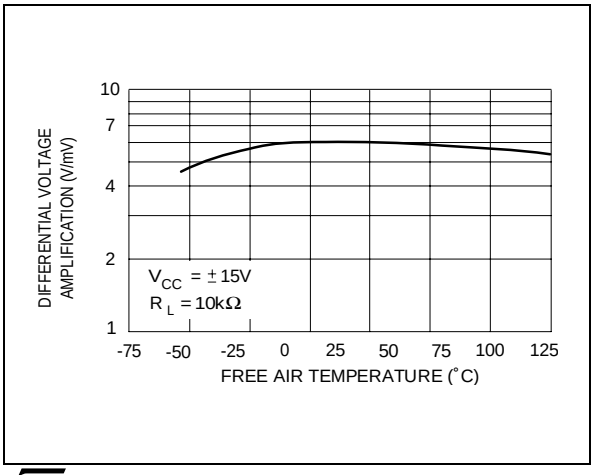
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus LOAD RESISTANCE



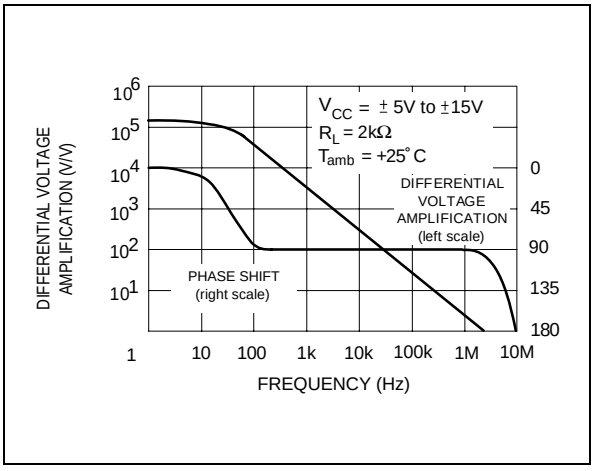
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus FREQUENCY



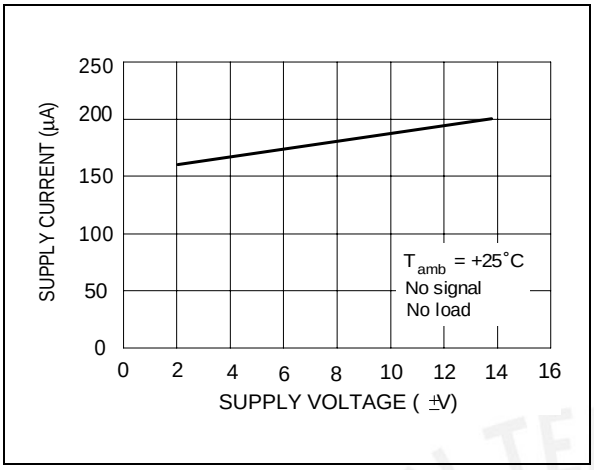
DIFFERENTIAL VOLTAGE AMPLIFICATION versus FREE AIR TEMPERATURE



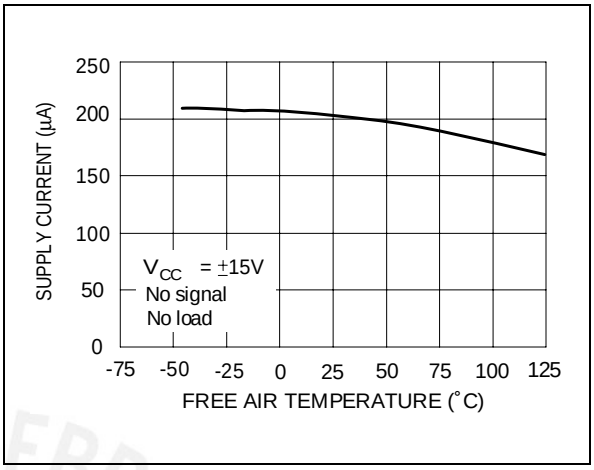
LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT versus FREQUENCY



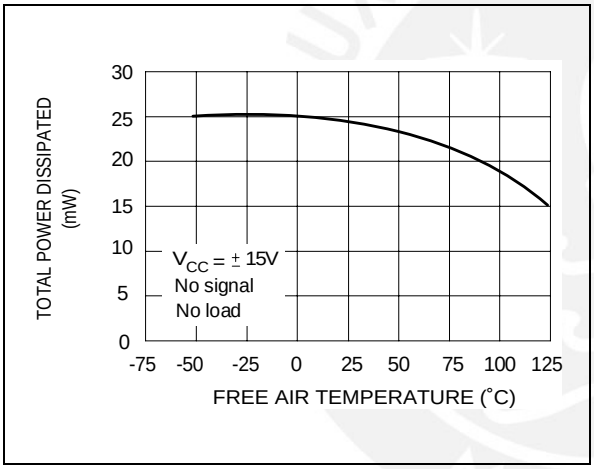
SUPPLY CURRENT PER AMPLIFIER versus SUPPLY VOLTAGE



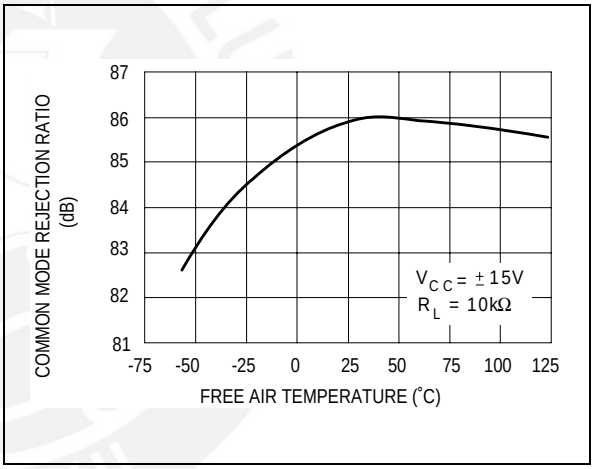
SUPPLY CURRENT PER AMPLIFIER versus FREE AIR TEMPERATURE



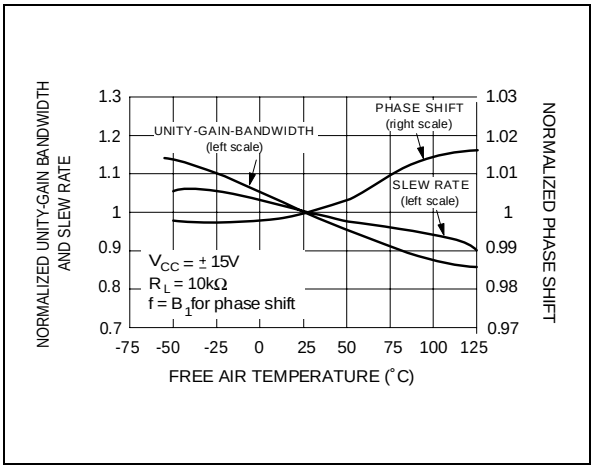
TOTAL POWER DISSIPATED versus FREE AIR TEMPERATURE



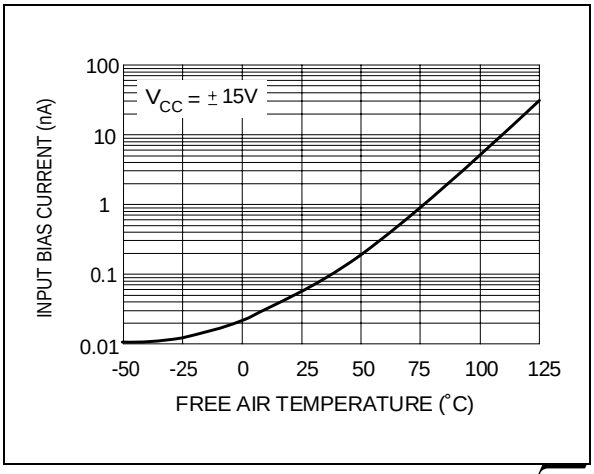
COMMON MODE REJECTION RATIO versus FREE AIR TEMPERATURE



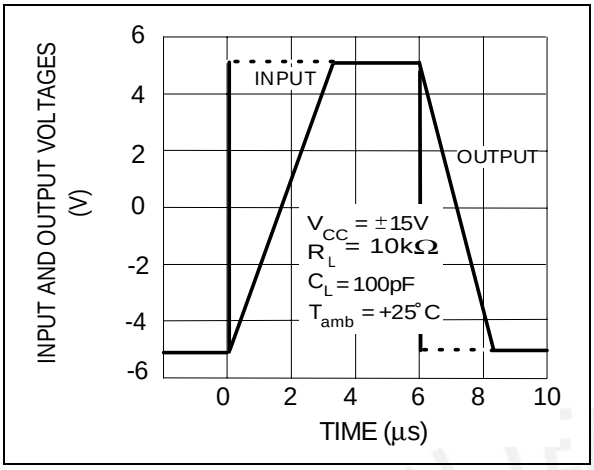
NORMALIZED UNITY GAIN BANDWIDTH SLEW RATE, AND PHASE SHIFT versus TEMPERATURE



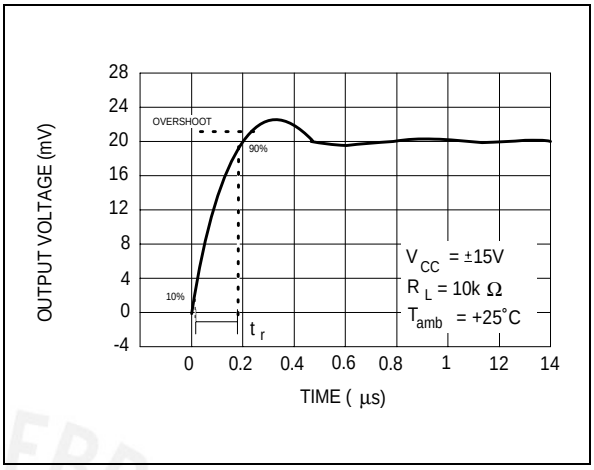
INPUT BIAS CURRENT versus FREE AIR TEMPERATURE



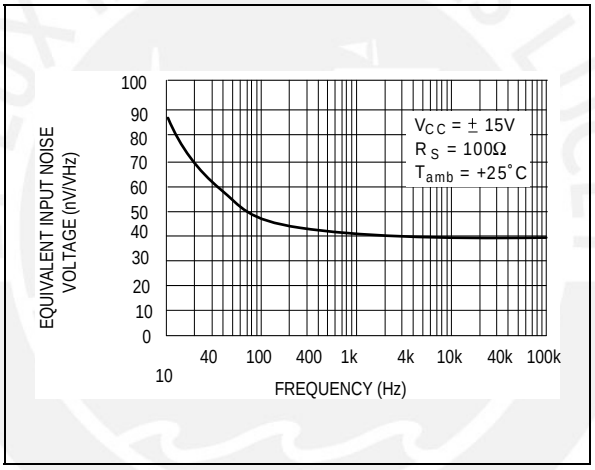
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



OUTPUT VOLTAGE versus ELAPSED TIME



EQUIVALENT INPUT NOISE VOLTAGE versus FREQUENCY



PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower

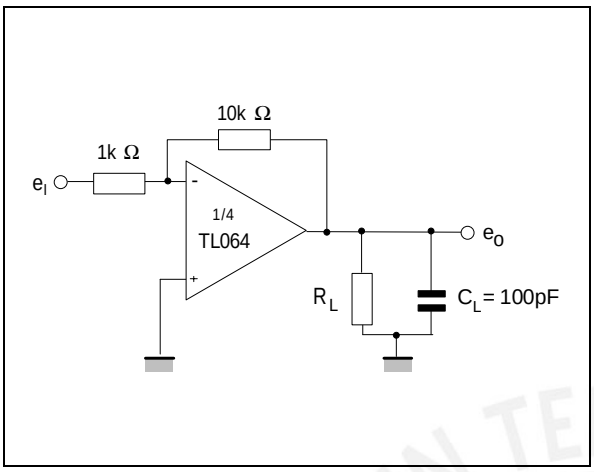
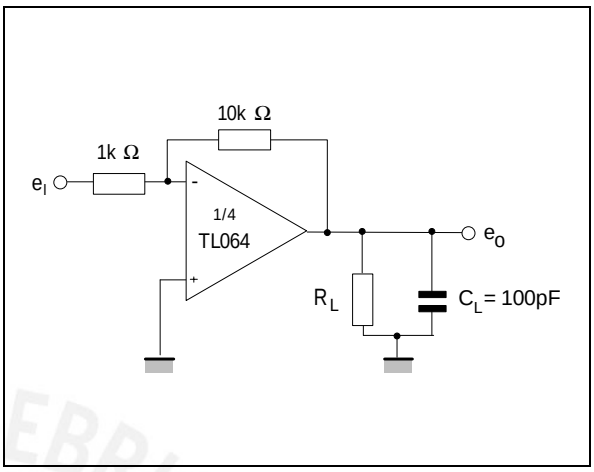
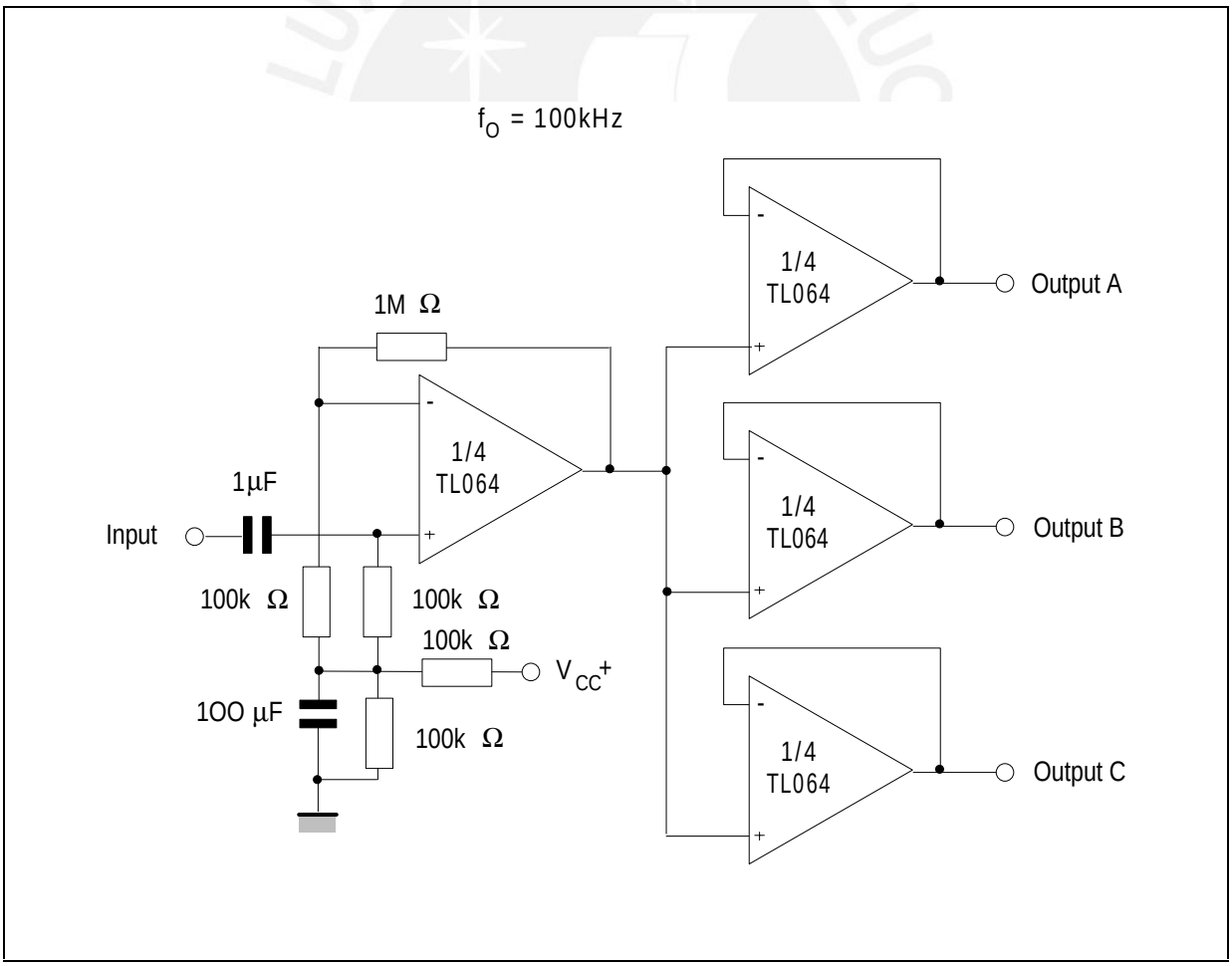


Figure 2 : Gain-of-10 Inverting Amplifier

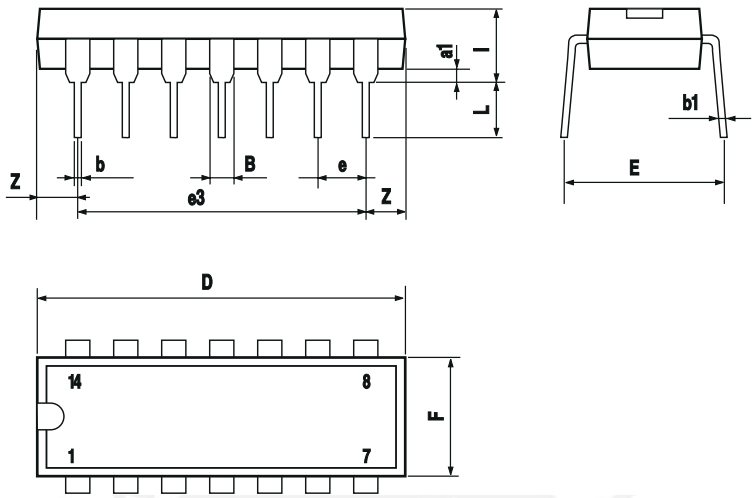


TYPICAL APPLICATIONS

AUDIO DISTRIBUTOR AMPLIFIER



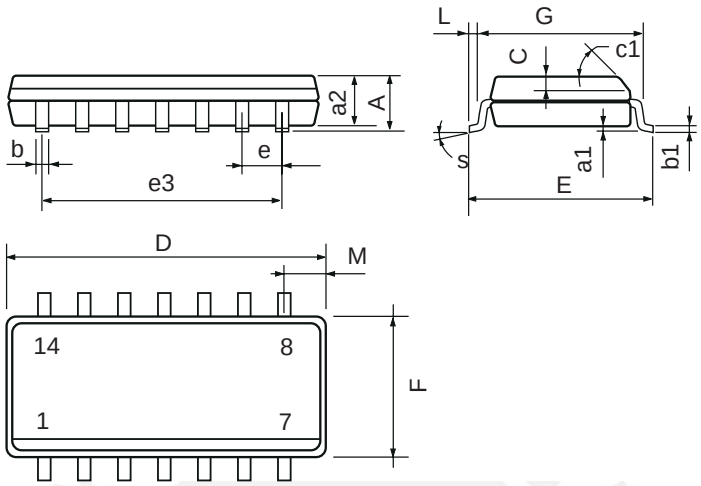
PACKAGE MECHANICAL DATA
14 PINS - PLASTIC DIP



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

PACKAGE MECHANICAL DATA

14 PINS - PLASTIC MICROPACKAGE (SO)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D (1)	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F (1)	3.8		4.0	0.150		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.020		0.050
M			0.68			0.027
S	8° (max.)					

Note : (1) D and F do not include mold flash or protrusions - Mold flash or protrusions shall not exceed 0.15mm (.066 inc) ONLY FOR DATA BOOK.

```
%% Apertura del serie (COM)

%borrar previos
delete(instrfind({'Port'},{'COM4'}));
%crear objeto serie
s=serial('COM4');
set(s,'Baudrate',9600); % se configura la velocidad a 9600 Baudios
set(s,'StopBits',1); % se configura bit de parada a uno
set(s,'DataBits',8); % se configura que el dato es de 8 bits, debe estar
entre 5 y 8
set(s,'Parity','odd'); % se configura sin paridad
set(s,'Terminator','CR/LF');% "c" caracter con que finaliza el envío
warning('off','MATLAB:serial:fscanf:unsuccessfulRead');
%abrir puerto
fopen(s);

%% Preparar medida

% parámetros de medidas
tmax = 10; % tiempo de captura en s
rate = 79; % resultado experimental
% preparar la figura
f = figure('Name','Captura');
a = axes('XLim',[0 tmax],'YLim',[0 5.1]);
l1 = line(nan,nan,'Color','r','LineWidth',2);

xlabel('Tiempo (s)')
ylabel('Voltaje (V)')
title('Captura de señal EMG')
grid on
hold on

%% Bucle
% inicializar
v1 = zeros(1,tmax*rate);
i = 1;
t = 0;

% ejecutar bucle cronometrado
tic
while t<tmax
    t = toc;
    % leer del puerto serie
    a = fscanf(s,'%d')';
    v1(i)=a(1)*5/256;
    % dibujar en la figura
    x = linspace(0,i/rate,i);
    set(l1,'YData',v1(1:i),'XData',x);
    drawnow
    % seguir
    i = i+1;
end
% resultado del cronometro
clc;
fprintf('%g s de captura a %g cap/s \n',t,i/t);
```

```
%%

fclose(s);
delete(s);
clear s;
```

```
% Apertura del serie (COM)

%borrar previos
delete(instrfind({'Port'},{'COM4'}));
%crear objeto serie
s=serial('COM4');
set(s,'Baudrate',9600); % se configura la velocidad a 9600 Baudios
set(s,'StopBits',1); % se configura bit de parada a uno
set(s,'DataBits',8); % se configura que el dato es de 8 bits, debe estar
entre 5 y 8
set(s,'Parity','odd'); % se configura sin paridad
set(s,'Terminator','CR/LF');% "c" caracter con que finaliza el envío
warning('off','MATLAB:serial:fscanf:unsuccessfulRead');
%abrir puerto
fopen(s);

%% Preparar medida

% parámetros de medidas
tmax = 10; % tiempo de captura en s
rate = 55; % resultado experimental

% preparar la figura
f1 = figure('Name','Captura');
a = axes('XLim',[0 tmax],'YLim',[0 5.1]);
l1 = line(nan,nan,'Color','r','LineWidth',2);
xlabel('Tiempo (s)')
ylabel('Voltaje (V)')
grid on
hold on

f2 = figure('Name','Captura');
b = axes('XLim',[0 tmax],'YLim',[0 5.1]);
l2 = line(nan,nan,'Color','b','LineWidth',2);
xlabel('Tiempo (s)')
ylabel('Voltaje (V)')
title('Captura de la señal de EMG')
grid on
hold on

%% Bucle
% inicializar
v1 = zeros(1,tmax*rate);
v2 = zeros(1,tmax*rate);
i = 1;
t = 0;

% ejecutar bucle cronometrado
tic
while t<tmax
    t = toc;
    % leer del puerto serie
    a = fscanf(s,'%d,%d')';
    v1(i)=a(1)*5/256;
    v2(i)=a(2)*5/256;
    % dibujar en la figura
```

```
    x = linspace(0,i/rate,i);
    set(l1,'YData',v1(1:i),'XData',x);
    set(l2,'YData',v2(1:i),'XData',x);
    drawnow
    % seguir
    i = i+1;
end
% resultado del cronometro
clc;
fprintf('%g s de captura a %g cap/s \n',t,i/t);


%%

fclose(s);
delete(s);
clear s;
```

```
; ****************************************************
; BASIC .ASM template file for AVR
; ****************************************************

.include "C:\VMLAB\include\m8def.inc"


; Define here Reset and interrupt vectors, if any
;
.def    dato=r18
.def    canal=r17
.cseg
        .org 0
reset:
  rjmp start

;************************************************
;************PROGRAMA PRINCIPAL*******************
;************************************************
start:

ldi     R16,high(RAMEND)    ;Valor inicial del puntero de pila
out     SPH,R16
ldi     R16,low(RAMEND)
out     SPL,R16

ldi     r16, $FF
out     ddrb, r16
ldi     r16,0
out     portb, r16
rcall   Configura_ADC
rcall Configura_USART
ldi     canal, 0

Empezar_conversion:
; Bit6 = ADSC, Start Conversion
        cpi     canal,0
        breq    analog_0
        cpi     canal,1
        breq    analog_1
        cpi     canal,2
        breq    analog_2
```

```
        cpi     canal,3
        breq    analog_3
        cpi     canal,4
        breq    analog_4
        cpi     canal,5
        breq    analog_5

analog_0:
        cbi     ADMUX, 0        ;se elige canal 0
        cbi     ADMUX, 1
        cbi     ADMUX, 2
        sbi     ADCSR, 6
Esperar_final0:
        sbic    ADCSR, 6
        rjmp    Esperar_final0
        in              dato, ADCH    ;solo ADCH xq res = 8 bits
        rcall   usart
  inc   canal
        rjmp    Empezar_conversion

analog_1:
        sbi     ADMUX, 0        ;se elige canal 1
        cbi     ADMUX, 1
        cbi     ADMUX, 2
        sbi     ADCSR, 6
Esperar_final1:
        sbic    ADCSR, 6
        rjmp    Esperar_final1
        in              dato, ADCH    ;solo ADCH xq res = 8 bits
        rcall   usart
        inc     canal
        rjmp    Empezar_conversion

        analog_2:
        cbi     ADMUX, 0        ;se elige canal 2
        sbi     ADMUX, 1
        cbi     ADMUX, 2
        sbi     ADCSR, 6
Esperar_final2:
        sbic    ADCSR, 6
        rjmp    Esperar_final2
        in              dato, ADCH    ;solo ADCH xq res = 8 bits
```

```
        rcall   usart
        inc     canal
        rjmp    Empezar_conversion

        analog_3:
        sbi     ADMUX, 0        ;se elige canal 3
        sbi     ADMUX, 1
        cbi     ADMUX, 0
        sbi     ADCSR, 6
Esperar_final3:
        sbic    ADCSR, 6
        rjmp    Esperar_final3
        in              dato, ADCH    ;solo ADCH xq res = 8 bits
        rcall   usart
        inc     canal
        rjmp    Empezar_conversion

        analog_4:
        cbi     ADMUX, 0        ;se elige canal 4
        cbi     ADMUX, 1
        sbi     ADMUX, 2
        sbi     ADCSR, 6
Esperar_final4:
        sbic    ADCSR, 6
        rjmp    Esperar_final4
        in              dato, ADCH    ;solo ADCH xq res = 8 bits
        rcall   usart
        inc     canal
        rjmp    Empezar_conversion

        analog_5:
        sbi     ADMUX, 0        ;se elige canal 5
        cbi     ADMUX, 1
        sbi     ADMUX, 2
        sbi     ADCSR, 6
Esperar_final5:
        sbic    ADCSR, 6
        rjmp    Esperar_final5
        in              dato, ADCH    ;solo ADCH xq res = 8 bits
        rcall   usart
        ldi     canal, 0
        rjmp    Empezar_conversion
```

```
;*****************************************************
;*****************************************************
;*************COnfigura ADC*****************************
;*****************************************************
Configura_ADC:
push r16

; PC: entrada, pull-up off
ldi r16,$00
out DDRC, r16
;ldi r16,$00
;out PORTC, r16

; Ref = AVcc = Vcc, Left Adjust(n=8bits)
ldi r16, 0b01100000
out ADMUX, r16

;ADC enabled, ADCclk = 1/32 clk
ldi r16, 10000101
out ADCSR, r16

pop r16
ret

;*****************************************************
;*****************************************************
;*************COnfigura USART*************************
;*****************************************************
Configura_USART:
push r16

;U2X = 1 velocidad doble
ldi     r16, (0<<RXC | 0<<TXC | 1<<U2X | 0<<MPCM)
out     UCSRA, r16

;velocidad 9600, 16Mhz
ldi     r16, high($CF)
out     UBRRH, r16
ldi     r16, low($cF)
out     UBRRL, r16
```

```
;comunicacion asincrona, paridad impar, 1 bit de parada, 8 bits de datos
ldi     r16, (1<<URSEL | 0<<UMSEL | 1<<UPM1 | 1<<UPM0 | 0<<USBS | 1<<UCSZ1 | 1<<UCSZ0)
out     UCSRC, r16

;interrupciones inhabilitadas, TX y Rx habilitadas
ldi     r16, (0<<RXCIE | 0<<TXCIE | 0<<UDRIE | 1<<RXEN | 1<<TXEN | 0<<UCSZ2 | 0<<TXB8)
out     UCSRB, r16

pop     r16
ret


;*****************************************************
;*****************************************************
;************DELAY ******************************
;*****************************************************
delay:
        nop
        nop
        nop
        ldi r20, 0
        demora:
        inc r20
        cpi r20, 10
        brne demora
        nop
        nop
        nop
ret

;*****************************************************
;*****************************************************
;************USART ******************************
;*****************************************************

usart:

        EsperaTxLibre:
        sbis UCSRA, UDRE
        rjmp EsperaTxLibre
```

```
        out UDR, dato

ret
```