3.3A, 400V, 1.800 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17404.

Features

- 3.3A, 400V
- $r_{DS(ON)} = 1.800\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

Packaging

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BRAND</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRF720</td>
<td>TO-220AB</td>
<td>IRF720</td>
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</tbody>
</table>

NOTE: When ordering, use the entire part number.
## Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain to Source Voltage (Note 1)</td>
<td>VDS</td>
<td>ID = 250µA, VGS = 0V, (Figure 10)</td>
<td>400</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Continuous Drain Current</td>
<td>ID</td>
<td></td>
<td>3.3</td>
<td>A</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Pulsed Drain Current (Note 3)</td>
<td>IDM</td>
<td></td>
<td>13</td>
<td>A</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Gate to Source Voltage</td>
<td>VGS</td>
<td>±20</td>
<td></td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Power Dissipation</td>
<td>Pd</td>
<td></td>
<td>50</td>
<td>W</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Linear Derating Factor</td>
<td>EAS</td>
<td></td>
<td>190</td>
<td>mJ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating and Storage Temperature</td>
<td>Tj, Tstg</td>
<td>-55 to 150°C</td>
<td></td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Maximum Temperature for Soldering</td>
<td>TL</td>
<td></td>
<td>300</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package Body for 10s, See Techbrief 334</td>
<td>Tpkg</td>
<td></td>
<td>260</td>
<td>°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**CAUTION:** Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTE:**
1. \( T_J = 25°C \) to 125°C.

## Electrical Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain to Source On Resistance (Note 2)</td>
<td>Dso(on)</td>
<td>Id = 1.8A, VGS = 10V, (Figures 8, 9)</td>
<td>-</td>
<td>1.5</td>
<td>1.8</td>
<td>Ω</td>
</tr>
<tr>
<td>Forward Transconductance (Note 2)</td>
<td>( \alpha_{fs} )</td>
<td>VDS ≥ 10V, ID = 2.0A, (Figure 12)</td>
<td>1.7</td>
<td>2.7</td>
<td>S</td>
<td></td>
</tr>
<tr>
<td>Turn-On Delay Time</td>
<td>Id(on)</td>
<td>VDS = 200V, ID = 3.3A, RGS = 18Ω, VGS = 10V, RL = 50Ω, MOSFET Switching Times are Essentially Independent of Operating Temperature</td>
<td>-</td>
<td>10</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>Rise Time</td>
<td>Ir</td>
<td></td>
<td>-</td>
<td>14</td>
<td>21</td>
<td>ns</td>
</tr>
<tr>
<td>Turn-Off Delay Time</td>
<td>Id(off)</td>
<td></td>
<td>-</td>
<td>30</td>
<td>45</td>
<td>ns</td>
</tr>
<tr>
<td>Fall Time</td>
<td>If</td>
<td></td>
<td>-</td>
<td>13</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>Gate to Source Charge</td>
<td>Qgs</td>
<td>Gate Charge is Essentially Independent of Operating Temperature</td>
<td>-</td>
<td>2.0</td>
<td>-</td>
<td>nC</td>
</tr>
<tr>
<td>Gate to Drain “Miller” Charge</td>
<td>Qgd</td>
<td></td>
<td>-</td>
<td>6.0</td>
<td>-</td>
<td>nC</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>Ciss</td>
<td>VDS = 25V, VGS = 0V, f = 1MHz, (Figure 10)</td>
<td>-</td>
<td>360</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>Coss</td>
<td></td>
<td>-</td>
<td>55</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>Reverse Transfer Capacitance</td>
<td>Crss</td>
<td></td>
<td>-</td>
<td>20</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>Internal Drain Inductance</td>
<td>LD</td>
<td>Measured From the Contact Screw on Tab to Center of Die</td>
<td>-</td>
<td>3.5</td>
<td>-</td>
<td>nH</td>
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<tr>
<td>Internal Source Inductance</td>
<td>LS</td>
<td>Measured From the Source Lead, 6mm (0.25in) From Header to Source Bonding Pad</td>
<td>-</td>
<td>4.5</td>
<td>-</td>
<td>nH</td>
</tr>
<tr>
<td>Thermal Resistance, Junction to Case</td>
<td>Rinjc</td>
<td></td>
<td>-</td>
<td>2.5</td>
<td>-</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal Resistance, Junction to Ambient</td>
<td>Rinja</td>
<td>Free Air Operation</td>
<td>-</td>
<td>80</td>
<td>-</td>
<td>°C/W</td>
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## Source to Drain Diode Specifications

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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</thead>
<tbody>
<tr>
<td>Continuous Source to Drain Current</td>
<td>ISD</td>
<td>Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Rectifier</td>
<td>-</td>
<td>-</td>
<td>3.3</td>
<td>A</td>
</tr>
<tr>
<td>Pulse Source to Drain Current (Note 3)</td>
<td>ISDM</td>
<td></td>
<td>-</td>
<td>-</td>
<td>13</td>
<td>A</td>
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Source to Drain Diode Voltage (Note 2)  

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source to Drain Diode Voltage</td>
<td>VSD</td>
<td>TJ = 25°C, ISD = 3.3A, VGS = 0V, (Figure 13)</td>
<td>-</td>
<td>-</td>
<td>1.6</td>
<td>V</td>
</tr>
<tr>
<td>Reverse Recovery Time</td>
<td>trr</td>
<td>TJ = 25°C, ISD = 3.3A, dISD/dt = 100A/µs</td>
<td>120</td>
<td>-</td>
<td>600</td>
<td>ns</td>
</tr>
<tr>
<td>Reverse Recovery Charge</td>
<td>QRR</td>
<td>TJ = 25°C, ISD = 3.3A, dISD/dt = 100A/µs</td>
<td>0.64</td>
<td>-</td>
<td>3.0</td>
<td>µC</td>
</tr>
</tbody>
</table>

**NOTES:**

2. Pulse test: pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. VDD = 50V, starting TJ = 25°C, L = 31µH, RG = 25Ω, peak IAS = 3.3A.

### Typical Performance Curves  Unless Otherwise Specified

**FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE**

**FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE**

**FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE**

\[
Z_{J,C}(\text{TJ}) = P_{DM} \times t_1 + Z_{\text{th JC}} + T_C
\]

\[
\text{NOTES:}
\begin{align*}
D & = \frac{t_1}{t_2} \\
\text{DUTY FACTOR} & = D \\
\text{PEAK TJ} & = P_{DM} \times Z_{\text{th JC}} + T_C
\end{align*}
\]
Typical Performance Curves Unless Otherwise Specified (Continued)

**FIGURE 4. FORWARD BIAS SAFE OPERATING AREA**

- Operation in this area may be limited by $r_{DS(on)}$.
- $T_J = \text{MAX RATED}$
- $T_C = 25^\circ\text{C}$
- Single pulse

**FIGURE 5. OUTPUT CHARACTERISTICS**

- Pulse duration = 80 $\mu$s
- Duty cycle = 0.5% max

**FIGURE 6. SATURATION CHARACTERISTICS**

**FIGURE 7. TRANSFER CHARACTERISTICS**

**FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT**

**FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE**
Typical Performance Curves

FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE
Test Circuits and Waveforms

FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

FIGURE 17. SWITCHING TIME TEST CIRCUIT

FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

FIGURE 19. GATE CHARGE TEST CIRCUIT

FIGURE 20. GATE CHARGE WAVEFORMS
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- FRFET™
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- GTO™
- HiSeC™
- ISOLPLANAR™
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- PACMAN™
- POP™
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<th>Definition</th>
</tr>
</thead>
<tbody>
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<td>This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.</td>
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